15V, 4A Step-Up µModule Regulator

FEATURES

- **Complete Solution in <1cm² (Single-Sided PCB) or 0.5cm² (Dual-Sided PCB)**
- **Input Voltage Range: 1.8V to 5.5V, Down to 0.7V After Start-Up**
- **Output Voltage Range: 2.5V to 15V**
- **4A Switch Current**
- **Dual Phase Operation**
- **±3% Maximum Total DC Output Voltage Regulation Over Load, Line and Temperature**
- **Output Disconnect in Shut Down**
- Inrush Current Limit
- External Frequency Synchronization
- Selectable Burst Mode® Operation
- Output Overvoltage and Overtemperature Protection
- 6.25mm × 6.25mm × 2.42mm BGA package

APPLICATIONS

- RF Microwave Power Amplifiers
- Battery Powered DC Motors
- 3.3V Bus Telecom Transceivers

DESCRIPTION

The LTM®4661 is a synchronous step-up switching mode µModule® (power module) regulator in a 6.25mm × 6.25mm × 2.42mm BGA package. Included in the package are the switching controller, power FETs, inductor and all support components. Operating over an input voltage of 1.8V to 5.5V, down to 0.7V after start-up, the LTM4661 regulates an output voltage of 2.5V to 15V set by an external resistor. It provides up to 4A switch current. Only bulk input and output capacitors are needed.

The LTM4661 1MHz switching frequency and dual phase single output architecture enable fast transient response to line and load changes and a significant reduction of output ripple voltage. It supports frequency synchronization, PolyPhase® operation and selectable Burst Mode operation.

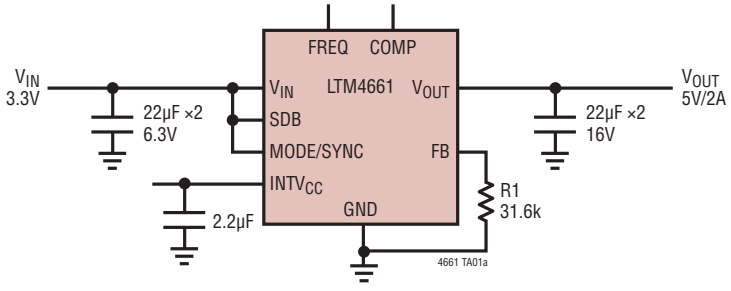
The LTM4661 features a true output disconnect during shutdown and inrush current limit at start-up. It also has short-circuit, overvoltage and overtemperature protection.

The LTM4661 is Pb-free and RoHS compliant.

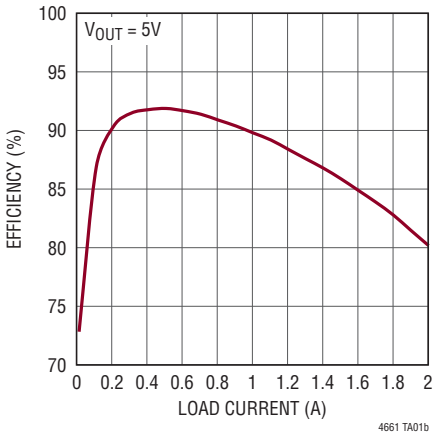
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TYPICAL APPLICATION

5V/2A DC/DC Step-Up µModule Regulator



Efficiency vs Output Current at 3.3V Input



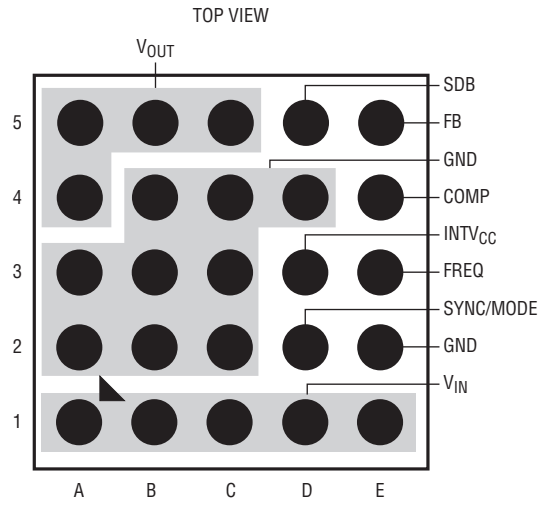
ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN} ..... –0.3V to 6V
V_{OUT} ..... –0.3V to 18V
COMP, FREQ ..... –0.3V to $INTV_{CC}$
SYNC/MODE, SDB ..... –0.3V to 6V
Operating Internal Temperature Range
(Note 2) ..... –40°C to 125°C
Storage Temperature Range ..... –55°C to 125°C
Peak Solder Reflow Body Temperature ..... 250°C

PIN CONFIGURATION

(See Pin Functions, Pin Configuration Table)



BGA PACKAGE
25-Lead (6.25mm × 6.25mm × 2.42mm)
T_{JMAX} = 125°C, θ_{JCtop} = 17°C/W, $\theta_{JCbottom}$ = 11°C/W,
$\theta_{JB} + \theta_{BA}$ = 22°C/W, θ_{JA} = 22°C/W
WEIGHT = 0.25g

ORDER INFORMATION

PART NUMBER	PAD OR BALL FINISH	PART MARKING*		PACKAGE TYPE	MSL RATING	TEMPERATURE RANGE (Note 2)
		DEVICE	FINISH CODE			
LTM4661EY#PBF	SAC305 (RoHS)	LTM4661Y	e1	BGA	4	–40°C to 125°C
LTM4661IY#PBF	SAC305 (RoHS)	LTM4661Y	e1	BGA	4	–40°C to 125°C
LTM4661IY	SnPb (63/37)	LTM4661Y	e0	BGA	4	–40°C to 125°C

- Contact the factory for parts specified with wider operating temperature ranges. *Pad or ball finish code is per IPC/JEDEC J-STD-609.
- Recommended LGA and BGA PCB Assembly and Manufacturing Procedures
- LGA and BGA Package and Tray Drawings

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified internal operating temperature range, otherwise specifications are at T_A = 25°C (Note 2), V_{IN} = 3.3V, per the typical application.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Switching Regulator Section: per Channel							
V_{IN}	Input DC Voltage	$V_{OUT} \geq 2.5V$	●	0.7		5.5	V
$V_{IN(MIN)}$	Minimum Start-Up Voltage	V_{OUT} = 0V	●		1.6	1.8	
$V_{OUT(RANGE)}$	Output Voltage Range		●	2.5		15	V
$V_{OUT(DC)}$	Output Voltage, Total Variation with Line and Load	R_{FB} = 31.6k, SYNC/MODE = $INTV_{CC}$ V_{IN} = 3.3V, V_{OUT} = 5V, I_{OUT} = 0A to 2A	●	4.85	5	5.15	V
$I_{Q(VIN)}$	Input Supply Bias Current	V_{IN} = 3.3V, V_{OUT} = 5V, SYNC/MODE = $INTV_{CC}$, I_{OUT} = 5mA V_{IN} = 3.3V, V_{OUT} = 5V, SYNC/MODE = GND, I_{OUT} = 5mA Shutdown, SDB = 0, V_{IN} = 3.3V			10 8.5 0.5		mA mA µA
$I_{S(VIN)}$	Input Supply Current	V_{IN} = 3.3V, V_{OUT} = 5V, I_{OUT} = 2A			3.7		A
$I_{OUT(DC)}$	Output Continuous Current Range	V_{IN} = 3.3V, V_{OUT} = 5V (Note 3) V_{IN} = 3.3V, V_{OUT} = 12V		0 0		2 0.7	A A
ΔV_{OUT} (Line)/V_{OUT}	Line Regulation Accuracy	V_{OUT} = 12V, V_{IN} = 1.8V to 5.5V, I_{OUT} = 0A	●		0.1	0.5	%/V
ΔV_{OUT} (Load)/V_{OUT}	Load Regulation Accuracy	V_{IN} = 3.3V, V_{OUT} = 5V, I_{OUT} = 0A to 2A	●		0.1	2	%
$V_{OUT(AC)}$	Output Ripple Voltage	I_{OUT} = 0A, C_{OUT} = 2×22µF Ceramic V_{IN} = 3.3V, V_{OUT} = 5V			3		mV
$\Delta V_{OUT(START)}$	Turn-On Overshoot	I_{OUT} = 0A, C_{OUT} = 2×22µF Ceramic, V_{IN} = 3.3V, V_{OUT} = 5V			30		mV
t_{START}	Turn-On Time	C_{OUT} = 2×22µF Ceramic, No Load, V_{IN} = 3.3V, V_{OUT} = 5V			10		ms
ΔV_{OUTLS}	Peak Deviation for Dynamic Load	Load: 0% to 25% to 0% of Full Load C_{OUT} = 2×22µF Ceramic, V_{IN} = 3.3V, V_{OUT} = 5V			200		mV
t_{SETTLE}	Settling Time for Dynamic Load Step	Load: 0% to 25% to 0% of Full Load C_{OUT} = 2×22µF Ceramic, V_{IN} = 3.3V, V_{OUT} = 5V			500		uS
V_{FB}	Voltage at V_{FB} Pin	I_{OUT} = 0A, V_{IN} = 3.3V, V_{OUT} = 5V, SYNC/MODE = $INTV_{CC}$	●	1.17	1.2	1.23	V
I_{FB}	Current at V_{FB} Pin	(Note 4)			1	50	nA
R_{FBHI}	Resistor Between V_{OUT} and V_{FB} Pins			99.5	100	100.5	kΩ
Duty(MIN)	Minimum Duty Cycle	FB = 1.4V (Note 4)				0	%
Duty(MAX)	Maximum Duty Cycle	FB = 1.0V (Note 4)		90	94		%
SDB Input Voltage		SDB Input High SDB Input Low			1.2 0.35		V V
I_{SDB}	SDB Input Current	SDB = 5.5V			1	2	µA
V_{INTVCC}	Internal V_{CC} Voltage	V_{IN} < 2.8V, V_{OUT} > 5V		3.9	4.25	4.6	V
f_{OSC}	Switching Frequency				1		MHz
SYNC Range	SYNC Frequency Range			0.5		1.5	MHz
SYNC/MODE		Sync Input High Voltage Sync Input Low Voltage			1.6 0.35		V V
$I_{SYNC/MODE}$		SYNC/MODE = 5.5V			1	2	µA

ELECTRICAL CHARACTERISTICS

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTM4661 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTM4661E is guaranteed to meet performance specifications over the 0°C to 125°C internal operating temperature range. Specifications over the full –40°C to 125°C internal operating temperature range are assured by design, characterization and correlation with statistical process controls. The LTM4661I is guaranteed to meet specifications over the full –40°C to 125°C internal operating temperature range. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance and other environmental factors.

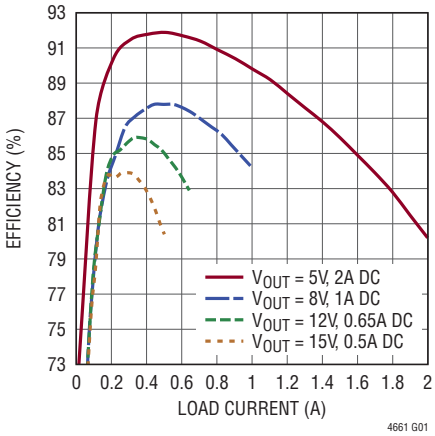
Note 3: See output current derating curves for different V_{IN}, V_{OUT} and T_A.

Note 4: 100% tested at wafer level.

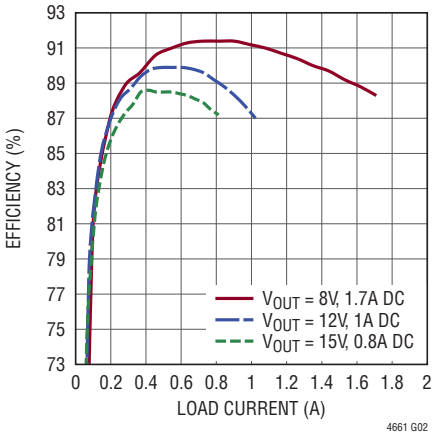
Note 5: The LTM4661 includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 170°C when overtemperature shutdown is active. Continuous operation above the specified maximum operation junction temperature may result in device degradation or failure.

TYPICAL PERFORMANCE CHARACTERISTICS

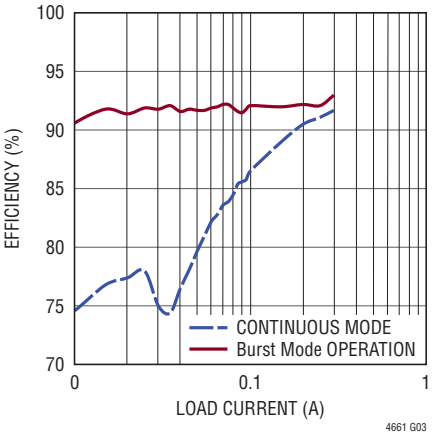
Efficiency vs Output Current, V_{IN} = 3.3V



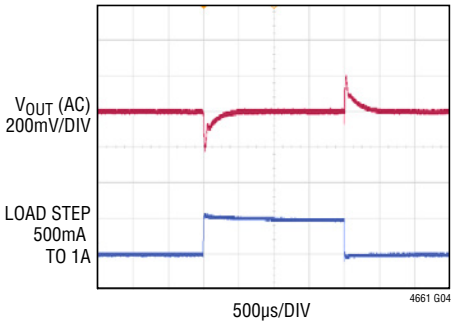
Efficiency vs Output Current, V_{IN} = 5V



Burst vs Continuous Mode Efficiency, V_{IN} = 3.3V

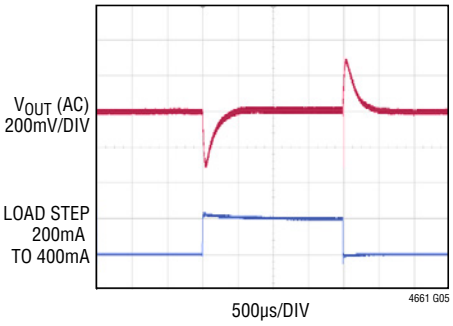


5V Output Load Transient Response



V_{IN} = 3.3V, V_{OUT} = 5V
f_S = 1MHz (DEFAULT)
500mA TO 1A LOAD STEP
C_{OUT} = 2×22µF CERAMIC

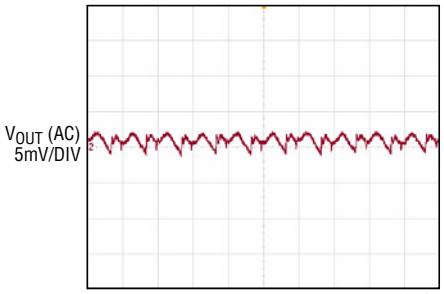
12V Output Load Transient Response



V_{IN} = 3.3V, V_{OUT} = 12V
f_S = 1MHz (DEFAULT)
200mA TO 400mA LOAD STEP
C_{OUT} = 2×22µF CERAMIC

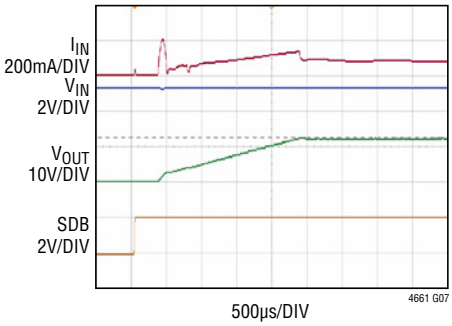
TYPICAL PERFORMANCE CHARACTERISTICS

Steady State Output Ripple



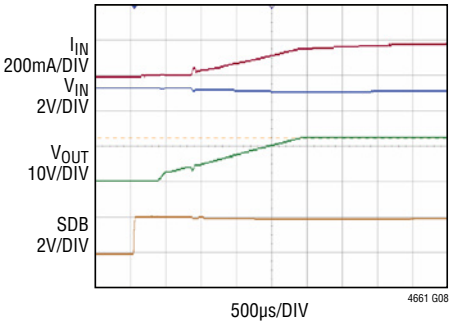
V_{IN} = 3.3V,
V_{OUT} = 5V
f_S = 1MHz (DEFAULT)
C_{OUT} = 2×22µF CERAMIC

Start-Up Waveform with No Load Applied



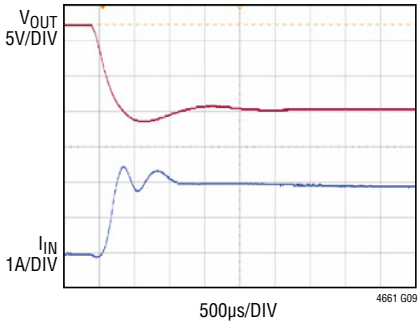
V_{IN} = 3.3V,
V_{OUT} = 12V
f_S = 1MHz (DEFAULT)
C_{OUT} = 2×22µF CERAMIC

Start-Up Waveform with 0.5A Load Applied



V_{IN} = 3.3V,
V_{OUT} = 12V
f_S = 1MHz (DEFAULT)
C_{OUT} = 2×22µF CERAMIC

Short-Circuit Response



V_{IN} = 3.3V,
V_{OUT} = 12V
f_S = 1MHz (DEFAULT)
C_{OUT} = 2×22µF CERAMIC

PIN FUNCTIONS

V_{IN} (A1, B1, C1, D1, E1): Power Input Pins. Apply input voltage between these pins and GND pins. Recommend placing input decoupling capacitance directly between V_{IN} pins and GND pins.

V_{OUT} (A4, A5, B5, C5): Power Output Pins of the Switching Mode Regulator. Apply output load between these pins and GND pins. Recommend placing output decoupling capacitance directly between these pins and GND pins.

GND (A2, A3, B2 to B4, C2 to C4, D4, E2): Power Ground Pins for Both Input and Output Returns.

SYNC/MODE (D2): Burst Mode Operation Selection Pin and External Synchronization Input to Phase Detector Pin. Connect this pin to $INTV_{CC}$ to operate the module in forced continuous mode. Connect this pin to GND to enable Burst Mode operation. A clock more than 100ns on the pin will force the module operating in continuous mode and synchronized to the external clock applied to this pin. The external clock frequency must be higher than the self-running frequency programmed by FREQ pin. See frequency programming in the Applications Information section.

$INTV_{CC}$ (D3): Internal Regulator Output. The internal power drivers and control circuits are powered from this voltage. Decouple this pin to power ground with a minimum of 2.2µF low ESR ceramic capacitor. The $INTV_{CC}$ voltage is regulated at the lower of V_{IN} and 4.25V. When V_{IN} falls below 3V and V_{OUT} is higher than V_{IN}, $INTV_{CC}$ will regulate to the lower of approximately V_{OUT} and 4.25V. A UVLO event occurs if $INTV_{CC}$ drops below 1.5V, typical.

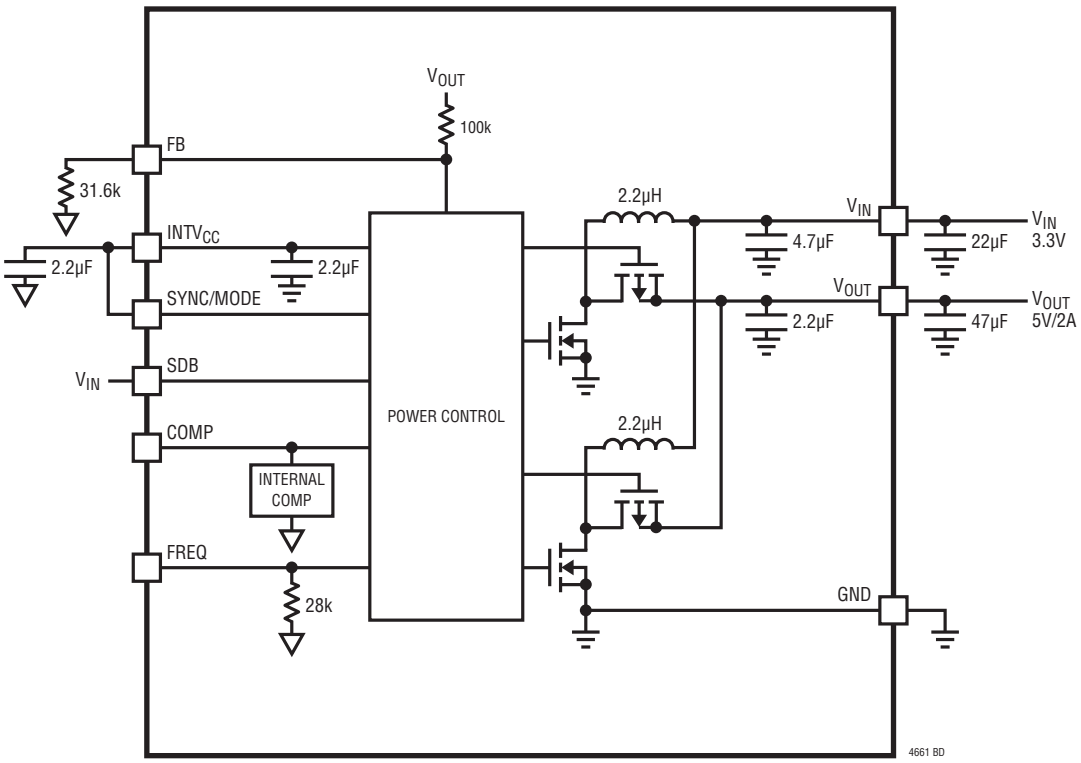
FREQ (E3): Frequency Set Internally to 1MHz. An external resistor can be placed from this pin to ground to increase frequency or from this pin to $INTV_{CC}$ to reduce frequency. See the Applications Information section for frequency adjustment.

SDB (D5): Shutdown Control Input of the µModule Regulator. Pulling this pin above 1.6V enables normal, free-running operation. Forcing this pin below 0.25V shuts the regulator off, with quiescent current below 1µA. Do not leave this pin floating.

COMP (E4): Current Control Threshold and Error Amplifier Compensation Point of the Switching Mode Regulator. Tie the COMP pins together for parallel operation. The device is internal compensated.

FB (E5): The Negative Input of the Error Amplifier for the Switching Mode Regulator. Internally, this pin is connected to V_{OUT} with a 100kΩ 0.5% precision resistor. Different output voltages can be programmed with an additional resistor between FB and GND pins. In PolyPhase operation, tying the FB pins together allows for parallel operation. See the Applications Information section for details.

BLOCK DIAGRAM



OPERATION

The LTM4661 is a dual-phase single-output standalone non-isolated step-up switching mode DC/DC power supply. This module provides a precisely regulated output voltage programmable via one external resistor from 1.2V to 15V and provides up to 4A switch current (see Table 1) with few external input and output ceramic capacitors. It also offers the unique ability to start up from inputs as low as 1.8V and continue to operate from inputs as low as 0.7V for output voltages greater than 2.5V. The typical application schematic is shown in Figure 17.

The LTM4661 contains an integrated fixed frequency, current mode regulator, power MOSFETs, inductor and other supporting discrete components. The default switching frequency is 1MHz. For switching noise-sensitive applications, the switching frequency can be adjusted by external resistors and the µModule regulator can be externally synchronized to a clock at least 100ns minimum.

With current mode control and internal feedback loop compensation, the LTM4661 module has sufficient stability margins and good transient performance with a wide range of output capacitors, even with all ceramic output capacitors.

Pulling the SDB pin above 1.6V enables module operation and forcing it below 0.25V shuts the module off with quiescent current below 1µA. At light load currents, Burst Mode operation can be enabled to achieve higher efficiency compared to continuous mode (CCM) by setting the SYNC/MODE pin to GND. An internal 10ms soft-start limits inrush current during start-up and simplifies the design process while minimizing the number of external components.

APPLICATIONS INFORMATION

The typical LTM4661 application circuit is shown in Figure 17. External component selection is primarily determined by the input voltage, the output voltage and the maximum load current.

Minimum Input Voltage

The LTM4661 is designed to allow start-up from input voltages as low as 1.8V. When V_{OUT} exceeds 2.5V, the LTM4661 continues to regulate its output, even when V_{IN} falls as low as 0.7V. This feature extends operating times by maximizing the amount of energy that can be extracted from the input source. The limiting factors for the application become the availability of the power source to supply sufficient power to the output at the low input voltage, and the maximum duty cycle, which is clamped at 94%.

In a step-up boost converter, the duty cycle can be calculated at:

$$D = 1 - \frac{V_{IN} \bullet \eta}{V_{OUT}}$$

where η is the converter efficiency. 85% is a good estimate to start with.

Note that at low input voltages, voltage drops due to series resistance become critical and greatly limit the power delivery capability of the converter.

Output Current Capability

The LTM4661 is designed to provide up to 4A switch current. Due to the nature of the boost converter, the actually output current capability depends highly on the input/output voltage ratio. The peak inductor current, same as switch current, in a boost converter can be calculated as:

$$I_{SW} = \frac{V_{IN} \bullet D}{2 \bullet f_S \bullet L} + \frac{I_{OUT}}{1 - D}$$

where D is the duty cycle showing above and f_S = 1MHz and L = 2.2µH/2 = 1.1µH.

Based on common input and output values, Table 1 lists different output current capability of the LTM4661 module.

Table 1. Output Current Capability vs Input Voltage

V_{IN} (V)	3.3				5		
V_{OUT} (V)	5	8	12	15	8	12	15
Output Current (A)	1.9	1	0.7	0.5	1.7	1	0.7
Efficiency (%)	82	84	83	81	88	87	88
Peak Switch Current (A)	4	3.8	3.9	4	3.94	4.1	4.1

Output Voltage Programming

The PWM controller has an internal 1.2V reference voltage. As shown in the Block Diagram, a 100k 0.5% internal feedback resistor connects V_{OUT} and FB pins together. Adding a resistor R_{FB} from FB pin to GND, programs the output voltage:

$$R_{FB} = \frac{1.2V}{V_{OUT} - 1.2V} \bullet 100k$$

Table 2. V_{FB} Resistor Value vs Various Output Voltages

V_{OUT} (V)	1.2	2.5	3.3	5	8	12	15
R_{FB} (k)	OPEN	93.1	57.6	31.6	17.8	11.0	8.66

For parallel operation of N-piece of LTM4661 modules, the following equation can be used to solve for R_{FB}:

$$R_{FB} = \frac{1.2V}{V_{OUT} - 1.2V} \bullet \frac{100k}{N}$$

Multiphase Operation

The LTM4661 uses a unique dual-phase single-output architecture, rather than the conventional single phase of other boost converters. By interleaving two phases equally spaced 180° apart, both input and output current ripple get significantly reduced as well as the amount of input and output decoupling capacitor required.

APPLICATIONS INFORMATION

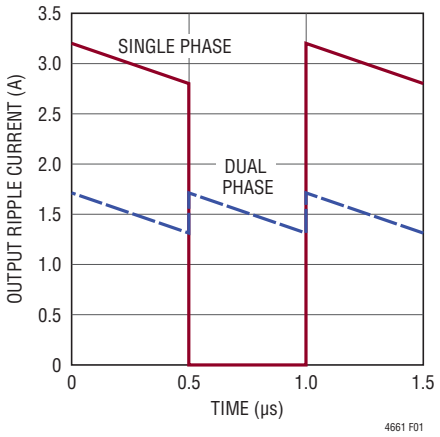


Figure 1. Comparison of Output Ripple Current with Single Phase and Dual Phase Boost Converter

Input Decoupling Capacitors

The LTM4661 module should be connected to a low AC-impedance DC source. For each module, one piece 10µF input ceramic capacitor is required for RMS ripple current decoupling. Bulk input capacitor is only needed when the input source impedance is compromised by long inductive leads, traces or not enough source capacitance. The bulk capacitor can be an electrolytic aluminum capacitor and polymer capacitor.

Output Decoupling Capacitors

With an optimized high frequency, high bandwidth, two phase interleaving design, only single piece of 22µF low ESR output ceramic capacitor is required for each LTM4661 module to achieve low output voltage ripple and very good transient response. Additional output filtering may be required by the system designer, if further reduction of output ripples or dynamic transient spikes is required. The LTpowerCAD® Design Tool is available to download online for output ripple, stability and transient response analysis.

Soft-Start

The LTM4661 contains internal circuitry to provide soft-start operation. The soft-start utilizes a linearly increasing ramp of the error amplifier reference voltage from zero to its nominal value of 1.2V in approximately 10ms, with the internal control loop driving V_{OUT} from zero to its final programmed value. This limits the inrush current drawn from the input source. As a result, the duration of the soft-start is largely unaffected by the size of the output capacitor or the output regulation voltage. The soft-start period is reset by a shutdown command on SDB, a UVLO event on $INTV_{CC}$ ($INTV_{CC}$ < 1.5V), an overvoltage event on V_{OUT} (V_{OUT} ≥ 16.5V), or an overtemperature event (TSD is invoked when the die temperature exceeds 170°C). Upon removal of these fault conditions, the LTM4661 will soft-start the output voltage.

Burst Mode Operation

In applications where high efficiency at light load current are more important than output voltage ripple, Burst Mode operation could be used by connecting SYNC/MODE pin to GND to improve light load efficiency. The output current (I_{OUT}) capability in Burst Mode operation is significantly less than in continuous current mode (CCM) and varies with V_{IN} and V_{OUT}, as shown in Figure 2. The LTM4661 will operate in CCM mode even if Burst Mode operation is commanded during soft-start.

In Burst Mode operation, only one phase of the LTM4661 is operational, while the other phase is disabled. The phase inductor current is initially charged to approximately 700mA by turning on the N-channel MOSFET switch, at which point the N-channel switch is turned off and the P-channel synchronous switch is turned on,

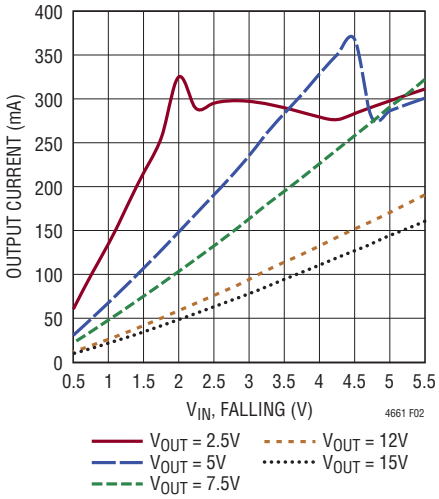


Figure 2. Burst Mode Output Current vs V_{IN}

APPLICATIONS INFORMATION

delivering current to the output. When the inductor current discharges to approximately zero, the cycle repeats. In Burst Mode operation, energy is delivered to the output until the nominal regulation value is reached, then the LTM4661 transitions into a very low quiescent current sleep state. In sleep, the output switches are turned off and the LTM4661 consumes only 25µA of quiescent current. When the output voltage droops approximately 1%, switching resumes. This maximizes efficiency at very light loads by minimizing switching and quiescent losses. Output voltage ripple in Burst Mode operation is typically 1% to 2% peak-to-peak. Additional output capacitance (22µF or greater), or the addition of a small feedforward capacitor (10pF to 50pF) connected between V_{OUT} and FB, can help further reduce the output ripple.

Operation Frequency

The operating frequency of the LTM4661 is optimized to achieve the compact package size and the minimum output ripple voltage while still keeping high efficiency. The default operating frequency is internally set to 1MHz. In most applications, no additional frequency adjusting is required.

If any operating frequency other than 1MHz is required by application, the operating frequency can be increased by adding a resistor, R_{FSET}, between the FREQ pin and GND, as shown in Figure 18. The operating frequency can be calculated as:

$$f_s(MHz) = \frac{28 + R_{FSET}(k\Omega)}{R_{FSET}(k\Omega)}$$

Frequency Synchronization

The switching frequency of the LTM4661 can be synchronized to a desired frequency by applying a clock of *twice* the desired frequency to the SYNC/MODE pin. Also, the free running frequency needs to be adjusted to a frequency approximately 80% of the desired frequency. Please use the equation in the Operation Frequency section to calculate the external R_{FSET} resistor value.

For example, if the LTM4661 needs to be synchronized to 1.5MHz switching frequency, an external clock of 3MHz needs to supply to SYNC/MODE pin while adding a 140kΩ R_{FSET} resistor between FREQ pin and GND to program the free run frequency to 1.2MHz.

Shutdown

The boost converter is disabled by pulling SDB below 0.25V and enabled by pulling SDB above 1.6V. Note that SDB pin can be driven above V_{IN} or V_{OUT}, as long as it is limited to less than its absolute maximum rating.

Thermal Shutdown

If the die temperature exceeds 170°C typical, the LTM4661 will go into thermal shutdown (TSD). All switches will be shut off until the die temperature drops by approximately 7°C, when the device reinitiates a soft-start and switching is re-enabled.

Output Disconnect

The LTM4661's output disconnect feature eliminates body diode conduction of the internal P-channel MOSFET rectifiers. This feature allows for V_{OUT} to discharge to 0V during shutdown and draw no current from the input source. Inrush current will also be limited at turn-on, minimizing surge currents seen by the input supply. The output disconnect feature also allows V_{OUT} to be pulled high, without back-feeding the power source connected to V_{IN}.

Short-Circuit Protection

The LTM4661 output disconnect feature allows output short-circuit protection while maintaining a maximum set current limit. To reduce power dissipation under overload and short-circuit conditions, the peak switch current limits are reduced to approximately 2A. Once V_{OUT} exceeds approximately 1.5V, the current limits are reset to their nominal values of 3.5A peak switching current per phase.

Output Overvoltage Protection

An overvoltage condition occurs when V_{OUT} exceeds approximately 16.5V. Switching is disabled and the internal soft-start ramp is reset. Once V_{OUT} drops below approximately 16V, a soft-start is initiated and switching is allowed to resume. If the boost converter output is lightly loaded such that the time constant of the output

APPLICATIONS INFORMATION

capacitance, C_{OUT} and the output load resistance, R_{OUT} is near or greater than the soft-start time of approximately 10ms, the soft-start ramp may end before or soon after switching resumes, defeating the inrush current limiting of the closed-loop soft-start following an overvoltage event.

Thermal Considerations and Output Current Derating

The thermal resistances reported in the Pin Configuration section of the data sheet are consistent with those parameters defined by JESD51-9 and are intended for use with finite element analysis (FEA) software modeling tools that leverage the outcome of thermal modeling, simulation and correlation to hardware evaluation performed on a µModule package mounted to a hardware test board—also defined by JESD51-9 ("Test Boards for Area Array Surface Mount Package Thermal Measurements"). The motivation for providing these thermal coefficients in found in JESD51-12 ("Guidelines for Reporting and Using Electronic Package Thermal Information").

Many designers may opt to use laboratory equipment and a test vehicle such as the demo board to anticipate the µModule regulator's thermal performance in their application at various electrical and environmental operating conditions to compliment any FEA activities. Without FEA software, the thermal resistances reported in the Pin Configuration section are in and of themselves not relevant to providing guidance of thermal performance; instead, the derating curves provided in the data sheet can be used in a manner that yields insight and guidance pertaining to one's application usage and can be adapted to correlate thermal performance to one's own application.

The Pin Configuration section typically gives four thermal coefficients explicitly defined in JESD51-12; these coefficients are quoted or paraphrased below:

1. θ_{JA}, the thermal resistance from junction to ambient, is the natural convection junction-to-ambient air thermal resistance measured in a one cubic foot sealed enclosure. This environment is sometimes referred to as "still air" although natural convection causes the air to move. This value is determined with the part mounted to a JESD51-9 defined test board, which does not reflect an actual application or viable operating condition.
2. $\theta_{JCbottom}$, the thermal resistance from junction to ambient, is the natural convection junction-to-ambient air thermal resistance measured in a one cubic foot sealed enclosure. This environment is sometimes referred to as "still air" although natural convection causes the air to move. This value is determined with the part mounted to a JESD51-9 defined test board, which does not reflect an actual application or viable operating condition.
3. θ_{JCtop}, the thermal resistance from junction to top of the product case, is determined with nearly all of the component power dissipation flowing through the top of the package. As the electrical connections of the typical µModule are on the bottom of the package, it is rare for an application to operate such that most of the heat flows from the junction to the top of the part. As in the case of $\theta_{JCbottom}$, this value may be useful for comparing packages but the test conditions don't generally match the user's application.
4. θ_{JB}, the thermal resistance from junction to the printed circuit board, is the junction-to-board thermal resistance where almost all of the heat flows through the bottom of the µModule and into the board, and is really the sum of the $\theta_{JCbottom}$ and the thermal resistance of the bottom of the part through the solder joints and through a portion of the board. The board temperature is measured a specified distance from the package, using a two sided, two layer board. This board is described in JESD51-9.

A graphical representation of the aforementioned thermal resistances is given in Figure 3; blue resistances are contained within the µModule regulator, whereas green resistances are external to the µModule.

As a practical matter, it should be clear to the reader that no individual or subgroup of the four thermal resistance parameters defined by JESD51-12 or provided in the Pin Configuration section replicates or conveys normal operating conditions of a µModule. For example, in normal board-mounted applications, never does 100% of the device's total power loss (heat) thermally conduct

APPLICATIONS INFORMATION

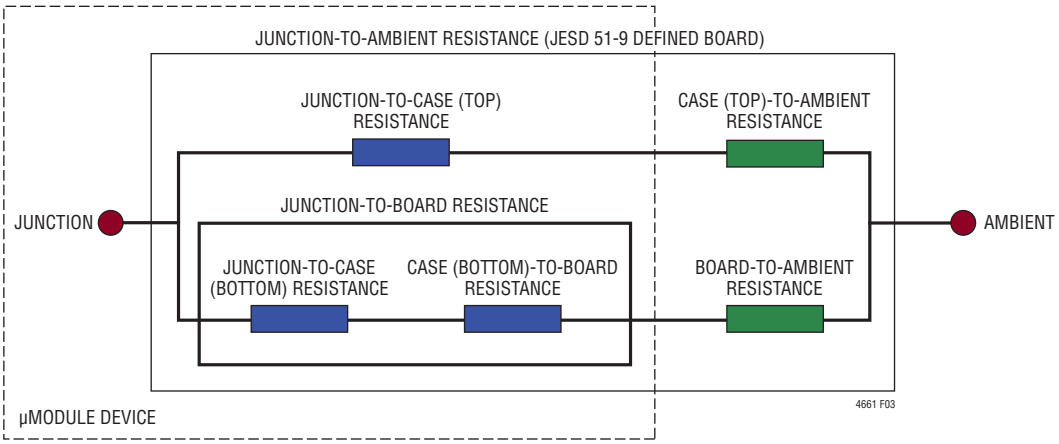


Figure 3. Graphical Representation of JESD51-12 Thermal Coefficients

exclusively through the top or exclusively through bottom of the µModule—as the standard defines for θ_{JCtop} and $\theta_{JCbottom}$, respectively. In practice, power loss is thermally dissipated in both directions away from the package—granted, in the absence of a heat sink and airflow, a majority of the heat flow is into the board.

Within a SIP (system-in-package) module, be aware there are multiple power devices and components dissipating power, with a consequence that the thermal resistances relative to different junctions of components or die are not exactly linear with respect to total package power loss. To reconcile this complication without sacrificing modeling simplicity—but also, not ignoring practical realities—an approach has been taken using FEA software modeling along with laboratory testing in a controlled-environment chamber to reasonably define and correlate the thermal resistance values supplied in this data sheet: (1) Initially, FEA software is used to accurately build the mechanical geometry of the µModule and the specified PCB with all of the correct material coefficients along with accurate power loss source definitions; (2) this model simulates a software-defined JEDEC environment consistent with JESD51-9 to predict power loss heat flow and temperature readings at different interfaces that enable the calculation of the JEDEC-defined thermal resistance values; (3) the model and FEA software is used to evaluate the µModule with heat sink and airflow; (4) having solved for and analyzed these thermal resistance values and simulated various operating conditions in the software model, a thorough laboratory evaluation replicates the simulated conditions with thermocouples within a controlled-environment chamber while operating the device at the same power loss as that which was simulated. An outcome of this process and due diligence yields a set of derating curves provided in other sections of this data sheet. After these laboratory tests have been performed and correlated to the µModule model, then the θ_{JB} and θ_{BA} are summed together to correlate quite well with the µModule model with no airflow or heat sinking in a properly defined chamber. This θ_{JB} + θ_{BA} value is shown in the Pin Configuration section and should accurately equal the θ_{JA} value because approximately 100% of power loss flows from the junction through the board into ambient with no airflow or top mounted heat sink.

The 5V, 8V, 12V and 15V output power loss curves in Figures 4 to 7 can be used in coordination with the load current derating curves in Figures 8 to 14 for calculating an approximate θ_{JA} thermal resistance for the LTM4661 with various heat sinking and airflow conditions. The power loss curves are taken at room temperature and are increased with multiplicative factors according to the ambient temperature. These approximate factors is 1.4 assuming the junction temperature at 110°C. The output voltages are chosen to include the lower and higher output voltage ranges for correlating the thermal resistance. Thermal models are derived from several temperature measurements in a controlled temperature chamber along with thermal modeling analysis. The junction temperatures are monitored while ambient temperature is increased with and without airflow. The power loss increase with ambient temperature

APPLICATIONS INFORMATION

change is factored into the derating curves. The junctions are maintained at 110°C maximum while lowering output current or power with increasing ambient temperature. The decreased output current will decrease the internal module loss as ambient temperature is increased. The monitored junction temperature of 110°C minus the ambient operating temperature specifies how much module temperature rise can be allowed. As an example, in Figure 13 the load current is derated to ~0.35A at ~80°C with no air or heat sink and the power loss for the 3.3V to 15V at 0.35A output is about 1.4W. The 1.4W loss is calculated with the ~1.0W room temperature loss from the 3.3V to 15V power loss curve at 0.35A, and the 1.4 multiplying factor. If the 80°C ambient temperature is subtracted from the 110°C junction temperature, then the difference of 30°C divided by 1.4W equals a 21.4°C/W θ_{JA} thermal resistance. Table 3 specifies a 21°C/W value which is very close. Table 3 to Table 6 provide equivalent thermal resistances for 5V, 8V, 12V and 15V outputs with and without airflow and heat sinking. The derived thermal resistances in Tables 3 to 6 for the various conditions can be multiplied by the calculated power loss as a function of ambient temperature to derive temperature rise above ambient, thus maximum junction temperature. Room temperature power loss can be derived from the efficiency curves in the Typical Performance Characteristics section and adjusted with the above ambient temperature multiplicative factors. The printed circuit board is a 1.6mm thick four layer board with two ounce copper for the two outer layers and one ounce copper all four layers. The PCB dimensions are 65mm × 65mm.

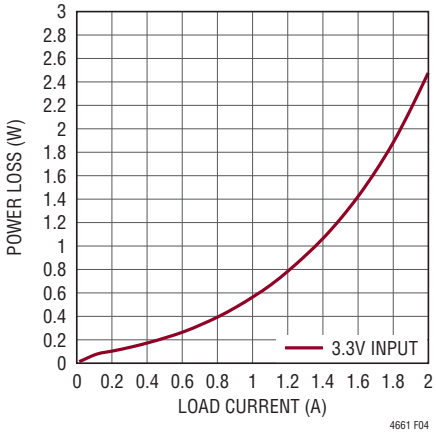


Figure 4. 5V Output Power Loss

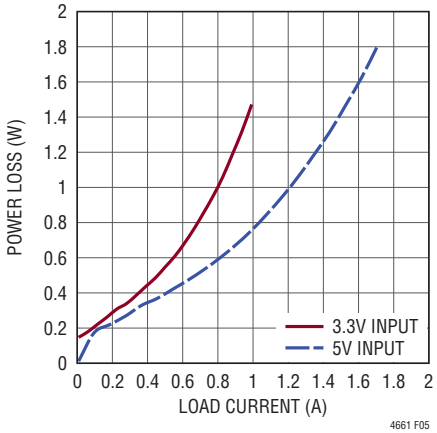


Figure 5. 8V Output Power Loss

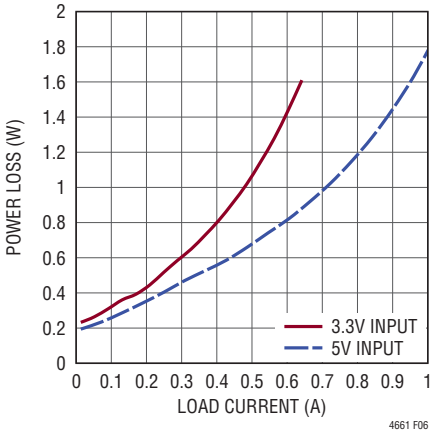


Figure 6. 12V Output Power Loss

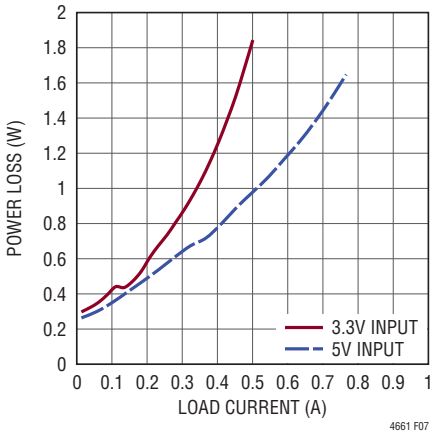


Figure 7. 15V Output Power Loss

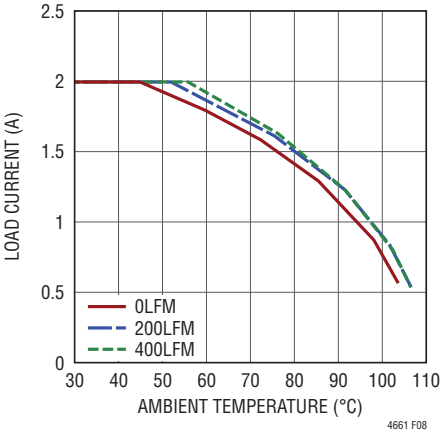


Figure 8. 3.3V to 5V Derating Curve, No Heat Sink

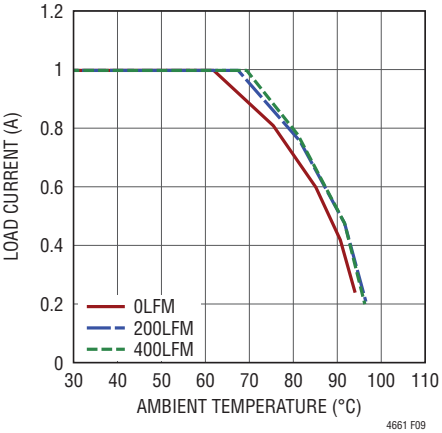


Figure 9. 3.3V to 8V Derating Curve, No Heat Sink

APPLICATIONS INFORMATION

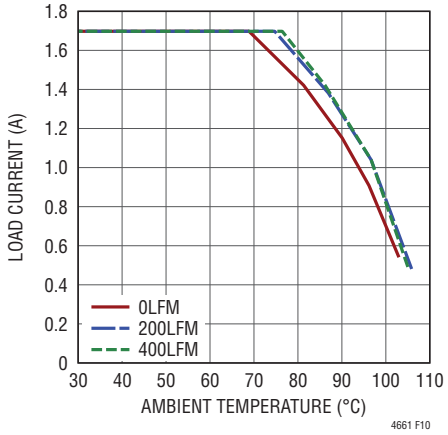


Figure 10. 5V Input to 8V Output Derating Curve, No Heat Sink

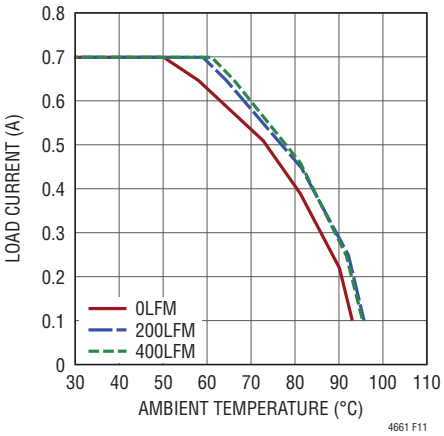


Figure 11. 3.3V Input to 12V Output Derating Curve, No Heat Sink

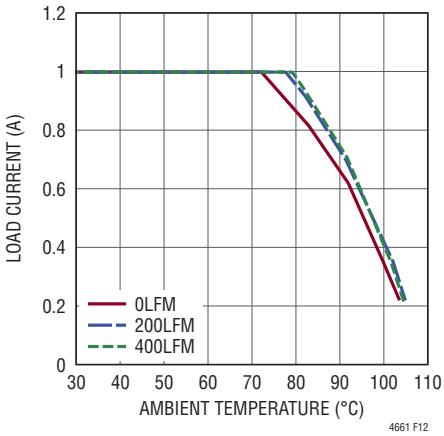


Figure 12. 5V Input to 12V Output Derating Curve, No Heat Sink

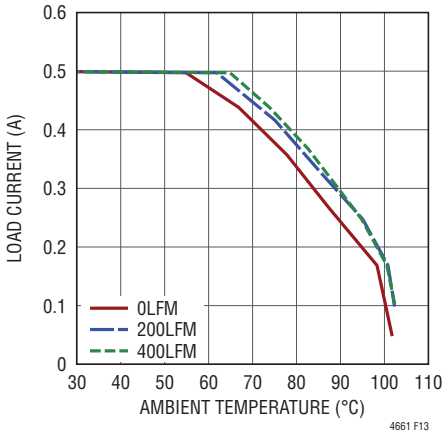


Figure 13. 3.3V Input to 15V Output Derating Curve, No Heat Sink

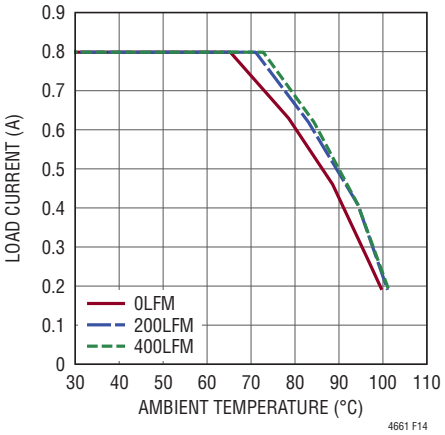


Figure 14. 5V Input to 15V Output Derating Curve, No Heat Sink

APPLICATIONS INFORMATION

Table 3. 5V Output

DERATING CURVE	V_{IN} (V)	POWER LOSS CURVE	AIRFLOW (LFM)	HEAT SINK	θ_{JA} (°C/W)
Figure 8	3.3	Figure 4	0	None	21
Figure 8	3.3	Figure 4	200	None	19
Figure 8	3.3	Figure 4	400	None	18

Table 4. 8V Output

DERATING CURVE	V_{IN} (V)	POWER LOSS CURVE	AIRFLOW (LFM)	HEAT SINK	θ_{JA} (°C/W)
Figure 9, Figure 10	3.3, 5	Figure 5	0	None	21
Figure 9, Figure 10	3.3, 5	Figure 5	200	None	19
Figure 9, Figure 10	3.3, 5	Figure 5	400	None	18

Table 5. 12V Output

DERATING CURVE	V_{IN} (V)	POWER LOSS CURVE	AIRFLOW (LFM)	HEAT SINK	θ_{JA} (°C/W)
Figure 11, Figure 12	3.3, 5	Figure 6	0	None	21
Figure 11, Figure 12	3.3, 5	Figure 6	200	None	19
Figure 11, Figure 12	3.3, 5	Figure 6	400	None	18

Table 6. 15V Output

DERATING CURVE	V_{IN} (V)	POWER LOSS CURVE	AIRFLOW (LFM)	HEAT SINK	θ_{JA} (°C/W)
Figure 13, Figure 14	3.3, 5	Figure 7	0	None	21
Figure 13, Figure 14	3.3, 5	Figure 7	200	None	19
Figure 13, Figure 14	3.3, 5	Figure 7	400	None	18

APPLICATIONS INFORMATION

Figure 15 shows a measured thermal picture of the LTM4661 running from 3.3V input to 12V output at 0.8A DC current with 200LFM airflow and no heat sink.

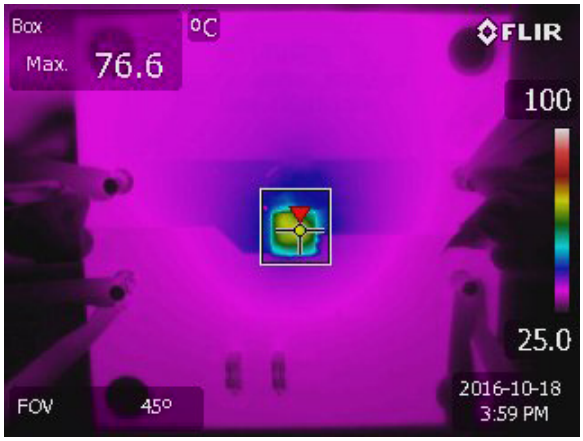


Figure 15. Thermal Image, 3.3V Input to 12V Output at 0.8A, 200LFM Airflow, No Heat Sink

Safety Considerations

The LTM4661 modules do not provide galvanic isolation from V_{IN} to V_{OUT}. There is no internal fuse. If required, a slow blow fuse with a rating twice the maximum input current needs to be provided to protect each unit from catastrophic failure. The device does support thermal shutdown and overcurrent protection.

Layout Checklist/Example

The high integration of LTM4661 makes the PCB board layout very simple and easy. However, to optimize its electrical and thermal performance, some layout considerations are still necessary.

- Use large PCB copper areas for high current paths, including V_{IN}, GND and V_{OUT}. It helps to minimize the PCB conduction loss and thermal stress.
- Place high frequency ceramic input and output capacitors next to the V_{IN}, PGND and V_{OUT} pins to minimize high frequency noise.
- Place a dedicated power ground layer underneath the unit.
- To minimize the via conduction loss and reduce module thermal stress, use multiple vias for interconnection between top layer and other power layers.
- Do not put vias directly on the pad, unless they are capped or plated over.
- For parallel modules, tie the V_{OUT}, V_{FB} and COMP pins together. Use an internal layer to closely connect these pins together.
- Bring out test points on the signal pins for monitoring.

Figure 16 gives a good example of the recommended layout.

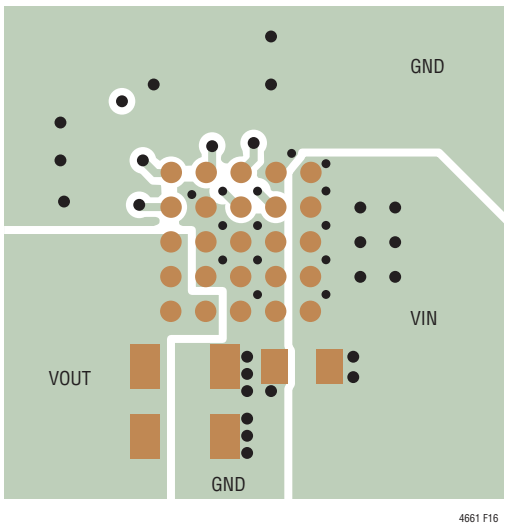


Figure 16. Recommended PCB Layout

APPLICATIONS INFORMATION

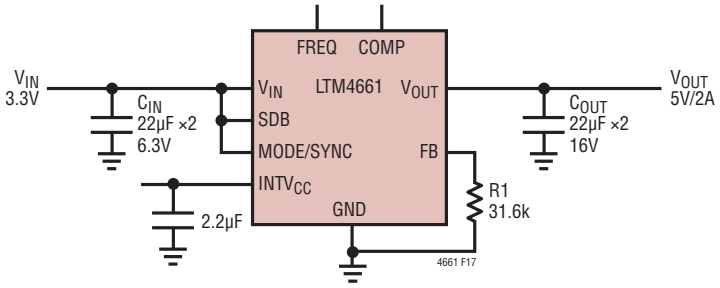


Figure 17. 3.3V Input to 5V Output, at 2A Design

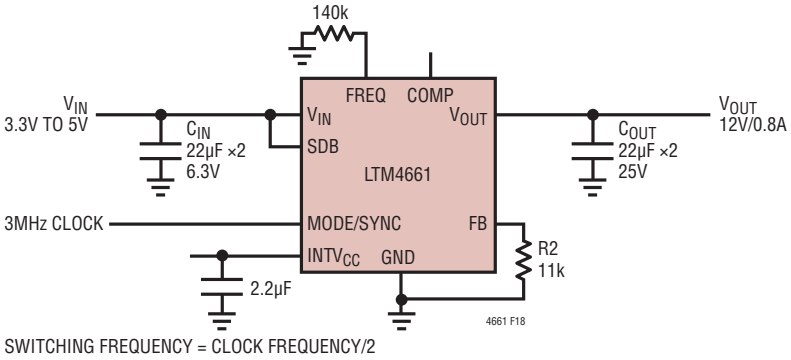


Figure 18. 3.3V to 5V Input, 12V Output Design with External Clock

APPLICATIONS INFORMATION

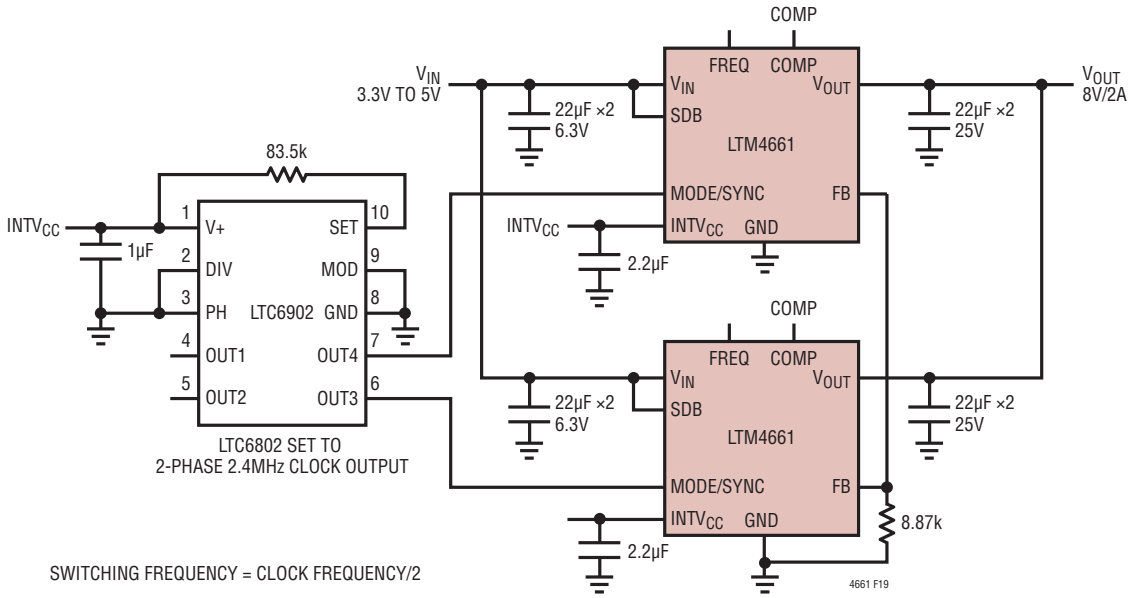


Figure 19. Two LTM4661 Module Parallel Design for 8V/2A Output Running at 1.2MHz

PACKAGE DESCRIPTION

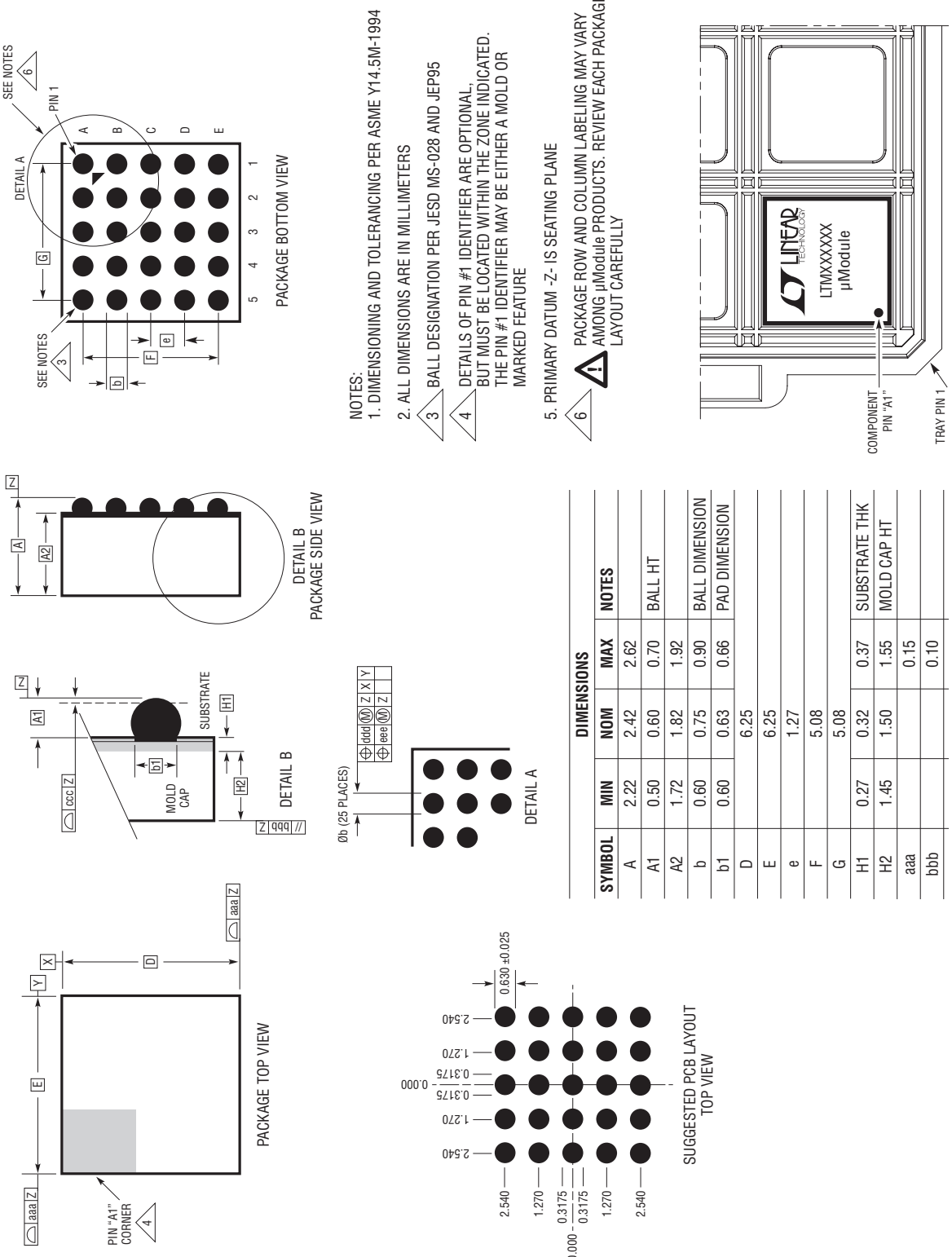
PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG µModule PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY.

LTM4661 Component BGA Pinout

PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION
A1	V_{IN}	A2	GND	A3	GND	A4	V_{OUT}	A5	V_{OUT}
B1	V_{IN}	B2	GND	B3	GND	B4	GND	B5	V_{OUT}
C1	V_{IN}	C2	GND	C3	GND	C4	GND	C5	V_{OUT}
D1	V_{IN}	D2	SYNC/MODE	D3	$INTV_{CC}$	D4	GND	D5	SDB
E1	V_{IN}	E2	GND	E3	FREQ	E4	COMP	E5	FB

PACKAGE DESCRIPTION

BGA Package
25-Lead (6.25mm × 6.25mm × 2.42mm)
(Reference LTC DWG # 05-08-1502 Rev A)



DIMENSIONS

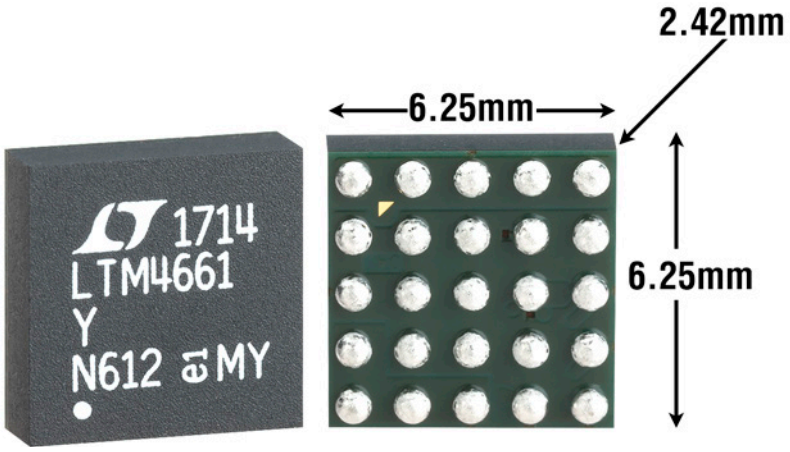
SYMBOL	MIN	NOM	MAX	NOTES
A	2.22	2.42	2.62	
A1	0.50	0.60	0.70	BALL HT
A2	1.72	1.82	1.92	
b	0.60	0.75	0.90	BALL DIMENSION
b1	0.60	0.63	0.66	PAD DIMENSION
D		6.25		
E		6.25		
e		1.27		
F		5.08		
G		5.08		
H1	0.27	0.32	0.37	SUBSTRATE THK
H2	1.45	1.50	1.55	MOLD CAP HT
aaa			0.15	
bbb			0.10	

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	10/18	Updated condition based on ATE H/W: C_{OUT} = 2 × 22µF Added clarity to $I_{MODE/SYNC}$ condition: SYNC/MODE = 5.5V Removed Note 3, Note 5, Note 6; Not referenced in data sheet Changed “RUN” to “SDB”	3 3 4 5

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PACKAGE PHOTO



DESIGN RESOURCES

SUBJECT	DESCRIPTION	
µModule Design and Manufacturing Resources	Design: • Selector Guides • Demo Boards and Gerber Files • Free Simulation Tools	Manufacturing: • Quick Start Guide • PCB Design, Assembly and Manufacturing Guidelines • Package and Board Level Reliability
µModule Regulator Products Search	1. Sort table of products by parameters and download the result as a spread sheet. 2. Search using the Quick Power Search parametric table. Quick Power Search INPUT | V_{in}(Min) V V_{in}(Max) V OUTPUT | V_{Out} V I_{out} A FEATURES | Low EMI Ultrathin Internal Heat Sink Multiple Outputs Search	
Digital Power System Management	Analog Devices' family of digital power supply management ICs are highly integrated solutions that offer essential functions, including power supply monitoring, supervision, margining and sequencing, and feature EEPROM for storing user configurations and fault logging.	

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTM8054	36V_{IN}, 5.4A Buck-Boost µModule Regulator	5V ≤ V_{IN} ≤ 36V, 1.2V ≤ V_{OUT} ≤ 36V, 11.25mm × 15mm × 3.42mm BGA
LTM8045	SEPIC (Boost) or Inverting µModule Regulator	2.8V ≤ V_{IN} ≤ 18V. ±2.5V ≤ V_{OUT} ≤ ±15V, I_{OUT} is Up to 700mA. 6.25mm × 11.25mm x 4.92mm BGA
LTM8049	Dual, SEPIC (Boost) and/or Inverting µModule Regulator	2.6V ≤ V_{IN} ≤ 20V, ±2.5V ≤ V_{OUT} ≤ ±24V, I_{OUT} is Up to 1.5A, 9mm × 15mm × 2.42mm BGA
LTM4622	Ultrathin, 20V_{IN}, Dual 2.5A Step-Down µModule Regulator	3.6V ≤ V_{IN} ≤ 20V, 0.6V ≤ V_{OUT} ≤ 5.5V, 6.25mm × 6.25mm × 1.82mm LGA, 6.25mm × 6.25mm × 2.42mm BGA
LTM4643	Ultrathin, 20V_{IN}, Quad 3A Step-Down µModule Regulator	4V ≤ V_{IN} ≤ 20V, 0.6V ≤ V_{OUT} ≤ 3.3V, 9mm × 15mm × 1.82mm LGA, 9mm × 15mm × 2.42mm BGA

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