EN55022B Compliant 58V, 4A Step-Down DC/DC µModule Regulator

FEATURES

- **Complete Low EMI Switch Mode Power Supply**
- **EN55022 Class B Compliant**
- **Wide Input Voltage Range: 3.1V to 58V**
- **Up to 4A Output Current**
- **Output Voltage Range: 0.5V ≤ V_{OUT} ≤ 0.94 • V_{IN}**
- **±1.67% Total DC Output Voltage Error Over Line, Load and Temperature (–40°C to 125°C)**
- **Parallel and Current Share with Multiple LTM4653s**
- **Analog Output Current Indicator**
- **Programmable Input Voltage Limiting**
- Constant-Frequency Current Mode Control
- Power Good Indicator and Programmable Soft-Start
- Overcurrent/Overvoltage/Overtemperature Protection
- 15mm × 9mm × 5.01mm BGA Package

APPLICATIONS

- Avionics, Industrial Control and Test Equipment
- Video, Imaging and Instrumentation
- 48V Telecom and Network Power Supplies
- RF Systems

DESCRIPTION

The LTM®4653 is an ultralow noise 58V, 4A DC/DC step-down µModule® regulator designed to meet the radiated emissions requirements of EN55022. Conducted emission requirements can be met by adding standard filter components. Included in the package are the switching controller, power MOSFETs, inductor, filters and support components.

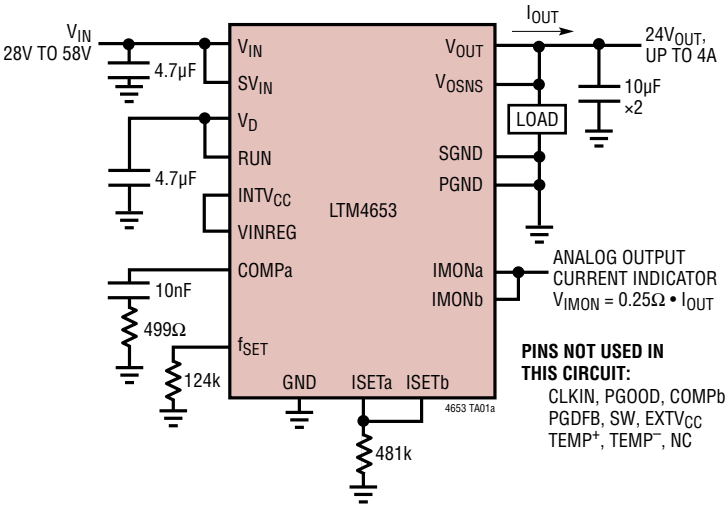
Operating over an input voltage range of 3.1V to 58V, the LTM4653 supports an output voltage range of 0.5V to 94% of V_{IN}, and a switching frequency range of 250kHz to 3MHz (400kHz default), each set by a single resistor. For high load currents, the LTM4653 can be paralleled in PolyPhase® operation and synchronized to an external clock. Only the bulk input and output filter capacitors are needed to finish the design.

The LTM4653 is offered in a 15mm × 9mm × 5.01mm BGA package with SnPb or RoHS compliant terminal finish.

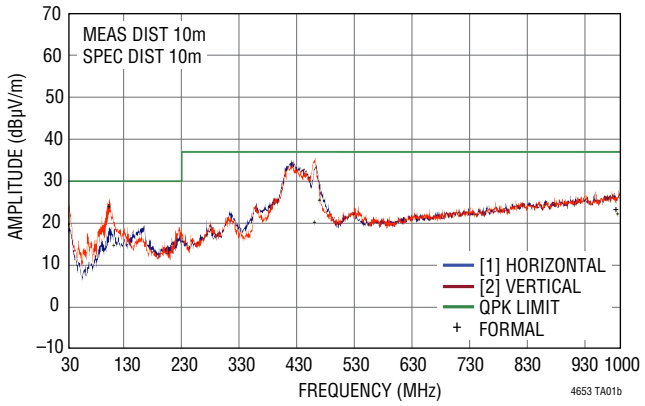
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TYPICAL APPLICATION

4A, 24V Output Low EMI DC/DC µModule Regulator with Analog Output Current Indicator



Radiated Emission Scan in a 10m Chamber LTM4653 Delivering 24V_{OUT} at 3.5A, from 48V_{IN}



Rev. A

ABSOLUTE MAXIMUM RATINGS

(Note 1) (All Voltages Relative to V_{OUT}^- Unless Otherwise Indicated)

Terminal Voltages

V_{IN}, V_D, SV_{IN}, SW, ISETa, V_{OUT}, V_{OSNS} .....–0.3V to 60V
GND, ISETb, $EXTV_{CC}$ ..... –0.3V to 28V
RUN ..... GND–0.3V to PGND+60V
$INTV_{CC}$, PGDFB, VINREG, COMPa, COMPb,
IMONa, IMONb ..... –0.3V to 4V
f_{SET} .....–0.3V to $INTV_{CC}$
CLKIN, PGOOD (Relative to GND) ..... –0.3V to 6V

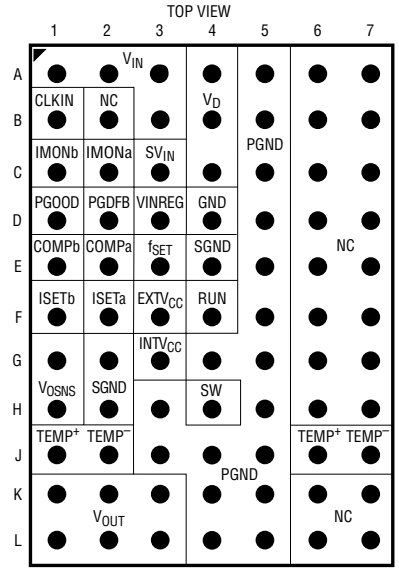
Terminal Currents

$INTV_{CC}$ Peak Output Current (Note 8).....30mA
$TEMP^+$.....–1mA to 10mA
$TEMP^-$ .....–10mA to 1mA

Temperatures

Internal Operating Temperature Range
(Note 2) ..... –40°C to 125°C
Storage Temperature Range ..... –55°C to 125°C
Peak Solder Reflow Package
Body Temperature ..... 245°C

PIN CONFIGURATION



BGA PACKAGE
77-PIN (15mm × 9mm × 5.01mm)
$T_{J(MAX)}$ = 125°C; θ_{JA} = 15.5°C/W;
θ_{JCtop} = 20.6°C/W; θ_{JCbot} = 5.1°C/W;
WEIGHT = 1.8 GRAMS

NOTES:
1) θ VALUES ARE DETERMINED BY SIMULATION PER JESD51 CONDITIONS.
2) θ_{JA} VALUE IS OBTAINED WITH DEMO BOARD.
3) REFER TO APPLICATION INFORMATION SECTION FOR LAB MEASUREMENT AND DERATING INFORMATION.

ORDER INFORMATION

PART NUMBER	PAD OR BALL FINISH	PART MARKING*		PACKAGE TYPE	MSL RATING	TEMPERATURE RANGE (SEE NOTE 2)
		DEVICE	FINISH CODE			
LTM4653EY#PBF	SAC305 (RoHS)	LTM4653Y	e1	BGA	3	–40°C to 125°C
LTM4653IY#PBF	SAC305 (RoHS)		e1			–40°C to 125°C
LTM4653IY	SnPb (63/37)		e0			–40°C to 125°C

- Contact the factory for parts specified with wider operating temperature ranges. *Pad or ball finish code is per IPC/JEDEC J-STD-609.
- Recommended LGA and BGA PCB Assembly and Manufacturing Procedures
- LGA and BGA Package and Tray Drawings

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified internal operating temperature range (Note 2). T_A = 25°C, Test Circuit, V_{IN} = SV_{IN} = 48V, $EXTV_{CC}$ = 24V, RUN = 3.3V, R_{ISET} = 480k, R_{fSET} = 57.6kΩ, f_{SW} = 1.5MHz (CLKIN driven with 1.2MHz clock signal) unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$SV_{IN(DC)}$, $V_{IN(DC)}$	Input DC Voltage		●	3.1		58	V
$V_{OUT(RANGE)}$	Range of Output Voltage Regulation	0.5V ≤ ISETa - SGND ≤ 0.94V_{IN}, I_{OUT} = 0A (See Note 6)	●	0.5		0.94V_{IN}	V
$V_{OUT(24VDC)}$	Output Voltage Total Variation with Line and Load at V_{OUT} = 24V	28V ≤ V_{IN} ≤ 58V, 0A ≤ I_{OUT} ≤ 4A, C_{INH} = 4.7µF, C_D = 4.7µF, C_{OUTH} = 2 × 47µF, CLKIN driven with 1.5MHz Clock	●	23.6	24	24.4	V
$V_{OUT(0.5VDC)}$	Output Voltage Total Variation with Line and Load at V_{OUT} = 0.5V	Measuring V_{OSNS} - ISETa 3.1V ≤ V_{IN} ≤ 13.2V, 0A ≤ I_{OUT} ≤ 4A, C_{INH} = 4.7µF, C_D = 4.7µF, C_{OUTH} = 2 × 47µF, ISETa = 500mV, R_{fSET} = N/U (Note 5)	●	–15	0	15	mV
Input Specifications							
$V_{IN(UVLO)}$	SV_{IN} Undervoltage Lockout Threshold	SV_{IN} Rising SV_{IN} Falling Hysteresis	● ● ●	 2.4 150	2.85 2.6 250	3.1 2.9	V V mV
$V_{IN(OVLO)}$	SV_{IN} Overvoltage Lockout Rising	(Note 4)		64	68		V
$V_{IN(HYS)}$	SV_{IN} Overvoltage Lockout Hysteresis	(Note 4)			2	4	V
$I_{INRUSH(VIN)}$	Input Inrush Current at Start-Up	C_{INH} = 4.7µF, C_D = 4.7µF, C_{OUTH} = 2 × 47µF; I_{OUT} = 0A, ISETa Electrically Connected to ISETb			300		mA
$I_{Q(SVIN)}$	Input Supply Bias Current	Shutdown, RUN = GND RUN = V_{IN}			16 450	30	µA µA
$I_{S(VIN, FCM)}$	Input Supply Current	CLKIN Open Circuit, I_{OUT} = 4A			2.1		A
$I_{S(VIN, SHUTDOWN)}$	Input Supply Current in Shutdown	Shutdown, RUN = GND			4		µA
Output Specifications							
I_{OUT}	V_{OUT} Output Continuous Current Range	(Note 3)		0		4	A
$\Delta V_{OUT(LINE)}/V_{OUT}$	Line Regulation Accuracy	I_{OUT} = 0A, 28V ≤ V_{IN} ≤58V	●		0.05	0.1	%
$\Delta V_{OUT(LOAD)}/V_{OUT}$	Load Regulation Accuracy	V_{IN} = 48V, 0A ≤ I_{OUT} ≤ 4A	●		0.05	0.75	%
$V_{OUT(AC)}$	Output Voltage Ripple, V_{OUT}	V_{IN} = 12V, ISETa = 5V			2		mV_{P-P}
f_s	V_{OUT} Ripple Frequency	ISETa = 5V, R_{fSET} = 57.6k, CLKIN Open Circuit	●	1.7	1.95	2.2	MHz
$\Delta V_{OUT(START)}$	Turn-On Overshoot				8		mV
t_{START}	Turn-On Start-Up Time	Delay Measured from V_{IN} Toggling from 0V to 48V to PGOOD Exceeding 3V; PGOOD Having a 100k Pull-Up to 3.3V, VPGFB Resistor-Divider Network as Shown in Test Circuit, R_{ISETa} = 480k, ISETa Electrically Connected to ISETb and CLKIN Driven with 1.5MHz Clock	●		4	9	ms
$\Delta V_{OUT(LS)}$	Peak Output Voltage Deviation for Dynamic Load Step	I_{OUT}: 0A to 2A and 2A to 0A Load Steps in 1µs, C_{OUTH} = 47µF × 2			400		mV
t_{SETTLE}	Settling Time for Dynamic Load Step	I_{OUT}: 0A to 2A and 2A to 0A Load Steps in 1µs, C_{OUTH} = 47µF × 2			50		µs
$I_{OUT(OCL)}$	I_{OUT}^- Output Current Limit				5.5		A
Control Section							
I_{ISETa}	Reference Current of ISETa Pin	V_{ISETa} = 0.5V, 3.1V ≤ V_{IN} ≤ 13.2V V_{ISETa} = 24V, 28V ≤ V_{IN} ≤ 58V	● ●	49.3 49	50 50	50.7 51	µA µA
I_{VOSNS}	V_{OSNS} Leakage Current	V_{IN} = SV_{IN} = RUN = ISETa = 58V			600		µA
$t_{ON(MIN)}$	Minimum On-Time	(Note 4)			60		ns

ELECTRICAL CHARACTERISTICS

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SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{RUN}	RUN Turn-On/-Off Thresholds	RUN Input Turn-On Threshold, RUN Rising RUN Hysteresis	●	1.08	1.2 130	1.32	V mV
I_{RUN}	RUN Leakage Current	RUN = 3.3V	●		0.1	50	nA
Oscillator and Phase-Locked Loop (PLL)							
f_{OSC}	Oscillator Frequency Accuracy	V_{IN} = 12V, ISETa = 5V, and: f_{SET} Open Circuit R_{fSET} = 57.6kΩ (See f_s Specification)	●	360	400 1.95	440	kHz MHz
f_{SYNC}	PLL Synchronization Capture Range	V_{IN} = 12V, ISETa = 5V, CLKIN Driven with a GND-Referred Clock Toggling from 0.4V to 1.2V and Having a Clock Duty Cycle: From 10% to 90%; f_{SET} Open Circuit From 40% to 60%; R_{fSET} = 57.6kΩ		250 1.3		550 3	kHz MHz
V_{CLKIN}	CLKIN Input Threshold	V_{CLKIN} Rising V_{CLKIN} Falling		1.2		 0.4	V V
I_{CLKIN}	CLKIN Input Current	V_{CLKIN} = 5V V_{CLKIN} = 0V		 –20	230 –5	500	µA µA
Power Good Feedback Input and Power Good Output							
OV_{PGDFB}	Output Overvoltage PGOOD Upper Threshold	PGDFB Rising	●	620	645	675	mV
UV_{PGDFB}	Output Undervoltage PGOOD Lower Threshold	PGDFB Falling	●	525	555	580	mV
ΔV_{PGDFB}	PGOOD Hysteresis	PGDFB Returning			8		mV
R_{PGDFB}	Resistor Between PGDFB and SGND			4.94	4.99	5.04	kΩ
R_{PGOOD}	PGOOD Pull-Down Resistance	V_{PGOOD} = 0.1V, V_{PGDFB} < UV_{PGDFB} or V_{PGDFB} > OV_{PGDFB}			700	1500	Ω
$I_{PGOOD(LEAK)}$	PGOOD Leakage Current	V_{PGOOD} = 3.3V, UV_{PGDFB} < V_{PGDFB} < OV_{PGDFB}			0.1	1	µA
$t_{PGOOD(DELAY)}$	PGOOD Delay	PGOOD Low to High (Note 4) PGOOD High to Low (Note 4)			$16/f_{SW(HZ)}$ $64/f_{SW(HZ)}$		s s
Current Monitor and Input Voltage Regulation Pins							
h_{IMONa}	I_{OUT}/I_{IMONa}	Ratio of V_{OUT} Output Current to I_{IMONa} Current, I_{OUT} = 4A	●	36	40	44	k
$I_{OS(IMON)}$	I_{MONa} Offset Current	I_{IMONa} at I_{OUT} = 0A		–5		5	µA
I_{MONb} Resistor	Resistor Between I_{MONb} and SGND			9.8	10	10.2	kΩ
V_{IMONa}	I_{MONa} Servo Voltage	IMONa Voltage During Output Current Regulation	●	1.9	2.0	2.1	V
V_{VINREG}	VINREG Servo Voltage	VINREG Voltage During Output Current Regulation	●	1.8	2.0	2.2	V
I_{VINREG}	VINREG Leakage Current	VINREG = 2V			1		nA
$INTV_{CC}$ Regulator							
V_{INTVCC}	Channel Internal V_{CC} Voltage, No $INTV_{CC}$ Loading (I_{INTVCC} = 0mA)	3.6V ≤ SV_{IN} ≤ 58V, $EXTV_{CC}$ = Open Circuit 5V ≤ SV_{IN} ≤ 58V, 3.2V ≤ $EXTV_{CC}$ ≤ 26.5V		3.15 2.85	3.4 3.0	3.65 3.15	V V
$V_{EXTVCC(TH)}$	$EXTV_{CC}$ Switchover Voltage	(Note 4)			3.15		V
$\Delta V_{INTVCC(LOAD)}/V_{INTVCC}$	$INTV_{CC}$ Load Regulation	0mA ≤ I_{INTVCC} ≤ 30mA		–2	0.5	2	%

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified internal operating temperature range (Note 2). T_A = 25°C, Test Circuit, V_{IN} = SV_{IN} = 48V, $EXTV_{CC}$ = 24V, RUN = 3.3V, R_{ISET} = 480k, R_{fSET} = 57.6kΩ, f_{SW} = 1.5MHz (CLKIN driven with 1.2MHz clock signal) unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Temperature Sensor							
ΔV_{TEMP}	Temperature Sensor Forward Voltage, $V_{TEMP}^+ - V_{TEMP}^-$	I_{TEMP}^+ = 100µA and I_{TEMP}^- = –100µA at T_A = 25°C			0.6		V
$TC_{\Delta V(TEMP)}$	ΔV_{TEMP} Temperature Coefficient				–2.0		mV/°C

Note 1: Stresses beyond those listing under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating conditions for extended periods may affect device reliability and lifetime.

Note 2: The LTM4653 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTM4653E is guaranteed to meet performance specifications over the 0°C to 125°C internal operating temperature range. Specifications over the full –40°C to 125°C internal operating temperature range are assured by design, characterization and correlation with statistical process controls. The LTM4653I is guaranteed to meet specifications over the full internal operating temperature range. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance and other environmental factors.

Note 3: See output current derating curves for different V_{IN}, V_{OUT}, and T_A, located in the Applications Information section.

Note 4: Minimum on-time, V_{IN} Overvoltage Lockout and Overvoltage Lockout Hysteresis, and $EXTV_{CC}$ Switchover Threshold are tested at wafer sort.

Note 5: To ensure minimum on time criteria is met, $V_{OUT(0.5VDC)}$ high-line regulation is tested at 13.2V_{IN}, with f_{SET} and CLKIN open circuit. See the Applications Information section.

Note 6. See Applications Information Section for Dropout Criteria.

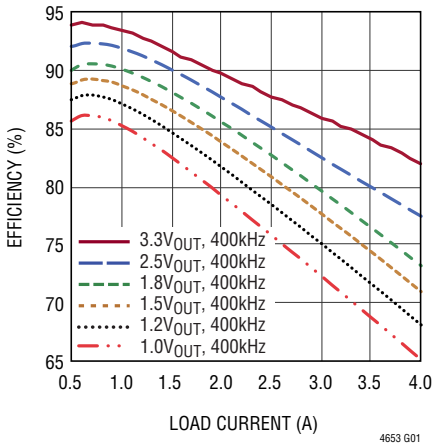
Note 7. This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

Note 8. The $INTV_{CC}$ Abs Max peak output current is specified as the sum of current drawn by circuits internal to the module biased off of $INTV_{CC}$ and current drawn by external circuits biased off of $INTV_{CC}$. See the Applications Information section.

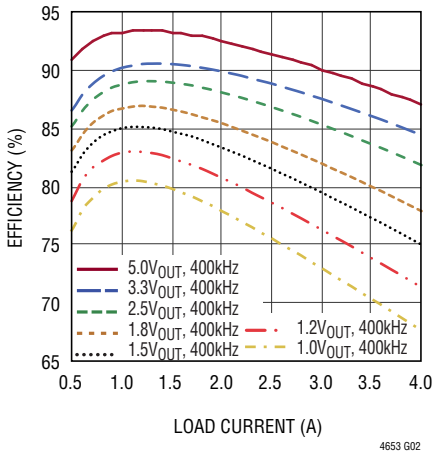
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

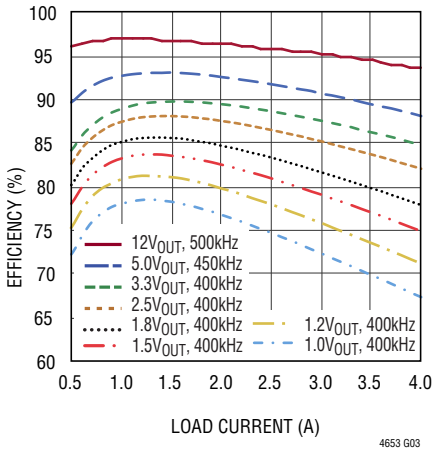
Efficiency vs Load Current at $5V_{IN}$, Forced Continuous Mode



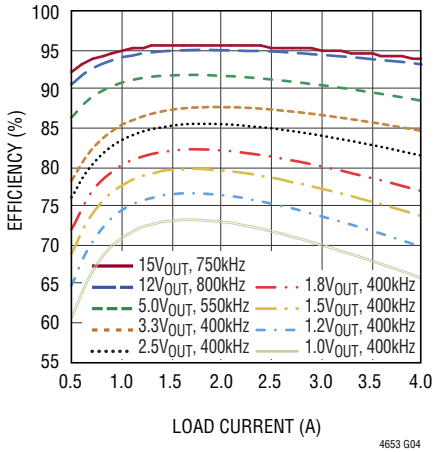
Efficiency vs Load Current at $12V_{IN}$, Forced Continuous Mode



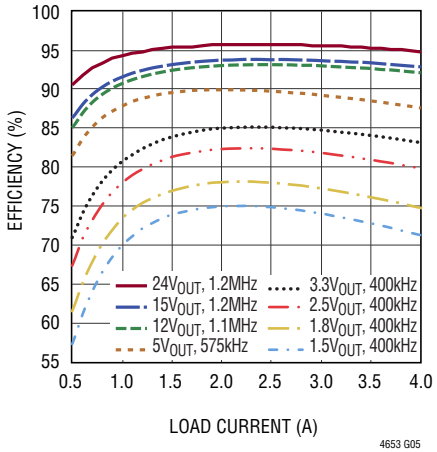
Efficiency vs Load Current at $15V_{IN}$, Forced Continuous Mode



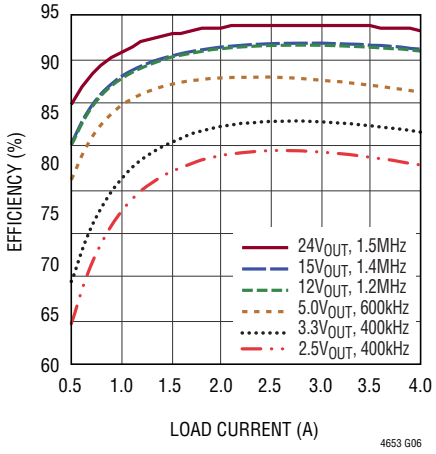
Efficiency vs Load Current at $24V_{IN}$, Forced Continuous Mode



Efficiency vs Load Current at $36V_{IN}$, Forced Continuous Mode



Efficiency vs Load Current at $48V_{IN}$, Forced Continuous Mode



3.3V Transient Response, $48V_{IN}$

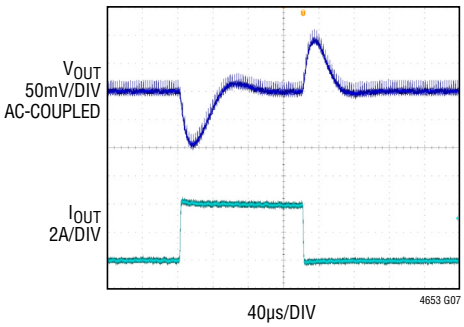


FIGURE 32 CIRCUIT, $48V_{IN}$,
C_{INH} = C_D = 4.7µF, C_{OUT} = 2 x 100µF,
R_{fSET} = N/A, R_{ISET} = 66.5kΩ,
C_{TH} = 10nF, R_{TH} = 604Ω,
R_{EXTVCC} = N/A, C_{EXTVCC} = N/A,
2A to 4A LOAD STEP AT 2A/µs

12V Transient Response, $48V_{IN}$

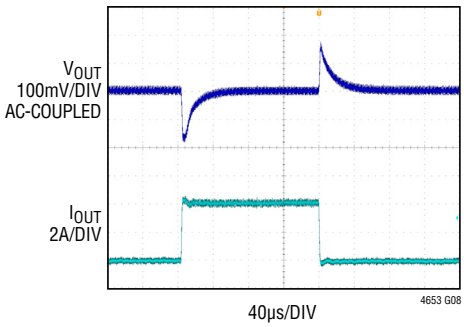


FIGURE 32 CIRCUIT, $48V_{IN}$,
C_{INH} = C_D = 4.7µF, C_{OUT} = 2 x 22µF,
R_{fSET} = 124k, R_{ISET} = 240kΩ,
C_{TH} = 10nF, R_{TH} = 562Ω,
R_{EXTVCC} = 49.9Ω, C_{EXTVCC} = 1µF,
2A to 4A LOAD STEP AT 2A/µs

1V Transient Response, $24V_{IN}$

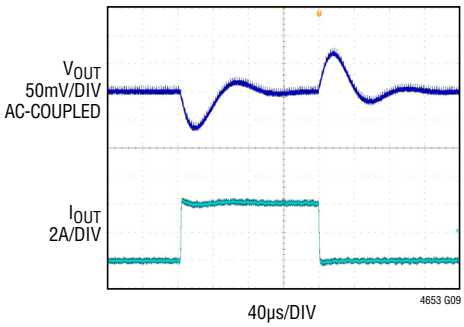


FIGURE 32 CIRCUIT, $24V_{IN}$,
C_{INH} = C_D = 4.7µF, C_{OUT} = 3 x 100µF,
R_{fSET} = N/A, R_{ISET} = 20kΩ,
C_{TH} = 6.8nF, R_{TH} = 681Ω,
R_{EXTVCC} = N/A, C_{EXTVCC} = N/A,
2A to 4A LOAD STEP AT 2A/µs

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

Start-Up, No Load

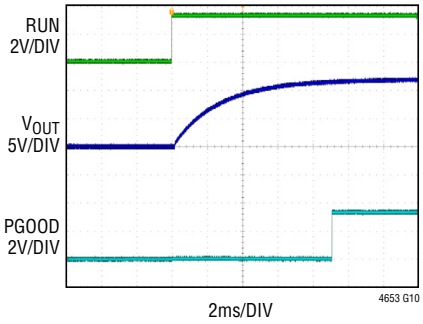


FIGURE 32 CIRCUIT, 48V_{IN},
C_{INH} = C_D = 4.7µF, C_{OUT} = 2 x 22µF,
R_{fSET} = 124k, R_{ISET} = 240kΩ,
R_{PGDFB} = 95.3kΩ,
C_{TH} = 10nF, R_{TH} = 562Ω,
R_{EXTVCC} = 49.9Ω, C_{EXTVCC} = 1µF,
NO LOAD

Start-Up, 4A Load

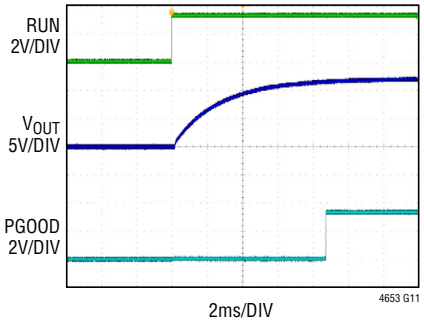


FIGURE 32 CIRCUIT, 48V_{IN},
C_{INH} = C_D = 4.7µF, C_{OUT} = 2 x 22µF,
R_{fSET} = 124k, R_{ISET} = 240kΩ,
R_{PGDFB} = 95.3kΩ,
C_{TH} = 10nF, R_{TH} = 562Ω,
R_{EXTVCC} = 49.9Ω, C_{EXTVCC} = 1µF,
3Ω RESISTIVE LOAD

Start-Up, Pre-Bias

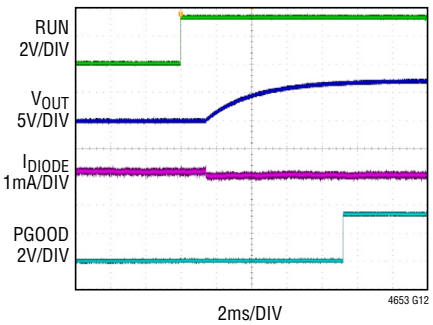


FIGURE 32 CIRCUIT, 48V_{IN},
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R_{fSET} = 124k, R_{ISET} = 240kΩ,
R_{PGDFB} = 95.3kΩ,
C_{TH} = 10nF, R_{TH} = 562Ω,
R_{EXTVCC} = 49.9Ω, C_{EXTVCC} = 1µF,
V_{OUT} PRE-BIASED TO 5V
THROUGH 1N4148 DIODE

Short Circuit, No Load

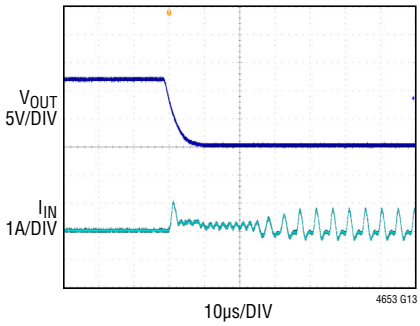


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R_{fSET} = 124k, R_{ISET} = 240kΩ,
R_{PGDFB} = 95.3kΩ,
C_{TH} = 10nF, R_{TH} = 562Ω,
R_{EXTVCC} = 49.9Ω, C_{EXTVCC} = 1µF,
NO LOAD PRIOR TO APPLICATION
OF OUTPUT SHORT-CIRCUIT

Short Circuit, 4A Load

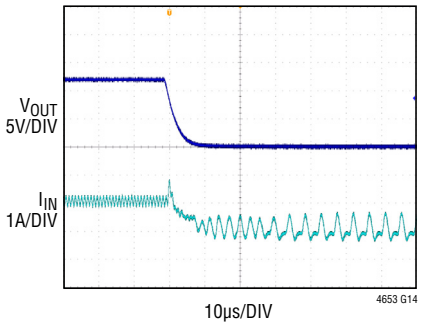


FIGURE 32 CIRCUIT, 48V_{IN},
C_{INH} = C_D = 4.7µF, C_{OUT} = 2 x 22µF,
R_{fSET} = 124k, R_{ISET} = 240kΩ,
R_{PGDFB} = 95.3kΩ,
C_{TH} = 10nF, R_{TH} = 562Ω,
R_{EXTVCC} = 49.9Ω, C_{EXTVCC} = 1µF,
3Ω RESISTIVE LOAD PRIOR TO
APPLICATION OF OUTPUT
SHORT-CIRCUIT

PIN FUNCTIONS

PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG µModule PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY.

V_{IN} (A1-A3, B3): Power Input Pins. Apply input voltage and input decoupling capacitance directly between V_{IN} and a ground (PGND) plane.

V_D (A4, B4, C4): Drain of the Converter's Primary Switching MOSFET. Apply at minimum one 4.7µF high frequency ceramic decoupling capacitor directly from V_D to PGND. Give this capacitor higher layout priority (closer proximity to the module) than any V_{IN} decoupling capacitors.

SV_{IN} (C3): Input Voltage Supply for Small-Signal Circuits. SV_{IN} is the input to the $INTV_{CC}$ LDO. Connect SV_{IN} directly to V_{IN}. No decoupling capacitor is needed on this pin.

PGND (A5, B5, C5, D5, E5, F5, G4-5, H3, H5, J3-5, K4-5, L4-5): Power Ground Pins of the LTM4653. Connect all pins to the application's PGND plane.

V_{OUT} (K1-3, L1-3): Power Output Pins of the LTM4653. Connect all pins to the application's power V_{OUT} plane. Apply the output filter capacitors and the output load between a power V_{OUT} plane and the application's PGND plane.

GND (D4): Ground Pin of the LTM4653. Electrically connect to the application's PGND plane.

V_{OSNS} (G1, H1): Output Voltage Sense and Feedback Signal. Connect V_{OSNS} to V_{OUT} at the point of load (POL). Pins G1 and H1 are electrically connected to each other internal to the module, and thus it is only necessary to connect one V_{OSNS} pin to V_{OUT} at the POL. The remaining V_{OSNS} pin can be used for redundant connectivity or routed to an ICT test point for design-for-test considerations, as desired.

SGND (E4, G2, H2): Signal Ground Pins of the LTM4653. Connect Pin H2 to PGND directly under the LTM4653. The SGND pins at locations E4 and G2 are electrically connected to each other internal to the module, and thus it is only necessary to connect one SGND pin to PGND under the module. The remaining SGND pins can be used for redundant connectivity or routed to an ICT test point for design-for-test considerations, as desired.

RUN (F4): Run Control Pin. A voltage above 1.2V commands the Module to regulate its output voltage. Undervoltage lockout (UVLO) can be implemented by connecting RUN to the midpoint node formed by a resistor-divider between V_{IN} and GND. RUN features 130mV of hysteresis. See the Applications Information section.

$INTV_{CC}$ (G3): Internal Regulator, 3.3V Nominal Output. Internal control circuits and MOSFET-drivers derive power from $INTV_{CC}$ bias. When operating $3.1V < SV_{IN} \leq 58V$, an LDO generates $INTV_{CC}$ from SV_{IN} when RUN is logic high (RUN > 1.2V). No external decoupling is required. When RUN is logic low (RUN - GND < 1.2V), the $INTV_{CC}$ LDO is off, i.e., $INTV_{CC}$ is unregulated. (Also see $EXTV_{CC}$.)

$EXTV_{CC}$ (F3): External Bias, Auxiliary Input to the $INTV_{CC}$ Regulator. When $EXTV_{CC}$ exceeds 3.2V and SV_{IN} exceeds 5V, the $INTV_{CC}$ LDO derives power from $EXTV_{CC}$ bias instead of the SV_{IN} path. This technique can reduce LDO losses considerably, resulting in a corresponding reduction in module junction temperature. For applications in which $4V \leq V_{OUT} \leq 26.5V$, connect $EXTV_{CC}$ to V_{OUT} through a resistor. (See the Applications Information section for resistor value.) When taking advantage of this $EXTV_{CC}$ feature, locally decouple $EXTV_{CC}$ to PGND with a 1µF ceramic—otherwise, leave $EXTV_{CC}$ open circuit.

ISETb (F1): 1.5nF Soft-Start Capacitor. Connect ISETb to ISETa to achieve default soft-start characteristics, if desired. See ISETa.

ISETa (F2): Accurate 50µA Current Source. Positive input to the error amplifier. Connect a resistor (R_{ISET}) from this pin to SGND to program the desired LTM4653 output voltage, $V_{OUT} = R_{ISET} \bullet 50\mu A$. A capacitor can be connected from ISETa to SGND to soft-start the output voltage and reduce start-up inrush current. Connect ISETa to ISETb in order to achieve default soft-start, if desired. (See ISETb.)

In addition, the output of the LTM4653 can track a voltage applied between the ISETa pin and the SGND pins. (See the Applications Information section.)

PIN FUNCTIONS

PGOOD (D1): Power Good Indicator, Open-Drain Output Pin. PGOOD is high impedance when PGDFB is within approximately ±7.5% of 0.6V. PGOOD is pulled to GND when PGDFB is outside this range.

PGDFB (D2): Power Good Feedback Programming Pin. Connect PGDFB to V_{OSNS} through a resistor, R_{PGDFB}. R_{PGDFB} configures the voltage threshold of V_{OUT} for which PGOOD toggles its state. If the PGOOD feature is used, set R_{PGDFB} to:

$$R_{PGDFB} = \left(\frac{V_{OUT}}{0.6V} - 1\right) \bullet 4.99k$$

otherwise, leave PGDFB open circuit.

A small filter capacitor (220pF) internal to the LTM4653 on this pin provides high frequency noise immunity for the PGOOD output indicator.

f_{SET} (E3): Oscillator Frequency Programming Pin. The default switching frequency of the LTM4653 is 400kHz. Often, it is necessary to increase the programmed frequency by connecting a resistor between f_{SET} and SGND. (See the Applications Information section.) Note that the synchronization range of CLKIN is approximately ±40% of the oscillator frequency programmed by the f_{SET} pin.

CLKIN (B1): Mode Select and Oscillator Synchronization Input. Leave CLKIN open circuit for forced continuous mode operation. Alternatively, this pin can be driven to synchronize the switching frequency of the LTM4653 to a clock signal. In this condition, the LTM4653 operates in forced continuous mode and the cycle-by-cycle turn-on of the primary power MOSFET M_T is coincident with the rising edge of the clock applied to CLKIN. Note the synchronization range of CLKIN is approximately ±40% of the oscillator frequency programmed by the f_{SET} pin. (See the Applications Information section.)

COMPa (E2): Current Control Threshold and Error Amplifier Compensation Node. The trip threshold of LTM4653's current comparator increases with a corresponding rise in COMPa voltage. A small filter cap (10pF) internal to the LTM4653 on this pin introduces a high-frequency roll-off of the error-amplifier response, yielding good noise rejection in the control-loop. COMPa is often electrically connected to COMPb in one's application, thus applying default loop compensation. Loop compensation (a series resistor-capacitor) can be applied externally to COMPa if desired or needed, instead. (See COMPb.)

COMPb (E1): Internal Loop Compensation Network. For most applications, the internal, default loop compensation of the LTM4653 is suitable to apply "as is", and yields very satisfactory results: apply the default loop compensation to the control loop by simply connecting COMPa to COMPb. When more specialized applications require a personal touch to the optimization of control loop response, this can be accomplished by connecting a series resistor-capacitor network from COMPa to SGND—and leaving COMPb open circuit.

VINREG (D3): Input Voltage Regulation Programming Pin. Optionally connect this pin to the midpoint node formed by a resistor-divider between V_D and SGND. When the voltage on VINREG falls below approximately 2V, a VINREG control loop servos V_{OUT} to decrease the power inductor current and thus regulate VINREG at 2V. (See the Applications Information section.)

If this input voltage regulation feature is not desired, connect VINREG to $INTV_{CC}$.

IMONa (C2): Power Inductor Current Analog Indicator Pin and Current Limit Programming Pin. The current flowing out of this pin is equal to 1/40,000 of the average power inductor current. To construct a voltage (V_{IMONa}) that is proportional to the power inductor current, optionally apply a parallel resistor-capacitor network to this pin and terminate it to SGND.

IMONa can be connected to IMONb if the default resistor-capacitor termination network provided by IMONb is desired: 1V at full scale (4A) load current. (See IMONb.) If this analog indicator feature is not desired, connect IMONa to SGND.

If IMONa ever exceeds a trip threshold of approximately 2V, an IMON control loop servos V_{OUT} to decrease power inductor current and thus regulate IMONa at 2V. In this manner, the average current limit inception threshold of the LTM4653 can be configured. (See the Applications Information section.)

PIN FUNCTIONS

IMONb (C1): Power Inductor Analog Indicator Current Default Termination R-C Network. A 10kΩ resistor in parallel with a 10nF capacitor and terminating to SGND connect to this pin. Connect IMONb to IMONa to achieve default power inductor analog indicator current characteristics: 1V at full scale (4A) load current. (See IMONa.)

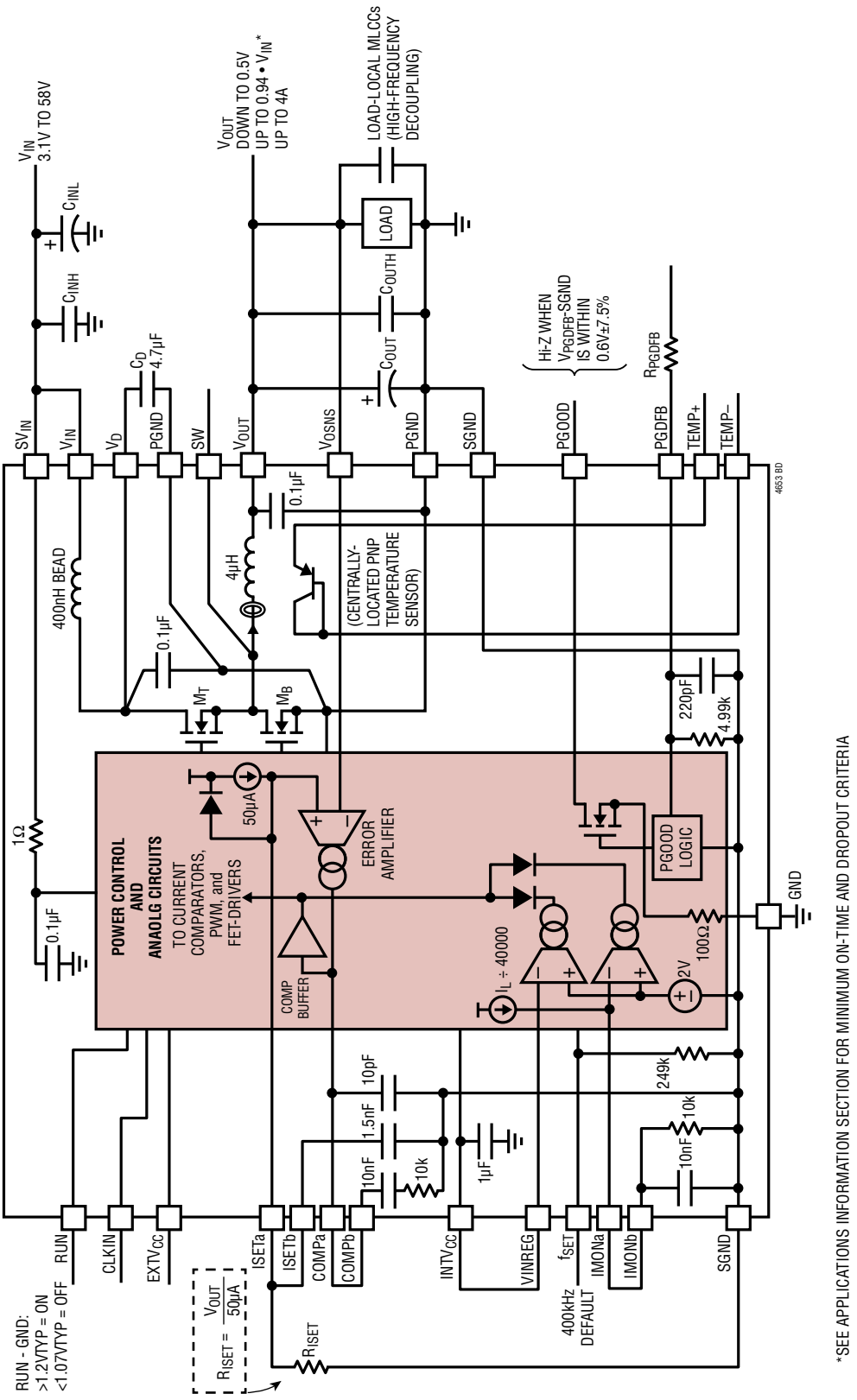
TEMP+ (J1, J6): Temperature Sensor, Positive Input. Emitter of a 2N3906-genre PNP bipolar junction transistor (BJT). Optionally interface to temperature monitoring circuitry such as LTC®2997, LTC2990, LTC2974 or LTC2975. Otherwise leave electrically open. Pins J1 and J6 are electrically connected together internal to the LTM4653, and thus it is only necessary to connect one TEMP+ pin to monitoring circuitry. The remaining TEMP+ pin can be used for redundant connectivity or routed to an ICT test point for design-for-test considerations, as desired.

TEMP– (J2, J7): Temperature Sensor, Negative Input. Collector and base of a 2N3906-genre PNP bipolar junction transistor (BJT). Optionally interface to temperature monitoring circuitry such as LTC2997, LTC2990, LTC2974 or LTC2975. Otherwise leave electrically open. Pins J2 and J7 are electrically connected together internal to the LTM4653, and thus it is only necessary to connect one TEMP– pin to monitoring circuitry. The remaining TEMP– pin can be used for redundant connectivity or routed to an ICT test point for design-for-test considerations, as desired.

SW (H4): Switching Node of Switching Converter Stage. Used for test purposes. May be routed a short distance with a thin trace to a local test point to monitor switching action of the converter, if desired, but do not route near any sensitive signals; otherwise, leave electrically open circuit.

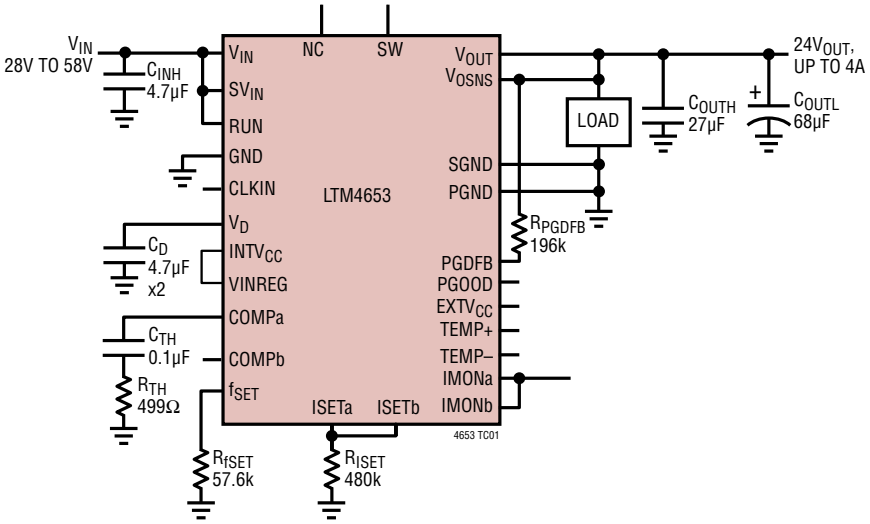
NC (A6-7, B2, B6-7, C6-7, D6-7, E6-7, F6-7, G6-7, H6-7, K6-7, L6-7): No connect pins, i.e., pins with no internal connection. The NC pins predominantly serve to provide improved mounting of the module to the board. In one's layout, NC pins are permitted to remain electrically unconnected or can be connected as desired, e.g., connected to a GND plane for heat-spreading purposes and/or to facilitate routing.

SIMPLIFIED BLOCK DIAGRAM



*SEE APPLICATIONS INFORMATION SECTION FOR MINIMUM ON-TIME AND DROPOUT CRITERIA

TEST CIRCUIT



DECOUPLING REQUIREMENTS

T_A = 25°C. Refer to Test Circuit

APPLICATION	SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Test Circuit	C_{INH}, C_D	External High Frequency Input Capacitor Requirement, 28V ≤ V_{IN} ≤ 58V, V_{OUT} = 24V	I_{OUT} = 4A		9.4		µF
	C_{OUTH}	External High Frequency Output Capacitor Requirement 28V ≤ V_{IN} ≤ 58V, V_{OUT} = 24V	I_{OUT} = 4A		22		µF

OPERATION

Power Module Description

The LTM4653 is a non-isolated switch mode DC/DC step-down power supply. It can provide up to 4A output current with a few external input and output capacitors. Set by a single resistor, R_{ISET}, the LTM4653 regulates a positive output voltage, V_{OUT}. V_{OUT} can be set to as low as 0.5V to as high as $0.94V_{IN}$. The LTM4653 operates from a positive input supply rail, V_{IN}, between 3.1V and 58V. The typical application schematic is shown in Figure 32.

The LTM4653 contains an integrated constant-frequency current mode regulator, power MOSFETs, power inductor, EMI filter and other supporting discrete components. The nominal switching frequency range is from 400kHz to 3MHz, and the default operating frequency is 400kHz. It can be externally synchronized to a clock, from 250kHz to 3MHz. See the Applications Information section. The LTM4653 supports internal and external control loop compensation. Internal loop compensation is selected by connecting the COMPa and COMPb pins. Using internal loop compensation, the LTM4653 has sufficient stability margins and good transient performance with a wide range of output capacitors—even ceramic-only output capacitors. For external loop compensation, see the Applications Information section. LTpowerCAD® is available for transient load step and stability analysis. Input filter and noise cancellation circuitry reduces noise-coupling to the module's inputs and outputs, ensuring the module's electromagnetic interference (EMI) meets the limits of EN55022 Class B (see Figure 6 to Figure 8).

Pulling the RUN pin below 1.2V forces the LTM4653 into a shutdown state. A capacitor can be applied from ISETa to SGND to program the output voltage ramp-rate; or, the default LTM4653 ramp-rate can be set by connecting ISETa to ISETb; or, voltage tracking can be implemented by interfacing rail voltages to the ISETa pin. See the Applications Information section.

Multiphase operation can be employed by applying an external clock source to the LTM4653's synchronization input, the CLKIN pin. See the Typical Applications section.

LDO losses within the module are reduced by connecting $EXTV_{CC}$ to V_{OUT} through an RC-filter or by connecting $EXTV_{CC}$ to a suitable voltage source.

IMONa is an analog output current indicator pin. It sources a current proportional to the LTM4653's load current. When IMONa is electrically connected to IMONb, the voltage on the IMONa/IMONb node is proportional to load current—with 1V corresponding to 4A load. IMONa can be interfaced to an external parallel-RC network instead of the one provided by IMONb. If IMONa ever exceeds 2V, a servo loop reduces the LTM4653's output current in order to keep IMONa at or below 2V. Through this servo mechanism, a parallel RC network can be connected to IMONa to implement an average current limit function—if desired. When the feature is not needed, connect IMONa to SGND.

The LTM4653 also features a spare control pin called VINREG, with a 2V servo threshold, which can be used to reduce the input current draw during input line sag ("brownout") conditions. Connect VINREG to $INTV_{CC}$ when this feature is not needed.

TEMP+ and TEMP– pins give access to a diode-connected PNP transistor, making it possible to monitor the LTM4653's internal temperature—if desired.

External component selection is primarily determined by the maximum load current and output voltage. Refer to Table 7 and the Test Circuit for recommended external component values.

V_{IN} to V_{OUT} Step-Down Ratios

There are restrictions on the V_{IN} to V_{OUT} step-down ratio that the LTM4653 can achieve. The maximum duty cycle of the LTM4653 is 96% typical. The V_{IN} to V_{OUT} minimum dropout voltage is a function of load current when operating in high duty cycle applications. As an example, $V_{OUT(24VDC)}$ from the Electrical Characteristics table highlights the LTM4653's ability to regulate $24V_{OUT}$ at up to 4A from $28V_{IN}$, when running at a switching frequency, f_{SW}, of 1.5MHz.

At very low duty cycles, the LTM4653's on-time of M_T each switching cycle should be designed to exceed the LTM4653 control loop's specified minimum on-time of 60ns, $t_{ON(MIN)}$, (guardband to 90ns), i.e.:

$$\frac{D}{f_{SW}} > T_{ON(MIN)}$$

OPERATION

where D (unitless) is the duty-cycle of M_T, given by:

$$D = \frac{V_{OUT}}{V_{IN}}$$

In rare cases where the minimum on-time restriction is violated, the frequency of the LTM4653 automatically and gradually folds back down to approximately one-fifth of its programmed switching frequency to allow V_{OUT} to remain in regulation. See the Frequency Adjustment section. Be reminded of Notes 2, 3 and 5 in the Electrical Characteristics section regarding output current guidelines.

Input Capacitors

The LTM4653 achieves low input conducted EMI noise due to tight layout and high-frequency bypassing of MOSFETs M_T and M_B within the module itself. A small filter inductor (400nH) is integrated in the input line (from V_{IN} to V_D), providing further noise attenuation—again, local to the switching MOSFETs. The V_D and V_{IN} pins are available for external input capacitors—C_D and C_{INH}—to form a high-frequency π filter. As shown in the Simplified Block Diagram, the ceramic capacitor C_D on the LTM4653's V_D pins handles the majority of the RMS current into the DC/DC converter power stage and requires careful selection, for that reason.

See Figure 6 to Figure 8 for demonstration of LTM4653's EMI performance, meeting the radiated emissions requirements of EN55022B.

The input capacitance, C_D, is needed to filter the pulsed current drawn by M_T. To prevent excessive voltage sag on V_D, a low-effective series resistance (low-ESR, such as an X7R ceramic) input capacitor should be used, sized appropriately for the maximum C_D RMS ripple current:

$$I_{CD(RMS)} = \frac{I_{OUT(MAX)}}{\eta\%} \bullet \sqrt{D \bullet (1-D)}$$

where η% is the estimated efficiency of the power module. (See Typical Performance Characteristics graphs.)

Several capacitors may be paralleled to meet the application's target size, height, and C_D RMS ripple current rating. For lower input voltage applications, sufficient bulk input capacitance is needed to counteract line sag and transient effects during output load changes. The bulk capacitor can be a switcher-rated aluminum electrolytic capacitor or a Polymer capacitor. Suggested values for C_D and C_{INH} are found in Table 7.

A final precaution regarding ceramic capacitors concerns the maximum input voltage rating of the LTM4653's V_{IN}, SV_{IN}, and V_D pins. A ceramic input capacitor combined with trace or cable inductance forms a high Q (underdamped) tank circuit. If the LTM4653 circuit is plugged into a live supply, the input voltage can ring to twice its nominal value, possibly exceeding the device's rating. This situation is easily avoided; see the Hot-Plugging Safely section.

Output Capacitors

Output capacitors C_{OUTH} and C_{OUTL} are applied to V_{OUT} of the LTM4653. Sufficient capacitance and low ESR are called for, to meet the output voltage ripple, loop stability, and transient requirements. C_{OUTL} can be a low ESR tantalum or polymer capacitor. C_{OUTH} is a ceramic capacitor. The typical output capacitance is 22µF (type X5R material, or better), if ceramic-only output capacitors are used.

Table 7 shows a matrix of suggested output capacitors optimized for 2A transient step-loads applied at 2A/µs. Additional output filtering may be required by the system designer, if further reduction of output ripple or dynamic transient spike is required. The LTpowerCAD design tool is available for transient and stability analysis. Stability criteria are considered in the Table 7 matrix, and LTpowerCAD is available for stability analysis. Multiphase operation will reduce effective output ripple as a function of the number of phases. Application Note 77 discusses this noise reduction versus output ripple current cancellation, but the output capacitance should be considered carefully as a function of stability and transient response. LTpowerCAD can be used to calculate the output ripple reduction as the number of implemented phases increases by N times. External loop compensation can be applied to COMPa if needed, for transient response optimization.

Forced Continuous Operation

Leave the CLKIN pin open circuit to command the LTM4653 for forced continuous operation. In this mode, the control loop is allowed to command the inductor peak

OPERATION

current to approximately –1A, allowing for significant negative average current. Clocking the CLKIN pin at a frequency within ±40% of the target switching frequency commanded by the f_{SET} pin synchronizes M_T's turn-on to the rising edge of the CLKIN pin.

Output Voltage Programming, Tracking and Soft-Start

The LTM4653 regulates its output voltage, V_{OUT}, according to the differential voltage present across ISETa and SGND. In most applications, the output voltage is set by simply connecting a resistor, R_{ISET}, from ISETa to SGND, according to:

$$R_{ISET} = \frac{V_{OUT}}{50\mu A}$$

Since the LTM4653 control loop servos its output voltage according to the voltage between ISETa and SGND: placing a capacitor, C_{SS}, parallel to R_{SET} configures the ramp-up rate of ISETa and thus V_{OUT}. In the time domain, the output voltage ramp-up after the RUN pin is toggled from low to high (t = 0s) is given by:

$$V_{OUT}(t) = I_{ISETa} \bullet R_{ISET} \bullet \left(1 - e^{-\frac{t}{R_{ISET} \bullet C_{SS}}}\right)$$

The soft-start time, t_{SS}, is defined as the time it takes for V_{OUT} to ramp from 0V to 90% of its final value:

$$t_{SS} = -R_{ISET} \bullet C_{SS} \bullet \ln(1 - 0.9)$$

or

$$t_{SS} = 2.3 \bullet R_{ISET} \bullet C_{SS}$$

A default value of C_{SS} = 1.5nF can be implemented by connecting ISETa to ISETb. For other ramp-up rates, connect an external C_{SS} capacitor parallel to R_{ISET}. When starting up into a pre-biased V_{OUT}, the LTM4653 stays in a sleep mode, keeping M_T and M_B off until V_{ISETa} equals V_{OSNS}—after which, the DC/DC converter commences switching action and V_{OUT} is ramped according to the voltage commanded by ISETa.

Since the LTM4653 control loop servos its V_{OSNS} voltage to match that of ISETa's, the LTM4653's output can be configured to track any voltage applied to ISETa, referenced to SGND.

Frequency Adjustment

The default switching frequency (f_{SW}) of the LTM4653 is 400kHz. This is suitable for low-V_{IN} ($V_{IN} \le 5V$) applications and low-V_{OUT} ($V_{OUT} \le 3.3V$) applications. For a practical design, the LTM4653's inductor ripple current (ΔI_{PK-PK}) is suggested to be less than ~2A_{PK-PK}. Choose f_{SW} according to:

$$f_{SW} = \frac{V_{OUT} \bullet (1 - D)}{L \bullet \Delta I_{PK-PK}}$$

where the value of LTM4653's power inductor, L, is 4µH.

To avoid cycle-skipping, impose restrictions on f_{SW}, to ensure minimum on time criteria is met:

$$f_{SW} < \frac{D}{T_{ON(MIN)}}$$

The LTM4653's minimum on-time, $t_{ON(MIN)}$, is specified as 60ns. For a practical design, it is recommended to guardband to 90ns.

To configure the LTM4653 for a higher switching frequency than its default of 400kHz, apply a resistor, R_{fSET}, between the f_{SET} pin and SGND. R_{fSET} is given (in MΩ) by:

$$R_{fSET}(M\Omega) = \frac{1}{10pF \bullet [f_{SW}(MHz) - 0.4(MHz)]}$$

The relationship of R_{fSET} to programmed f_{SW} is shown in Figure 1. See Table 7 for recommended f_{SW} and corresponding R_{fSET} values for various combinations of V_{IN} and V_{OUT}.

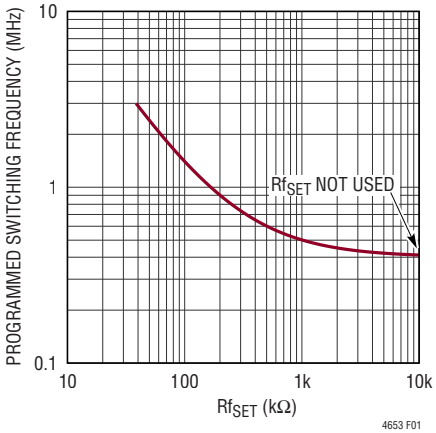


Figure 1. Relationship Between R_{fSET} and Target f_{SW}

APPLICATIONS INFORMATION

Power Module Protection

The LTM4653's current mode control architecture provides fast cycle-by-cycle current limit in an overcurrent condition, as shown in the Typical Performance Characteristics section. If the output voltage collapses sufficiently due to an overload or short-circuit condition, minimum on-time will be violated and the internal oscillator will then fold-back automatically to one-fifth of the LTM4653's programmed switching frequency—thereby reducing the output current and affording the load a chance to recover.

The LTM4653 features input overvoltage shutdown protection: when V_{IN} > 68V, switching action ceases (with 4V of hysteresis)—however, be advised that this protection is only active outside the LTM4653's safe operating area (see Note 1 and Note 4 of the Electrical Characteristics table).

The LTM4653 ceases switching action if internal temperatures exceed 165°C. The control IC resumes operation after a 10°C cool-down hysteresis. Note that these typical parameters are based on measurements in a lab oven and are not production tested. This overtemperature protection is intended to protect the device during momentary overload conditions. The maximum rated junction temperature will be exceeded when this overtemperature protection is active. Continuous operation above the specified absolute maximum operating junction temperature may impair device reliability or permanently damage the device.

The LTM4653 does not feature any specialized output overvoltage protection beyond what is inherent to the control loop's servo mechanism.

RUN Pin Enable

The RUN pin is used to enable the power module or sequence the power module. The threshold is 1.2V. The RUN pin can be used to provide an undervoltage lockout (UVLO) function by connecting a resistor divider from the input supply to the RUN pin, as shown in Figure 2. Undervoltage lockout keeps the LTM4653 in shutdown until the supply input voltage is above a certain voltage programmed by the user. The RUN pin hysteresis voltage

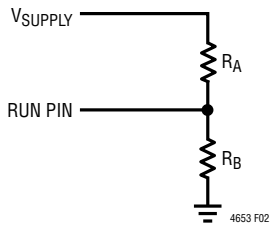


Figure 2. Undervoltage Lockout Resistive Divider

prevents noise from falsely tripping UVLO. Resistors are chosen by first selecting R_B (refer to Figure 2). Then:

$$R_A = R_B \bullet \left(\frac{V_{IN(ON)}}{1.2V} - 1 \right)$$

where $V_{IN(ON)}$ is the input voltage at which the undervoltage lockout is overcome and the supply turns on. R_A may be replaced with a hardwired connection from V_D to RUN. The V_{IN} turn-off voltage, $V_{IN(OFF)}$ is given by:

$$V_{IN(OFF)} = 1.07V \bullet \left(\frac{R_A}{R_B} + 1 \right)$$

If UVLO is not needed, RUN can be connected to LTM4653's V_D or V_{IN} pins.

When RUN is below its threshold, UVLO is engaged, M_T and M_B are turned off, $INTV_{CC}$ ceases to be regulated, and ISETa is discharged to SGND by internal circuitry.

Loop Compensation

External loop compensation may be preferred for some applications and can be implemented easily, as follows: leave COMPb open circuit; connect a series-R_C network (R_{TH} and C_{TH}) from COMPa to SGND; in some instances, connect a capacitor (C_{THP}) from COMPa to SGND (paralleling the R_{TH-CTH} series-RC network). See Table 7 for suggested input and output capacitances for a variety of operating conditions. Additionally, the LTpowerCAD design tool is available for transient and stability analysis.

APPLICATIONS INFORMATION

Hot-Plugging Safely

The small size, robustness and low impedance of ceramic capacitors make them an attractive option for the input bypass capacitors (C_D and C_{INH}) of the LTM4653. However, these capacitors can cause problems if the LTM4653 is plugged into a live supply (see Analog Devices Application Note 88 for a complete discussion). The low loss ceramic capacitor combined with stray inductance in series with the power source forms an under damped tank circuit, and the voltage at the V_{IN} pin of the LTM4653 can ring to twice the nominal input voltage, possibly exceeding the LTM4653's rating and damaging the part. If the input supply is poorly controlled or the user will be plugging the LTM4653 into an energized supply, the input network should be designed to prevent this overshoot by introducing a damping element into the path of current flow. This is often done by adding an inexpensive electrolytic bulk capacitor (C_{INL}) across the input terminals of the LTM4653. The selection criteria for C_{INL} calls for: an ESR high enough to damp the ringing; a capacitance value several times larger than C_{INH}. C_{INL} does not need to be located physically close to the LTM4653; it should be located close to the application board's input connector, instead.

Input Disconnect/Input Short Considerations

If at any point the input supply is removed with the output voltage still held high through its capacitor, power will be drawn from the output capacitor to power the module, until the output voltage drops below the minimum SV_{IN}/V_{IN} requirements of the module.

However, if the SV_{IN}/V_{IN} pins are grounded while the output is held high, regardless of the RUN state, parasitic body diodes inside the LTM4653 will pull current from the output through the V_{OUT} pins. Depending on the size of the output capacitor and the resistivity of the short, high currents may flow through the internal body diode, and cause damage to the part. If discharge of SV_{IN}/V_{IN} by the input source is possible, preventative measures should be taken to prevent current flow through the internal body diode. Simple solutions would be placing a Schottky diode in series with the supply (Figure 3), or placing a Schottky diode from V_{OUT} to SV_{IN}/V_{IN} (Figure 4). Applications with loads that experience large load-step release, load dump or other mechanisms that invoke reverse energy flow in the Figure 3 circuit may need a suitably-rated Zener diode protection clamp, to limit the resulting transient voltage rise on SV_{IN}/V_{IN} and C_{IN}.

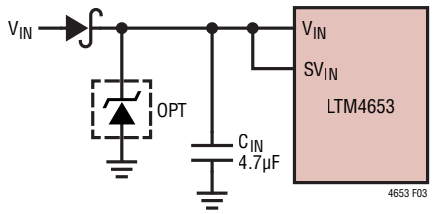


Figure 3. Schottky Diode in Series with the Supply

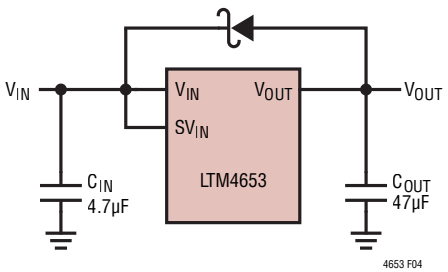


Figure 4. Schottky Diode from V_{OUT} to V_{IN}

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$INTV_{CC}$ and $EXTV_{CC}$ Connection

When RUN is logic high, an internal low dropout regulator regulates an internal supply, $INTV_{CC}$, that powers the control circuitry for driving LTM4653's internal MOSFETs. $INTV_{CC}$ is regulated at 3.3V. In this manner, the LTM4653's $INTV_{CC}$ is directly powered from SV_{IN}, by default. The gate driver current through the LDO is about 20mA for a typical 1MHz application. The internal LDO power dissipation can be calculated as:

$$P_{LDO_LOSS(INTVCC)} = 20mA \bullet (SV_{IN} - 3V)$$

The LDO draws current off of $EXTV_{CC}$ instead of SV_{IN} when $EXTV_{CC}$ is higher than 3.2V and SV_{IN} is above 5V. For output voltages of 4V and higher, $EXTV_{CC}$ can be connected to V_{OUT} through an RC-filter. When the internal LDO derives power from $EXTV_{CC}$ instead of SV_{IN}, the internal LDO power dissipation is:

$$P_{LDO_LOSS(EXTVCC)} = 20mA \bullet (V_{OUT} - 3V)$$

The recommended value of the resistor between V_{OUT} and $EXTV_{CC}$ is roughly V_{OUT} • 4Ω/V. This resistor, R_{EXTVCC}, must be rated to continually dissipate $(0.02A)^2 \bullet R_{EXTVCC}$. The primary purpose of this resistor is to prevent $EXTV_{CC}$ overstress under a fault condition. For example, when an inductive short-circuit is applied to the module's output, V_{OUT} may be briefly dragged below PGND—forward biasing the PGND-to-$EXTV_{CC}$ body diode. This resistor limits the magnitude of current flow in $EXTV_{CC}$. Bypass $EXTV_{CC}$ with 1µF of X5R (or better) MLCC.

Multiphase Operation

Multiple LTM4653 devices can be paralleled for higher output current applications. For lowest input and output voltage and current ripples, it is advisable to synchronize paralleled LTM4653s to an external clock (within ±40% of the target switching frequency set by f_{SET}—see Test Circuit 1). See Figure 34 for an example of a synchronizing circuit.

LTM4653 modules can be paralleled without synchronizing circuits: just be aware that some beat-frequency ripple will be present in the output voltage and reflected input current by virtue of the fact that such modules are not operating at identical, synchronized switching frequencies.

The LTM4653 device is an inherently current mode controlled device, so parallel modules will have good current sharing's shown in Figure 35. This helps balance the thermals on the design.

To parallel LTM4653s, connect the respective COMPa, ISETa, and V_{OSNS} pins of each LTM4653 together to share the current evenly. In addition, tie the respective RUN pins of paralleled LTM4653 devices together, to ensure proper start-up and shutdown behavior. Figure 34 shows a schematic of LTM4653 devices operating in parallel.

Note that for parallel applications, V_{OUT} can be set by a single, common resistor on the ISETa net:

$$R_{ISET} = \frac{V_{OUT}}{50\mu A \bullet N}$$

where N is the number of LTM4653 modules in parallel configuration.

Depending on the duty cycle of operation, the output voltage ripple achieved by paralleled, synchronized LTM4653 modules may be considerably smaller than what is yielded by a single-phase solution. Application Note 77 provides a detailed explanation of multiphase operation (relevant to parallel LTM4653 applications) pertaining to noise reduction and output and input ripple current cancellation. Regardless of ripple current cancellation, it remains important for the output capacitance of paralleled LTM4653 applications to be designed for loop stability and transient response. LTpowerCAD is available for such analysis.

Figure 5 illustrates the RMS ripple current reduction as a function of the number of interleaved (paralleled and synchronized) LTM4653 modules—derived from Application Note 77.

Radiated EMI Noise

The generation of radiated EMI noise is an inherent disadvantage of switching regulators. Fast switching turn-on and turn-off of the power MOSFETs—necessary

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for achieving high efficiency—create high-frequency (~30MHz+) $\Delta I/\Delta t$ changes within DC/DC converters. This activity tends to be the dominant source of high-frequency EMI radiation in such systems. The high level of device integration within LTM4653—including optimized gate-driver and critical front-end π filter inductor—delivers low radiated EMI noise performance. Figure 6 to Figure 8 show typical examples of LTM4653 meeting the radiated emission limits established by EN55022 Class B.

Thermal Considerations and Output Current Derating

The thermal resistances reported in the Pin Configuration section of this data sheet are consistent with those parameters defined by JESD51-12 and are intended for use with finite element analysis (FEA) software modeling tools that leverage the outcome of thermal modeling, simulation, and correlation to hardware evaluation performed on a µModule package mounted to a hardware test board. The motivation for providing these thermal coefficients is found in JESD51-12 ("Guidelines for Reporting and Using Electronic Package Thermal Information").

Many designers may opt to use laboratory equipment and a test vehicle such as the demo board to predict the µModule regulator's thermal performance in their application at various electrical and environmental operating conditions to compliment any FEA activities. Without FEA software, the thermal resistances reported in the Pin Configuration section are, in and of themselves, not relevant to providing guidance of thermal performance; instead, the derating curves provided in this data sheet can be used in a manner that yields insight and guidance pertaining to one's application-usage, and can be adapted to correlate thermal performance to one's own application.

The Pin Configuration section gives four thermal coefficients explicitly defined in JESD51-12; these coefficients are quoted or paraphrased below:

1. θ_{JA}, the thermal resistance from junction to ambient, is the natural convection junction-to-ambient air thermal resistance measured in a one cubic foot sealed enclosure. This environment is sometimes referred to as "still air" although natural convection causes the air to move. This value is determined with the part mounted to a JESD51-9 defined test board, which does not reflect an actual application or viable operating condition.

2. $\theta_{JCbottom}$, the thermal resistance from junction to the bottom of the product case, is determined with all of the component power dissipation flowing through the bottom of the package. In the typical µModule regulator, the bulk of the heat flows out the bottom of the package, but there is always heat flow out into the ambient environment. As a result, this thermal resistance value may be useful for comparing packages but the test conditions don't generally match the user's application.

3. θ_{JCtop}, the thermal resistance from junction to top of the product case, is determined with nearly all of the component power dissipation flowing through the top of the package. As the electrical connections of the typical µModule regulator are on the bottom of the package, it is rare for an application to operate such that most of the heat flows from the junction to the top of the part. As in the case of $\theta_{JCbottom}$, this value may be useful for comparing packages but the test conditions don't generally match the user's application.

4. θ_{JB}, the thermal resistance from junction to the printed circuit board, is the junction-to-board thermal resistance where almost all of the heat flows through the bottom of the µModule regulator and into the board, and is really the sum of the $\theta_{JCbottom}$ and the thermal resistance of the bottom of the part through the solder joints and through a portion of the board. The board temperature is measured a specified distance from the package, using a two sided, two layer board. This board is described in JESD51-9.

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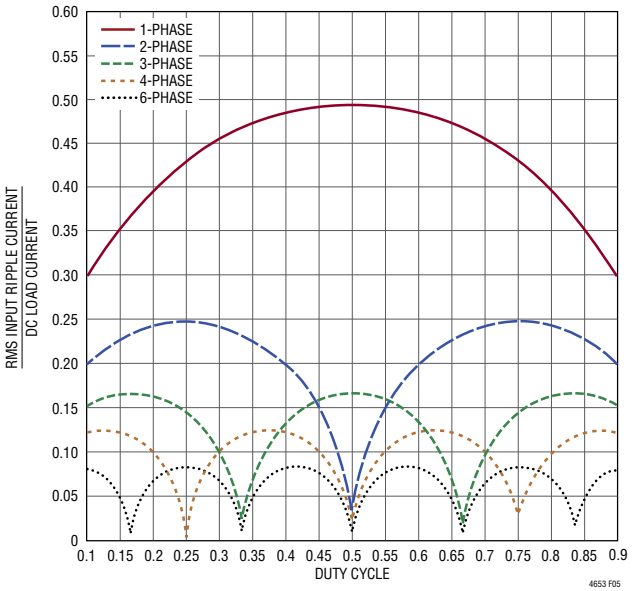


Figure 5. Normalized Input RMS Ripple Current vs Duty Cycle for One to Six LTM4653s (Phases)

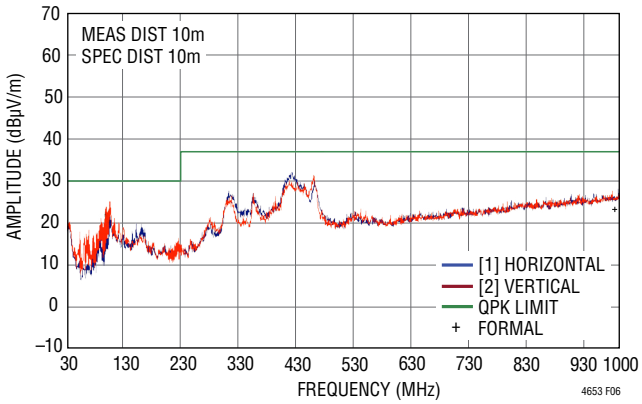


Figure 6. Radiated Emissions Scan of the LTM4653. Producing 24V_{OUT} at 4A, from 29.5V_{IN}. DC2327A Hardware. f_{SW} = 1.2MHz. Measured in a 10m Chamber. Peak Detect Method

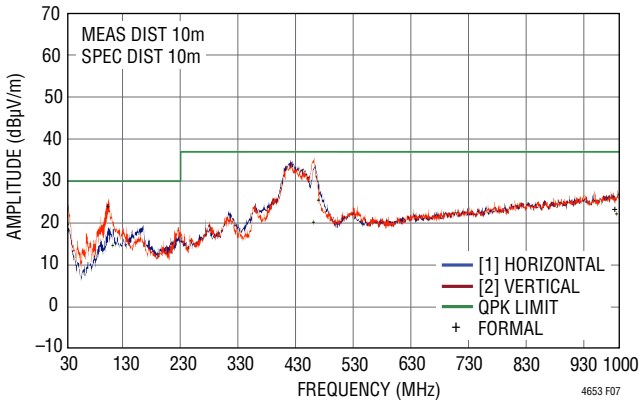


Figure 7. Radiated Emissions Scan of the LTM4653 Producing 24V_{OUT} at 3.5A, from 48V_{IN}. DC2327A Hardware. f_{SW} = 1.2MHz. Measured in a 10m Chamber. Peak Detect Method

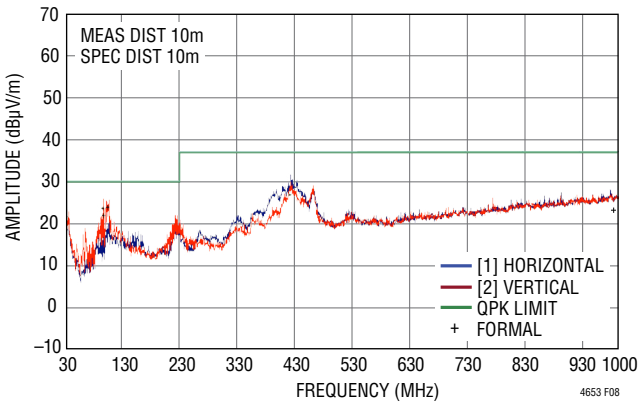


Figure 8. Radiated Emissions Scan of the LTM4653. Producing 12V_{OUT} at 3A, from 58V_{IN}. DC2327A Hardware. f_{SW} = 1.2MHz. Measured in a 10m Chamber. Peak Detect Method

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A graphical representation of the aforementioned thermal resistances is given in Figure 9; blue resistances are contained within the µModule regulator, whereas green resistances are external to the µModule package.

As a practical matter, it should be clear to the reader that no individual or sub-group of the four thermal resistance parameters defined by JESD51-12 or provided in the Pin Configuration section replicates or conveys normal operating conditions of a µModule regulator. For example, in normal board-mounted applications, never does 100% of the device's total power loss (heat) thermally conduct exclusively through the top or exclusively through bottom of the µModule package—as the standard defines for θ_{JCtop} and $\theta_{JCbottom}$, respectively. In practice, power loss is thermally dissipated in both directions away from the package—granted, in the absence of a heat sink and airflow, a majority of the heat flow is into the board.

Within the LTM4653, be aware there are multiple power devices and components dissipating power, with a consequence that the thermal resistances relative to different junctions of components or die are not exactly linear with respect to total package power loss. To reconcile this complication without sacrificing modeling simplicity—but also not ignoring practical realities—an approach has been taken using FEA software modeling along with laboratory testing in a controlled-environment chamber to reasonably define and correlate the thermal resistance values supplied in this data sheet: (1) Initially, FEA software is used to accurately build the mechanical geometry of the LTM4653 and the specified PCB with all of the correct material coefficients along with accurate power loss source definitions; (2) this model simulates a software-defined JEDEC environment consistent with JESD51-9 and JESD51-12 to predict power loss heat flow and temperature readings at different interfaces that enable the calculation of the JEDEC-defined thermal resistance values; (3) the model and FEA software is used to evaluate the LTM4653 with heat sink and airflow; (4) having solved for and analyzed these thermal resistance values and simulated various operating conditions in the software model, a thorough laboratory evaluation replicates the simulated conditions with thermocouples within a controlled environment chamber while operating the device at the same power loss as that which was simulated. The outcome of this process and due diligence yields the set of derating curves provided in later sections of this data sheet, along with well-correlated JESD51-12-defined θ values provided in the Pin Configuration section of this data sheet.

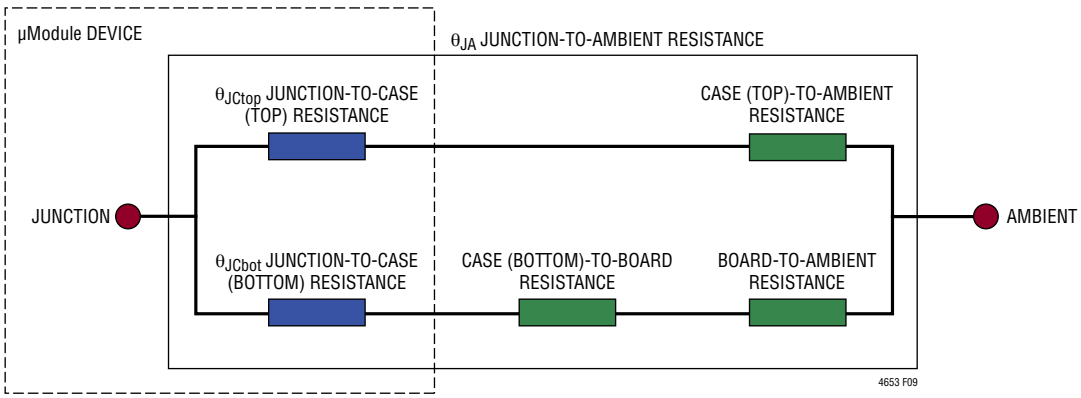


Figure 9. Graphical Representation of JESD51-12 Thermal Coefficients

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The 1V, 5V, and 15V and 24V power loss curves in Figure 10, Figure 11 and Figure 12 respectively can be used in coordination with the load current derating curves in Figure 13 to Figure 30 for calculating an approximate θ_{JA} thermal resistance for the LTM4653 with various heat sinking and air flow conditions. These thermal resistances represent demonstrated performance of the LTM4653 on DC2327A hardware; a 4-layer FR4 PCB measuring 99mm × 133mm × 1.6mm using outer and inner copper weights of 2oz and 1oz, respectively. The power loss curves are taken at room temperature, and are increased with multiplicative factors with ambient temperature. These approximate factors are listed in Table 1. (Compute the factor by interpolation, for intermediate temperatures.) The derating curves are plotted with the LTM4653's output initially sourcing 4A and the ambient temperature at 20°C. The output voltages are 1V, 5V, 15V and 24V. These are chosen to include the lower and higher output voltage ranges for correlating the thermal resistance. In all derating curves, the switching frequency of operation follows guidance provided by Table 7. Thermal models are derived from several temperature measurements in a controlled temperature chamber along with thermal modeling analysis. The junction temperatures are monitored while ambient temperature is increased with and without air flow, and with and without a heat sink attached with thermally conductive adhesive tape. The power loss increase with ambient temperature change is factored into the derating curves. The junctions are maintained at 120°C maximum while lowering output current or power while increasing ambient temperature. The decreased output current decreases the internal module loss as ambient temperature is increased. The monitored junction temperature of 120°C minus the ambient operating temperature specifies how much module temperature rise can be allowed. As an example in Figure 27, the load current is derated to 2.5A at 70°C ambient with 200LFM airflow and no heat sink and the room temperature (25°C) power loss for this $48V_{IN}$ to $24V_{OUT}$ at $2.5A_{OUT}$ condition is 3.9W. A 4.5W loss is calculated by multiplying the 3.9W room temperature loss from the $48V_{IN}$ to $24V_{OUT}$ power loss curve at 2.5A (Figure 12), with the 1.15 multiplying factor at 70°C ambient (from Table 1). If the 70°C ambient temperature is subtracted from the 120°C junction temperature, then the difference of 50°C divided by 4.5W yields a thermal resistance, θ_{JA}, of 11.1°C/W—in good agreement with Table 4. Tables 2, 3 and 4 provide equivalent thermal resistances for 1V, 5V and 15V and 24V outputs with and without air flow and heat sinking. The derived thermal resistances in Tables 2, 3 and 4 for the various conditions can be multiplied by the calculated power loss as a function of ambient temperature to derive temperature rise above ambient, thus maximum junction temperature. Room temperature power loss can be derived from the efficiency curves in the Typical Performance Characteristics section and adjusted with ambient temperature multiplicative factors from Table 1.

Table 1. Power Loss Multiplicative Factors vs Ambient Temperature

AMBIENT TEMPERATURE	POWER LOSS MULTIPLICATIVE FACTOR
Up to 40°C	1.00
50°C	1.05
60°C	1.10
70°C	1.15
80°C	1.20
90°C	1.25
100°C	1.30
110°C	1.35
120°C	1.40

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Table 2. 1V Output

DERATING CURVE	V_{IN} (V)	POWER LOSS CURVE	AIRFLOW (LFM)	HEAT SINK	θ_{JA} (°C/W)
Figure 13, Figure 14, Figure 15	5, 12, 24	Figure 10, Figure 11	0	None	13.9
Figure 13, Figure 14, Figure 15	5, 12, 24	Figure 10, Figure 11	200	None	11.4
Figure 13, Figure 14, Figure 15	5, 12, 24	Figure 10, Figure 11	400	None	10.7
Figure 16, Figure 17, Figure 18	5, 12, 24	Figure 10, Figure 11	0	BGA Heat Sink	13.3
Figure 16, Figure 17, Figure 18	5, 12, 24	Figure 10, Figure 11	200	BGA Heat Sink	11.0
Figure 16, Figure 17, Figure 18	5, 12, 24	Figure 10, Figure 11	400	BGA Heat Sink	10.3

Table 3. 5V Output

DERATING CURVE	V_{IN} (V)	POWER LOSS CURVE	AIRFLOW (LFM)	HEAT SINK	θ_{JA} (°C/W)
Figure 19, Figure 20, Figure 21	12, 24, 48	Figure 10, Figure 11, Figure 12	0	None	13.9
Figure 19, Figure 20, Figure 21	12, 24, 48	Figure 10, Figure 11, Figure 12	200	None	11.4
Figure 19, Figure 20, Figure 21	12, 24, 48	Figure 10, Figure 11, Figure 12	400	None	10.7
Figure 22, Figure 23, Figure 24	12, 24, 48	Figure 10, Figure 11, Figure 12	0	BGA Heat Sink	13.3
Figure 22, Figure 23, Figure 24	12, 24, 48	Figure 10, Figure 11, Figure 12	200	BGA Heat Sink	11.0
Figure 22, Figure 23, Figure 24	12, 24, 48	Figure 10, Figure 11, Figure 12	400	BGA Heat Sink	10.3

Table 4. 15V and 24V Output

DERATING CURVE	V_{IN} (V)	POWER LOSS CURVE	AIRFLOW (LFM)	HEAT SINK	θ_{JA} (°C/W)
Figure 25, Figure 26, Figure 27	24, 48	Figure 11, Figure 12	0	None	13.9
Figure 25, Figure 26, Figure 27	24, 48	Figure 11, Figure 12	200	None	11.4
Figure 25, Figure 26, Figure 27	24, 48	Figure 11, Figure 12	400	None	10.7
Figure 28, Figure 29, Figure 30	24, 48	Figure 11, Figure 12	0	BGA Heat Sink	13.3
Figure 28, Figure 29, Figure 30	24, 48	Figure 11, Figure 12	200	BGA Heat Sink	11.0
Figure 28, Figure 29, Figure 30	24, 48	Figure 11, Figure 12	400	BGA Heat Sink	10.3

Table 5. Heat Sink Manufacturer (Thermally Conductive Adhesive Tape Pre-Attached)

HEAT SINK MANUFACTURER	PART NUMBER	WEBSITE
Cool Innovations	3-0504035UT411	www.coolinnovations.com

Table 6. Thermally Conductive Adhesive Tape Vendor

THERMALLY CONDUCTIVE ADHESIVE TAPE MANUFACTURER	PART NUMBER	WEBSITE
Chomerics	T411	www.chomerics.com

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Table 7. LTM4653 Output Voltage Response vs Component Matrix. Performance of Figure 32 Circuit with Values Here Indicated. Load-Stepping from 2A to 4A Load Current, at 2A/µs. Typical Measured Values

C_{OUTH} VENDORS	PART NUMBER	C_{OUTH} VENDORS	PART NUMBER
AVX	12066D107MAT2A (100µF, 6.3V, 1206 Case Size)	AVX	12105D106MAT2A (10µF, 50V, 1210 Case Size)
Murata	GRM31CR60J107M (100µF, 6.3V, 1206 Case Size)	Murata	GRM32ER61H106M (10µF, 50V, 1210 Case Size)
Taiyo Yuden	JMK316BBJ107MLHT (100µF, 6.3V, 1206 Case Size)	Taiyo Yuden	UMK325BJ106M (10µF, 50V, 1210 Case Size)
TDK	C3216X5R0J107M (100µF, 6.3V, 1206 Case Size)	TDK	C3225X5R1H106M (10µF, 50V, 1210 Case Size)
AVX	1210YD476MAT2A (47µF, 16V, 1210 Case Size)	C_{INH}/C_D VENDORS	PART NUMBER
Murata	GRM32ER61C476M (47µF, 16V, 1210 Case Size)	Murata	GRM32ER71K475M (4.7µF, 80V, 1210 Case Size)
Taiyo Yuden	EMK325BJ476MM (47µF, 16V, 1210 Case Size)	AVX	12065C475MAT2A (4.7µF, 50V, 1206 Case Size)
AVX	12103D226MAT2A (22µF, 25V, 1210 Case Size)	Murata	GRM31CR71H475M (4.7µF, 50V, 1206 Case Size)
Taiyo Yuden	TMK325BJ226MM (22µF, 25V, 1210 Case Size)	Taiyo Yuden	UMK316AB7475ML (4.7µF, 50V, 1206 Case Size)
TDK	C3225X5R1E226M (22µF, 25V, 1210 Case Size)	TDK	C3216X5R1H475M (4.7µF, 50V, 1206 Case Size)

V_{OUT} (V)	V_{IN} (V)	C_{INH}	C_D	C_{OUTH}	R_{TH} (Ω)	C_{TH} (nF)	R_{ISET} (kΩ)	R_{PGDFB} (kΩ)	f_{SW} (kHz)	R_{ISET} (kΩ)	R_{EXTVCC} (Ω)	LOAD STEP TRANSIENT DROOP (mV)	LOAD STEP PK-PK DEVIATION (mV)	RECOVERY TIME (µs)
1	5	4.7µF	4.7µF	100µF x 3	681	6.8	20	3.32	400	N/A	N/A	70	145	55
1	12	4.7µF	4.7µF	100µF x 3	681	6.8	20	3.32	400	N/A	N/A	70	145	50
1	24	4.7µF	4.7µF	100µF x 3	681	6.8	20	3.32	400	N/A	N/A	70	145	50
1.2	5	4.7µF	4.7µF	100µF x 3	665	6.8	24	4.99	400	N/A	N/A	70	145	50
1.2	12	4.7µF	4.7µF	100µF x 3	665	6.8	24	4.99	400	N/A	N/A	70	145	50
1.2	24	4.7µF	4.7µF	100µF x 3	665	6.8	24	4.99	400	N/A	N/A	70	145	50
1.5	5	4.7µF	4.7µF	100µF x 3	665	6.8	30.1	7.5	400	N/A	N/A	70	145	50
1.5	12	4.7µF	4.7µF	100µF x 3	665	6.8	30.1	7.5	400	N/A	N/A	70	145	50
1.5	24	4.7µF	4.7µF	100µF x 3	665	6.8	30.1	7.5	400	N/A	N/A	70	145	50
1.5	36	4.7µF	4.7µF	100µF x 3	665	6.8	30.1	7.5	400	N/A	N/A	70	145	50
1.8	5	4.7µF	4.7µF	100µF x 3	665	8.2	36	10	400	N/A	N/A	70	145	50
1.8	12	4.7µF	4.7µF	100µF x 3	665	8.2	36	10	400	N/A	N/A	70	145	50
1.8	24	4.7µF	4.7µF	100µF x 3	665	8.2	36	10	400	N/A	N/A	70	145	50
1.8	36	4.7µF	4.7µF	100µF x 3	665	8.2	36	10	400	N/A	N/A	70	145	50
2.5	5	4.7µF	4.7µF	100µF x 3	649	8.2	50	15.8	400	N/A	N/A	70	145	50
2.5	12	4.7µF	4.7µF	100µF x 3	649	8.2	50	15.8	400	N/A	N/A	70	145	50
2.5	24	4.7µF	4.7µF	100µF x 3	649	8.2	50	15.8	400	N/A	N/A	70	145	50
2.5	36	4.7µF	4.7µF	100µF x 3	649	8.2	50	15.8	400	N/A	N/A	70	145	50
2.5	48	4.7µF	4.7µF	100µF x 3	649	8.2	50	15.8	400	N/A	N/A	70	145	50
3.3	5	4.7µF	4.7µF	100µF x 2	604	10	66.5	22.6	400	N/A	N/A	90	190	50
3.3	12	4.7µF	4.7µF	100µF x 2	604	10	66.5	22.6	400	N/A	N/A	90	190	50
3.3	24	4.7µF	4.7µF	100µF x 2	604	10	66.5	22.6	400	N/A	N/A	90	185	50
3.3	36	4.7µF	4.7µF	100µF x 2	604	10	66.5	22.6	400	N/A	N/A	90	180	50
3.3	48	4.7µF	4.7µF	100µF x 2	604	10	66.5	22.6	400	N/A	N/A	90	180	50
5	12	4.7µF	4.7µF	47µF x 2	499	10	100	36.5	400	N/A	20	130	260	45
5	24	4.7µF	4.7µF	47µF x 2	499	10	100	36.5	550	665	20	130	260	45
5	36	4.7µF	4.7µF	47µF x 2	499	10	100	36.5	575	576	20	130	260	45
5	48	4.7µF	4.7µF	47µF x 2	499	10	100	36.5	600	499	20	130	260	45
12	15	4.7µF	4.7µF	22µF x 2	499	10	240	95.3	500	1000	49.9	170	350	40
12	24	4.7µF	4.7µF	22µF x 2	499	10	240	95.3	800	249	49.9	170	350	40
12	36	4.7µF	4.7µF	22µF x 2	499	10	240	95.3	1100	143	49.9	170	350	40
12	48	4.7µF	4.7µF	22µF x 2	499	10	240	95.3	1200	124	49.9	170	350	40
15	24	4.7µF	4.7µF	22µF x 2	499	10	301	121	750	287	60.4	170	350	40
15	36	4.7µF	4.7µF	22µF x 2	499	10	301	121	1200	124	60.4	170	350	40
15	48	4.7µF	4.7µF	22µF x 2	499	10	301	121	1400	100	60.4	170	350	40
24	36	4.7µF	4.7µF	10µF x 2	499	10	481	196	1200	124	100	220	430	35
24	48	4.7µF	4.7µF	10µF x 2	499	10	481	196	1500	90.9	100	220	440	35

APPLICATIONS INFORMATION—DERATING CURVES

See Table 1 for f_{SW} and R_{EXTVCC}.

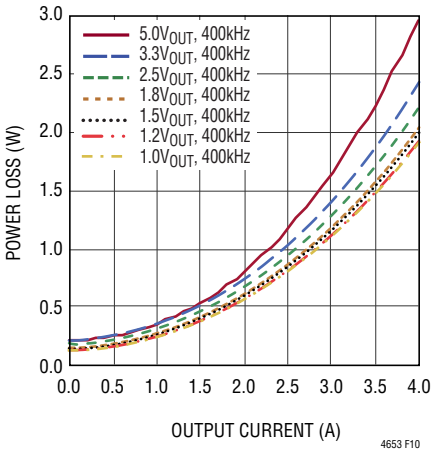


Figure 10. $12V_{IN}$ Power Loss Curve

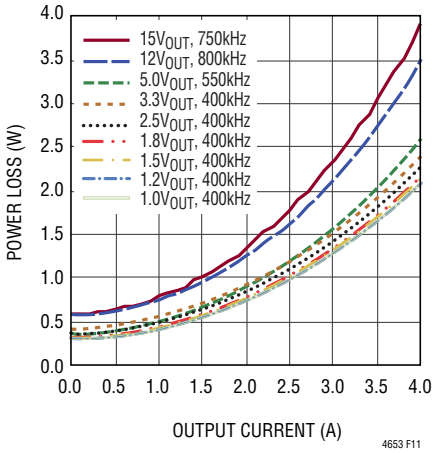


Figure 11. $24V_{IN}$ Power Loss Curve

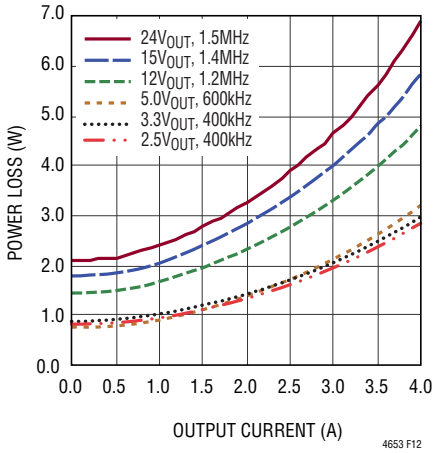


Figure 12. $48V_{IN}$ Power Loss Curve

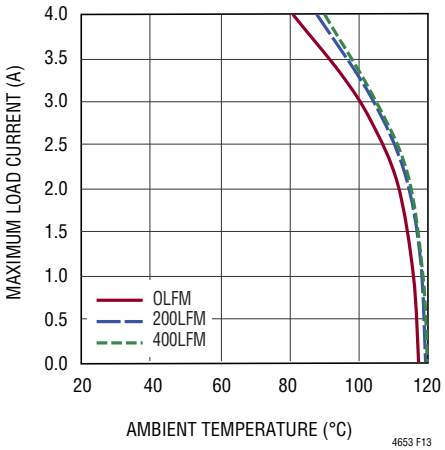


Figure 13. 5V to $1V_{OUT}$ Derating Curve, No Heat Sink

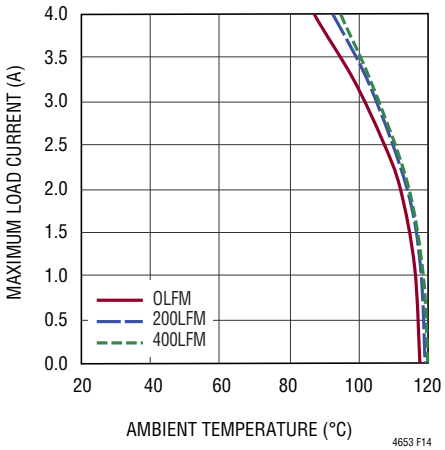


Figure 14. 12V to $1V_{OUT}$ Derating Curve, No Heat Sink

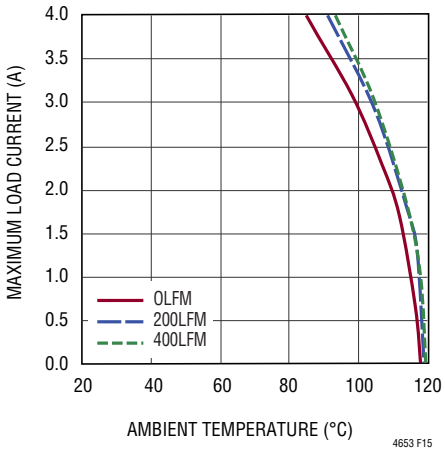


Figure 15. 24V to $1V_{OUT}$ Derating Curve, No Heat Sink

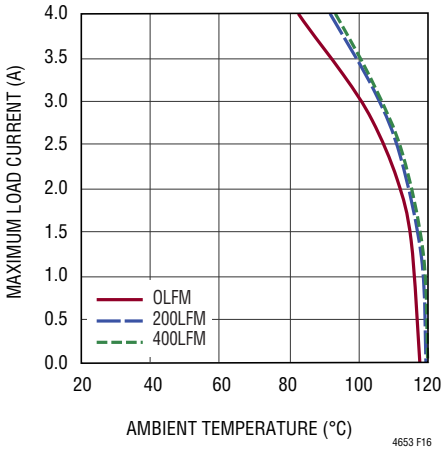


Figure 16. 5V to $1V_{OUT}$ Derating Curve, with BGA Heat Sink

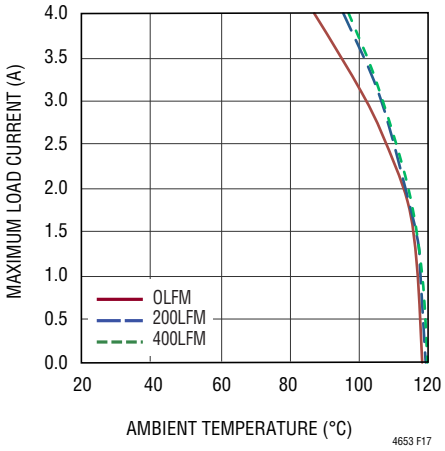


Figure 17. 12V to $1V_{OUT}$ Derating Curve, with BGA Heat Sink

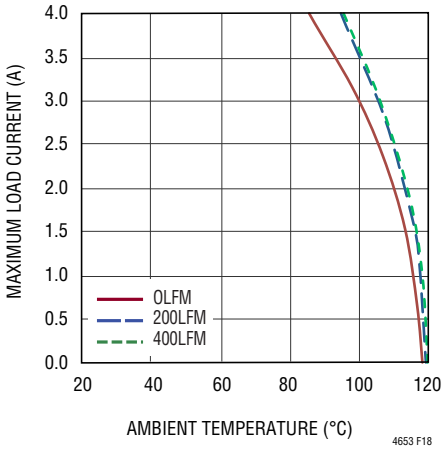


Figure 18. 24V to $1V_{OUT}$ Derating Curve, with BGA Heat Sink

APPLICATIONS INFORMATION—DERATING CURVES

See Table 1 for f_{SW} and R_{EXTVCC}.

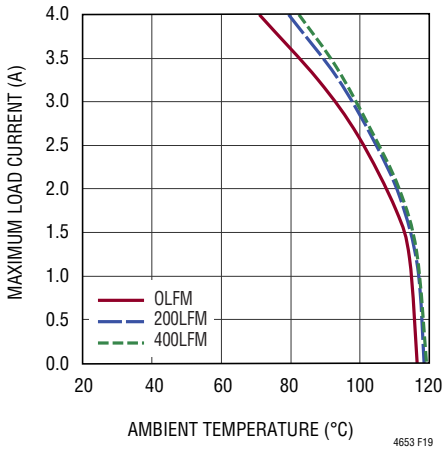


Figure 19. 12V to 5V_{OUT} Derating Curve, No Heat Sink

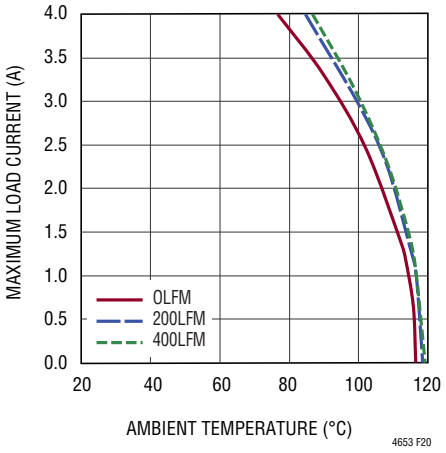


Figure 20. 24V to 5V_{OUT} Derating Curve, No Heat Sink

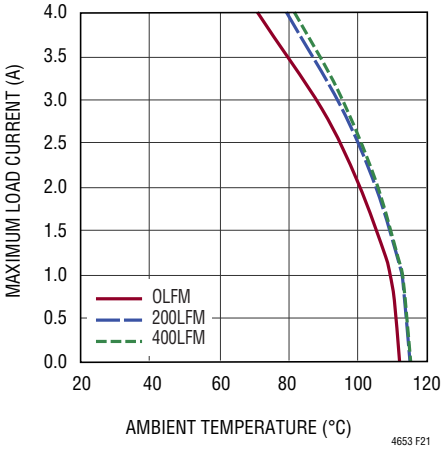


Figure 21. 48V to 5V_{OUT} Derating Curve, No Heat Sink

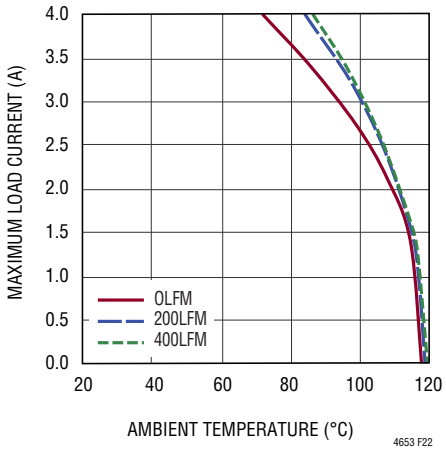


Figure 22. 12V to 5V_{OUT} Derating Curve, with BGA Heat Sink

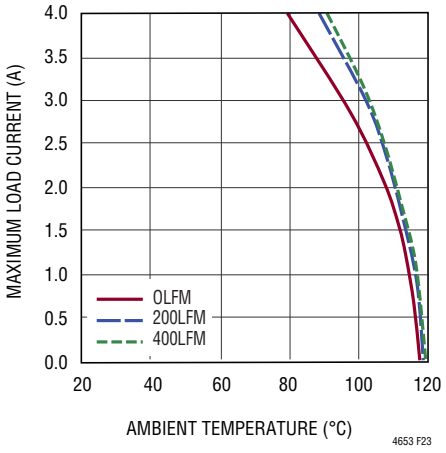


Figure 23. 24V to 5V_{OUT} Derating Curve, with BGA Heat Sink

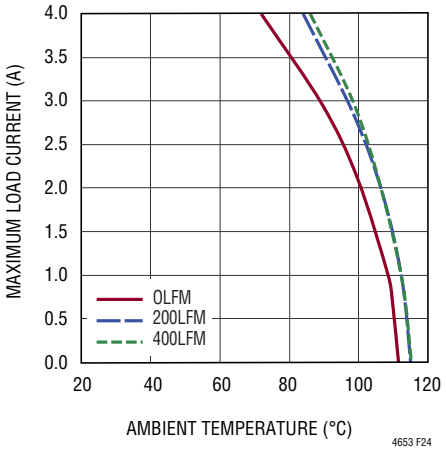


Figure 24. 48V to 5V_{OUT} Derating Curve, with BGA Heat Sink

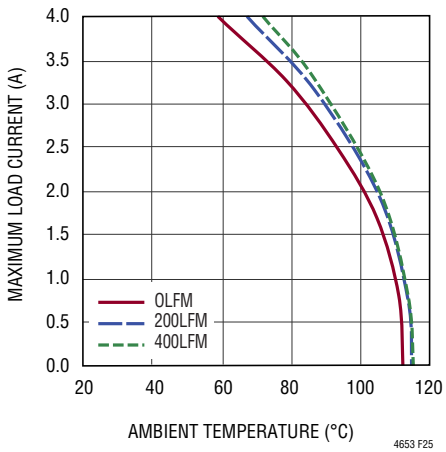


Figure 25. 24V to 15V_{OUT} Derating Curve, No Heat Sink

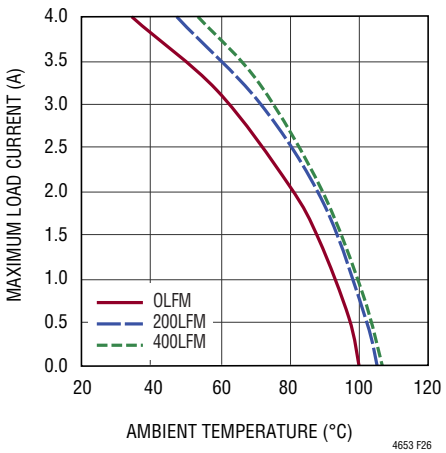


Figure 26. 48V to 15V_{OUT} Derating Curve, No Heat Sink

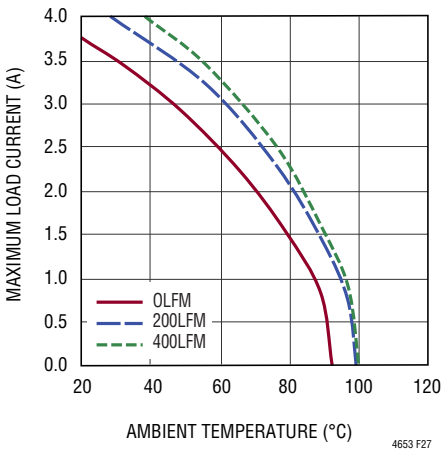


Figure 27. 48V to 24V_{OUT} Derating Curve, No Heat Sink

APPLICATIONS INFORMATION—DERATING CURVES

See Table 1 for f_{SW} and R_{EXTVCC}.

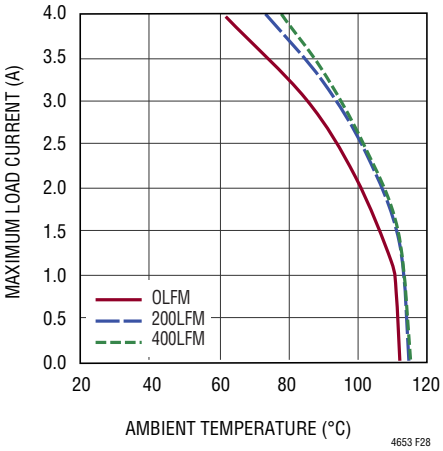


Figure 28. 24V to 15V_{OUT} Derating Curve, with BGA Heat Sink

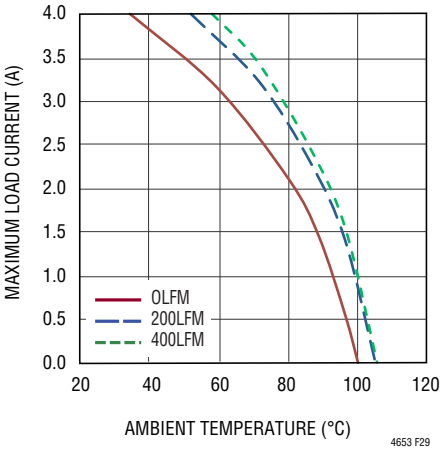


Figure 29. 48V to 15V_{OUT} Derating Curve, with BGA Heat Sink

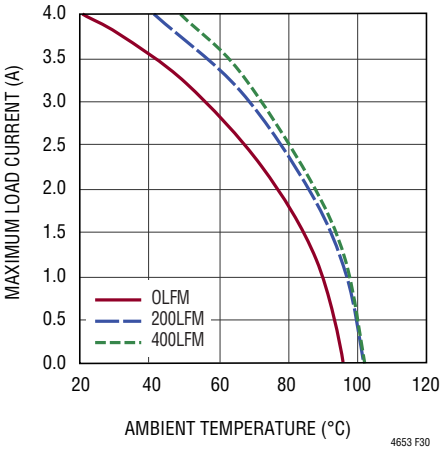


Figure 30. 48V to 24V_{OUT} Derating Curve, with BGA Heat Sink

APPLICATIONS INFORMATION

Safety Considerations

The LTM4653 does not provide galvanic isolation from V_{IN} to V_{OUT}. There is no internal fuse. If required, a slow blow fuse with a rating twice the maximum input current needs to be provided to protect the unit from catastrophic failure.

The fuse or circuit breaker, if used, should be selected to limit the current to the regulator in case of a M_T MOSFET fault. If M_T fails, the system's input supply will source very large currents to V_{OUT} through M_T. This can cause excessive heat and board damage depending on how much power the input voltage can deliver to this system. A fuse or circuit breaker can be used as a secondary fault protector in this situation. The LTM4653 does feature overcurrent and overtemperature protection.

Layout Checklist/Example

The high integration of LTM4653 makes the PCB board layout straightforward. However, to optimize its electrical and thermal performance, some layout considerations are still necessary.

- Use large PCB copper areas for high current paths, including V_{IN}, PGND and V_{OUT}. Doing so helps to minimize the PCB conduction loss and thermal stress.
- Place high frequency ceramic input and output capacitors next to the V_{IN}, V_D, PGND and V_{OUT} pins to minimize high frequency noise.
- Place a dedicated power ground layer underneath the LTM4653.
- To minimize the via conduction loss and reduce module thermal stress, use multiple vias for interconnection between top layer and other power layers.
- Do not put vias directly on pads, unless they are capped or plated over.
- Use a separate SGND copper plane for components connected to signal pins. Connect SGND to PGND directly under the module.
- For parallel module applications, connect the V_{OUT}, V_{OSNS}, RUN, ISETa, COMPa and PGOOD pins together as shown in Figure 34.
- Bring out test points on the signal pins for monitoring.

Figure 31 gives a good example of the recommended LTM4653 layout.

APPLICATIONS INFORMATION

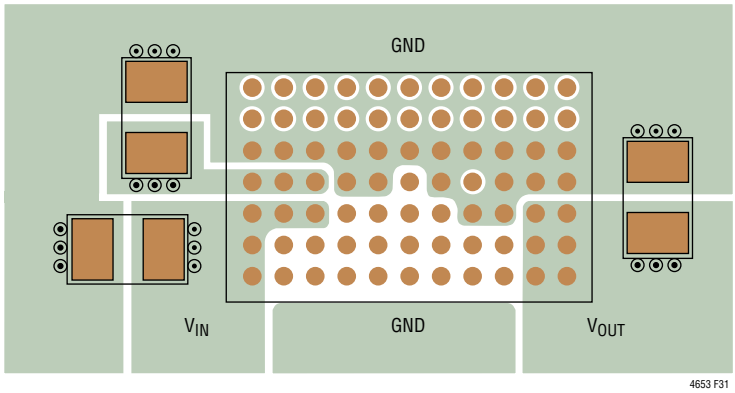


Figure 31. Recommend PCB Layout, Package Top View

TYPICAL APPLICATIONS

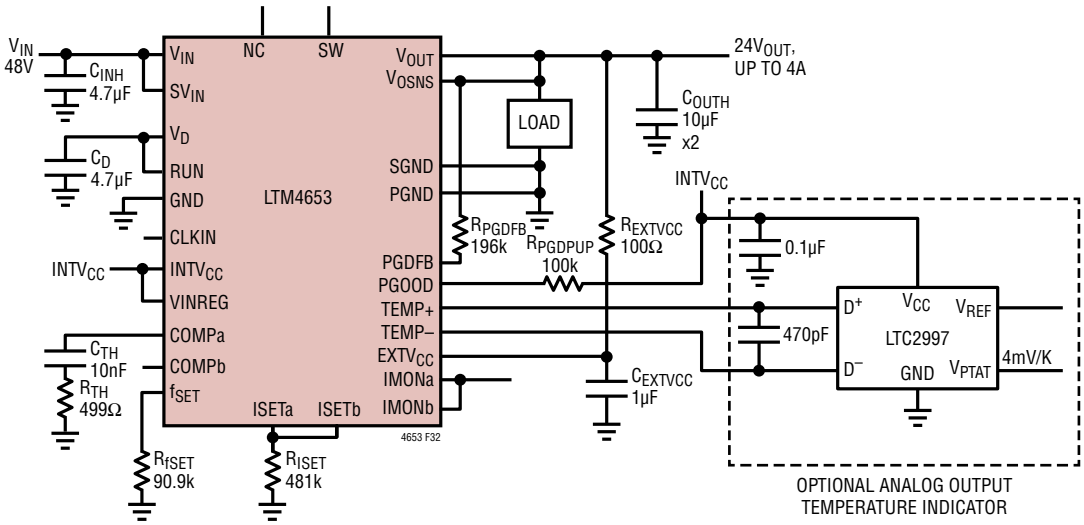


Figure 32. 4A, 24V Output DC/DC µModule Regulator

TYPICAL APPLICATIONS

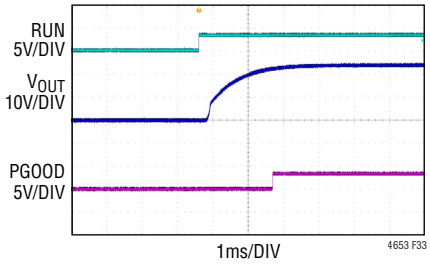


Figure 33. Start-Up Waveforms at $48V_{IN}$, Figure 32 Circuit

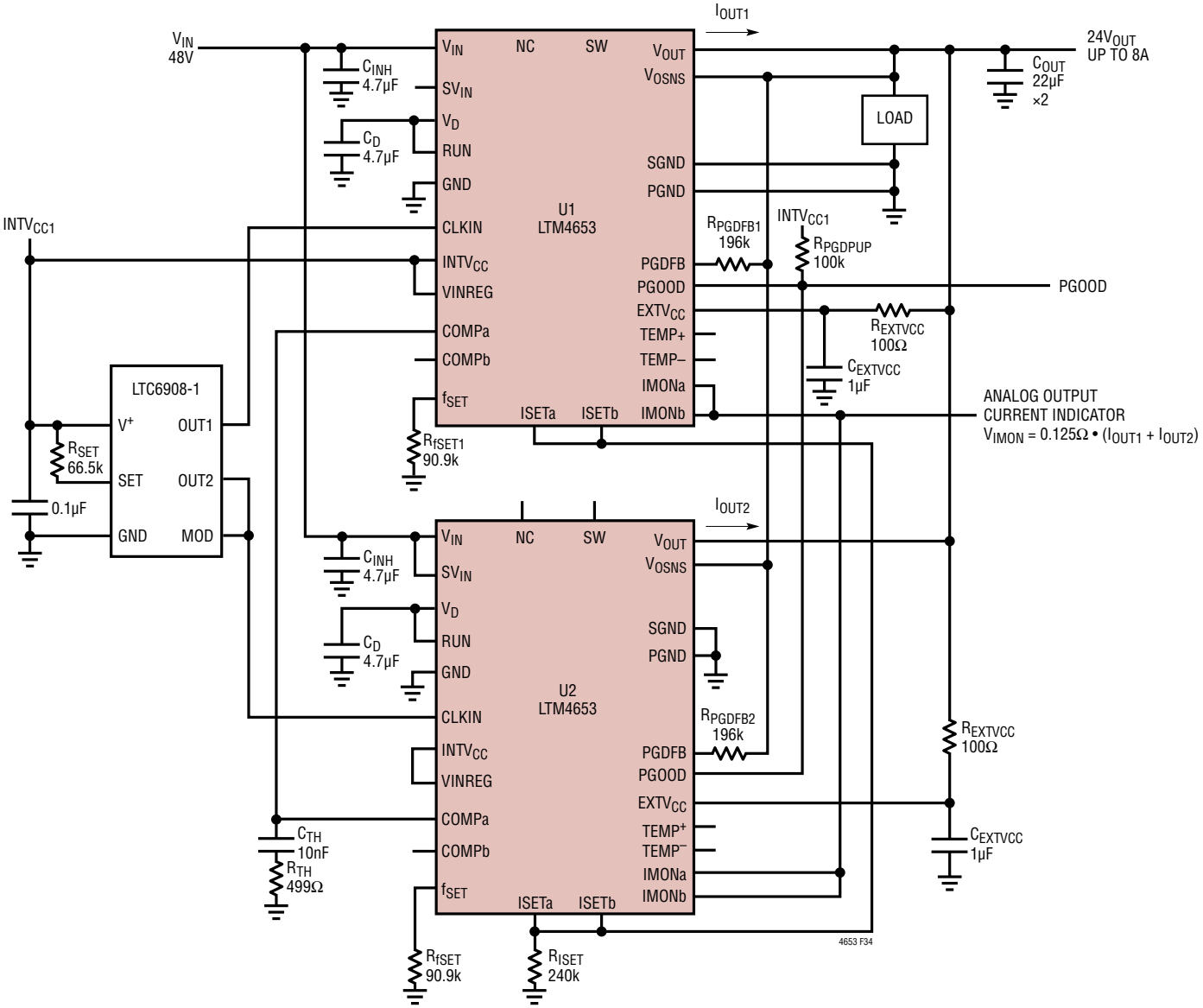


Figure 34. 24V Output at Up to 8A from 48V Input, 2-Phase Parallel with Analog Output Current Indicator

TYPICAL APPLICATIONS

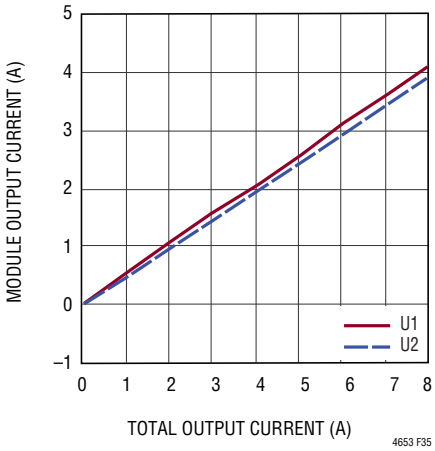


Figure 35. Current Sharing Performance of LTM4653s in Figure 34 Circuit

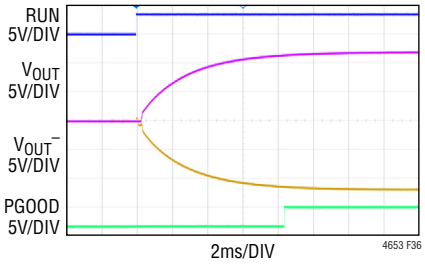
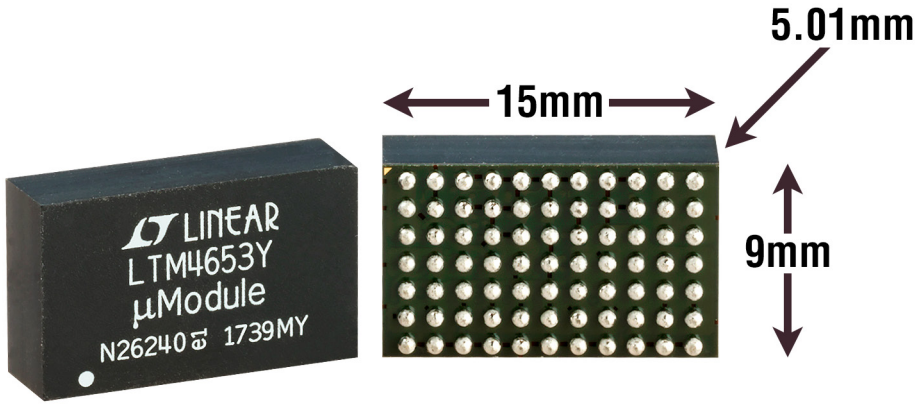


Figure 36. Concurrent ±12V Supply, Output Voltage Start-Up Waveforms, Figure 37 Circuit

PACKAGE PHOTOGRAPH



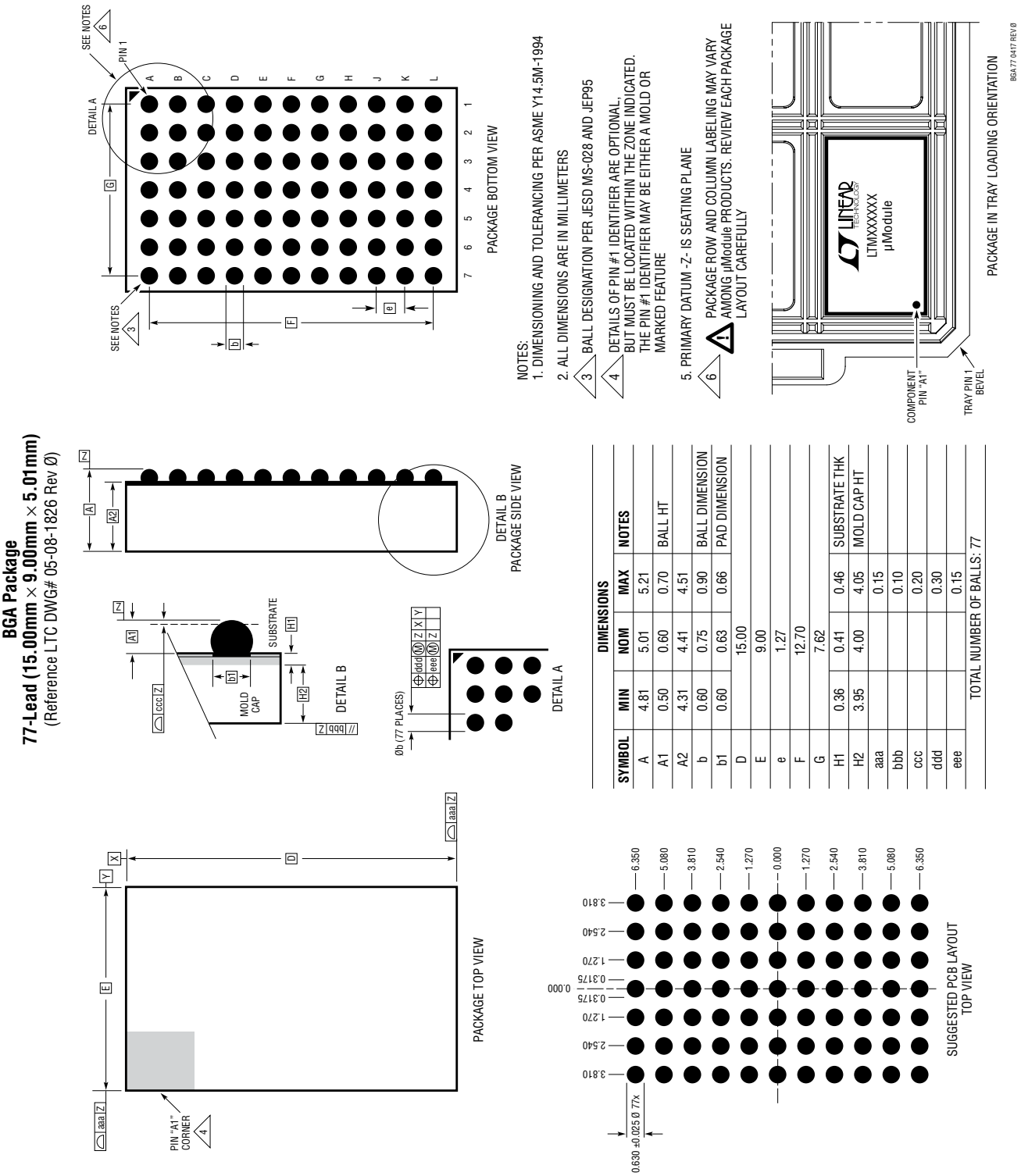
PACKAGE DESCRIPTION

Table 8. LTM4653 Component BGA Pinout

PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION
A1	V_{IN}	B1	CLKIN	C1	IMONb	D1	PGOOD	E1	COMPb	F1	ISETb
A2	V_{IN}	B2	NC	C2	IMONa	D2	PGDFB	E2	COMPa	F2	ISETa
A3	V_{IN}	B3	V_{IN}	C3	SV_{IN}	D3	VINREG	E3	f_{SET}	F3	$EXTV_{CC}$
A4	V_D	B4	V_D	C4	V_D	D4	GND	E4	SGND	F4	RUN
A5	PGND	B5	PGND	C5	PGND	D5	PGND	E5	PGND	F5	PGND
A6	NC	B6	NC	C6	NC	D6	NC	E6	NC	F6	NC
A7	NC	B7	NC	C7	NC	D7	NC	E7	NC	F7	NC

PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION
G1	V_{OSNS}	H1	V_{OSNS}	J1	$TEMP^+$	K1	V_{OUT}	L1	V_{OUT}
G2	SGND	H2	SGND	J2	$TEMP^-$	K2	V_{OUT}	L2	V_{OUT}
G3	$INTV_{CC}$	H3	PGND	J3	PGND	K3	V_{OUT}	L3	V_{OUT}
G4	PGND	H4	SW	J4	PGND	K4	PGND	L4	PGND
G5	PGND	H5	PGND	J5	PGND	K5	PGND	L5	PGND
G6	NC	H6	NC	J6	$TEMP^+$	K6	NC	L6	NC
G7	NC	H7	NC	J7	$TEMP^-$	K7	NC	L7	NC

PACKAGE DESCRIPTION



DIMENSIONS				
SYMBOL	MIN	NOM	MAX	NOTES
A	4.81	5.01	5.21	
A1	0.50	0.60	0.70	BALL HT
A2	4.31	4.41	4.51	
b	0.60	0.75	0.90	BALL DIMENSION
b1	0.60	0.63	0.66	PAD DIMENSION
D		15.00		
E		9.00		
e		1.27		
F		12.70		
G		7.62		
H1	0.36	0.41	0.46	SUBSTRATE THK
H2	3.95	4.00	4.05	MOLD CAP HT
aaa			0.15	
bbb			0.10	
ccc			0.20	
ddd			0.30	
eee			0.15	

TOTAL NUMBER OF BALLS: 77

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	02/20	Added Input Disconnect/Input Short Considerations section	17
		Corrected resistor value to 100k from 100Ω	29, 34

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TYPICAL APPLICATION

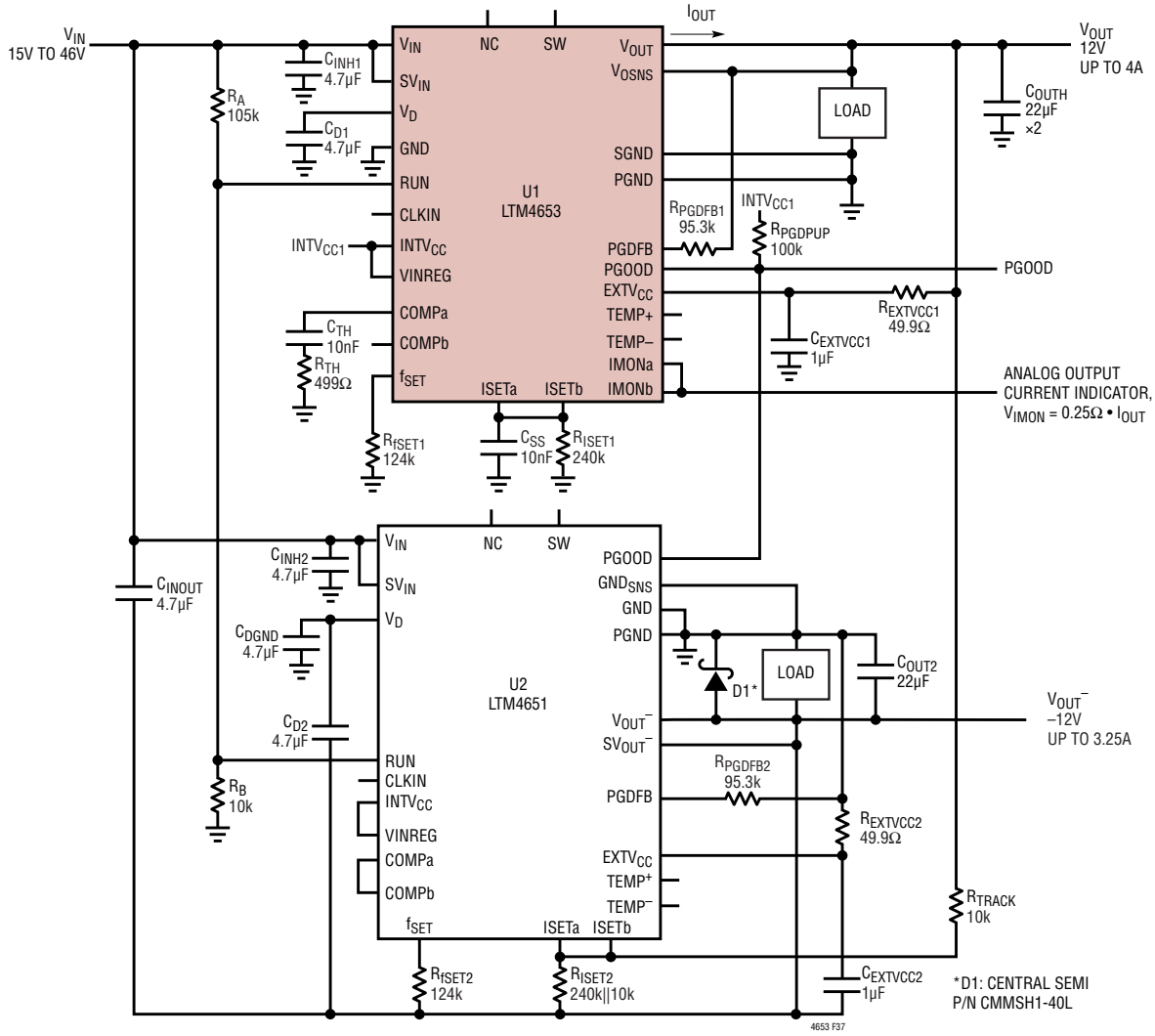


Figure 37. Concurrent ±12V Supply. See Figure 36 for Output Voltage Start-Up Waveforms

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTM4651	EN55022B Compliant, 58V_{IN}, 24W Inverting-Output µModule Regulator	3.6V ≤ V_{IN} ≤ 58V, –26.5V ≤ V_{OUT} ≤ –0.5V, I_{OUT} ≤ 4A. 15mm × 9mm × 5.01mm BGA
LTM8045	SEPIC or Inverting µModule DC/DC Converter	2.8V ≤ V_{IN} ≤ 18V, ±2.5V ≤ V_{OUT} ≤ ±15V. $I_{OUT(DC)}$ ≤ 700mA. 6.25mm × 11.25mm × 4.92mm BGA
LTM8049	Dual, SEPIC and/or Inverting µModule DC/DC Converter	2.6V ≤ V_{IN} ≤ 20V, ±2.5V ≤ V_{OUT} ≤ ±24V. $I_{OUT(DC)}$ ≤ 1A/Channel. 9mm × 15mm × 2.42mm BGA
LTM8071	60V, 5A Step-Down µModule Regulator	3.6V ≤ V_{IN} ≤ 60V, 0.97V ≤ V_{OUT} ≤ 15V, 9mm ×11.25mm × 3.32mm BGA
LTM8073	60V, 3A Step-Down µModule Regulator	3.4V ≤ V_{IN} ≤ 60V, 0.8V ≤ V_{OUT} ≤ 15V. 6.25mm × 9mm × 3.32mm BGA
LTM8064	58V, ±6A CVCC Step-Down µModule Regulator	6V ≤ V_{IN} ≤ 58V, 1.2V ≤ V_{OUT} ≤ 36V. 11.9mm × 16mm × 4.92mm BGA
LTM4613	EN55022B Compliant, 36V, 8A µModule Regulator	5V ≤ V_{IN} ≤ 36V, 3.3V ≤ V_{OUT} ≤ 15V. 15mm × 15mm × 4.32mm LGA, and 15mm × 15mm × 4.92mm BGA

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