25A DC/DC Step-Down µModule Regulator

FEATURES

- **4.7V to 15V Input Voltage Range**
- **0.6V to 1.8V Output Voltage Range**
- **25A DC Output Current**
- **±1.2% Total DC Output Voltage Error (–40°C to 125°C)**
- **High Reliability N + 1 Phase Redundancy Supported**
- **Internal or External Control Loop Compensation**
- **Differential Remote Sense Amplifier for Precision Regulation**
- **Current Mode Control/Fast Transient Response**
- **Multiphase Current Sharing Up to 150A**
- **Built-In Temperature Monitoring**
- Selectable Pulse-Skipping, Burst Mode® Operation
- Soft-Start/Voltage Tracking
- Frequency Synchronization
- Output Overvoltage Protection
- Output Overcurrent Foldback Protection
- 9mm × 15mm × 3.51mm BGA Package

APPLICATIONS

- Telecom, Networking and Industrial Equipment
- Point of Load Regulation

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DESCRIPTION

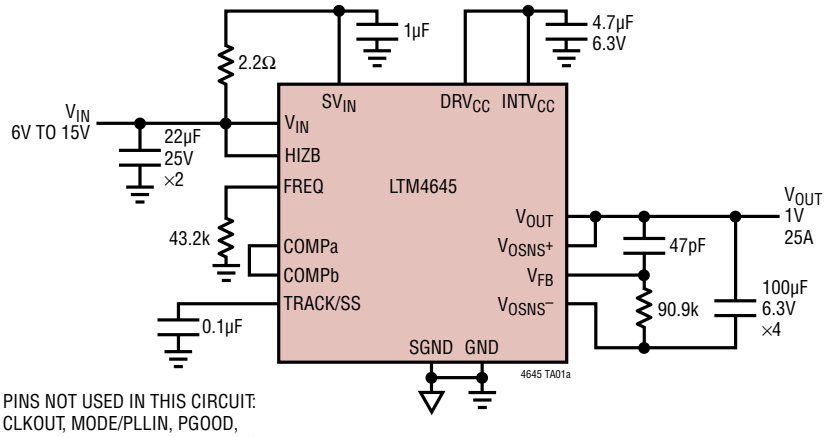
The LTM®4645 is a 25A output switching mode step-down DC/DC µModule® (power module) regulator. Included in the package are the switching controller, power FETs, inductor and all supporting components. Operating over an input voltage range of 4.7V to 15V, the LTM4645 supports an output voltage range of 0.6V to 1.8V, set by a single external resistor. Only a few input and output capacitors are needed.

Its high efficiency design delivers about 86% efficiency from 12V input to 1.0V output with 25A continuous load current. High switching frequency and a current-mode architecture enable a very fast transient response to line and load changes without sacrificing stability. The device supports frequency synchronization, programmable multiphase operation, N+1 phase redundancy, and output voltage tracking for supply rail sequencing.

Fault protection features include overvoltage and overcurrent protection. The power module is offered in a space saving 9mm × 15mm × 3.51mm BGA package. The LTM4645 is available with SnPb (BGA) or RoHS compliant terminal finish.

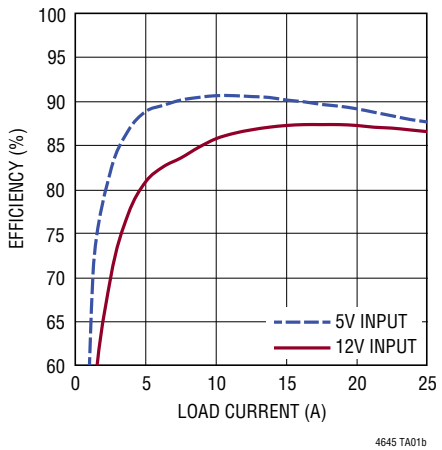
TYPICAL APPLICATION

12V_{IN}, 1V_{OUT}, 25A DC/DC µModule Regulator



PINS NOT USED IN THIS CIRCUIT:
CLKOUT, MODE/PLLIN, PGOOD,
PHASMD, PWM, RUN, SW, TEMP+, TEMP–

Efficiency vs Output Current at 1V Output

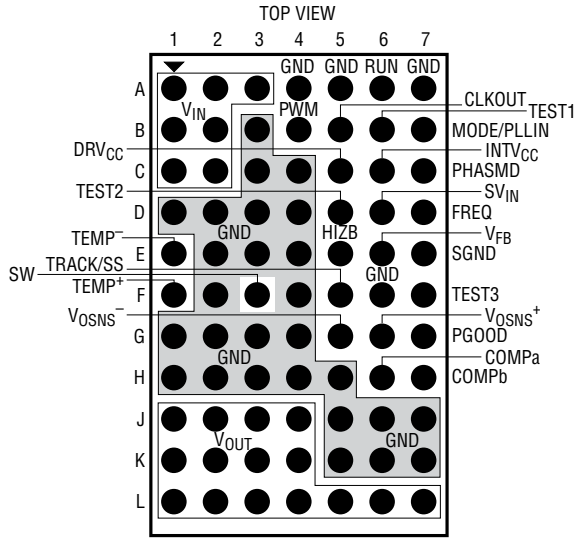


ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN}, SV_{IN}, HIZB ..... –0.3V to 16V
V_{OUT}, ... –0.3V to 3.5V
$INTV_{CC}$, DRV_{CC}, PGOOD, RUN ..... –0.3V to 6V
MODE/PLLIN, TRACK/SS, V_{OSNS}^+, V_{OSNS}^-, CLKOUT, COMPa, COMPb, V_{FB}, PHASMD, FREQ ..... –0.3V to $INTV_{CC}$
Operating Junction Temperature (Note 2) .. –40 to 125°C
Storage Temperature Range ..... –55 to 125°C
Peak Solder Reflow Body Temperature ..... 250°C
$TEMP^+$, $TEMP^-$ ..... –0.3V to 0.8V

PIN CONFIGURATION



BGA PACKAGE
77-LEAD (9mm × 15mm × 3.51mm)

$T_{J(MAX)}$ = 125°C, θ_{JA} = 9.5°C/W, $\theta_{JCbottom}$ = 4°C/W, θ_{JCtop} = 6.7°C/W, θ_{JB} = 4.5°C/W
θ_{JA} DERIVED FROM 95mm × 76mm PCB WITH SIX LAYERS; WEIGHT = 1.3g
θ VALUES DETERMINED PER JESD51-12

ORDER INFORMATION

http://www.linear.com/product/LTM4645#orderinfo

PART NUMBER	PAD OR BALL FINISH	PART MARKING*		PACKAGE TYPE	MSL RATING	TEMPERATURE RANGE (Note 2)
		DEVICE	FINISH CODE			
LTM4645EY#PBF	SAC305 (RoHS)	LTM4645Y	e1	BGA	3	–40°C to 125°C
LTM4645IY#PBF	SAC305 (RoHS)	LTM4645Y	e1	BGA	3	–40°C to 125°C
LTM4645IY	SnPb (63/37)	LTM4645Y	e0	BGA	3	–40°C to 125°C

Consult Marketing for parts specified with wider operating temperature ranges. *Device temperature grade is indicated by a label on the shipping container. Pad or ball finish code is per IPC/JEDEC J-STD-609.

- Terminal Finish Part Marking: www.linear.com/leadfree
- Recommended LGA and BGA PCB Assembly and Manufacturing Procedures: www.linear.com/umodule/pcbassembly
- LGA and BGA Package and Tray Drawings: www.linear.com/packaging

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified internal operating temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{IN} = 12V, per the typical application.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Input DC Voltage		●	4.7		15	V
$V_{OUT(RANGE)}$	Output Voltage Range	V_{IN} = 4.7V to 15V	●	0.6		1.8	V
$V_{OUT(DC)}$	Output Voltage, Total Variation with Line and Load	C_{IN} = 22µF × 4, C_{OUT} = 100µF Ceramic, 470µF POSCAP, R_{FB} = 60.4k, MODE = GND, V_{IN} = 4.7V to 15V, I_{OUT} = 0A to 25A	●	1.186	1.200	1.214	V
Input Specifications							
$I_{Q(VIN)}$	Input Supply Bias Current	V_{IN} = 12V, V_{OUT} = 1.2V, Burst Mode Operation, I_{OUT} = 0A V_{IN} = 12V, V_{OUT} = 1.2V, Pulse-Skipping Mode, I_{OUT} = 0A V_{IN} = 12V, V_{OUT} = 1.2V, Switching Continuous, I_{OUT} = 0A Shutdown, RUN = 0, V_{IN} = 12V			11 25 170 90		mA mA mA µA
$I_{S(VIN)}$	Input Supply Current	V_{IN} = 12V, V_{OUT} = 1.2V, I_{OUT} = 25A			3.0		A
Output Specifications							
$I_{OUT(DC)}$	Output Continuous Current Range	V_{IN} = 12V, V_{OUT} = 1.2V (Note 4)		0		25	A
$\Delta V_{OUT(LINE)}/V_{OUT}$	Line Regulation Accuracy	V_{OUT} = 1.2V, V_{IN} from 4.7V to 15V, I_{OUT} = 0A	●		0.005	0.05	%/V
$\Delta V_{OUT(LOAD)}/ V_{OUT}$	Load Regulation Accuracy	V_{OUT} = 1.2V, I_{OUT} = 0A to 25A, V_{IN} = 12V (Note 4)	●		0.1	0.3	%
$V_{OUT(AC)}$	Output Ripple Voltage	C_{OUT} = 100µF Ceramic × 6, V_{IN} = 12V, V_{OUT} = 1.2V, I_{OUT} = 0A			15		mV
$\Delta V_{OUT(START)}$	Turn-On Overshoot	C_{OUT} = 100µF Ceramic × 6, V_{IN} = 12V, V_{OUT} = 1.2V, I_{OUT} = 0A			20		mV
t_{START}	Turn-On Time	C_{OUT} = 100µF Ceramic × 6 V_{IN} = 12V, V_{OUT} = 1.2V, No Load, TRACK/SS = 0.01µF			5		ms
ΔV_{OUTLS}	Peak Deviation for Dynamic Load	Load: 0% to 50% to 0% of Full Load, C_{OUT} = 100µF Ceramic × 6, V_{IN} = 12V, V_{OUT} = 1.2V			36		mV
t_{SETTLE}	Settling Time for Dynamic Load Step	Load: 0% to 50% to 0% of Full Load, C_{OUT} = 100µF Ceramic × 6, V_{IN} = 12V, V_{OUT} = 1.2V			15		µs
I_{OUTPK}	Output Current Limit	V_{IN} = 12V, V_{OUT} = 1.2V			35		A
Control Specifications							
V_{FB}	Voltage at V_{FB} Pin	I_{OUT} = 0A, V_{OUT} = 1.2V	●	594	600	606	
I_{FB}	Current at V_{FB} Pin	(Note 7)			–30	–100	nA
$I_{TRACK/SS}$	Track Pin Soft-Start Pull-Up Current	TRACK/SS = 0V			1.25		µA
$t_{ON(MIN)}$	Minimum On-Time	(Note 3)			90		ns
R_{FBHI}	Resistor Between V_{OUT_LCL} and V_{FB} Pins			60.05	60.40	60.75	kΩ
V_{RUN}	RUN Pin On Threshold	V_{RUN} Rising		1.2	1.35	1.45	V
V_{RUNHYS}	RUN Pin On Hysteresis				180		mV
UVLO	Undervoltage Lockout	V_{INTVCC} Falling			4		V
$UVLO_{HYS}$	UVLO Hysteresis				400		mV
V_{HIZB}	HIZB Pin On Threshold	V_{HIZB} Rising			2.3		V
$V_{HIZBHYS}$	HIZB Pin On Hysteresis				800		mV

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified internal operating temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{IN} = 12V, per the typical application.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
PGOOD							
R_{PGOOD}	PGOOD Pull-Down Resistance				90	200	Ω
V_{PGOOD}	PGOOD Trip Level	V_{FB} With Respect to Set Output V_{FB} Ramping Negative V_{FB} Ramping Positive			 –7.5 7.5		 % %
V_{PGL}	PGOOD Voltage Low	I_{PGOOD} = 2mA			0.1	0.3	V
$INTV_{CC}$ Linear Regulator							
V_{INTVCC}	Internal V_{CC} Voltage	V_{IN} ≥ 12V		5.3	5.5	5.7	V
V_{INTVCC} Load Reg	$INTV_{CC}$ Load Regulation	I_{CC} = 0mA to 10mA			0.5		%
Oscillator and Phase-Locked Loop							
f_{SYNC}	SYNC Capture Range			300		1000	kHz
f_{SW}	Switching Frequency	R_{FREQ} = 47.5kΩ		540	600	660	kHz
I_{FREQ}	FREQ Pin Current	V_{FREQ} = 0.8V			20		µA
R_{MODE_PLLIN}	Mode_PLLIN Input Resistance				250		kΩ
$V_{IH_MODE_PLLIN}$	Clock Input Level High			2.0			V
$V_{IL_MODE_PLLIN}$	Clock Input Level Low					1.2	V
θ_{CLKOUT}	CLKOUT to SW Phase Delay	V_{PHSMD} = 0V V_{PHSMD} = 1/4 $INTV_{CC}$ V_{PHSMD} = Float V_{PHSMD} = 3/4 $INTV_{CC}$ V_{PHSMD} = $INTV_{CC}$			90 90 120 60 180		Deg Deg Deg Deg Deg

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTM4645 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTM4645E is guaranteed to meet performance specifications over the 0°C to 125°C internal operating temperature range. Specifications over the full –40°C to 125°C internal operating temperature range are assured by design, characterization and correlation with statistical process controls. The LTM4645I is guaranteed to meet specifications over the full –40°C to 125°C internal operating temperature range. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance and other environmental factors.

Note 3: The minimum on-time condition is specified for a peak-to-peak inductor ripple current of ~40% of I_{MAX} Load. (See the Applications Information section)

Note 4: See output current derating curves for different V_{IN}, V_{OUT} and T_A.

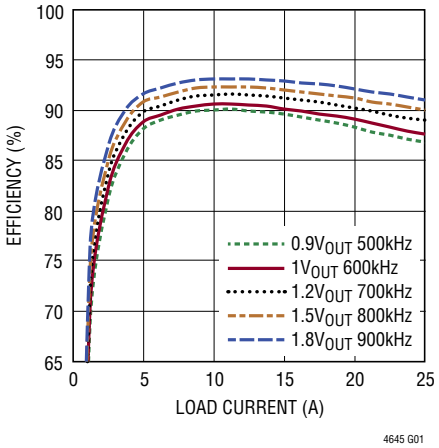
Note 5: Limit current into the RUN pin to less than 2mA.

Note 6: Guaranteed by design.

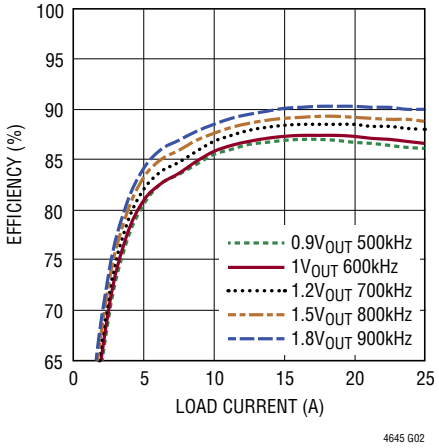
Note 7: 100% tested at wafer level.

TYPICAL PERFORMANCE CHARACTERISTICS

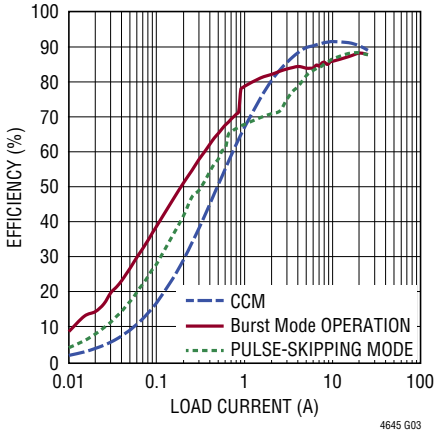
Efficiency vs Output Current, V_{IN} = 5V



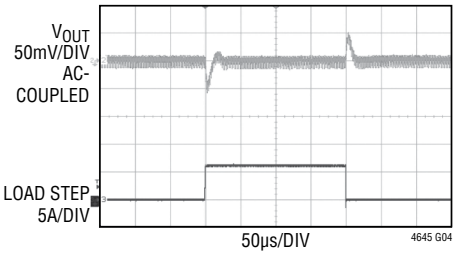
Efficiency vs Output Current, V_{IN} = 12V



CCM, Burst Mode and Pulse-Skipping Mode Efficiency V_{IN} = 12V, V_{OUT} = 1.2V, 750kHz

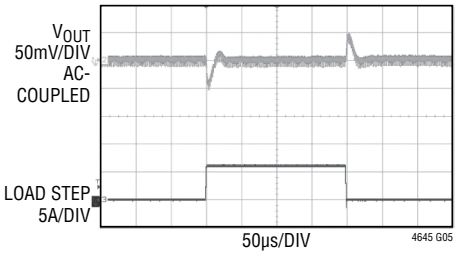


0.9V Output Load Step Transient Response



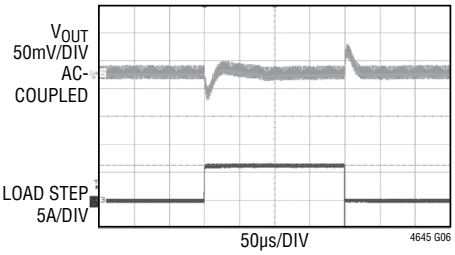
V_{IN} = 12V, V_{OUT} = 0.9V, F_S = 500kHz
C_{OUT} = 6 × 100µF CERAMIC
C_{FF} = 33pF
0A TO 6.25A LOAD STEP, 10A/µs

1V Output Load Step Transient Response



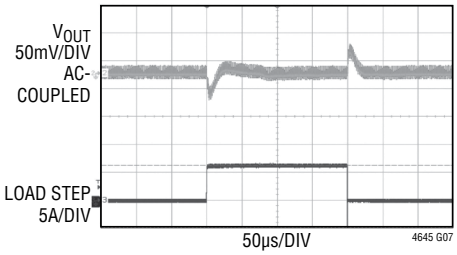
V_{IN} = 12V, V_{OUT} = 1V, F_S = 600kHz
C_{OUT} = 6 × 100µF CERAMIC
C_{FF} = 33pF
0A TO 6.25A LOAD STEP, 10A/µs

1.2V Output Load Step Transient Response



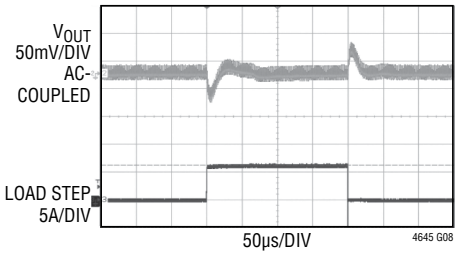
V_{IN} = 12V, V_{OUT} = 1.2V, F_S = 700kHz
C_{OUT} = 6 × 100µF CERAMIC
C_{FF} = 33pF
0A TO 6.25A LOAD STEP, 10A/µs

1.5V Output Load Step Transient Response



V_{IN} = 12V, V_{OUT} = 1.5V, F_S = 800kHz
C_{OUT} = 6 × 100µF CERAMIC
C_{FF} = 33pF
0A TO 6.25A LOAD STEP, 10A/µs

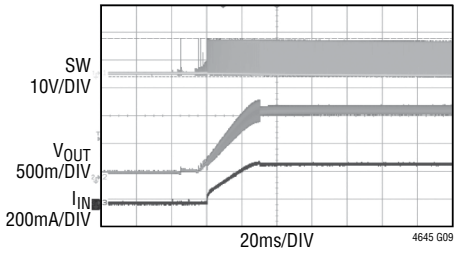
1.8V Output Load Step Transient Response



V_{IN} = 12V, V_{OUT} = 1.8V, F_S = 900kHz
C_{OUT} = 6 × 100µF CERAMIC
C_{FF} = 33pF
0A TO 6.25A LOAD STEP, 10A/µs

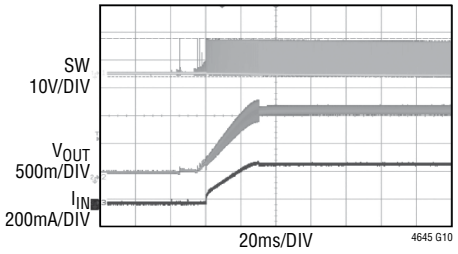
TYPICAL PERFORMANCE CHARACTERISTICS

Start-Up with No Load Applied



V_{IN} = 12V, V_{OUT} = 1.2V, F_S = 700kHz, NO LOAD
C_{OUT} = 1 × 47µF CERAMIC + 1 × 470µF SPCAP
C_{SS} = 0.1µF

Start-Up with 25A Load Applied



V_{IN} = 12V, V_{OUT} = 1.2V, F_S = 700kHz, NO LOAD
C_{OUT} = 1 × 47µF CERAMIC + 1 × 470µF SPCAP
C_{SS} = 0.1µF

PIN FUNCTIONS

PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG µModule PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY.

V_{IN} (A1-A3, B1-B2, C1-C2): Power Input Pins. Apply input voltage between these pins and GND pins. Recommend placing input decoupling capacitance directly between V_{IN} pins and GND pins.

GND (A4, A7, B3, C3, C4, D1-D4, E2-E4, F2, F4, F6, G1-G4, H1-H5, J5-J7, K5-K7): Ground Pins for Both Input and Output Returns. All ground pins need to connect with large copper areas underneath the unit.

RUN (A6): Run Control Pin. A voltage above 1.35V will turn on the module. This is a 1µA pull-up current on this pin. Once the RUN pin rises above the 1.35V threshold the pull-up current increases to 5µA.

PWM (B4): Control PWM Three-State Output Signal. For monitor and test purpose only. Do not drive this pin.

CLKOUT (B5): Clock output with phase control using the PHASMD pin to enable multiphase operation between devices. See the Applications Information section.

TEST1, TEST2, TEST3 (B6, D5, F7): These pins are for µModule initial test purposes. Please connect these pins to GND with a large GND copper area.

MODE/PLLIN (B7): Mode Selection Pin and External Synchronization Pin. Connect this pin to SGND to force the module into force continuous current mode (CCM) of operation. Connect to $INTV_{CC}$ to enable pulse-skipping mode of operation. Leaving the pin floating will enable Burst Mode operation. A clock on the pin will force the module into continuous current mode of operation and synchronized to the external clock applied to this pin. See the Applications Information section.

SV_{IN} (D6): Signal V_{IN}. Input voltage to the internal 5.5V regulator for the control circuitry of the regulator. Tie this pin to V_{IN} pin through a 2.2Ω plus 1µF R-C filter in most application. See the Application Information section.

DRV_{CC} (C5): Power Input Pin for the MOSFET driver circuitry. Connect to $INTV_{CC}$ output for the application with the input voltage 6V and above or connect this pin to an external supply 4.5V or above through a 2.2Ω plus 1µF R-C filter. See the Application Information section.

$INTV_{CC}$ (C6): Internal 5.5V LDO for driving the control circuitry decouple with pin to GND with a minimum of 2.2µF low ESR ceramic capacitor. The 5.5V LDO has a 50mA current limit.

PHASMD (C7): This pin determines the relative phases between the internal controller and the CLKOUT signal. See Table 2 in the Application Information section.

FREQ (D7): Frequency Set Pin. A 20µA current is sourced from this pin. A resistor from this pin to ground sets a voltage that in turn programs the operating frequency. Alternatively, this pin can be driven with a DC voltage that can set the operating frequency. See the Applications Information section.

HIZB (E5): Phase Shedding Input Pin. When this pin is low, TRACK/SS, COMP and PWM pin go to high impedance. Tie to $INTV_{CC}$ or V_{IN} to disable this function.

V_{FB} (E6): The Negative Input of the Error Amplifier. Internally, this pin is connected to V_{OSNS}^+ with a 60.4k 0.5% precision resistor. Different output voltages can be programmed with an additional resistor between V_{FB} and V_{SNS}^- pins. In PolyPhase® operation, tying the V_{FB} pins together allows for parallel operation. See the Applications Information section for details.

SGND (E7): Signal Ground Pin. Return ground path for all analog and low power circuitry. Tie a single connection to the output capacitor GND in the application. See layout guidelines in Figure 22.

SW (F3): Switching node of the circuit is used for testing purposes. Also an R-C snubber network can be applied to reduce or eliminate switch node ringing, or otherwise leave floating. See the Applications Information section.

TRACK/SS (F5): Output Voltage Tracking Pin and Soft-Start Inputs. The pin has a 1.25µA pull-up current. A capacitor from this pin to ground will set a soft-start ramp rate. In tracking, the regulator output can be tracked to a different voltage. The voltage ramp rate at his pin sets the voltage ramp rate of the output. See the Applications Information section.

PIN FUNCTIONS

V_{OSNS}^- (G5): Input to the Remote Sense Amplifier. This pin connects to the ground remote sense point at the output load.

V_{OSNS}^+ (G6): Input to the Remote Sense Amplifier. Internally, this pin is connected to V_{FB} with a 60.4k 0.5% precision resistor.

PGOOD (G7): Output Voltage Power Good Indicator. Open-drain logic output that is pulled to ground when the output voltage is not within ±7.5% of the regulation point.

COMPa (H6): Current Control Threshold and Error Amplifier Compensation Point. The current comparator threshold increases with this control voltage. Small filter capacitor (10pF) internal to LTM4645 on this pin provides good noise rejection in the control loop. Tie to COMPb pin to use internal compensation in the vast majority of applications. Whereas, when more specialized applications require an optimization of control loop response, connect an R-C compensation network from COMPa to SGND. Tie COMPa pins together in parallel operation. See the Applications Information section.

COMPb (H7): Internal Loop Compensation Networks. Tie to COMPa to provide internal loop compensation for majority of applications. Float this pin if internal loop compensation not used. See COMPa description.

V_{OUT} (J1-J4, K1-K4, L1-L7): Power Output Pins. Apply output load between these pins and GND pins. Recommend placing output decoupling capacitance directly between these pins and GND pins. See Table 1.

$TEMP^+$ (F1): Temperature Monitor. An internal diode connected PNP transistor. See the Applications Information section.

$TEMP^-$ (E1): Low Side of the Internal Temperature Monitor.

BLOCK DIAGRAM

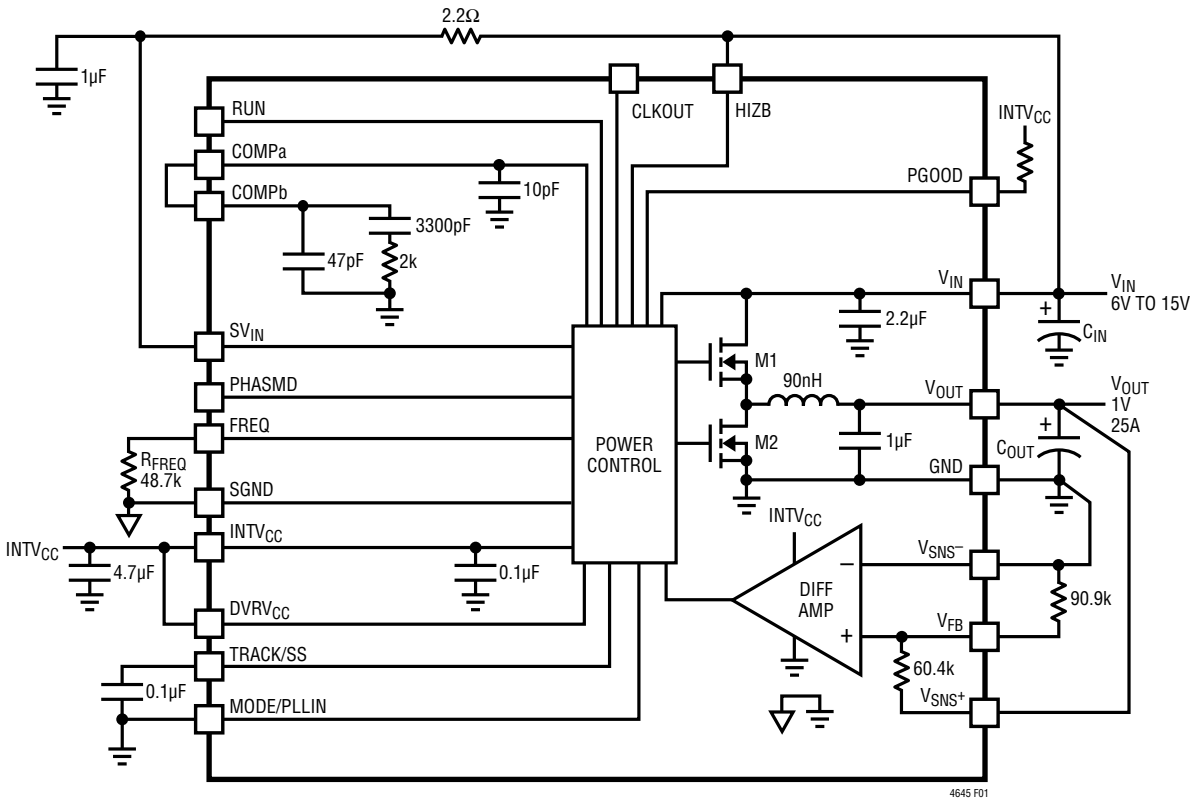


Figure 1. Simplified LTM4645 Block Diagram

DECOUPLING REQUIREMENTS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
C_{IN}	External Input Capacitor Requirement (V_{IN} = 4.7V to 15V, V_{OUT} = 1V)	I_{OUT} = 25A		44		µF
C_{OUT}	External Output Capacitor Requirement (V_{IN} = 4.7V to 15V, V_{OUT} = 1V)	I_{OUT} = 25A		300		µF

OPERATION

Power Module Description

The LTM4645 is a high performance single output standalone nonisolated switching mode DC/DC power supply. It can provide a 25A output with few external input and output capacitors. This module provides precisely regulated output voltages programmable via external resistors from 0.6V DC to 1.8V DC over a 4.7V to 15V input range. The typical application schematic is shown in Figure 23 and Figure 24.

The LTM4645 has an integrated constant-frequency current mode regulator, power MOSFETs, inductor, and other supporting discrete components. The switching frequency range is optimized from 400kHz to 900kHz, depending on output voltage. For switching noise-sensitive applications, it can externally program to or be synchronized to a clock from 300kHz to 1MHz subject to minimum on-time and inductor ripple current limitations. See the Applications Information section.

The LTM4645 is designed to use either external or internal control loop compensation by shorting COMPb and COMPa pins together. With current mode control, the internal loop compensation has sufficient stability margins and good transient performance with a wide range of output capacitors, even with all ceramic output capacitors. Table 5 provides a guideline for input and output capacitances for several different output conditions using the internal loop compensation. The LTpowerCAD® design tool is available to download for optimizing the loop stability and transient response.

Current mode control provides cycle-by-cycle fast current limit in an overcurrent condition. An internal overvoltage monitor protects the output voltage in the event of an overvoltage >10%. The top MOSFET is turned off and the bottom MOSFET is turned on until the output is cleared.

Pulling the RUN pin below 1.35V forces the regulator into a shutdown state. The TRACK/SS pin is used for programming the output voltage ramp and voltage tracking during start-up. See the Application Information section.

Multiphase operation can be easily employed by cascading the MODE/PLLIN input to the CLKOUT output. See the Applications Information section and Figure 25 for example.

For high reliability environment, N+1 phase redundancy can be easily implemented in LTM4645 together with a hot swap controller, such as the LTC®4226, for extra system protection. By connecting the HIZB pin to the gate of the hot swap switch, any fault channel can be disconnected while the rest of the system is not affected. See Applications Information section and Figure 27 for example.

High efficiency at light loads can be accomplished with phase shedding in multiphase operation or with selectable pulse-skipping mode or Burst Mode operation in single phase operation. Efficiency graphs are provided for light load operation in the Typical Performance Characteristics section.

A remote sense amplifier is provided for accurately sensing output voltages at the load point.

A $TEMP^+$ and $TEMP^-$ pins are provided to allow the internal device temperature to be monitored using an onboard diode connected PNP transistor.

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The typical LTM4645 application circuit is shown in Figure 23 and Figure 24. External component selection is primarily determined by the maximum load current and output voltage. Refer to Table 5 for specific external capacitor requirements for particular applications.

V_{IN} to V_{OUT} Step-Down Ratios and Minimum On-Time

There are restrictions in the V_{IN} to V_{OUT} step-down ratio that can be achieved for a given input, output voltage and frequency. The minimum on-time, $t_{ON(MIN)}$, limits the smallest time duration that the module is capable of turning on the top MOSFET. It is determined by internal timing delays, and the gate charge required turning on the top MOSFET. At very low duty cycles, the minimum 90ns on-time must be maintained and satisfy the equation:

$$t_{ON} = \frac{V_{OUT}}{V_{IN} \bullet FREQ} > 90ns$$

If the duty cycle falls below what can be accommodated by the minimum on-time, the controller will begin to skip cycles. The output voltage will continue to be regulated, but the output ripple voltage of inductor ripple and current will increase. The minimum on-time can be increased by lowering the switching frequency.

Output Voltage Programming

The PWM controller has an internal 0.6V reference voltage. As shown in the Block Diagram, a 60.4k, 0.5% accuracy internal feedback resistor connects from the V_{OSNS}^+ pin to the V_{FB} pin.

The output voltage will default to 0.6V with no feedback resistor. Adding a resistor R_{FB} from V_{FB} to V_{OSNS}^- programs the output voltage:

$$V_{OUT} = 0.6V \bullet \frac{60.4k + R_{FB}}{R_{FB}}$$

Table 1. V_{FB} Resistor Table vs Various Output Voltages

V_{OUT} (V)	0.6	0.9	1.0	1.2	1.5	1.8
R_{FB} (kΩ)	OPEN	121	90.9	60.4	40.2	30.1
Frequency (kHz)	400	500	600	700	800	900
R_{FREQ} (kΩ)	37.4	43.2	48.7	53.6	59	64.9

In multiphase single output application. Only one set of differential sensing amplifier and one set of feedback resistor are required while connecting V_{OUT}, V_{FB} and COMP of different channels together. See Figure 25 for paralleling application.

Input Capacitors

The LTM4645 module should be connected to a low AC-impedance DC source. Additional input capacitors are needed for the RMS input ripple current rating. The $I_{CIN(RMS)}$ equation which follows can be used to calculate the input capacitor requirement. Typically 22µF ceramics are a good choice with RMS ripple current ratings of ~2A each. A 47µF to 100µF surface mount aluminum electrolytic bulk capacitor can be used for more input bulk capacitance. This bulk input capacitor is only needed if the input source impedance is compromised by long inductive leads, traces or not enough source capacitance. If low impedance power planes are used, then this bulk capacitor is not needed.

For a buck converter, the switching duty cycle can be estimated as:

$$D = \frac{V_{OUT}}{V_{IN}}$$

Without considering the inductor ripple current, for each output, the RMS current of the input capacitor can be estimated as:

$$I_{CIN(RMS)} = \frac{I_{OUT(MAX)}}{\eta\%} \bullet \sqrt{D \bullet (1-D)}$$

In the previous equation, η% is the estimated efficiency of the power module. The bulk capacitor can be a switcher-rated electrolytic aluminum capacitor or a Polymer capacitor.

Output Capacitors

The LTM4645 is designed for low output voltage ripple noise. The bulk output capacitors defined as C_{OUT} are chosen with low enough effective series resistance (ESR) to meet the output voltage ripple and transient requirements. C_{OUT} can be a low ESR tantalum capacitor, low ESR Polymer capacitor or ceramic capacitors. Please note small

APPLICATIONS INFORMATION

22pF to 47pF feedforward capacitor (C_{FF}) is necessary for all ceramic output application to achieve enough phase margin. The typical output capacitance range is from 400µF to 800µF. Additional output filtering may be required by the system designer if further reduction of output ripple or dynamic transient spikes is required. Table 5 shows a matrix of different output voltages and output capacitors to minimize the voltage droop and overshoot during a 6A/µs transient (at 10A/µs slew rate). The table optimizes total equivalent ESR and total output capacitance to optimize the transient performance. Multiphase operation will reduce effective output ripple as a function of the number of phases. Application Note 77 discusses this reduction versus output ripple current cancellation. But the output capacitance should be considered carefully as a function of stability and transient response. The Linear Technology LTpowerCAD Design Tool can calculate the output ripple reduction as the number of implemented phase's increases by N times and provide stability analysis.

Burst Mode Operation

The LTM4645 is capable of Burst Mode operation in which the power MOSFETs operate intermittently based on load demand, thus saving quiescent current. For applications where maximizing the efficiency at very light loads is a high priority, Burst Mode operation should be applied. To enable Burst Mode operation, simply float the MODE_PLLIN pin. During Burst Mode operation, the peak current of the inductor is set to approximately one-third of the maximum peak current value in normal operation even though the voltage at the COMPa pin indicates a lower value. The voltage at the COMPa pin drops when the inductor's average current is greater than the load requirement. As the COMPa voltage drops below 0.5V, the burst comparator trips, causing the internal sleep line to go high and turn off both power MOSFETs.

In sleep mode, the internal circuitry is partially turned off, reducing the quiescent current. The load current is now being supplied from the output capacitors. When the output voltage drops, causing COMPa to rise, the internal sleep line goes low, and the LTM4645 resumes normal operation. The next oscillator cycle will turn on the top power MOSFET and the switching cycle repeats.

Pulse-Skipping Mode Operation

In applications where low output ripple and high efficiency at intermediate currents are desired, pulse-skipping mode should be used. Pulse-skipping operation allows the LTM4645 to skip cycles at low output loads, thus increasing efficiency by reducing switching loss. Tying the MODE_PLLIN pin to $INTV_{CC}$ enables pulse-skipping operation. With pulse-skipping mode at light load, the internal current comparator may remain tripped for several cycles, thus skipping operation cycles. This mode has lower ripple than Burst Mode operation and maintains a higher frequency operation than Burst Mode operation.

Forced Continuous Operation

In applications where fixed frequency operation is more critical than low current efficiency, and where the lowest output ripple is desired, forced continuous operation should be used. Forced continuous operation can be enabled by tying the MODE_PLLIN pin to GND. In this mode, inductor current is allowed to reverse during low output loads, the COMPa voltage is in control of the current comparator threshold throughout, and the top MOSFET always turns on with each oscillator pulse. During start-up, forced continuous mode is disabled and inductor current is prevented from reversing until the LTM4645's output voltage is in regulation.

Frequency Selection

The LTM4645 device is operated over a range of frequencies to improve power conversion efficiency. It is recommended to operate the lower output voltages or lower duty cycle conversions at lower frequencies to improve efficiency by lowering power MOSFET switching losses. Higher output voltages or higher duty cycle conversions can be operated at higher frequencies to limit inductor ripple current. The efficiency graphs will show an operating frequency chosen for that condition. See Table 1 for optimized frequency for various output voltages.

The LTM4645 switching frequency can be set with an external resistor from the f_{SET} pin to SGND. An accurate 20µA current source into the resistor will set a voltage that programs the frequency or a DC voltage can be applied. Figure 2 shows a graph of frequency setting verses programming voltage.

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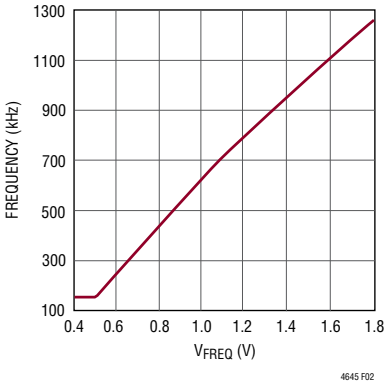


Figure 2. Relationship Between Switching Frequency and FREQ Pin Voltage

PLL and Frequency Synchronization

For some switching noise sensitive applications, LTM4645 can be synchronized from 300kHz to 1MHz subject to minimum on-time and inductor current ripple limitation with an input clock that has a high level above 2V and a low level below 0.8V at the MODE_PLLIN pin. Once the LTM4645 is synchronizing to an external clock frequency, it will always be running in forced continuous current operation. The 300kHz low end operation frequency limit is suggested to limit inductor ripple current.

Multiphase Operation

For outputs that demand more than 25A of load current, multiple LTM4645 devices can be paralleled to provide more output current without increasing input and output voltage ripple.

The MODE_PLLIN pin allows the LTM4645 to synchronize to an external clock (between 300kHz and 1MHz) and the internal phase-locked loop allows the LTM4645 to lock onto an incoming clock phase as well. The CLKOUT signal can be connected to the MODE_PLLIN pin of the following stage to line up both the frequency and the phase of the entire system. Tying the PHASMD pin to $INTV_{CC}$, three-fourths of $INTV_{CC}$, floating or, SGND generates a phase difference (between V_{OUT} and CLKOUT) of 180 degrees, 60 degrees, 120 degrees, 90 degrees respectively. A total of 12 phases can be cascaded to run simultaneously with respect to each other by programming the PHASMD pin of each LTM4645 channel to different levels. Figure 3 shows a 2-phase, 3-phase, 4-phase, and 6-phase design example for clock phasing.

PHASE SELECTION

V_{OUT} PHASE	CLKOUT PHASE	PHASMD (V)
0	90	0
0	90	1/4 $INTV_{CC}$
0	120	FLOAT
0	60	3/4 $INTV_{CC}$
0	180	$INTV_{CC}$

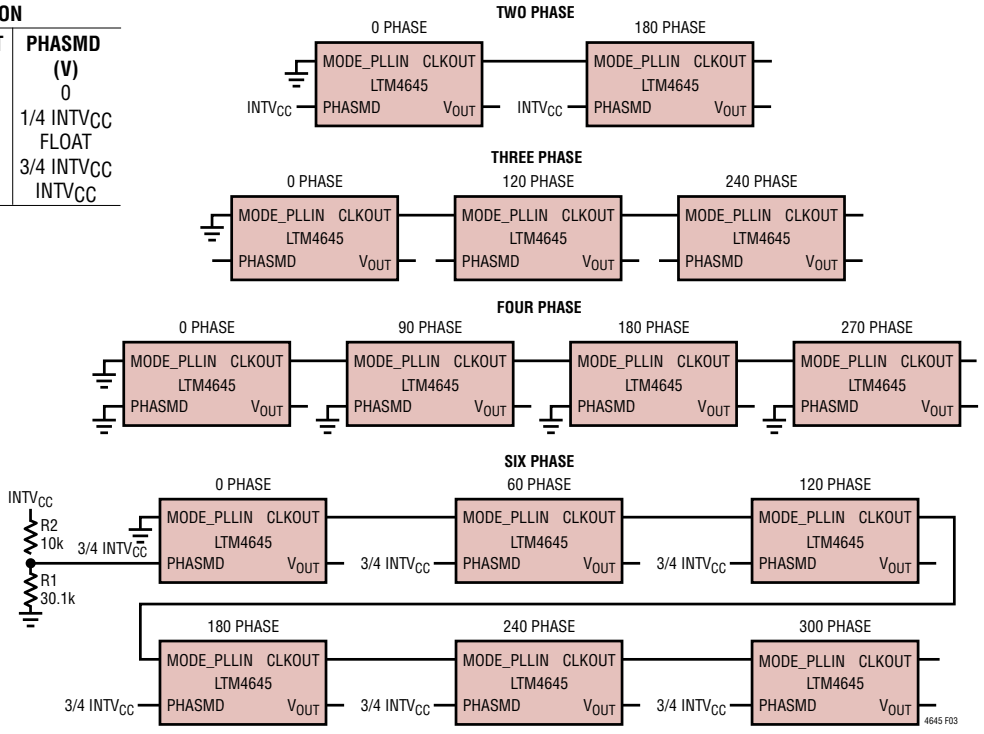


Figure 3. Phase Selection Examples

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The LTM4645 device is an inherently current mode controlled device, so parallel modules will have good current sharing. This will balance the thermals in the design. Tie the COMPa, V_{FB}, TRACK/SS and RUN pins of each LTM4645 together to share the current evenly. Figures 25 and 28 show a schematic of the parallel design.

Table 2. PHASMD and CLKOUT Signal Relationship

PHASMD	GND	1/4 $INTV_{CC}$	FLOAT	3/4 $INTV_{CC}$	$INTV_{CC}$
CLKOUT	90°	90°	120°	60°	180°

A multiphase power supply could significantly reduce the amount of ripple current in both the input and output capacitors. The RMS input ripple current is reduced by, and the effective ripple frequency is multiplied by, the number of phases used (assuming that the input voltage is greater than the number of phases used times the output voltage). The output ripple amplitude is also reduced by the number of phases used.

Input RMS Ripple Current Cancellation

Application Note 77 provides a detailed explanation of multiphase operation. The input RMS ripple current cancellation mathematical derivations are presented, and a graph is displayed representing the RMS ripple current reduction as a function of the number of interleaved phases (see Figure 4).

Soft-Start And Output Voltage Tracking

The TRACK/SS pin provides a means to either soft-start the regulator or track it to a different power supply. A capacitor on the TRACK/SS pin will program the ramp rate of the output voltage. An internal 1.25µA current source will charge up the external soft-start capacitor towards $INTV_{CC}$ voltage. When the TRACK/SS voltage is below 0.6V, it will take over the internal 0.6V reference voltage to control the output voltage. The total soft-start time can be calculated as:

$$t_{SS} = 0.6 \bullet \frac{C_{SS}}{1.25\mu A}$$

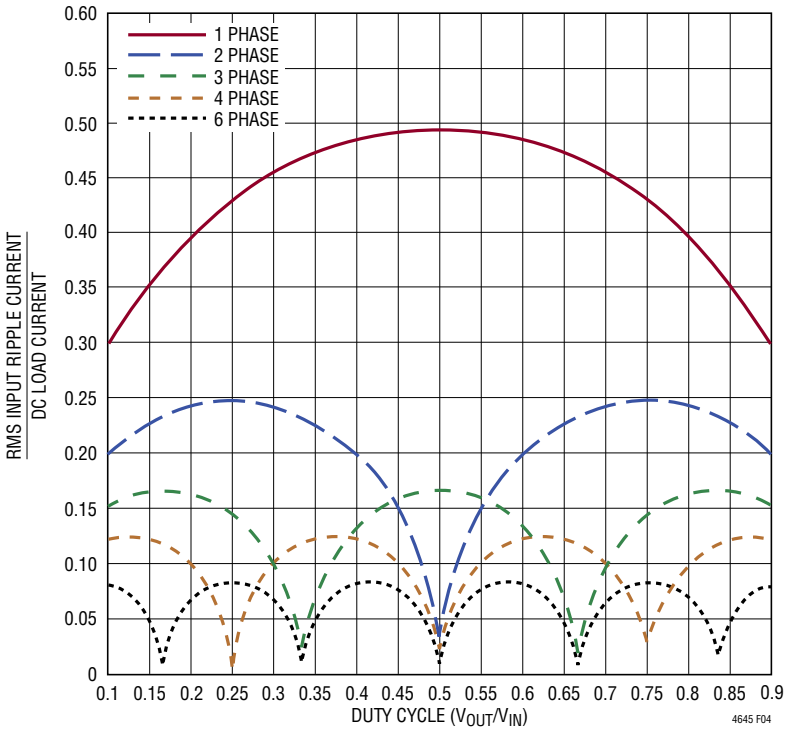


Figure 4. Normalized Input RMS Ripple Current vs Duty Cycle for One to Six µModule Regulators (Phases)

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where C_{SS} is the capacitance on the TRACK/SS pin. Current foldback and forced continuous mode are disabled during the soft-start process.

Output voltage tracking can also be programmed externally using the TRACK/SS pin. The output can be tracked up and down with another regulator. Figure 5 and Figure 6 show an example waveform and schematic of ratiometric tracking where the slave regulator's output slew rate is proportional to the master's.

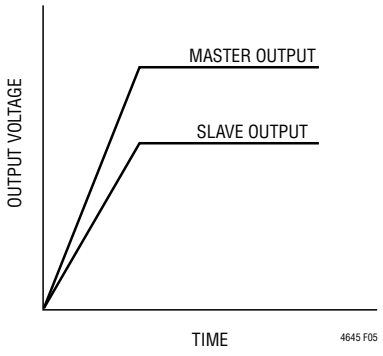


Figure 5. Output Ratiometric Tracking Waveform

Since the slave regulator's TRACK/SS is connected to the master's output through a $R_{TR(TOP)}/R_{TR(BOT)}$ resistor divider and its voltage used to regulate the slave output voltage when TRACK/SS voltage is below 0.6V, the slave output voltage and the master output voltage should satisfy the following equation during start-up:

$$V_{OUT(SL)} \bullet \frac{R_{FB(SL)}}{R_{FB(SL)} + 60.4k} =$$

$$V_{OUT(MA)} \bullet \frac{R_{TR(BOT)}}{R_{TR(TOP)} + R_{TR(BOT)}}$$

The $R_{FB(SL)}$ is the feedback resistor and the $R_{TR(TOP)}/R_{TR(BOT)}$ is the resistor divider on the TRACK/SS pin of the slave regulator, as shown in Figure 6.

Following the previous equation, the ratio of the master's output slew rate (MR) to the slave's output slew rate (SR) is determined by:

$$\frac{MR}{SR} = \frac{\frac{R_{FB(SL)}}{R_{FB(SL)} + 60.4k}}{\frac{R_{TR(BOT)}}{R_{TR(TOP)} + R_{TR(BOT)}}}$$

For example, $V_{OUT(MA)}$ = 1.5V, MR = 1.5V/1ms and $V_{OUT(SL)}$ = 1.2V, SR = 1.2V/1ms, from the equation, we could solve that $R_{TR(TOP)}$ = 60.4k and $R_{TR(BOT)}$ = 40.2k are a good combination for the ratiometric tracking. The TRACK/SS pin will have the 2.5µA current source on when a resistive divider is used to implement tracking on the

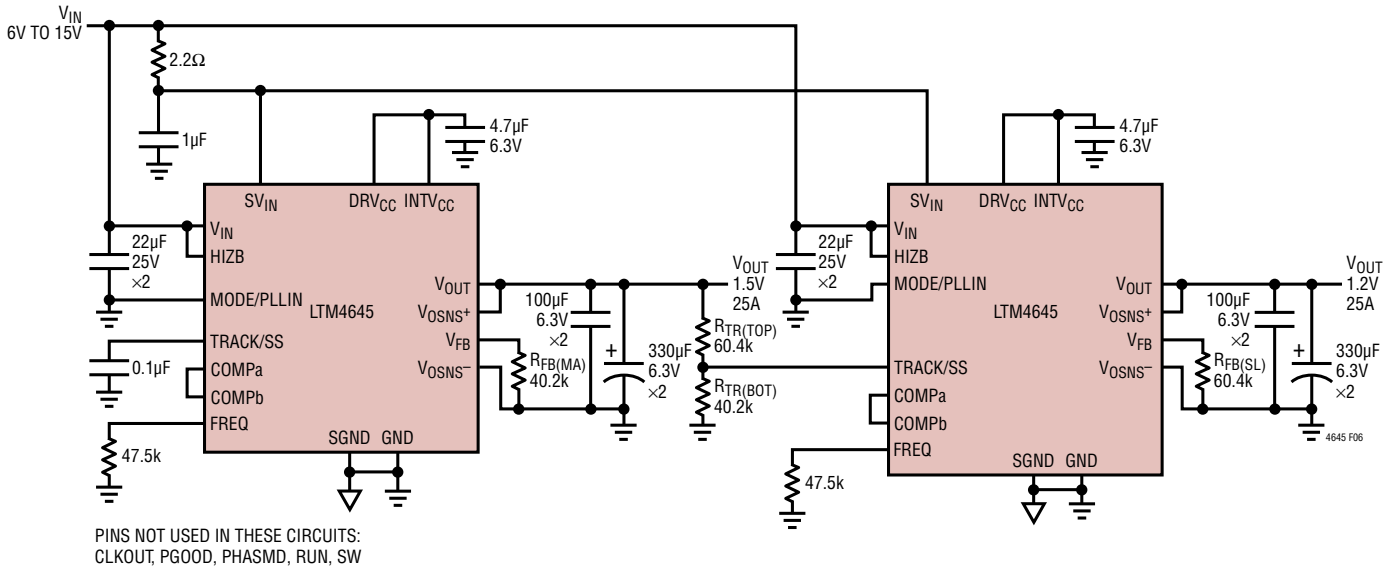


Figure 6. Example Schematic of Ratiometric Output Voltage Tracking

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slave regulator. This will impose an offset on the TRACK/SS pin input. Smaller value resistors with the same ratios as the resistor values calculated from the above equation can be used. For example, where the 60.4k is used then a 6.04k can be used to reduce the TRACK/SS pin offset to a negligible value.

The coincident output tracking can be recognized as a special ratiometric output tracking in which the master's output slew rate (MR) is the same as the slave's output slew rate (SR), waveform as shown in Figure 7.

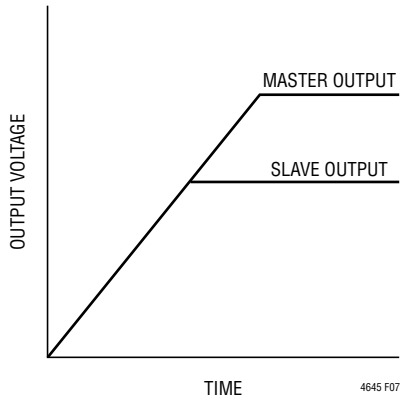


Figure 7. Output Coincident Tracking Waveform

From the equation, we could easily find that, in coincident tracking, the slave regulator's TRACK/SS pin resistor divider is always the same as its feedback divider:

$$\frac{R_{FB(SL)}}{R_{FB(SL)}+60.4k}=\frac{R_{TR(BOT)}}{R_{TR(TOP)}+R_{TR(BOT)}}$$

For example, $R_{TR(TOP)}$ = 60.4k and $R_{TR(BOT)}$ = 60.4k is a good combination for coincident tracking for a $V_{OUT(MA)}$ =1 .5V and $V_{OUT(SL)}$ = 1.2V application.

Run Enable

The RUN pin has an enable threshold of 1.45V maximum, typically 1.35V with 180mV of hysteresis. It controls the turn-on of the µModule. The RUN pin can be pulled up to V_{IN} for 5V operation, or a 5V Zener diode can be placed on the pin and a 10k to 100k resistor can be placed up to higher than 5V input for enabling the µModule. The RUN pin can also be used for output voltage sequencing.

In parallel operation the RUN pins can be tie together and controlled from a single control. The RUN pin can also be left floating. The RUN pin has a 1µA pull-up current source that increases to 5µA during ramp-up. Please note that the RUN pin has an ABSMAX voltage of 6V.

Differential Remote Sense Amplifier

An accurate differential remote sense amplifier is build into the LTM4645 to sense output voltages accurately at the remote load points. This is especially true for high current loads. It is very important that the V_{OSNS}^+ and V_{OSNS}^- are connected properly at the remote output sense point, and the feedback resistor R_{FB} is connected to between V_{FB} pin to V_{OSNS}^- pin. Review the schematics in Figure 23 for reference.

In multiphase single output application. Only one set of differential sensing amplifier and one set of feedback resistor are required while connecting RUN, TRACK/SS, V_{OUT}, V_{FB} and COMPa of different channels together. See Figure 25 for paralleling application.

Power Good

The PGOOD pins are open-drain pins that can be used to monitor valid output voltage regulation. This pin monitors a ±7.5% window around the regulation point. A resistor can be pulled up to a particular supply voltage no greater than 6V maximum for monitoring.

Overvoltage and Overcurrent Protection

The LTM4645 has over current protection (OCP) in a short circuit. The internal current comparator threshold folds back during a short to reduce the output current. An overvoltage condition (OVP) above 10% of the regulated output voltage will force the top MOSFET off and the bottom MOSFET on until the condition is cleared. Foldback current limit is disabled during soft-start or tracking start-up.

Pre-Biased Output Start-Up

In the application that require the power supply to start up with a pre-bias on the output capacitors, the LTM4645 module can safely power up into a pre-biased output without discharging it.

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The LTM4645 accomplishes this by disabling both the top and bottom MOSFETs until the TRACK/SS pin voltage and the internal soft-start voltage are above the V_{FB} pin voltage.

N+1 Phase Redundancy and Hot Swap

The HIZB pin can be used to force both top and bottom MOSFET to turn off while not pulling down the COMPa and TRACK/SS pins. In a multiphase system N+1 redundancy can be achieved via the HIZB pin. When combined with a hot swap controller, such as the LTC4211, the HIZB pin could be connected to the gate of the hot swap switch. When a damaged MOSFET triggers the hot swap controller, it also disables the corresponding channel's power, disconnecting it. Since COMPa and TRACK/SS pins are unaffected, it does not affect the rest of the system. The propagation delay from HIZB falling to both top and bottom MOSFET turned off is <200ns. See Figure 27 for example.

SW Pins and Snubbering Circuit

The SW pin is generally for testing purposes by monitoring the pin. The SW pin can also be used to dampen out switch node ringing caused by LC parasitic in the switched current path. Usually a series R-C combination is used called a snubber circuit. The resistor will dampen the resonance and the capacitor is chosen to only affect the high frequency ringing across the resistor.

If the stray inductance or capacitance can be measured or approximated then a somewhat analytical technique can be used to select the snubber values. The inductance is usually easier to predict. It combines the power path board inductance in combination with the MOSFET interconnect bond wire inductance.

First the SW pin can be monitored with a wide bandwidth scope with a high frequency scope probe. The ring frequency can be measured for its value. The impedance Z can be calculated:

$$Z_L = 2\pi \bullet f \bullet L$$

where f is the resonant frequency of the ring, and L is the total parasitic inductance in the switch path. If a resistor is selected that is equal to Z, then the ringing should be dampened. The snubber capacitor value is chosen so that its impedance is equal to the resistor at the ring frequency. Calculated by:

$$Z_C = \frac{1}{2\pi \bullet f \bullet C}$$

These values are a good place to start. Modification to these components should be made to attenuate the ringing with the least amount the power loss.

Stability Compensation

The LTM4645 has already been internally optimized and compensated for all output voltages and capacitor combinations including all ceramic capacitor applications when COMPb is tied to COMPa. Please note that a 22pF to 47pF feedforward capacitor (C_{FF}) is required connecting from V_{OUT} to V_{FB} pin for all ceramic capacitor application to achieve high bandwidth control loop compensation with enough phase margin. Table 5 is provided for most application requirements using the optimized internal compensation. For specific optimized requirement, disconnect COMPb from COMPa and apply a Type II C-R-C compensation network from COMPa to SGND to achieve external compensation. The LTpowerCAD design tool is available to download online to perform specific control loop optimization and analyze the control stability and load transient performance.

SV_{IN}, PV_{IN}, $INTV_{CC}$ AND DRV_{CC}

SV_{IN} is the filtered input voltage to the internal 5.5V LDO regulator to power the control circuitry of the regulator. Connect SV_{IN} to V_{IN} through a 2.2Ω and 1µF R-C filter.

$INTV_{CC}$ is the output of the 5.5V LDO. Decouple it with a minimum 2.2µF ceramic capacitor. Connect $INTV_{CC}$ to SV_{IN} directly if SV_{IN} is less than 6V.

PV_{IN} is the power input connected to power MOSFETs and the DRV_{CC} is the supply voltage for the driver circuity to drive both power MOSFETs. DRV_{CC} could connect to an

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external supply higher than 4.5V or V_{IN}(V_{IN} < 6V) directly through a 2.2Ω plus 1µF R-C filter. In the application with the input voltage 6V or above, DRV_{CC} could also connect to $INTV_{CC}$ 5.5V output directly.

See Figure 23 for a typical application circuit for input 6V or above. See Figure 24 for a typical application circuit for input from 4.7V to 5.5V.

Please note that $INTV_{CC}$ and DRV_{CC} has 6V ABSMAX voltage rating.

Temperature Monitoring

Measuring the absolute temperature of a diode is possible due to the relationship between current, voltage and temperature described by the classic diode equation:

$$I_D = I_S \bullet e\left(\frac{V_D}{\eta \bullet V_T}\right)$$

or

$$V_D = \eta \bullet V_T \bullet \ln\frac{I_D}{I_S}$$

where I_D is the diode current, V_D is the diode voltage, η is the ideality factor (typically close to 1.0) and I_S (saturation current) is a process dependent parameter. V_T can be broken out to:

$$V_T = \frac{k \bullet T}{q}$$

where T is the diode junction temperature in Kelvin, q is the electron charge and k is Boltzmann's constant. V_T is approximately 26mV at room temperature (298K) and scales linearly with Kelvin temperature. It is this linear temperature relationship that makes diodes suitable temperature sensors. The I_S term in the previous equation is the extrapolated current through a diode junction when the diode has zero volts across the terminals. The I_S term varies from process to process, varies with temperature, and by definition must always be less than I_D. Combining all of the constants into one term:

$$K_D = \frac{\eta \bullet k}{q}$$

where $K_D = 8.62 \bullet 10^{-5}$, and knowing $\ln(I_D/I_S)$ is always positive because I_D is always greater than I_S, leaves us with the equation that:

$$V_D = T(KELVIN) \bullet K_D \bullet \ln\frac{I_D}{I_S}$$

where V_D appears to increase with temperature. It is common knowledge that a silicon diode biased with a current source has an approximate –2mV/°C temperature relationship (Figure 8), which is at odds with the equation. In fact, the I_S term increases with temperature, reducing the $\ln(I_D/I_S)$ absolute value yielding an approximate –2mV/°C composite diode voltage slope.

To obtain a linear voltage proportional to temperature we cancel the I_S variable in the natural logarithm term to remove the I_S dependency from the equation 1. This is accomplished by measuring the diode voltage at two currents I_1, and I_2, where $I_1 = 10 \bullet I_2$) and subtracting we get:

$$\Delta V_D = T(KELVIN) \bullet K_D \bullet IN\frac{I_1}{I_S} - T(KELVIN) \bullet K_D \bullet IN\frac{I_2}{I_S}$$

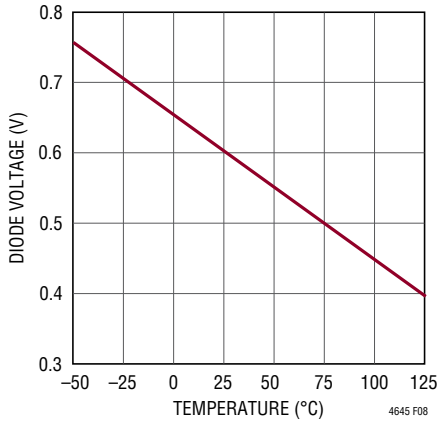


Figure 8. Diode Voltage V_D vs Temperature T(°C)

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Combining like terms, then simplifying the natural log terms yields:

$$\Delta V_D = T(KELVIN) \bullet K_D \bullet IN(10)$$

and redefining constant

$$K_D' = K_D \bullet IN(10) = \frac{198\mu V}{K}$$

yields

$$\Delta V_D = K'_D \bullet T(KELVIN)$$

Solving for temperature:

$$T(KELVIN) = \frac{\Delta V_D}{K_D'} \; (^{\circ}CELSIUS) = T(KELVIN) - 273.15$$

where

300°K = 27°C

means that is we take the difference in voltage across the diode measured at two currents with a ratio of 10, the resulting voltage is 198µV per Kelvin of the junction with a zero intercept at 0 Kelvin.

The diode connected PNP transistor between the $TEMP^+$ and $TEMP^-$ pin can be used to monitor the internal temperature of the LTM4645. See Figure 23 for an example.

Thermal Considerations

The thermal resistances reported in the Pin Configuration section of the data sheet are consistent with those parameters defined by JESD51-12 and are intended for use with finite element analysis (FEA) software modeling tools that leverage the outcome of thermal modeling, simulation, and correlation to hardware evaluation performed on an µModule package mounted to a hardware test board. The motivation for providing these thermal coefficients in found in JESD 51-12 ("Guidelines for Reporting and Using Electronic Package Thermal Information").

Many designers may opt to use laboratory equipment and a test vehicle such as the demo board to predict the µModule regulator's thermal performance in their application at various electrical and environmental operating conditions to compliment any FEA activities. Without FEA software, the thermal resistances reported in the Pin Configuration section are, in and of themselves, not relevant to providing guidance of thermal performance; instead, the derating curves provided in this data sheet can be used in a manner that yields insight and guidance pertaining to one's application usage, and can be adapted to correlate thermal performance to one's own application.

The Pin Configuration section gives four thermal coefficients explicitly defined in JESD 51-12; these coefficients are quoted or paraphrased below:

1. θ_{JA}, the thermal resistance from junction to ambient, is the natural convection junction-to-ambient air thermal resistance measured in a one cubic foot sealed enclosure. This environment is sometimes referred to as "still air" although natural convection causes the air to move. This value is determined with the part mounted to a 95mm × 76mm PCB with six layers.
2. $\theta_{JCbottom}$, the thermal resistance from junction to the bottom of the product case, is determined with all of the component power dissipation flowing through the bottom of the package. In the typical µModule regulator, the bulk of the heat flows out the bottom of the package, but there is always heat flow out into the ambient environment. As a result, this thermal resistance value may be useful for comparing packages but the test conditions don't generally match the user's application.
3. θ_{JCtop}, the thermal resistance from junction to top of the product case, is determined with nearly all of the component power dissipation flowing through the top of the package. As the electrical connections of the typical µModule regulator are on the bottom of the package, it is rare for an application to operate such that most of the heat flows from the junction to the top of the part. As in the case of $\theta_{JCbottom}$, this value may be useful for comparing packages but the test conditions don't generally match the user's application.
4. θ_{JB}, the thermal resistance from junction to the printed circuit board, is the junction-to-board thermal resistance where almost all of the heat flows through the bottom of the µModule package and into the board, and is really the sum of the $\theta_{JCbottom}$ and the thermal resistance of the bottom of the part through the solder joints and a portion of the board. The board temperature is measured a specified distance from the package.

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A graphical representation of the aforementioned thermal resistances is given in Figure 9; blue resistances are contained within the µModule regulator, whereas green resistances are external to the µModule package. As a practical matter, it should be clear to the reader that no individual or sub-group of the four thermal resistance parameters defined by JESD 51-12 or provided in the Pin Configuration section replicates or conveys normal operating conditions of a µModule regulator. For example, in normal board-mounted applications, never does 100% of the device's total power loss (heat) thermally conduct exclusively through the top or exclusively through bottom of the µModule package—as the standard defines for θ_{JCtop} and $\theta_{JCbottom}$, respectively. In practice, power loss is thermally dissipated in both directions away from the package—granted, in the absence of a heat sink and airflow, a majority of the heat flow is into the board.

Within the LTM4645, be aware there are multiple power devices and components dissipating power, with a consequence that the thermal resistances relative to different junctions of components or die are not exactly linear with respect to total package power loss. To reconcile this complication without sacrificing modeling simplicity—but also not ignoring practical realities—an approach has been taken using FEA software modeling along with laboratory testing in a controlled-environment chamber to reasonably define and correlate the thermal resistance values supplied in this data sheet: (1) Initially, FEA software is used to accurately build the mechanical geometry of the LTM4645 and the specified PCB with all of the correct material coefficients along with accurate power loss source definitions; (2) this model simulates a software-defined JEDEC environment consistent with JESD51-12 to predict power loss heat flow and temperature readings at different interfaces that enable the calculation of the JEDEC-defined thermal resistance values; (3) the model and FEA software is used to evaluate the LTM4645 with heat sink and airflow; (4) having solved for and analyzed these thermal resistance values and simulated various operating conditions in the software model, a thorough laboratory evaluation replicates the simulated conditions with thermocouples within a controlled-environment chamber while operating the device at the same power loss as that which was simulated. The outcome of this process and due diligence yields the set of derating curves shown in this data sheet.

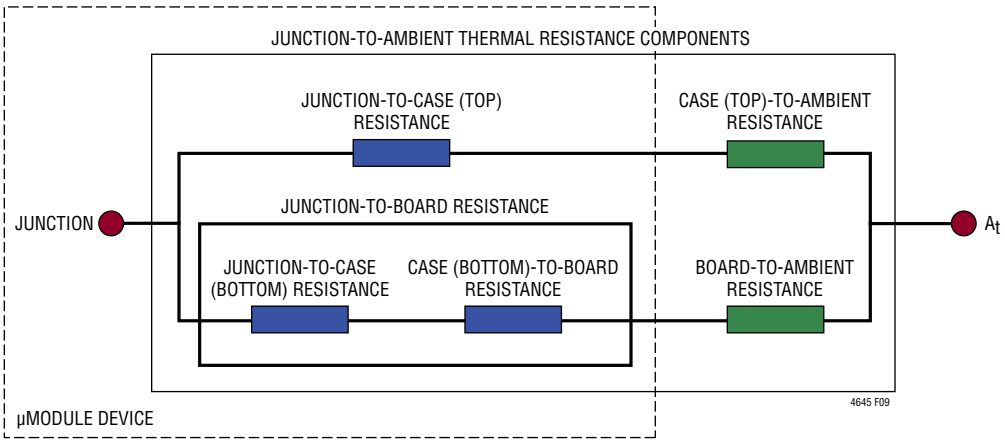


Figure 9. Graphical Representation of JESD51-12 Thermal Coefficients

APPLICATIONS INFORMATION

The LTM4645 has been designed to effectively remove heat from both the top and bottom of the package. The bottom substrate material has very low thermal resistance to the printed circuit board. An external heat sink can be applied to the top of the device for excellent heat sinking with airflow. Basically all power dissipating devices are mounted directly to the substrate and the top exposed metal. This provides two low thermal resistance paths to remove heat.

Figures 10 and 11 show the thermal images of the LTM4645 with no heat sink and no airflow running at 1V/25A and 1.8V/25A.

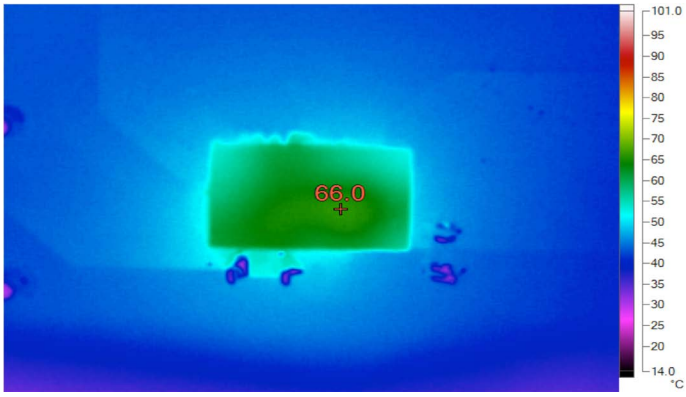


Figure 10. LTM4645 $12V_{IN}$ to $1V_{OUT}$ at 25A with No Air Flow and No Heat Sink

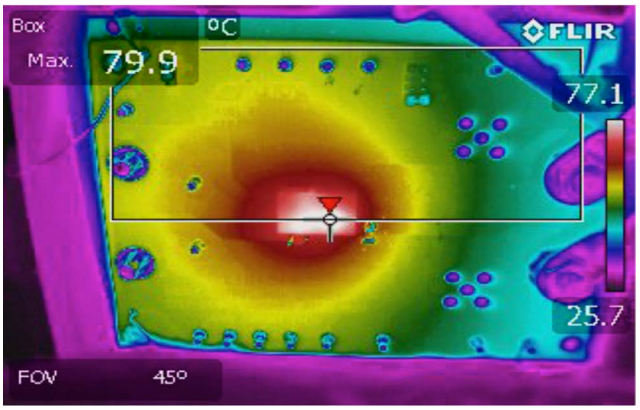


Figure 11. LTM4645 $12V_{IN}$ to $1.8V_{OUT}$ at 25A with No Air Flow and No Heat Sink

Safety Considerations

The LTM4645 modules do not provide isolation from V_{IN} to V_{OUT}. There is no internal fuse. If required, a slow blow fuse with a rating twice the maximum input current needs to be provided to protect each unit from catastrophic failure.

The fuse or circuit breaker should be selected to limit the current to the regulator during overvoltage in case of an internal top MOSFET fault. If the internal top MOSFET fails, then turning it off will not resolve the overvoltage, thus the internal bottom MOSFET will turn on indefinitely trying to protect the load. Under this fault condition, the input voltage will source very large currents to ground through the failed internal top MOSFET and enabled internal bottom MOSFET. This can cause excessive heat and board damage depending on how much power the input voltage can deliver to this system. A fuse or circuit breaker can be used as a secondary fault protector in this situation. The device does support over current protection. The $TEMP^+$ and $TEMP^-$ pins are provided for monitoring internal temperature, and can be used to detect the need for thermal shutdown that can be done by controlling the HIZB pin.

Output Current Derating

The 1V, 1.5V power loss curves in Figures 12 to 13 can be used in coordination with the load current derating curves in Figures 14 to 21 for calculating an approximate θ_{JA} thermal resistance for the LTM4645 with various heat sinking and airflow conditions. The power loss curves are taken at room temperature and are increased with a multiplicative factor according to the junction temperature, which is 1.3 for 120°C. The derating curves are plotted with the output current starting at 25A and the ambient temperature at ~30°C. The output voltages are 1V and 1.5V. These are chosen to include the lower and higher output voltage ranges for correlating the thermal resistance. Thermal models are derived from several temperature measurements in a controlled temperature chamber along with thermal modeling analysis. The junction temperatures are monitored while ambient temperature is increased with and without airflow. The power loss increase with

APPLICATIONS INFORMATION

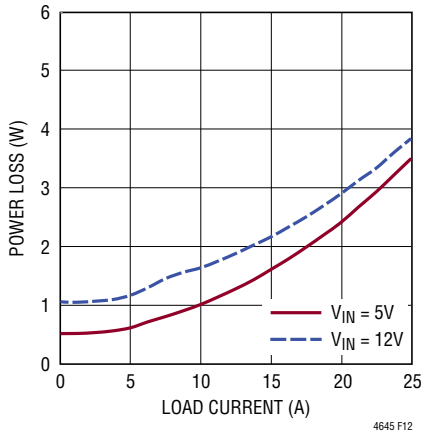


Figure 12. 1V Power Loss Curve

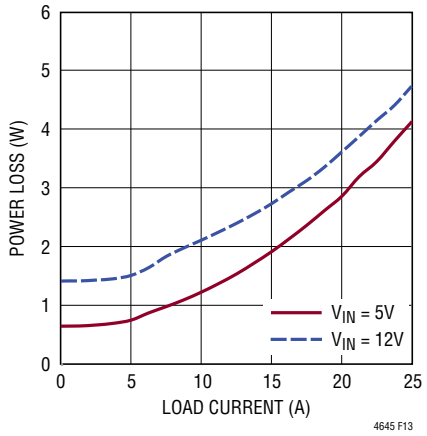


Figure 13. 1.5V Power Loss Curve

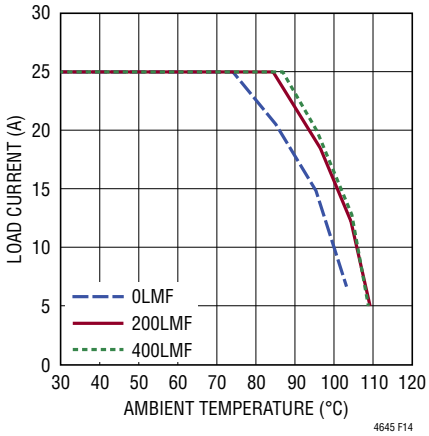


Figure 14. 12V to 1V Derating Curve, No Heat Sink

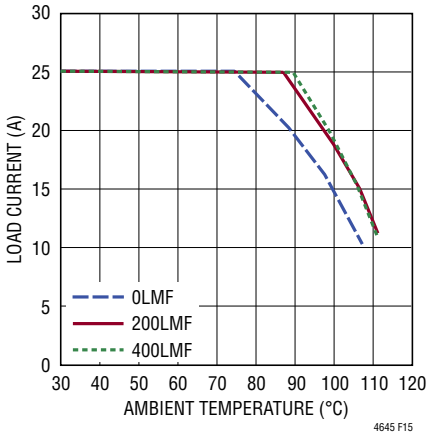


Figure 15. 5V to 1V Derating Curve, No Heat Sink

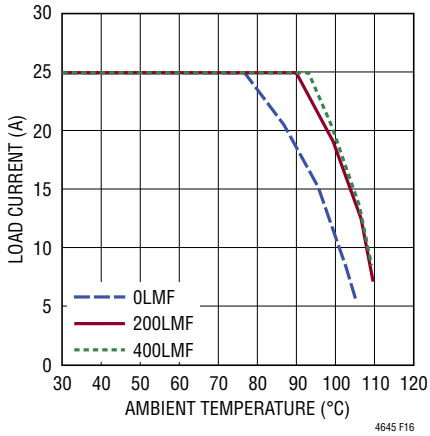


Figure 16. 12V to 1V Derating Curve, BGA Heat Sink

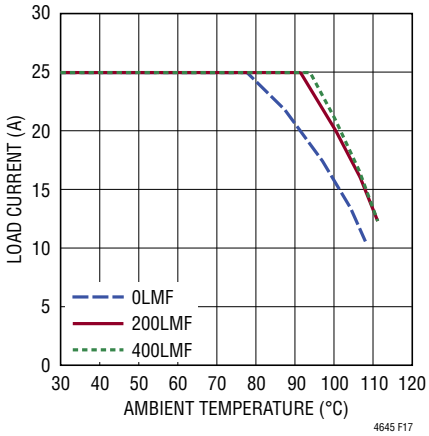


Figure 17. 5V to 1V Derating Curve, BGA Heat Sink

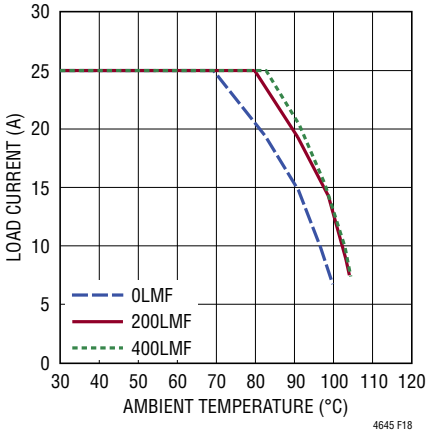


Figure 18. 12V to 1.5V Derating Curve, No Heat Sink

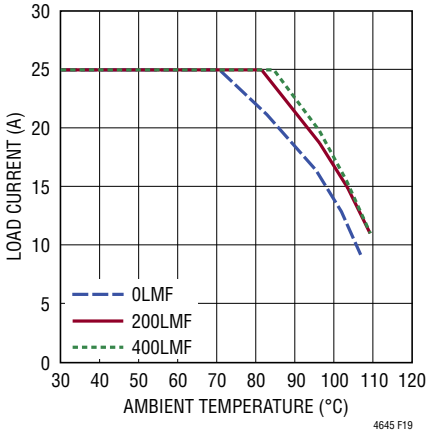


Figure 19. 5V to 1.5V Derating Curve, No Heat Sink

APPLICATIONS INFORMATION

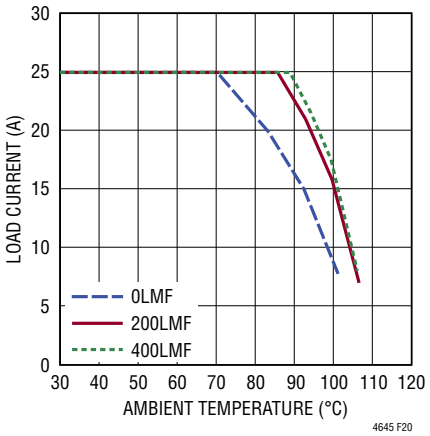


Figure 20. 12V to 1.5V Derating Curve, BGA Heat Sink

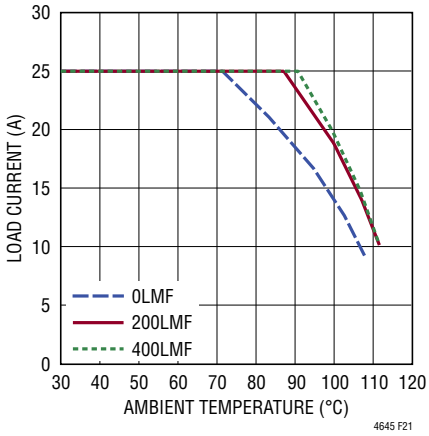


Figure 21. 5V to 1.5V Derating Curve, BGA Heat Sink

Table 3. 1.0V Output

DERATING CURVE	V_{IN} (V)	POWER LOSS CURVE	AIR FLOW (LFM)	HEAT SINK	θ_{JA} (°C/W)
Figures 14, 15	5, 12	Figure 12	0	None	9
Figures 14, 15	5, 12	Figure 12	200	None	6.5
Figures 14, 15	5, 12	Figure 12	400	None	6
Figures 16, 17	5, 12	Figure 12	0	BGA Heat Sink	8.5
Figures 16, 17	5, 12	Figure 12	200	BGA Heat Sink	5.5
Figures 16, 17	5, 12	Figure 12	400	BGA Heat Sink	5

Table 4. 1.5V Output

DERATING CURVE	V_{IN} (V)	POWER LOSS CURVE	AIR FLOW (LFM)	HEAT SINK	θ_{JA} (°C/W)
Figures 18, 19	5, 12	Figure 13	0	None	9
Figures 18, 19	5, 12	Figure 13	200	None	6.5
Figures 18, 19	5, 12	Figure 13	400	None	6
Figures 20, 21	5, 12	Figure 13	0	BGA Heat Sink	8.5
Figures 20, 21	5, 12	Figure 13	200	BGA Heat Sink	5.5
Figures 20, 21	5, 12	Figure 13	400	BGA Heat Sink	5

Heat Sink Manufacturer	Part Number	Website
Aavid Thermalloy	375424B00034G	www.aavid.com
Cool Innovations	4-050503P to 4-050508P	www.coolinnovations.com

APPLICATIONS INFORMATION

Table 5. Output Voltage Response vs Component Matrix (Refer to Figure 23) 0A to 7A Load Step Typical Measured Values

	C_{IN} VENDORS	VALUE	PART NUMBER	C_{OUT} VENDORS	VALUE	PART NUMBER
Bulk				Panasonic SP-CAP	470µF 2.5V	EEFSX0E471E4
				Panasonic POSCAP	470µF 2.5V	2R5TPD470M5
				Panasonic POSCAP	470µF 6.3V	6TPD470M5
Ceramic	Taiyo Yuden	22µF, 25V, 1206, X7S	C3216X7S0J226M	Murata	100µF, 6.3V, 1206, X5R	GRM31CR60J107M
	Murata	22µF, 25V,1206, X5R	GRM31CR61E226KE15L	TDK	100µF, 6.3V, 1206, X5R	C3216X5R0G107M
				Murata	220µF, 4V, 1206, X5R	GRM31CR60G227M
				Taiyo Yuden	220µF, 2.5V, 1206, X5R	PMK316DBJ227MLHT

Ceramic Cap Only

V_{IN} (V)	V_{OUT} (V)	C_{IN} (CERAMIC)	C_{OUT} (CERAMIC)	C_{OUT} (BULK)	C_{FF} (pF)	DROOP (mV)	P-P DEVIATION (mV)	RECOVERY TIME (µs)	LOAD STEP (A)	SLEW RATE (A/µs)	R_{FB} (kΩ)	FREQ (kHz)
5, 12	0.9	22µF × 3	100µF × 6	N/A	47pF	0	109	130	6	10	121	500
5, 12	1	22µF × 3	100µF × 6	N/A	47µF	0	102	130	6	10	90.9	600
5, 12	1.2	22µF × 3	100µF × 6	N/A	47µF	0	97	140	6	10	60.4	700
5, 12	1.5	22µF × 3	100µF × 6	N/A	47µF	0	100	140	6	10	40.2	800
5, 12	1.8	22µF × 3	100µF × 6	N/A	47µF	0	107	150	6	10	30.1	900

Bulk and Ceramic Cap

V_{IN} (V)	V_{OUT} (V)	C_{IN} (CERAMIC)	C_{OUT} (CERAMIC)	C_{OUT} (BULK)	C_{FF} (pF)	DROOP (mV)	P-P DEVIATION (mV)	RECOVERY TIME (µs)	LOAD STEP (A)	SLEW RATE (A/µs)	R_{FB} (kΩ)	FREQ (kHz)
5, 12	0.9	22µF × 3	47µF × 2	470µF	N/A	0	109	30	6	10	121	500
5, 12	1	22µF × 3	47µF × 2	470µF	N/A	0	107	40	6	10	90.9	600
5, 12	1.2	22µF × 3	47µF × 2	470µF	N/A	0	122	40	6	10	60.4	700
5, 12	1.5	22µF × 3	47µF × 2	470µF	N/A	0	131	50	6	10	40.2	800
5, 12	1.8	22µF × 3	47µF × 2	470µF	N/A	0	142	50	6	10	30.1	900

APPLICATIONS INFORMATION

ambient temperature change is factored into the derating curves. The junctions are maintained at ~120°C maximum while lowering output current or power with increasing ambient temperature. The decreased output current will decrease the internal module loss as ambient temperature is increased. The monitored junction temperature of 120°C minus the ambient operating temperature specifies how much module temperature rise can be allowed, as an example, in Figure 20 the load current is derated to 15A at 100°C with no air or heat sink and the power loss for the 12V to 1.5V at 15A output is about 3.5W. The 3.5W loss is calculated with the 2.7W room temperature loss from the 12V to 1.5V power loss curve at 15A, from Figure 13, and the 1.3 multiplying factor at 120°C junction. If the 100°C ambient temperature is subtracted from the 120°C junction temperature, then the difference of 20°C divided by 3.5W equals a 5.7°C/W θ_{JA} thermal resistance. Table 4 specifies a 5.5°C/W value which is very close. Tables 3 and 4 provide equivalent thermal resistances for 1.0V and 1.5V outputs with and without airflow and heat sinking. The derived thermal resistances in Tables 3 and 4 for the various conditions can be multiplied by the calculated power loss as a function of ambient temperature to derive temperature rise above ambient, thus maximum junction temperature. Room temperature power loss can be derived from the efficiency curves in the Typical Performance Characteristics section and adjusted with the above ambient temperature multiplicative factors. The printed circuit board is a 1.6mm thick six layer board with two ounce copper for all layers. The PCB dimensions are 95mm × 76mm. The BGA heat sinks are listed in Table 4.

Layout Checklist/Example

The high integration of LTM4645 makes the PCB board layout very simple and easy. However, to optimize its electrical and thermal performance, some layout considerations are still necessary.

- Use large PCB copper areas for high current paths, including V_{IN}, GND, and V_{OUT}. It helps to minimize the PCB conduction loss and thermal stress.
- Place high frequency ceramic input and output capacitors next to the V_{IN}, PGND and V_{OUT} pins to minimize high frequency noise.
- Place a dedicated power ground layer underneath the unit.
- To minimize the via conduction loss and reduce module thermal stress, use multiple vias for interconnection between top layer and other power layers.
- Do not put via directly on the pad, unless they are capped or plated over.
- Use a separated SGND ground copper area for components connected to signal pins. Connect the SGND to GND underneath the unit.
- For parallel modules, tie the V_{OUT}, V_{FB}, and COMP pins together. Use an internal layer to closely connect these pins together. The TRACK pin can be tied a common capacitor for regulator soft-start.
- Bring out test points on the signal pins for monitoring.

Figure 22 gives a good example of the recommended layout.

APPLICATIONS INFORMATION

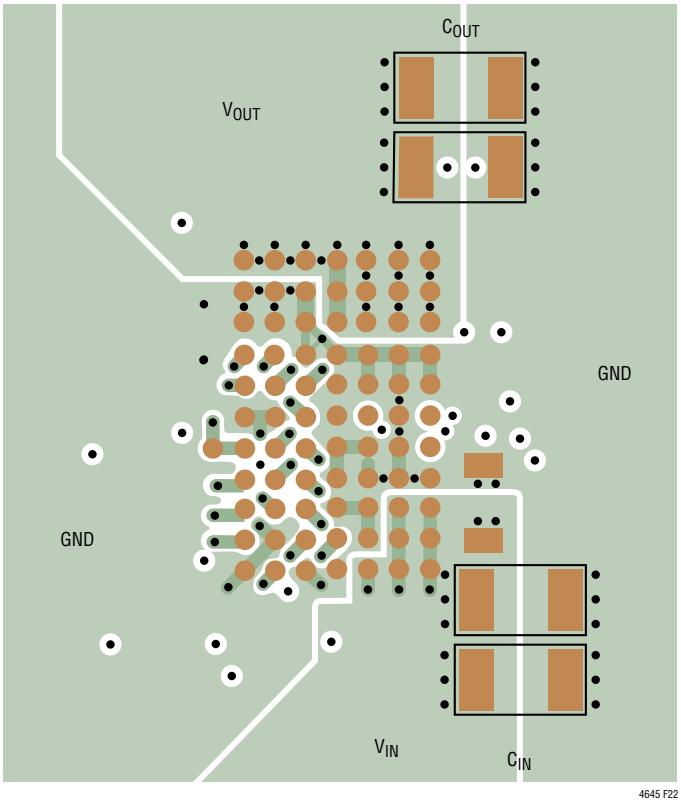


Figure 22. Recommended PCB Layout

TYPICAL APPLICATIONS

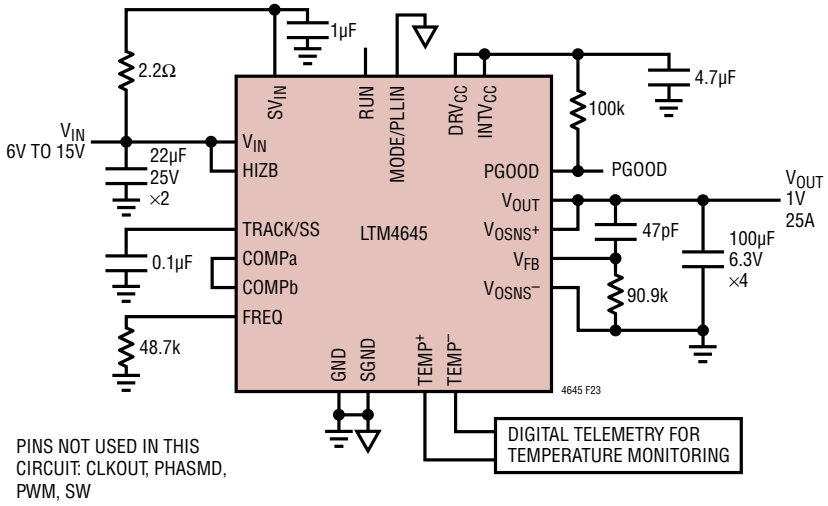


Figure 23. Typical 6V to 15V Input 1.0V at 25A Output Design

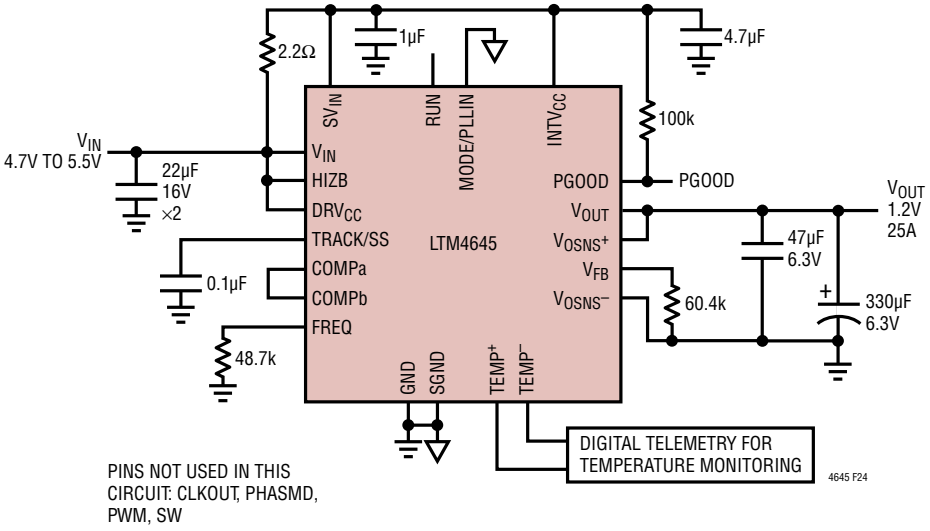


Figure 24. Typical 4.7V to 5.5V Input 1.2V at 25A Output Design

TYPICAL APPLICATIONS

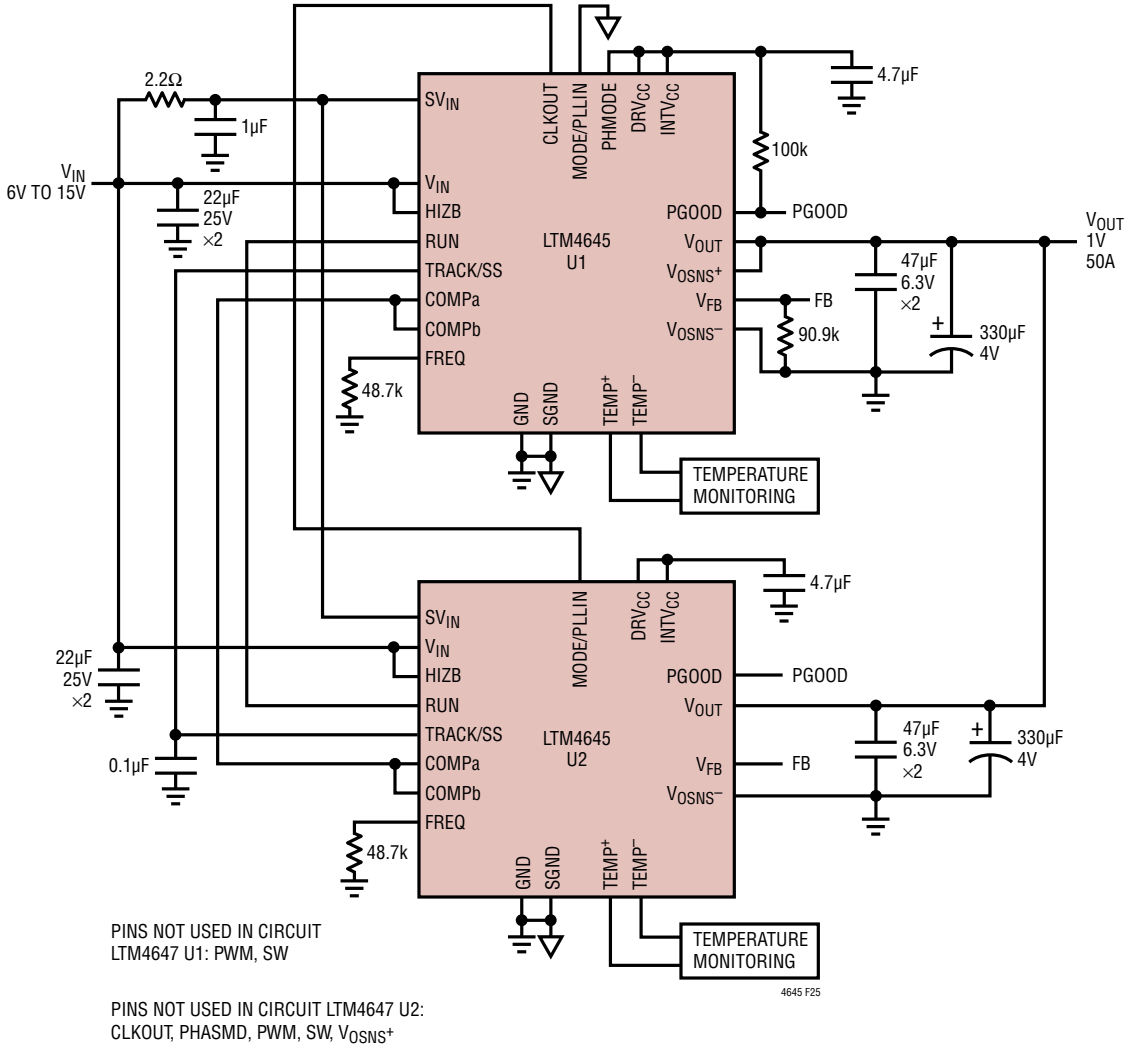
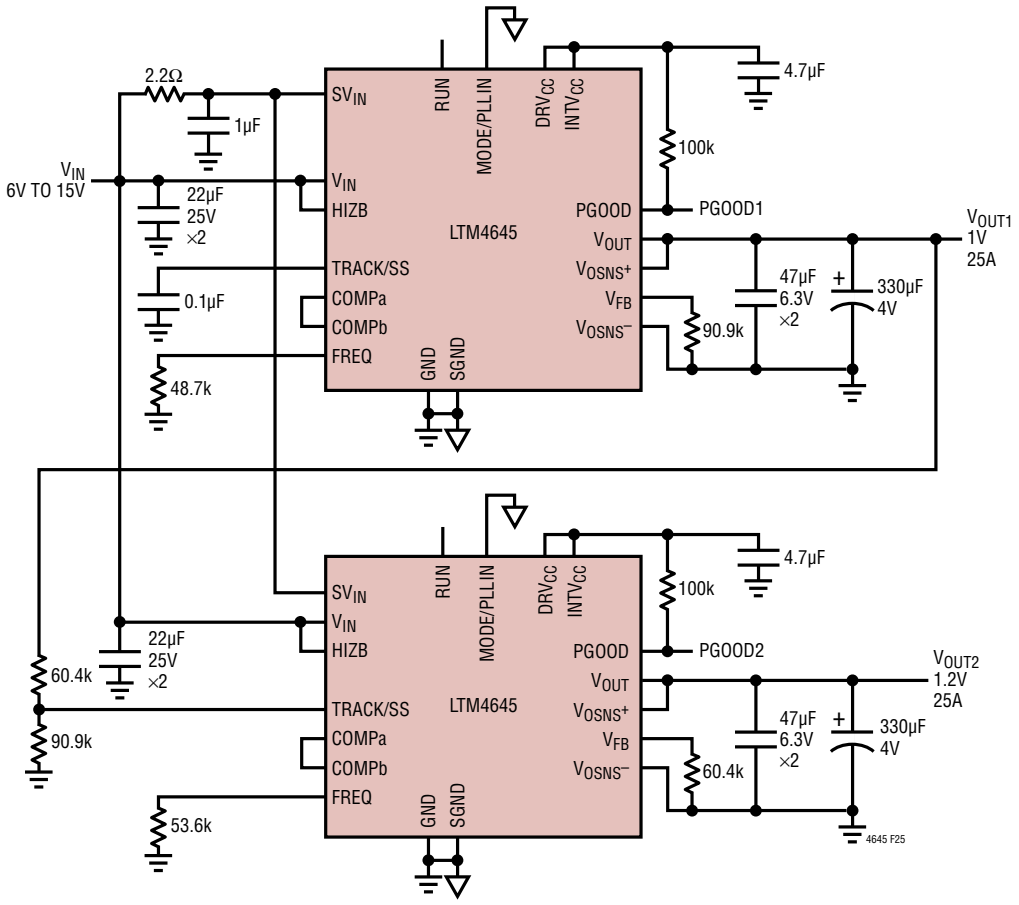


Figure 25. 6V to 15V Input, 1.0V Output at 50A

TYPICAL APPLICATIONS



PINS NOT USED IN LTM4647 U1 AND U2
CIRCUITS: CLKOUT, PHASMD, PWM, SW, TEMP+, TEMP–

Figure 26. 6V to 15V Input, 1.0V and 1.2V Output with Tracking

TYPICAL APPLICATIONS

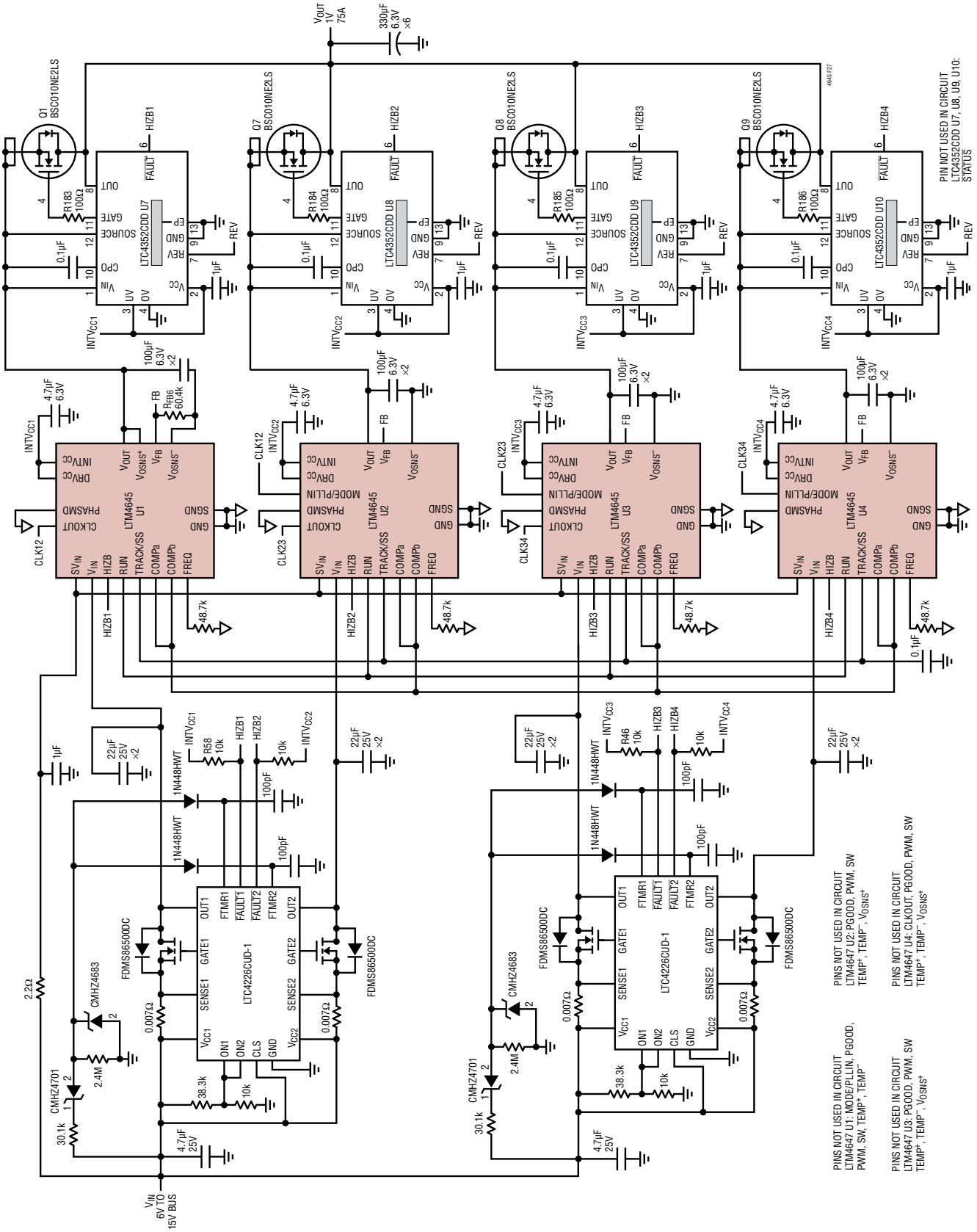


Figure 27. 3-Phase 1V at 75A Design with Extra 1 Phase 25A Redundancy

TYPICAL APPLICATIONS

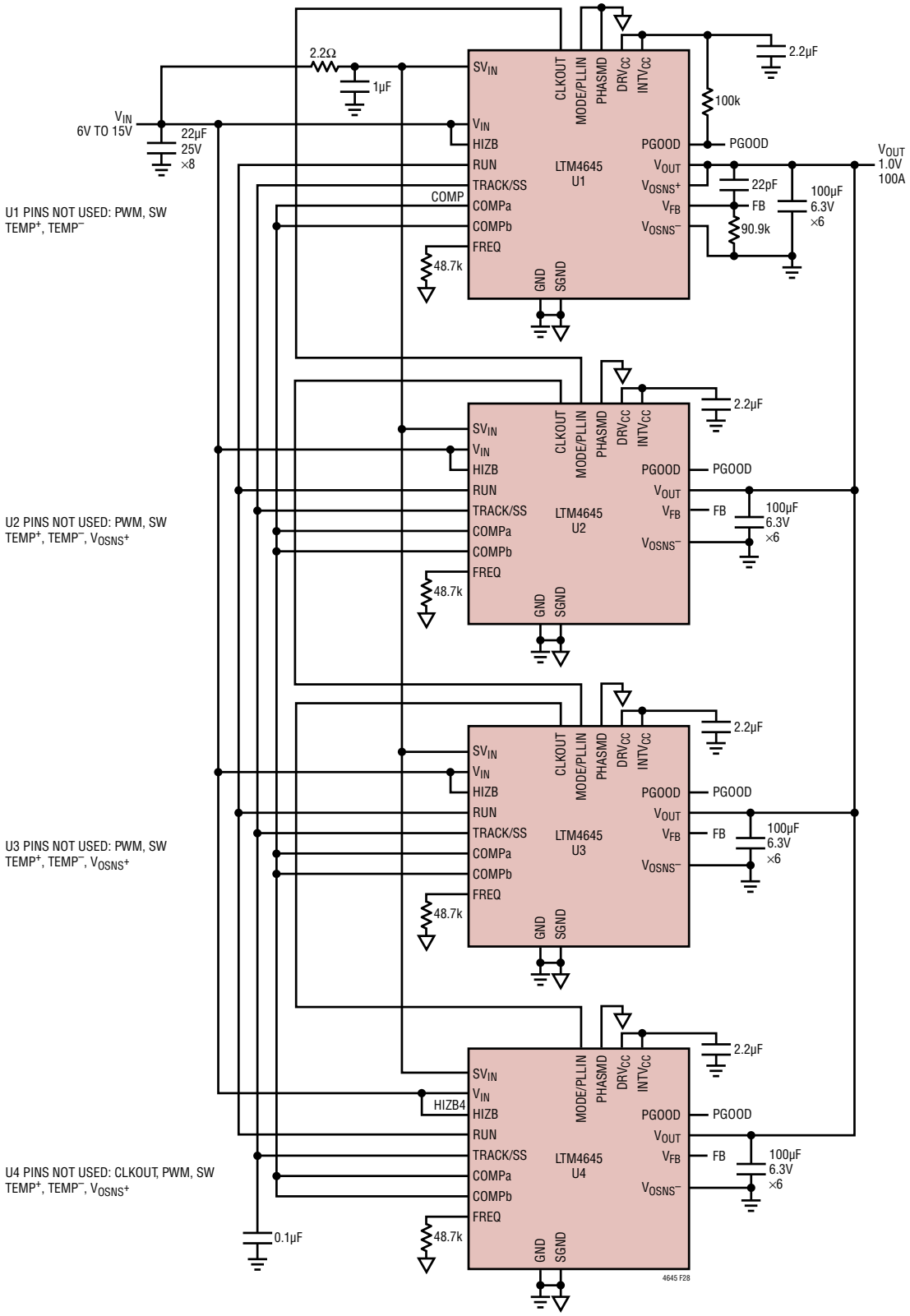


Figure 28. 4 Phase 1V at 100A Design

PACKAGE DESCRIPTION

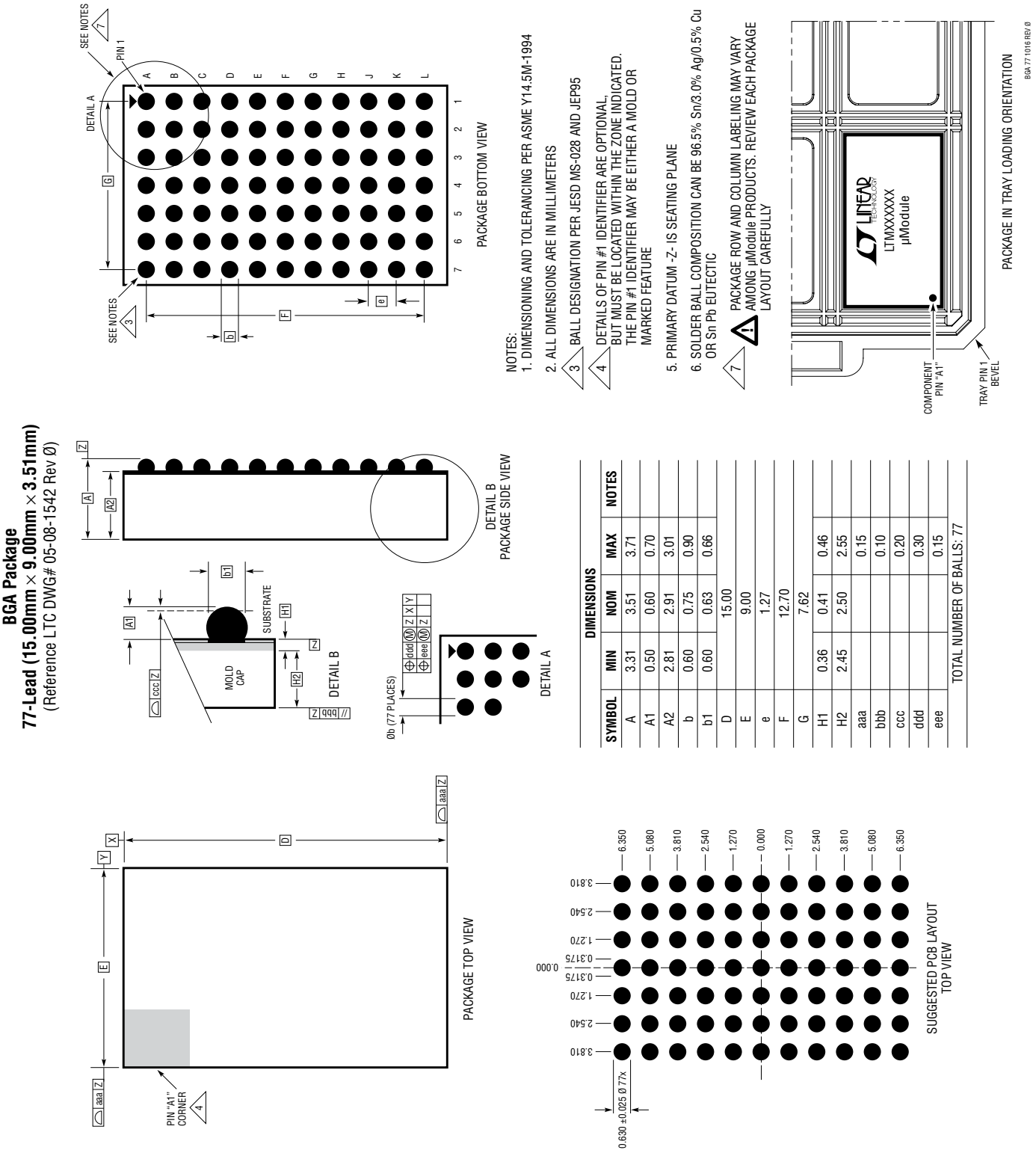
LTM4645 Component BGA Pinout

PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION
A1	V_{IN}	B1	V_{IN}	C1	V_{IN}	D1	GND	E1	$TEMP^{-}$	F1	$TEMP^{+}$
A2	V_{IN}	B2	V_{IN}	C2	V_{IN}	D2	GND	E2	GND	F2	GND
A3	V_{IN}	B3	GND	C3	GND	D3	GND	E3	GND	F3	SW
A4	GND	B4	PWM	C4	GND	D4	GND	E4	GND	F4	GND
A5	GND	B5	CLKOUT	C5	DRV_{CC}	D5	TEST2	E5	HIZB	F5	TRACK/SS
A6	RUN	B6	TEST1	C6	$INTV_{CC}$	D6	SV_{IN}	E6	V_{FB}	F6	GND
A7	GND	B7	MODE/PLLIN	C7	PHASMD	D7	FREQ	E7	SGND	F7	TEST3

PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION
G1	GND	H1	GND	J1	V_{OUT}	K1	V_{OUT}	L1	V_{OUT}
G2	GND	H2	GND	J2	V_{OUT}	K2	V_{OUT}	L2	V_{OUT}
G3	GND	H3	GND	J3	V_{OUT}	K3	V_{OUT}	L3	V_{OUT}
G4	GND	H4	GND	J4	V_{OUT}	K4	V_{OUT}	L4	V_{OUT}
G5	V_{OSNS}^{-}	H5	GND	J5	GND	K5	GND	L5	V_{OUT}
G6	V_{OSNS}^{+}	H6	COMPa	J6	GND	K6	GND	L6	V_{OUT}
G7	PGOOD	H7	COMPb	J7	GND	K7	GND	L7	V_{OUT}

PACKAGE DESCRIPTION

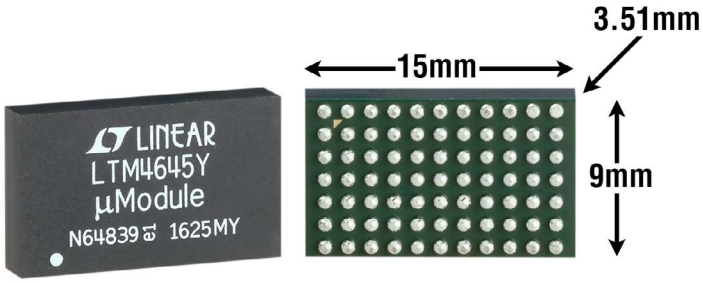
Please refer to http://www.linear.com/product/LTM4645#packaging for the most recent package drawings.



DIMENSIONS				
SYMBOL	MIN	NOM	MAX	NOTES
A	3.31	3.51	3.71	
A1	0.50	0.60	0.70	
A2	2.81	2.91	3.01	
b	0.60	0.75	0.90	
b1	0.60	0.63	0.66	
D		15.00		
E		9.00		
e		1.27		
F		12.70		
G		7.62		
H1	0.36	0.41	0.46	
H2	2.45	2.50	2.55	
aaa			0.15	
bbb			0.10	
ccc			0.20	
ddd			0.30	
eee			0.15	
TOTAL NUMBER OF BALLS: 77				

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

PACKAGE PHOTO



DESIGN RESOURCES

SUBJECT	DESCRIPTION	
µModule Design and Manufacturing Resources	Design: • Selector Guides • Demo Boards and Gerber Files • Free Simulation Tools	Manufacturing: • Quick Start Guide • PCB Design, Assembly and Manufacturing Guidelines • Package and Board Level Reliability
µModule Regulator Products Search	1. Sort table of products by parameters and download the result as a spread sheet. 2. Search using the Quick Power Search parametric table. Quick Power Search Input V_{in} (Min) V V_{in} (Max) V Output V_{out} V I_{out} A Search	
TechClip Videos	Quick videos detailing how to bench test electrical and thermal performance of µModule products.	
Digital Power System Management	Linear Technology's family of digital power supply management ICs are highly integrated solutions that offer essential functions, including power supply monitoring, supervision, margining and sequencing, and feature EEPROM for storing user configurations and fault logging.	

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTM4637	20A µModule Regulator	$4.5V \le V_{IN} \le 20V$, $0.6V \le V_{OUT} \le 5.5V$, 15mm × 15mm × 4.32mm (LGA), 15mm × 15mm × 4.92mm (BGA)
LTM4647	30A µModule Regulator, Pin Compatible with LTM4645	$4.7V \le V_{IN} \le 15V$, $0.6V \le V_{OUT} \le 1.8V$. 9mm × 15mm × 5.01mm (BGA)
LTM4636	40A µModule Regulator, ±1% V_{OUT} Accuracy	$4.75V \le V_{IN} \le 15V$, $0.6V \le V_{OUT} \le 3.3V$, 16mm × 16mm × 7.12mm (BGA)
LTM4631	Dual 10A, Single 20A µModule Regulator, 1.91mm Package Height	$4.5V \le V_{IN} \le 15V$, $0.6V \le V_{OUT} \le 1.8V$, 16mm × 16mm × 1.91mm (LGA)
LTM4620A	Dual 13A or Single 26A µModule Regulator, $V_{OUT} \le 5.3V$	$4.5V \le V_{IN} \le 15V$, $0.6V \le V_{OUT} \le 5.3V$, 15mm × 15mm × 4.41mm (LGA), 15mm × 15mm × 5.01mm (BGA)
LTM4630/ LTM4630-1	Dual 18A or Single 36A µModule Regulator, External Compensation(–1), ±0.8V V_{OUT} Accuracy (–1A)	$4.5V \le V_{IN} \le 15V$, $0.6V \le V_{OUT} \le 1.8V$, 16mm × 16mm × 4.41mm (LGA), 16mm × 16mm × 5.01mm (BGA)
LTM4630A	Dual 18A or Single 36A µModule Regulator, $V_{OUT} \le 5.3V$	$4.5V \le V_{IN} \le 15V$, $0.6V \le V_{OUT} \le 5.3V$, 16mm × 16mm × 4.41mm (LGA)
LTM4650/ LTM4650-1	Dual 25A or Single 50A µModule Regulator, External Compensation(–1), ±0.8V V_{OUT} Accuracy (–1A)	$4.5V \le V_{IN} \le 15V$, $0.6V \le V_{OUT} \le 1.8V$, 16mm × 16mm × 5.01mm (BGA)
LTM4650A	Dual 25A or Single 50A µModule Regulator, $V_{OUT} \le 5.5V$	$4.5V \le V_{IN} \le 16V$, $0.6V \le V_{OUT} \le 5.5V$. 16mm × 16mm × 5.01mm (BGA)
LTM4676A	Dual 13A or Single 26A µModule Regulator with PSM	$4.5V \le V_{IN} \le 17V$, $0.5V \le V_{OUT} \le 5.5V$, 16mm × 16mm × 5.01mm (BGA)
LTM4677	Dual 25A or Single 50A µModule Regulator with PSM	$4.5V \le V_{IN} \le 16V$, $0.5V \le V_{OUT} \le 1.8V$, 16mm × 16mm × 5.01mm (BGA)

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