Hybrid Step-Down Synchronous Controller

FEATURES

- **Wide V_{IN} Range: 10V to 72V (80V ABS Max)**
- **Soft Switching for Low Noise Operation**
- Phase-Lockable Fixed Frequency 200kHz to 1.5MHz
- ±1% Output Voltage Accuracy
- R_{SENSE} or DCR Current Sensing
- Programmable CCM, DCM, or Burst Mode® Operation
- CLKOUT Pin for Multiphase Operation
- Short Circuit Protected
- $EXTV_{CC}$ Input for Improved Efficiency
- Monotonic Output Voltage Start-Up
- Optional External Reference
- 32-Pin (5mm × 5mm) QFN

APPLICATIONS

- Intermediate Bus Converters
- High Current Distributed Power Systems
- Telecom, Datacom, and Storage Systems
- Automotive Applications

DESCRIPTION

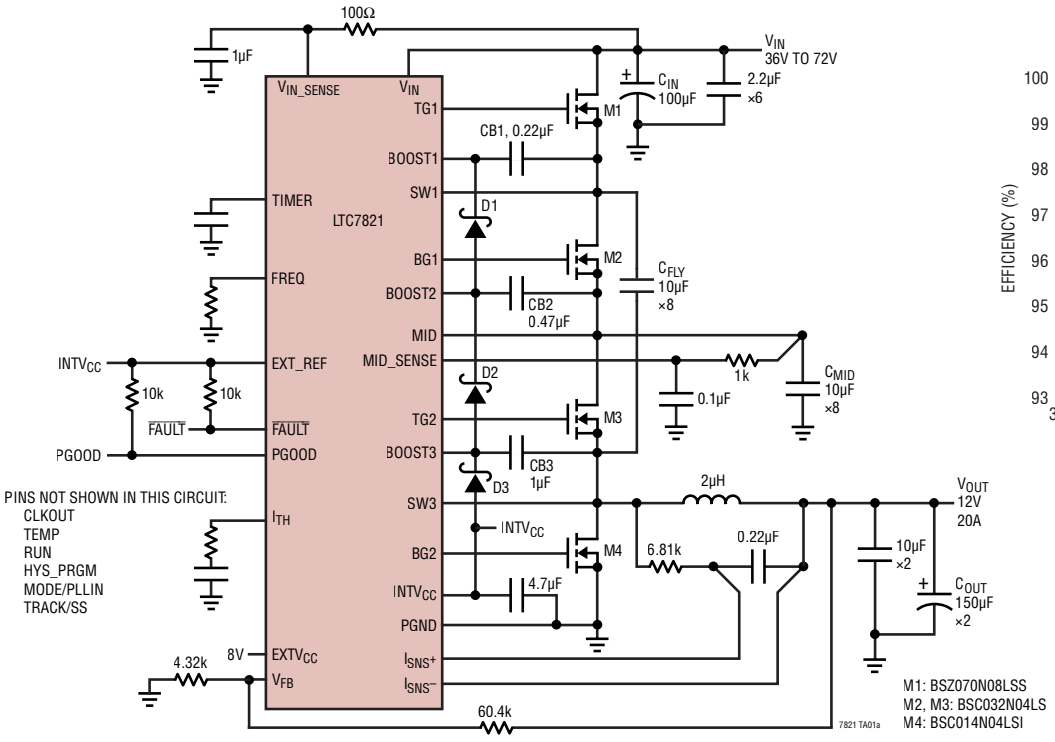
The LTC®7821 uses a proprietary architecture that merges a soft switching charge pump topology with a synchronous step-down converter to provide superior efficiency and EMI performance compared to traditional switching architectures.

In a typical 48V to 12V application, efficiency of greater than 97% is attainable with the LTC7821 switching at 500kHz. The same efficiency can only be achieved with a traditional controller switching at one-third the frequency. Higher switching frequencies allow the use of smaller inductances that yield faster transient response and smaller solution size.

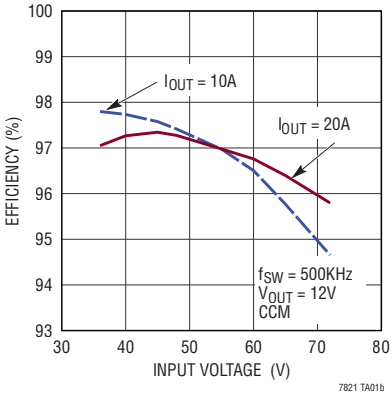
The LTC7821 can be easily paralleled to provide higher output currents with its accurate current sharing capability and frequency synchronization function.

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TYPICAL APPLICATION



Efficiency at Various V_{IN} for V_{OUT} = 12V



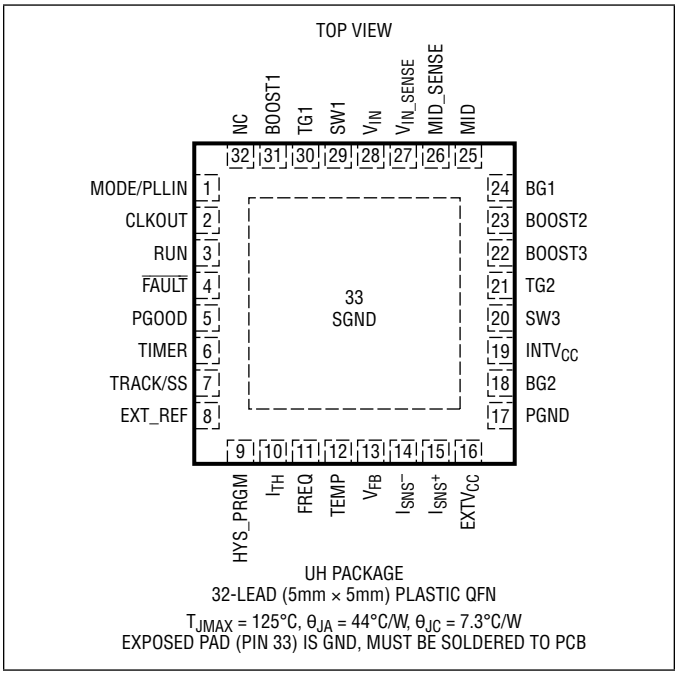
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ABSOLUTE MAXIMUM RATINGS

(Note 1)

Input Supply Voltage (V_{IN}, V_{IN_SENSE}) ..... –0.3V to 80V
Top Side Driver Voltages
  BOOST1 ..... –0.3V to 86V
  BOOST2, BOOST3 ..... –0.3V to 46V
Switch Voltages
  SW1 ..... 0V to 80V
  SW3 ..... –0.3V to 40V
MID, MID_SENSE ..... –0.3V to 40V
(BOOST1-SW1), (BOOST2-MID),
(BOOST3-SW3) ..... –0.3V to 6V
I_{SNS}^+, I_{SNS}^- ..... –0.3V to 40V
($I_{SNS}^+ - I_{SNS}^-$) ..... ±0.6V
$EXTV_{CC}$ ..... –0.3V to 40V
TEMP, FREQ, EXT_REF, V_{FB} ..... –0.3V to $INTV_{CC}$
HYS_PRGM, I_{TH}, RUN, TRACK/SS ..... –0.3V to $INTV_{CC}$
$\overline{FAULT}$, PGOOD ..... –0.3V to 80V
TIMER, MODE/PLLIN ..... –0.3V to $INTV_{CC}$
$INTV_{CC}$ Peak Output Current 100mA
Operating Junction Temperature Range
  (Notes 2, 3, 9) ..... –40°C to 125°C
Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



UH PACKAGE
32-LEAD (5mm × 5mm) PLASTIC QFN
T_{JMAX} = 125°C, θ_{JA} = 44°C/W, θ_{JC} = 7.3°C/W
EXPOSED PAD (PIN 33) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

http://www.linear.com/product/LTC7821#orderinfo

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC7821EUH#PBF	LTC7821EUH#TRPBF	7821	32-Lead (5mm × 5mm) Plastic QFN	–40°C to 125°C
LTC7821IUH#PBF	LTC7821IUH#TRPBF	7821	32-Lead (5mm × 5mm) Plastic QFN	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{IN} = V_{IN_SENSE} = 48V, V_{RUN} = 5V, $EXTV_{CC}$ = 9V, EXT_REF = 5.6V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Main Control Loops							
V_{IN}	Input Voltage Range			10		72	V
	Output Voltage Range	(Note 4)		0.9		$\frac{V_{IN}}{2} - 2.5$	V
V_{FB}	Regulated Feedback Voltage	I_{TH} Voltage (Note 5)	●	0.792	0.8	0.808	V
I_{FB}	Feedback Current	(Note 5)			±10	±50	nA
$V_{REFLNREG}$	Reference Voltage Line Regulation	V_{IN} = 36V to 72V (Note 5)			0.003	0.02	%/V
$V_{LOADREG}$	Output Voltage Load Regulation	(Note 5) ΔI_{TH} Voltage = 1.2V to 0.7V ΔI_{TH} Voltage = 1.2V to 1.6V	 ● ●		 0.016 –0.016	 0.1 –0.1	 % %
g_m	Transconductance Amplifier g_m	I_{TH} = 1.2V; Sink/Source 5µA (Note 5)			2		mmho
I_{VIN}	Input DC Supply Current Normal Mode Shutdown Precharging Phase	(Note 6) V_{RUN} = 0V, $EXTV_{CC}$ = 0V V_{IN} = 20V, V_{MID} = V_{MID_SENSE} = 9V, V_{SW1} = 15V, V_{SW3} = 10V V_{IN} = 48V, V_{MID} = V_{MID_SENSE} = 20V, $V_{SW1} \geq$ 36V, V_{SW3} = 12V			 0.5 240 40 84		 mA µA mA mA
I_{VIN_SENSE}	Input DC Supply Current Normal Mode Shutdown	(Note 6) V_{RUN} = 0V			 1 45		 mA µA
I_{EXTVCC}	Input DC Supply Current	(Note 6)			2.2		mA
I_{MID}	MID Pin Current				45		µA
I_{MID_SENSE}	MID_SENSE Pin Current				4		µA
V_{UVLO}	V_{IN} Undervoltage Lockout	V_{IN} Ramping Up	●		8.8	9.4	V
V_{UVLO_HYST}	UVLO Hysteresis				0.28		V
V_{SENSE}	Current Sense Threshold	V_{ISNS^-} = 0V	●	45	50	55	mV
$I_{SNS+/-}$	$ISNS^+$ and $ISNS^-$ Pin Current	V_{ISNS^+} = V_{ISNS^-} = 12V	●			1.2	µA
$I_{TRACK/SS}$	Soft-Start Charge Current	$V_{TRACK/SS}$ = 0V		–9	–10	–11	µA
V_{RUN_ON}	RUN Pin On Threshold	V_{RUN} Rising	●	1.1	1.3	1.6	V
I_{RUN}	RUN Pin Current	V_{RUN} = 0V			1		µA
V_{RUN_HYST}	RUN Pin Hysteresis				0.1		V
$V_{EXT_REF_UC}$	EXT_REF Upper Clamp Limit	(Note 5)	●	0.85	0.9		V
$V_{EXT_REF_LC}$	EXT_REF Lower Clamp Limit	(Note 5)	●		0.40	0.45	V
$V_{SEL_EXT_REF}$	EXT_REF De-Select Threshold (Ramping Up)				1.3		V
I_{EXT_REF}	EXT_REF Pin Current	V_{EXT_REF} = 0.6V		–150			nA
V_{TEMP_TRIP}	TEMP Pin Trip Point, Rising		●		1.22	1.25	V
$V_{TEMP_TRIP_HYST}$	TEMP Pin Trip Point Hysteresis				100		mV
I_{TEMP}	TEMP Pin Current	V_{TEMP} = 1V			1		nA
$V_{BSTUVLO}$	Undervoltage Lockout of (BOOST1-SW1), (BOOST2- V_{MID}) and (BOOST3-SW3)	Difference Voltage, Rising			4.4		V
$V_{BSTUVLO_HYST}$	Bootstrap Undervoltage Lockout Hysteresis				1.4		V
T_{OUT}	TEMP Trip TimeOut				100		ms

ELECTRICAL CHARACTERISTICS

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SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$INTV_{CC}$ Linear Regulator							
V_{INTVCC}	Internal V_{CC} Regulator	10V < V_{IN} < 72V, V_{EXTVCC} = 0V		5.65	5.8	5.95	V
V_{LDOINT}	$INTV_{CC}$ Load Regulation	I_{CC} = 1mA to 50mA, V_{IN} = 12V, V_{EXTVCC} = 0V			–0.6	–2	%
V_{EXTVCC}	$EXTV_{CC}$ Switchover Voltage	$EXTV_{CC}$ Ramping Positive, I_{CC} = 1mA			7		V
V_{EXTVCC_HYS}	$EXTV_{CC}$ Switchover Voltage Hysteresis				200		mV
V_{LDOEXT}	$EXTV_{CC}$ Load Regulation	V_{EXTVCC} = 12V, I_{CC} = 1mA to 50mA			–0.6	–2	%
Oscillator and Phase Lock Loop							
f_{NOM}	Nominal Frequency	R_{FREQ} = 68kΩ		440	490	550	kHz
f_{LOW}	Lowest Frequency	V_{FREQ} = 0V		20	50	100	kHz
f_{HIGH}	Highest Frequency	V_{FREQ} = $INTV_{CC}$		1400	1700	2000	kHz
f_{SYNC_LOW}	Lowest Synchronizing Frequency			200			kHz
f_{SYNC_HIGH}	Highest Synchronizing Frequency					1500	KHz
I_{FREQ}	Frequency Setting Current	V_{FREQ} = 0V	●	–9	–10	–11	µA
$R_{MODE/PLLIN}$	MODE/PLLIN Resistance				250		kΩ
$CLKOUT_{HIGH}$	CLKOUT High Amplitude				2.4		V
$CLKOUT_{LOW}$	CLKOUT Low Amplitude				0		V
PGOOD Output							
V_{PG1}	PGOOD 1st Trip Level (with Delay)	V_{FB} with Respect to Regulated Voltage V_{FB} Ramping Up (Overvoltage 1st Level) V_{FB} Ramping Down (Undervoltage 1st Level)		 6 –5.5	 8.5 –7.5	 11 –9.5	 % %
V_{PG1_HYST}	PGOOD 1st Trip Level Hysteresis (with Delay)				15		mV
V_{PG2}	PGOOD 2nd Trip Level	V_{FB} with Respect to Regulated Voltage V_{FB} Ramping Up (Overvoltage 2nd Level) V_{FB} Ramping Down (Undervoltage 2nd Level)			 15 –25		 % %
V_{PG2_HYST}	PGOOD 2nd Trip Level Hysteresis				15		mV
V_{PGL}	PGOOD Voltage Low	I_{PGOOD} = 0.6mA			0.4	0.5	V
I_{PGOOD}	PGOOD Leakage Current	V_{PGOOD} = 80V				1	µA
Capacitor Balancing							
V_{TIMER_LOW}	Voltage At TIMER Pin To Start Capacitor Balancing				0.5		V
V_{TIMER_HIGH}	Voltage At TIMER Pin To Stop Capacitor Balancing				1.25		V
I_{TIMER}	TIMER Pin Charge Current	V_{TIMER} = 0.9V V_{TIMER} = 2.8V	● ●	–6 –3	–7 –3.5	–8 –4	µA µA
V_{HYS_PRGM}	Capacitor Balancing Window Comparator Threshold	V_{HYS_PRGM} = 0V V_{HYS_PRGM} = 1.2V V_{HYS_PRGM} = $INTV_{CC}$			±0.3 ±1.2 ±0.8		V V V
I_{HYS_PRGM}	HYS_PRGM Pin Current	V_{HYS_PRGM} = 0V	●	–9	–10	–11	µA
$V_{\overline{FAULT}}$	$\overline{FAULT}$ Pin Voltage Low	$I_{\overline{FAULT}}$ = 0.6mA			0.2	0.4	V
$I_{\overline{FAULT}}$	$\overline{FAULT}$ Leakage Current	$V_{\overline{FAULT}}$ = 80V				1	µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{IN} = V_{IN_SENSE} = 48V, V_{RUN} = 5V, $EXTV_{CC}$ = 9V, EXT_REF = 5.6V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$I_{FLYSRC1}$	Current Out of SW1 During Capacitor Balancing	(V_{SW1} – V_{SW3}) < V_{IN}/2, V_{SW3} = 12V			40		mA
$I_{FLYSNK1}$	Current into SW1 During Capacitor Balancing	(V_{SW1} – V_{SW3}) > V_{IN}/2, V_{SW3} = 12V			6		mA
$I_{FLYSNK3}$	Current into SW3 During Capacitor Balancing	(V_{SW1} – V_{SW3}) < V_{IN}/2, V_{SW3} = 12V			40		mA
$I_{FLYSRC3}$	Current Out of SW3 During Capacitor Balancing	(V_{SW1} – V_{SW3}) < V_{IN}/2, V_{SW3} = 12V			6		mA
I_{MID_SRC}	Current Out of MID During Capacitor Balancing	V_{MID} < V_{IN}/2, V_{MID} = V_{MID_SENSE} = 20V V_{SW1} ≥ 36V, V_{SW3} = 12V			60		mA
I_{MID_SNK}	Current into MID During Capacitor Balancing	V_{MID} > V_{IN}/2, V_{MID} = V_{MID_SENSE} = 28V V_{SW1} ≥ 36V, V_{SW3} = 12V			40		mA
Gate Driver							
TG1,2	Pull-Up ON Resistance Pull-Down ON Resistance				2 1		Ω Ω
BG1, 2	Pull-Up ON Resistance Pull-Down ON Resistance				2 1		Ω Ω
TG1,2 t_r TG1,2 t_f	TG1, TG2 Transition Time: Rise Time Fall Time	(Note 7)			 4 4		 ns ns
BG1,2 t_r BG1,2 t_f	BG1, BG2 Transition Time: Rise Time Fall Time	(Note 7)			 4 4		 ns ns
T_{1D}	TG1 Off to BG1 On				45		ns
T_{2D}	TG2 Off to BG2 On				20		ns
T_{3D}	TG1 Off to TG2 Off				25		ns
T_{4D}	BG1 Off to TG1 On				40		ns
T_{5D}	BG2 Off to TG2 On				20		ns
T_{6D}	BG1 Off to BG2 Off				20		ns
$t_{on(MIN)}$	Minimum On-Time	(Note 8)			210		ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC7821E is guaranteed to meet performance specifications from 0°C to 85°C. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC7821I is guaranteed to meet performance specifications over the full –40°C to 125°C operating junction temperature range. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors.

Note 3: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formulas:

LTC7821UH: $T_J = T_A + (P_D \bullet 44°C/W)$

Note 4: Output voltage range is guaranteed by design. For output voltage setting, read "Output Voltage Setting" and "Minimum V_{OUT}" in the "Applications Information" section.

Note 5: The LTC7821 is tested in a feedback loop that servos V_{ITH} to a specified voltage and measures the resultant V_{FB}.

Note 6: Dynamic supply current is higher due to the gate charge being delivered at the switching frequency. See Applications Information.

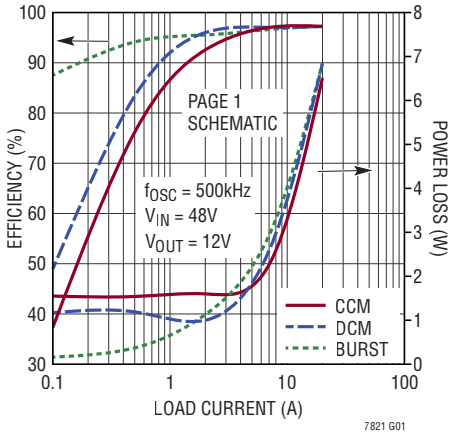
Note 7: Rise and fall times are measured using 10% and 90% levels. Delay times are measured using 50% levels.

Note 8: The minimum on-time condition is specified for an inductor peak-to-peak ripple current ≥ 40% of I_{MAX} (see Minimum On-Time Considerations in the Applications Information section)

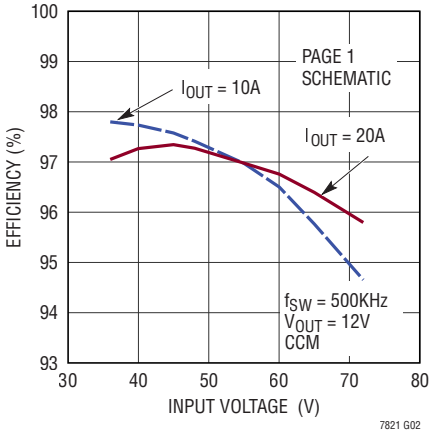
Note 9: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C when overtemperature protection is active. Continuous operation above the specified maximum junction temperature may impair device reliability or permanently damage the device.

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

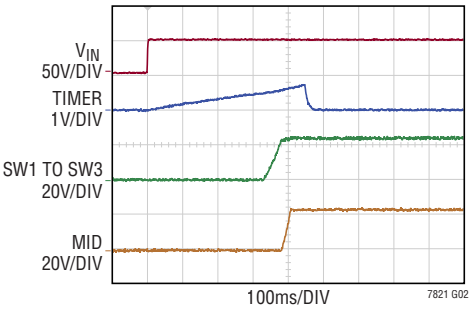
Efficiency and Power Loss In Different Modes vs Load Current



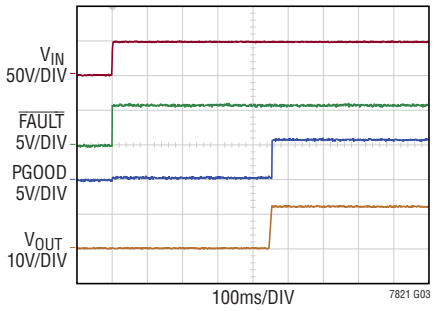
Efficiency at Various V_{IN} for V_{OUT} = 12V



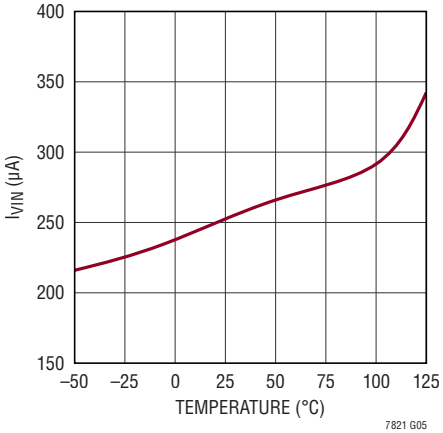
LTC7821 Start-Up Characteristic (Pre-Balancing Period)



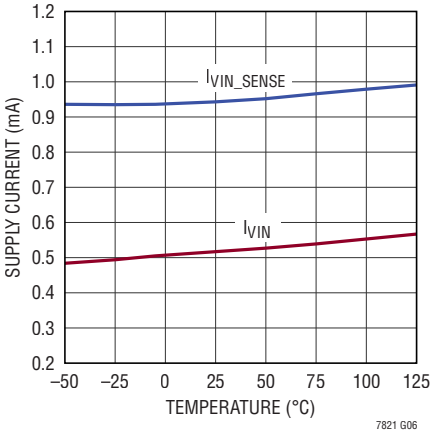
LTC7821 Start-Up Characteristic



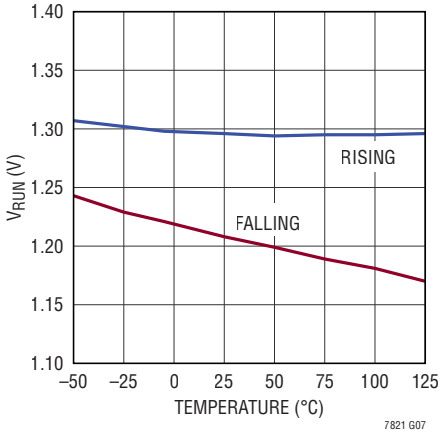
Shutdown Current vs Temperature



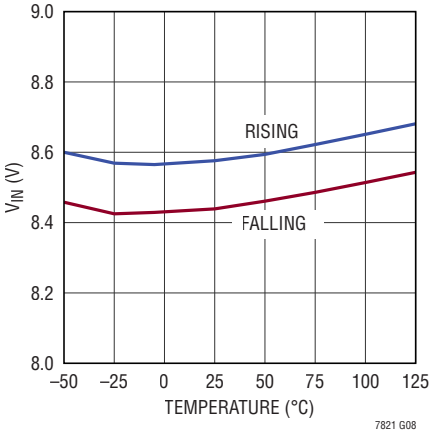
Quiescent Current vs Temperature



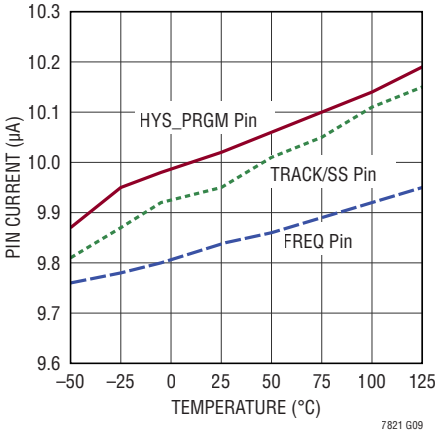
Shutdown (RUN) Threshold vs Temperature



Input Voltage UVLO Threshold vs Temperature



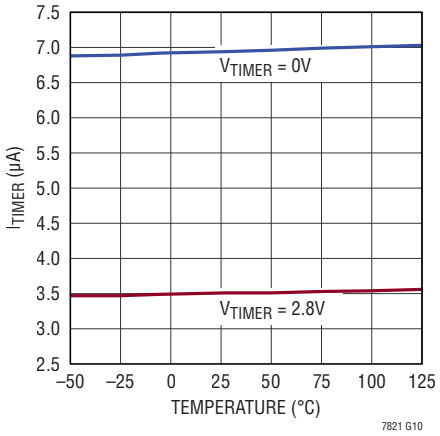
HYS_PRGM, TRACK/SS and FREQ Pin Current vs Temperature



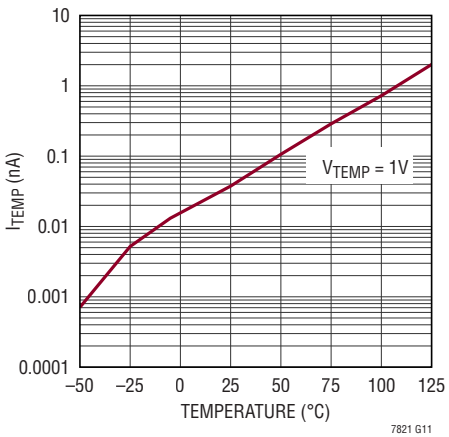
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TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

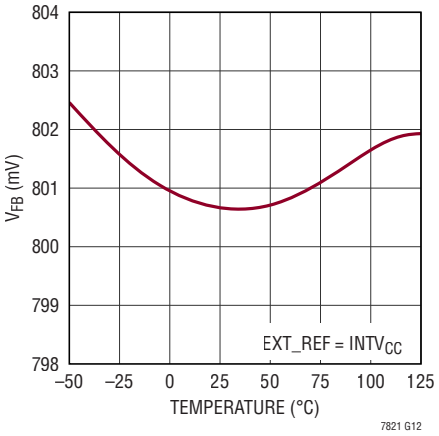
TIMER Pin Current vs Temperature



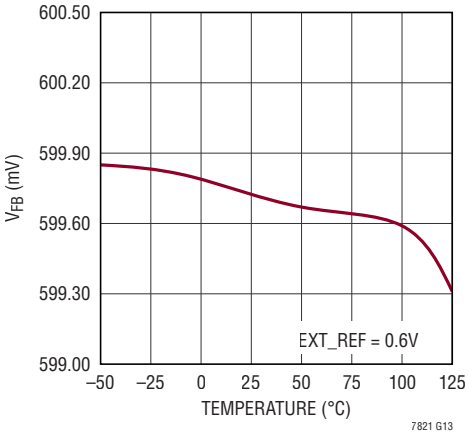
TEMP Pin Current vs Temperature



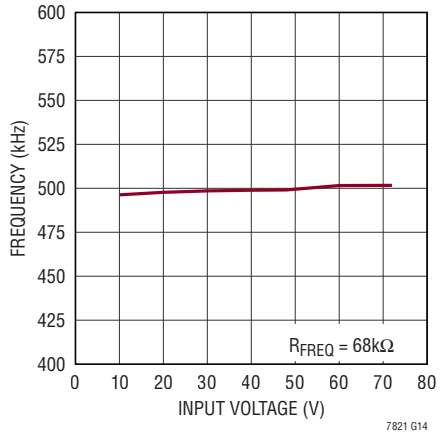
Regulated Feedback Voltage vs Temperature



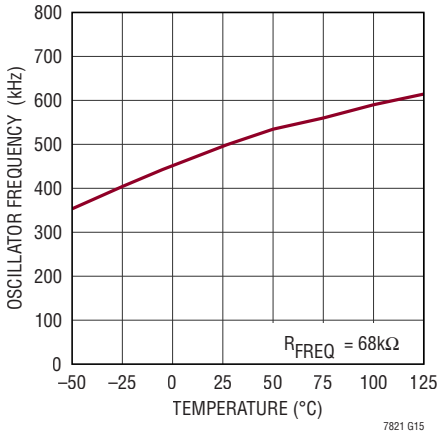
Regulated Feedback Voltage vs Temperature



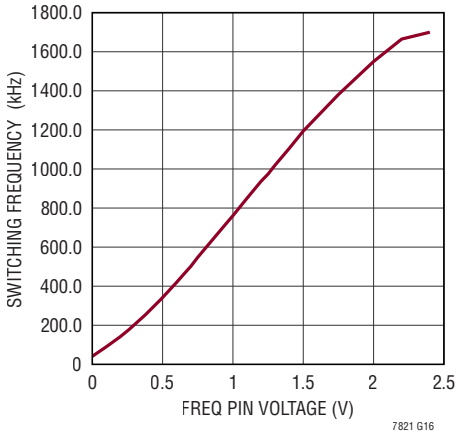
Oscillator Frequency vs Input Voltage



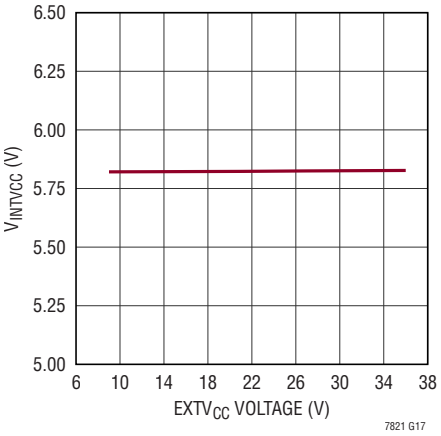
Oscillator Frequency vs Temperature



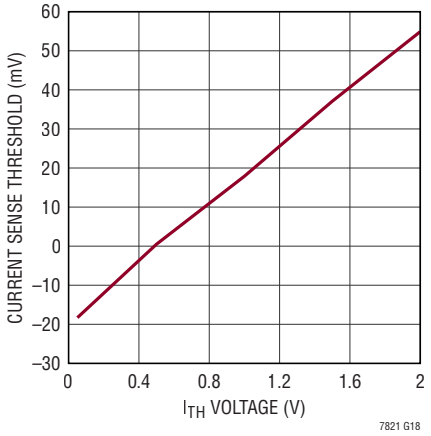
Switching Frequency vs Voltage at FREQ Pin



$INTV_{CC}$ Line Regulation (Supply from $EXTV_{CC}$)

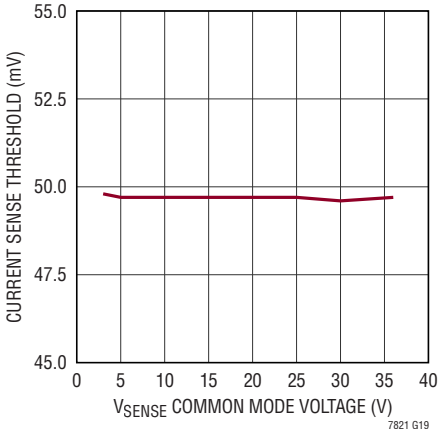


Current Sense Threshold vs I_{TH} Voltage

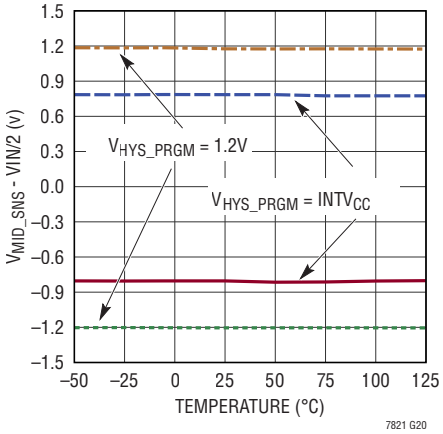


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

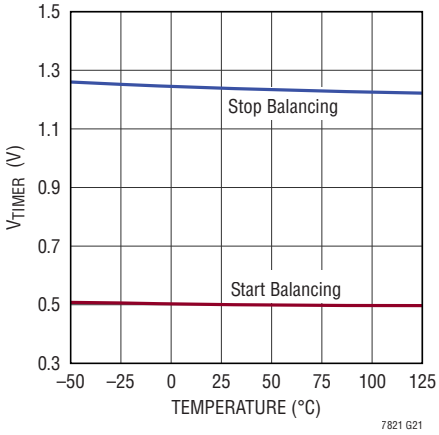
Maximum Current Sense Threshold vs Common Mode Voltage



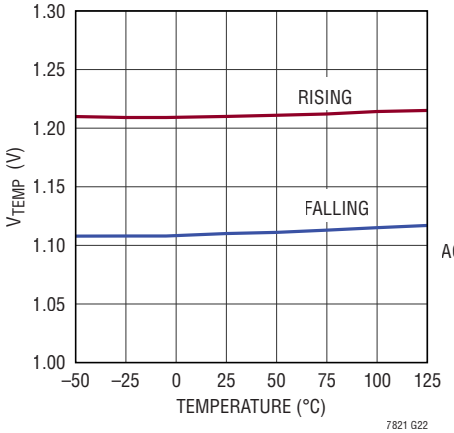
HYS_PRGM Voltage Window vs Temperature



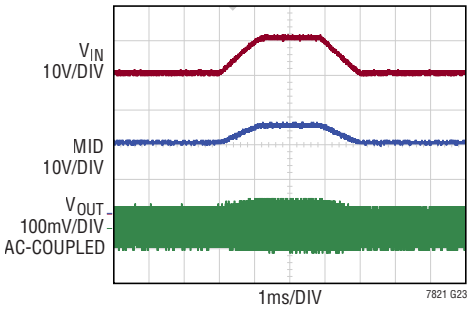
Voltage at Timer Pin to Start and Stop Capacitor Balancing vs Temperature



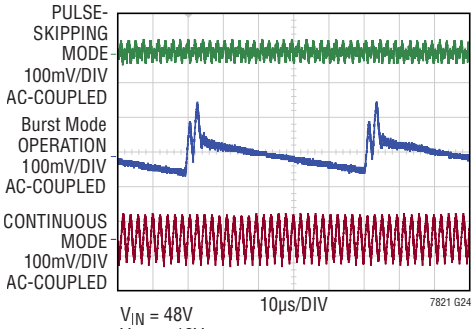
TEMP Pin Trip Voltage vs Temperature



Line Transient 10V/ms

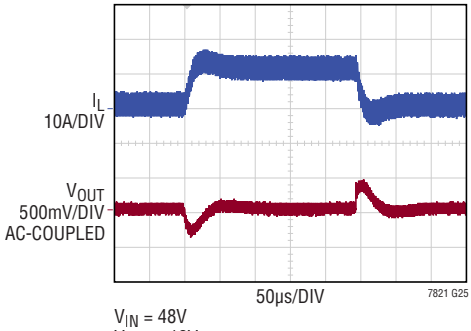


Steady-State Output Voltage Ripple of Typical Application



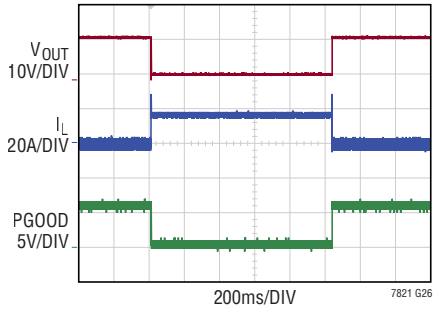
V_{IN} = 48V
V_{OUT} = 12V
I_{LOAD} = 30mA

Load Transient 2A–12A–2A of Typical Application

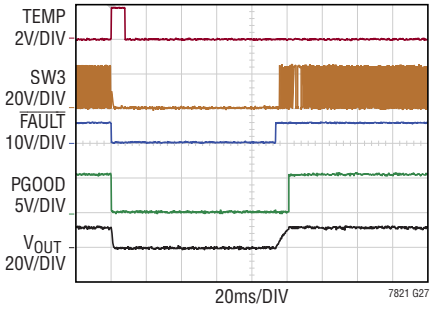


V_{IN} = 48V
V_{OUT} = 12V
f_{SW} = 500kHz

Short-Circuit and Recovery



TEMP Fault Characteristic



PIN FUNCTIONS

MODE/PLLIN (Pin 1): Mode Selection or External Synchronization Input to Phase Detector. When external synchronization is not used, this pin selects the operating modes and can be tied to SGND, to $INTV_{CC}$ or left floating. If the pin is connected to SGND, it enables forced continuous mode while a connection to $INTV_{CC}$ enables pulse-skipping mode. Floating the pin enables Burst Mode operation.

For external sync, apply a clock signal to this pin. The integrated PLL along with its internal compensation network will synchronize the internal oscillator to this clock. Forced continuous mode will be enabled.

CLKOUT (Pin 2): Clock Output Pin. This pin outputs a clock 180° out of phase with the main operating clock of the LTC7821.

RUN (Pin 3): Run Control Input. A voltage above 1.3V turns the controller ON. There is a 1µA pull-up current on this pin when its voltage is below 1.3V.

$\overline{\text{FAULT}}$ (Pin 4): Open Drain Output pin. When the signal goes low, it indicates one of the following conditions:

(a) In the capacitor balancing phase, capacitors C_{FLY} or C_{MID} (see Typical Application) are not charged to $V_{IN}/2$. A low $\overline{\text{FAULT}}$ indicates an abnormal condition that is preventing C_{FLY} or C_{MID} from being be charged up to $V_{IN}/2$.

(b) During normal operation, the voltage deviates from $V_{IN}/2$ by a window amount set by the voltage on the HYS_PRGM pin.

(c) The die temperature exceeds its internally set limit or the PTC resistor connected as the lower leg of a resistor divider trips the TEMP pin threshold.

During any of these condition, the TRACK/SS pin will also be pulled low.

PGOOD (Pin 5): Power Good Pin. This is an open drain output. PGOOD is pulled to ground when the voltage of the V_{FB} pin is not within ±7.5% of its set point after an internal 50µs mask timer expires. It will also be pulled low when $\overline{\text{FAULT}}$ is tripped.

TIMER (Pin 6): Charge Balancing Timer Input. A capacitor connected from this pin to ground sets the amount of time allocated to charge C_{FLY} and C_{MID} to $V_{IN}/2$ during the capacitor balancing phase. It also sets the auto-retry timeout, should the capacitors fail to reach this voltage within the set time. Capacitors C_{FLY} and C_{MID} begin and end charging when the TIMER voltage is between 0.5V and 1.2V, respectively. If the capacitor is balanced before the TIMER voltage reaches 1.2V, this voltage is reset to ground and normal operation begins. However, if the balance is not reached when the voltage reaches 1.2V, then the charging of the capacitors stops and the auto-retry timeout period begins. The TIMER capacitor will now slew at half the rate until it reaches 4V and then resets to zero and begins to slew at 1x rate. Once it reaches 0.5V, the C_{FLY} and C_{MID} begin to charge again and the process repeats.

TRACK/SS (Pin 7): Output Voltage Tracking and Soft-Start Input. The LTC7821 regulates the V_{FB} voltage to the lowest of three voltages: 0.8V, the voltage on the EXT_REF pin or the voltage on the TRACK/SS pin. An internal 10µA pull-up current source is connected to this pin. A capacitor to ground at this pin sets the ramp time to the final regulated output voltage. Alternatively, a resistor divider from another voltage supply connected to this pin allows the LTC7821 output voltage to track the other supply during start-up.

EXT_REF (Pin 8): External Reference Input. A voltage applied to this pin forces the V_{FB} to regulate to this voltage. Internal clamps set at 0.4V and 0.93V limit the lower and upper bounds of V_{FB} regulation. Connecting this pin to $INTV_{CC}$ will cause the internal reference to be used for output voltage regulation.

HYS_PRGM (Pin 9): There is a 10µA current flowing out of this pin. A voltage created by connecting a resistor from this pin to ground sets an equal amount of window threshold around $V_{IN}/2$ to a window comparator. When the voltage at MID_{SENSE} is not within this window threshold, $\overline{\text{FAULT}}$ will be pulled low and switching will stop. C_{FLY} and C_{MID} will be rebalanced to half of V_{IN} before resuming normal operation.

I_{TH} (Pin 10): Current Control Threshold and Error Amplifier Compensation Point. The current comparator threshold increases with its I_{TH} control voltage.

FREQ (Pin 11): Frequency Set Pin. There is a 10µA current flowing out of this pin. A resistor to ground sets a voltage which in turn programs the frequency.

PIN FUNCTIONS

TEMP (Pin 12): Temperature Sensing Input. Using a PTC resistor as the lower leg of a resistor divider, connect the TEMP pin to the common point of the divider. The PTC resistor is used to monitor a hot spot on the PCB. Once it reaches the TEMP threshold of 1.22V, the LTC7821 stops switching for 100ms before retrying. Ground this pin if not used.

V_{FB} (Pin 13): Error Amplifier Feedback Input. This pin receives the remotely sensed feedback voltage from an external resistive divider across the output.

I_{SNS}– (Pin 14): Current Sense Comparator Input. The (–) input to the current comparator is Kelvin connected to the output voltage of the controller.

I_{SNS}+ (Pin 15): Current Sense Comparator Input. The (+) input to the current comparator is normally Kelvin connected to the DCR sensing networks or current sensing resistor.

$EXTV_{CC}$ (Pin 16): External Power Input to an Internal LDO Connected to $INTV_{CC}$. This LDO supplies $INTV_{CC}$ power, bypassing the internal LDO powered from V_{IN} whenever $EXTV_{CC}$ is higher than 6.4V. Do not float or exceed 40V on this pin.

PGND (Pin 17): Driver Power Ground. Connect this pin closely to the source of bottom (synchronous) N-channel MOSFET M4, the (–) terminal of C_{IN} and the (–) terminal of C_{VCC}.

BG2 (Pin 18): Gate Drive for the Bottom (synchronous) N-Channel MOSFET. The voltage swings from slightly below ground to $INTV_{CC}$.

$INTV_{CC}$ (Pin 19): Internal Regulator Output. The bottom synchronous gate driver and control circuits are powered from this regulator. Bypass this pin to PGND with a minimum of 4.7µF low ESR tantalum or ceramic capacitor. Do not use the $INTV_{CC}$ pin for any purpose other than described in this data sheet.

SW3 (Pin 20): Switch Node Connection to Inductor and One Terminal of Flying Capacitor. Voltage swing at this pin is from slightly below ground to $V_{IN}/2$.

TG2 (Pin 21): Floating Gate Drive for Second Lowermost N-Channel MOSFET. The voltage swings equal to $INTV_{CC}$ superimposed on the switch node voltage SW3.

BOOST1, BOOST2, BOOST3 (Pin 31, 23, 22): Bootstrapped Supplies to Floating Drivers. Capacitors are connected between the BOOSTx and SWx (MID) pin. Voltage swing at the BOOST1 pin is from ($V_{IN}/2$ + $INTV_{CC}$) to (V_{IN} + $INTV_{CC}$). Voltage at the BOOST2 pin is at ($V_{IN}/2$ + $INTV_{CC}$). Voltage swing at the BOOST3 pin is from $INTV_{CC}$ to ($V_{IN}/2$ + $INTV_{CC}$).

BG1 (Pin 24): Floating Gate Drive for Second Uppermost N-Channel MOSFET. The voltage swings between ($V_{IN}/2$ + $INTV_{CC}$) and $V_{IN}/2$.

MID (Pin 25): Half Supply from V_{IN}. Do not use this to source current. Connect a bypass capacitor from this node to PGND.

MID_{SENSE} (Pin 26): Half Supply Monitor. Provides Kelvin sensing input for the comparator that monitors the voltage between MID_{SENSE} and ground. An RC filter can be added from MID to this pin to filter out noise.

V_{IN_SENSE} (Pin 27): V_{IN} Kelvin Sensing Input. Allows an internal $V_{IN}/2$ to be generated for LTC7821 control circuit usage. For a cleaner supply, an RC filter can be added from V_{IN} to this pin.

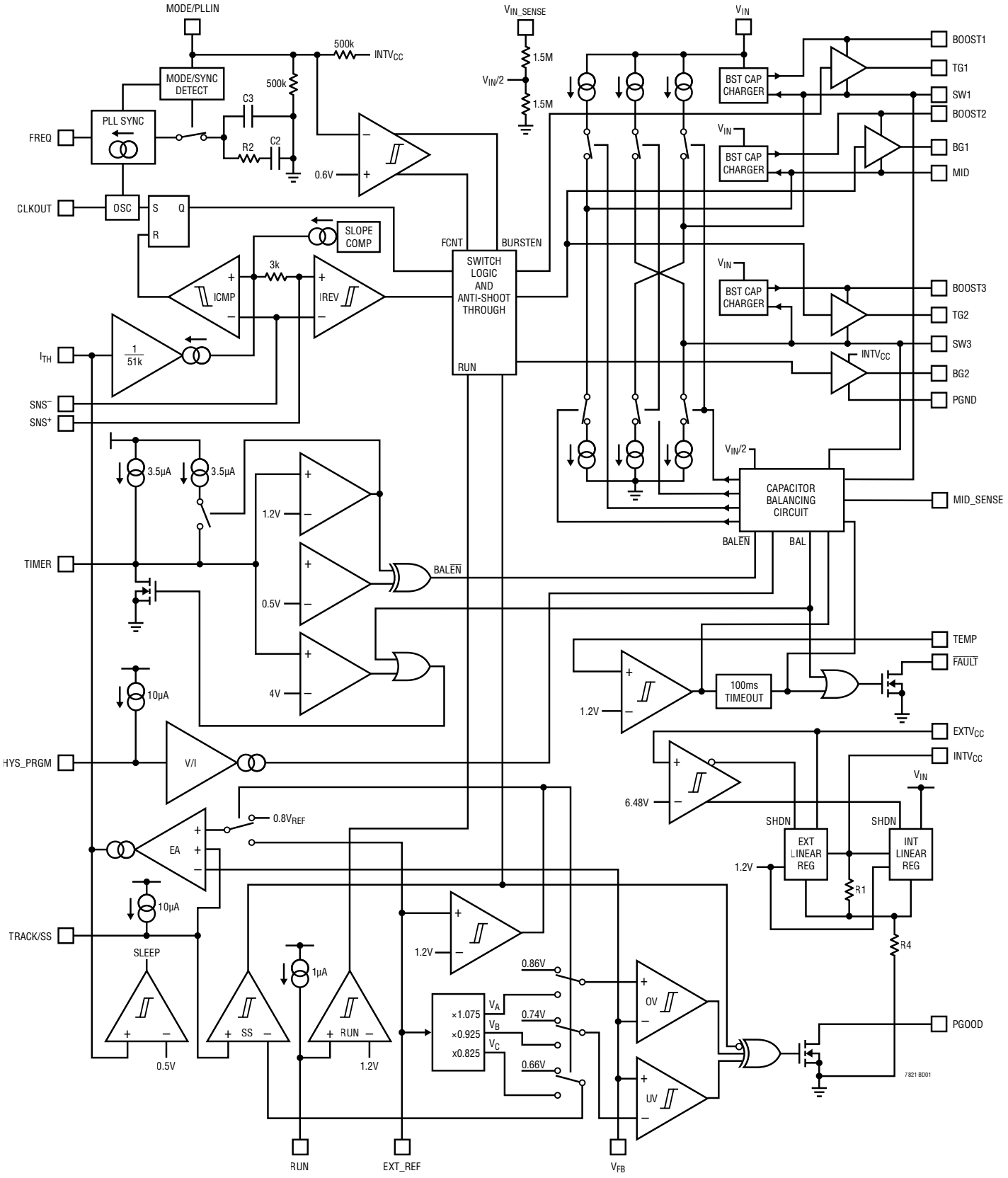
V_{IN} (Pin 28): Main Input Supply. Bypass this pin to PGND with a capacitor.

SW1 (Pin 29): Switch Node Connection to One Terminal of Flying Capacitor. Voltage swing at this pin is from $V_{IN}/2$ voltage to V_{IN}.

TG1 (Pin 30): Floating Gate Drive for Uppermost N-Channel MOSFET. The voltage swings equal to $INTV_{CC}$ superimposed on the switch node voltage SW1.

SGND (Exposed Pad, Pin 33): Signal Ground. All Small-signal components and compensation components should connect to this ground, which in turn connects to PGND at one point. Exposed pad must be soldered to the PCB, providing a local ground for the control components of the IC, and be tied to the PGND pin under the IC.

BLOCK DIAGRAM



OPERATION

Capacitor Balancing Phase

During initial power up, the voltage across the flying capacitor (C_{FLY}) and C_{MID} are measured. If either of these voltages are not at $V_{IN}/2$, the TIMER's capacitor will be allowed to charge up. When the TIMER capacitor's voltage reaches 0.5V, internal current sources to bring C_{FLY} voltage to $V_{IN}/2$ are turned ON. After the C_{FLY} voltage has reached $V_{IN}/2$, C_{MID} will then be charged to $V_{IN}/2$. The TRACK/SS pin is pulled low during this duration and all external MOSFETs are shut off. The $\overline{FAULT}$ pin will not be pulled low during this initial power up. If the voltages across C_{FLY} and C_{MID} reach $V_{IN}/2$ before the TIMER capacitor's voltage reaches 1.2V, the TRACK/SS will be released and allowed to charge up. The TIMER pin will reset to ground and remain there. Normal operation will begin (see Figure 1A).

If, however, the C_{FLY} or C_{MID} voltage is not at $V_{IN}/2$ when V_{TIMER} reaches 1.2V, the internal current sources will be turned OFF and the TIMER capacitor will be charged at half the initial rate until it reaches 4V. Timer will then be reset to zero, and the LTC7821 will repeat the above process again until C_{FLY} and C_{MID} are at $V_{IN}/2$(See Figure 1B).

During normal operation, only C_{MID} is monitored for deviation away from $V_{IN}/2$ by a window amount set by a resistor connected from HYS_PRGM to ground. The voltage across this resistor sets the same amount of window threshold above and below $V_{IN}/2$. If V_{CMID} leaves this voltage window, all switching will stop and the TRACK/SS pin will be pulled low. Corresponding internal current sources will be turned on to bring C_{FLY} and C_{MID} voltages back to $V_{IN}/2$. $\overline{FAULT}$ will be pulled low and released once the balancing is complete. During this balancing period, PGOOD will also be pulled low. The TRACK/SS pin is also allowed to charge up upon the completion of balancing. Connecting HYS_PRGM to $INTV_{CC}$ sets the window threshold to ±0.8V around $V_{IN}/2$. (see Figure 2)

Main Control Loop

Once the capacitor balancing phase is completed, normal operation begins. MOSFETs M1 and M3 are turned ON when the clock sets the RS latch, and turned off when the main current comparator, I_{CMP}, resets the RS latch. MOSFETs M2 and M4 are then turned on. The peak inductor

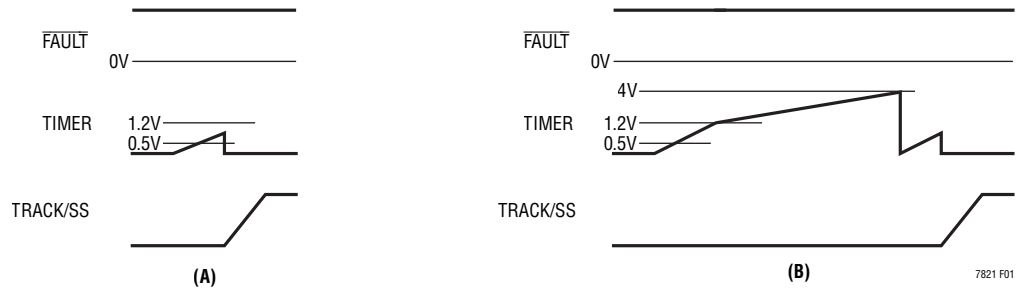


Figure 1. Charge Balancing During Power Up with (A) Balancing Completed within One Timer Period and (B) More Than One Timer Period

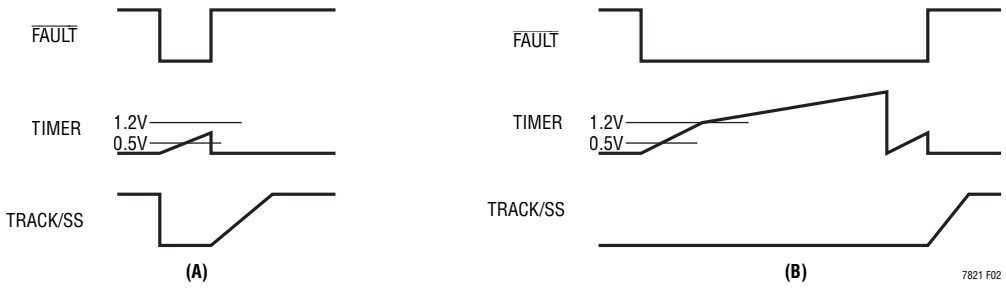


Figure 2. Charge Balancing During Normal Operation with (A) Balancing Completed within One Timer Period and (B) More Than One Timer Period

OPERATION

current at which I_{CMP} resets the RS latch is controlled by the voltage on the I_{TH} pin, which is the output of the error amplifier EA. The V_{FB} pin receives the voltage feedback signal, which is compared to the internal reference voltage by the EA. When the load current increases, it causes a slight decrease in V_{FB} relative to the 0.8V reference, which in turn causes the I_{TH} voltage to increase until the average inductor current matches the new load current. After MOSFETs M1 and M3 have turned OFF, MOSFETs M2 and M4 are turned ON until either the inductor current starts to reverse, as indicated by the reverse current comparator I_{REV}, or the beginning of the next cycle.

During the switching of M1/M3 and M2/M4, capacitor C_{FLY} is alternately connected in series with or parallel to C_{MID}. The voltage at MID will be approximately at $V_{IN}/2$.

$INTV_{CC}/EXTV_{CC}$ Power

Power for the bootstrap drivers and bottom MOSFET and most internal circuitry is derived from the $INTV_{CC}$ pin. When the $EXTV_{CC}$ pin is grounded or tied to a voltage less than 7V, an internal 5.8V linear regulator supplies $INTV_{CC}$ power from V_{IN}. If $EXTV_{CC}$ is taken above 7V, this linear regulator is turned OFF and another 5.8V linear regulator turns ON to provide the $INTV_{CC}$ power from $EXTV_{CC}$. Using the $EXTV_{CC}$ pin allows the $INTV_{CC}$ power to be derived from a high efficiency external source, resulting in an overall increase in system efficiency.

Bootstrap Capacitor Refresh

Each of the three uppermost MOSFET drivers is biased from its respective floating bootstrap capacitor, CB1 to CB3, which are refreshed during switching through a charge pump configuration consisting of diodes D1 to D3 and the external MOSFETs.

During the charge balancing phase or light load condition when switching may stop for extended amount of time, the voltage across the bootstrap capacitor may decrease sufficiently that the gate drive voltage is not optimal. Undervoltage detectors monitor the voltage across each of the bootstrap capacitors. When any of them goes below 3V, an internal current source of 1mA will be turned ON to charge that bootstrap capacitor through the upper plate of the capacitor. A 1mA sinking source that is connected to the bottom plate of the bootstrap capacitor will also be turned ON to sink away this current. This ensures a net zero residual current at the bottom plate capacitor node, hence avoiding any impact on the bias condition of that node. When CB1 and CB2/CB3 reach 4.3V and 4.47V respectively, the refreshing stops. When CB2 and CB3 need to be refreshed, all switching stops.

Shutdown and Start-Up (RUN and TRACK/SS Pins)

When the RUN pin is below 1.3V, the $INTV_{CC}$ linear regulator along with all the internal circuitry that is powered from this supply, is disabled. The main control loop will also be disabled. Releasing the RUN pin will allow the internal 1µA current source to pull this pin up, thus enabling the part. The RUN pin can also be driven directly by logic but ensure that this voltage does not exceed the Absolute Maximum Rating of 6V.

The slew rate of the output voltage V_{OUT} can be controlled by the voltage on the TRACK/SS pin. When the voltage on the TRACK/SS is less than the internal reference of 0.8V (or EXT_REF if this feature is invoked), the LTC7821 regulates the V_{FB} voltage to the TRACK/SS voltage instead of to the reference. This allows the TRACK/SS pin to be used to program the soft-start period by connecting an external capacitor from the TRACK/SS pin to SGND. An internal 10µA pull-up current charges this capacitor, creating a voltage ramp on the TRACK/SS pin. As the TRACK/SS voltage rises linearly from 0V to the reference voltage (and beyond), the output voltage V_{OUT} rises smoothly from zero to the final value. Alternatively, the TRACK/SS pin can be used to cause the start-up of V_{OUT} to track that of another supply. Typically this requires connecting to the TRACK/SS pin an external resistor divider from the other supply to ground (see Application Information section).

Light Load Current Operation (Burst Mode Operation, Pulse-Skipping Mode, or Continuous Conduction)

The LTC7821 can be enabled to enter high efficiency Burst Mode operation, constant-frequency pulse-skipping mode, or forced continuous conduction mode. To select forced continuous operation, tie the MODE/PLLIN pin to a DC voltage below 0.6V (e.g., SGND). To select pulse-skipping mode of operation, tie the MODE/PLLIN pin to $INTV_{CC}$. To select Burst Mode operation, float the MODE/PLLIN pin.

OPERATION

When the controller is enabled for Burst Mode operation, the peak current in the inductor is set to approximately one-third of the maximum sense voltage even though the voltage on the I_{TH} pin indicates a lower value. If the average inductor current is higher than the load current, the error amplifier output, EA, will decrease the voltage on the I_{TH} pin. When the I_{TH} voltage drops below 0.5V, the internal sleep signal goes high (enabling sleep mode) and all external MOSFETs are turned off. In sleep mode, the load current is supplied by the output capacitor. As the output voltage decreases, the EA's output begins to rise. When the output voltage drops enough, the sleep signal goes low, and the controller resumes normal operation by turning on the external MOSFETs on the next cycle of the internal oscillator. When a controller is enabled for Burst Mode operation, the inductor current is not allowed to reverse. The reverse current comparator (IREV) turns off the bottom external MOSFET M4 and M2 just before the inductor current reaches zero, preventing it from reversing and going negative. Thus, the controller operates in discontinuous operation.

In forced continuous operation, the inductor current is allowed to reverse at light loads or under large transient conditions. The peak inductor current is determined by the voltage on the I_{TH} pin. In this mode, the efficiency at light loads is lower than in Burst Mode operation. However, continuous mode has the advantages of lower output ripple and less interference with audio circuitry.

When the MODE/PLLIN pin is connected to $INTV_{CC}$, the LTC7821 operates in PWM pulse-skipping mode at light loads. At very light loads, the current comparator I_{CMP} may remain tripped for several cycles and force the external MOSFETs M1 and M3 to stay off for the same number of cycles (i.e., skipping pulses). The inductor current is not allowed to reverse (discontinuous operation). This mode, like forced continuous operation, exhibits low output ripple as well as low audio noise and reduced RF interference as compared to Burst Mode operation. It provides higher low current efficiency than forced continuous mode, but not nearly as high as Burst Mode operation.

Frequency Selection and Phase-Locked Loop (FREQ and MODE/PLLIN Pins)

The selection of switching frequency is a trade-off between efficiency and component size. Low frequency operation increases efficiency by reducing MOSFET switching losses, but requires larger inductance and/or output capacitance to maintain low output ripple voltage. In addition, it will also require larger BOOST capacitance and balancing capacitance (C_{FLY} and C_{MID}) since the refresh rate is lower. The switching frequency of the LTC7821's controller can be selected using the FREQ pin. If the MODE/PLLIN pin is not being driven by an external clock source, the FREQ pin can be used to program the controller's operating frequency from 50kHz to 1.7MHz.

There is a 10µA current flowing out of the FREQ pin, so the user can program the controller's switching frequency with a single resistor to SGND.

A phase-locked loop (PLL) is integrated on the LTC7821 to synchronize the internal oscillator to an external clock source that is connected to the MODE/PLLIN pin. The controller operates in forced continuous mode when it is synchronized. The PLL loop filter network is integrated inside the LTC7821. The phase-locked loop is capable of locking any frequency within the range of 200kHz to 1.5MHz. The frequency setting resistor should always be present to set the controller's initial switching frequency before locking to the external clock.

Temperature Monitoring

When the LTC7821 die temperature reaches 150°C, switching stops and TRACK/SS pin is pulled low. Charge balancing is also disabled.

The LTC7821 can provide hotspot monitoring via the TEMP pin. By using a PTC thermistor as the lower leg of a resistor divider and connecting the common point of this divider to the TEMP pin, the voltage increases drastically when the temperature reaches beyond the Curie point of the PTC thermistor as shown in Figure 3. The characteristic of the PTC thermistor is shown in Figure 4. When the TEMP pin reaches 1.22V, all switching stops for 100ms.

OPERATION

The voltage on the TRACK/SS pin and $\overline{FAULT}$ is pulled low and is released after 100ms (Figure 5) if the voltage on the TEMP pin goes below 1.1V during this 100ms timeout. If the TEMP pin voltage remains above 1.1V, the timeout period will be extended until the voltage drops below 1.1V.

The temperature that is use to trigger the hotspot protection will determine the thermistor selection. This temperature will be the Curie point of the thermistor, which is often defined as having two times its resistance at 25°C. With the Curie point resistance of the thermistor known, $R2_{CURIE}$, the upper resistance, R1, can be selected by the following equation:

$$R1 = \frac{R2_{CURIE}\,(V_{EXT} - 1.22)}{1.22}$$

Power Good (PGOOD Pin)

When V_{FB} pin voltage is not within ±10% of the internal 0.8V reference or the reference set by EXT_REF, the PGOOD pin is pulled low. The PGOOD pin is also pulled low when the RUN pin is below 1.3V or when the LTC7821 is in the soft-start or tracking phase. The PGOOD pin will flag power good immediately when the V_{FB} pin is within the ±10% of the reference window. However, there is an internal 50µs power bad mask when V_{FB} goes out the ±10% window. The PGOOD pin is allowed to be pulled up by an external resistor to sources of up to 80V.

FAULT ($\overline{FAULT}$ Pin)

During initial power up of the LTC7821 or when enabling the part via the RUN pin, the $\overline{FAULT}$ pin will not be pulled low even when C_{FLY} and/or C_{MID} needed to be rebalanced to $V_{IN}/2$. But during normal operation, when rebalancing is needed, the $\overline{FAULT}$ will be pulled low. Another condition that causes the $\overline{FAULT}$ to go low is thermal shutdown, either caused by the internal die temperature reaching 150°C or the voltage at TEMP pin reaching 1.22V. The $\overline{FAULT}$ pin is allowed to be pulled up by an external resistor to sources of up to 80V.

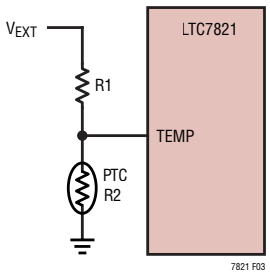


Figure 3. Temperature Monitoring Setup

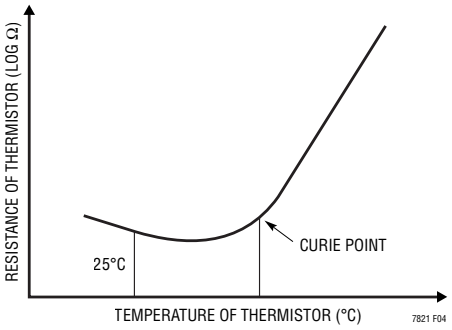


Figure 4. Characteristic of a Thermistor

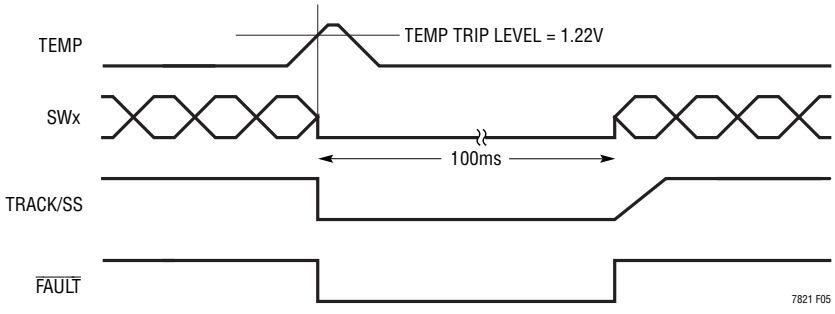


Figure 5. Temperature Trip Characteristic

APPLICATIONS INFORMATION

The "Typical Application" on the first page is a basic LTC7821 application circuit. The LTC7821 can be configured to use either DCR (inductor resistance) sensing or resistor sensing. The choice between the two current sensing schemes is largely a design trade-off between cost, power consumption, and accuracy. DCR sensing is popular because it saves an expensive current sensing resistor and is more power efficient, especially in high current applications. However, a current sensing resistor provides the most accurate current limit for the application. Other external component selection is driven by the load requirement, and begins with the selection of R_{SENSE} (if R_{SENSE} is used). Next C_{FLY}, C_{MID}, and the power MOSFETs are selected, followed by the input and output capacitors. In addition to the power level, switching frequency plays a role in selecting the balancing capacitance (C_{FLY} and C_{MID}) and the inductance of the inductor.

ISNS+ and ISNS– Pins

The ISNS+ and ISNS– pins are the inputs to the current comparators. The common mode input voltage range of the current comparators is 0V to 36V. Both ISNS pins are high impedance inputs with small leakage currents of less than 1.2µA. When the ISNS pins ramp up from 0V to 2.4V, small base currents flow out of the ISNS pins. When the ISNS pins ramp down from 36V to 2V, the small base currents flow into the ISNS pins. The high impedance inputs to the current comparators allow accurate DCR sensing. However, care must be taken not to float these pins during normal operation.

Filter components mutual to the sense lines should be placed close to the LTC7821, and the sense lines should run close together to a Kelvin connection underneath the current sense element (shown in Figure 6). Sensing current elsewhere can effectively add parasitic inductance and capacitance to the current sense element, degrading the information at the sense terminals and making the programmed current limit unpredictable. If DCR sensing is used (Figure 7b), sense resistor R1 should be placed close to the switching node, to prevent noise from coupling into sensitive small-signal nodes. The capacitor C1 should be placed close to the IC pins.

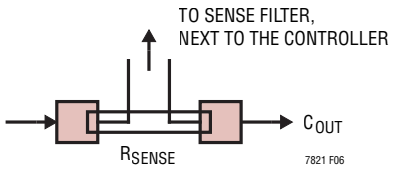


Figure 6. Sense Lines Placement with Sense Resistor

Resistor Current Sensing

The hybrid architecture of the LTC7821 generates a voltage rail of half the V_{IN} supply to the step-down control loop. Therefore the current ripple calculation and its operating duty cycle is referred to the voltage at the MID pin which is approximately at $V_{IN/2}$.

A typical sensing circuit using a discrete resistor is shown in Figure 7a. R_{SENSE} is chosen based on the required output current.

The current comparator has a maximum threshold of 50mV and its inputs have a common mode range of 0V to 36V. The current comparator threshold sets the peak of the inductor current, yielding a maximum average output current I_{MAX} equal to the peak value less half the peak-to-peak ripple current, ΔI_L. To calculate the sense resistor value, use the equation:

$$R_{SENSE} = \frac{50mV}{I_{(MAX)} + \frac{\Delta I_L}{2}}$$

Because of possible PCB noise in the current sensing loop, the AC current sensing ripple of $\Delta V_{SENSE} = \Delta I_L \bullet R_{SENSE}$ also needs to be verified in the design to get a good signal-to-noise ratio.

In general, for a reasonably good PCB layout, a 10mV ΔV_{SENSE} voltage is recommended as a conservative number to start with, either for R_{SENSE} or DCR sensing applications, for duty cycles less than 40%. For applications where the inductor's ripple current could be greater than 50% and operating at 750kHz and above, the sense resistor's parasitic inductance has to be taken into consideration since its contribution is no longer negligible.

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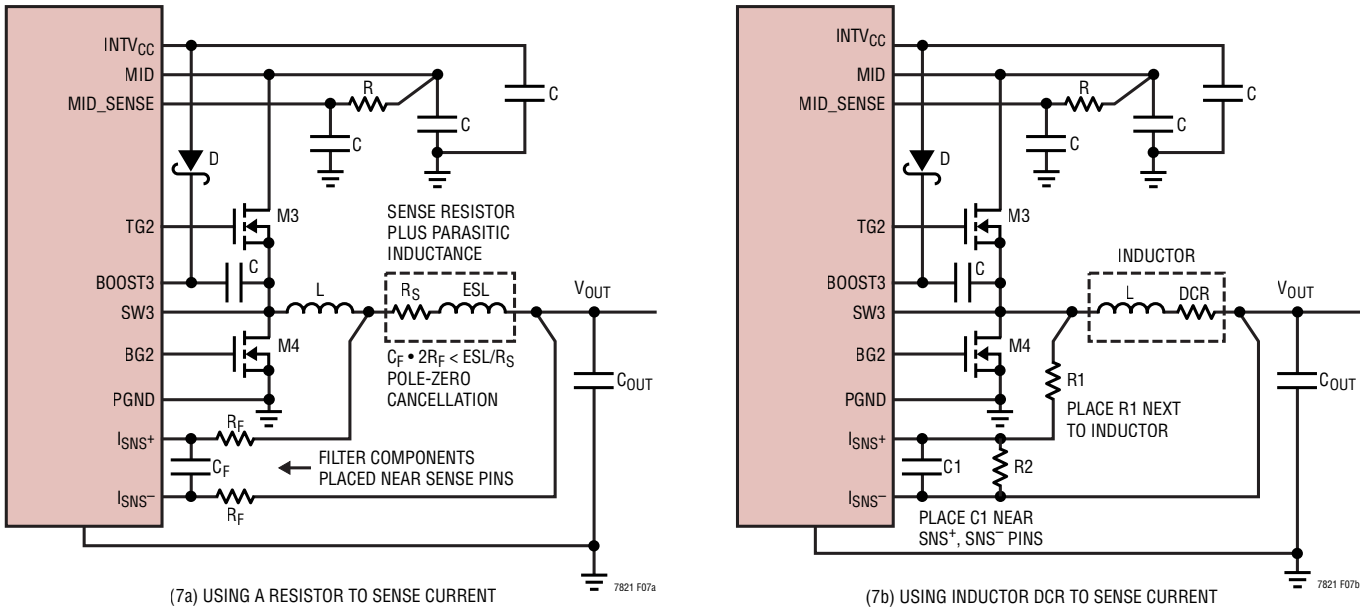


Figure 7. Two Different Methods of Sensing Current

In an application where the sense resistor's parasitic inductance contribution is negligible, a small RC filter placed near the IC is enough to reduce the effects of capacitive and inductive noise coupled in the sense traces on the PCB. A typical filter consists of two series 10Ω resistors connected to a parallel 1000pF capacitor, resulting in a time constant of 20ns. However, the same RC filter with minor modifications can be used to extract the resistive component of the current sense signal in the presence of significant parasitic inductance in the sense resistor. For example, Figure 8 illustrates the voltage waveform across a 1mΩ sense resistor with a 2010 footprint for the 12V/20A converter operating at 100% load. The waveform is the superposition of a purely resistive component and a purely inductive component. It was measured using two scope probes and waveform math to obtain a differential measurement. Based on additional measurements of the inductor ripple current and the on-time and off-time of the top switch, the value of the parasitic inductance was determined to be 0.3nH using the equation:

$$ESL = \frac{V_{ESL(STEP)}}{\Delta I_L} \bullet \left(\frac{t_{ON} \bullet t_{OFF}}{t_{ON} + t_{OFF}} \right)$$

If the RC time constant is chosen to be close to the parasitic inductance divided by the sense resistor (L/R), the resulting waveform looks resistive again, as shown in Figure 9.

Check the sense resistor manufacturer's data sheet for information about parasitic inductance. In the absence of data, measure the voltage drop directly across the sense resistor to extract the magnitude of the ESL step and use

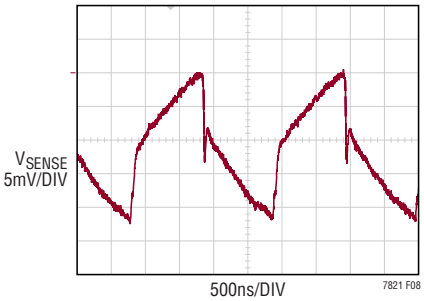


Figure 8. Voltage Waveform Measured Directly Across the Sense Resistor

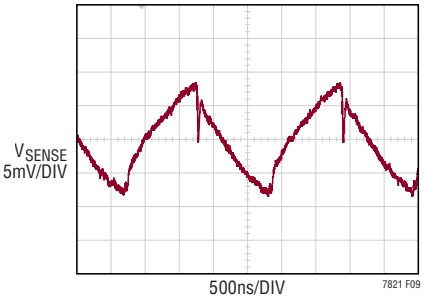


Figure 9. Voltage Waveform Measured After the Sense Resistor Filter, C_F = 1nF, R_F = 100Ω

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the equation to determine the ESL. However, do not over filter. Keep the RC time constant less than or equal to the inductor time constant to maintain a high enough ripple voltage on V_{RSENSE}. The filter components need to be placed close to the IC. The positive and negative sense traces need to be routed as a differential pair and Kelvin connected to the sense resistor.

Inductor DCR Sensing

For applications requiring the highest possible efficiency at high load currents, the LTC7821 is capable of sensing the voltage drop across the inductor DCR, as shown in Figure 7b. The DCR of the inductor represents the small amount of DC winding resistance of the copper, which can be less than 1mΩ for today's low value, high current inductors. In a high current application requiring such an inductor, conduction loss through a sense resistor would cost several points of efficiency compared to DCR sensing.

If the external R1|| R2 • C1 time constant is chosen to be exactly equal to the L/DCR time constant, the voltage drop across the external capacitor is equal to the drop across the inductor DCR multiplied by R2/(R1 + R2). R2 scales the voltage across the sense terminals for applications where the DCR is greater than the target sense resistor value. To properly dimension the external filter components, the DCR of the inductor must be known. It can be measured using a good RLC meter, but the DCR tolerance is not always the same and varies with temperature; consult the manufacturers' data sheets for detailed information.

Using the inductor ripple current value from the Inductor Value Calculation section, the target sense resistor value is:

$$R_{SENSE(EQUIV)} = \frac{50mV}{I_{(MAX)} + \frac{\Delta I_L}{2}}$$

To ensure that the application will deliver full load current over the full operating temperature range, choose the minimum value for the Maximum Current Sense Threshold ($V_{SENSE(MAX)}$) in the Electrical Characteristics table.

Next, determine the DCR of the inductor. Where provided, use the manufacturer's maximum value, usually given at 20°C. Increase this value to account for the temperature coefficient of resistance, which is approximately 0.4%/°C. A conservative value for $T_{L(MAX)}$ is 100°C. To scale the maximum inductor DCR to the desired sense resistor value, use the divider ratio:

$$R_D = \frac{R_{SENSE(EQUIV)}}{DCR(MAX)\ AT\ T_{L(MAX)}}$$

C1 is usually selected to be in the range of 0.047µF to 0.47µF. This forces R1|| R2 to around 2kΩ, reducing error that might have been caused by the SENSE pins' 1.2µA current. $T_{L(MAX)}$ is the maximum inductor temperature.

The equivalent resistance R1||R2 is scaled to the room temperature inductance and maximum DCR:

$$R1||R2 = \frac{L}{(DCR\ AT\ 20°C) \bullet C1}$$

The sense resistor values are:

$$R1 = \frac{R1||R2}{R_D};\quad R2 = \frac{R1 \bullet R_D}{1 - R_D}$$

The maximum power loss in R1 is related to duty cycle, and will occur in continuous mode at the maximum input voltage:

$$P_{LOSS_R1} = \frac{(V_{MID} - V_{OUT}) \bullet V_{OUT}}{R1}$$

where V_{MID} is half the voltage of V_{IN}.

Ensure that R1 has a power rating higher than this value. If high efficiency is necessary at light loads, consider this power loss when deciding whether to use DCR sensing or sense resistors. Light load power loss can be modestly higher with a DCR network than with a sense resistor, due to the extra switching losses incurred through R1. However, DCR sensing eliminates a sense resistor, reduces conduction losses and provides higher efficiency at heavy loads. Peak efficiency is about the same with either method.

To maintain a good signal to noise ratio for the current sense signal, use a minimum ΔV_{SENSE} of 10mV for duty

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cycles less than 40%. For a DCR sensing application, the actual ripple voltage will be determined by the equation:

$$\Delta V_{SENSE} = \frac{V_{MID} - V_{OUT}}{R1 \bullet C1} \bullet \frac{V_{OUT}}{V_{MID} \bullet f_{OSC}}$$

Slope Compensation and Inductor Peak Current

Slope compensation provides stability in constant frequency architectures by preventing subharmonic oscillations at high duty cycles. It is accomplished internally by adding a compensating ramp to the inductor current signal at duty cycles in excess of 40%. Normally, this results in a reduction of maximum inductor peak current for duty cycles >40%. However, the LTC7821 uses a scheme that counteracts this compensating ramp, which allows the maximum inductor peak current to remain unaffected throughout all duty cycles.

Inductor Value Calculation

Given the desired input and output voltages, the inductor value and operating frequency f_{OSC} directly determine the inductor's peak-to-peak ripple current:

$$I_{RIPPLE} = \frac{V_{OUT}}{V_{MID}} \bullet \frac{V_{MID} - V_{OUT}}{f_{OSC} \bullet L}$$

Lower ripple current reduces core losses in the inductor, ESR losses in the output capacitors, and output voltage ripple. Thus, highest efficiency operation is obtained at low frequency with a small ripple current. Achieving this, however, requires a large inductor.

A reasonable starting point is to choose a ripple current that is about 40% of $I_{OUT(MAX)}$ for a duty cycle less than 40%. Note that the largest ripple current occurs at the highest input voltage. To guarantee that ripple current does not exceed a specified maximum, the inductor should be chosen according to:

$$L \geq \frac{V_{MID} - V_{OUT}}{f_{OSC} \bullet I_{RIPPLE}} \bullet \frac{V_{OUT}}{V_{MID}}$$

For duty cycles greater than 40%, the 10mV current sense ripple voltage requirement is relaxed because the slope compensation signal aids the signal-to-noise ratio and because a lower limit is placed on the inductor value to avoid subharmonic oscillations. To ensure stability for duty cycles up to the maximum of 95%, use the following equation to find the minimum inductance.

$$L_{MIN} > \frac{V_{OUT}}{f_{SW} \bullet I_{LOAD(MAX)}} \bullet 1.4$$

where

L_{MIN} is in units of µH

f_{SW} is in units of MHz

Inductor Core Selection

Once the inductance value is determined, the type of inductor must be selected. Core loss is independent of core size for a fixed inductor value, but it is very dependent on inductance selected. As inductance increases, core losses go down. Unfortunately, increased inductance requires more turns of wire and therefore copper losses will increase.

Ferrite designs have very low core loss and are preferred at high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates hard, which means that inductance collapses abruptly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current and consequent output voltage ripple. Do not allow the core to saturate!

Power MOSFET Selection

Four external power MOSFETs must be selected for the LTC7821. The gate drive voltages to these MOSFETs are derived from the $INTV_{CC}$ voltage, which is typically 5.8V. Hence logic-level threshold MOSFETs must be selected. Only the upper-most MOSFET requires a BV_{DSS} greater than V_{IN}, because this MOSFET sees the full V_{IN} voltage during start-up. The other MOSFETs, M2 to M4, need only have a BV_{DSS} greater than $V_{IN}/2$.

During operation, the type of switching also impacts how each power MOSFET is selected. M1 and M2 operate in soft switching mode, so they should have low Qoss •

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Rds_{ON} product. M3 and M4 operate in a manner similar to traditional buck converter, with M3 hard switching while M4 operates in zero voltage switching (ZVS). Therefore M3 and M4 should be chosen with the lowest (Qgd • Rds_{ON}) and (Qg • Rds_{ON}) product, respectively.

MOSFET input capacitance is a combination of several components but can be taken from the typical gate charge curve included on most data sheets (see Figure 10). The curve is generated by forcing a constant input current into the gate of a common source, current source loaded stage and then plotting the gate voltage versus time.

The initial slope is the effect of the gate-to-source and the gate-to-drain capacitance. The flat portion of the curve is the result of the Miller multiplication effect of the gate-to-drain capacitance as the drain drops the voltage across the current source load. The upper sloping line is due to the drain-to-gate accumulation capacitance and the gate-to-source capacitance. The Miller charge (the increase in coulombs on the horizontal axis from a-to-b while the curve is flat) is specified for a given V_{DS} drain voltage, but can be adjusted for different V_{DS} voltage by multiplying the ratio of the application V_{DS} to the curve specified V_{DS} value. A way to estimate the C_{MILLER} term is to take the change in gate charge from point a-and-b on a manufacturer's data sheet and divide by the specified V_{DS} voltage. C_{MILLER} is the most important selection criteria for determining the transition loss term in the MOSFET M3 but is not directly specified on MOSFET data sheets. C_{RSS} and C_{Oss} are specified sometimes but definitions of these parameters are not included.

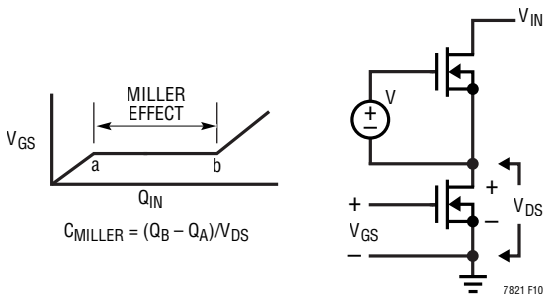


Figure 10. Gate Change Characteristic

In a traditional synchronous buck converter, the current flowing through the upper and lower MOSFET is the same as the inductor current (see Figure 11). In the hybrid topology of the LTC7821, the MOSFET and inductor currents do not match, because the capacitors play a role in energy transfer to the output.

In the first phase (see Figure 12a), M1 and M3 are ON and the capacitor C_{MID} provides part of the inductor current via M3. The rest of the inductor's current is provided through C_{FLY} via M1. If the capacitance of C_{FLY} is the same as C_{MID}, then the inductor's current is equally supplied by both capacitors as shown in Figure 12b. Therefore compared to the traditional buck converter with the same amount of inductor current, less current flowing through M3 means lower switching loss and conduction loss. Since M3 switches hard, this reduction in current reduces the switching loss significantly.

In the 2nd phase, M2 and M4 are ON (see Figure 13a). In this phase, M4 not only has to supply the full inductor

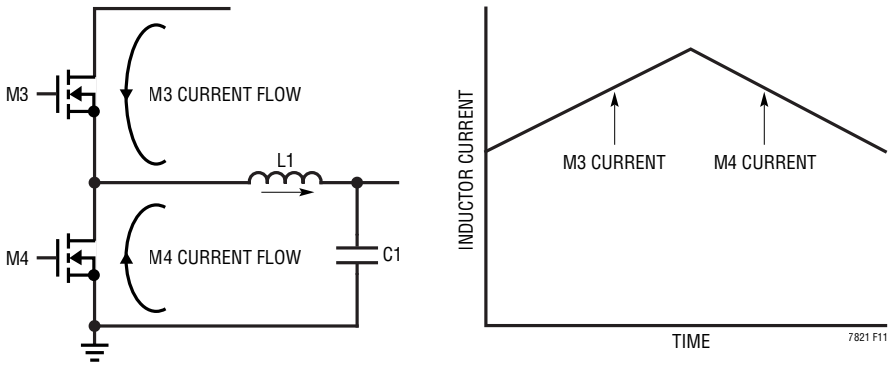
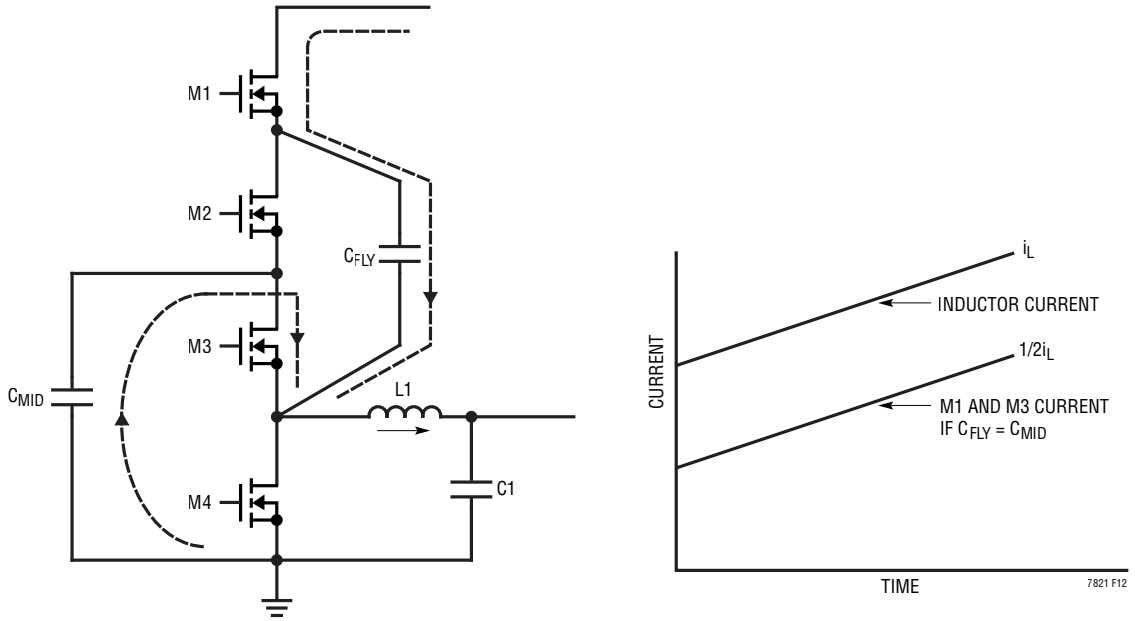


Figure 11. MOSFET's Current of Traditional Synchronous Buck Converter

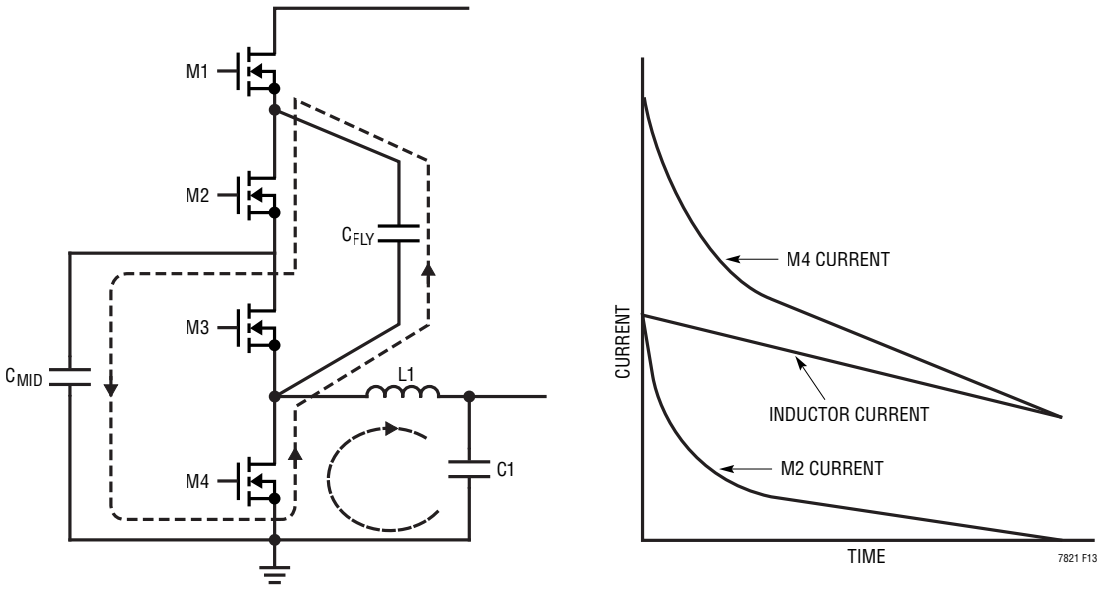
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(12a) CURRENT PATH OF M1 AND M3

(12b) M1 AND M3 CURRENT MAGNITUDE

Figure 12. First Phase M1 and M3 Current Flow



(13a) CURRENT PATH OF M2 AND M4

(13b) M2 AND M4 CURRENT MAGNITUDE

Figure 13. Second Phase M2 and M4 Current Flow

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current, but also carries the balancing current that flows between C_{FLY} and C_{MID} due to an imbalance of voltage between the two capacitors at the end of phase 1. Therefore M4 has an increase in conduction losses compared to its counterpart in a traditional buck converter. The current flowing through M2 is dependent on the voltage differential between the capacitors, their ESR, R_{DSON} of M2 and M4, and inductance of the MOSFETs, capacitors, and board traces (see Figure 13b).

When the controller is operating in continuous mode the duty cycles for M1, M3, M2 and M4 are given by:

$$\text{M1, M3 Switch Duty Cycle} = \frac{2 \bullet V_{OUT}}{V_{IN}}$$

$$\text{M2, M4 Switch Duty Cycle} = \frac{V_{IN} - 2 \bullet V_{OUT}}{V_{IN}}$$

The power dissipation of M1 and M3 is given by:

$$P_{M1} = \left(\frac{I_{MAX} \bullet C_{FLY}}{C_{FLY} + C_{MID}}\right)^2 \left(\frac{2 \bullet V_{OUT}}{V_{IN}}\right)(1+\delta)R_{DS(ON)}$$

$$P_{M3} = \left(\frac{I_{MAX} \bullet C_{MID}}{C_{FLY} + C_{MID}}\right)^2 \left(\frac{2 \bullet V_{OUT}}{V_{IN}}\right)(1+\delta)R_{DS(ON)} + \left(\frac{V_{IN}}{2}\right)^2 \left(\frac{I_{MAX} \bullet C_{MID}}{2 \bullet (C_{FLY} + C_{MID})}\right)(R_{DR})(C_{MILLER}) \bullet \left[\frac{1}{V_{INTVCC} - V_{TH(MIN)}} + \frac{1}{V_{TH(MIN)}}\right] \bullet f$$

where δ is the temperature dependency of $R_{DS(ON)}$, R_{DR} is the effective top driver resistance (approximately 2Ω at $V_{GS} = V_{MILLER}$), and V_{IN} is the input supply. $V_{TH(MIN)}$ is the data sheet specified typical gate threshold voltage specified in the power MOSFET data sheet at the specified drain current. C_{MILLER} is the calculated capacitance using the gate charge curve from the MOSFET data sheet and the technique described above.

If the switching loss contribution of P_{M3} is relatively small compared to its conduction loss, then the overall power dissipation ($P_{M1} + P_{M3}$) will be the lowest when $C_{FLY} = C_{MID}$.

The power dissipation of M2 and M4 is harder to calculate, because the current flowing through these MOSFETs exhibits a 2nd order system response due to the presence of parasitic package inductance of the MOSFETs and capacitors, ESR of the capacitors, $R_{DS(ON)}$ of the MOSFETs and the capacitance of C_{MID} and C_{FLY}. Complicating the matter is that the current could exhibit overdamped, critically damped or underdamped characteristics, depending on the RLC values mentioned above; this would impact the RMS current significantly. Use ADI/LTC power tool to help select M2 and M4.

With the RMS current flowing through M2 and M4 determined, the power dissipation is given by:

$$P_{M2} = I^2_{rms2} \bullet (1+\delta)R_{DS(ON)}$$

$$P_{M4} = I^2_{rms4} \bullet (1+\delta)R_{DS(ON)}$$

C_{FLY} and C_{MID} Selection

In this hybrid topology, capacitors C_{FLY} and C_{MID} are part of the energy transfer elements. Therefore ceramic capacitors are attractive since they have the lowest ESR. However, care should be taken when choosing this type of capacitor. During operation the DC voltage across the C_{FLY} and C_{MID} is approximately half the V_{IN} supply, therefore the voltage rating of the capacitors should be greater than that. As a general rule, select the voltage rating of the capacitor to be twice the operating voltage of the capacitor. For the same voltage rating and capacitance, a larger case size will have a lower failure rate.

In addition, the operating temperature of the capacitors needs to be considered. For operating temperature above 85°C, capacitors with the X7R dielectric need to be used while X5R dielectric is adequate for operation below 85°C. For long term reliability of the capacitor, keep the temperature rise of the capacitor to be below 20°C, preferably 10°C. The temperature rise of the capacitor is dependent on the amount of RMS current through the capacitor and the operating frequency. Consult the manufacturer's data sheet for this data.

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Ceramic capacitors also have a large voltage coefficient, losing close to half their capacitance when the DC bias across a given capacitor is half its rated voltage. The DC bias effect on a capacitor is greater when the case size is smaller. Factor in these effects when deciding on the capacitance.

The ripple voltage of C_{FLY} and C_{MID} is given by:

$$V_{CFLY_RIPPLE} = \frac{I_{OUT} \bullet t_{ON}}{2 \bullet C_{FLY}}$$

$$V_{CMID_RIPPLE} = \frac{I_{OUT} \bullet t_{ON}}{2 \bullet C_{MID}}$$

where I_{OUT} is the output current and t_{ON} is the on-time of M1 and M3.

The ripple voltage on C_{FLY} and C_{MID}, (V_{CFLY_RIPPLE}, V_{CMID_RIPPLE}), contributes significantly to the power dissipated in M2 and M4 (see Power MOSFET Selection section). As a good starting point, select enough capacitance such that the ripple on each capacitor is less than 1% of the DC bias voltage of the capacitor. For example, if the DC bias voltage of the capacitor is 24V, keep the ripple to be less than 240mV. For the lowest conduction loss of MOSFETs M1 and M3 (see Power MOSFET Selection section), select the capacitance of C_{MID} to be the same as that of C_{FLY}.

Schottky Diode and Bootstrap Capacitors Selection

Three diodes are used to form a charge pump circuit to provide the drive voltages for MOSFETs M1 to M3. Figure 14 shows the diodes configuration. The voltages across the following bootstrap capacitors are approximately:

$$V_{BST1_SW1} = V_{INTVCC} - V_{F_D1} - V_{F_D2} - V_{F_D3}$$

$$V_{BST2_MID} = V_{INTVCC} - V_{F_D2} - V_{F_D3}$$

$$V_{BST2_SW3} = V_{INTVCC} - V_{F_D3}$$

where V_{F_DX} is the forward voltage of diode X.

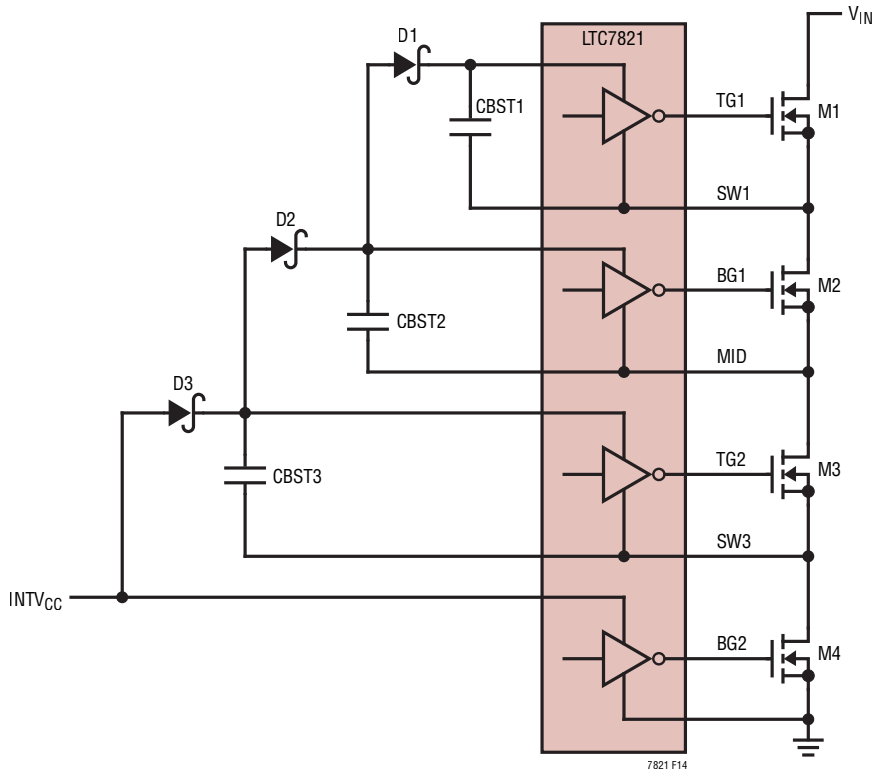


Figure 14. External Charge Pump

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To obtain the most translation in voltage from V_{INTVCC} to drive M1, Schottky diodes are recommended.

The reverse voltage seen by each of the Schottky diodes is approximately:

$$V_{R_DIODE} \cong \frac{V_{IN}}{2}$$

Pay attention to the leakage current when selecting the forward drop of the diodes. In general, the lower the forward drop for the same amount of current flowing through the diode, the higher the leakage current. As these diodes will be operating with large reverse bias for high V_{IN} applications, the leakages are higher, especially at higher operating temperatures.

The charge pump diodes operate as conduits for transferring charge from one capacitor to another and as such are subjected to transient current rather than a DC current. Hence peak forward surge rating is more important than the average current rating. A surge rating of 750mA is a good starting point.

Since the bootstrap capacitor acts as a supply for the MOSFET's driver, select large enough capacitance so that the voltage does not droop considerably when the MOSFETs are being turned ON. As with the C_{MILLER} estimation described in the Power Selection section, the user can use the same graph to obtain the total gate charge for a given gate drive voltage. This can then easily converted to its equivalent gate capacitance by:

$$C_G = \frac{Q_G}{V_{GS}}$$

If the bootstrap capacitor voltage is not allowed to droop by more than 1%, then:

$$C_{BST} \geq 99C_G$$

Besides acting as a supply for their respective MOSFET drivers, C_{BST2} and C_{BST3} also serve as charge pump capacitors. As a good starting point, size C_{BST2} and C_{BST3} as follows:

$$C_{BST3} \geq 2C_{BST2} \geq 2C_{BST1}$$

Soft-Start and Tracking

The LTC7821 has the ability to either soft-start by itself with a capacitor or track the output of another channel or external supply. When configured to soft-start by itself, a capacitor should be connected to its TRACK/SS pin and ground. When RUN pin voltage is below 1.22V, the TRACK/SS is actively pulled to ground in this shutdown state. Once the RUN pin voltage is above 1.22V, the controller powers up and a soft-start current of 10µA begins to flow out of the TRACK/SS pin. However, the TRACK/SS will start charging its soft-start capacitor only after charge balance is completed and the associated active pull-down of the TRACK/SS is released. Note that soft-start or tracking is achieved not by limiting the maximum output current of the controller but by controlling the output ramp voltage according to the ramp rate on the TRACK/SS pin. Current fold-back is disabled during this phase to ensure smooth soft-start or tracking. Depending on whether the EXT_REF feature has been invoked or not, the soft-start or tracking range is defined to be either the voltage range from 0V to 0.8V or 0V to V_{EXT_REF} on the TRACK/SS pin. The total soft-start time can be calculated as:

$$t_{SOFT-START} = \left(0.8 \text{ or } V_{EXT_REF}\right) \bullet \frac{C_{SS}}{10\mu A}$$

Regardless of the mode selected by the MODE/PLLIN pin, the regulator will always start in pulse-skipping mode up to TRACK/SS = 82.5% of 0.8V or V_{EXT_REF}.

Output Voltage Tracking

The LTC7821 allows the user to program how its output ramps up and down by means of the TRACK/SS pins. Through this pin, the output can be set up to either coincidentally or ratio-metrically track another supply's output, as shown in Figure 15. In the following discussions, V_{OUT1} refers to another supply's output (master channel) while V_{OUT2} refers to the LTC7821 output (slave channel) that tracks V_{OUT1}. To implement the coincident tracking in Figure 15a, connect an additional resistive divider to V_{OUT1} and connect its midpoint to the TRACK/SS pin of the LTC7821. The ratio of this divider should be the same as that of the slave channel's feedback divider shown in Figure 16a. In this tracking mode, V_{OUT1} must be set higher than V_{OUT2}.

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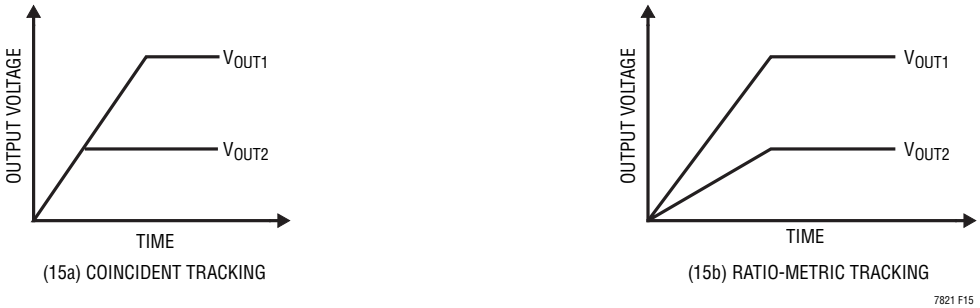


Figure 15. Two Different Methods of Output Voltage Tracking

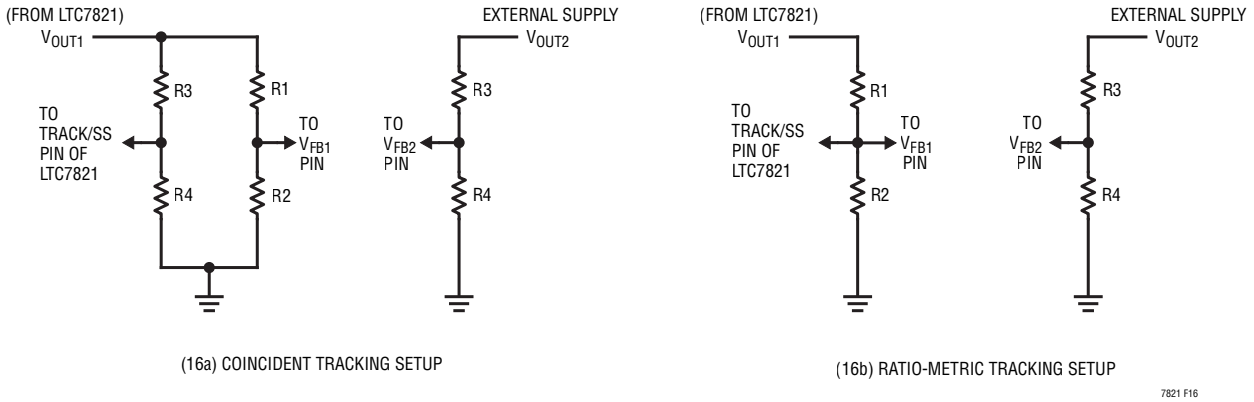


Figure 16. Setup for Coincident and Ratio-Metric Tracking

To implement the ratiometric tracking in Figure 15b, the ratio of the V_{OUT2} divider should be exactly the same as the master channel's feedback divider ratio shown in Figure 16b.

In order to track down another channel or supply after the soft-start has successfully reached 82.5% of 0.8V or V_{EXT_REF}, it is recommended to set the LTC7821 into force continuous mode operation by setting the MODE/PLLIN = 0V. For no load condition, the LTC7821 should be in force continuous mode to ensure good tracking of the master supply.

By selecting different resistors, the LTC7821 can achieve different modes of tracking including the two in Figure 15. The ratio-metric mode uses one less pair of resistors compared to the coincident mode but has lesser output accuracy on V_{OUT2} and is also fully coupled to any variations in V_{OUT1}. In both modes, there is an error in output voltage setting cause by the pin current of TRACK/SS. To minimize this error, use smaller resistor values in the divider.

Output Voltage Setting

The LTC7821 uses its internal reference of 0.8V when the $V_{EXT_REF} \geq 1.3V$. The output voltage is given by:

$$V_{OUT} = 0.8 \bullet \left(1 + \frac{R2}{R1}\right)$$

If the applied voltage to the EXT_REF is less than 1.3V, then V_{OUT} will track EXT_REF voltages between 0.4V and 0.9V, as indicated by the characteristic in Figure 17.

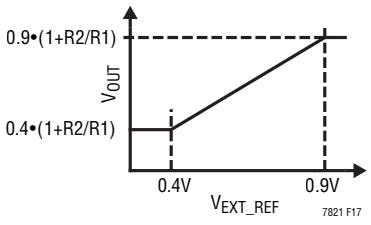


Figure 17. Output Voltage Set By EXT_REF Pin

APPLICATIONS INFORMATION

Due to its unique architecture, the optimal efficiency for the LTC7821 is when $V_{OUT} \cong V_{IN}/4$. For applications that demand optimal efficiency within a range of V_{IN}, EXT_REF could be used to track this V_{IN} variation while maintaining a 4:1 step down ratio at the output. In this type of setup the output voltage will also change with the input. Figure 18 shows a 48V to 12V setup that accounts for V_{IN} variation between 36V to 72V.

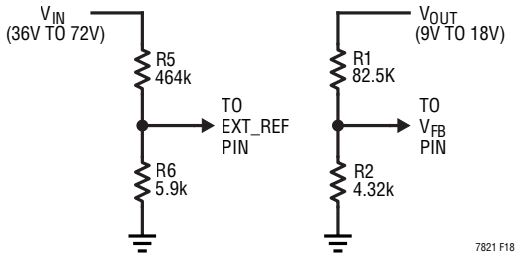


Figure 18. Output Voltage to Track V_{IN} in 4:1 Ratio

The minimum output voltage that can be set for the LTC7821 is limited by the charge balancing circuit and its minimum on-time. The charge balancing circuitry requires at least 2V on the output and is independent of V_{IN}. The minimum on time determines the minimum V_{OUT} by:

$$V_{OUT(MIN)} = \frac{V_{MID} \bullet t_{ON(MIN)}}{T_S}$$

Where T_S is the switching period.

Hence,

$$V_{OUT(MIN)} = MAX\left(2.5V, \frac{V_{MID} \bullet t_{ON(MIN)}}{T_S}\right)$$

The internal charge balancing circuitry requires a minimum differential voltage between $V_{IN}/2$ and V_{OUT} of 2.5V to operate. This limits the maximum output voltage setting to:

$$V_{OUT(MAX)} = \frac{V_{IN}}{2} - 2.5$$

For applications where the load is resistive and acts like a discharging path, the minimum V_{OUT} can be lowered to 0.8V.

Minimum V_{OUT}

During the C_{FLY} capacitor balancing phase, a current of approximately 40mA (I_{SRC}) flows out of SW1 node to charge the flying capacitor C_{FLY} to $V_{IN}/2$. To prevent this current from charging C_{OUT}, an identical amount is sunk (I_{SNK}) away at SW3 node. Figure 21 shows the current path. A minimum output voltage of 2V is needed to ensure the complete sinking of the sourcing current.

In applications that need the output to be regulated below 2V, a resistive load can be added across V_{OUT} to ensure that the voltage will not exceed the regulated value during the capacitor balancing phase. The resistive load value is given by:

$$R_{LOAD} < \frac{V_{OUT}}{0.04}$$

Select R_{LOAD} to be about 70% of the calculated value.

HYS_PRGM Voltage

The voltage on the HYS_PRGM pin sets a window (threshold) centered on $V_{IN}/2$ for fault protection purpose. During operation, if the voltage across MID_SNS and ground deviates beyond this window, a fault is indicated and capacitor balancing begins. Therefore setting the correct window is important as it adds another layer of protection to the power system. In continuous switching, the first order approximate impedance at MID is given by:

$$Z_{MID} = \frac{1}{8 \bullet C_{FLY} \bullet f_{SW}} \bullet \left(\frac{e^{\frac{D1 \bullet T_S}{2 \bullet \tau 1}} + e^{\frac{-D1 \bullet T_S}{2 \bullet \tau 1}}}{e^{\frac{D1 \bullet T_S}{2 \bullet \tau 1}} - e^{\frac{-D1 \bullet T_S}{2 \bullet \tau 1}}} + \frac{e^{\frac{D2 \bullet T_S}{2 \bullet \tau 2}} + e^{\frac{-D2 \bullet T_S}{2 \bullet \tau 2}}}{e^{\frac{D2 \bullet T_S}{2 \bullet \tau 2}} - e^{\frac{-D2 \bullet T_S}{2 \bullet \tau 2}}} \right)$$

$$= \frac{1}{8 \bullet C_{FLY} \bullet f_{SW}} \bullet \left(\coth\left(\frac{D1 \bullet T_S}{2 \bullet \tau 1}\right) + \coth\left(\frac{D2 \bullet T_S}{2 \bullet \tau 2}\right) \right)$$

where:

T_S = Switching period

f_{SW} = Switching frequency

D1 = Duty cycle of MOSFET 1 and 3

D2 = Duty cycle of MOSFET 2 and 4

$\tau 1 = (R_{ON1} + R_{ON3} + R_{ESR_FLY}) \bullet C_{FLY}$

$\tau 2 = (R_{ON2} + R_{ON4} + R_{ESR_FLY}) \bullet C_{FLY}$

R_{ONX} = Resistance of MOSFET X in Ω

APPLICATIONS INFORMATION

Figure 19a shows a typical LTC7821 output stage setup while 19b shows the equivalent circuit. Note that M3 and M4 form the buck converter switches, taking its power from MID, with its voltage given by:

$$V_{MID} = \frac{V_{IN}}{2} - \left(I_{OUT} \bullet \frac{V_{OUT}}{V_{IN}} \bullet \frac{1}{\eta} \right) \bullet Z_{MID}$$

where η = efficiency of the buck converter.

A good conservative number to use for η is 0.9.

The above equation gives us the average MID voltage and does not include the AC ripple on it. The C_{MID} ripple voltage is given by (see C_{FLY} and C_{MID} Selection section):

$$V_{CMID_RIPPLE} = \frac{I_{OUT} \bullet t_{ON}}{2C_{MID}}$$

Therefore the maximum deviation of MID voltage from $V_{IN}/2$ is given by:

$$\Delta V_{MID_IDEAL} = \frac{V_{IN}}{2} - V_{MID} - \frac{I_{OUT} \bullet t_{ON}}{2C_{MID}}$$

Use the above equation as a guideline to set the HYS_PRGM voltage.

Design Example

A 48V to 5V, 25A operating at 500kHz application is used as an example. Since the output current is high, DCR sensing is used to regulate the current loop.

For 500kHz operation, a 68k resistor is connected from FREQ to ground.

Since V_{IN} = 48V, Infineon BSC027N06LS5 is chosen for M1. This is an 60V MOSFET. For M2 to M4, 30V MOSFETs are sufficient for this application. For M2 and M3, Infineon BSC032N04LS are selected and an Infineon BSC014N04LSI is selected for M4.

$$\text{M1, M3 DUTY CYCLE} = \frac{5}{24} = 0.208$$

$$T_{OFF} = (1 - 0.208) \bullet 2\mu s = 1.58\mu s$$

With inductor current ripple initially scaled to 40% of output current, $\Delta I_L = 0.4 \bullet 25 = 10A$,

$$\text{Hence, } L = \frac{V_{OUT} \bullet T_{OFF}}{\Delta I_L} = \frac{5 \bullet 1.58 \bullet 10^{-6}}{10} = 0.79\mu H$$

An inductance of 0.9µH is selected (Coilcraft SER2011-901L) instead and this give ΔI_L = 8.8A. The RMS current through the inductor is:

$$I_{RMS_L} = \sqrt{\left(I^2_{OUT} + \frac{\Delta I^2_L}{12} \right)}$$

$$= \sqrt{25^2 + \frac{0.4^2}{12}}$$

$$= 25.2A$$

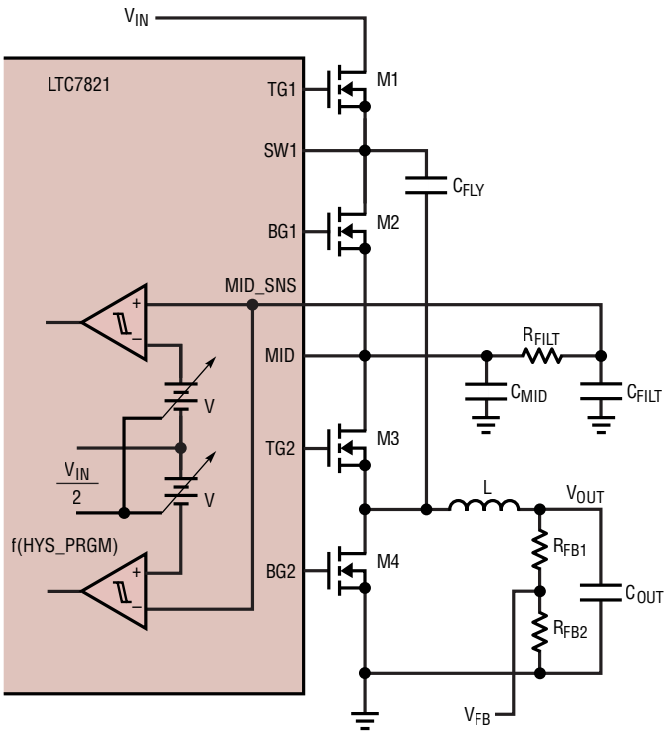
From the manufacturer data sheet, the rise in temperature of the inductor is 15°C. However, this rise does not account for the conduction of heat from the MOSFETs through the PCB that increases the overall inductor's temperature. Depending on how the board is being laid out and how much air flow is applied, the net increase in temperature could be higher. For this design example, assume the net temperature rise to be 50°C.

The typical DCR of the inductor is typically 1.2mΩ with a maximum of 1.34 mΩ and with a 50°C rise in temperature and assuming the temperature coefficient of the DCR at 0.4%/°C, the maximum DCR is:

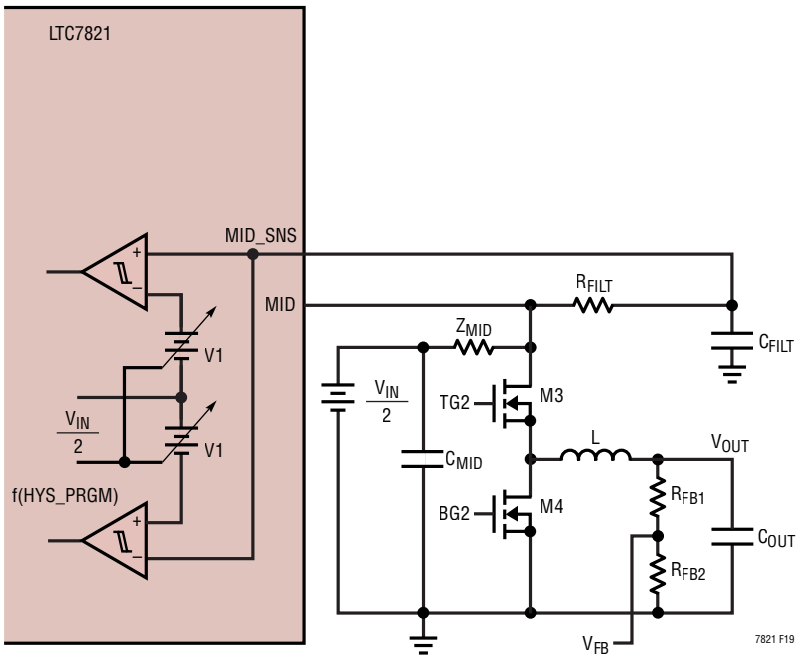
$$R_{DC\Delta = 15°C} = 1.34 \bullet \left(1 + \frac{0.4 \bullet 50}{100} \right) \bullet 10^{-3}$$

$$= 1.61m\Omega$$

APPLICATIONS INFORMATION



(19a) LTC7821 OUTPUT SETUP



(19b) LTC7821 THEVEVIN OUTPUT EQUIVALENT

Figure 19. LTC7821 Output Setup

APPLICATIONS INFORMATION

With a V_{SENSE} = 50mV, the DCR will set the peak inductor current to be 31A. With a ripple ΔI_L of 8.8A, the application will provide 25A of output current.

For the sensing network, select C1 = 0.22µF, then:

$$R8 = \frac{L}{C1 \bullet DCR}$$
$$= 3.4k\Omega$$

For the design, a 3.32k resistor is used.

The next components to select are the C_{MID} and C_{FLY}. In this example,

$$C_{MID} = C_{FLY}$$

To maintain ripple at C_{MID} and C_{FLY} to be 1% of its DC bias:

$$\Delta V_{CMID} \text{ and } \Delta V_{CFLY} = 0.01 \bullet 24$$
$$= 240mV$$

Hence,

$$C_{FLY} = \frac{I_{OUT} \bullet t_{ON}}{2 \bullet \Delta V_{CMID}}$$
$$= \frac{25 \bullet 0.42 \bullet 10^{-6}}{2 \bullet 0.24}$$
$$= 21.88\mu F$$
$$= C_{MID}$$

The voltage rating chosen for these capacitors is 50V and even with this rating, the actual capacitance is lower due to its voltage coefficient. 6 × 10µF is chosen for each C_{MID} and C_{FLY}. With this value of C_{MID}, the voltage ripple at MID is now:

$$V_{CMID_ripple} = \frac{I_{OUT} \bullet t_{ON}}{2 \bullet 60 \bullet 10^{-6}}$$
$$= 87.5mV$$

The next components to select are the bootstrap capacitors. For M1, the gate charge needed to charge its gate from V_{GS} = 0V to 6V is:

$$Q_G = 9nC$$

Therefore, it's equivalent gate capacitance is:

$$C_G = \frac{Q_G}{V_{GS}} = 1.5nF$$

Hence, $C_{BST1} = 99 \bullet C_G$

$$= 0.15\mu F$$

Use, C_{BST1} = 0.22µF

C_{BST2} = 0.47µF

C_{BST3} = 1µF

For the Schottky diodes, Central's CMDSH-4 are used.

From the manufacturer data sheet, the R_{DSON} of M1 to M4 are 3.1mΩ, 3.2mΩ, 3.2mΩ, and 1.4mΩ respectively. The equivalent impedance at MID node, Z_{MID}, can be calculated to be:

$$Z_{MID} = \frac{1}{8 \bullet C_{FLY} \bullet f_{SW}} \bullet \left(\coth\left(\frac{D1 \bullet T_S}{2 \bullet \tau 1}\right) + \coth\left(\frac{D2 \bullet T_S}{2 \bullet \tau 2}\right)\right)$$
$$= 18.15m\Omega$$

This will result in an average MID voltage of:

$$V_{MID} = V_{IN}/2 - (31A \bullet 18.15m\Omega)$$
$$= 23.437V$$

Factoring in the ripple voltage on C_{MID}, the minimum V_{MID} is:

$$V_{MID_MIN} = 23.437 - 0.0875$$
$$= 23.35V$$

This is 650mV lower than the ideal voltage of 24V at MID point. Therefore set the voltage at HYST_PRGM pin to be 1V with a resistor of 100k.

The completed circuit for this design example is shown in Figure 20.

APPLICATIONS INFORMATION

Minimum On-Time Considerations

Minimum on-time $t_{ON(MIN)}$ is the smallest time duration that the LTC7821 is capable of turning on the top MOSFET. It is determined by internal timing delays and the gate charge required to turn on the top MOSFET. Low duty cycle applications may approach this minimum on-time limit and care should be taken to ensure that:

$$t_{ON(MIN)} < \frac{2 \bullet V_{OUT}}{V_{IN}(f)}$$

If the duty cycle falls below what can be accommodated by the minimum on-time, the controller will begin to skip cycles. The output voltage will continue to be regulated, but the ripple voltage and current will increase.

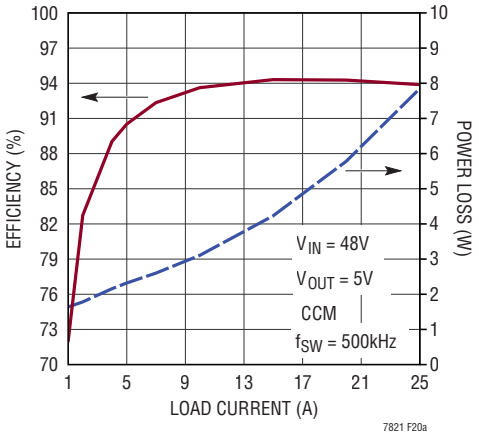
The minimum on-time for the LTC7821 is approximately 210ns, with reasonably good PCB layout, minimum 30% inductor current ripple and at least 10mV – 15mV ripple on the current sense signal. The minimum on-time can be affected by PCB switching noise in the voltage and current loop. As the peak sense voltage decreases the minimum on-time increases. This is of particular concern in forced continuous applications with low ripple current at light loads. If the duty cycle drops below the minimum on-time limit in this situation, a significant amount of cycle skipping can occur with correspondingly larger current and voltage ripple.

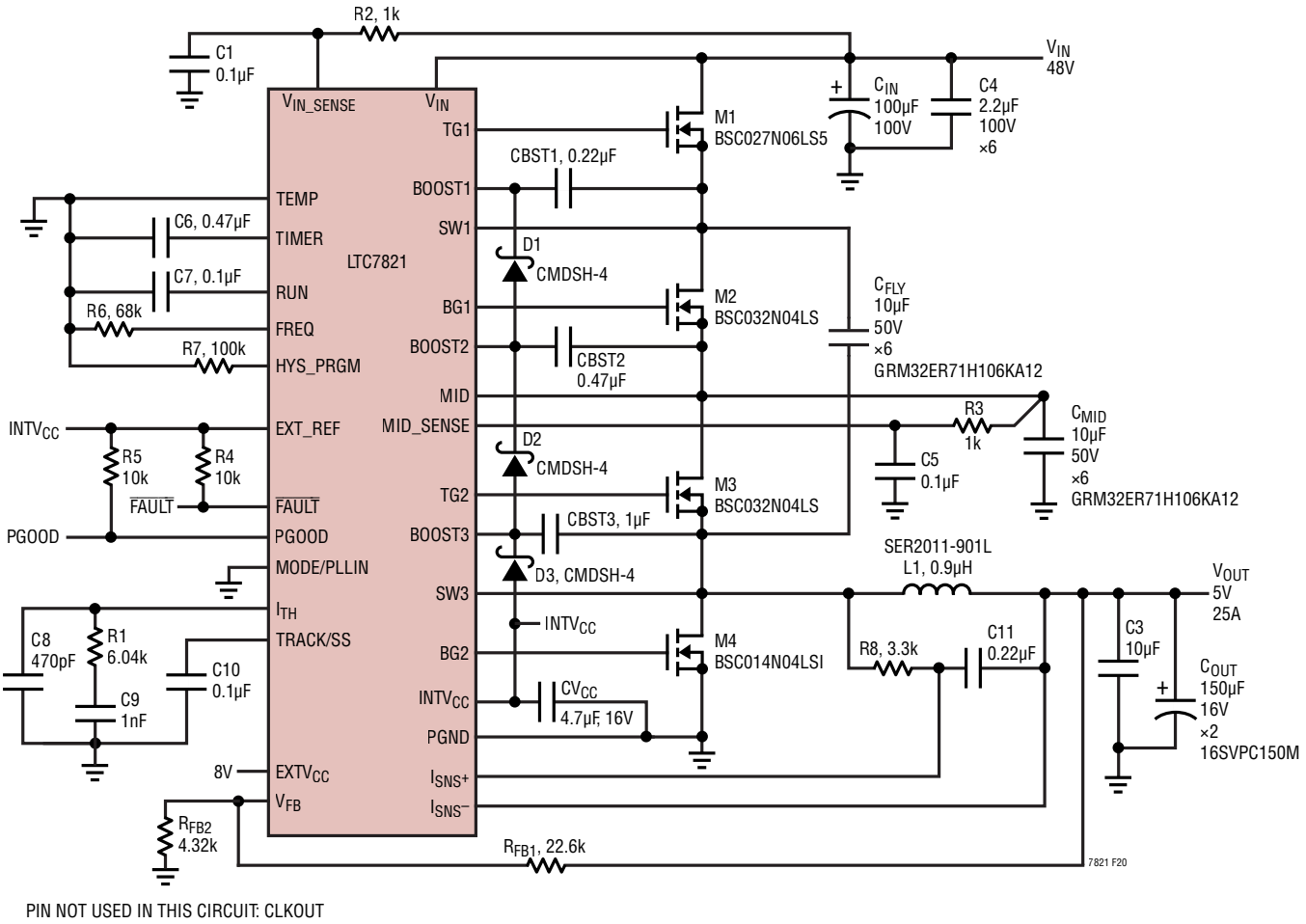
Multiphase Operation

For high output power applications, two LTC7821's can be paralleled to create a dual phase single output configuration. Figure 22 shows the key signal connections between the two LTC7821s.

APPLICATIONS INFORMATION

Efficiency and Power Loss for 48V to 5V vs Load Current





PIN NOT USED IN THIS CIRCUIT: CLKOUT

Figure 20. A 48V to 5V, 500kHz, 25A Application

APPLICATIONS INFORMATION

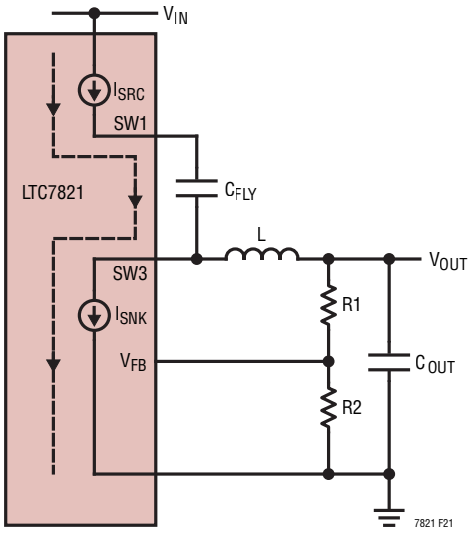


Figure 21. C_{FLY} Prebias Current Path

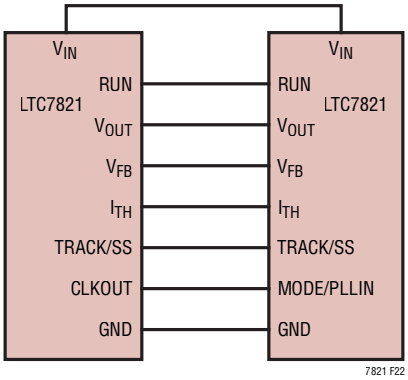
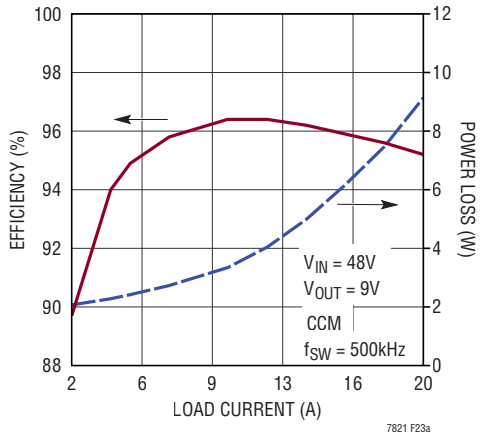
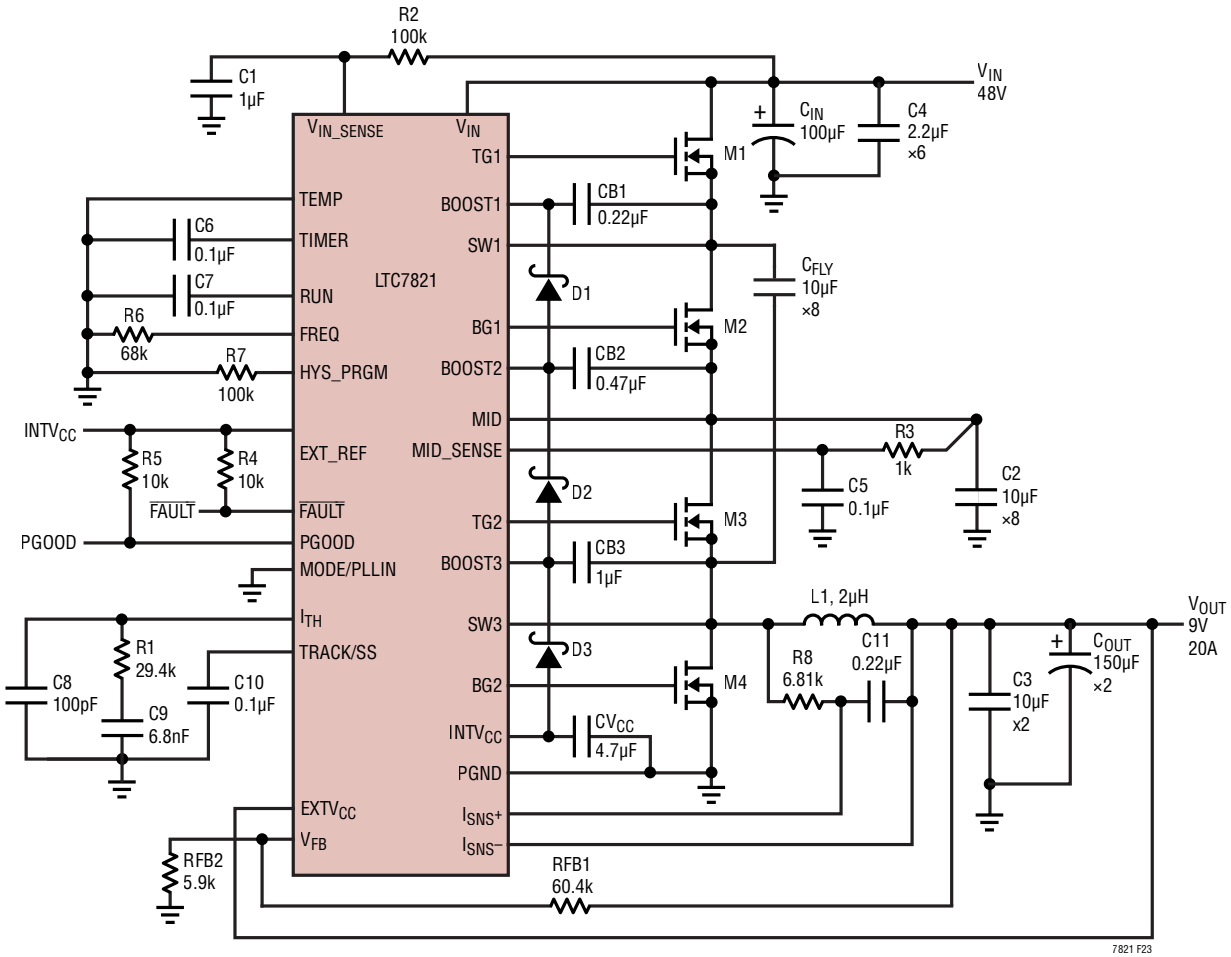


Figure 22. Connection of Key Signals of LTC7821 for Dual Phase Operation

APPLICATIONS INFORMATION

Efficiency and Power Loss for 48V to 9V vs Load Current





M1: INFINEON BSC057N08NS3
M2, M3: INFINEON BSC032N04LS
M4: INFINEON BSC014N04LSI

L1: COILCRAFT SER2011-202ML
CFLY, C2: MURATA GRM32ER71H106KA12
D1 TO D3: CENTRAL SEMICONDUCTOR CMDSH-4

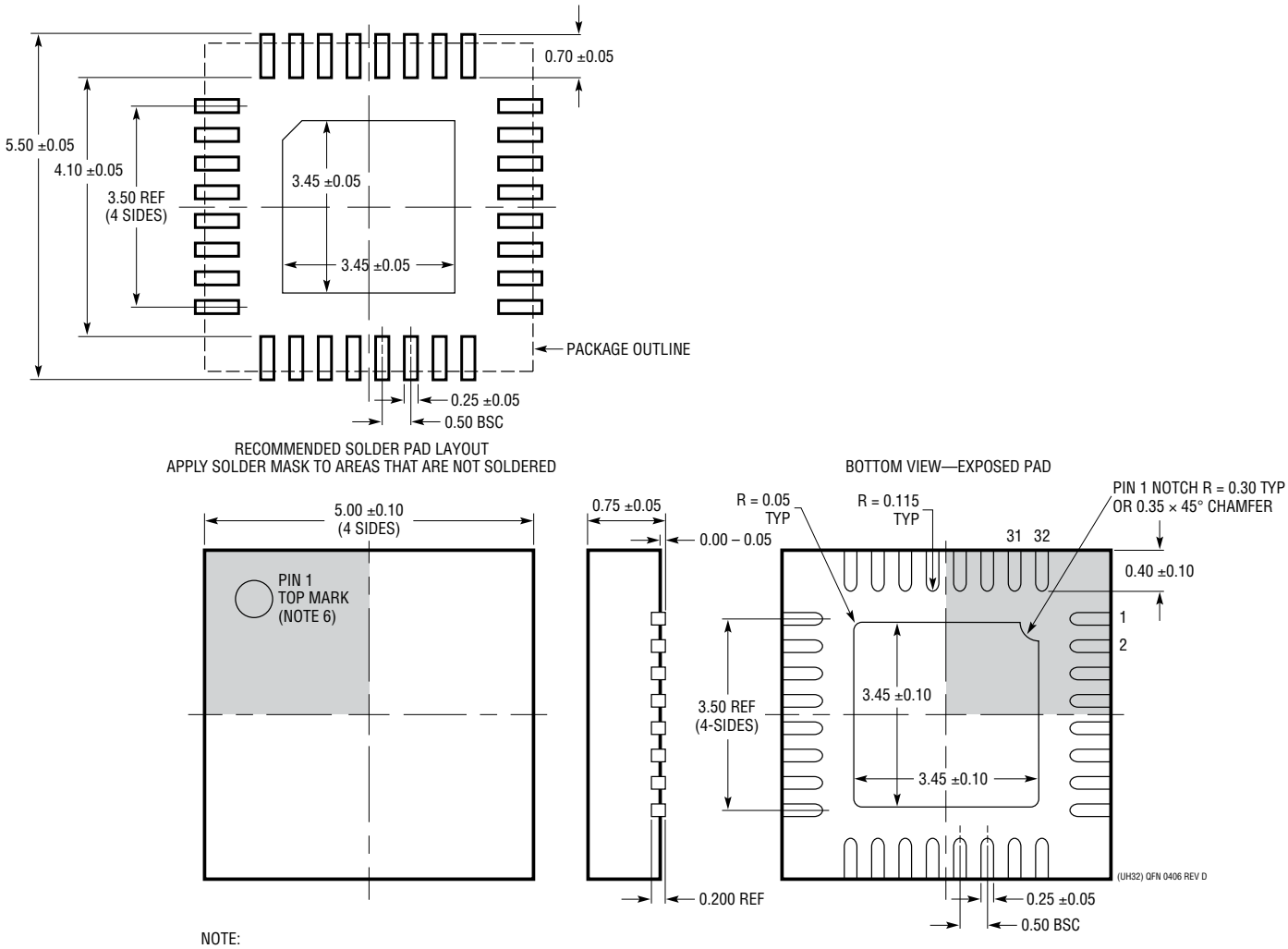
PIN NOT USED IN THIS CIRCUIT: CLKOUT

Figure 23. 500kHz 48V to 9V, 20A Step-Down Converter

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LTC7821#packaging for the most recent package drawings.

UH Package
32-Lead Plastic QFN (5mm × 5mm)
(Reference LTC DWG # 05-08-1693 Rev D)



NOTE:
1. DRAWING PROPOSED TO BE A JEDEC PACKAGE OUTLINE
   M0-220 VARIATION WHHD-(X) (TO BE APPROVED)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE
   MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION
   ON THE TOP AND BOTTOM OF PACKAGE

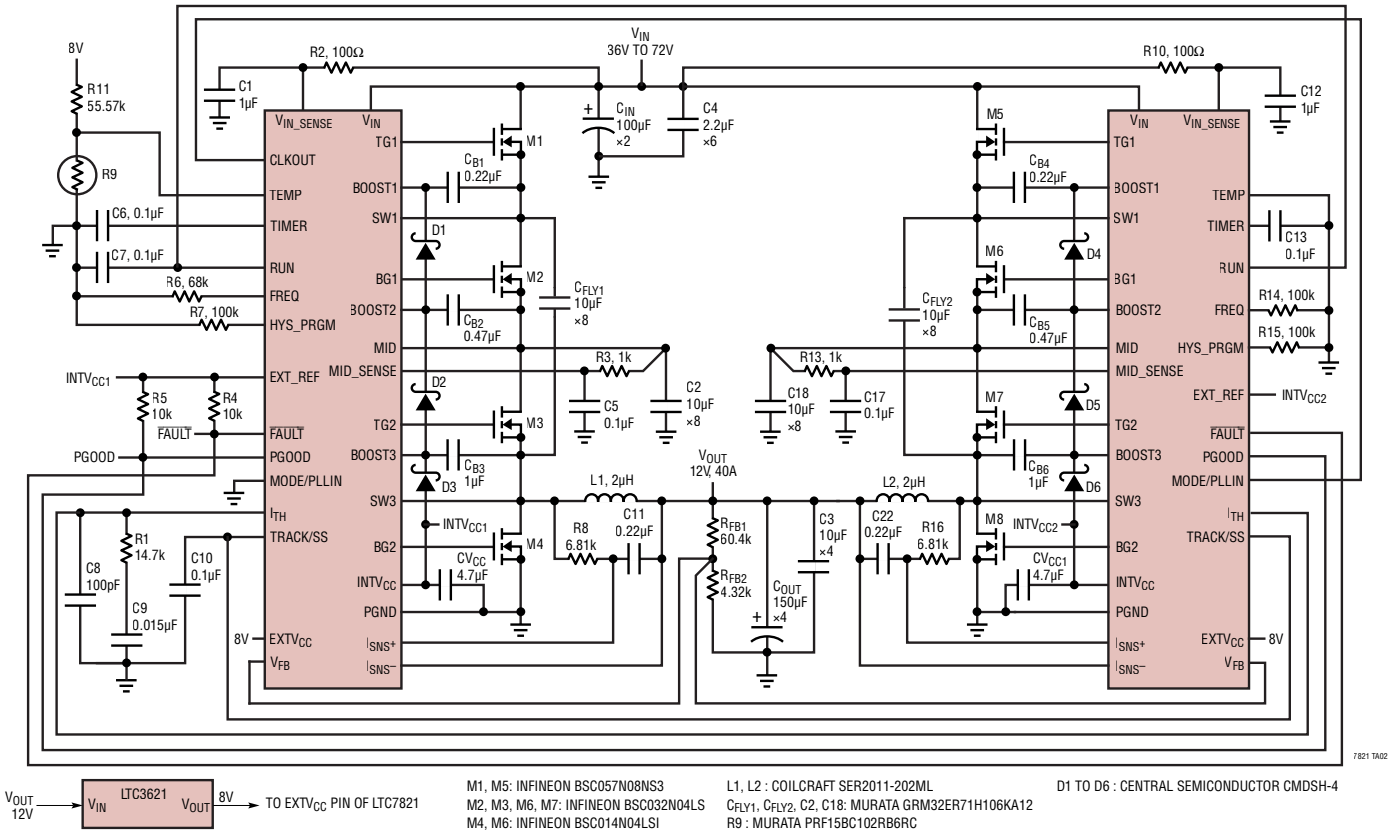
Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	04/18	Corrected Note 4 to Note 5 on EC table	3
		Corrected conditions for I_{VIN}, VIN_SENSE and g_m	3
		Remove references to Timing Diagram	5
		Update RUN pin description	9
		Corrected current source on RUN pin from 10µA to 1µA	11
		Fixed text formatting on “RD” symbol	18
		Updated Soft-Start time formula for clarity	24
		Corrected C11 to C1	28

TYPICAL APPLICATION

High Efficiency 500kHz 2-Phase 48V to 12V at 40A Step-Down Converter



M1, M5: INFINEON BSC057N08NS3
M2, M3, M6, M7: INFINEON BSC032N04LS
M4, M6: INFINEON BSC014N04LSI

L1, L2 : COILCRAFT SER2011-202ML
C_{FLY1}, C_{FLY2}, C2, C18: MURATA GRM32ER71H106KA12
R9 : MURATA PRF15BC102RB6RC

D1 TO D6 : CENTRAL SEMICONDUCTOR CMDSH-4

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC7820	Fixed Ratio High Power Inductorless (Charge Pump) DC/DC Controller	6V < V ≤ V_{IN} 72V, Fixed 50% Duty Cycle, 100kHz to 1MHz Switching Frequency (4mm × 5mm) UFD Package
LTC3895	150V Low I_Q, Synchronous Step-Down DC/DC Controller	4V ≤ V_{IN} ≤ 140V, 150V_{PK}, 0.8V ≤ V_{OUT} ≤ 24V, I_Q = 50µA, PLL Fixed Frequency 50kHz to 900kHz
LTC3810	100V Synchronous Step-Down DC/DC Controller	Constant On-Time Valley Current Mode 6.2V ≤ V_{IN} ≤ 100V, 0.8V ≤ V_{OUT} ≤ 0.93V_{IN}, SSOP-28
LTC3891	60V, Low I_Q, Synchronous Step-Down DC/DC Controller with 99% Duty Cycle	4V ≤ V_{IN} ≤ 60V, 0.8V ≤ V_{OUT} ≤ 24V, I_Q = 50µA, PLL Fixed Frequency 50kHz to 900kHz
LT3840	60V, Low I_Q, Synchronous Step-Down Controller with Integrated Buck-Boost Bias Voltage Regulator	2.5V ≤ V_{IN} ≤ 60V, 1.23V ≤ V_{OUT} ≤ 60V, I_Q = 75µA, Synchronizable Fixed Frequency 100kHz to 600kHz
LTC3892/ LTC3892-1	60V Low I_Q, Dual, 2-Phase Synchronous Step-Down DC/DC Controller with 99% Duty Cycle	4V ≤ V_{IN} ≤ 60V, 0.8V ≤ V_{OUT} ≤ 0.99V_{IN}, PLL Fixed Frequency 50kHz to 900kHz, Adjustable 5V to 10V Gate Drive, I_Q = 29µA
LTC7813	Low I_Q, Synchronous Boost + Buck DC/DC Controller	4.5V (Down to 2.2V After Start-Up) ≤ V_{IN} ≤ 60V, 0.8V ≤ V_{OUT} ≤ 60V, Adjustable 5V to 10V Gate Drive, I_Q = 33µA
LT8705A	80V V_{IN} and V_{OUT} Synchronous 4-Switch Buck-Boost DC/DC Controller	2.8V ≤ V_{IN} ≤ 80V, 100kHz to 400kHz Programmable Operating Frequency (5mm × 7mm) QFN-38 and TSSOP-38
LTC3886	60V Dual Output Step-Down Controller with PSM	4.5V ≤ V_{IN} ≤ 60V, 0.5V ≤ V_{OUT} (±0.5%) ≤ 13.8V, Input Current Sense, I^2C/PMBus Interface with EEPROM and 16-Bit ADC
LTC3871	Bidirectional Multiphase Synchronous Buck or Boost Controller	Regulation of Input Voltage, Output Voltage or Current V_{HIGH} Up to 100V, V_{LOW} Voltages Up to 30V

Rev A

D16842-0-4/18(A)

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