LTC6910-1
LTC6910-2/LTC6910-3

Digitally Controlled Programmable Gain Amplifiers in SOT-23

FEATURES

- **3-Bit Digital Gain Control in Three Gain-Code Options**
- **Rail-to-Rail Input Range**
- **Rail-to-Rail Output Swing**
- **Single or Dual Supply: 2.7V to 10.5V Total**
- 11MHz Gain Bandwidth Product
- Input Noise Down to 8nV/$\sqrt{Hz}$
- System Dynamic Range to 120dB
- Input Offset Voltage: 1.5mV
- 8-Pin Low Profile (1mm) SOT-23 (ThinSOT™) Package

APPLICATIONS

- Data Acquisition Systems
- Dynamic Gain Changing
- Automatic Ranging Circuits
- Automatic Gain Control

DESCRIPTION

The LTC®6910 family are low noise digitally programmable gain amplifiers (PGAs) that are easy to use and occupy very little PC board space. The inverting gain is adjustable using a 3-bit digital input to select gains of 0, 1, 2, 5, 10, 20, 50 and 100V/V in the LTC6910-1; 0, 1, 2, 4, 8, 16, 32 and 64V/V in the LTC6910-2; and 0, 1, 2, 3, 4, 5,6 and 7V/V in the LTC6910-3.

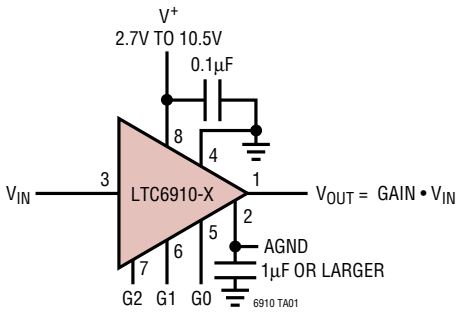
The LTC6910-Xs are inverting amplifiers with rail-to-rail output. When operated with unity gain, they will also process rail-to-rail input signals. A half-supply reference generated internally at the AGND pin supports single power supply applications. Operating from single or split supplies from 2.7V to 10.5V, the LTC6910-X family is offered in an 8-lead SOT-23 package.

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U.S. Patent Number 6121908.

TYPICAL APPLICATION

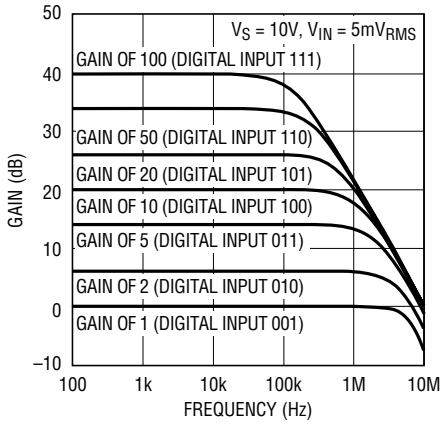
Single Supply Programmable Amplifier

DIGITAL INPUTS			GAIN IN VOLTS/VOLT		
G2	G1	G0	6910-1	6910-2	6910-3
0	0	0	0	0	0
0	0	1	–1	–1	–1
0	1	0	–2	–2	–2
0	1	1	–5	–4	–3
1	0	0	–10	–8	–4
1	0	1	–20	–16	–5
1	1	0	–50	–32	–6
1	1	1	–100	–64	–7



PIN 2 (AGND) PROVIDES BUILT-IN HALF-SUPPLY REFERENCE WITH INTERNAL RESISTANCE OF 5k. AGND CAN ALSO BE DRIVEN BY A SYSTEM ANALOG GROUND REFERENCE NEAR HALF SUPPLY

Frequency Response (LTC6910-1)

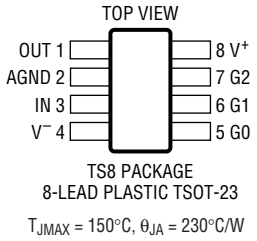


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Total Supply Voltage (V+ to V–) 11V
Input Current ..... ±25mA
Operating Temperature Range (Note 2)
LTC6910-1C, -2C, -3C ..... –40°C to 85°C
LTC6910-1I, -2I, -3I ..... –40°C to 85°C
LTC6910-1H, -2H, -3H ..... –40°C to 125°C
Specified Temperature Range (Note 3)
LTC6910-1C, -2C, -3C ..... –40°C to 85°C
LTC6910-1I, -2I, -3I ..... –40°C to 85°C
LTC6910-1H, -2H, -3H ..... –40°C to 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)..... 300°C

PACKAGE/ORDER INFORMATION



TS8 PACKAGE
8-LEAD PLASTIC TSOT-23

T_{JMAX} = 150°C, θ_{JA} = 230°C/W

ORDER PART NUMBER
LTC6910-1CTS8 LTC6910-1ITS8 LTC6910-1HTS8 LTC6910-2CTS8 LTC6910-2ITS8 LTC6910-2HTS8 LTC6910-3CTS8 LTC6910-3ITS8 LTC6910-3HTS8
TS8 PART MARKING*
LTB5 (6910-1) LTACQ (6910-2) LTACS (6910-3)

Consult LTC Marketing for parts specified with wider operating temperature ranges.

*The temperature grades are identified by a label on the shipping container.

GAIN SETTINGS AND PROPERTIES

Table 1. LTC6910-1

G2	G1	G0	NOMINAL VOLTAGE GAIN		NOMINAL LINEAR INPUT RANGE (V_{P-P})			NOMINAL INPUT IMPEDANCE (kΩ)
			Volts/Volt	(dB)	Dual 5V Supply	Single 5V Supply	Single 3V Supply	
0	0	0	0	–120	10	5	3	(Open)
0	0	1	–1	0	10	5	3	10
0	1	0	–2	6	5	2.5	1.5	5
0	1	1	–5	14	2	1	0.6	2
1	0	0	–10	20	1	0.5	0.3	1
1	0	1	–20	26	0.5	0.25	0.15	1
1	1	0	–50	34	0.2	0.1	0.06	1
1	1	1	–100	40	0.1	0.05	0.03	1

GAIN SETTINGS AND PROPERTIES

Table 2. LTC6910-2

G2	G1	G0	NOMINAL VOLTAGE GAIN		NOMINAL LINEAR INPUT RANGE (V_{P-P})			NOMINAL INPUT IMPEDANCE (kΩ)
			Volts/Volt	(dB)	Dual 5V Supply	Single 5V Supply	Single 3V Supply	
0	0	0	0	–120	10	5	3	(Open)
0	0	1	–1	0	10	5	3	10
0	1	0	–2	6	5	2.5	1.5	5
0	1	1	–4	12	2.5	1.25	0.75	2.5
1	0	0	–8	18.1	1.25	0.625	0.375	1.25
1	0	1	–16	24.1	0.625	0.313	0.188	1.25
1	1	0	–32	30.1	0.313	0.156	0.094	1.25
1	1	1	–64	36.1	0.156	0.078	0.047	1.25

Table 3. LTC6910-3

G2	G1	G0	NOMINAL VOLTAGE GAIN		NOMINAL LINEAR INPUT RANGE (V_{P-P})			NOMINAL INPUT IMPEDANCE (kΩ)
			Volts/Volt	(dB)	Dual 5V Supply	Single 5V Supply	Single 3V Supply	
0	0	0	0	–120	10	5	3	(Open)
0	0	1	–1	0	10	5	3	10
0	1	0	–2	6	5	2.5	1.5	5
0	1	1	–3	9.5	3.33	1.67	1	3.3
1	0	0	–4	12	2.5	1.25	0.75	2.5
1	0	1	–5	14	2	1	0.6	2
1	1	0	–6	15.6	1.67	0.83	0.5	1.7
1	1	1	–7	16.9	1.43	0.71	0.43	1.4

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications that apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_S = 5V, AGND = 2.5V, Gain = 1 (Digital Inputs 001), R_L = 10k to midsupply point, unless otherwise noted.

PARAMETER	CONDITIONS		C, I SUFFIXES MIN	C, I SUFFIXES TYP	C, I SUFFIXES MAX	H SUFFIX MIN	H SUFFIX TYP	H SUFFIX MAX	UNIT
Specifications for the LTC6910-1, LTC6910-2 and LTC6910-3									
Total Supply Voltage		●	2.7		10.5	2.7		10.5	V
Supply Current	V_S = 2.7V, V_{IN} = 1.35V	●		2	3		2	3	mA
	V_S = 5V, V_{IN} = 2.5V	●		2.4	3.5		2.4	3.5	mA
	V_S = ±5V, V_{IN} = 0V, Pins 5, 6, 7 = –5V or 5V	●		3	4.5		3	4.5	mA
	V_S = ±5V, V_{IN} = 0V, Pin 5 = 4.5V, Pins 6, 7 = 0.5V (Note 4)	●		3.5	4.9		3.5	4.9	mA
Output Voltage Swing LOW (Note 5)	V_S = 2.7V, R_L = 10k to Midsupply Point	●		12	30		12	30	mV
	V_S = 2.7V, R_L = 500Ω to Midsupply Point	●		50	100		50	100	mV
	V_S = 5V, R_L = 10k to Midsupply Point	●		20	40		20	40	mV
	V_S = 5V, R_L = 500Ω to Midsupply Point	●		90	160		90	160	mV
	V_S = ±5V, R_L = 10k to 0V	●		30	50		30	50	mV
	V_S = ±5V, R_L = 500Ω to 0V	●		180	250		180	270	mV
Output Voltage Swing HIGH (Note 5)	V_S = 2.7V, R_L = 10k to Midsupply Point	●		10	20		10	20	mV
	V_S = 2.7V, R_L = 500Ω to Midsupply Point	●		50	80		50	85	mV
	V_S = 5V, R_L = 10k to Midsupply Point	●		10	30		10	30	mV
	V_S = 5V, R_L = 500Ω to Midsupply Point	●		80	150		80	150	mV
	V_S = ±5V, R_L = 10k to 0V	●		20	40		20	40	mV
	V_S = ±5V, R_L = 500Ω to 0V	●		180	250		180	250	mV
Output Short-Circuit Current (Note 6)	V_S = 2.7V			±27			±27		mA
	V_S = ±5V			±35			±35		mA
AGND Open-Circuit Voltage	V_S = 5V	●	2.45	2.5	2.55	2.45	2.5	2.55	V
AGND Rejection (i.e., Common Mode Rejection or CMRR)	V_S = 2.7V, V_{AGND} = 1.1V to Upper AGND Limit	●	55	80		50	80		dB
	V_S = ±5V, V_{AGND} = –2.5V to 2.5V	●	55	75		50	75		dB
Power Supply Rejection Ratio (PSRR)	V_S = 2.7V to ±5V	●	60	80		60	80		dB
Signal Attenuation at Gain = 0 Setting	Gain = 0 (Digital Inputs 000), f = 20kHz	●		–122			–122		dB
Slew Rate	V_S = 5V, V_{OUT} = 2.8V_{P-P}			12			12		V/µs
	V_S = ±5V, V_{OUT} = 2.8V_{P-P}			16			16		V/µs
Digital Input “High” Voltage	V_S = 2.7V	●	2.43			2.43			V
	V_S = 5V	●	4.5			4.5			V
	V_S = ±5V	●	4.5			4.5			V
Digital Input “Low” Voltage	V_S = 2.7V	●			0.27			0.27	V
	V_S = 5V	●			0.5			0.5	V
	V_S = ±5V	●			0.5			0.5	V
Digital Input Leakage Current Magnitude	$V^- \le$ (Digital Input) $\le V^+$				2			2	µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications that apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_S = 5V, AGND = 2.5V, Gain = 1 (Digital Inputs 001), R_L = 10k to midsupply point, unless otherwise noted.

PARAMETER	CONDITIONS		LTC6910-1C/LTC6910-1I MIN	LTC6910-1C/LTC6910-1I TYP	LTC6910-1C/LTC6910-1I MAX	LTC6910-1H MIN	LTC6910-1H TYP	LTC6910-1H MAX	UNIT
Specifications for LTC6910-1 Only									
Voltage Gain (Note 7)	V_S = 2.7V, Gain = 1, R_L = 10k	●	−0.05	0	0.07	−0.06	0	0.07	dB
	V_S = 2.7V, Gain = 1, R_L = 500Ω	●	−0.1	−0.02	0.06	−0.12	−0.02	0.08	dB
	V_S = 2.7V, Gain = 2, R_L = 10k	●	5.96	6.02	6.08	5.96	6.02	6.08	dB
	V_S = 2.7V, Gain = 5, R_L = 10k	●	13.85	13.95	14.05	13.83	13.95	14.05	dB
	V_S = 2.7V, Gain = 10, R_L = 10k	●	19.7	19.9	20.1	19.7	19.9	20.1	dB
	V_S = 2.7V, Gain = 10, R_L = 500Ω	●	19.6	19.85	20.1	19.4	19.85	20.1	dB
	V_S = 2.7V, Gain = 20, R_L = 10k	●	25.7	25.9	26.1	25.65	25.9	26.1	dB
	V_S = 2.7V, Gain = 50, R_L = 10k	●	33.5	33.8	34.1	33.4	33.8	34.1	dB
	V_S = 2.7V, Gain = 100, R_L = 10k	●	39	39.6	40.2	38.7	39.6	40.2	dB
	V_S = 2.7V, Gain = 100, R_L = 500Ω	●	37.4	39	40.1	36.4	39	40.1	dB
	V_S = 5V, Gain = 1, R_L = 10k	●	−0.05	0	0.07	−0.05	0	0.07	dB
	V_S = 5V, Gain = 1, R_L = 500Ω	●	−0.1	−0.01	0.08	−0.11	−0.01	0.08	dB
	V_S = 5V, Gain = 2, R_L = 10k	●	5.96	6.02	6.08	5.955	6.02	6.08	dB
	V_S = 5V, Gain = 5, R_L = 10k	●	13.8	13.95	14.1	13.75	13.95	14.1	dB
	V_S = 5V, Gain = 10, R_L = 10k	●	19.8	19.9	20.1	19.75	19.9	20.1	dB
	V_S = 5V, Gain = 10, R_L = 500Ω	●	19.6	19.85	20.1	19.45	19.85	20.1	dB
	V_S = 5V, Gain = 20, R_L = 10k	●	25.8	25.9	26.1	25.70	25.9	26.1	dB
	V_S = 5V, Gain = 50, R_L = 10k	●	33.5	33.8	34.1	33.4	33.8	34.1	dB
	V_S = 5V, Gain = 100, R_L = 10k	●	39.3	39.7	40.1	39.1	39.7	40.1	dB
	V_S = 5V, Gain = 100, R_L = 500Ω	●	38	39.2	40.1	37	39.2	40.1	dB
	V_S = ±5V, Gain = 1, R_L = 10k	●	−0.05	0	0.07	−0.05	0	0.07	dB
	V_S = ±5V, Gain = 1, R_L = 500Ω	●	−0.1	−0.01	0.08	−0.1	−0.01	0.08	dB
	V_S = ±5V, Gain = 2, R_L = 10k	●	5.96	6.02	6.08	5.96	6.02	6.08	dB
	V_S = ±5V, Gain = 5, R_L = 10k	●	13.80	13.95	14.1	13.80	13.95	14.1	dB
	V_S = ±5V, Gain = 10, R_L = 10k	●	19.8	19.9	20.1	19.75	19.9	20.1	dB
	V_S = ±5V, Gain = 10, R_L = 500Ω	●	19.7	19.9	20.1	19.6	19.9	20.1	dB
	V_S = ±5V, Gain = 20, R_L = 10k	●	25.8	25.95	26.1	25.75	25.95	26.1	dB
	V_S = ±5V, Gain = 50, R_L = 10k	●	33.7	33.85	34	33.6	33.85	34	dB
	V_S = ±5V, Gain = 100, R_L = 10k	●	39.4	39.8	40.2	39.25	39.8	40.2	dB
	V_S = ±5V, Gain = 100, R_L = 500Ω	●	38.8	39.6	40.1	38	39.6	40.1	dB
Offset Voltage Magnitude (Internal Op Amp) ($V_{OS(OA)}$) (Note 8)		●		1.5	9		1.5	11	mV
Offset Voltage Drift (Internal Op Amp) (Note 8)				6			8		µV/°C
Offset Voltage Magnitude (Referred to "IN" Pin) ($V_{OS(IN)}$)	Gain = 1	●		3	15		3	18	mV
	Gain = 10	●		1.7	10		1.7	12	mV
DC Input Resistance (Note 9)	DC V_{IN} = 0V								
	Gain = 0			>100			>100		MΩ
	Gain = 1	●		10			10		kΩ
	Gain = 2	●		5			5		kΩ
	Gain = 5	●		2			2		kΩ
	Gain = 10, 20, 50, 100	●		1			1		kΩ

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications that apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_S = 5V, AGND = 2.5V, Gain = 1 (Digital Inputs 001), R_L = 10k to midsupply point, unless otherwise noted.

PARAMETER	CONDITIONS		LTC6910-1C/LTC6910-1I MIN	TYP	MAX	LTC6910-1H MIN	TYP	MAX	UNIT
Specifications for LTC6910-1 Only									
DC Small-Signal Output Resistance	Gain = 0			0.4			0.4		Ω
	Gain = 1			0.7			0.7		Ω
	Gain = 2			1			1		Ω
	Gain = 5			1.9			1.9		Ω
	Gain = 10			3.4			3.4		Ω
	Gain = 20			6.4			6.4		Ω
	Gain = 50			15			15		Ω
	Gain = 100			30			30		Ω
Gain-Bandwidth Product	Gain = 100, f_{IN} = 200kHz		8	11	14	8	11	14	MHz
		●	6	11	16	5	11	16	MHz
Wideband Noise (Referred to Input)	f = 1kHz to 200kHz								
	Gain = 0 Output Noise			3.8			3.8		μV_{RMS}
	Gain = 1			10.7			10.7		μV_{RMS}
	Gain = 2			7.3			7.3		μV_{RMS}
	Gain = 5			5.2			5.2		μV_{RMS}
	Gain = 10			4.5			4.5		μV_{RMS}
	Gain = 20			4.2			4.2		μV_{RMS}
	Gain = 50			3.9			3.9		μV_{RMS}
	Gain = 100			3.4			3.4		μV_{RMS}
Voltage Noise Density (Referred to Input)	f = 50kHz								
	Gain = 1			24			24		$nV/\sqrt{Hz}$
	Gain = 2			16			16		$nV/\sqrt{Hz}$
	Gain = 5			12			12		$nV/\sqrt{Hz}$
	Gain = 10			10			10		$nV/\sqrt{Hz}$
	Gain = 20			9.4			9.4		$nV/\sqrt{Hz}$
	Gain = 50			8.7			8.7		$nV/\sqrt{Hz}$
	Gain = 100			7.6			7.6		$nV/\sqrt{Hz}$
Total Harmonic Distortion	Gain = 10, f_{IN} = 10kHz, V_{OUT} = $1V_{RMS}$			–90			–90		dB
				0.003			0.003		%
	Gain = 10, f_{IN} = 100kHz, V_{OUT} = $1V_{RMS}$			–77			–77		dB
				0.014			0.014		%
AGND (Common Mode) Input Voltage Range (Note 10)	V_S = 2.7V	●	0.55		1.6	0.7		1.5	V
	V_S = 5V	●	0.7		3.65	1		3.25	V
	V_S = ±5V	●	–4.3		3.5	–4.3		3.35	V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications that apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_S = 5V, AGND = 2.5V, Gain = 1 (Digital Inputs 001), R_L = 10k to midsupply point, unless otherwise noted.

PARAMETER	CONDITIONS		LTC6910-2C/LTC6910-2I MIN	TYP	MAX	LTC6910-2H MIN	TYP	MAX	UNIT
Specifications for LTC6910-2 Only									
Voltage Gain (Note 7)	V_S = 2.7V, Gain = 1, R_L = 10k	●	–0.06	0	0.08	–0.07	0	0.08	dB
	V_S = 2.7V, Gain = 1, R_L = 500Ω	●	–0.1	–0.02	0.06	–0.11	–0.02	0.06	dB
	V_S = 2.7V, Gain = 2, R_L = 10k	●	5.96	6.02	6.1	5.95	6.02	6.1	dB
	V_S = 2.7V, Gain = 4, R_L = 10k	●	11.9	12.02	12.12	11.9	12.02	12.12	dB
	V_S = 2.7V, Gain = 8, R_L = 10k	●	17.8	17.98	18.15	17.8	17.98	18.15	dB
	V_S = 2.7V, Gain = 8, R_L = 500Ω	●	17.65	17.95	18.15	17.55	17.95	18.15	dB
	V_S = 2.7V, Gain = 16, R_L = 10k	●	23.75	24	24.2	23.75	24	24.2	dB
	V_S = 2.7V, Gain = 32, R_L = 10k	●	29.7	30	30.2	29.65	30	30.2	dB
	V_S = 2.7V, Gain = 64, R_L = 10k	●	35.3	35.75	36.2	35.2	35.75	36.2	dB
	V_S = 2.7V, Gain = 64, R_L = 500Ω	●	34.2	35.3	36.2	33.7	35.3	36.2	dB
	V_S = 5V, Gain = 1, R_L = 10k	●	–0.06	0	0.08	–0.06	0	0.08	dB
	V_S = 5V, Gain = 1, R_L = 500Ω	●	–0.1	–0.01	0.08	–0.11	–0.01	0.08	dB
	V_S = 5V, Gain = 2, R_L = 10k	●	5.96	6.02	6.1	5.96	6.02	6.1	dB
	V_S = 5V, Gain = 4, R_L = 10k	●	11.85	12.02	12.15	11.85	12.02	12.15	dB
	V_S = 5V, Gain = 8, R_L = 10k	●	17.85	18	18.15	17.85	18	18.15	dB
	V_S = 5V, Gain = 8, R_L = 500Ω	●	17.65	17.9	18.15	17.6	17.9	18.15	dB
	V_S = 5V, Gain = 16, R_L = 10k	●	23.85	24	24.15	23.78	24	24.15	dB
	V_S = 5V, Gain = 32, R_L = 10k	●	29.7	30	30.2	29.7	30	30.2	dB
	V_S = 5V, Gain = 64, R_L = 10k	●	35.6	35.9	36.2	35.5	35.9	36.2	dB
	V_S = 5V, Gain = 64, R_L = 500Ω	●	34.8	35.5	36	34.2	35.5	36	dB
	V_S = ±5V, Gain = 1, R_L = 10k	●	–0.05	0	0.07	–0.05	0	0.07	dB
	V_S = ±5V, Gain = 1, R_L = 500Ω	●	–0.1	–0.01	0.08	–0.1	–0.01	0.08	dB
	V_S = ±5V, Gain = 2, R_L = 10k	●	5.96	6.02	6.1	5.96	6.02	6.1	dB
	V_S = ±5V, Gain = 4, R_L = 10k	●	11.9	12.02	12.15	11.9	12.02	12.15	dB
	V_S = ±5V, Gain = 8, R_L = 10k	●	17.85	18	18.15	17.85	18	18.15	dB
	V_S = ±5V, Gain = 8, R_L = 500Ω	●	17.80	17.95	18.1	17.72	17.95	18.1	dB
	V_S = ±5V, Gain = 16, R_L = 10k	●	23.85	24	24.15	23.8	24	24.15	dB
	V_S = ±5V, Gain = 32, R_L = 10k	●	29.85	30	30.15	29.78	30	30.15	dB
	V_S = ±5V, Gain = 64, R_L = 10k	●	35.7	35.95	36.2	35.7	35.95	36.2	dB
	V_S = ±5V, Gain = 64, R_L = 500Ω	●	35.2	35.8	36.2	34.8	35.8	36.2	dB
Offset Voltage Magnitude (Internal Op Amp) ($V_{OS(OA)}$) (Note 8)		●		1.5	9		1.5	11	mV
Offset Voltage Drift (Internal Op Amp) (Note 8)		●		6			8		µV/°C
Offset Voltage Magnitude (Referred to "IN" Pin) ($V_{OS(IN)}$)	Gain = 1	●		3	15		3	17	mV
	Gain = 8	●		2	10		2	12	mV
DC Input Resistance (Note 9)	DC V_{IN} = 0V								
	Gain = 0			>100			>100		MΩ
	Gain = 1	●		10			10		kΩ
	Gain = 2	●		5			5		kΩ
	Gain = 4	●		2.5			2.5		kΩ
	Gain = 8, 16, 32, 64	●		1.25			1.25		kΩ

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications that apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_S = 5V, AGND = 2.5V, Gain = 1 (Digital Inputs 001), R_L = 10k to midsupply point, unless otherwise noted.

PARAMETER	CONDITIONS		LTC6910-2C/LTC6910-2I MIN	TYP	MAX	LTC6910-2H MIN	TYP	MAX	UNIT
Specifications for LTC6910-2 Only									
DC Small-Signal Output Resistance	Gain = 0			0.4			0.4		Ω
	Gain = 1			0.7			0.7		Ω
	Gain = 2			1			1		Ω
	Gain = 4			1.6			1.6		Ω
	Gain = 8			2.8			2.8		Ω
	Gain = 16			5			5		Ω
	Gain = 32			10			10		Ω
	Gain = 64			20			20		Ω
Gain-Bandwidth Product	Gain = 64, f_{IN} = 200kHz		9	13	16	9	13	16	MHz
		●	7	13	19	7	13	19	MHz
Wideband Noise (Referred to Input)	f = 1kHz to 200kHz								
	Gain = 0 Output Noise			3.8			3.8		μV_{RMS}
	Gain = 1			10.7			10.7		μV_{RMS}
	Gain = 2			7.3			7.3		μV_{RMS}
	Gain = 4			5.3			5.3		μV_{RMS}
	Gain = 8			4.6			4.6		μV_{RMS}
	Gain = 16			4.2			4.2		μV_{RMS}
	Gain = 32			4			4		μV_{RMS}
	Gain = 64			3.6			3.6		μV_{RMS}
Voltage Noise Density (Referred to Input)	f = 50kHz								
	Gain = 1			24			24		$nV/\sqrt{Hz}$
	Gain = 2			16			16		$nV/\sqrt{Hz}$
	Gain = 4			12			12		$nV/\sqrt{Hz}$
	Gain = 8			10.3			10.3		$nV/\sqrt{Hz}$
	Gain = 16			9.4			9.4		$nV/\sqrt{Hz}$
	Gain = 32			9			9		$nV/\sqrt{Hz}$
	Gain = 64			8.1			8.1		$nV/\sqrt{Hz}$
Total Harmonic Distortion	Gain = 8, f_{IN} = 10kHz, V_{OUT} = $1V_{RMS}$			–90			–90		dB
				0.003			0.003		%
	Gain = 8, f_{IN} = 100kHz, V_{OUT} = $1V_{RMS}$			–77			–77		dB
				0.014			0.014		%
AGND (Common Mode) Input Voltage Range (Note 10)	V_S = 2.7V	●	0.85		1.55	0.85		1.55	V
	V_S = 5V	●	0.7		3.6	0.7		3.6	V
	V_S = ±5V	●	–4.3		3.4	–4.3		3.4	V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications that apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_S = 5V, AGND = 2.5V, Gain = 1 (Digital Inputs 001), R_L = 10k to midsupply point, unless otherwise noted.

PARAMETER	CONDITIONS		LTC6910-3C/LTC6910-3I MIN	TYP	MAX	LTC6910-3H MIN	TYP	MAX	UNIT
Specifications for LTC6910-3 Only									
Voltage Gain (Note 7)	V_S = 2.7V, Gain = 1, R_L = 10k	●	−0.05	0	0.07	−0.05	0	0.09	dB
	V_S = 2.7V, Gain = 1, R_L = 500Ω	●	−0.1	−0.02	0.06	−0.11	−0.02	0.06	dB
	V_S = 2.7V, Gain = 2, R_L = 10k	●	5.93	6.02	6.08	5.93	6.02	6.09	dB
	V_S = 2.7V, Gain = 3, R_L = 10k	●	9.35	9.5	9.7	9.35	9.5	9.75	dB
	V_S = 2.7V, Gain = 4, R_L = 10k	●	11.9	11.98	12.2	11.9	11.98	12.2	dB
	V_S = 2.7V, Gain = 4, R_L = 500Ω	●	11.8	11.98	12.2	11.75	11.98	12.2	dB
	V_S = 2.7V, Gain = 5, R_L = 10k	●	13.85	13.92	14.05	13.8	13.92	14.05	dB
	V_S = 2.7V, Gain = 6, R_L = 10k	●	15.4	15.5	15.6	15.4	15.5	15.6	dB
	V_S = 2.7V, Gain = 7, R_L = 10k	●	16.7	16.85	17	16.7	16.85	17	dB
	V_S = 2.7V, Gain = 7, R_L = 500Ω	●	16.55	16.8	17	16.47	16.8	17	dB
	V_S = 5V, Gain = 1, R_L = 10k	●	−0.05	0	0.07	−0.05	0	0.07	dB
	V_S = 5V, Gain = 1, R_L = 500Ω	●	−0.1	−0.01	0.08	−0.1	−0.01	0.08	dB
	V_S = 5V, Gain = 2, R_L = 10k	●	5.96	6.02	6.08	5.96	6.02	6.08	dB
	V_S = 5V, Gain = 3, R_L = 10k	●	9.45	9.54	9.65	9.45	9.54	9.65	dB
	V_S = 5V, Gain = 4, R_L = 10k	●	11.85	12.02	12.15	11.85	12.02	12.15	dB
	V_S = 5V, Gain = 4, R_L = 500Ω	●	11.8	11.95	12.15	11.75	11.95	12.15	dB
	V_S = 5V, Gain = 5, R_L = 10k	●	13.8	13.95	14.05	13.8	13.95	14.05	dB
	V_S = 5V, Gain = 6, R_L = 10k	●	15.35	15.5	15.65	15.35	15.5	15.65	dB
	V_S = 5V, Gain = 7, R_L = 10k	●	16.7	16.85	17	16.7	16.85	17	dB
	V_S = 5V, Gain = 7, R_L = 500Ω	●	16.6	16.8	17	16.5	16.8	17	dB
	V_S = ±5V, Gain = 1, R_L = 10k	●	−0.06	0	0.07	−0.06	0	0.07	dB
	V_S = ±5V, Gain = 1, R_L = 500Ω	●	−0.1	−0.01	0.08	−0.12	−0.01	0.08	dB
	V_S = ±5V, Gain = 2, R_L = 10k	●	5.96	6.02	6.08	5.96	6.02	6.08	dB
	V_S = ±5V, Gain = 3, R_L = 10k	●	9.4	9.54	9.65	9.4	9.54	9.65	dB
	V_S = ±5V, Gain = 4, R_L = 10k	●	11.85	12	12.2	11.85	12	12.2	dB
	V_S = ±5V, Gain = 4, R_L = 500Ω	●	11.8	12	12.2	11.8	12	12.2	dB
	V_S = ±5V, Gain = 5, R_L = 10k	●	13.8	13.95	14.1	13.8	13.95	14.1	dB
	V_S = ±5V, Gain = 6, R_L = 10k	●	15.35	15.5	15.7	15.35	15.5	15.7	dB
	V_S = ±5V, Gain = 7, R_L = 10k	●	16.7	16.85	17.05	16.7	16.85	17.05	dB
	V_S = ±5V, Gain = 7, R_L = 500Ω	●	16.65	16.8	17	16.6	16.8	17	dB
Offset Voltage Magnitude (Internal Op Amp) ($V_{OS(OA)}$) (Note 8)		●		1.5	8		1.5	8	mV
Offset Voltage Drift (Internal Op Amp) (Note 8)		●		6			8		µV/°C
Offset Voltage Magnitude (Referred to "IN" Pin) ($V_{OS(IN)}$)	Gain = 1	●		3	15		3	15	mV
	Gain = 4	●		1.9	10		1.9	10	mV
DC Input Resistance (Note 9)	DC V_{IN} = 0V								
	Gain = 0			>100			>100		MΩ
	Gain = 1	●		10			10		kΩ
	Gain = 2	●		5			5		kΩ
	Gain = 3	●		3.3			3.3		kΩ
	Gain = 4	●		2.5			2.5		kΩ
	Gain = 5	●		2			2		kΩ
	Gain = 6	●		1.7			1.7		kΩ
	Gain = 7	●		1.4			1.4		kΩ

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications that apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_S = 5V, AGND = 2.5V, Gain = 1 (Digital Inputs 001), R_L = 10k to midsupply point, unless otherwise noted.

PARAMETER	CONDITIONS		LTC6910-3C/LTC6910-3I MIN	TYP	MAX	LTC6910-3H MIN	TYP	MAX	UNIT
Specifications for LTC6910-3 Only									
DC Small-Signal Output Resistance	Gain = 0			0.4			0.4		Ω
	Gain = 1			0.7			0.7		Ω
	Gain = 2			1			1		Ω
	Gain = 3			1.3			1.3		Ω
	Gain = 4			1.6			1.6		Ω
	Gain = 5			1.9			1.9		Ω
	Gain = 6			2.2			2.2		Ω
	Gain = 7			2.5			2.5		Ω
Gain-Bandwidth Product	Gain = 7, f_{IN} = 200kHz	●		11			11		MHz
Wideband Noise (Referred to Input)	f = 1kHz to 200kHz								
	Gain = 0 Output Noise			3.8			3.8		μV_{RMS}
	Gain = 1			10.7			10.7		μV_{RMS}
	Gain = 2			7.3			7.3		μV_{RMS}
	Gain = 3			6.1			6.1		μV_{RMS}
	Gain = 4			5.3			5.3		μV_{RMS}
	Gain = 5			5.2			5.2		μV_{RMS}
	Gain = 6			4.9			4.9		μV_{RMS}
	Gain = 7			4.7			4.7		μV_{RMS}
Voltage Noise Density (Referred to Input)	f = 50kHz								
	Gain = 1			24			24		$nV/\sqrt{Hz}$
	Gain = 2			16			16		$nV/\sqrt{Hz}$
	Gain = 3			14			14		$nV/\sqrt{Hz}$
	Gain = 4			12			12		$nV/\sqrt{Hz}$
	Gain = 5			11.6			11.6		$nV/\sqrt{Hz}$
	Gain = 6			11.2			11.2		$nV/\sqrt{Hz}$
	Gain = 7			10.5			10.5		$nV/\sqrt{Hz}$
Total Harmonic Distortion	Gain = 4, f_{IN} = 10kHz, V_{OUT} = $1V_{RMS}$			–90 0.003			–90 0.003		dB %
	Gain = 4, f_{IN} = 100kHz, V_{OUT} = $1V_{RMS}$			–80 0.01			–80 0.01		dB %
AGND (Common Mode) Input Voltage Range (Note 10)	V_S = 2.7V	●	0.85		1.55	0.85		1.55	V
	V_S = 5V	●	0.7		3.6	0.7		3.6	V
	V_S = ±5V	●	–4.3		3.4	–4.3		3.4	V

Note 1: Absolute Maximum Ratings are those values beyond which the life of the device may be impaired.

Note 2: The LTC6910-XC and LTC6910-XI are guaranteed functional over the operating temperature range of –40°C to 85°C. The LTC6910-XH are guaranteed functional over the operating temperature range of –40°C to 125°C.

Note 3: The LTC6910-XC are guaranteed to meet specified performance from 0°C to 70°C. The LTC6910-XC are designed, characterized and expected to meet specified performance from –40°C to 85°C but are not tested or QA sampled at these temperatures. LTC6910-XI are guaranteed to meet specified performance from –40°C to 85°C. The LTC6910-XH are guaranteed to meet specified performance from –40°C to 125°C.

Note 4: Operating all three logic inputs at 0.5V causes the supply current to increase typically 0.1mA from this specification.

Note 5: Output voltage swings are measured as differences between the output and the respective supply rail.

Note 6: Extended operation with output shorted may cause junction temperature to exceed the 150°C limit and is not recommended.

Note 7: Gain is measured with a DC large-signal test using an output excursion between approximately 30% and 70% of supply voltage.

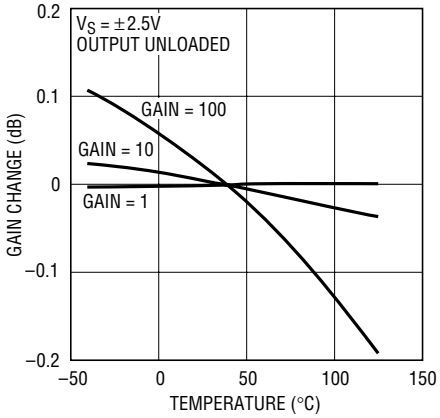
Note 8: Offset voltage referred to "IN" pin is (1 + 1/G) times offset voltage of the internal op amp, where G is nominal gain magnitude. See Applications Information.

Note 9: Input resistance can vary by approximately ±30% part-to-part at a given gain setting.

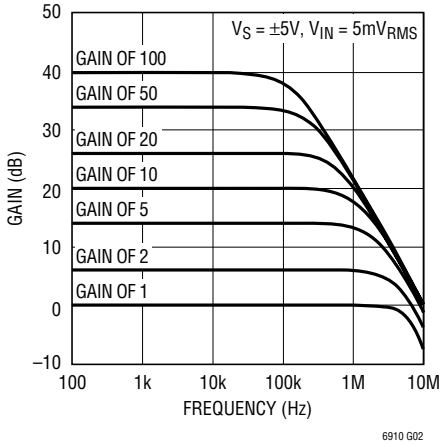
Note 10: At limits of AGND input range, open-loop gain of internal op amp may be greater than, or as much as 15dB below, its value at nominal AGND value.

TYPICAL PERFORMANCE CHARACTERISTICS (LTC6910-1)

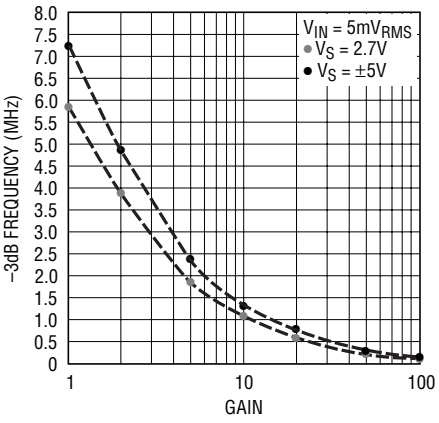
LTC6910-1 Gain Shift vs Temperature



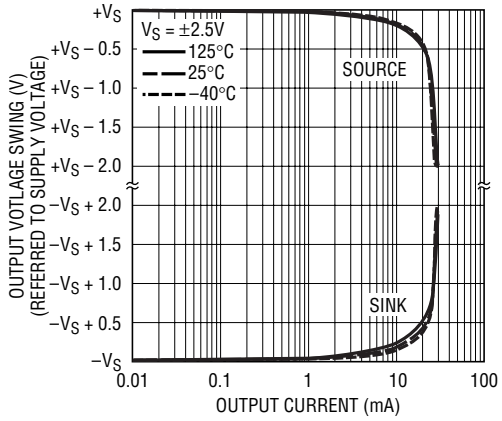
LTC6910-1 Frequency Response



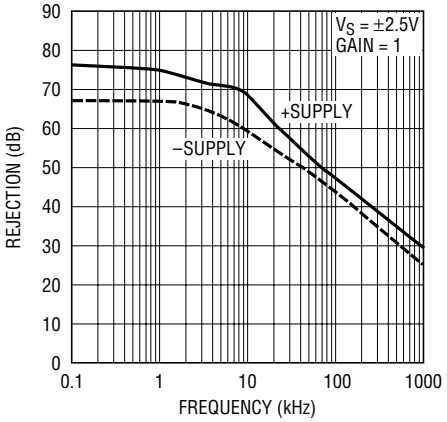
LTC6910-1 –3dB Bandwidth vs Gain Setting



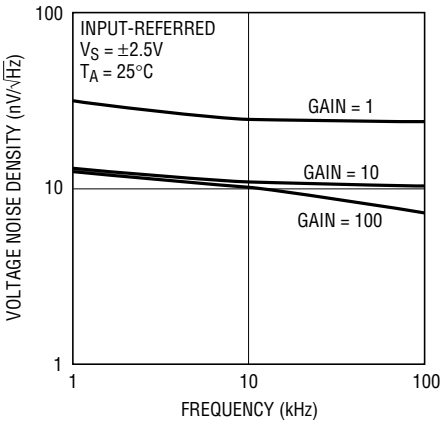
LTC6910-1 Output Voltage Swing vs Load Current



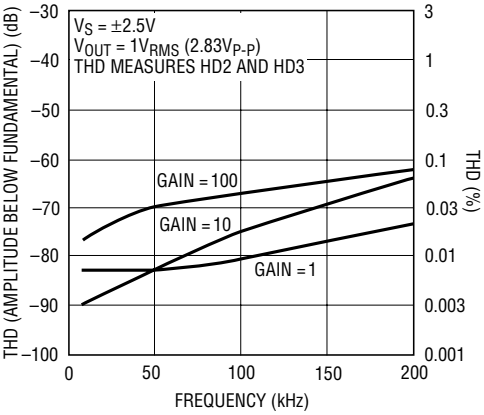
LTC6910-1 Power Supply Rejection vs Frequency



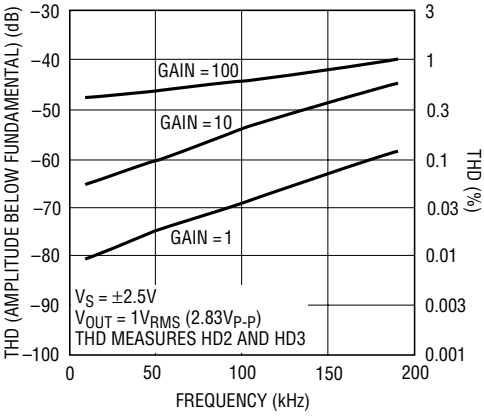
LTC6910-1 Noise Density vs Frequency



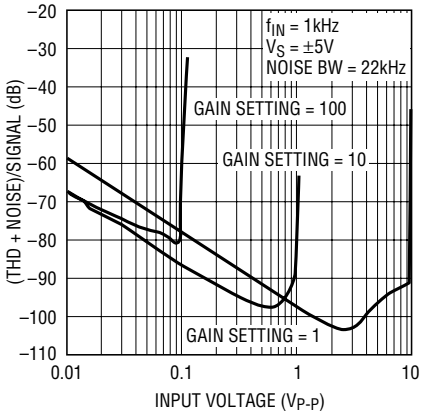
LTC6910-1 Distortion with Light Loading (R_L = 10k)



LTC6910-1 Distortion with Heavy Loading (R_L = 500Ω)

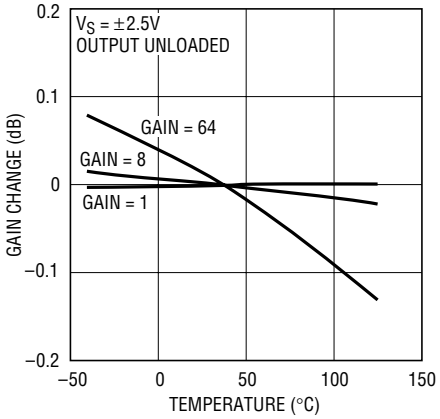


LTC6910-1 THD + Noise vs Input Voltage



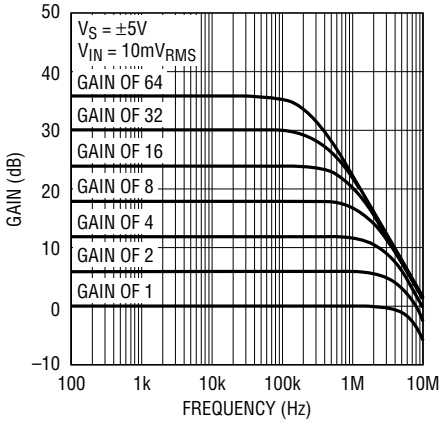
TYPICAL PERFORMANCE CHARACTERISTICS (LTC6910-2)

LTC6910-2 Gain Shift vs Temperature



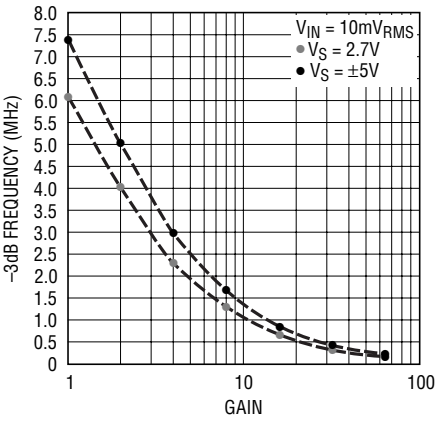
6910 G10

LTC6910-2 Frequency Response



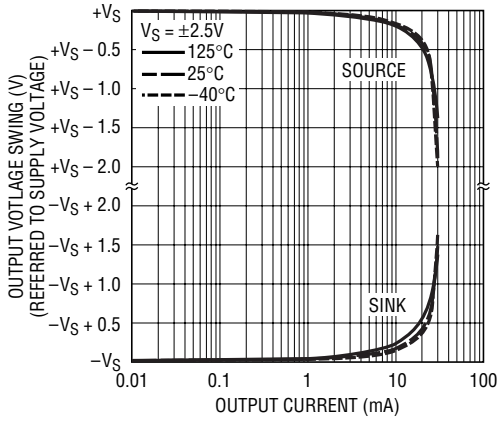
6910 G11

LTC6910-2 –3dB Bandwidth vs Gain Setting



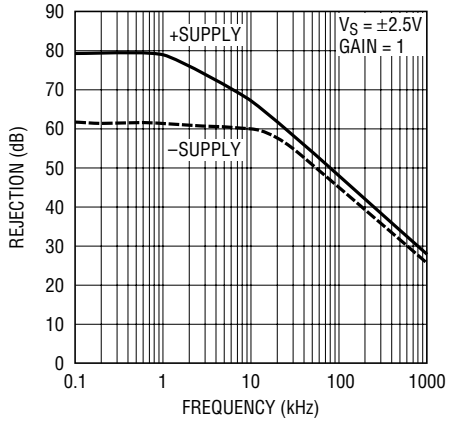
6910 G12

LTC6910-2 Output Voltage Swing vs Load Current



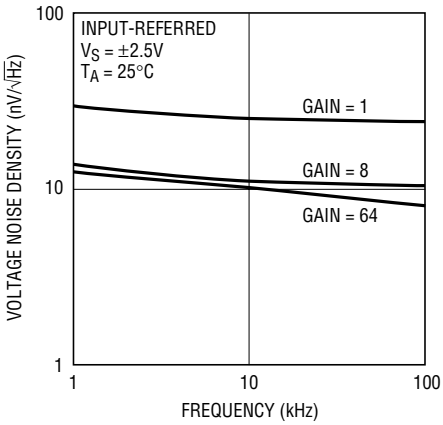
6910 G13

LTC6910-2 Power Supply Rejection vs Frequency



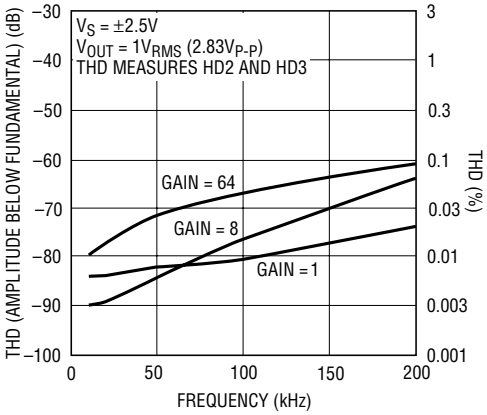
6910 G14

LTC6910-2 Noise Density vs Frequency



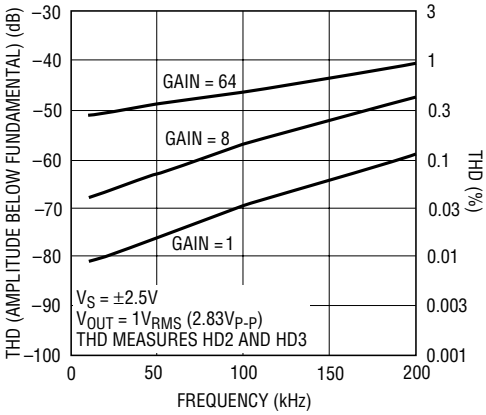
6910 G15

LTC6910-2 Distortion with Light Loading (R_L = 10k)



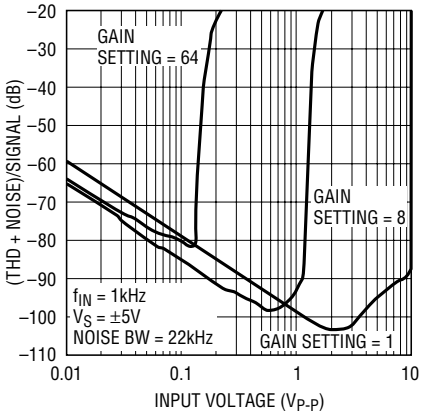
6910 G16

LTC6910-2 Distortion with Heavy Loading (R_L = 500Ω)



6910 G17

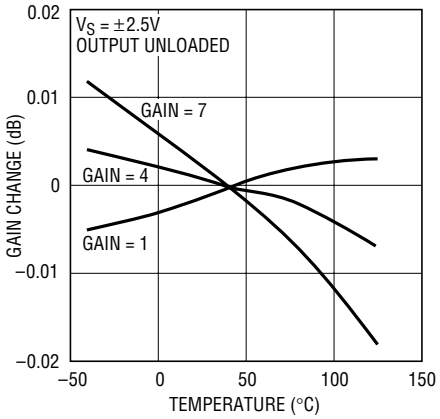
LTC6910-2 THD + Noise vs Input Voltage



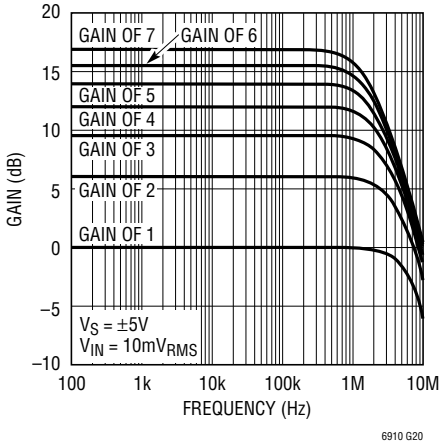
6910 G18

TYPICAL PERFORMANCE CHARACTERISTICS (LTC6910-3)

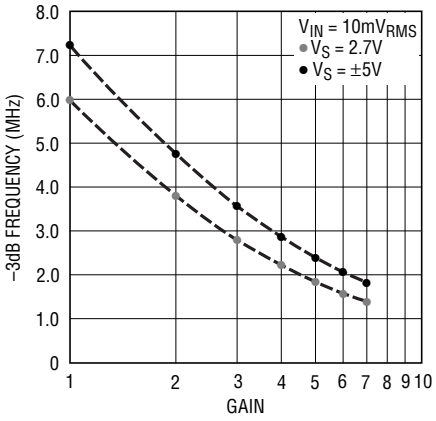
LTC6910-3 Gain Shift vs Temperature



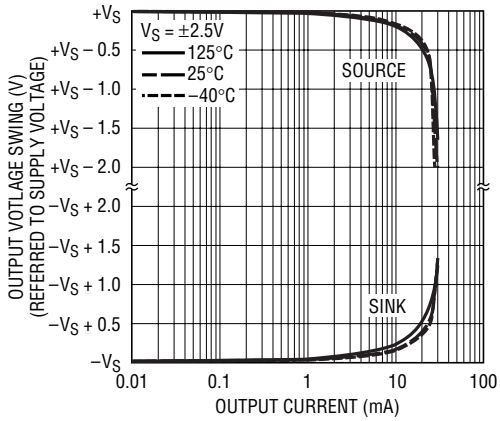
LTC6910-3 Frequency Response



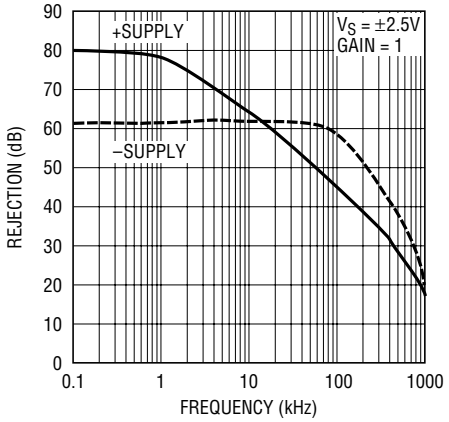
LTC6910-3 –3dB Bandwidth vs Gain Setting



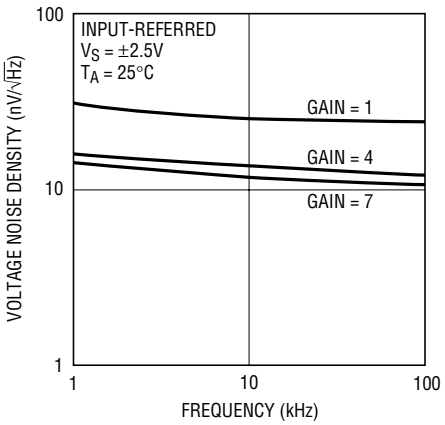
LTC6910-3 Output Voltage Swing vs Load Current



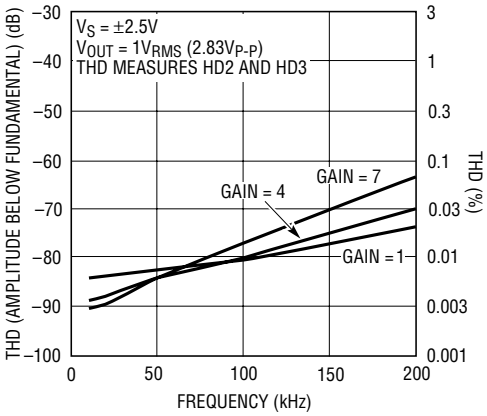
LTC6910-3 Power Supply Rejection vs Frequency



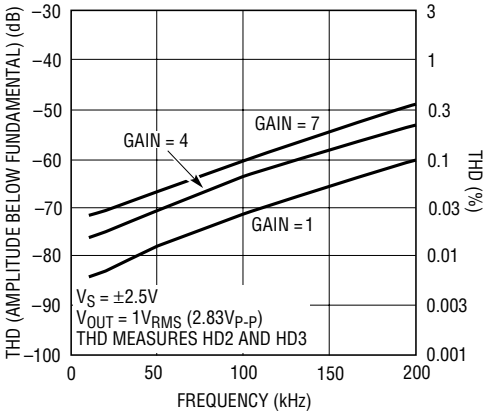
LTC6910-3 Noise Density vs Frequency



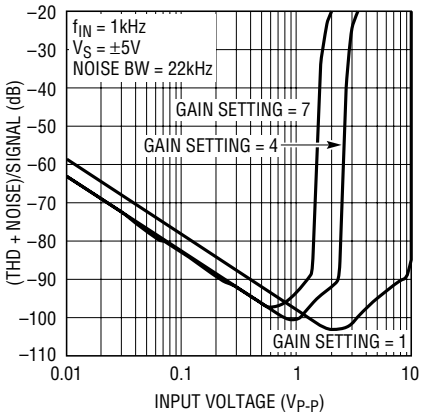
LTC6910-3 Distortion with Light Loading (R_L = 10k)



LTC6910-3 Distortion with Heavy Loading (R_L = 500Ω)



LTC6910-3 THD + Noise vs Input Voltage



PIN FUNCTIONS

OUT (Pin 1): Analog Output. This is the output of an internal operational amplifier and swings to near the power supply rails (V^+ and $V^–$) as specified in the Electrical Characteristics table. The internal op amp remains active at all times, including the zero gain setting (digital input 000). As with other amplifier circuits, loading the output as lightly as possible will minimize signal distortion and gain error. The Electrical Characteristics table shows performance at output currents up to 10mA and current limits that occur when the output is shorted to midsupply at 2.7V and ±5V supplies. Signal outputs above 10mA are possible but current-limiting circuitry will begin to affect amplifier performance at approximately 20mA. Long-term operation above 20mA output is not recommended. Do not exceed maximum junction temperature of 150°C. The output will drive capacitive loads up to 50pF. Capacitances higher than 50pF should be isolated by a series resistor to preserve AC stability.

AGND (Pin 2): Analog Ground. The AGND pin is at the midpoint of an internal resistive voltage divider, developing a potential halfway between the V^+ and $V^–$ pins, with an equivalent series resistance to the pin of nominally 5kΩ (Figure 4). AGND is also the noninverting input of the internal op amp, which makes it the ground reference voltage for the IN and OUT pins. Because of this, very "clean" grounding is important, including an analog ground plane surrounding the package.

Recommended analog ground plane connection depends on how power is applied to the LTC6910-X (Figures 1, 2, and 3). Single power supply applications typically use $V^–$ for the system signal ground. The analog ground plane in single-supply applications should therefore tie to $V^–$, and the AGND pin should be bypassed to this ground plane by a high quality capacitor of at least 1µF (Figure 1). The AGND pin then provides an internal analog reference voltage at half the supply voltage (with internal resistance of approximately 5kΩ) which is the center of the swing range for both input and output. Dual supply applications with symmetrical supplies (such as ±5V) have a natural system ground at zero volts, which can drive the analog ground plane; AGND then connects directly to the ground plane, making zero volts the input and output reference voltage for the LTC6910-X (Figure 2). Finally, if a dual power supply is asymmetrical, the supply ground is still the natural ground plane voltage. To maximize signal swing capability with an asymmetrical supply, however, it is often desirable to refer the LTC6910-X's analog input and output to a voltage equidistant from the two supply rails V^+ and $V^–$. The AGND pin will provide such a potential when open-circuited and bypassed with a capacitor (Figure 3), just as with a single power supply, but now the ground plane connection is different and the LTC6910-X's V^+ and $V^–$ pins are both isolated from this ground plane.

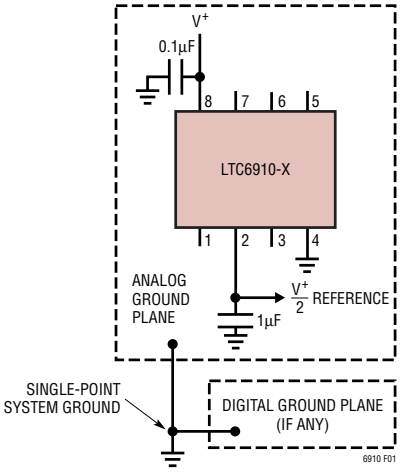


Figure 1. Single Supply Ground Plane Connection

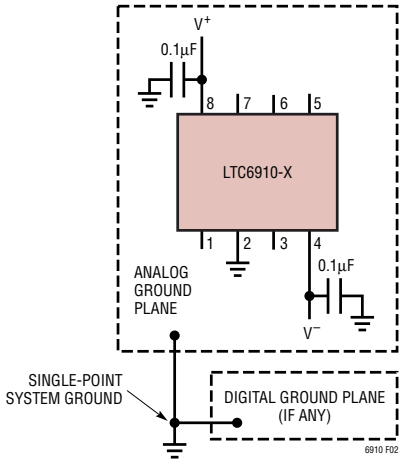


Figure 2. Symmetrical Dual Supply Ground Plane Connection

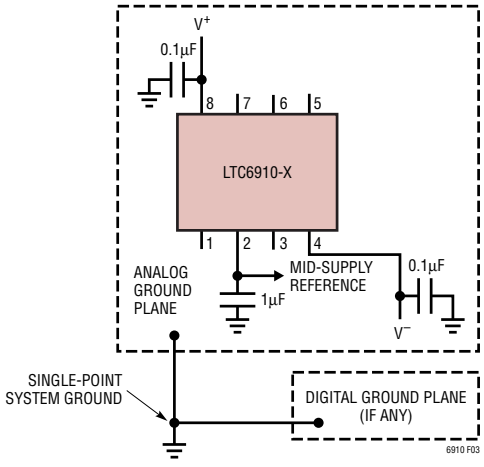


Figure 3. Asymmetrical Dual Supply Ground Plane Connection

PIN FUNCTIONS

Where AGND does not connect to a ground plane, as in Figures 1 and 3, it is important to AC-bypass the AGND pin. This is especially true when AGND is used as a reference voltage for other circuitry. Also, without a bypass capacitor, wideband noise will enter the signal path from the internal voltage divider resistors that set the DC voltage on AGND. This noise can reduce SNR by 3dB at high gain settings. The resistors present a Thévenin equivalent of approximately 5k to the AGND pin. An external capacitor from AGND to the ground plane, whose impedance is well below 5k at frequencies of interest, will suppress this noise. A 1µF high quality capacitor is effective in suppressing resistor noise for frequencies down to 1kHz. Larger capacitors extend this suppression to proportionately lower frequencies. This issue does not arise in symmetrical dual supply applications (Figure 2) because AGND goes directly to ground.

In applications requiring an analog ground reference other than halfway between the supply rails, the user can override the built-in analog ground reference by tying the AGND pin to a reference voltage within the AGND voltage range specified in the Electrical Characteristics table. The AGND pin will load the external reference with approximately 5k returned to the mid-supply potential. AGND should still be capacitively bypassed to a ground plane as noted above. Do not connect the AGND pin to the V^- pin.

IN (Pin 3): Analog Input. The input signal to the amplifier in the LTC6910-X is the voltage difference between the IN and AGND pins. The IN pin connects internally to a digitally controlled resistance whose other end is a current summing point at the same potential as the AGND pin (Figure 4). At unity gain (digital input 001), the value of this input resistance is approximately 10kΩ and the IN voltage range is rail-to-rail (V^+ to V^-). At gain settings above unity (digital input 010 or higher), the input resistance falls. Also, the linear input voltage range falls in inverse proportion to gain. (The higher gains are designed to boost lower level signals with good noise performance.) Tables 1, 2, and 3 summarize this behavior. In the "zero" gain state (digital input 000), analog switches disconnect the IN pin internally and this pin presents a very high input resistance. The input may vary from rail to rail in the "zero" gain setting but the output is insensitive to it and remains at the AGND potential. Circuitry driving the IN pin must consider the LTC6910-X's input resistance and the variation of this resistance when used at multiple gain settings. Signal sources with significant output resistance may introduce a gain error as the source's output resistance and the LTC6910-X's input resistance form a voltage divider. This is especially true at the higher gain settings where the input resistance is lowest.

In single supply voltage applications at elevated gain settings (digital input 010 or higher), it is important to remember that the LTC6910-X's DC ground reference for both input and output is AGND, not V^-. With increasing gains, the LTC6910-X's input voltage range for unclipped output is no longer rail-to-rail but shrinks toward AGND. The OUT pin also swings positive or negative with respect to AGND. At unity gain (digital input 001), both IN and OUT voltages can swing from rail to rail (Tables 1, 2, 3).

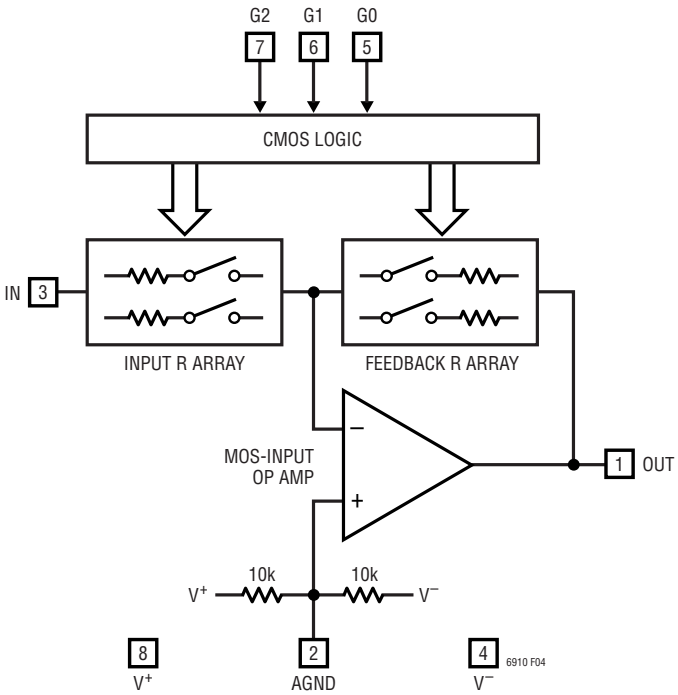


Figure 4. Block Diagram

PIN FUNCTIONS

V^-, V^+ (Pins 4, 8): Power Supply Pins. The V^+ and V^- pins should be bypassed with 0.1µF capacitors to an adequate analog ground plane using the shortest possible wiring. Electrically clean supplies and a low impedance ground are important for the high dynamic range available from the LTC6910-X (see further details under AGND). Low noise linear power supplies are recommended. Switching power supplies require special care to prevent switching noise coupling into the signal path, reducing dynamic range.

G0, G1, G2 (Pins 5, 6, 7): CMOS-Level Digital Gain-Control Inputs. G2 is the most significant bit (MSB). These pins control the voltage gain from IN to OUT pins (see Table 1, Table 2 and Table 3). Digital input code 000 causes a "zero" gain with very low output noise. In this "zero" gain state the IN pin is disconnected internally, but the OUT pin remains active and forced by the internal op amp to the voltage present on the AGND pin. Note that the voltage gain from IN to OUT is inverting: OUT and IN pins always swing on opposite sides of the AGND potential. The G pins are high impedance CMOS logic inputs and must be connected (they will float to unpredictable voltages if open circuited). No speed limitation is associated with the digital logic because it is memoryless and much faster than the analog signal path.

APPLICATIONS INFORMATION

Functional Description

The LTC6910 family are small outline, wideband inverting DC amplifiers whose voltage gain is digitally programmable. Each delivers a choice of eight voltage gains, controlled by the 3-bit digital inputs to the G pins, which accept CMOS logic levels. The gain code is always monotonic; an increase in the 3-bit binary number (G2 G1 G0) causes an increase in the gain. Table 1, Table 2 and Table 3 list the nominal voltage gains for LTC6910-1, LTC6910-2 and LTC6910-3 respectively. Gain control within each amplifier occurs by switching resistors from a matched array in or out of a closed-loop op amp circuit using MOS analog switches (Figure 4). Bandwidth depends on gain setting. Curves in the Typical Performance Characteristics section show measured frequency responses.

Digital Control

Logic levels for the LTC6910-X digital gain control inputs (Pins 5, 6, 7) are nominally rail-to-rail CMOS. Logic 1 is V^+, logic 0 is V^- or alternatively 0V when using ±5V supplies. The part is tested with the values listed in the Electrical Characteristics table (Digital Input "High" and "Low" Voltages), which are 10% and 90% of full excursion on the inputs. That is, the tested logic levels are 0.27V and 2.43V with a 2.7V supply, 0.5V and 4.5V levels with 0V and 5V supply rails, and 0.5V and 4.5V logic levels at ±5V supplies. Do not attempt to drive the digital inputs with TTL logic levels (such as HCT or LS logic), which normally do not swing near +5V. TTL sources should be adapted with CMOS drivers or suitable pull-up resistors to 5V so that they will swing to the positive rail.

Timing Constraints

Settling time in the CMOS gain-control logic is typically several nanoseconds and faster than the analog signal path. When amplifier gain changes, the limiting timing is analog, not digital, because the effects of digital input changes are observed only through the analog output (Figure 4). The LTC6910-X's logic is static (not latched) and therefore lacks bus timing requirements. However, as with any programmable-gain amplifier, each gain change causes an output transient as the amplifier's output moves, with finite speed, toward a differently scaled version of the input signal. Varying the gain faster than the output can settle produces a garbled output signal. The LTC6910-X analog path settles with a characteristic time constant or time scale, τ, that is roughly the standard value for a first order band limited response:

$$\tau = 1 / (2 \pi f_{-3dB}),$$

where f_{-3dB} is the –3dB bandwidth of the amplifier. For example, when the upper –3dB frequency is 1MHz, τ is about 160ns. The bandwidth, and therefore τ, varies with gain (see Frequency Response and –3dB Bandwidth curves in Typical Performance Characteristics). After a gain change it is the *new* gain value that determines the settling time constant. Exact settling timing depends on the gain change, the input signal and the possibility of slew limiting at the output. However as a basic guideline, the range of τ is 20ns to 1400ns for the LTC6910-1, 20ns to 900ns for the LTC6910-2 and 20ns to 120ns for the LTC6910-3. These numbers correspond to the ranges of –3dB Bandwidth in the plots of that title under Typical Performance Characteristics.

Offset Voltage vs Gain Setting

The electrical tables list DC offset (error) voltage at the inputs of the internal op-amp in Figure 4, $V_{OS(OA)}$, which is the source of DC offsets in the LTC6910-X. The tables also show the resulting, gain dependent offset voltage referred to the IN pin, $V_{OS(IN)}$. These two measures are related through the feedback/input resistor ratio, which equals the nominal gain-magnitude setting, G:

$$V_{OS(IN)} = (1 + 1/G)\, V_{OS(OA)}$$

Offset voltages at any gain setting can be inferred from this relationship. For example, an internal offset $V_{OS(OA)}$ of 1mV will appear referred to the IN pin as 2mV at a gain setting G of 1, or 1.5mV at a gain setting of 2. At high gains, $V_{OS(IN)}$ approaches $V_{OS(OA)}$. (Offset voltage can be of either polarity; it is a statistical parameter centered on zero.) The MOS input circuitry of the internal op amp in Figure 4 draws negligible input currents (unlike some op amps), so only $V_{OS(OA)}$ and G affect the overall amplifier's offset.

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Offset Nulling and Drift

Because internal op amp offset voltage $V_{OS(OA)}$ is gain independent as noted above, offset trimming can be readily added at the AGND pin, which drives the noninverting input of the internal op amp. Such a trim shifts the AGND voltage slightly from the system's analog ground reference, where AGND would otherwise connect directly. This is convenient when a low resistance analog ground potential or analog ground reference exists, for the return of a voltage divider as in Figure 5a. When adjusted for zero DC output voltage when the LTC6910-X has zero DC input voltage, this DC nulling will hold at other gain settings also.

Figure 5a shows the basic arrangement for dual-supply applications. A voltage divider (R1 and R2) scales external reference voltages $+V_{REF}$ and $-V_{REF}$ to a range equaling or slightly exceeding the approximately ±10mV op amp offset-voltage range. Resistor R1 is chosen to drop the ±10mV maximum trim voltage when the potentiometer is set to either end. Thus if V_{REF} is 5V, R1 should be about 100Ω. Note also that the two internal 10k resistors in Figure 4 tend to bias AGND toward the mid-point of V^+ and V^-. The external voltage divider will swamp this effect if R1 is much less than 5kΩ. When considering the effect of the internal 10k resistors, note that they form a Thévenin equivalent of 5k in series with an open-circuit voltage at the halfway potential $(V^+ + V^-)/2$. (Although tightly matched, these internal 10k resistors also have an absolute tolerance of up to ±30% and a temperature coefficient of typically –30ppm/°C.) Also, as described under Pin Functions for AGND, a bypass capacitor C1 is always advisable when AGND is not connected directly to a ground plane.

With this trim technique in place, the remaining DC offset sources are drifts with temperature (typically 6μV/°C referred to $V_{OS(OA)}$), shifts in the LTC6910-X's supply voltage divided by the PSRR factors, supply voltage shifts coupling through the two 10k internal resistors of Figure 4, and of course any shifts in the reference voltages that supply $+V_{REF}$ and $-V_{REF}$ in Figure 5a.

Figure 5b illustrates how to make an offset voltage adjustment relative to the mid-supply potential in single supply applications. Resistor values shown provide at least a ±10mV adjustment range assuming the minimum values for the internal resistors at pin 2 and a supply potential of 5V. For single supply systems where all circuitry is DC referenced to some other fixed bias potential, an offset adjustment scheme is shown in Figure 5c. A low value for R1 overrides the internal resistors at pin 2 and applies the system DC bias to the LTC6910. Actual values for the adjustment components depend on the magnitude of the DC bias voltage. Offset adjustment component values shown are an example with a single 5V V_{CC} supply and a 1.25V system DC reference voltage.

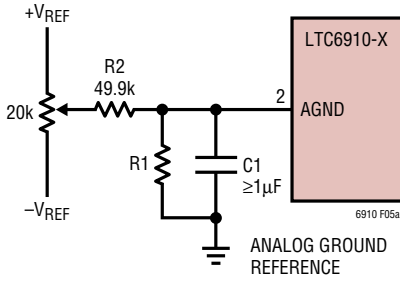


Figure 5a. Offset Nulling (Dual Supplies)

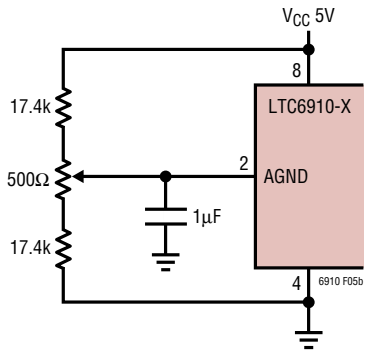


Figure 5b. Offset Nulling (Single Supply, Half Supply Reference)

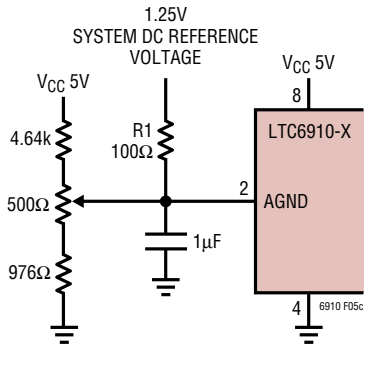


Figure 5c. Offset Nulling (Single Supply, External Reference)

APPLICATIONS INFORMATION

Analog Input and DC Levels

As described in Tables 1, 2 and 3 and under Pin Functions, the IN pin presents a variable input resistance returned internally to a potential equal to that at the AGND pin (within a small offset-voltage error). This input resistance varies with digital gain setting, becoming infinite (open circuit) at "zero" gain (digital input 000), and as low as 1kΩ at high gain settings. It is important to allow for this input-resistance variation with gain, when driving the LTC6910-X from other circuitry. Also, as the gain increases above unity, the DC linear input-voltage range (corresponding to rail-to-rail swing at the OUT pin) shrinks toward the AGND potential. The output swings positive or negative around the AGND potential (in the opposite direction from the input, because the gain is inverting).

AC-Coupled Operation

Adding a capacitor in series with the IN pin makes the LTC6910-X into an AC-coupled amplifier, suppressing the source's DC level (and even minimizing the offset voltage from the LTC6910-X itself). No further components are required because the input of the LTC6910-X biases itself correctly when a series capacitor is added. The IN pin connects to an internal variable resistor (and floats when DC open-circuited to a well defined voltage equal to the AGND input voltage at nonzero gain settings). The value of this internal input resistor varies with gain setting over a total range of about 1k to 10k, depending on version (the rightmost columns of Table 1, Table 2 and Table 3). Therefore, with a series input capacitor the low frequency cutoff will also vary with gain. For example, for a low frequency corner of 1kHz or lower, use a series capacitor of 0.16µF or larger. A 0.16µF capacitor has a reactance of 1kΩ at 1kHz, giving a 1kHz lower –3dB frequency for gain settings of 10V/V through 100V/V in the LTC6910-1. If the LTC6910-1 is operated at lower gain settings with an 0.16µF input capacitor, the higher input resistance will reduce the lower corner frequency down to 100Hz at a gain setting of 1V/V. These frequencies scale inversely with the value of the input capacitor.

Note that operating the LTC6910-X in zero gain mode (digital inputs 000) open circuits the IN pin and this demands some care if employed with a series input capacitor. When the chip enters the zero gain mode, the opened IN pin tends to freeze the voltage across the capacitor to the value it held just before the zero gain state. This can place the IN pin at or near the DC potential of a supply rail (the IN pin may also drift to a supply potential in this state due to small junction leakage currents). To prevent driving the IN pin outside the supply limit and potentially damaging the chip, avoid AC input signals in the zero gain state with a series capacitor. Also, switching later to a nonzero gain value will cause a transient pulse at the output of the LTC6910-X (with a time constant set by the capacitor value and the new LTC6910-X input resistance value). This occurs because the IN pin returns to the AGND potential and transient current flows to charge the capacitor to a new DC drop.

SNR and Dynamic Range

The term "dynamic range" is much used (and abused) with signal paths. Signal-to-noise ratio (SNR) is an unambiguous comparison of signal and noise levels, measured in the same way and under the same operating conditions. In a variable gain amplifier, however, further characterization is useful because both noise and maximum signal level in the amplifier will vary with the gain setting, in general. In the LTC6910-X, maximum output signal is independent of gain (and is near the full power supply voltage, as detailed in the Swing sections of the Electrical Characteristics table). The maximum input level falls with increasing gain, and the input-referred noise falls as well (as listed also in the table). To summarize the useful signal range in such an amplifier, we define Dynamic Range (DR) as the ratio of maximum input (at unity gain) to minimum input-referred noise (at maximum gain). (These two numbers are measured commensurately, in RMS Volts. For deterministic signals such as sinusoids, $1V_{RMS}$ = $2.828V_{P-P}$.) This DR has a physical interpretation as the range of signal levels that will experience an SNR above unity V/V or 0dB. At a 10V total power supply, DR in the LTC6910-1 (gains 0V to 100V/V) is typically 120dB (the ratio of a nominal $9.9V_{P-P}$, or $3.5V_{RMS}$, maximum input to the $3.4\mu V_{RMS}$ high gain input noise). The corresponding DR for the LTC6910-2 (gains 0V to 64V) is also 120dB; for

TYPICAL APPLICATIONS

the LTC6910-3 (gains 0V to 7V/V) it is 117dB. The SNR from an amplifier is the ratio of input level to input-referred noise, and can be 110dB with the LTC6910 family at unity gain.

Construction and Instrumentation Cautions

Electrically clean construction is important in applications seeking the full dynamic range of the LTC6910-X amplifier. Short, direct wiring will minimize parasitic capacitance and inductance. High quality supply bypass capacitors of 0.1µF near the chip provide good decoupling from a clean, low inductance power source. But several cm of wire (i.e., a few microhenrys of inductance) from the power supplies, unless decoupled by substantial capacitance (≥10µF) near the chip, can cause a high-Q LC resonance in the hundreds of kHz in the chip's supplies or ground reference. This may impair circuit performance at those frequencies. A compact, carefully laid out printed circuit board with a good ground plane makes a significant difference in minimizing distortion. Finally, equipment to measure amplifier performance can itself introduce distortion or noise floors. Checking for these limits with a wire replacing the chip is a prudent routine procedure.

Expanding an ADC's Dynamic Range

Figure 6 shows a compact data acquisition system for wide ranging input levels. This figure combines an LTC6910-X programmable amplifier (8-lead TSOT-23) with an LTC1864 analog-to-digital converter (ADC) in an 8-lead MSOP. This ADC has 16-bit resolution and a maximum sampling rate of 250ksps. An LTC6910-1, for example, expands the ADC's input amplitude range by 40dB while operating from the same single 5V supply. The 499Ω resistor and 270pF capacitor couple cleanly between the LTC6910-X's output and the switched-capacitor input of the LTC1864. The 270pF capacitor should be an NPO or X7R type, and lead length and inductance in the connections to the LTC1864 inputs must be minimized, to achieve the full performance capability of this circuit. (See LTC 1864 data sheet for further general information.)

At a gain setting of 10V/V in an LTC6910-1 (digital input 100) and a 250ksps sampling rate in the LTC1864, a 10kHz input signal at 60% of full scale shows a THD of –87dB at the digital output of the ADC. 100kHz input signals under the same conditions produce THD values around –75dB. Noise effects (both random and quantization) in the ADC are divided by the gain of the amplifier when referred to V_{IN} in Figure 4. Because of this, the circuit can acquire a signal that is 40dB down from full scale of $5V_{P-P}$ with an SNR of over 70dB. Such performance from an ADC alone (70 + 40 = 110dB of useful dynamic range at 250ksps), if available, would be far more expensive.

Low Noise AC Amplifier with Programmable Gain and Bandwidth

Analog data acquisition can exploit band limiting as well as gain to suppress unwanted signals or noise. Tailoring an analog front end to both the level and bandwidth of each source maximizes the resulting SNR.

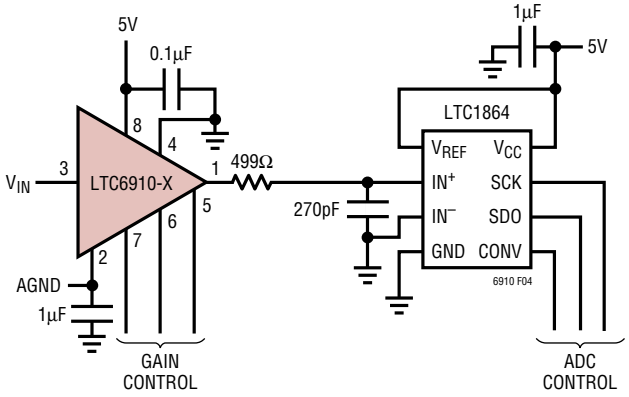


Figure 6. Expanding an ADC's Dynamic Range

TYPICAL APPLICATION

Figure 7 shows a block diagram and Figure 8 the practical circuit for a low noise amplifier with gain and bandwidth independently programmable over 100:1 ranges. One LTC6910-X controls the gain and another controls the bandwidth. An LT1884 dual op amp forms an integrating lowpass loop with capacitor C2 to set the programmable upper corner frequency. The LT1884 also supports rail-to-rail output swings over the total supply voltage range of 2.7V to 10.5V. AC coupling through capacitor C1 establishes a fixed low frequency corner of 1Hz, which can be adjusted by changing C1. Alternatively, shorting C1 makes the amplifier DC coupled. (If DC gain is not needed, however, the AC coupling suppresses several error sources: any shifts in DC levels, low frequency noise and all amplifier DC offset voltages other than the low internally trimmed LT1884 offset in the integrating amplifier. If desired, another coupling capacitor in series with the input can relax the requirements on DC input level as well.)

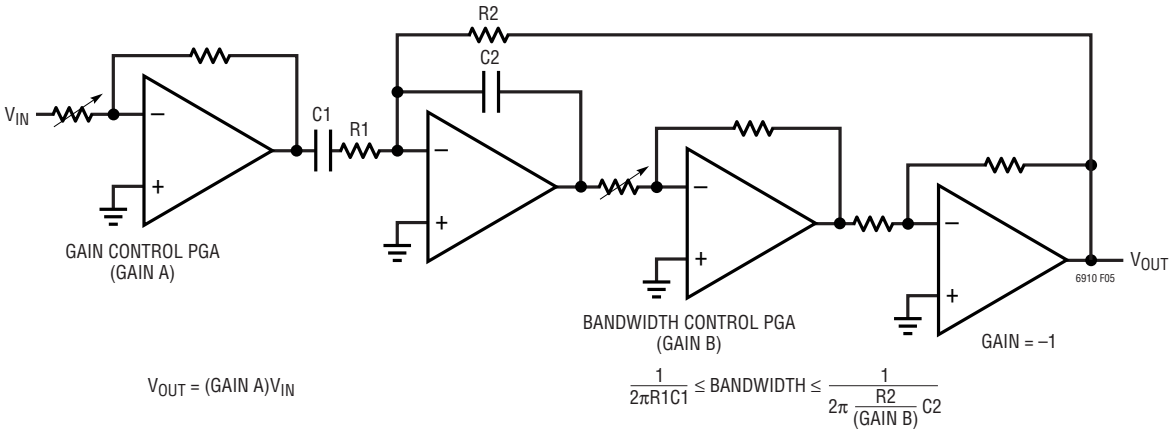
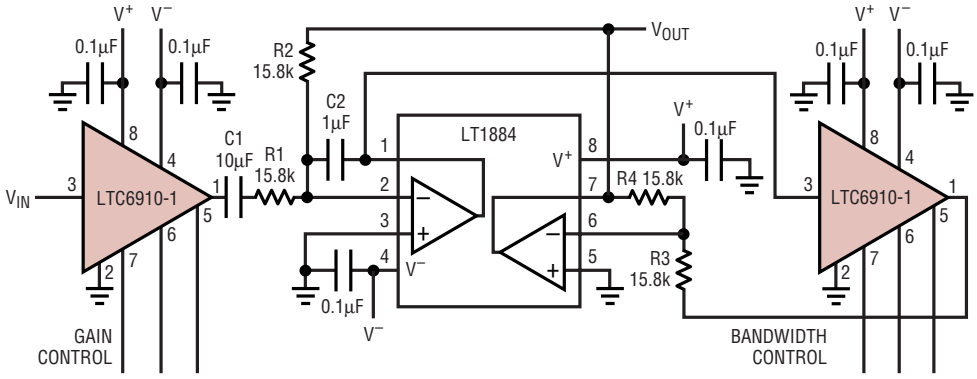


Figure 7. Block Diagram of an AC Amplifier with Programmable Gain and Bandwidth

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Measured frequency responses in Figure 8 with LTC6910-1 PGAs demonstrate bandwidth settings of 10Hz, 100Hz and 1kHz, with digital codes at the BW inputs of respectively 001, 100 and 111, and unity gain in each case. By scaling C2, this circuit can serve other bandwidths, such as a maximum of 10kHz with 0.1µF using LT1884 (gain-bandwidth product around 1MHz). Noise floor from internal sources yields an output SNR of 76dB with 10mV$_{P-P}$ input, gain of 100 and 100Hz bandwidth; for 100mV$_{P-P}$ input, gain of 10 and 1000Hz bandwidth it is 64dB.



Gain vs Frequency

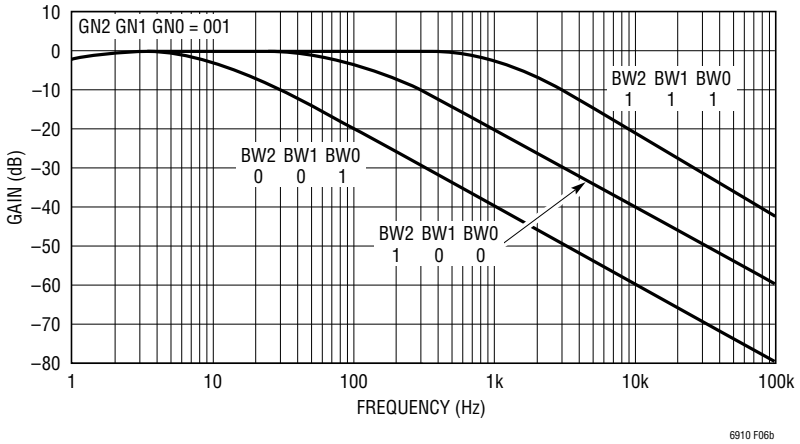
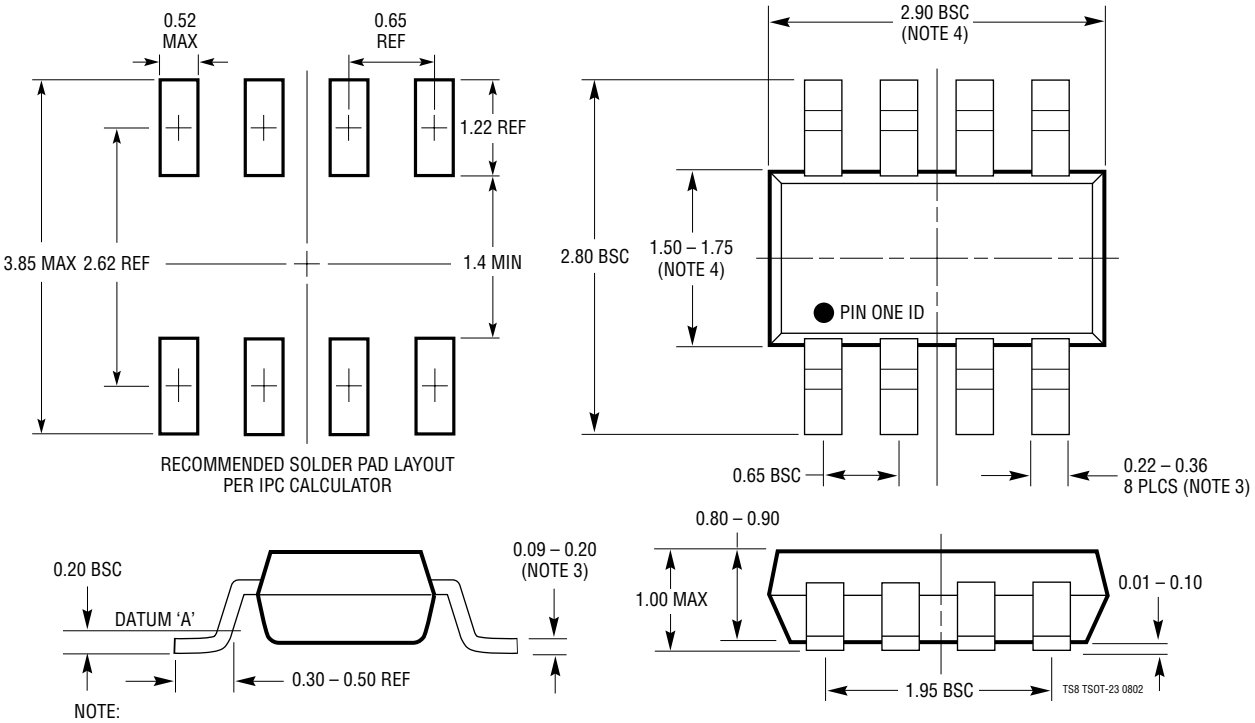


Figure 8. Low Noise AC Amplifier with Programmable Gain and Bandwidth

PACKAGE DESCRIPTION

TS8 Package
8-Lead Plastic TSOT-23
(Reference LTC DWG # 05-08-1637)



NOTE:
1. DIMENSIONS ARE IN MILLIMETERS
2. DRAWING NOT TO SCALE
3. DIMENSIONS ARE INCLUSIVE OF PLATING
4. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH AND METAL BURR
5. MOLD FLASH SHALL NOT EXCEED 0.254mm
6. JEDEC PACKAGE REFERENCE IS MO-193

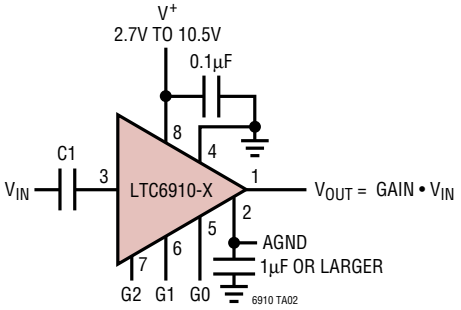
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TYPICAL APPLICATION

AC-Coupled Single Supply Amplifiers

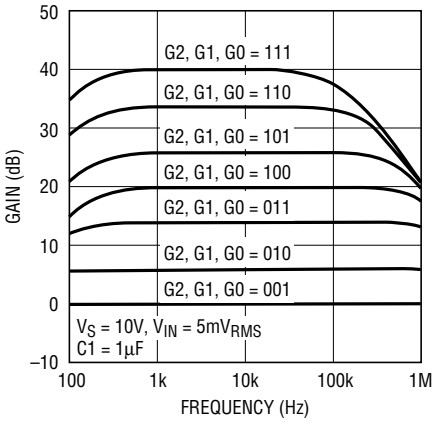
DIGITAL INPUTS G2	G1	G0	LTC6910-1 PASSBAND GAIN	LTC6910-1 LOWER –3dB FREQ (C1 = 1µF)	LTC6910-2 PASSBAND GAIN	LTC6910-2 LOWER –3dB FREQ (C1 = 1µF)	LTC6910-3 PASSBAND GAIN	LTC6910-3 LOWER –3dB FREQ (C1 = 1µF)
0	0	0	0	—	0	—	0	—
0	0	1	–1	16Hz	–1	16Hz	–1	16Hz
0	1	0	–2	32Hz	–2	32Hz	–2	32Hz
0	1	1	–5	80Hz	–4	64Hz	–3	48Hz
1	0	0	–10	160Hz	–8	127Hz	–4	64Hz
1	0	1	–20	160Hz	–16	127Hz	–5	80Hz
1	1	0	–50	160Hz	–32	127Hz	–6	95Hz
1	1	1	–100	160Hz	–64	127Hz	–7	111Hz

C1 VALUE SETS LOWER CORNER FREQUENCY. THE TABLE SHOWS THIS FREQUENCY WITH C1 = 1µF. THIS FREQUENCY SCALES INVERSELY WITH C1

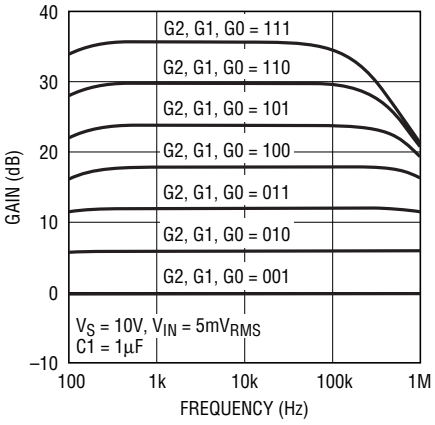


PIN 2 (AGND) SETS DC OUTPUT VOLTAGE AND HAS BUILT-IN HALF-SUPPLY REFERENCE WITH INTERNAL RESISTANCE OF 5k. AGND CAN ALSO BE DRIVEN BY A SYSTEM ANALOG GROUND REFERENCE NEAR HALF SUPPLY

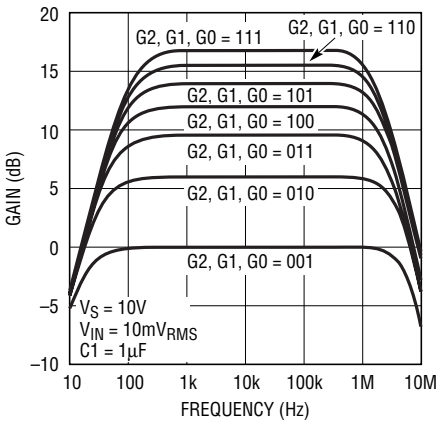
Frequency Response, LTC6910-1



Frequency Response, LTC6910-2



Frequency Response, LTC6910-3



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT®1228	100MHz Gain Controlled Transconductance Amplifier	Differential Input, Continuous Analog Gain Control
LT1251/LT1256	40MHz Video Fader and Gain Controlled Amplifier	Two Input, One Output, Continuous Analog Gain Control
LTC1564	10kHz to 150kHz Digitally Controlled Filter and PGA	Continuous Time, Low Noise 8th Order Filter and 4-Bit PGA
LTC6911	Dual Matched Programmable Gain Amplifier	Dual 6910 in a 10 Lead MSOP
LTC6915	Zero Drift Instrumentation Amplifier with Programmable Gain	Zero Drift, Digitally Programmable Gain Up to 4096 V/V

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LT/TP 0404 1K REV A • PRINTED IN USA
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