Multiphase Oscillator with Spread Spectrum Frequency Modulation

FEATURES

- **2-, 3- or 4-Phase Outputs**
- **Optional Spread Spectrum Frequency Modulation for Improved EMC Performance**
- **5kHz to 20MHz Frequency Range**
- One External Resistor Sets the Frequency
- One External Resistor Sets Percent Frequency Spreading
- 400µA Typical Supply Current, V_S = 3V, 1MHz
- Frequency Error ≤1.5% Max, 5kHz to 10MHz (T_A = 25°C)
- Frequency Error ≤2% Max, 5kHz to 10MHz (T_A = 0°C to 70°C)
- ±40ppm/°C Temperature Stability
- Fast Start-Up Time: 50µs to 1.5ms
- 100Ω CMOS Output Driver
- Operates from a Single 2.7V to 5.5V Supply
- Available in 10-Lead MS Package

APPLICATIONS

- Switching Power Supply Clock Reference
- Portable and Battery-Powered Equipment
- PDAs
- Cell Phones
- Clocking Switched Capacitor Filters

DESCRIPTION

The LTC®6902 is a precision, low power and easy-to-use oscillator that provides multiphase outputs in a small package. The oscillator frequency is set by a single external resistor (R_{SET}). The LTC6902 also provides an optional spread spectrum frequency modulation (SSFM) capability that can be activated and controlled by an additional external resistor (R_{MOD}).

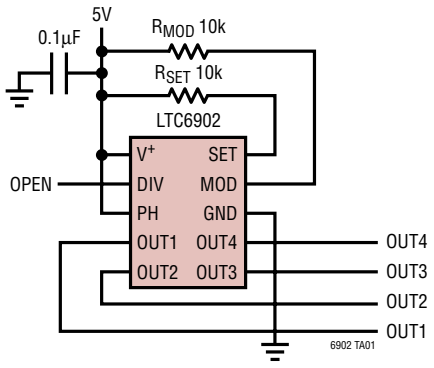
The LTC6902's master oscillator is controlled by the R_{SET} resistor and has a range of 100kHz and 20MHz. In order to accommodate a wider output frequency range, a programmable divider (divide by 1, 10 or 100) is included. The integrated programmable multiphase circuit provides either 2-, 3- or 4-phase waveforms.

The LTC6902's SSFM capability modulates the oscillator's frequency by a pseudorandom noise (PRN) signal to spread the oscillator's energy over a wide frequency band. This spreading decreases the peak electromagnetic radiation level and improves electromagnetic compatibility (EMC) performance. The amount of frequency spreading is programmable by a single additional external resistor (R_{MOD}) and is disabled by grounding the MOD pin.

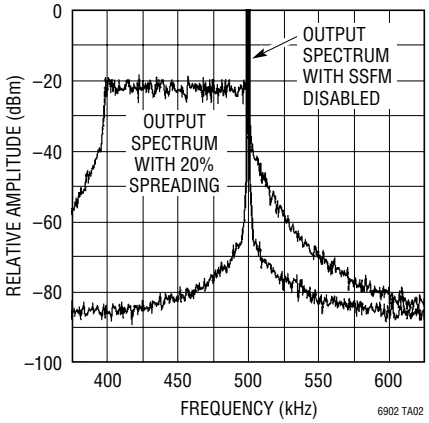
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TYPICAL APPLICATION

500kHz, 4-Phase Clock with 20% Frequency Spreading



Output Frequency Spectrum With and Without SSFM

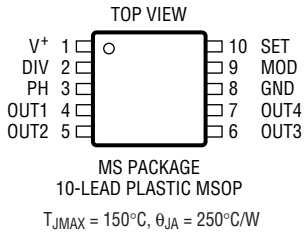


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage (V^+) to GND .....–0.3V to 6V
Voltage On Any Pin
(Referred to GND) .....–0.3V to (V^+ + 0.3V)
Operating Temperature Range (Note 9)
LTC6902C ..... –40°C to 85°C
LTC6902I ..... –40°C to 85°C
Specified Temperature Range (Note 10)
LTC6902C ..... –40°C to 85°C
LTC6902I ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec).....300°C

PACKAGE/ORDER INFORMATION



MS PACKAGE
10-LEAD PLASTIC MSOP

T_{JMAX} = 150°C, θ_{JA} = 250°C/W

ORDER PART NUMBER
LTC6902CMS LTC6902IMS
MS PART MARKING
LTK2 LTK3

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V^+ = 2.7V to 5.5V, R_L= 5k, C_L = 5pF, Pin 3 (PH) = 0V (2-phase, M = 1) unless otherwise specified. Pin 9 (MOD) is at 0V unless otherwise specified. R_{SET} is defined as a resistor connected from the SET pin to the V^+ pin. R_{MOD} is defined as a resistor connected from the MOD pin to the V^+ pin.

SYMBOL	PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
Δf_{OUT}	Frequency Accuracy (Notes 2, 3)	V^+ = 5V	5kHz ≤ f_{OUT} ≤ 10MHz			±0.5	±1.5	%
			1kHz ≤ f_{OUT} ≤ 5kHz			±2.0		%
			10MHz ≤ f_{OUT} ≤ 20MHz	●		±3.0	±4.0	%
			5kHz ≤ f_{OUT} ≤ 10MHz, LTC6902C	●			±2.0	%
			5kHz < f_{OUT} ≤ 10MHz, LTC6902I	●			±2.5	%
		V^+ = 2.7V	5kHz ≤ f_{OUT} ≤ 10MHz			±0.5	±1.5	%
			1kHz ≤ f_{OUT} ≤ 5kHz			±2.0		%
			5kHz ≤ f_{OUT} ≤ 10MHz, LTC6902C	●			±2.0	%
			5kHz ≤ f_{OUT} ≤ 10MHz, LTC6902I	●			±2.5	%
R_{SET}	Frequency Setting Resistor Range	$\lvert\Delta f_{OUT}\rvert$ < 1.5%, V^+ = 5V		●	20		400	kΩ
		$\lvert\Delta f_{OUT}\rvert$ < 1.5%, V^+ = 2.7V		●	20		400	kΩ
$\Delta f_{OUT}/\Delta T$	Frequency Drift Over Temperature (Note 3)	R_{SET} = 63.2k		●		±0.004		%/°C
$\Delta f_{OUT}/\Delta V$	Frequency Drift Over Supply (Note 3)	V^+ = 2.7V to 5V, R_{SET} = 63.2k		●		0.04	0.12	%/V
	Timing Jitter (Note 4)	20k ≤ R_{SET} ≤ 400k						
		Pin 2 = V^+ (N = 100)				0.1		%
		Pin 2 = Open (N = 10)				0.2		%
		Pin 2 = 0V (N = 1)				0.6		%
	Long-Term Stability of Output Frequency					300		ppm/$\sqrt{kHr}$
	Duty Cycle (Note 5)	Pin 2 = V^+ or Open (N = 100 or 10)						
		Pin 3 = 0V (2-Phase, M = 1)		●	49.0	50.0	51.0	%
		Pin 3 = Open (3-Phase, M = 3)		●	32.3	33.3	34.3	%
		Pin 3 = V^+ (4-Phase, M = 4)		●	49.0	50.0	51.0	%
		Pin 2 = 0V (N = 1)						
		Pin 3 = 0V (2-Phase, M = 1)		●	45.0	50.0	55.0	%
		Pin 3 = Open (3-Phase, M = 3)		●	32.3	33.3	34.3	%
		Pin 3 = V^+ (4-Phase, M = 4)		●	49.0	50.0	51.0	%

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V^+ = 2.7V to 5.5V, R_L= 5k, C_L = 5pF, Pin 3 (PH) = 0V (2-phase, M = 1) unless otherwise specified. Pin 9 (MOD) is at 0V unless otherwise specified. R_{SET} is defined as a resistor connected from the SET pin to the V^+ pin. R_{MOD} is defined as a resistor connected from the MOD pin to the V^+ pin.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V^+	Operating Supply Range		●	2.7		5.5	V
I_S	Power Supply Current	R_{SET} = 400k, R_L = ∞, Pin 2 = V^+ (N = 100), f_{OUT} = 5kHz					
		V^+ = 5V	●		0.35	0.55	mA
		V^+ = 2.7V	●		0.32	0.50	mA
		R_{SET} = 20k, R_L = ∞, Pin 2 = 0V (N = 1), f_{OUT} = 10MHz					
		V^+ = 5V	●		2.35	3.50	mA
		V^+ = 2.7V	●		1.40	1.80	mA
		R_{SET} = 400k, R_L = ∞, Pin 2 = V^+ (N = 100), R_{MOD} = 800k					
		V^+ = 5V	●		0.45	0.63	mA
		V^+ = 2.7V	●		0.34	0.50	mA
		R_{SET} = 20k, R_L = ∞, Pin 2 = 0V (N = 1), R_{MOD} = 40k					
		V^+ = 5V	●		2.50	3.60	mA
		V^+ = 2.7V	●		1.40	1.90	mA
V_{IH_DIV}	High Level DIV Input Voltage		●	V^+ – 0.4			V
V_{IL_DIV}	Low Level DIV Input Voltage		●			0.4	V
I_{DIV}	DIV Input Current (Note 6)	Pin 2 = V^+, V^+ = 5V	●		2	4	µA
		Pin 2 = 0V, V^+ = 5V	●	–4	–2		µA
V_{IH_PH}	High Level PH Input Voltage		●	V^+ – 0.4			V
V_{IL_PH}	Low Level PH Input Voltage		●			0.4	V
I_{PH}	PH Input Currrent (Note 6)	Pin 3 = V^+, V^+ = 5V	●		2	4	µA
		Pin 3 = 0V, V^+ = 5V	●	–4	–2		µA
V_{OH}	High Level Output Voltage (Note 6) (OUT1, OUT2, OUT3, OUT4)	V^+ = 5V, I_{OH} = –1mA	●	4.75	4.90		V
		V^+ = 5V, I_{OH} = –4mA	●	4.40	4.70		V
		V^+ = 2.7V, I_{OH} = –1mA	●	2.35	2.6		V
		V^+ = 2.7V, I_{OH} = –4mA	●	1.85	2.2		V
V_{OL}	Low Level Output Voltage (Note 6) (OUT1, OUT2, OUT3, OUT4)	V^+ = 5V, I_{OL} = 1mA	●		0.05	0.15	V
		V^+ = 5V, I_{OL} = 4mA	●		0.20	0.40	V
		V^+ = 2.7V, I_{OL} = 1mA	●		0.1	0.3	V
		V^+ = 2.7V, I_{OL} = 4mA	●		0.4	0.7	V
t_r	Output Rise Time (Note 7) (OUT1, OUT2, OUT3, OUT4)	V^+ = 5V, Pin 2 = V^+ or Open (N = 100 or N = 10)			14		ns
		V^+ = 5V, Pin 2 = 0V (N = 1)			7		ns
		V^+ = 2.7V, Pin 2 = V^+ or Open (N = 100 or N = 10)			19		ns
		V^+ = 2.7V, Pin 2 = 0V (N = 1)			11		ns
t_f	Output Fall Time (Note 7) (OUT1, OUT2, OUT3, OUT4)	V^+ = 5V, Pin 2 = V^+ or Open (N = 100 or N = 10)			13		ns
		V^+ = 5V, Pin 2 = 0V (N = 1)			6		ns
		V^+ = 2.7V, Pin 2 = V^+ or Open (N = 100 or N = 10)			19		ns
		V^+ = 2.7V, Pin 2 = 0V (N = 1)			10		ns
	Spread Spectrum Frequency Modulation Spreading Percentage (Downspread from Maximum Frequency) Percent = 100 • (f_{MAX} – f_{MIN})/f_{MAX} (Note 8)	V^+ = 5V, N = 10, R_{SET} = 20k, R_{MOD} = 10k	●	35	40	45.0	%
		V^+ = 5V, N = 10, R_{SET} = 20k, R_{MOD} = 40k	●	7.5	10	12.5	%
		V^+ = 2.7V, N = 10, R_{SET} = 20k, R_{MOD} = 10k	●	35	40	45.0	%
		V^+ = 2.7V, N = 10, R_{SET} = 20k, R_{MOD} = 40k	●	7.5	10	12.5	%

ELECTRICAL CHARACTERISTICS

Note 1: Absolute Maximum Ratings are those values beyond which the life of the device may be impaired.

Note 2: Frequencies near 100kHz and 1MHz may be generated using two different values of R_{SET} (see Applications Information). For these frequencies, the error is specified under the following assumption: $20k < R_{SET} \leq 400k$ for $5kHz \leq f_{OUT} \leq 10MHz$.

Note 3: Frequency accuracy is defined as the deviation from the f_{OUT} equation.

Note 4: Jitter is the ratio of the peak-to-peak distribution of the period to the mean of the period. This specification is based on characterization and is not 100% tested.

Note 5: Guaranteed by 5V test.

Note 6: To conform with the Logic IC Standard convention, current out of a pin is arbitrarily given as a negative value.

Note 7: Output rise and fall times are measured between the 10% and the 90% power supply levels with no output loading. These specifications are based on characterization.

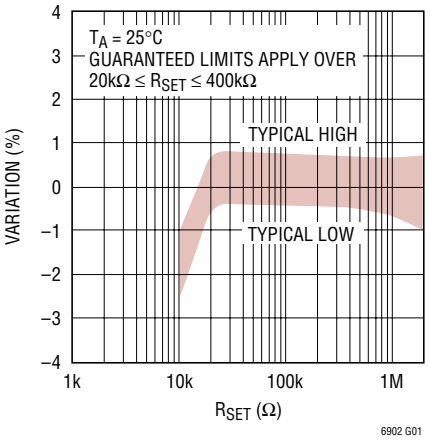
Note 8: f_{MAX} is defined as the highest frequency excursion and is equal to the f_{OUT} frequency set by the R_{SET} resistor. f_{MIN} is the lowest frequency excursion.

Note 9: The LTC6902CMS and LTC6902IMS are guaranteed functional over the operating temperature range of –40°C to 85°C.

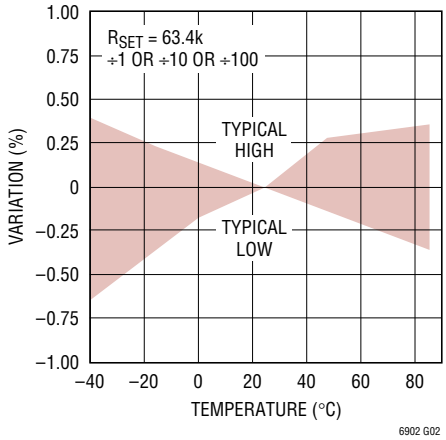
Note 10: The LTC6902CMS is guaranteed to meet 0°C to 70°C specifications and are designed, characterized and expected to meet the specified performance from –40°C to 85°C but is not tested or QA sampled at these temperatures. The LTC6902IMS is guaranteed to meet specified performance from –40°C to 85°C.

TYPICAL PERFORMANCE CHARACTERISTICS

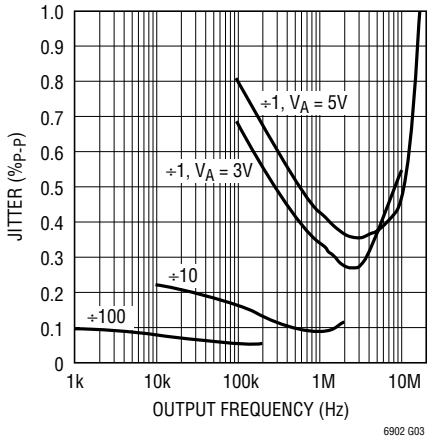
Frequency Variation vs R_{SET}



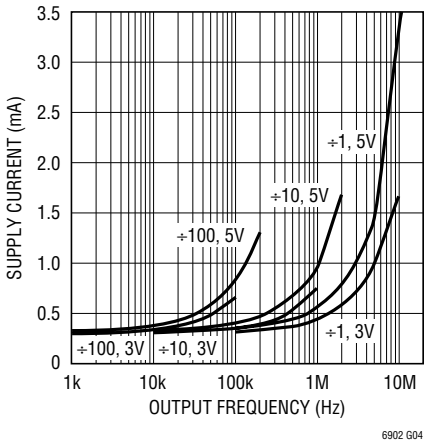
Frequency Variation Over Temperature



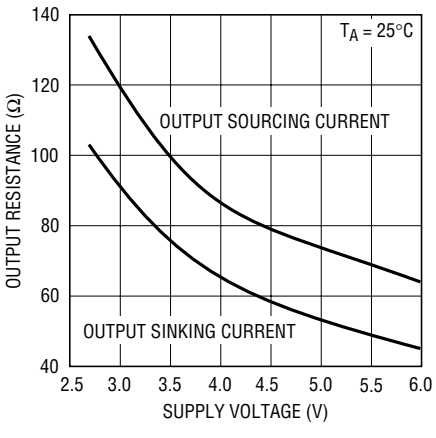
Peak-to-Peak Jitter vs Output Frequency (M = 1, 2-Phase Mode)



Supply Current vs Output Frequency [SSFM Disabled, 2-Phase Mode (M = 1)]

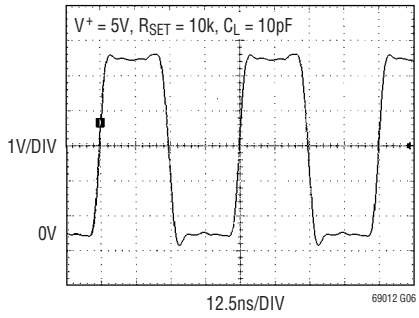


Output Resistance vs Supply Voltage

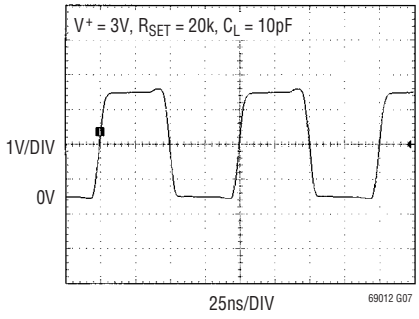


TYPICAL PERFORMANCE CHARACTERISTICS

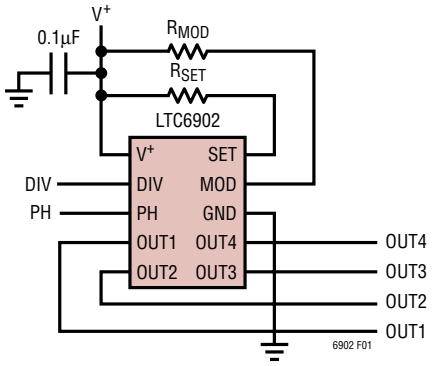
Output Operating at 20MHz, V_S = 5V



Output Operating at 10MHz, V_S = 3V



QUICK DESIGN GUIDE



$$f_{OUT} = \frac{10MHz}{N \bullet M} \bullet \left(\frac{20k\Omega}{R_{SET}}\right);\ 5kHz \le f_{OUT} \le 20MHz$$

$$\text{Spreading Percentage} = 20 \bullet \frac{R_{SET}}{R_{MOD}}$$

Figure 1. Typical Application with Design Equation

Step 1. Select Multiphase Mode, Setting M

By selecting the multiphase mode, a division parameter M is also chosen:

2-Phase: Connect PH Pin to GND	M = 1
3-Phase: Leave PH Open	M = 3
4-Phase: Connect PH Pin to V+	M = 4

Step 2. Choosing Programmable Divider Setting N

A. For applications using spread spectrum frequency modulation (SSFM) or applications that are constant frequency where low clock jitter is the primary specification:

DIVIDER SETTING		FREQUENCY RANGE (f_{OUT} • M)
N = 1	Connect DIV Pin to GND	2MHz to 20MHz
N = 10	Leave DIV Open	200kHz to 2MHz
N = 100	Connect DIV Pin to V+	<200kHz

Note: The frequency range numbers are for a 5V supply where a 20MHz output is the maximum frequency supported. For low supply applications (2.7V ≤ V+ ≤ 4V), the maximum rated output frequency is 10MHz and all of the above numbers should be halved.

B. For constant frequency applications where frequency accuracy is the primary specification:

DIVIDER SETTING		FREQUENCY RANGE (f_{OUT} • M)
N = 1	Connect DIV Pin to GND	> 500kHz*
N = 10	Leave DIV Open	50kHz to 500kHz
N = 100	Connect DIV Pin to V+	<50kHz

*The maximum frequency (f_{OUT} • M) is 20MHz for 5V applications and is 10MHz for low supply applications (2.7V ≤ V+ ≤ 4V).

QUICK DESIGN GUIDE

Step 3. Calculating the R_{SET} Resistor Value

The R_{SET} resistor, the multiphase mode and the divider setting set the output frequency (f_{OUT}) for constant frequency applications. For SSFM applications, the maximum frequency excursion (f_{MAX}) is equal to f_{OUT}.

$$R_{SET} = 20k\Omega \bullet \left(\frac{10MHz}{N \bullet M \bullet f_{OUT}} \right)$$

$$N = \begin{cases} 100 & DIV\ Pin = V^+ \\ 10 & DIV\ Pin = Open \\ 1 & DIV\ Pin = 0V \end{cases}$$

$$M = \begin{cases} 4 & (4\text{-}Phase\ Output)\ PH\ Pin = V^+ \\ 3 & (3\text{-}Phase\ Output)\ PH\ Pin = Open \\ 1 & (2\text{-}Phase\ Output)\ PH\ Pin = 0V \end{cases}$$

Step 4. Calculating the R_{MOD} Resistor Value

(Note: For constant frequency applications R_{MOD} is not required. Disable SSFM by connecting the MOD pin to GND)

$$R_{MOD} = 20 \bullet \frac{R_{SET}}{Spreading\ Percentage}$$

where the Spreading Percentage is defined by the following:

$$Spreading\ Percentage = 100 \bullet \frac{f_{MAX} - f_{MIN}}{f_{MAX}}$$

where f_{MAX} is the highest frequency excursion (set by the R_{SET} value calculated in Step 3) and f_{MIN} is the lowest frequency excursion.

Example

For a 4-phase, 250kHz clock with 40% spreading:

Connect PH Pin to $V^+ \rightarrow$ Selects 4-Phase Mode, M = 4
Leave DIV Pin Open $\rightarrow$ N = 10
R_{SET} = 20k $\rightarrow$ Sets $f_{OUT} = f_{MAX}$ = 250kHz
R_{MOD} = 10k $\rightarrow$ Sets Spreading to 40%

PIN FUNCTIONS

V^+ (Pin 1): Supply Voltage ($2.7V \leq V^+ \leq 5.5V$). The supply should be kept free from noise and ripple. It should be bypassed directly to a ground plane with a 0.1µF capacitor placed as close to the pin as possible.

DIV (Pin 2): Divider Setting Input. This three-state input selects among three divider settings determining the value of N in the frequency equation. Pin 2 should be tied to GND for the ÷1 setting, the highest frequency range. Floating Pin 2, leaving it open, divides the master oscillator by 10. Tie Pin 2 to V^+ for the ÷100 setting, the lowest frequency range. To detect a floating DIV pin, the LTC6902 places the pin at the midsupply point with active circuitry. Therefore, driving the DIV pin high requires sourcing approximately 2µA. Similarly, driving the DIV pin low requires sinking 2µA. When the DIV pin is floated, it should be bypassed by a 1nF capacitor to GND or it should be surrounded by a ground shield to prevent excessive coupling from other PCB traces.

PH (Pin 3): Phase Setting Input. This three-state input selects among three multiphase options. This sets the outputs to produce 2-phase, 3-phase or 4-phase signals. It also sets the value of M in the frequency equation. Pin 3 should be tied to GND for the 2-phase setting. This is the highest frequency range with M set to 1. Floating Pin 3, leaving it open, selects the 3-phase setting. This also sets M to 3. Tie Pin 3 to V^+ for the 4-phase setting. This is the lowest frequency range as M is set to 4. To detect a floating PH pin, the LTC6902 places the pin at the midsupply point with active circuitry. Therefore, driving the PH pin high requires sourcing approximately 2µA. Similarly, driving the PH pin low requires sinking 2µA. When the PH pin is floated, it should be bypassed by a 1nF capacitor to GND

PIN FUNCTIONS

or it should be surrounded by a ground shield to prevent excessive coupling from other PCB traces.

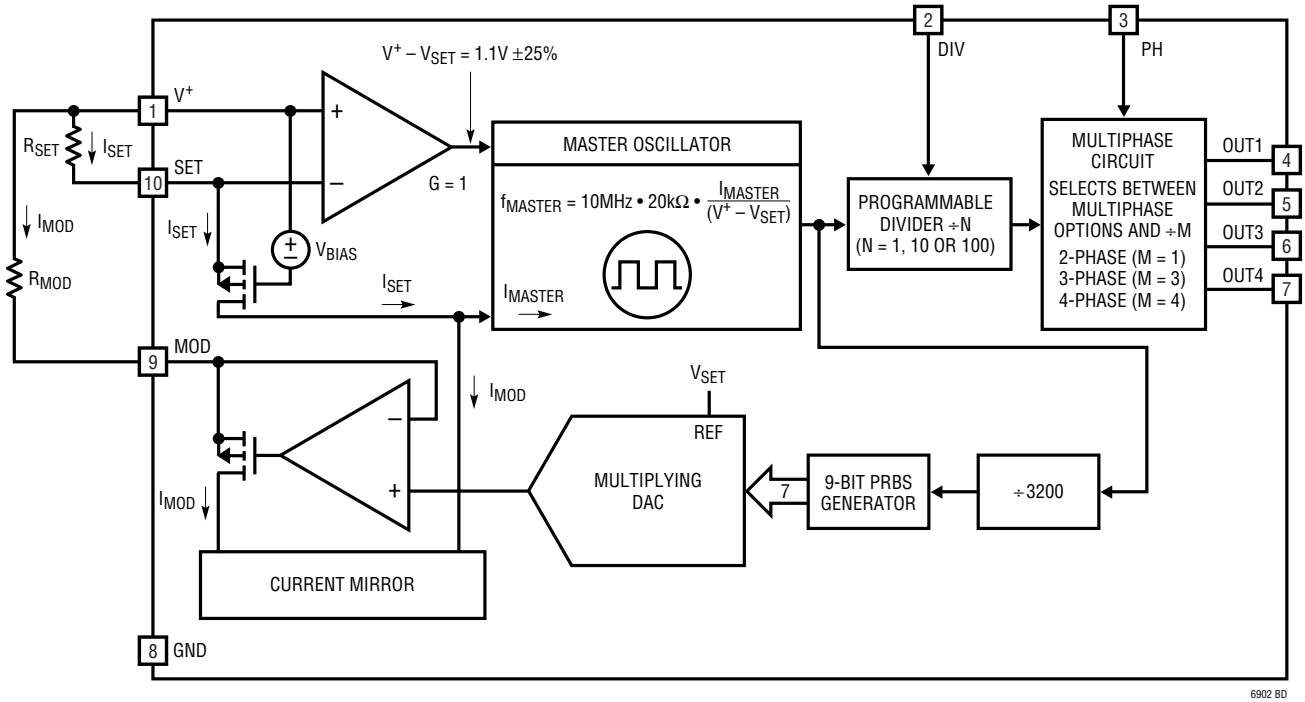
OUT1, OUT2, OUT3, OUT4 (Pins 4, 5, 6 and 7): Oscillator Outputs. These pins can drive 5kΩ and/or 10pF loads. Larger loads may cause inaccuracies due to supply bounce at high frequencies.

GND (Pin 8): Ground. Should be tied to a ground plane for best performance.

SET (Pin 10): Frequency Setting Resistor Input. The value of the resistor (R_{SET}) connected between Pin 10 and V^+ determines the oscillator frequency. The voltage on this pin is held at approximately 1.13V below the V^+ voltage. For best performance, use a precision metal film resistor with a value between 10k and 2M and limit the capacitance on this pin to less than 10pF.

MOD (Pin 9): Spread Spectrum Frequency Modulation Setting Resistor Input. The value of the resistor (R_{MOD}) connected between Pin 9 and V^+ determines the amount of frequency modulation. The output frequency is always modulated down from the frequency set by the R_{SET} resistor. For best performance, use a precision metal film resistor with a value between 10k and 2M and limit the capacitance on this pin to less than 10pF. The voltage on this pin is not static. Limiting the capacitance on this pin is important for the part to perform properly. **To disable the modulation, connect this pin to GND**. Grounding the MOD pin disables the modulation and shuts down the modulation circuitry to save power. **Leaving the pin open to disable the modulation is not recommended**. While leaving the pin open, $R_{MOD} \approx \infty$, gives the mathematical result of 0% modulation, the open pin is susceptible to external noise coupling that can effect frequency accuracy.

BLOCK DIAGRAM



THEORY OF OPERATION

As shown in the Block Diagram, the LTC6902's master oscillator is controlled by the ratio of the voltage between the V^+ and SET pins ($V^+ – V_{SET}$) and the current entering the master oscillator, I_{MASTER}. When the spread spectrum frequency modulation (SSFM) is disabled, I_{MASTER} is strictly determined by the $V^+ – V_{SET}$ voltage and the I_{SET} current. When SSFM is enabled, the current I_{MOD} (modulation current) is subtracted from the I_{SET} current to determine the I_{MASTER} current value. Here the I_{MASTER} current is maximally at I_{SET} but more often than not it is less than I_{SET} by a value determined by the I_{MOD} value. In this way the frequency of the master oscillator is modulated to produce a frequency that is always less than or equal to the frequency set by the I_{SET} current.

The voltage on the SET pin is forced to approximately 1.1V below V^+ by the PMOS transistor and its gate bias voltage. This voltage is accurate to ±8% at a particular input current and supply voltage (see Figure 2). The R_{SET} resistor, connected between the V^+ and SET pins, locks together the ($V^+ – V_{SET}$) voltage and the current I_{SET}. This allows the parts to attain excellent frequency accuracy regardless of the precision of the SET pin voltage. The LTC6902 is optimized for use with R_{SET} resistors between 10k and 2M. This corresponds to master oscillator frequencies between 100kHz and 20MHz. Additionally, the MOD pin's voltage tracks the SET pin's voltage. The R_{MOD} resistor connected between the V^+ and MOD pins similarly locks together the MOD pin voltage variation and the I_{MOD} current to once more yield excellent accuracy.

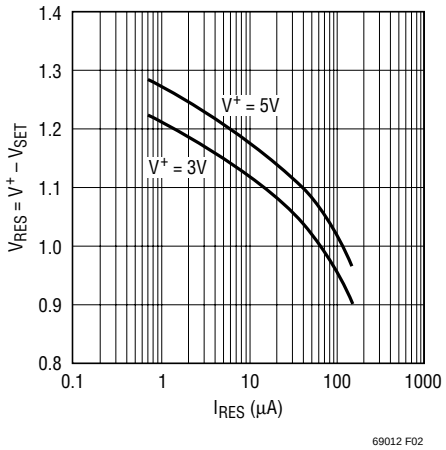


Figure 2. $V^+ – V_{SET}$ Variation with I_{RES}

The master oscillator's output is connected to the programmable divider. The output of the programmable divider is then connected to the multiphase circuit with its four outputs directly connected to output drivers. The final output frequency is determined by the R_{SET} resistor value, the programmable divider setting and the multiphase mode selected. The formula for setting the output frequency, f_{OUT}, is below:

$$f_{OUT} = \frac{10MHz}{N \bullet M} \bullet \left(\frac{20k\Omega}{R_{SET}} \right)$$

where:

$$N = \begin{cases} 100 & DIV\ Pin = V^+ \\ 10 & DIV\ Pin = Open \\ 1 & DIV\ Pin = 0V \end{cases}$$

$$M = \begin{cases} 4 & (4\text{-}Phase\ Output)\ PH\ Pin = V^+ \\ 3 & (3\text{-}Phase\ Output)\ PH\ Pin = Open \\ 1 & (2\text{-}Phase\ Output)\ PH\ Pin = 0V \end{cases}$$

When the spread spectrum frequency modulation (SSFM) is disabled, the frequency f_{OUT} is the final output frequency. When SSFM is enabled, f_{OUT} is the maximum output frequency with the R_{MOD} resistor value determining the minimum output frequency.

The programmable divider divides the master oscillator signal by 1, 10 or 100. The divide-by value is determined by the state of the DIV input (Pin 2). Tie DIV to GND or drive it below 0.5V to select ÷1. This is the highest frequency range, with the master output frequency passed directly to the multiphase circuit. The DIV pin may be floated or driven to midsupply to select ÷10, the intermediate frequency range. The lowest frequency range, ÷100, is selected by tying DIV to V^+ or driving it to within 0.4V of V^+. Figure 3 shows the relationship between R_{SET}, divider setting and output frequency, including the overlapping frequency ranges near 100kHz and 1MHz.

The multiphase circuit generates outputs that are either 2-, 3- or 4-phase waveforms. To generate the 3- and 4-phase output signals, the output from the programmable

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divider goes through further division. In addition to further division, the duty cycle of the output depends on the multiphase mode selected. Figure 4 shows the waveform at each output for 2-, 3- and 4-phase modes.

2-Phase Mode

In 2-phase mode, all outputs are nominally 50% duty cycle. OUT1 and OUT2 are 180 degrees out of phase. Stated differently, OUT2 is OUT1 inverted. However, OUT2 is **not** simply OUT1 routed through a standard logic inverter. This would lead to substantial delay for OUT2's transitions from OUT1's transitions. OUT1 and OUT2 are created by a delay matched inverting circuit. Apart from the basic inversion, the delay matching is determined by analog circuit parameters. With this type of design, OUT1 and OUT2 transitions are typically within 100ps. OUT3 and OUT4 are replications of OUT1 and OUT2 respectively. Since the two phases are generated via delay matched inverters, there is not any further division and the parameter M in the frequency setting equation is 1 (M = 1).

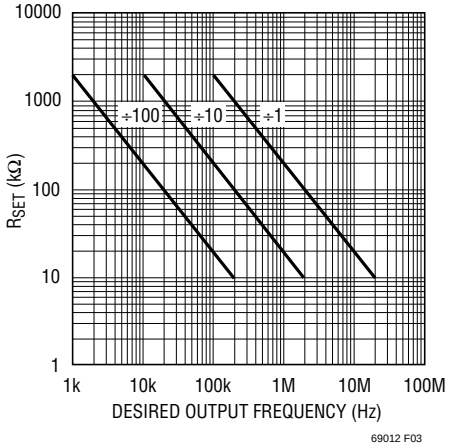


Figure 3. R_{SET} vs Desired Output Frequency (PH = GND, 2-Phase, M = 1)

3-Phase Mode

In 3-phase mode, OUT1, OUT2 and OUT3 are active and all three outputs have a 33.3% duty cycle. OUT4 is not active and is at a logic low state. The three active outputs are all 120 degrees out of phase. OUT2 lags OUT1 by 120 degrees and OUT3 lags OUT2 by 120 degrees. The signals are generated by a shift register. The output frequency is the programmable divider's output further divided 3 (M = 3).

4-Phase Mode

In 4-phase mode, all outputs have a 50% duty cycle. The outputs are all 90 degrees out of phase. OUT2 lags OUT1

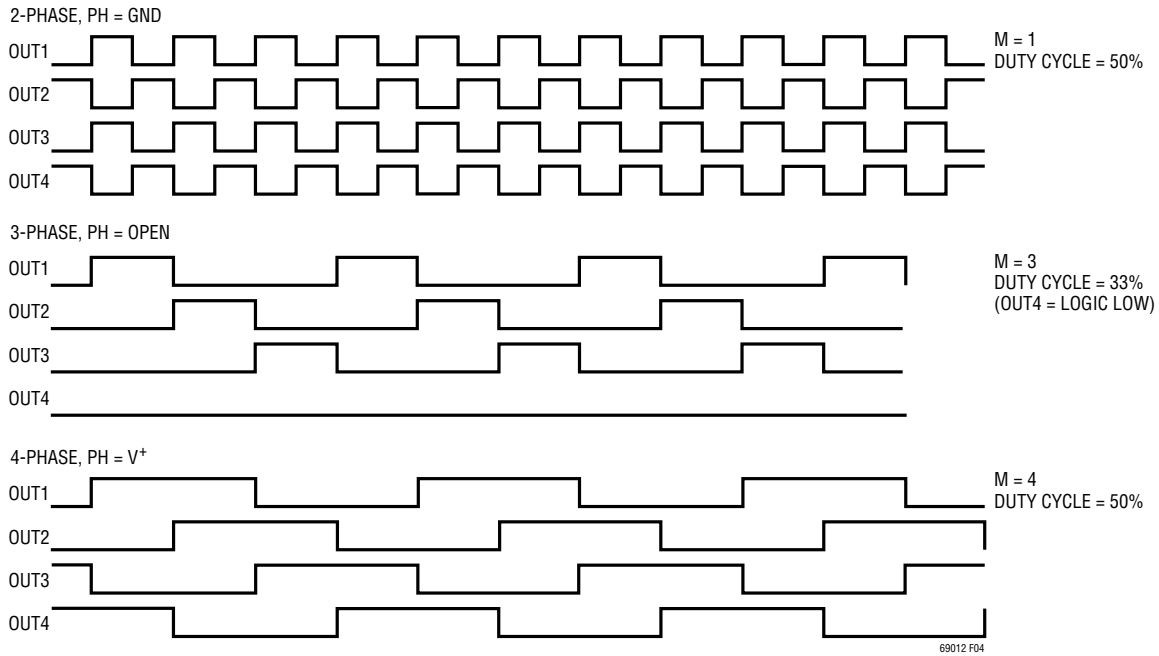


Figure 4. Mulitphase Output Waveforms

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by 90 degrees, OUT3 lags OUT2 by 90 degrees and OUT4 lags OUT3 by 90 degrees. The signals are generated by flip-flops. The output frequency is the programmable divider's output further divided 4 (M = 4).

The multiphase mode is determined by the state of the PH input (Pin 3). Tie the PH pin to GND or drive it below 0.5V to select the 2-phase mode. The PH pin may be floated or driven to midsupply to select the 3-phase mode. The 4-phase mode is selected by tying the PH pin to V^+ or driving it to within 0.4V of V^+.

The CMOS output drivers have an ON resistance that is typically less than 100Ω. In the ÷1 (high frequency) mode, the rise and fall times are typically 7ns with a 5V supply and 11ns with a 3V supply. These transition times maintain a clean square wave at 10MHz (20MHz at 5V supply). In the ÷10 and ÷100 modes, where the output frequency is much lower, slew rate control circuitry in the output driver increases the rise/fall times to typically 14ns for a 5V supply and 19ns for a 3V supply. The reduced slew rate lowers EMI (electromagnetic interference) and supply bounce.

Spread Spectrum Frequency Modulation

The LTC6902 provides the additional feature of spread spectrum frequency modulation (SSFM). The oscillator's frequency is modulated by a pseudorandom noise (PRN) signal to spread the oscillator's energy over a wide frequency band. This spreading decreases the peak electromagnetic radiation levels and improves electromagnetic compatibility (EMC) performance.

The amount of frequency spreading is determined by the external resistor R_{MOD} and the voltage between the V^+ and MOD pins ($V^+ – V_{MOD}$). Unlike the stationary SET pin voltage (V_{SET}), the MOD pin voltage (V_{MOD}) is a dynamic signal generated by a multiplying digital to analog converter (MDAC) referenced to V_{SET}. Referencing to V_{SET} negates errors due to variations of the V_{SET} voltage and locks the two voltages together. The V_{MOD} voltage is the V_{SET} voltage scaled by one fifth and multiplied by the digital code sent to the MDAC from the pseudorandom binary sequence (PRBS) generator. V_{MOD} varies in a pseudorandom noise-like manner. The ($V^+ – V_{MOD}$) voltage is 0V minimum and maximally one fifth (20%) of ($V^+ – V_{SET}$).

Referencing V_{MOD} to V_{SET} allows the ratio of R_{SET} to R_{MOD} to determine the amount of frequency spreading. Consider the case when R_{SET} is equal to R_{MOD}. Here, when the ($V^+ – V_{MOD}$) voltage is at its minimum of 0V, I_{MOD} = 0A, $I_{MASTER} = I_{SET}$ and the master oscillator is at its maximum frequency (f_{MAX}) which is the f_{OUT} frequency set by the R_{SET} resistor. Furthermore, when the ($V^+ – V_{MOD}$) voltage is at its maximum of 20% of ($V^+ – V_{SET}$), $I_{MOD} = 0.2 \bullet I_{SET}$, $I_{MASTER} = 0.8 \bullet I_{SET}$ and the master oscillator is at its minimum frequency (f_{MIN}) which is 80% of the f_{OSC} frequency set by the R_{SET} resistor. The general formula for the amount of frequency spreading is below:

$$\text{Frequency Spreading (in \%)} = 20 \bullet \frac{R_{SET}}{R_{MOD}}$$

where frequency spreading is defined as:

$$\text{Frequency Spreading (in \%)} = 100 \bullet \frac{f_{MAX} - f_{MIN}}{f_{MAX}}$$

The design procedure is to first choose the R_{SET} resistor value to set f_{MAX} (f_{OUT}) and then choose the R_{MOD} resistor value to set the amount of frequency spreading desired. Note that the frequency is always modulated to a lower value. This is often referred to as a down spread signal.

To disable the SSFM, connect the MOD pin to ground. Grounding the MOD pin disables the modulation and shuts down the modulation circuitry. While leaving the MOD pin open, $R_{MOD} = \infty$, gives a frequency spreading of 0%, this is not a good method of disabling the modulation. The open pin is susceptible to external noise coupling that can affect the output frequency accuracy. Grounding the MOD pin is the best way to disable the SSFM.

As stated previously the modulating waveform is a pseudorandom noise-like waveform. The pseudorandom signal is generated by a linear feedback shift register that is 9 bits long. The pseudorandom sequence will repeat every 512 (2^9) shift register clock cycles. The bottom seven bits of the shift register are sent in parallel to the MDAC which produces the V_{MOD} voltage. Being a digitally generated signal, the output is not a perfectly smooth waveform but consists of 128 (2^7) discrete steps that change every shift register

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clock cycle. Note that the shift register clock is the master oscillator's output divided by 3200. This results in a somewhat slow moving modulating signal where each step is separated in time by 3200/f_{MASTER} seconds and the pseudorandom sequence repeats every (512 • 3200)/f_{MASTER} seconds.

The servo loop in the LTC6902 cannot respond instantaneously to each step due to its limited bandwidth. The V_{MOD} voltage steps are converted to frequency steps by the servo loop. The servo loop has a bandwidth of about 25kHz that limits the frequency change rate and softens corners of the waveform. This is beneficial when the LTC6902 is used to clock switching regulators as will be discussed in the Applications Information section. Figure 5 illustrates the how the output frequency varies over time.

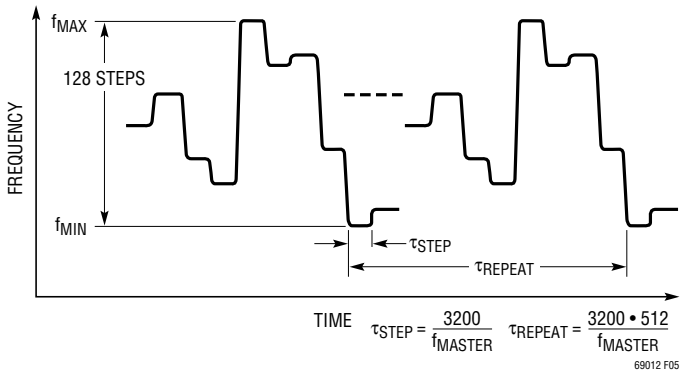


Figure 5

APPLICATIONS INFORMATION

SELECTING THE DIVIDER SETTING AND R_{SET} VALUE

The LTC6902's master oscillator has a frequency range spanning 0.1MHz to 20MHz. However, accuracy may suffer if the master oscillator is operated at greater than 10MHz with a supply voltage lower than 4V. A programmable divider extends the frequency range to greater than three decades. Additional frequency division may occur depending on the multiphase mode selected. The multiphase mode and the parameter M are generally dependent on the application's requirement and usually do not offer any additional design flexibility.

The LTC6902's master oscillator covers a 200:1 range while the programmable divider has 10:1 steps (1, 10, 100). This wide frequency range coupled with the part's programmable divider yields at least two solutions for any desired output frequency (the exception being the highest output frequencies that cannot be divided down). Choosing the best divider setting and the correct R_{SET} resistor value depends on the application.

For spread spectrum frequency modulated (SSFM) applications, choose the highest divider setting. This forces the master oscillator to run at its highest frequency. The pseudorandom signal generator is clocked by the master oscillator, not the output, and the faster the signal moves the greater the improvement in EMC performance. For most applications the multiphase mode is determined by the specific application's need. For these applications, the parameter M is predetermined and fixed. Table 1 lists the recommended output (f_{OUT}) frequency range for each divider setting when using SSFM.

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Table 1. Recommended Frequency Range vs Programmable Divider Setting for SSFM Applications or for Low Jitter Constant Frequency Applications

DIVIDER SETTING		FREQUENCY RANGE (f_{OUT} • M)
N = 1	DIV (Pin 2) = GND	2MHz to 20MHz
N = 10	DIV (Pin 2) = Open	200kHz to 2MHz
N = 100	DIV (Pin 2) = V^+	<200kHz

Note: The frequency range numbers are for a 5V supply where a 20MHz output is the maximum frequency supported. For low supply applications ($2.7V \leq V^+ \leq 4V$), the maximum rated output frequency is 10MHz and all of the above numbers should be halved.

For constant frequency applications, where SSFM is disabled, the best operating position depends on which parameter is most important in the application. For the lowest clock jitter it is best to set the divider to its highest setting as done above. The divider reduces the master oscillator's jitter. The higher the division number the greater the reduction in the master oscillator's jitter. For the best frequency accuracy it is best to run the programmable divider at its lowest setting, and thus, the master oscillator runs at a lower frequency. The lower master oscillator frequencies are more accurate and use less power. To determine a tradeoff between frequency accuracy and jitter consult the Typical Performance Characteristics curves. Table 2 lists the recommended output frequency range for each divider setting for continuous frequency applications where frequency accuracy is the primary specification.

Table 2. Recommended Frequency Range vs Programmable Divider Setting for Best Frequency Accuracy, Constant Frequency Applications (SSFM disabled)

DIVIDER SETTING		FREQUENCY RANGE (f_{OUT} • M)
N = 1	DIV (Pin 2) = GND	> 500kHz*
N = 10	DIV (Pin 2) = Open	50kHz to 500kHz
N = 100	DIV (Pin 2) = V^+	<50kHz

*The maximum frequency (f_{OUT} • M) is 20MHz for 5V applications and is 10MHz for low supply applications ($2.7V \leq V^+ \leq 4V$).

For some applications, the multiphase circuit is also useful in forcing the master oscillator to run at a higher or lower frequency. If the application requires a single clock source, the multiphase circuit can be set in whatever mode gives the highest or lowest divider number (M) and thus the highest or lowest master oscillator frequency. Additionally, if the application requires just two phases, the 4-phase mode can be selected with only the OUT1 and OUT3 outputs are used (or alternatively the OUT2 and OUT4 outputs).

For instance, a 500kHz, 2-phase clock can be obtained in four different ways. Table 3 lists the possible solutions. For an SSFM application, the preferred solution for best EMC performance is the last alternative where the master oscillator is at 20MHz. For a constant frequency application, the preferred solution is the first alternative with the master oscillator at 500kHz.

Table 3. Four Possible Ways to Obtain a 500kHz, 2-Phase Clock

R_{SET}	N	MULTIPHASE MODE	M	f_{MASTER}	OUTPUTS
400k	1	2	1	500kHz	OUT1, OUT2
100k	1	4	4	2MHz	OUT1, OUT3
40k	10	2	1	5MHz	OUT1, OUT2
10k	10	4	4	20MHz	OUT1, OUT3

After choosing the proper divider setting, determine the correct frequency-setting resistor. Because of the linear correspondence between oscillation period and resistance, a simple equation relates resistance with frequency.

$$R_{SET} = 20k \bullet \left(\frac{10MHz}{M \bullet N \bullet f_{OUT}} \right), \; N = \begin{cases} 100 \\ 10 \\ 1 \end{cases} \quad M = \begin{cases} 4 \\ 3 \\ 1 \end{cases}$$

(R_{SETMIN} = 10k, R_{SETMAX} = 2M)

Any resistor, R_{SET}, tolerance adds to the inaccuracy of the oscillator, f_{OUT}.

SETTING THE SPREAD SPECTRUM MODULATION SPREADING PERCENTAGE WITH THE LTC6902

Setting the spread spectrum modulation percentage on the LTC6902 is very simple and straightforward. Since the spreading is ratiometric, in percentage, the programmable divider and multiphase mode selection have no influence on the spreading percentage. In general, for greatest EMC improvement, each application should apply as much spreading as possible. The amount of spreading that any particular application can tolerate is dependent on the specific nature of that application. Once the R_{SET} resistor value is calculated to set f_{MAX} and the desired

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spreading is determined, the R_{MOD} value is calculated using the simple equation below:

$$R_{MOD} = 20 \bullet \frac{R_{SET}}{\text{Spreading Percentage}}$$

The only limitations for this formula are in the R_{MOD} value range and the spreading percentage range. The range of the R_{MOD} resistor value is the same as that for R_{SET} ranging from 10k to 400k. The LTC6902 is tested and specified for spreading of 10% and 40%. These are practical limits that would apply to many systems but they are not the actual limits of the part. The lower end limit is set by internal offsets and mismatches. At lower spreading percentages, these mismatches become more significant and the error from the calculated, desired spreading increases. A practical lower end limit would be about 5% spreading. At the higher end internal mismatching becomes less significant, however other factors come into play and a theoretical limit approaching 100% (f_{MIN} approaching zero) cannot be reliably achieved. A practical upper limit would be about 80% spreading.

To disable the SSFM, connect the MOD pin to ground. Grounding the MOD pin disables the modulation and shuts down the modulation circuitry. While leaving the MOD pin open, $R_{MOD} = \infty$, gives a frequency spreading of 0%, this is not a good method of disabling the modulation. The open pin is susceptible to external noise coupling that can affect the output frequency accuracy. Grounding the MOD pin is the best way to disable the SSFM.

DRIVING LOGIC CIRCUITS

The outputs of the LTC6902 are suitable for driving general digital logic circuits. The CMOS output drivers have an ON resistance that is typically less than 100Ω and are very similar in performance to HCMOS logic outputs. However, the form of frequency spreading used in the LTC6902 may not be suitable for many logic designs. Many logic designs have fairly tight timing and cycle-to-cycle jitter requirements. These systems often benefit from a spread spectrum clocking system where the frequency is slowly and linearly modulated by a triangular waveform, not a pseudorandom waveform. This type of frequency spreading maintains a minimal difference in the timing from one clock edge to the next adjacent clock edge (cycle-to-cycle jitter). The LTC6902 uses a pseudorandom modulating signal where the frequency transitions have been slowed and the corners rounded by a 25kHz lowpass filter. This filtered modulating signal may be acceptable for many logic systems but the cycle-to-cycle jitter issues must be considered carefully.

DRIVING SWITCHING REGULATORS

The LTC6902 is designed primarily to provide an accurate and stable clock for switching regulator systems, especially those systems with multiple switching regulators where all of the regulators are interleaved and are run at the same frequency. This lowers the input capacitor requirements and prevents beat notes formed by mixing numerous clock frequencies and their harmonics. The multiphase outputs have CMOS drivers with an ON resistance that is typically less than 100Ω and are very similar in performance to HCMOS logic outputs. This is suitable for directly driving most switching regulators and switching controllers. Linear Technology has a broad line of fully integrated switching regulators and switching regulator controllers designed for synchronization to an external clock. All of these parts have one pin assigned for external clock input. The nomenclature varies depending on the part's family history. SYNC, PLLIN, SYNC/MODE, SHDN, EXTCLK, FCB and S/S (shorthand for SYNC/SHDN) are examples of clock input pin names used with Linear Technology ICs. The exact operating details depend on the switching regulator in use, but generally switching is synchronized to the rising edge of the clock. Since the LTC6902's master oscillator is passed through inverters or flip-flops to generate its multiphase outputs, coincident rising edges (or falling edges) cannot occur. This is true even when the LTC6902 is used with a high percentage of spreading.

For the best EMC performance, the LTC6902 should be run with SSFM enabled and the master oscillator at its highest frequency. The pseudorandom modulation signal

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generator is driven by the master oscillator frequency, not the output frequency. This gives some design flexibility in the choice of the R_{SET} and the programmable divider setting. When making the choice, usually the faster master oscillator is the better choice. This is especially true when the main goal is to lower peak radiated or conducted signal levels measured during regulatory agency testing. Regulatory testing is done with strictly specified bandwidths and conditions. Modulating faster than the test bandwidth or as close to the bandwidth as possible gives the lowest readings. The optimal modulating rate is not as straightforward when the goal is to lower radiated signal levels interfering with other circuitry in the system. The modulation rate will have to be evaluated with the specific system conditions to determine the optimal rate. Depending on the specific frequency synchronization method a switching regulator employs, the modulation rate must be within the synchronization capability of the regulator. Many switching regulators use a phase-locked loop (PLL) for synchronization. For these parts, the PLL loop filter should be designed to have sufficient capture range and bandwidth.

Even when running the LTC6902 at the maximum modulation rate, the frequency hopping transitions are slowed by the part's servo loop. The frequency transitions are slowed by a 25kHz lowpass. This is an important feature when driving a switching regulator. The switching regulator is itself a servo loop with a bandwidth typically on the order of 1/10, but can vary from 1/50 to 1/2 of the operating frequency. When the input clock frequency's transition is within the bandwidth of the switching regulator, the regulator's output stays in regulation. If the transition is too sharp, beyond the bandwidth of the switching regulator, the regulator's output will experience a sharp jump and then settle back into regulation. If the bandwidth of the switching regulator is sufficiently high, beyond 25kHz, then there will not be any regulation issues.

One aspect of the output voltage that will change is the output ripple voltage. Every switching regulator has some output ripple at the clock frequency. For most switching regulator designs with fixed MOSFETs, fixed inductor, fixed capacitors, the amount of ripple will vary some with the regulator's operating frequency (the main exception being hysteresis architecture regulators). An increase in frequency results in lower ripple and a frequency decrease gives more ripple. This is true for static frequencies or dynamic frequency modulated systems. If the modulating signal was a triangle wave, the regulator's output would have a ripple that is amplitude modulated by the triangle wave. This repetitive signal on the power supply could cause system problems by mixing with other desired signals and giving a distorted output. Depending on the inductor design and triangle wave frequency, it may even result in an audible noise. The LTC6902 uses a pseudorandom noise-like modulating signal. This results in the regulator's output ripple being modulated by the wideband pseudorandom noise-like signal. On an oscilloscope, it looks essentially noise-like of even amplitude. The signal is broadband and any mixing issues are minimized. Additionally, the pseudorandom signal repeats at such a low rate that it is well below the audible range.

The LTC6902 directly drives many switching regulators. The LTC6902 with the spread spectrum frequency modulation results in improved EMC performance. If the bandwidth of the switching regulator is sufficient, not a difficult requirement in most cases, the regulator's regulation, efficiency and load response are maintained while peak electromagnetic radiation (or conduction) is reduced. Output ripple may be somewhat increased, but its behavior is very much like noise and its system impact is benign.

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POWER SUPPLY SENSITIVITY

Figure 6 shows the output frequency sensitivity to power supply voltage at several different temperatures. The LTC6902 has a guaranteed voltage coefficient of 0.1%/V but, as Figure 6 shows, the typical supply sensitivity is twice as low.

START-UP TIME

The start-up time and settling time to within 1% of the final value can be estimated by $t_{START} \cong R_{SET}(3.7\mu s/k\Omega) + 10\mu s$. Note the start-up time depends on R_{SET} and is independent from the setting of the divider pin. For instance with R_{SET} = 100k, the LTC6902 will settle with 1% of its 200kHz final value (N = 10) in approximately 380µs. Figure 7 shows start-up times for various R_{SET} resistors.

Jitter

The Peak-to-Peak Jitter vs Output Frequency graph, in the Typical Performance Characteristics section, shows the typical clock jitter as a function of oscillator frequency and power supply voltage. The capacitance from the SET pin, (Pin 3), to ground must be less than 10pF. If this requirement is not met, the jitter will increase.

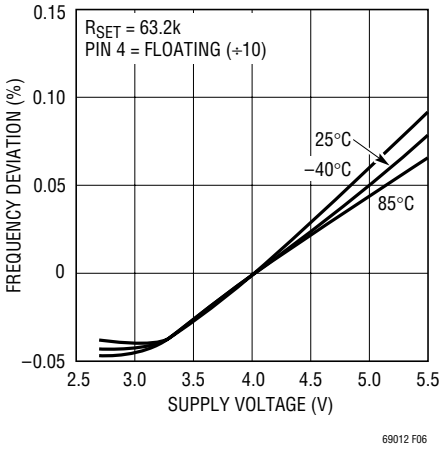


Figure 6. Supply Sensitivity

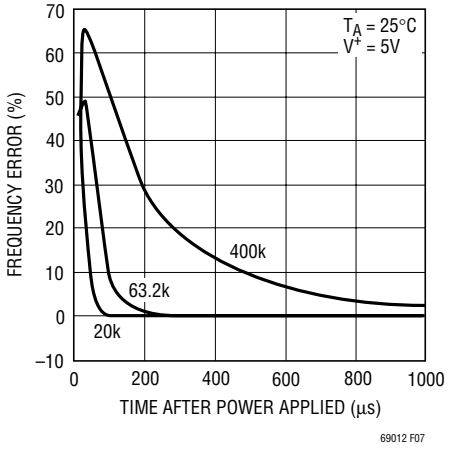
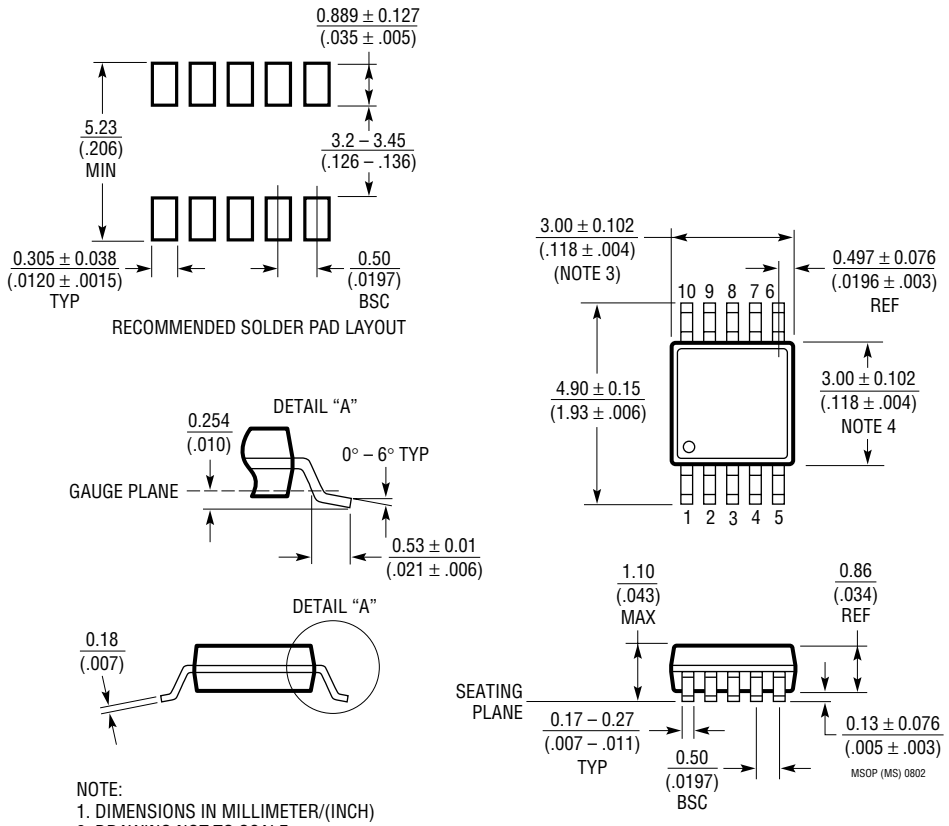


Figure 7. Start-Up Time

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PACKAGE DESCRIPTION

MS Package
10-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1661)



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1799	1kHz to 30MHz ThinSOT™ Oscillator	Single Output, Higher Frequency Operation
LTC6900	1kHz to 20MHz ThinSOT Oscillator	Single Output, Lower Power

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