isoSPI Isolated Communications Interface

FEATURES

- **1Mbps Isolated SPI Data Communications**
- **Simple Galvanic Isolation Using Standard Transformers**
- **Bidirectional Interface Over a Single Twisted Pair**
- **Supports Cable Lengths Up to 100 Meters**
- **Very Low EMI Susceptibility and Emissions**
- **Configurable for High Noise Immunity or Low Power**
- **Engineered for ISO26262 Compliant Systems**
- Requires No Software Changes in Most SPI Systems
- Ultralow, 2µA Idle Current
- Automatic Wake-Up Detection
- Operating Temperature Range: –40°C to 125°C
- 2.7V to 5.5V Power Supply
- Interfaces to All Logic from 1.7V to 5.5V
- Available in 16-Lead QFN and MSOP Packages

APPLICATIONS

- Industrial Networking
- Battery Monitoring Systems
- Remote Sensors

DESCRIPTION

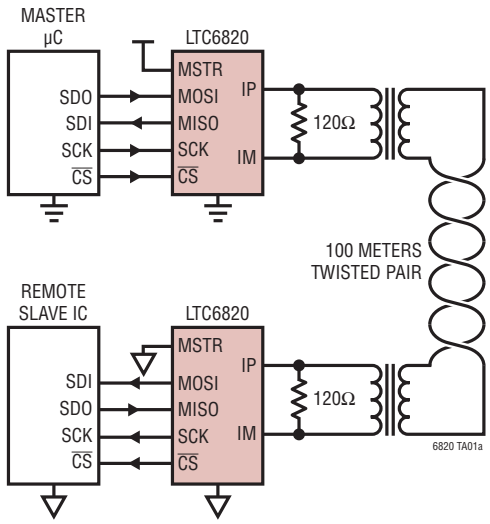
The LTC®6820 provides bidirectional SPI communications between two isolated devices through a single twisted-pair connection. Each LTC6820 encodes logic states into signals that are transmitted across an isolation barrier to another LTC6820. The receiving LTC6820 decodes the transmission and drives the slave bus to the appropriate logic states. The isolation barrier can be bridged by a simple pulse transformer to achieve hundreds of volts of isolation.

The LTC6820 drives differential signals using matched source and sink currents, eliminating the requirement for a transformer center tap and reducing EMI. Precision window comparators in the receiver detect the differential signals. The drive currents and the comparator thresholds are set by a simple external resistor divider, allowing the system to be optimized for required cable lengths and desired signal-to-noise performance.

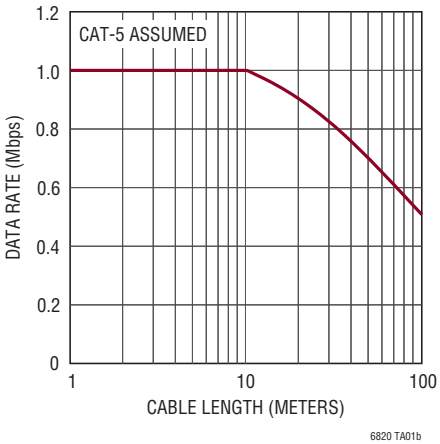
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TYPICAL APPLICATION

Microcontroller to SPI Slave Isolated Interface



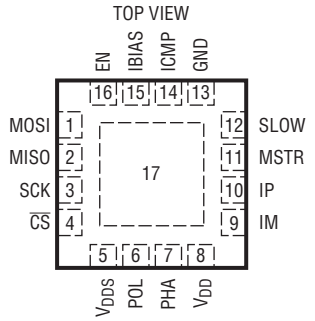
Data Rate vs Cable Length



ABSOLUTE MAXIMUM RATINGS (Notes 1, 2, 3)

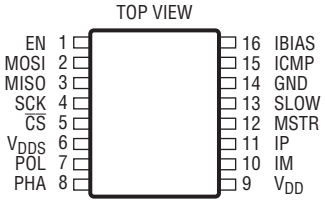
Input Supply Voltages (V_{DD} and V_{DDS}) to GND 6V
Pin Voltages
SCK, $\overline{CS}$, EN.....–0.3V to V_{DDS} + 0.3V (6V Max)
IBIAS, SLOW, IP, IM.....–0.3V to V_{DD} + 0.3V (6V Max)
All Other Pin Voltages..... –0.3V to 6V
Maximum Source/Sink Current
IP, IM 30mA
MOSI, MISO, SCK, $\overline{CS}$.....20mA
Operating Temperature Range
LTC6820I .....–40°C to 85°C
LTC6820H..... –40°C to 125°C
Specified Temperature Range
LTC6820I .....–40°C to 85°C
LTC6820H..... –40°C to 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)
MSOP .....300°C

PIN CONFIGURATION



UD PACKAGE
16-LEAD (3mm × 3mm) PLASTIC QFN

T_{JMAX} = 150°C, θ_{JA} = 58.7°C/W
EXPOSED PAD (PIN 17) PCB CONNECTION TO GND IS OPTIONAL



MS PACKAGE
16-LEAD PLASTIC MSOP

T_{JMAX} = 150°C, θ_{JA} = 120°C/W

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE
LTC6820IUD#PBF	LTC6820IUD#TRPBF	LGFM	16-Lead (3mm × 3mm) Plastic QFN	–40°C to 85°C
LTC6820HUD#PBF	LTC6820HUD#TRPBF	LGFM	16-Lead (3mm × 3mm) Plastic QFN	–40°C to 125°C
LTC6820IMS#PBF	LTC6820IMS#TRPBF	6820	16-Lead Plastic MSOP	–40°C to 85°C
LTC6820HMS#PBF	LTC6820HMS#TRPBF	6820	16-Lead Plastic MSOP	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Consult LTC Marketing for information on nonstandard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full specified temperature range, otherwise specifications are at T_A = 25°C. V_{DD} = 2.7V to 5.5V, V_{DDS} = 1.7V to 5.5V, R_{BIAS} = 2k to 20k unless otherwise specified. All voltages are with respect to GND.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Power Supply							
V_{DD}	Operating Supply Voltage Range		●	2.7		5.5	V
V_{DDS}	IO Supply Voltage Range (Level Shifting)	Affects $\overline{CS}$, SCK, MOSI, MISO and EN Pins	●	1.7		5.5	V
I_{DD}	Supply Current, READY/ACTIVE States (Note 4)	R_{BIAS} = 2kΩ (I_B = 1mA) $1/t_{CLK}$ = 0MHz $1/t_{CLK}$ = 1MHz	●	4	4.8 7	5.8	mA mA
		R_{BIAS} = 20kΩ (I_B = 0.1mA) $1/t_{CLK}$ = 0MHz $1/t_{CLK}$ = 1MHz	●	1.3	2 2.4	2.9	mA mA
	Supply Current, IDLE State	MSTR = 0V MSTR = V_{DD}	● ●		2 1	6 3	µA µA
I_{DDS}	IO Supply Current (Note 5)	SPI Inputs and EN Pin at 0V or V_{DDS}, SPI Outputs Unloaded	●			1	µA
Biasing							
V_{BIAS}	Voltage on IBIAS Pin	READY/ACTIVE State IDLE State	●	1.9	2.0 0	2.1	V V
I_B	Isolated Interface Bias Current (Note 6)	R_{BIAS} = 2k to 20k	●		V_{BIAS}/R_{BIAS}		mA
A_{IB}	Isolated Interface Current Gain	$V_A \leq$ 1.6V I_B = 1mA I_B = 0.1mA	● ●	18 18	20 20	22 24	mA/mA mA/mA
V_A	Transmitter Pulse Amplitude	$V_A = \lvert V_{IP} - V_{IM} \rvert$ V_{DD} < 3.3V $V_{DD} \geq$ 3.3V	● ●			V_{DD} – 1.7V 1.6	V V
V_{ICMP}	Threshold-Setting Voltage on ICMP Pin	$V_{TCMP} = A_{TCMP} \bullet V_{ICMP}$	●	0.2		1.5	V
$I_{LEAK(ICMP)}$	Leakage Current on ICMP Pin	V_{ICMP} = 0V to V_{DD}	●			±1	µA
$I_{LEAK(IP/IM)}$	Leakage Current on IP and IM Pins	IDLE State, $V_{IP} = V_{IM}$ = 0V to V_{DD}	●			±2	µA
A_{TCMP}	Receiver Comparator Threshold Voltage Gain	$V_{CM} = V_{DD}/2$ to V_{DD} – 0.2V, V_{ICMP} = 0.2V to 1.5V	●	0.4	0.5	0.6	V/V
V_{CM}	Receiver Common Mode Bias	IP/IM Not Driving			($V_{DD} - V_{ICMP}/3$ – 167mV)		V
R_{IN}	Receiver Input Resistance	Single-Ended to IP or IM	●	26	35	42	kΩ
Idle/Wake-Up (See Figures 13, 14, 15)							
V_{WAKE}	Differential Wake-Up Voltage (See Figure 13)	t_{DWELL} = 240ns	●	240			mV
t_{DWELL}	Dwell Time at V_{WAKE}	V_{WAKE} = 240mV	●	240			ns
t_{READY}	Start-Up Time After Wake Detection		●			8	µs
t_{IDLE}	Idle Time-Out Duration		●	4	5.7	7.5	ms
Digital I/O							
$V_{IH(CFG)}$	Digital Voltage Input High, Configuration Pins (PHA, POL, MSTR, SLOW)	V_{DD} = 2.7V to 5.5V (POL, PHA, MSTR, SLOW)	●	0.7 • V_{DD}			V
$V_{IL(CFG)}$	Digital Voltage Input Low, Configuration Pins (PHA, POL, MSTR, SLOW)	V_{DD} = 2.7V to 5.5V (POL, PHA, MSTR, SLOW)	●			0.3 • V_{DD}	V
$V_{IH(SPI)}$	Digital Voltage Input High, SPI Pins ($\overline{CS}$, SCK, MOSI, MISO)	V_{DDS} = 2.7V to 5.5V V_{DDS} = 1.7V to 2.7V	● ●	0.7 • V_{DDS} 0.8 • V_{DDS}			V V
$V_{IL(SPI)}$	Digital Voltage Input Low, SPI Pins ($\overline{CS}$, SCK, MOSI, MISO)	V_{DDS} = 2.7V to 5.5V V_{DDS} = 1.7V to 2.7V	● ●			0.3 • V_{DDS} 0.2 • V_{DDS}	V V
$V_{IH(EN)}$	Digital Voltage Input High, EN Pin	V_{DDS} = 2.7V to 5.5V V_{DDS} = 1.7V to 2.7V	● ●	2 0.85 • V_{DDS}			V V
$V_{IL(EN)}$	Digital Voltage Input Low, EN Pin	V_{DDS} = 2.7V to 5.5V V_{DDS} = 1.7V to 2.7V	● ●			0.8 0.25 • V_{DDS}	V V
V_{OH}	Digital Voltage Output High ($\overline{CS}$ and SCK)	V_{DDS} = 3.3V, Sourcing 2mA V_{DDS} = 1.7V, Sourcing 1mA	● ●	V_{DDS} – 0.2 V_{DDS} – 0.25			V V
V_{OL}	Digital Voltage Output Low (MOSI, MISO, $\overline{CS}$, SCK)	V_{DDS} = 3.3V, Sinking 3.3mA V_{DDS} = 1.7V, Sinking 1mA	● ●			0.2 0.2	V V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full specified junction temperature range, otherwise specifications are at T_A = 25°C. V_{DD} = 2.7V to 5.5V, V_{DDS} = 1.7V to 5.5V, R_{BIAS} = 2k to 20k unless otherwise specified. All voltages are with respect to GND.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$I_{LEAK(DIG)}$	Digital Pin Input Leakage Current	PHA, POL, MSTR, SLOW = 0V to V_{DD} $\overline{CS}$, SCK, MOSI, MISO, EN = 0V to V_{DDS}	●			±1	µA
$C_{I/O}$	Input/Output Pin Capacitance	(Note 9)				10	pF
Isolated Pulse Timing (See Figure 2)							
$t_{1/2PW(CS)}$	Chip-Select Half-Pulse Width		●	120	150	180	ns
$t_{INV(CS)}$	Chip-Select Pulse Inversion Delay		●			200	ns
$t_{DEL(CS)}$	Chip-Select Response Delay		●		140	190	ns
$t_{½PW(D)}$	Data Half-Pulse Width		●	40	50	60	ns
$t_{INV(D)}$	Data Pulse Inversion Delay		●			70	ns
$t_{DEL(D)}$	Data Response Delay	(Note 8)	●		75	120	ns
isoSPI™ Timing—Master (See Figures 3, 4)							
t_{CLK}	SCK Latching Edge to SCK Latching Edge	(Note 7) SLOW = 0 SLOW = 1	● ●	1 5			µs µs
t_1	MOSI Setup Time Before SCK Latching Edge	(Note 8)	●	25			ns
t_2	MOSI Hold Time After SCK Latching Edge		●	25			ns
t_3	SCK Low	$t_{CLK} = t_3 + t_4 \geq 1µs$	●	50			ns
t_4	SCK High	$t_{CLK} = t_3 + t_4 \geq 1µs$	●	50			ns
t_5	$\overline{CS}$ Rising Edge to $\overline{CS}$ Falling Edge		●	0.6			µs
t_6	SCK Latching Edge to $\overline{CS}$ Rising Edge	(Note 7)	●	1			µs
t_7	$\overline{CS}$ Falling Edge to SCK Latch Edge	(Note 7)	●	1			µs
t_8	SCK Non-Latch Edge to MISO Valid	(Note 8)	●			55	ns
t_9	SCK Latching Edge to Short ±1 Transmit		●			50	ns
t_{10}	$\overline{CS}$ Transition to Long ±1 Transmit		●			55	ns
t_{11}	$\overline{CS}$ Rising Edge to MISO Rising	(Note 8)	●			55	ns
isoSPI Timing—Slave (See Figures 3, 4)							
t_{12}	isoSPI Data Recognized to SCK Latching Edge	(Note 8) SLOW = 0 SLOW = 1	● ●	110 0.9	145 1.1	185 1.4	ns µs
t_{13}	SCK Pulse Width	SLOW = 0 SLOW = 1	● ●	90 0.9	115 1.1	150 1.4	ns µs
t_{14}	SCK Non-Latch Edge to isoSPI Data Transmit	(Note 8) SLOW = 0 SLOW = 1	● ●	115 0.9	145 1.1	190 1.4	ns µs
t_{15}	$\overline{CS}$ Falling Edge to SCK Non-Latch Edge	PHA = 1 SLOW = 0 SLOW = 1	● ●	90 0.9	120 1.1	160 1.4	ns µs
t_{16}	$\overline{CS}$ Falling Edge to isoSPI Data Transmit	SLOW = 0 SLOW = 1	● ●	200 1.8	265 2.2	345 2.8	ns µs
t_{17}	$\overline{CS}$ Rising Edge to SCK Latching Edge	PHA = 1 SLOW = 0 SLOW = 1	● ●	90 0.9	120 1.1	160 1.4	ns µs
t_{18}	$\overline{CS}$ Rising Edge to MOSI Rising Edge		●			35	ns
t_{RTN}	Data Return Delay	SLOW = 0 SLOW = 1	● ●		485 3.3	625 4	ns µs

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All currents into pins are positive, and all voltages are referenced to GND unless otherwise specified.

Note 3: The LTC6820I is guaranteed to meet specified performance from –40°C to 85°C. The LTC6820H is guaranteed to meet specified performance from –40°C to 125°C.

Note 4: Active supply current (I_{DD}) is dependent on the amount of time that the output drivers are active on IP and IM. During those times I_{DD} will increase by the 20 • I_B drive current. For the maximum data rate 1MHz, the drivers are active approximately 10% of the time if MSTR = 1, and 5%

ELECTRICAL CHARACTERISTICS

of the time if MSTR = 0. See Applications Information section for more detailed information.

Note 5: The IO supply pin, V_{DDS}, provides power for the SPI inputs and outputs, including the EN pin. If the inputs are near 0V or V_{DDS} (to avoid static current in input buffers) and the outputs are not sourcing current, then I_{DDS} includes only leakage current.

Note 6: The LTC6820 is guaranteed to meet specifications with R_{BIAS} resistor values ranging from 2k to 20k, with 1% or better tolerance. Those resistor values correspond to a typical I_B that can range from 0.1mA (for 20k) to 1mA (for 2k).

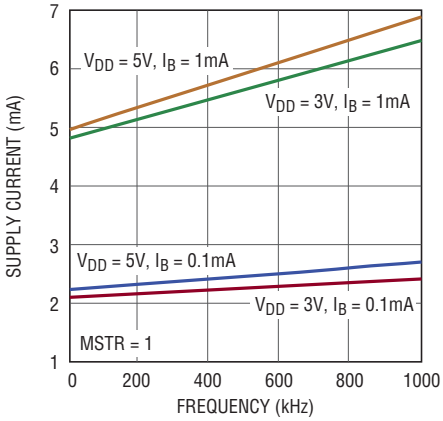
Note 7: These timing specifications are dependent on the delay through the cable, and include allowances for 50ns of delay each direction. 50ns corresponds to 10m of CAT-5 cable (which has a velocity of propagation of 66% the speed of light). Use of longer cables would require derating these specs by the amount of additional delay.

Note 8: These specifications do not include rise or fall time. While fall time (typically 5ns due to the internal pull-down transistor) is not a concern, rising-edge transition time t_{RISE} is dependent on the pull-up resistance and load capacitance. In particular, t_{12} and t_{14} require t_{RISE} < 110ns (if SLOW = 0) for the slave's setup and hold times. Therefore, the recommended time constant is 50ns or less. For example, if the total capacitance on the data pin is 25pF (including self capacitance $C_{I/O}$ of 10pF), the required pull-up resistor value is $R_{PU} \leq 2k\Omega$. If these requirements can't be met, use SLOW = 1.

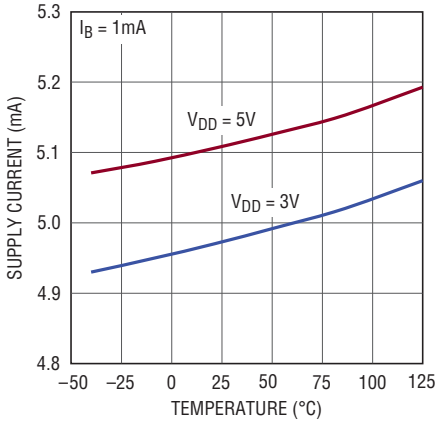
Note 9: Guaranteed by design. Not tested in production.

TYPICAL PERFORMANCE CHARACTERISTICS $V_{DD} = V_{DDS}$, unless otherwise noted.

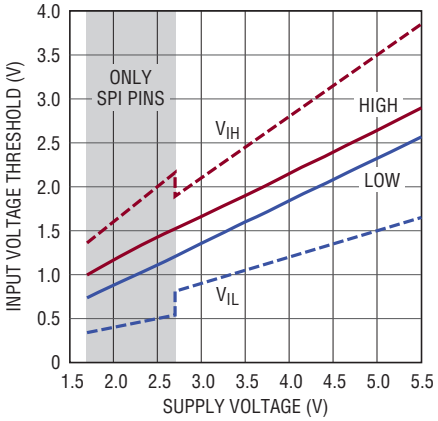
Supply Current (READY/ACTIVE) vs Clock Frequency



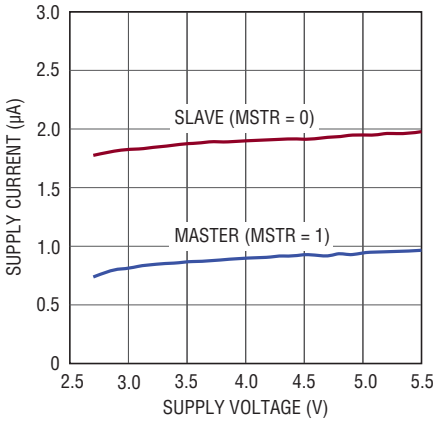
Supply Current (READY) vs Temperature



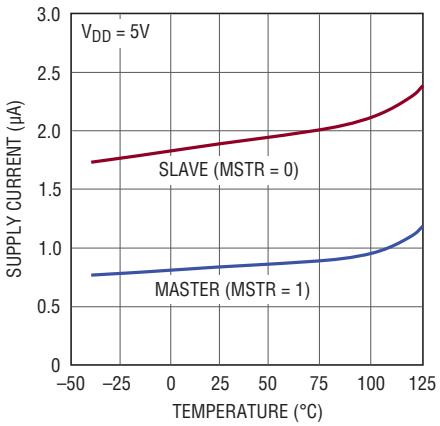
Input Voltage Threshold (Except EN Pin) vs Supply Voltage (V_{DD} or V_{DDS})



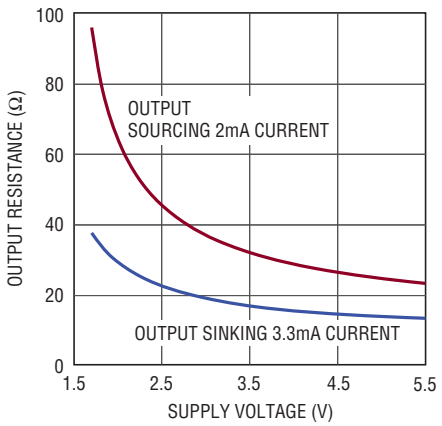
Supply Current (IDLE) vs Supply Voltage



Supply Current (IDLE) vs Temperature

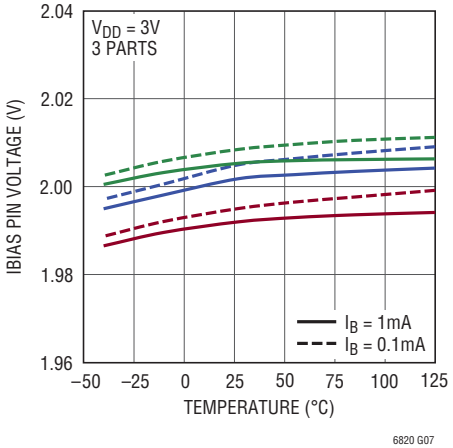


Output Resistance vs Supply Voltage (V_{OH}/V_{OL})

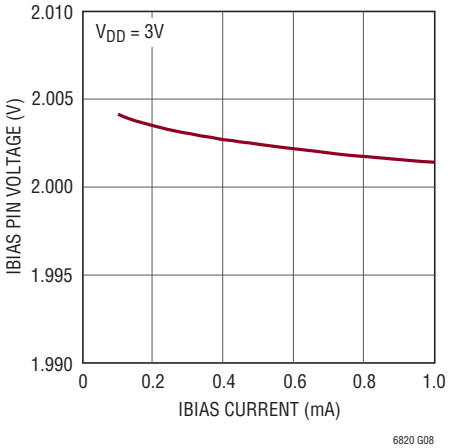


TYPICAL PERFORMANCE CHARACTERISTICS $V_{DD} = V_{DDS}$, unless otherwise noted.

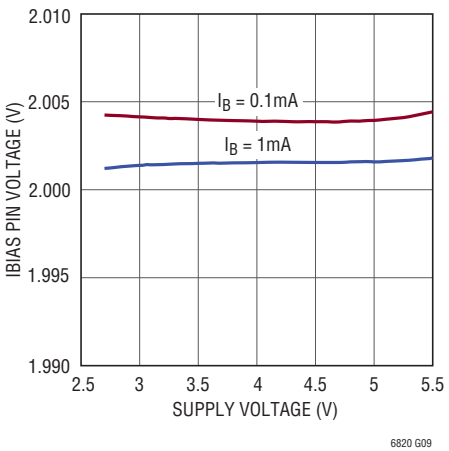
IBIAS Voltage vs Temperature



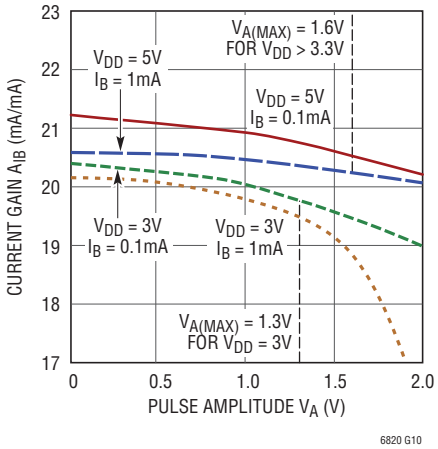
IBIAS Voltage Load Regulation



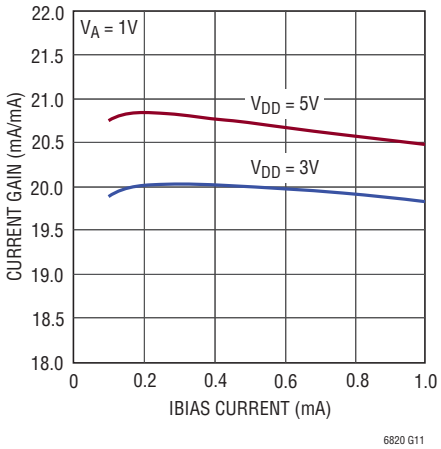
IBIAS Voltage vs Supply Voltage



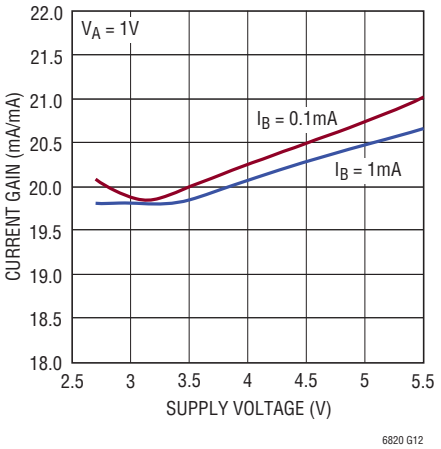
Driver Current Gain vs Amplitude



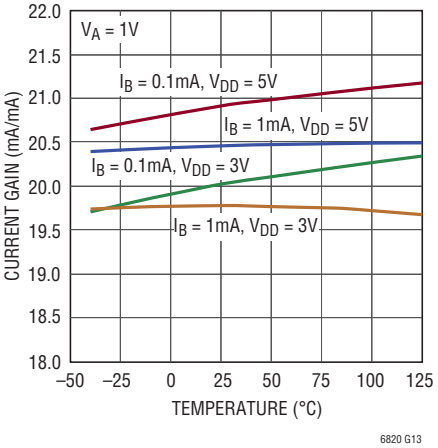
Driver Current Gain vs IBIAS Current (I_B)



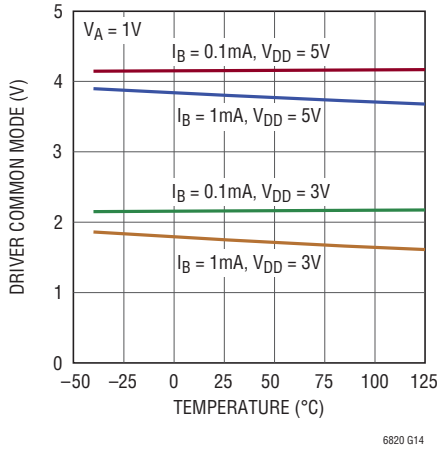
Driver Current Gain vs Supply Voltage



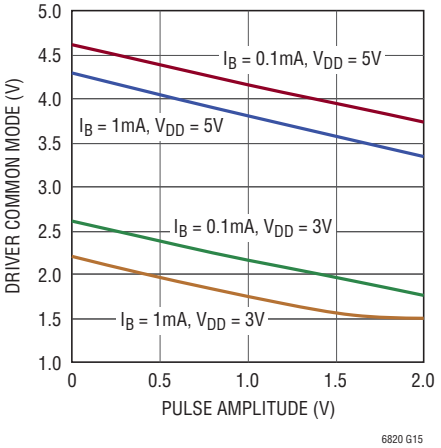
Driver Current Gain vs Temperature



Driver Common Mode Voltage vs Temperature

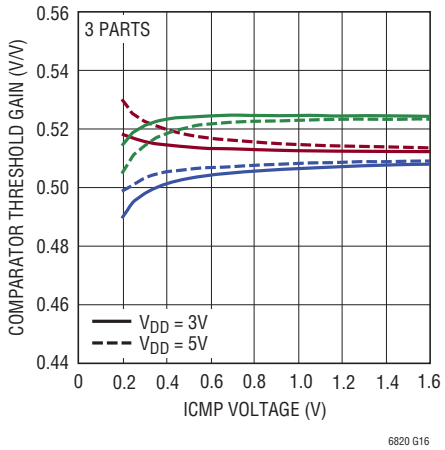


Driver Common Mode Voltage vs Pulse Amplitude

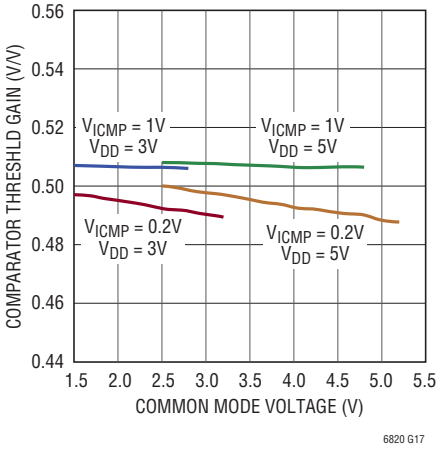


TYPICAL PERFORMANCE CHARACTERISTICS $V_{DD} = V_{DDS}$, unless otherwise noted.

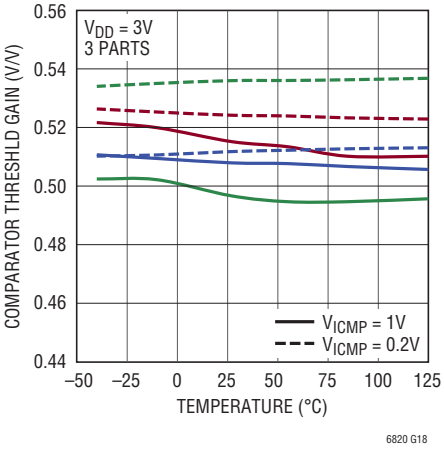
Comparator Threshold Gain vs ICMP Voltage



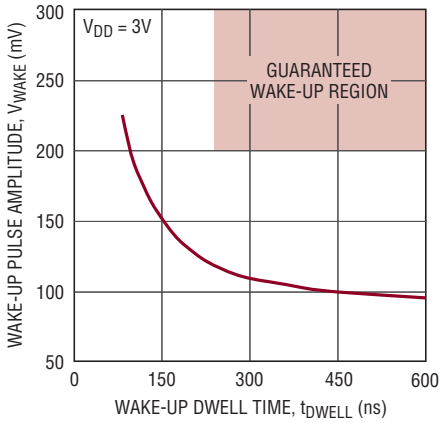
Comparator Threshold Gain vs Common Mode



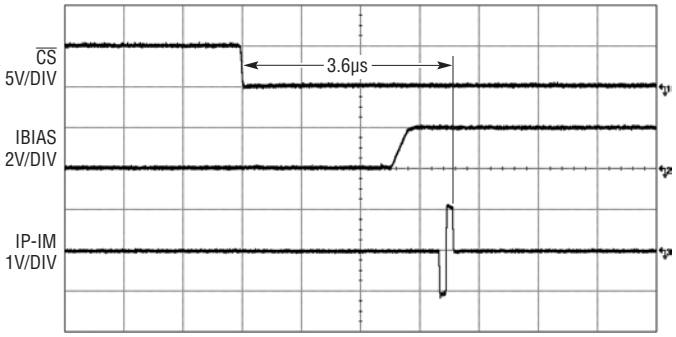
Comparator Threshold Gain vs Temperature



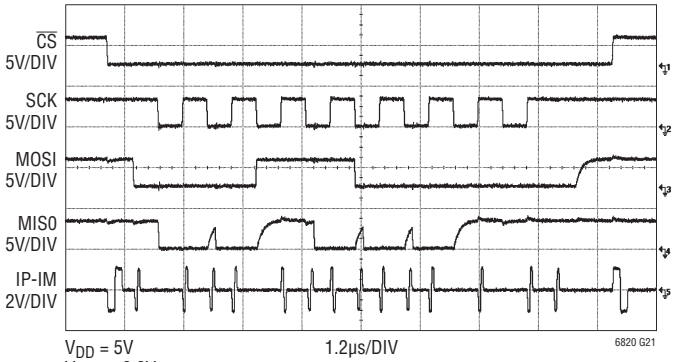
Wake-Up Pulse Amplitude vs Dwell Time



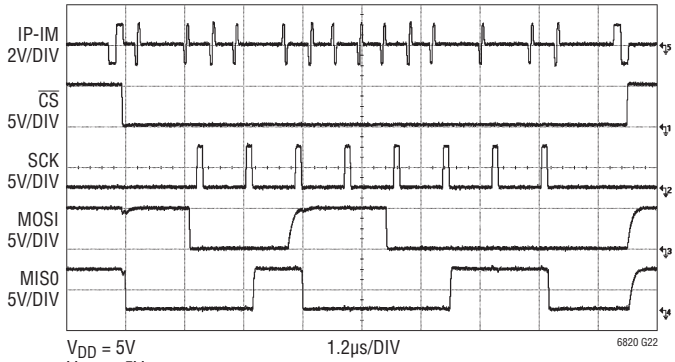
Start-Up Time



SPI Signal and isoSPI Pulses, MSTR = 1



SPI Signal and isoSPI Pulses, MSTR = 0



PIN FUNCTIONS (QFN/MSOP)

MOSI (Pin 1/Pin 2): SPI Master Out/Slave In Data. If connected on the master side of a SPI interface (MSTR pin high), this pin receives the data signal output from the master SPI controller. If connected on the slave side of the interface (MSTR pin low), this pin drives the data signal input to the slave SPI device. The output is open drain, so an external pull-up resistor to V_{DDS} is required.

MISO (Pin 2/Pin 3): SPI Master In/Slave Out Data. If connected on the master side of a SPI interface (MSTR pin high), this pin drives the data signal input to the master SPI controller. If connected on the slave side of the interface (MSTR pin low), this pin receives the data signal output from the slave SPI device. The output is open drain, so an external pull-up resistor to V_{DDS} is required.

SCK (Pin 3/Pin 4): SPI Clock Input/Output. If connected on the master side of the interface (MSTR pin high), this pin receives the clock signal from the master SPI controller. This input should not be pulled above V_{DDS}. If connected on the slave side of the interface (MSTR pin low), this pin outputs the clock signal to the slave device. The output driver is push-pull; no external pull-up resistor is needed.

$\overline{CS}$ (Pin 4/Pin 5): SPI Chip Select Input/Output. If connected on the master side of the interface (MSTR pin high), this pin receives the chip select signal from the master SPI controller. This input should not be pulled above V_{DDS}. If connected on the slave side of the interface (MSTR pin low), this pin outputs the chip select signal to the slave device. The output driver is push-pull; no external pull-up resistor is needed.

V_{DDS} (Pin 5/Pin 6): SPI Input/Output Power Supply Input. The output drivers for the SCK and $\overline{CS}$ pins use the V_{DDS} input as their positive power supply. The input threshold voltages of SCK, $\overline{CS}$, MOSI, MISO and EN are determined by V_{DDS}. May be tied to V_{DD} or to a supply above or below V_{DD} to level shift the SPI I/O. If separate from V_{DD}, connect a bypass capacitor of at least 0.01µF directly between V_{DDS} and GND.

POL (Pin 6/Pin 7): SPI Clock Polarity Input. Tie to V_{DD} or GND. See Operation section for details.

PHA (Pin 7/Pin 8): SPI Clock Phase Input. Tie to V_{DD} or GND. See Operation section for details.

V_{DD} (Pin 8/Pin 9): Device Power Supply Input. Connect a bypass capacitor of at least 0.01µF directly between V_{DD} and GND.

IM (Pin 9/Pin 10): Isolated Interface Minus Input/Output.

IP (Pin 10/Pin 11): Isolated Interface Plus Input/Output.

MSTR (Pin 11/Pin 12): Serial Interface Master/Slave Selector Input. Tie this pin to V_{DD} if the device is on the master side of the isolated interface. Tie this pin to GND if the device is on the slave side of the isolated interface.

SLOW (Pin 12/Pin 13): Slow Interface Selection Input. For clock frequencies at or below 200kHz, or if slave devices cannot meet timing requirements, this pin should be tied to V_{DD}. For clock frequencies above 200kHz, this pin should be tied to GND.

GND (Pin 13/Pin 14): Device Ground.

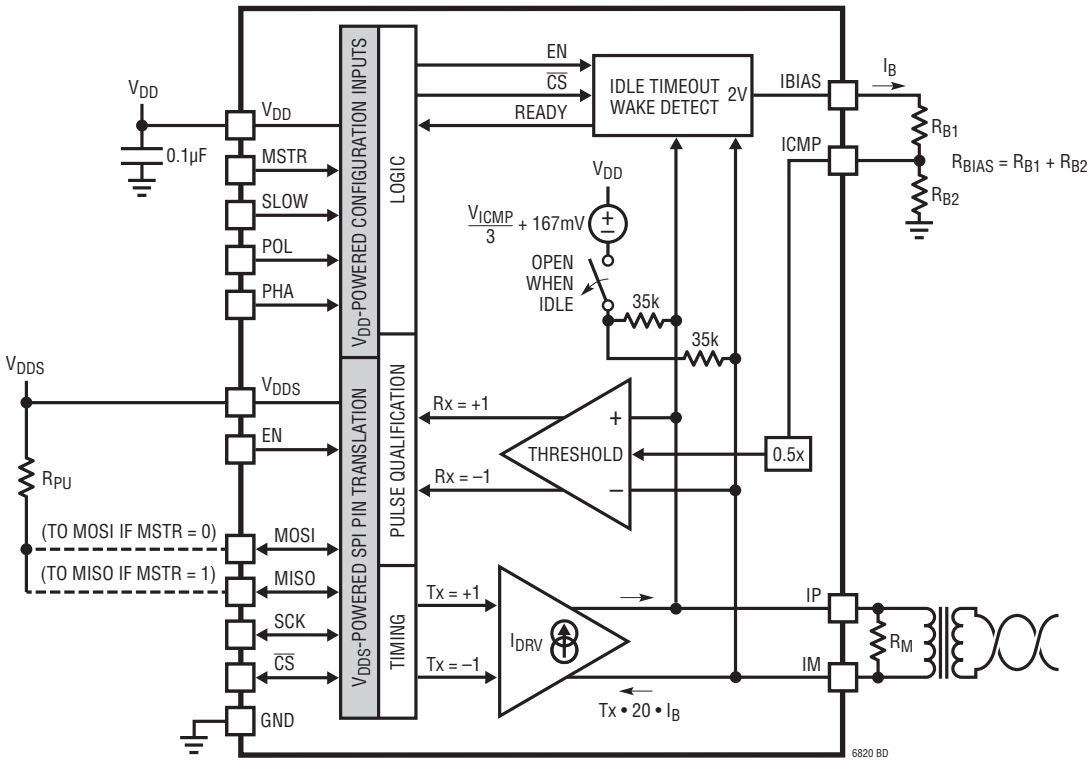
ICMP (Pin 14/Pin 15): Isolated Interface Comparator Voltage Threshold Set. Tie this pin to the resistor divider between IBIAS and GND to set the voltage threshold of the interface receiver comparators. The comparator thresholds are set to 1/2 the voltage on the ICMP pin.

IBIAS (Pin 15/Pin 16): Isolated Interface Current Bias. Tie IBIAS to GND through a resistor divider to set the interface output current level. When the device is enabled, this pin is approximately 2V. When transmitting pulses, the sink current on each of the IP and IM pins is set to 20 times the current sourced from pin IBIAS to GND. Limit the capacitance on the IBIAS pin to less than 50pF to maintain the stability of the feedback circuit regulating the IBIAS voltage.

EN (Pin 16/Pin 1): Device Enable Input. If high, this pin forces the LTC6820 to stay enabled, overriding the internal IDLE mode function. If low, the LTC6820 will go into IDLE mode after the $\overline{CS}$ pin has been high for 5.7ms (when MSTR pin is high) or after no signal on the IP/IM pins for 5.7ms (when MSTR pin is low). The LTC6820 will wake-up less than 8µs after $\overline{CS}$ falls (MSTR high) or after a signal is detected on IP/IM (MSTR low).

Exposed Pad (Pin 17, QFN Package Only): Exposed pad may be left open or connected to device GND.

BLOCK DIAGRAM



OPERATION

The LTC6820 creates a bidirectional isolated serial port interface (isoSPI) over a single twisted pair of wires, with increased safety and noise immunity over a nonisolated interface. Using transformers, the LTC6820 translates standard SPI signals ($\overline{CS}$, SCK, MOSI and MISO) into pulses that can be sent back and forth on twisted-pair cables.

A typical system uses two LTC6820 devices. The first is paired with a microcontroller or other SPI master. Its IP and IM transmitter/receiver pins are connected across an isolation barrier to a second LTC6820 that reproduces the SPI signals for use by one or more slave devices.

The transmitter is a current-regulated differential driver. The voltage amplitude is determined by the drive current and the equivalent resistive load (cable characteristic impedance and termination resistor, R_M).

The receiver consists of a window comparator with a differential voltage threshold, V_{TCMP}. When $V_{IP} – V_{IM}$ is greater than $+V_{TCMP}$, the comparator detects a logic +1. When $V_{IP} – V_{IM}$ is less than $–V_{TCMP}$, the comparator detects a logic –1. A logic 0 (null) indicates $V_{IP} – V_{IM}$ is between the positive and negative thresholds.

The comparator outputs are sent to pulse timers (filters) that discriminate between short and long pulses.

Selecting Bias Resistors

The adjustable signal amplitude allows the system to trade power consumption for communication robustness, and the adjustable comparator threshold allows the system to account for signal losses.

OPERATION

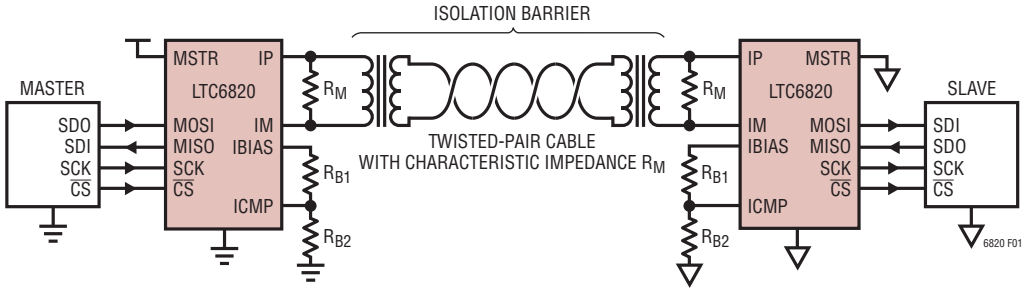


Figure 1. Typical System Using Two LTC6820 Devices

The transmitter drive current and comparator voltage threshold are set by a resistor divider ($R_{BIAS} = R_{B1} + R_{B2}$) between the IBIAS pin and GND, with the divided voltage tied to the ICMP pin. When the LTC6820 is enabled (not IDLE), I_{BIAS} is held at 2V, causing a current, I_B, to flow out of the IBIAS pin. The IP and IM pin drive currents are 20 • I_B. The comparator threshold is half the voltage on the ICMP pin (V_{ICMP}).

As an example, if divider resistor R_{B1} is 1.21k and resistor R_{B2} is 787Ω (so that R_{BIAS} = 2k), then:

$$I_B = \frac{2V}{R_{B1}+R_{B2}} = 1mA$$

$I_{DRV} = I_{IP} = I_{IM} = 20 \bullet I_B = 20mA$

$$V_{ICMP} = 2V \bullet \frac{R_{B2}}{R_{B1}+R_{B2}} = I_B \bullet R_{B2} = 788mV$$

$V_{TCMP} = 0.5 \bullet V_{ICMP} = 394mV$

In this example, the pulse drive current I_{DRV} will be 20mA, and the receiver comparators will detect pulses with IP-IM amplitudes greater than ±394mV.

If the isolation barrier uses 1:1 transformers connected by a twisted pair and terminated with 100Ω resistors on each end, then the transmitted differential signal amplitude (±) will be:

$$V_A = I_{DRV} \bullet \frac{R_M}{2} = 1V$$

(This result ignores transformer and cable losses, which will reduce the amplitude).

isoSPI Pulse Detail

The isoSPI transmitter can generate three voltage levels: $+V_A$, 0V, and $-V_A$. To eliminate the DC signal component and enhance reliability, isoSPI pulses are defined as symmetric pulse pairs. A +1 pulse pair is defined as a $+V_A$ pulse followed by a $-V_A$ pulse. A –1 pulse pair is $-V_A$ followed by $+V_A$.

The duration of each pulse is defined as $t_{1/2PW}$. (The total isoSPI pulse duration is 2 • $t_{1/2PW}$). The LTC6820 allows for two different $t_{1/2PW}$ values so that four types of pulses can be transmitted, as listed in Table 1.

Table 1. isoSPI Pulse Types

PULSE TYPE	FIRST LEVEL	SECOND LEVEL	ENDING LEVEL
Long +1	$+V_A$ (150ns)	$-V_A$ (150ns)	0V
Long –1	$-V_A$ (150ns)	$+V_A$ (150ns)	0V
Short +1	$+V_A$ (50ns)	$-V_A$ (50ns)	0V
Short –1	$-V_A$ (50ns)	$+V_A$ (50ns)	0V

Long pulses are used to transmit $\overline{CS}$ changes. Short pulses transmit data (MOSI or MISO). An LTC6820 detects four types of communication events from the SPI master: $\overline{CS}$ falling, $\overline{CS}$ rising, SCK latching MOSI = 0, and SCK latching MOSI = 1. It converts each event into one of the four pulse types, as shown in Table 2.

Table 2. Master Communication Events

SPI MASTER EVENT	TRANSMITTED PULSE
$\overline{CS}$ Rising	Long +1
$\overline{CS}$ Falling	Long –1
SCK Latching Edge, MOSI = 1	Short +1
SCK Latching Edge, MOSI = 0	Short –1

OPERATION

On the other side of the isolation barrier (i.e., the other end of the cable) another LTC6820 is configured to interface with a SPI slave. It receives the transmitted pulses and reconstructs the SPI signals on its output port, as shown in Table 3. In addition, the slave device may transmit a return data pulse to the master to set the state of MISO. See isoSPI Interaction and Timing for additional details.

Table 3. Slave SPI Port Output

RECEIVED PULSE	SPI PORT ACTION	RETURN PULSE
Long +1	Drive $\overline{CS}$ High	None
Long –1	Drive $\overline{CS}$ Low	Short –1 Pulse if MISO = 0 (No Return Pulse if MISO = 1)
Short +1	1. Set MOSI = 1 2. Pulse SCK	
Short –1	1. Set MOSI = 0 2. Pulse SCK	

A slave LTC6820 never transmits long ($\overline{CS}$) pulses. Furthermore, a slave will only transmit a short –1 pulse (when MISO = 0), never a +1 pulse. This allows for multiple slave devices on a single cable without risk of collisions (see Multidrop section).

isoSPI Pulse Specifications

Figure 2 details the timing specifications for the +1 and –1 isoSPI pulses. The same timing specifications apply to either version of these symmetric pulses. In the Electrical Characteristics table, these specifications are further separated into $\overline{CS}$ (long) and Data (short) parameters.

A valid pulse must meet the minimum spec for $t_{1/2PW}$ and the maximum spec for t_{INV}. In other words, the half-pulse width must be long enough to pass through the appropriate pulse timer, but short enough for the inversion to begin within the valid window of time.

The response observed at MOSI, MISO or $\overline{CS}$ will occur after delay t_{DEL} from the pulse inversion.

Setting Clock Phase and Polarity (PHA and POL)

SPI devices often use one clock edge to latch data and the other edge to shift data. This avoids timing problems associated with clock skew. There is no standard to specify whether the shift or latch occurs first. There is also no requirement for data to be latched on a rising or falling clock edge, although latching on the rising edge is most common. The LTC6820 supports all four SPI operating modes, as configured by the PHA and POL Pins.

Table 4. SPI Modes

MODE	POL	PHA	DESCRIPTION
0	0	0	SCK Idles Low, Latches on Rising (1st) Edge
1	0	1	SCK Idles Low, Latches on Falling (2nd) Edge
2	1	0	SCK Idles High, Latches on Falling (1st) Edge
3	1	1	SCK Idles High, Latches on Rising (2nd) Edge

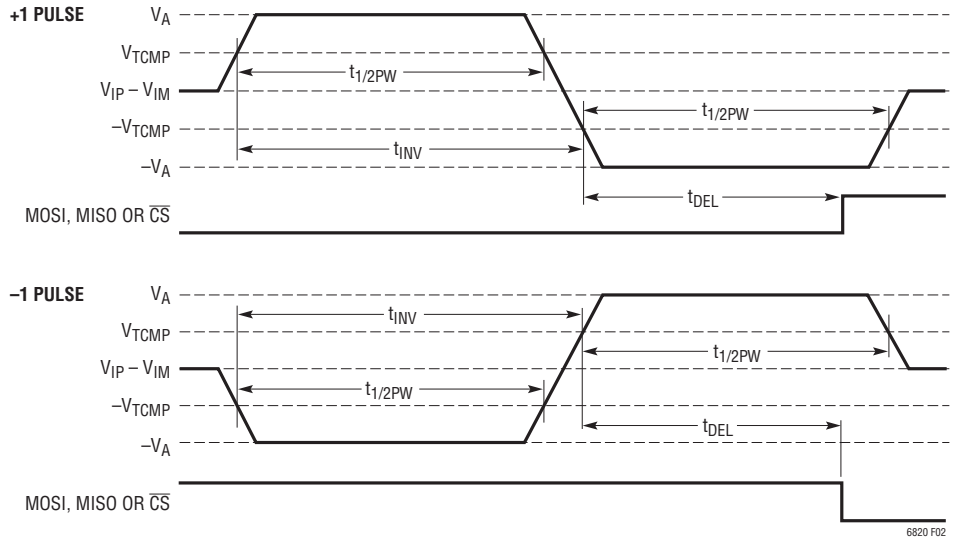


Figure 2. isoSPI Differential Pulse Detail

OPERATION

If POL = 0, SCK idles low. Data is latched on the rising (first) clock edge if PHA = 0 and on the falling (second) clock edge if PHA = 1.

If POL =1, SCK idles high. Data is latched on the falling (first) clock edge if PHA = 0 and on the rising (second) clock edge if PHA = 1.

The two most common configurations are mode 0 (PHA = 0 and POL = 0) and mode 3 (PHA = 1 and POL = 1) because these modes latch data on a rising clock edge.

isoSPI Interaction and Timing

The timing diagrams in Figures 3 and 4 show how an isoSPI in master mode (connected to a SPI master) interacts with an isoSPI in slave mode (connected to a SPI slave). Figure 3 details operation with PHA = 0 (and shows SCK signals for POL = 0 or 1). Figure 4 provides the timing diagram for PHA = 1. Although not shown, it is acceptable to use different SPI modes (PHA and POL settings) on the master and slave devices.

A master SPI device initiates communication by lowering $\overline{CS}$. The LTC6820 converts this transition into a Long –1 pulse on its IP/IM pins. The pulse traverses the isolation barrier (with an associated cable delay) and arrives at the IP/IM pins of the slave LTC6820. Once validated, the Long –1 pulse is converted back into a falling $\overline{CS}$ transition, this time supplied to the slave SPI device. If slave PHA = 1, SCK will also leave the idle state at this time.

Before the master SPI device supplies the first latching clock edge (usually a rising edge, but see Table 4 for exceptions), the slave LTC6820 must transmit the initial slave data bit S_N, which it determines by sampling the state of MISO after a suitable delay.

If MISO = 0, the slave will transmit a Short –1 pulse to the master. The master LTC6820 will receive and decode the pulse and set the master MISO = 0 (matching the slave). However, *if the slave MISO=1, the slave does not transmit a pulse.* The master will interpret this null response as a 1 and set the master MISO = 1. This makes it possible to connect multiple slave LTC6820's to a single cable with no conflicting signals (see Multidrop section).

After the falling $\overline{CS}$ sequence, every latching clock edge on the master converts the state of the MOSI pin into an isoSPI data pulse ($M_N, M_{N-1}, \ldots M_0$) while simultaneously latching the slave's data bit. As the slave LTC6820 receives each data bit it will set the slave MOSI pin to the proper state and then generate an SCK pulse before returning the slave's MISO data (either as a Short –1 pulse, or as a null).

At the end of communication, the final data bit sent by the slave (either as a pulse or null) will be ignored by the master controller. (The slave LTC6820 must return a data bit since it cannot predict when communications will cease.) The master SPI device can then raise $\overline{CS}$, which is transmitted to the slave in the form of a Long +1 pulse. The process ends with the slave LTC6820 transitioning $\overline{CS}$ high, and returning SCK to the idle state if PHA = 1.

Rise Time

MOSI and MISO outputs have open-drain drivers. The rise time t_{RISE} for the data output is determined by the pull-up resistance and load capacitance. R_{PU} must be small enough to provide adequate setup and hold times.

Slow Mode

When configured for slave operation, the LTC6820 provides two operating modes to ensure compatibility with a wide range of SPI timing scenarios. These modes are referred to as fast and slow mode, and are set using the SLOW pin. When configured for master operation, the SLOW pin setting has no effect on the LTC6820 operation. In this case, it is recommended to tie the SLOW pin to GND.

In fast mode (SLOW pin tied to GND), the LTC6820 can operate at clock rates up to 1MHz (t_{CLK} = 1µs). However, some SPI slave devices can't respond quickly enough to support this data rate. Fast mode requires a slave to operate with setup and response times of 100ns, as well as 100ns clock widths. In addition, allowances must be made for the RC rise time of MOSI and MISO's open-drain outputs. In slow mode (SLOW pin tied to V^+), the timing requirement are relaxed at the expense of maximum data rate. As indicated in the Electrical Characteristics, the clock pulses and required setup and response times are increased to 0.9µs minimum. Accordingly, the minimum t_{CLK} (controlled by the master) must be limited to 5µs. The SLOW pin setting has no effect on the master LTC6820 (with MSTR = 1).

OPERATION

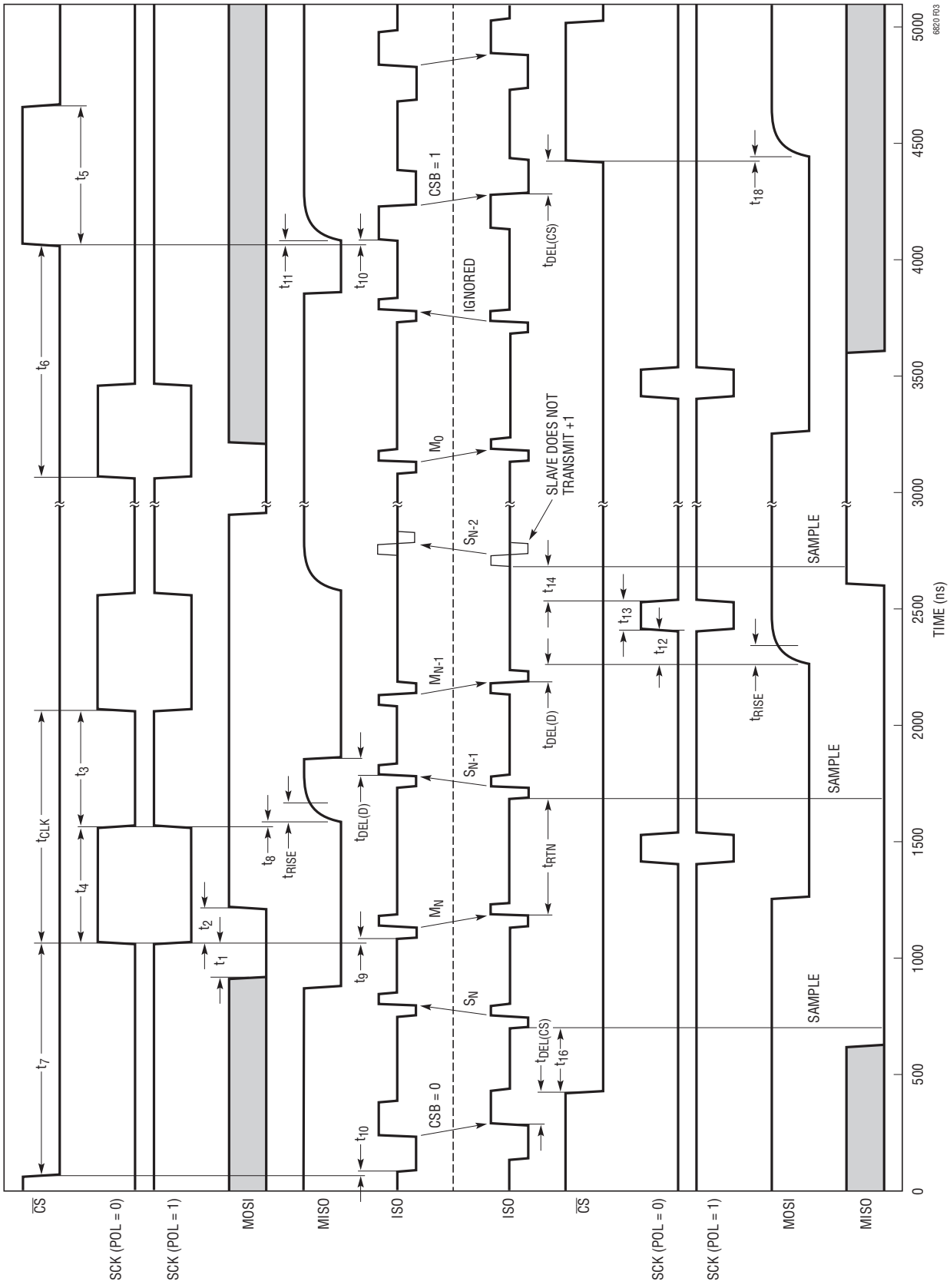


Figure 3. Transceiver Timing Diagram (PHA = 0)

OPERATION

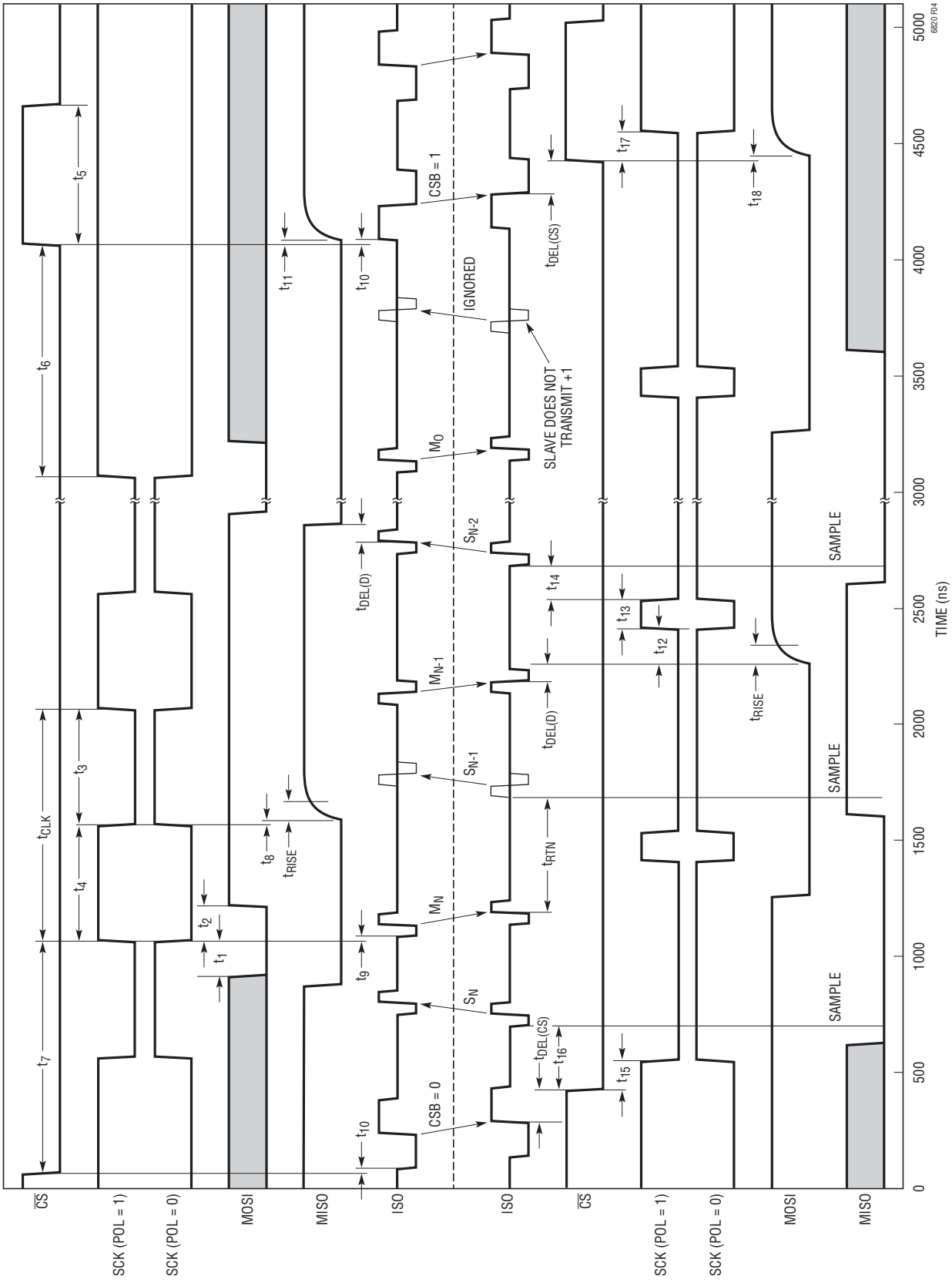


Figure 4. Transceiver Timing Diagram (PHA = 1)

OPERATION

Figure 6 demonstrates slow mode, as compared to fast mode in Figure 5.

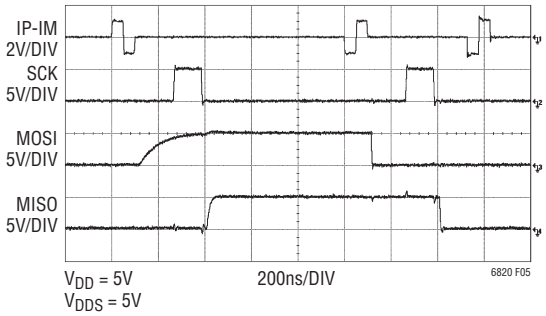


Figure 5. Fast Mode (SLOW = 0)

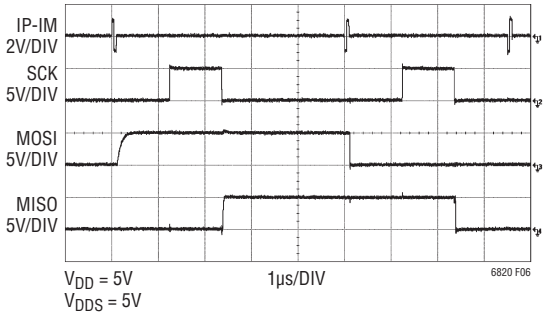


Figure 6. Slow Mode (SLOW = 1)

IP and IM Pulse Driver

The IP and IM pins transmit and receive the isoSPI pulses. The transmitter uses a current-regulated driver (see Figure 7) to establish the pulse amplitude, as determined by the IBIAS pin current, I_B, and the load resistance. The sinking current source is regulated to 20x the bias current I_B. The sourcing current source operates in a current-starved (resistive) manner to maintain the sourcing pin's voltage near V_{DD}, as shown in Figures 8 and 9. The common mode voltage (while driving) is dependent on bias current and output amplitude.

The output driver will regulate the common mode and peak swing of IP and IM to the proper levels, allowing for a broad range of output amplitude with fairly flat gain, as shown in Figure 10.

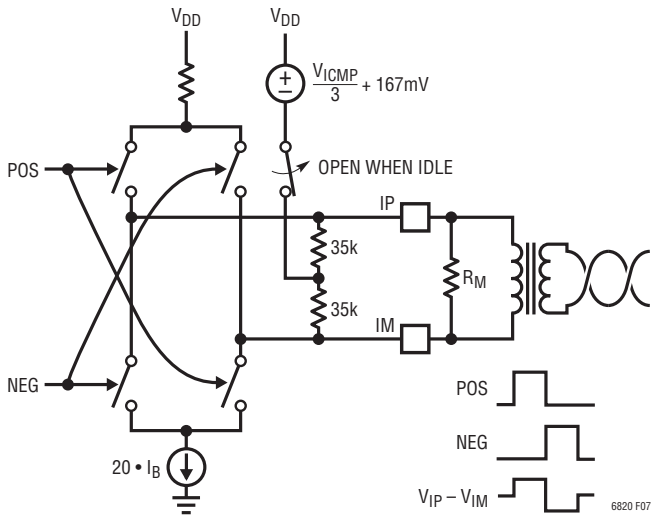


Figure 7. Pulse Driver

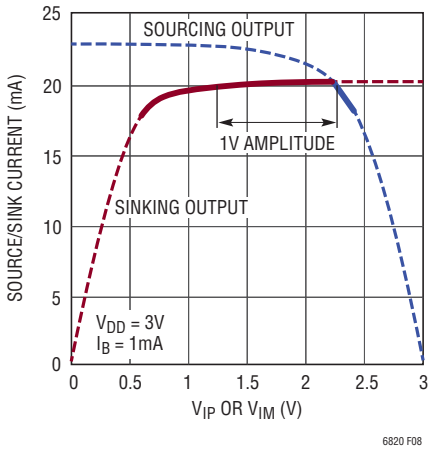


Figure 8. Drive Source/Sink vs Output Voltage

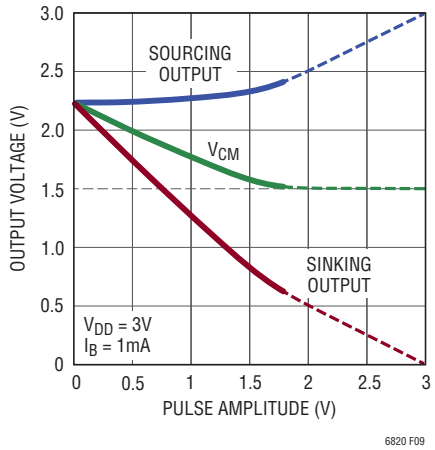


Figure 9. Output Voltages and Common Mode vs Amplitude

OPERATION

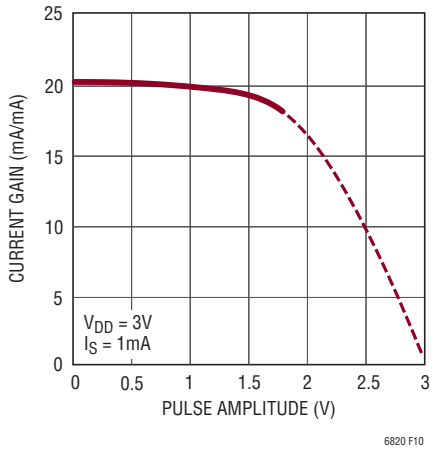


Figure 10. A_{IB} Current Gain vs Amplitude

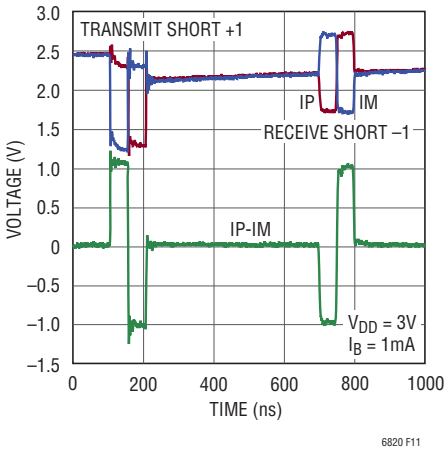


Figure 11. Transmitting and Receiving Data

This type of driver does not require a center-tapped transformer, but such a transformer may improve noise immunity, especially if it has a common mode choke. See the Applications Information section for additional details.

Receiver Common Mode Bias

When not transmitting, the output driver maintains IP and IM near V_{DD} with a pair of 35k (R_{IN}) resistors to a voltage of $V_{DD} – V_{ICMP}/3 – 167mV$. This weak bias network holds the outputs near their desired operating point without significantly loading the cable, which allows a large number of LTC6820's to be paralleled without affecting signal amplitude.

Figure 11 shows the differential and single-ended IP and IM signals while transmitting and receiving data. The driver forces the common mode voltage it needs while transmitting, then it returns to the bias level with a time constant of $R_{IN} • C_{LOAD}/2$, where C_{LOAD} is the sum of the capacitance at the IP and IM pins.

When the LTC6820 is in low power IDLE mode, the bias voltage is disconnected from the 35k resistors, resulting in a 70k differential load.

State Diagram

During periods of no communication, a low current IDLE (or shutdown) state is available to reduce power. In the IDLE state the LTC6820 shuts down most of the circuitry. A slave device uses a low current comparator to monitor for activity, so it has larger IDLE current.

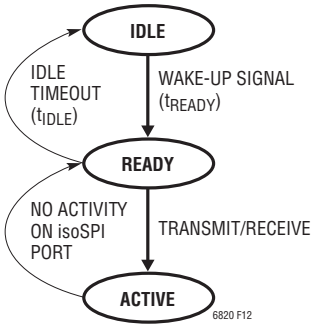


Figure 12. State Diagram

In the READY state all circuitry is enabled and ready to transmit or receive, but is not actively transmitting on IP and IM.

Supply current increases when actively communicating, so this condition is referred to as the ACTIVE state.

Supply Current

Table 5 provides equations for estimating I_{DD} in each state. The results are for average supply current (as opposed to peak currents), and make the assumption that a slave is returning an equal number of 0s and 1s (significant because the slave doesn't generate +1 data pulses, so the average driver current is smaller).

OPERATION

Table 5. I_{DD} Equations

STATE	MSTR	ESTIMATED I_{DD}
IDLE	0 (slave)	2µA
	1 (master)	1µA
READY	0 or 1	$1.7mA + 3 \bullet I_B$
ACTIVE	0 (slave)	$2mA + \left(3 + 20 \bullet \frac{100ns \bullet 0.5}{t_{CLK}}\right) \bullet I_B$
	1 (master)	$2mA + \left(3 + 20 \bullet \frac{100ns}{t_{CLK}}\right) \bullet I_B$

IDLE Mode and Wake-Up Detection

To conserve power, an LTC6820 in slave mode (MSTR = 0) will enter an IDLE state after 5.7ms (t_{IDLE}) of inactivity on the IP/IM pins. In this condition I_{DD} is reduced to less than 6µA and the SPI pins are idled ($\overline{CS}$ = 1, MOSI = 1 and SCK = POL).

The LTC6820 will continue monitoring the IP and IM pins using a low power AC-coupled detector. It will wake up when it sees a differential signal of 240mV or greater that persists for 240ns or longer. In practice, a long ($\overline{CS}$) isoSPI pulse is sufficient to wake the device up. Once the comparator generates the wake-up signal it can take up to 8µs (t_{READY}) for bias circuits to stabilize.

Figure 14 details the sequence of waking up a slave LTC6820 (placing it in the READY state), using it to communicate, then allowing it to return to the low power IDLE state.

A LTC6820 in master mode (MSTR = 1) doesn't use the wake-up detection comparator. A falling edge on $\overline{CS}$ will enable the isoSPI port within t_{READY}, and the LTC6820 will transmit a long ($\overline{CS}$) pulse as it leaves the IDLE state. (The polarity of the pulse matches the $\overline{CS}$ state at the end of t_{READY}).

The master LTC6820 will remain in the READY/ACTIVE state as long as $\overline{CS}$ = 0. If $\overline{CS}$ transitions high and EN = 0 it will enter the IDLE state, but not until t_{IDLE} expires. This prevents the device from shutting down between data packets.

In either master or slave mode the IDLE feature may be disabled by driving EN high. This forces the device to remain "ready" at all times.

Figure 15 demonstrates a simple procedure for waking a master (MSTR = 1) LTC6820 and its connected slave (MSTR = 0). A negative edge on $\overline{CS}$ causes the master to drive IBIAS to 2V and, after a short delay, transmit a long +1 pulse. (If $\overline{CS}$ remains low throughout t_{READY}, the LTC6820 would first generate a –1 pulse, then the +1 pulse when $\overline{CS}$ returns high). The long pulse serves as a wake-up signal for the slave device, which responds by driving its IBIAS pin to 2V and entering the READY state.

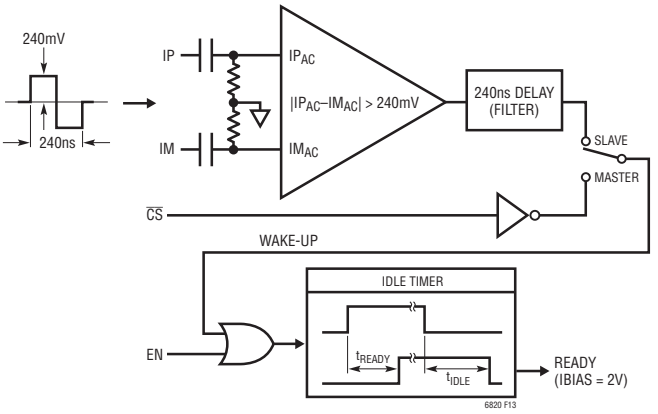


Figure 13. Wake-Up Detection and IDLE Timer

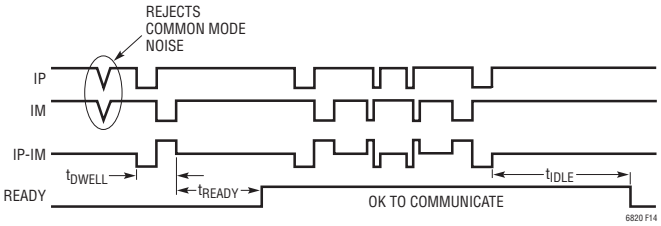


Figure 14. Slave LTC6820 Wake-Up/Idle Timing

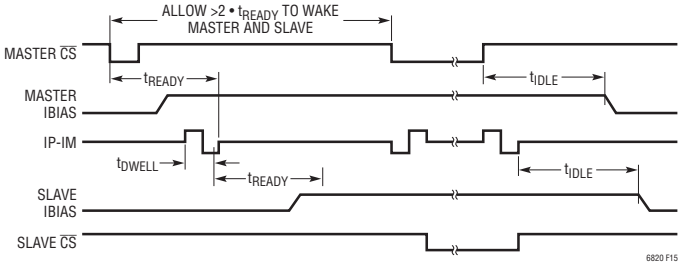


Figure 15. Master and Slave Wake-Up/Idle Sequence

OPERATION

Multidrop

Multiple slaves can be connected to a single master by connecting them in parallel (multidrop configuration)along one cable. As shown in Figure 16, the cable should be terminated only at the beginning (master) and the end. In between, the additional LTC6820's and their associated slave devices will be connected to "stubs" on the cable. These stubs should be kept short, with as little capacitance as possible, to avoid degrading the termination along the cable.

The multidrop scheme is only possible if the SPI slaves have certain characteristics:

- The SPI slaves must be addressable, because they will all see the same $\overline{CS}$ signal (as decoded by each slave LTC6820).
- When not addressed, the slave SDO must remain high.

When a slave is not addressed, its LTC6820 will not transmit data pulses as long as MISO (the SPI device's SDO) remains high. This eliminates the possibility for collisions, as only the addressed slave device will ever be returning data to the master.

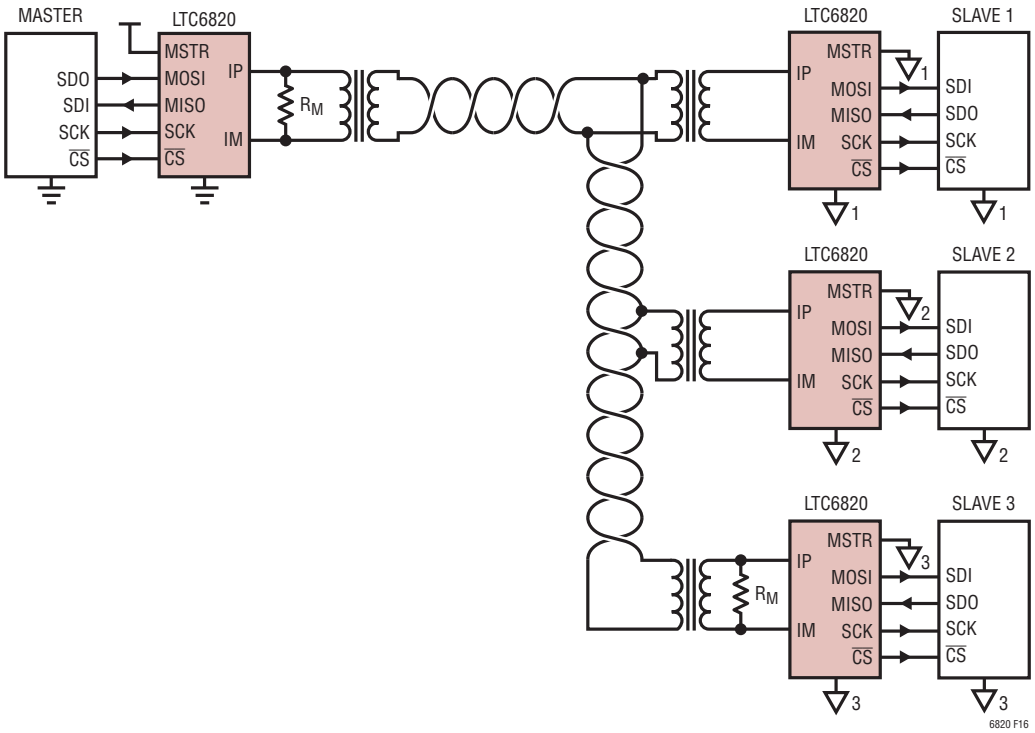


Figure 16. Multidropping Multiple Slaves on a Single Cable

APPLICATIONS INFORMATION

isoSPI Setup

The LTC6820 allows each application to be optimized for power consumption or for noise immunity. The power and noise immunity of an isoSPI system is determined by the programmed I_B current. The I_B current can range from 0.1mA to 1mA. A low I_B reduces the isoSPI power consumption in the READY and ACTIVE states, while a high I_B increases the amplitude of the differential signal voltage V_A across the matching termination resistor, R_M.

I_B is programmed by the sum of the R_{B1} and R_{B2} resistors connected between the I_{BIAS} pin and GND. For most applications setting I_B to 0.5mA is a good compromise between power consumption and noise immunity. Using this I_B setting with a 1:1 transformer and $R_M = 120\Omega$, R_{B1} should be set to 2.8k and R_{B2} set to 1.2k. In a typical CAT5 twisted pair these settings will allow for communication up to 50m.

For applications that require cables longer than 50m it is recommended to increase the amplitude V_A by increasing I_B to 1mA. This compensates for the increased insertion loss in the cable and maintains high noise immunity. So when using cables over 50m and, again, using a transformer with a 1:1 turns ratio and $R_M = 120\Omega$, R_{B1} would be 1.4k and R_{B2} would be 600Ω.

Other I_B settings can be used to reduce power consumption or increase the noise immunity as required by the application. In these cases when setting V_{ICMP} and choosing R_{B1} and R_{B2} resistor values the following rules should be used:

For cables 50 meters or less:

$I_B = 0.5mA$

$V_A = (20 \bullet I_B) \bullet (R_M/2)$

$V_{TCMP} = 1/2 \bullet V_A$

$V_{ICMP} = 2 \bullet V_{TCMP}$

$R_{B2} = V_{ICMP}/I_B$

$$R_{B1} = \left(\frac{2V}{I_B}\right) - R_{B2}$$

For cables over 50 meters:

$I_B = 1mA$

$V_A = (20 \bullet I_B) \bullet (R_M/2)$

$V_{TCMP} = 1/4 \bullet V_A$

$V_{ICMP} = 2 \bullet V_{TCMP}$

$R_{B2} = V_{ICMP}/I_B$

$$R_{B1} = \left(\frac{2V}{I_B}\right) - R_{B2}$$

The maximum data rate of an isoSPI link is determined by the length of the cable used. For cables 10 meters or less the maximum 1MHz SPI clock frequency is possible. As the length of the cable increases the maximum possible SPI clock rate decreases. This is a result of the increased propagation delays through the cable creating possible timing violations.

Cable delay affects three timing specifications, t_{CLK}, t_6, and t_7. In the Electrical Characteristics table, each is derated by 100ns to allow for 50ns of cable delay. For longer cables, the minimum timing parameters may be calculated as shown below:

t_{CLK}, t_6, and $t_7 > 0.9\mu s + 2 \bullet t_{CABLE}$

Pull-Up Resistance Considerations

The data output (MOSI if MSTR = 0, MISO if MSTR = 1) requires a pull-up resistor, R_{PU}. The rise time t_{RISE} is determined by R_{PU} and the capacitance on the pin. R_{PU} must be small enough to provide adequate setup and hold times. For a slave device, the time constant must be less than t_{12} and t_{14}. In fast mode, 50ns is recommended.

$R_{PU} < 50ns/C_{LOAD}$

Larger pull-up resistances, up to 5k, can be used in slow mode.

APPLICATIONS INFORMATION

Table 6. Typical R_{B1} and R_{B2} Values

MAX CABLE LENGTH	TURNS RATIO	TERMINATION RESISTANCE	I_B	V_A	V_{TCMP}	V_{ICMP}	R_{B2}	R_{B1}	IDRV	READY CURRENT
100m	1 :1	120Ω	1mA	1.2V	0.3V	0.6V	604Ω	1.4k	20mA	4.7mA
50m	1 :1	120Ω	0.5mA	0.6V	0.3V	0.6V	1.21k	2.8k	10mA	3.2mA
100m	1 :1	75Ω	1mA	0.75V	0.19V	0.38V	374Ω	1.62k	20mA	4.7mA
50m	1 :1	75Ω	0.5mA	0.375V	0.19V	0.38V	750Ω	3.24k	10mA	3.2mA

Transformer Selection Guide

As shown in Figure 1, a transformer or a pair of transformers are used to isolate the IP and IM signals between the two LTC6820's. The isoSPI signals have programmable pulse amplitudes up to 1.6V, and pulse widths of 50ns and 150ns. To meet these requirements, choose a transformer having a magnetizing inductance ranging from 50µH to 350µH, and a 1:1 or 2:1 turns ratio. Minimizing transformer insertion loss will reduce required transmit power; generally an insertion loss of less than –1.5dB is recommended.

For optimal common mode noise rejection, choose a center-tapped transformer or a transformer with an integrated common mode choke. The center tap can be tied to a 27pF or smaller capacitor (larger will restrict the driver's ability to set the common mode voltage). If the transformer has both a center tap and common mode choke on the primary side, a larger capacitor may be used.

Table 7 shows a recommended list of transformers for use with the LTC6820. 10/100BaseTX Ethernet transformers are inexpensive and work very well in this application. Ethernet transformers often include a common mode choke, which will improve common mode rejection as compared to other transformers.

Table 7. Recommended Transformers

MANUFACTURER	PART NUMBER	ISOLATION VOLTAGE	TURNS RATIO	CENTER TAP	CM CHOKE
PCA	EPF8119SE	$1500V_{RMS}$	1:1	Yes	Yes
Halo	TG110-AE050N5LF	$1500V_{RMS}$	1:1	Yes	Yes
Pulse	PE-68386NL	1500V DC	1:1	No	No
Murata	78613/3C	$1000V_{RMS}$	1:1	Yes	No
Murata	78604/3C	$1000V_{RMS}$	2:1	No	No
Pulse	HX1188NL	$1500V_{RMS}$	1:1	Yes	Yes
EPCOS	B82804A0354A110	1500V DC	1:1	No	No

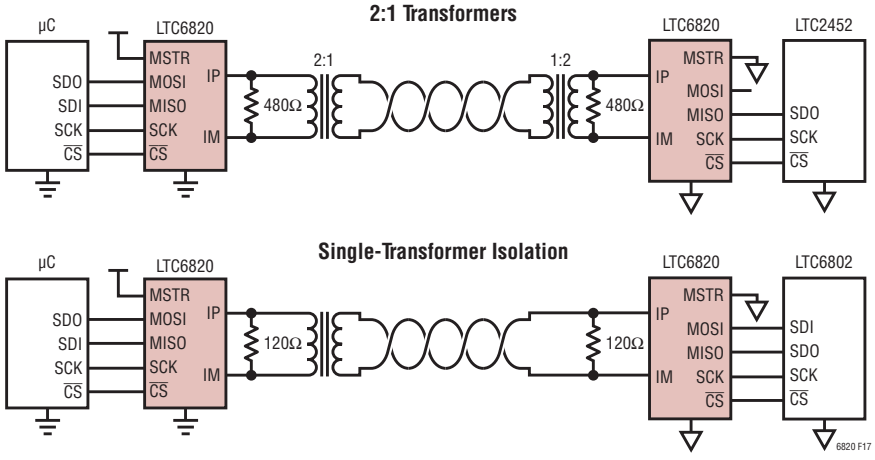


Figure 17. Alternative Isolation Barriers

APPLICATIONS INFORMATION

Capacitive Isolation Barrier

In some applications, where the environment is relatively noise free and only galvanic isolation is required, capacitors can be used in place of transformers as the isolation barrier. With capacitive coupling, the twisted pair cable is driven by a voltage and is subject to signal loss with cable length. This low cost isolated solution can be suitable for short distance interconnections (1 meter or less), such as between adjacent circuit boards or across a large PCB. The capacitors will provide galvanic isolation, but no common mode rejection. This option uses the drivers in a different way, by using pull up resistors to maintain the common mode near V_{DD}, only the sinking drive current has any effect. Figure 18 shows an example application circuit using a capacitive isolation barrier capable of driving 1 meter of cable.

MANUFACTURER	PART NUMBER	CAPACITANCE	VOLTAGE RATING
Murata	GCM188R72A104KA64	100nF	100V

EMC

When using the LTC6820, for the best electromagnetic compatibility (EMC) performance it is recommended to use a transformer with a center tap and a common mode choke as shown in Figure 19. The center tap of the transformer should be bypassed with a 27pF capacitor. The center tap capacitor will help attenuate common mode signals. Large center tap capacitors should be avoided as they will prevent the isoSPI transmitters common mode voltage from settling.

To improve common mode current rejection a common mode choke should also be placed in series with the IP and IM lines of the LTC6820. The common mode choke will both increase EMI immunity and reduce EMI emission. When choosing a common mode choke, the differential mode impedance should be 20Ω or less for signals 50MHz and below. Generally common mode chokes similiar to those used in Ethernet applications are recommended.

Table 8. Recommended Common Mode Chokes

MANUFACTURER	PART NUMBER	DIFFERENTIAL IMPEDANCE AT 50MHz	COMMON MODE IMPEDANCE AT 50MHz
TDK	ACT45B-220-2P	20Ω	5000Ω

Capacitive Isolation

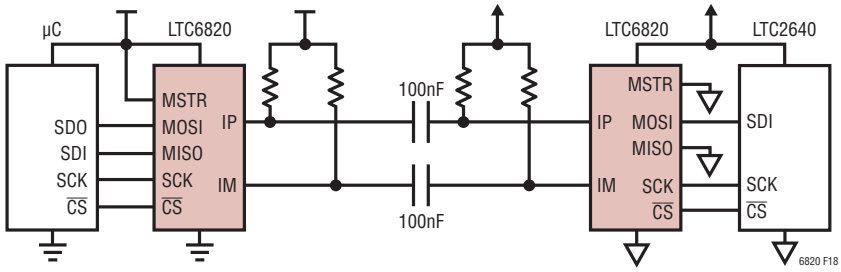


Figure 18. Capacitive Isolation Barrier

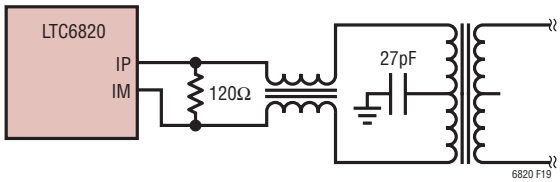


Figure 19. Connection of Transformer and Common Mode Choke

APPLICATIONS INFORMATION

Layout of the isoSPI signal lines also plays a significant role in maximizing the immunity of a circuit. The following layout guidelines should be followed:

1. The transformer should be placed as close to the isoSPI cable connector as possible. The distance should be kept less than 2cm. The LTC6820 should be placed at least 1cm to 2cm away from the transformer to help isolate the IC from the magnetic coupling fields.
2. On the top layer, no ground plane should be placed under the magnetic, the isoSPI connector, or in between the transformer and the connector.
3. The IP and IM traces should be isolated from surrounding circuits. No traces should cross the IP and IM lines, unless separated by a ground plane within the printed circuit board.

The isoSPI drive currents are programmable and allow for a tradeoff between power consumption and noise immunity. The noise immunity of the LTC6820 has been evaluated using a bulk current injection (BCI) test. The BCI test injects current into the twisted-pair lines at set levels over a frequency range of 1MHz to 400MHz. With the minimum I_B current, 0.1mA, the isoSPI serial link has been shown to pass a 40mA BCI test with no bit errors. A 40mA BCI test level is sufficient for most industrial applications. Automotive applications tend to have a higher BCI requirement so the recommended I_B is set to 1mA, the maximum power level. The isoSPI system has been shown to pass a 200mA BCI test with no transmitted bit errors. The 200mA test level is typical for automotive testing.

Software Layer

The isoSPI physical layer has high immunity to EMI and is not particularly susceptible to bit errors induced by noise, but for best results in a high noise environment it is recommended to implement a software layer that uses an error detection code like a cyclic redundancy check or check sum. Error detection codes will allow software detection of any bit error and will notify the system to retry the last erroneous serial communication.

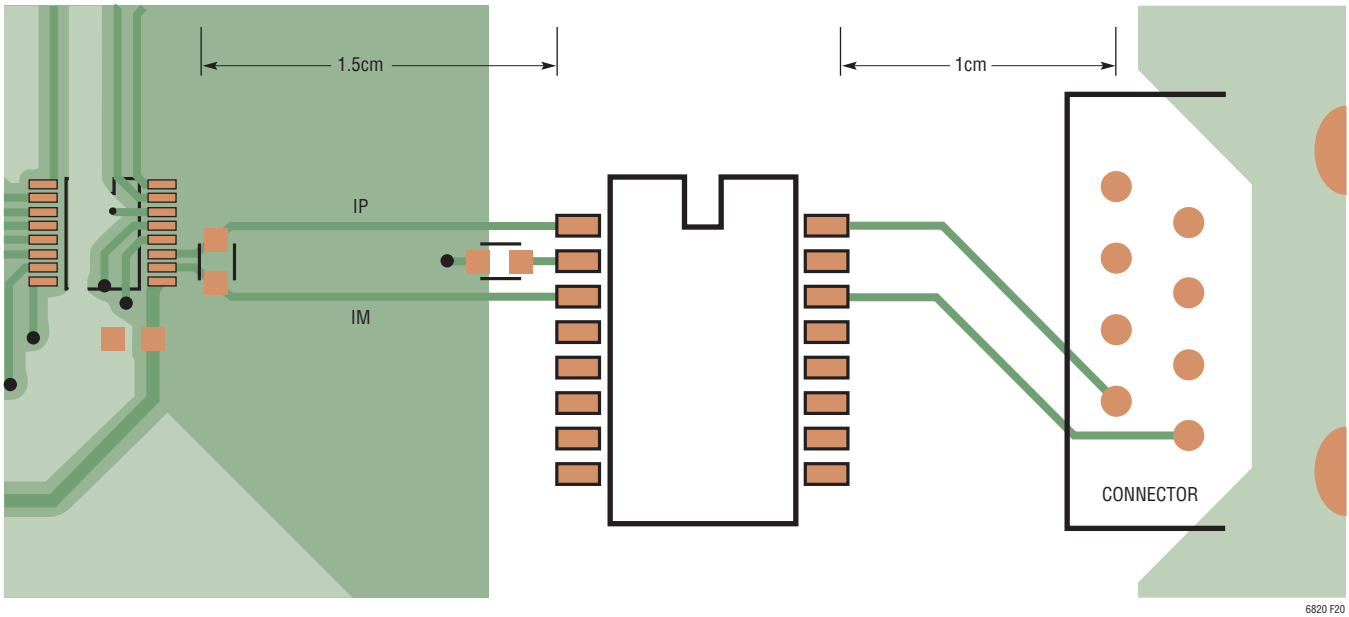
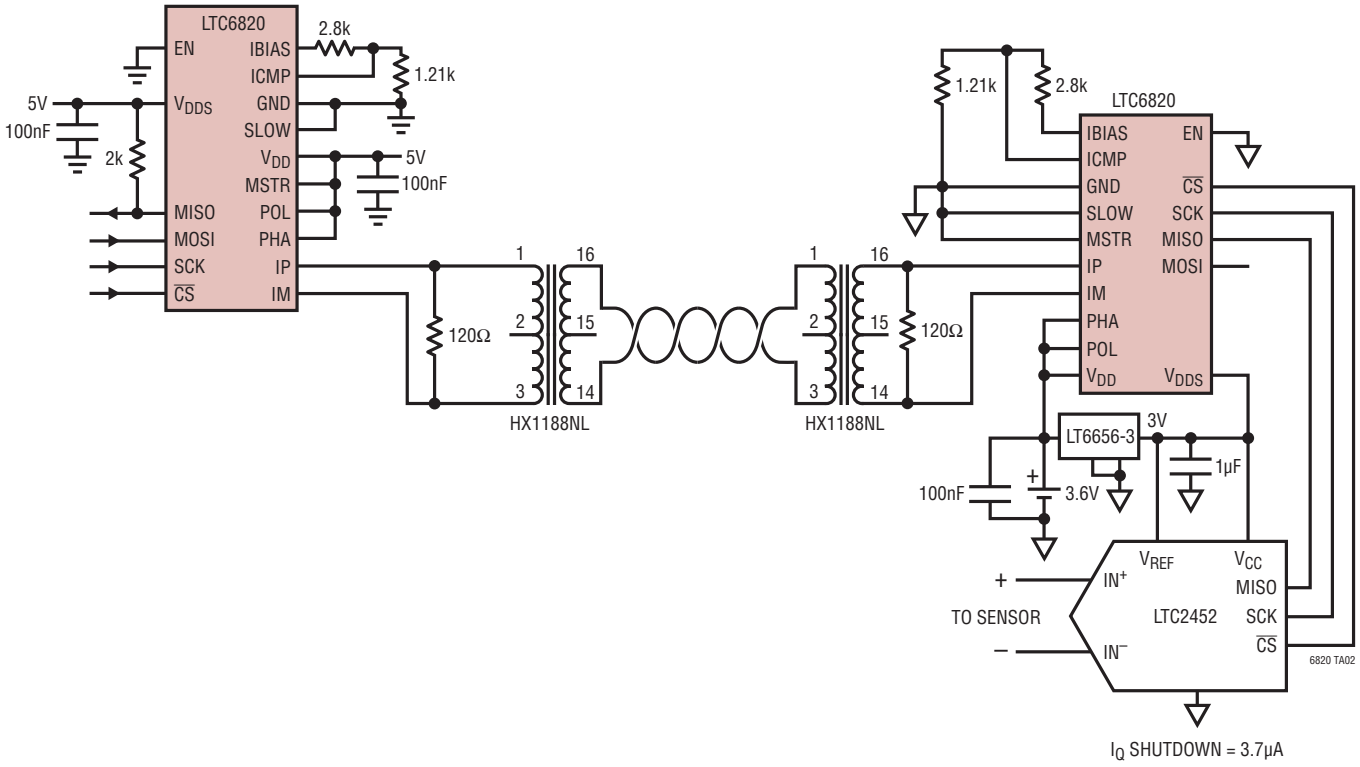


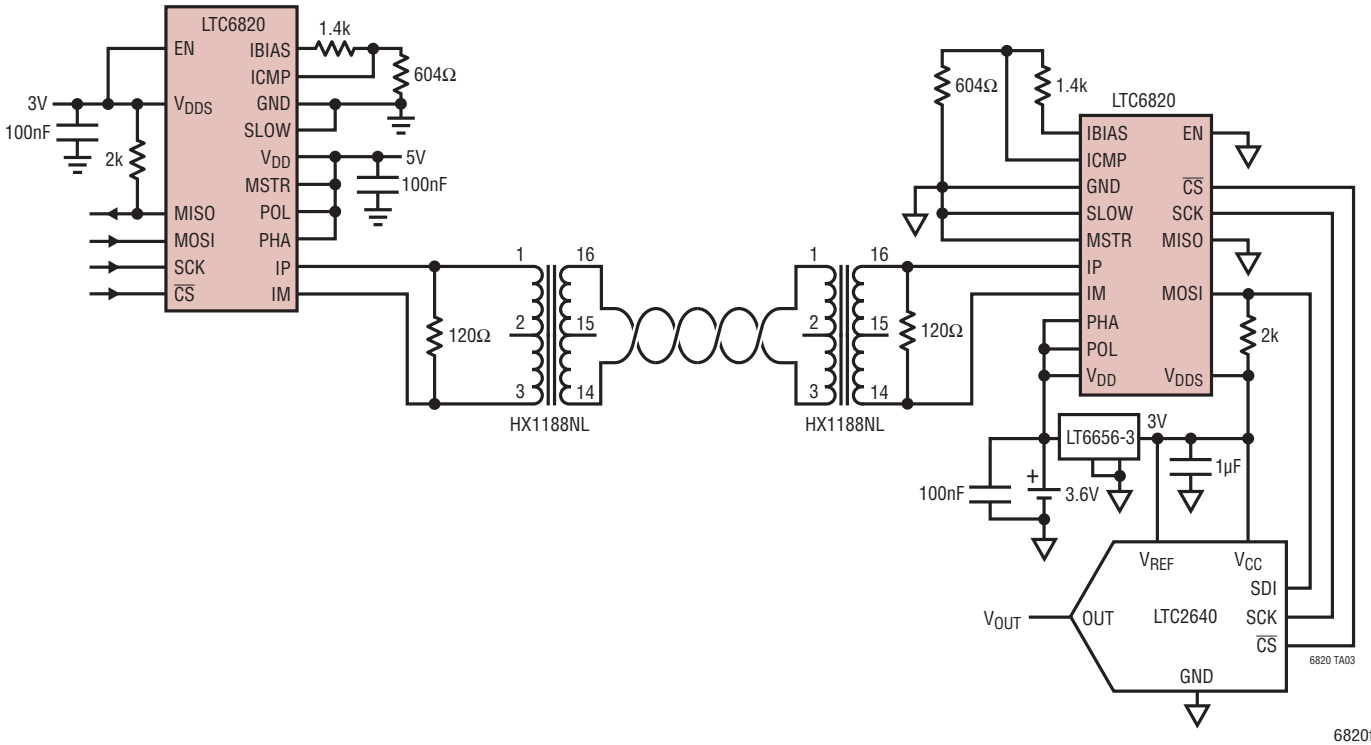
Figure 20. Example Layout

TYPICAL APPLICATIONS

Remote Sensor Monitor with Micropower Shutdown

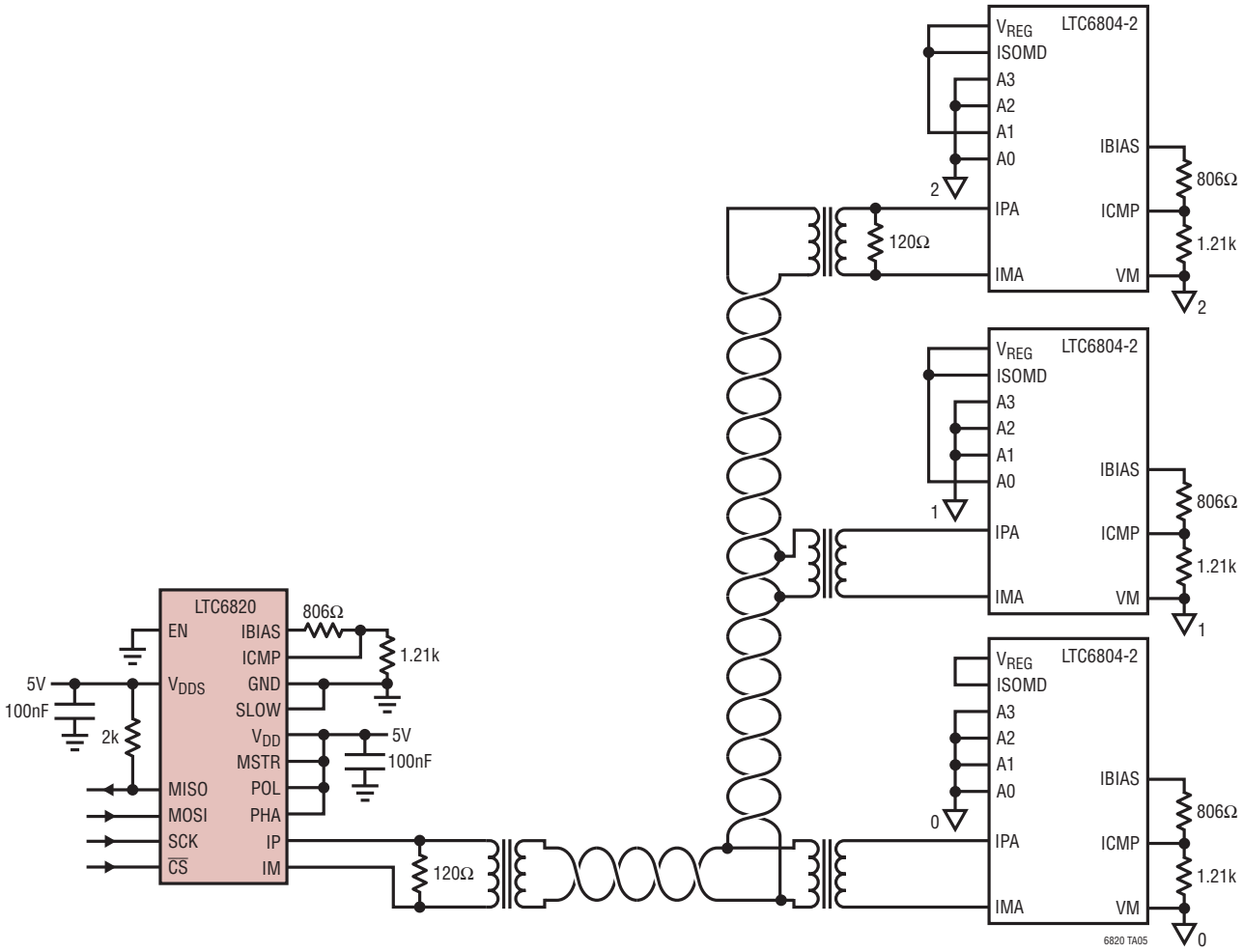


100 Meter Remote DAC Control



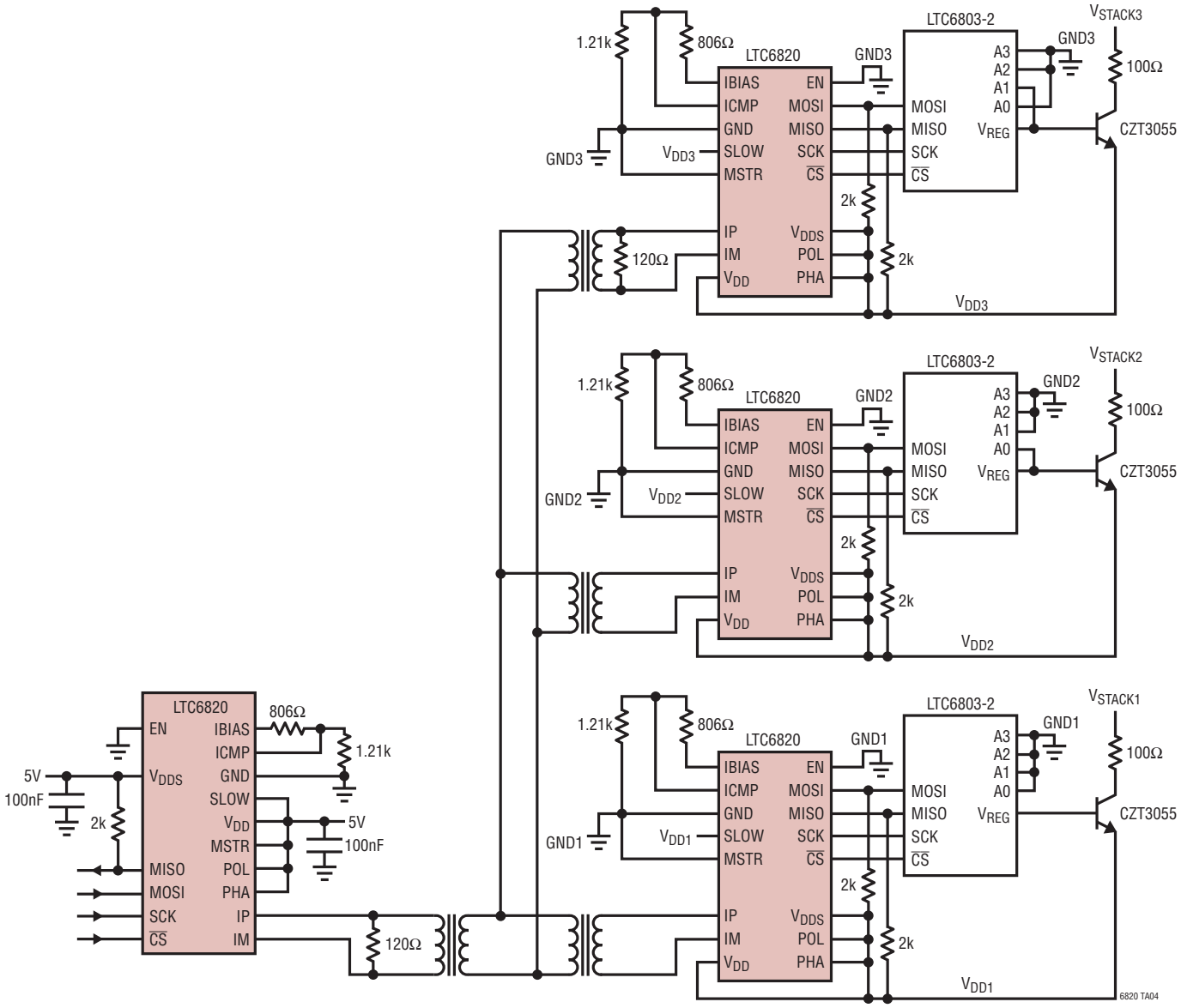
TYPICAL APPLICATIONS

Interfacing to Addressable Stack of LTC6804-2 Multicell Battery Monitors



TYPICAL APPLICATIONS

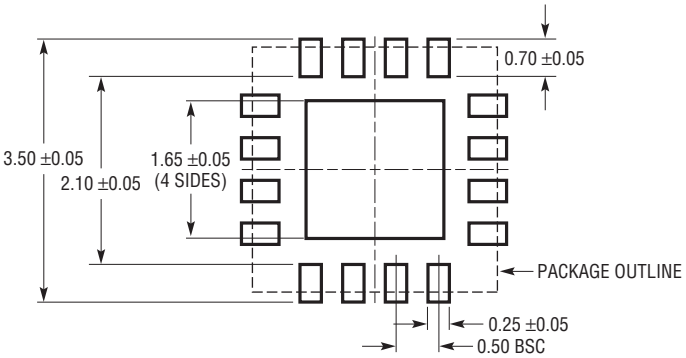
Battery Monitoring System Using a Multidrop isoSPI Link



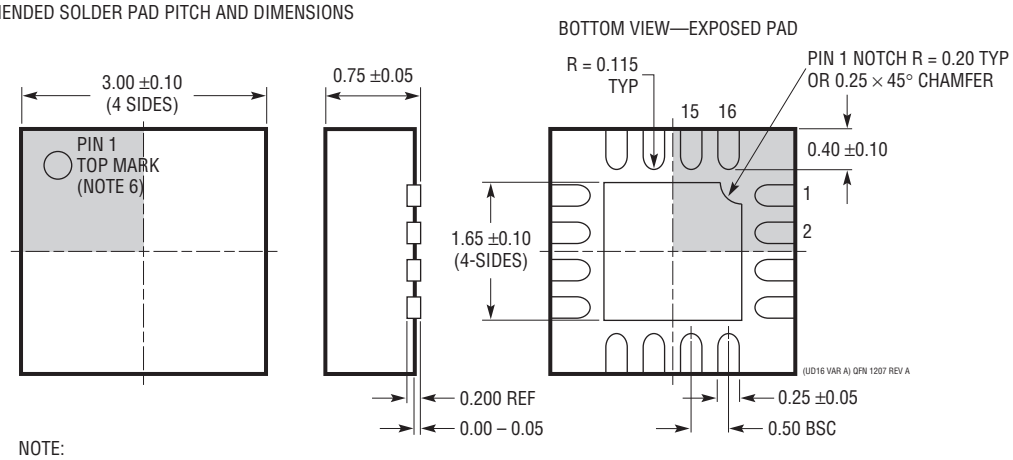
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

UD Package
16-Lead Plastic QFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1700 Rev A)
Exposed Pad Variation AA



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS

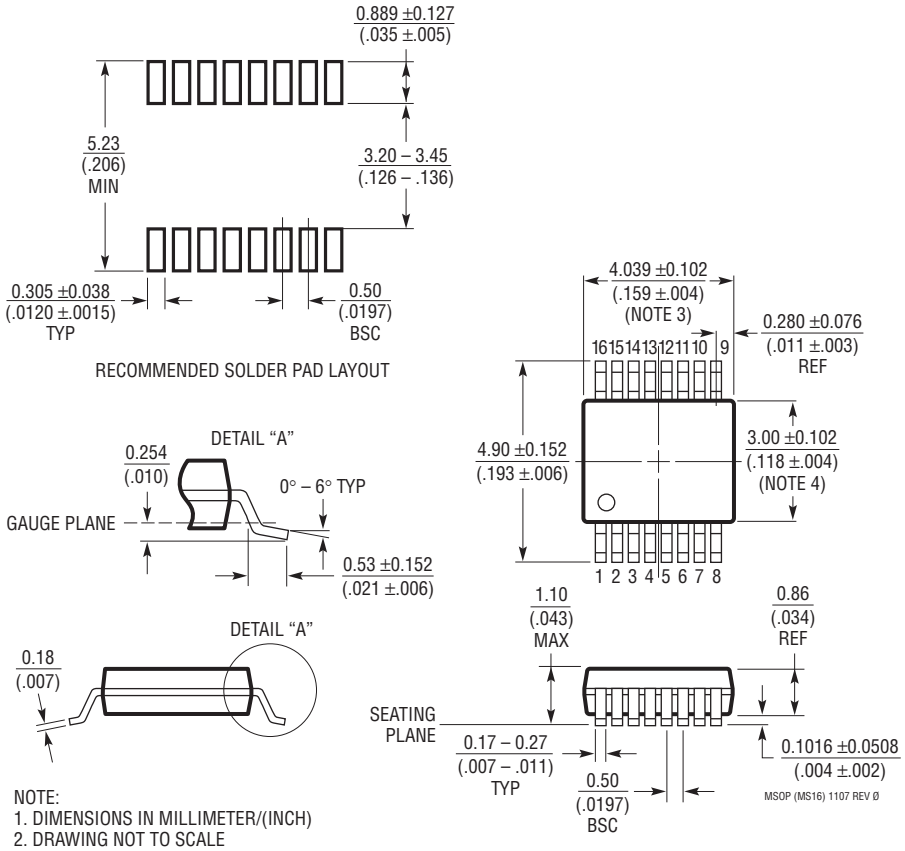


NOTE:
1. DRAWING CONFORMS TO JEDEC PACKAGE OUTLINE MO-220 VARIATION (WEED-4)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

MS Package
16-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1669 Rev Ø)

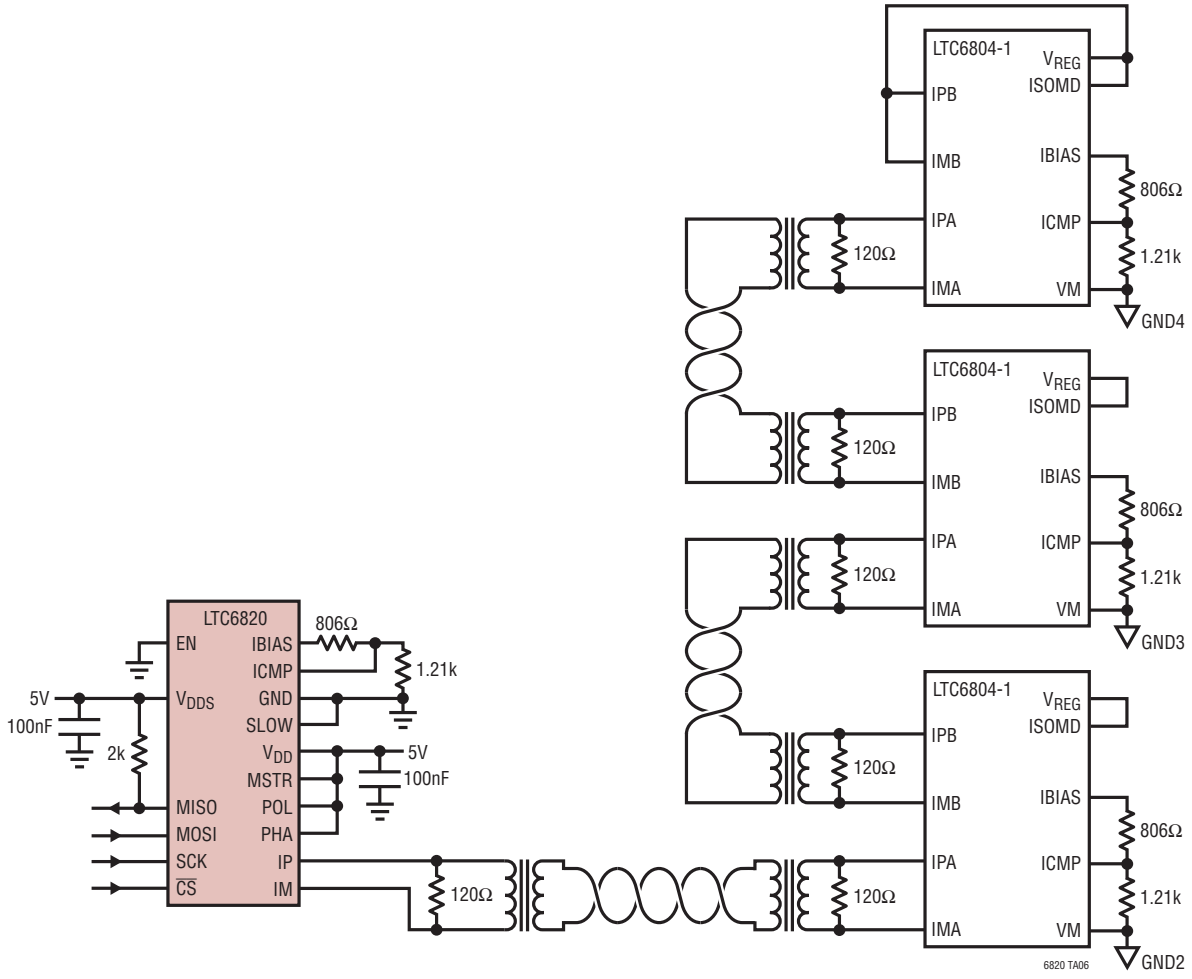


NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

TYPICAL APPLICATION

Interfacing to Daisy-Chained Stack of LTC6804-1 Multicell Battery Monitors



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC6803-2/ LTC6803-4	Multicell Battery Stack Monitor with an Individually Addressable SPI Interface	Functionality Equivalent to LTC6803-1/LTC6803-3, Allows for Parallel Communication Battery Stack Topologies
LTC6803-1/ LTC6803-3	Multicell Battery Stack Monitor with Daisy-Chained SPI Interface	Functionality Equivalent to LTC6803-2/LTC6803-4, Allows for Multiple Devices to Be Daisy Chained
LTC6903	1kHz to 68MHz Programmable Silicon Oscillator with SPI Interface	Frequency Resolution of 0.01%. No External Components Required. Operates on 2.7V to 5.5V.
LTC6804-1/ LTC6804-2	Multicell Battery Stack Monitor with Built-In isoSPI Interface	Includes isoSPI Interfaces for Communication with Master LTC6820 and to other LTC6804 Devices

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