2.7GHz, 5V, Low Noise, Rail-to-Rail Input Differential Amplifier/Driver

FEATURES

- **Low Noise: 1.6nV/√Hz RTI**
- **Low Power: 18mA at 5V**
- **Low Distortion (HD2/HD3):**
  - **–82dBc/–65dBc at 50MHz, $2V_{P-P}$**
  - **–97dBc/–91dBc at 25MHz, $2V_{P-P}$**
- **Rail-to-Rail Differential Input**
- 4.5V to 5.25V Supply Voltage Range
- Fully Differential Input and Output
- Adjustable Output Common Mode Voltage
- 800MHz –3dB Bandwidth with A_V = 1
- Gain-Bandwidth Product: 2.7GHz
- Low Power Shutdown
- Available in 8-Lead MSOP and 16-Lead 3mm × 3mm × 0.75mm QFN Packages

APPLICATIONS

- Differential Input ADC Driver
- Single-Ended to Differential Conversion
- Level-Shifting Ground-Referenced Signals
- Level-Shifting V_{CC}-Referenced Signals
- High-Linearity Direct Conversion Receivers

DESCRIPTION

The LTC®6405 is a very low noise, low distortion, fully differential input/output amplifier optimized for 5V, single supply operation. The LTC6405 input common mode range is rail-to-rail, while the output common mode voltage is independently adjustable by applying a voltage on the V_{OCM} pin. This makes the LTC6405 ideal for level shifting signals with a wide common mode range for driving 12-bit to 16-bit single supply, differential input ADCs.

A 2.7GHz gain-bandwidth product results in 65dB linearity for 50MHz input signals. The LTC6405 is unity gain stable and the closed-loop bandwidth extends from DC to 800MHz. The output voltage swing extends from near-ground to 4V, to be compatible with a wide range of ADC converter input requirements. The LTC6405 draws only 18mA, and has a hardware shutdown feature which reduces current consumption to 400µA.

The LTC6405 is available in a compact 3mm × 3mm 16-pin leadless QFN package, as well as an 8-lead MSOP package, and operates over a –40°C to 85°C temperature range.

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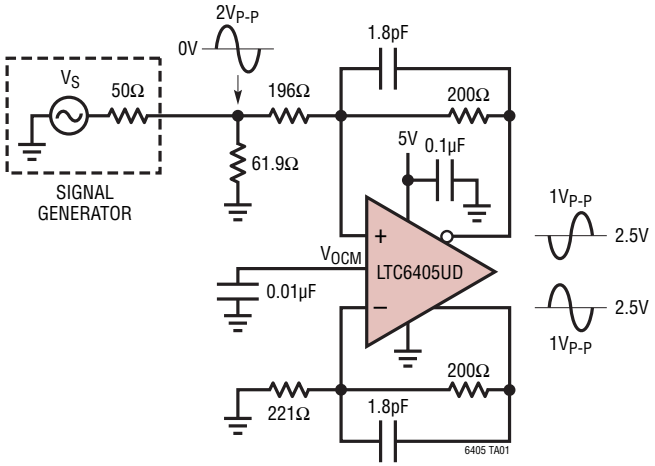
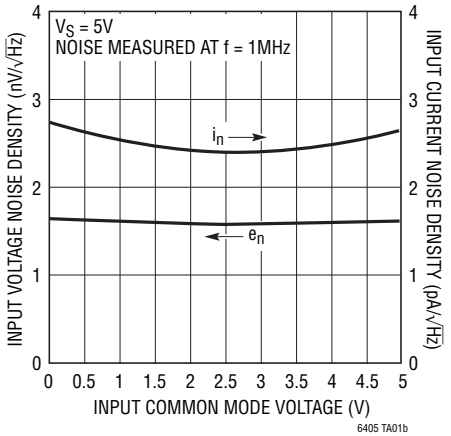
TYPICAL APPLICATION

Single-Ended Input to Differential Output with Common Mode Level Shifting



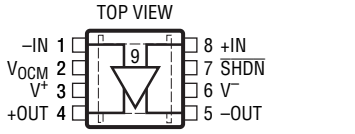
Input Noise Density vs Input Common Mode Voltage



ABSOLUTE MAXIMUM RATINGS (Note 1)

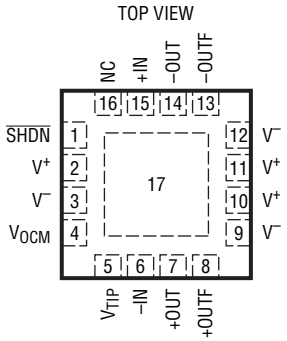
Total Supply Voltage (V^+ to V^-) 5.5V
Input Current
(+IN, –IN, V_{OCM}, $\overline{SHDN}$, V_{TIP}) (Note 2) ..... ±10mA
Output Short-Circuit Duration (Note 3) ..... Indefinite
Operating Temperature Range
(Note 4) ..... –40°C to 85°C
Specified Temperature Range (Note 5)
LTC6405I ..... –40°C to 85°C
LTC6405C ..... 0°C to 70°C
Junction Temperature ..... 150°C
Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



MS8E PACKAGE
8-LEAD PLASTIC MSOP

T_{JMAX} = 150°C, θ_{JA} = 40°C/W, θ_{JC} = 10°C/W
EXPOSED PAD (PIN 9) IS V^-, MUST BE SOLDERED TO PCB



UD PACKAGE
16-LEAD (3mm × 3mm) PLASTIC QFN

T_{JMAX} = 150°C, θ_{JA} = 68°C/W, θ_{JC} = 4.2°C/W
EXPOSED PAD (PIN 17) IS V^-, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE
LTC6405CMS8E#PBF	LTC6405CMS8E#TRPBF	LTDKN	8-Lead Plastic MSOP	0°C to 70°C
LTC6405IMS8E#PBF	LTC6405IMS8E#TRPBF	LTDKN	8-Lead Plastic MSOP	–40°C to 85°C
LTC6405CUD#PBF	LTC6405CUD#TRPBF	LDKP	16-Lead (3mm × 3mm) Plastic QFN	0°C to 70°C
LTC6405IUD#PBF	LTC6405IUD#TRPBF	LDKP	16-Lead (3mm × 3mm) Plastic QFN	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
This product is only offered in trays. For more information go to: http://www.linear.com/packaging/

DC ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V^+ = 5V, V^- = 0V, V_{CM} = V_{OCM} = V_{ICM} = 2.5V, $V_{\overline{SHDN}}$ = open, circuit component values in Figure 1 used, unless otherwise noted. V_S is defined as ($V^+ - V^-$). V_{OUTCM} is defined as ($V_{+OUT} + V_{-OUT}$)/2. V_{ICM} is defined as ($V_{+IN} + V_{-IN}$)/2. $V_{OUTDIFF}$ is defined as ($V_{+OUT} - V_{-OUT}$).

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OSDIFF}	Differential Offset Voltage (Input Referred)	V_{ICM} = 5V (Note 12) V_{ICM} = 2.5V V_{ICM} = 0V (Note 12)	● ● ●		±1 ±0.5 ±1	±7 ±3.5 ±7	mV mV mV
$\Delta V_{OSDIFF}/\Delta T$	Differential Offset Voltage Drift (Input Referred)	V_{ICM} = 5V (Note 12) V_{ICM} = 2.5V V_{ICM} = 0V (Note 12)	● ● ●		1.5 1 3		µV/°C µV/°C µV/°C
I_B	Input Bias Current (Note 6)	V_{ICM} = 5V V_{ICM} = 2.5V V_{ICM} = 0V	 ● 	 –24 	8 –7 –14	 	µA µA µA
I_{OS}	Input Offset Current (Note 6)	V_{ICM} = 5V V_{ICM} = 2.5V V_{ICM} = 0V	 ● 	 	±0.5 ±0.5 ±0.5	 ±4 	µA µA µA
R_{IN}	Input Resistance	Common Mode Differential Mode			230 3.5		kΩ kΩ
C_{IN}	Input Capacitance	Differential			1		pF
e_n	Differential Input Referred Noise Voltage Density	f = 1MHz, Not Including R_I/R_F Noise			1.6		$nV/\sqrt{Hz}$
i_n	Input Noise Current Density	f = 1MHz, Not Including R_I/R_F Noise			2.4		$pA/\sqrt{Hz}$
e_{nVOCM}	Input Referred Common Mode Output Noise Voltage Density	f = 1MHz			9.5		$nV/\sqrt{Hz}$
V_{ICMR} (Note 7)	Input Signal Common Mode Range	Op-Amp Inputs	●	V^-		V^+	V
CMRRI (Note 8)	Input Common Mode Rejection Ratio (Input Referred) $\Delta V_{ICM}/\Delta V_{OSDIFF}$	V_{ICM} from 0V to 5V	●	50	75		dB
CMRRIO (Note 8)	Output Common Mode Rejection Ratio (Input Referred) $\Delta V_{OCM}/\Delta V_{OSDIFF}$	V_{OCM} from 0.5V to 3.9V	●	50	75		dB
PSRR (Note 9)	Differential Power Supply Rejection ($\Delta V_S/\Delta V_{OSDIFF}$)	V_S = 4.5V to 5.25V	●	50	75		dB
PSRRCM (Note 9)	Output Common Mode Power Supply Rejection ($\Delta V_S/\Delta V_{OSCM}$)	V_S = 4.5V to 5.25V	●	55	70		dB
G_{CM}	Common Mode Gain ($\Delta V_{OUTCM}/\Delta V_{OCM}$)	V_{OCM} from 0.5V to 3.9V	●		1		V/V
ΔG_{CM}	Common Mode Gain Error 100 • (G_{CM} – 1)	V_{OCM} from 0.5V to 3.9V	●		±0.25	±0.8	%
BAL	Output Balance ($\Delta V_{OUTCM}/\Delta V_{OUTDIFF}$)	$\Delta V_{OUTDIFF}$ = 2V Single-Ended Input Differential Input	 ● ●	 	 –60 –65	 –40 –40	 dB dB
V_{OSCM}	Common Mode Offset Voltage ($V_{OUTCM} - V_{OCM}$)		●		±6	±15	mV
$\Delta V_{OSCM}/\Delta T$	Common Mode Offset Voltage Drift		●		20		µV/°C
V_{OUTCMR} (Note 7)	Output Signal Common Mode Range (Voltage Range for the V_{OCM} Pin)		●	0.5		3.9	V
R_{INVOCM}	Input Resistance, V_{OCM} Pin		●	13	19	25	kΩ
V_{OCM}	Self-Biased Voltage at the V_{OCM} Pin	V_{OCM} = Open	●	2.35	2.5	2.65	V
V_{OUT}	Output Voltage, High, +OUT/–OUT Pins	I_L = 0 I_L = –5mA	● ●	3.9 3.85	4 3.95		V V
	Output Voltage, Low, +OUT/–OUT Pins	I_L = 0 I_L = 5mA	● ●		0.3 0.42	0.45 0.54	V V
I_{SC}	Output Short-Circuit Current, +OUT/–OUT Pins (Note 10)		●	±40	±60		mA

DC ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V^+ = 5V, V^- = 0V, V_{CM} = V_{OCM} = V_{ICM} = 2.5V, $V_{\overline{SHDN}}$ = open, circuit component values in Figure 1 used, unless otherwise noted. V_S is defined as ($V^+ – V^-$). V_{OUTCM} is defined as ($V_{+OUT} + V_{–OUT}$)/2. V_{ICM} is defined as ($V_{+IN} + V_{–IN}$)/2. $V_{OUTDIFF}$ is defined as ($V_{+OUT} – V_{–OUT}$).

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
A_{VOL}	Large-Signal Open Loop Voltage Gain				90		dB
V_S	Supply Voltage Range		●	4.5		5.25	V
I_S	Supply Current		●		18	23	mA
$I_{\overline{SHDN}}$	Supply Current in Shutdown	$V_{\overline{SHDN}}$ = 0V	●		0.4	1	mA
$R_{\overline{SHDN}}$	$\overline{SHDN}$ Pull-Up Resistor	$V_{\overline{SHDN}}$ = 0V to 0.5V	●	30	50	70	kΩ
V_{IL}	$\overline{SHDN}$ Input Logic Low		●	1.25	1.8		V
V_{IH}	$\overline{SHDN}$ Input Logic High		●		2	2.55	V
t_{ON}	Turn-On Time				200		ns
t_{OFF}	Turn-Off Time				50		ns

AC ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V^+ = 5V, V^- = 0V, V_{CM} = V_{OCM} = V_{ICM} = 2.5V, $V_{\overline{SHDN}}$ = open, R_{LOAD} = 400Ω, circuit component values in Figure 2 used, unless otherwise noted. V_S is defined as ($V^+ – V^-$). V_{ICM} is defined as ($V_{+IN} + V_{–IN}$)/2. $V_{OUTDIFF}$ is defined as ($V_{+OUT} – V_{–OUT}$).

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
SR	Slew Rate	Differential Output			690		V/µS
GBW	Gain-Bandwidth Product	f_{TEST} = 27MHz			2.7		GHz
$f_{–3dB}$	–3dB Frequency (See Figure 2)	QFN Package MSOP Package		500 400	800 750		MHz MHz
	50MHz Distortion Differential Input, $V_{OUTDIFF}$ = $2V_{P-P}$ (Note 13)	V_{OCM} = 2.5V, V_S = 5V 2nd Harmonic 3rd Harmonic	 ●		 –80 –64	 –53	 dBc dBc
		V_{OCM} = 2.5V, V_S = 5V, R_{LOAD} = 800Ω 2nd Harmonic 3rd Harmonic			 –82 –66		 dBc dBc
		V_{OCM} = 2.5V, V_S = 5V, R_{LOAD} = 800Ω, R_I = R_F = 499Ω 2nd Harmonic 3rd Harmonic			 –82 –64		 dBc dBc
	50MHz Distortion Single-Ended Input, $V_{OUTDIFF}$ = $2V_{P-P}$ (Note 13)	V_{OCM} = 2.5V, V_S = 5V, R_{LOAD} = 800Ω, R_I = R_F = 499Ω 2nd Harmonic 3rd Harmonic			 –72 –77		 dBc dBc
	3rd-Order IMD at 49.5MHz, 50.5MHz	$V_{OUTDIFF}$ = $2V_{P-P}$ Envelope, R_{LOAD} = 800Ω			–63		dBc
	Equivalent OIP3 at 50MHz (Note 11)	R_{LOAD} = 800Ω			35.5		dBm
t_S	Settling Time	$V_{OUTDIFF}$ = 2V Step 1% Settling 0.1% Settling			 6 11		 ns ns
NF	Noise Figure at 50MHz	Shunt-Terminated to 50Ω, R_S = 50Ω Z_{IN} = 200Ω (R_I = 100Ω, R_F = 300Ω)			14.4 7.5		dB dB

ELECTRICAL CHARACTERISTICS

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Input pins (+IN, –IN, V_{OCM}, $\overline{SHDN}$ and V_{TIP}) are protected by steering diodes to either supply. If the inputs should exceed either supply voltage, the input current should be limited to less than 10mA. In addition, the inputs +IN, –IN are protected by a pair of back-to-back diodes. If the differential input voltage exceeds 1.4V, the input current should be limited to less than 10mA.

Note 3: A heat sink may be required to keep the junction temperature below the Absolute Maximum Rating when the output is shorted indefinitely.

Note 4: The LTC6405C/LTC6405I are guaranteed functional over the operating temperature range –40°C to 85°C.

Note 5: The LTC6405C is guaranteed to meet specified performance from 0°C to 70°C. The LTC6405C is designed, characterized, and expected to meet specified performance from –40°C to 85°C but is not tested or QA sampled at these temperatures. The LTC6405I is guaranteed to meet specified performance from –40°C to 85°C.

Note 6: Input bias current is defined as the average of the input currents flowing into the inputs (–IN, and +IN). Input Offset current is defined as the difference between the input currents ($I_{OS} = I_B^+ – I_B^–$).

Note 7: Input common mode range is tested using the test circuit of Figure 1 by taking 3 measurements of differential gain with a ±1VDC differential output with V_{ICM} = 0V; V_{ICM} = 2.5V; V_{ICM} = 5V, verifying that the differential gain has not deviated from the V_{ICM} = 2.5V case by more than 0.5%, and that the common mode offset (V_{OSCM}) has not deviated from the common mode offset at V_{ICM} = 2.5V by more than ±35mV.

The voltage range for the output common mode range is tested using the test circuit of Figure 1 by applying a voltage on the V_{OCM} pin and testing at both V_{OCM} = 2.5V and at the Electrical Characteristics table limits to verify that the common mode offset (V_{OSCM}) has not deviated by more than ±20mV from the V_{OCM} = 2.5V case.

Note 8: Input CMRR is defined as the ratio of the change in the input common mode voltage at the pins +IN or –IN to the change in differential input referred voltage offset. Output CMRR is defined as the ratio of the change in the voltage at the V_{OCM} pin to the change in differential input referred voltage offset. This specification is strongly dependent on feedback ratio matching between the two outputs and their respective inputs, and it is difficult to measure actual amplifier performance. (See the “Effects of Resistor Pair Mismatch” in the Applications Information section of this data sheet.) For a better indicator of actual amplifier performance independent of feedback component matching, refer to the PSRR specification.

Note 9: Differential Power Supply Rejection (PSRR) is defined as the ratio of the change in supply voltage to the change in differential input referred voltage offset. Common mode power supply rejection (PSRRCM) is defined as the ratio of the change in supply voltage to the change in the common mode offset, $V_{OUTCM} – V_{OCM}$.

Note 10: Extended operation with the output shorted may cause the junction temperature to exceed the 150°C limit.

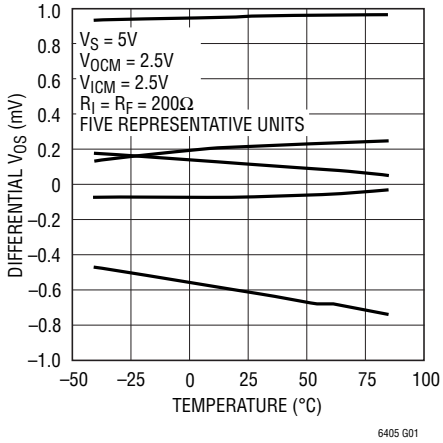
Note 11: Because the LTC6405 is a feedback amplifier with low output impedance, a resistive load is not required when driving an ADC. Therefore, typical output power can be very small in many applications. In order to compare the LTC6405 with “RF style” amplifiers that require 50Ω load, the output voltage swing is converted to dBm as if the outputs were driving a 50Ω load. For example, $2V_{P-P}$ output swing is equal to 10dBm using this convention.

Note 12: Includes offset/drift induced by feedback resistors mismatch. See the Applications Information section for more details.

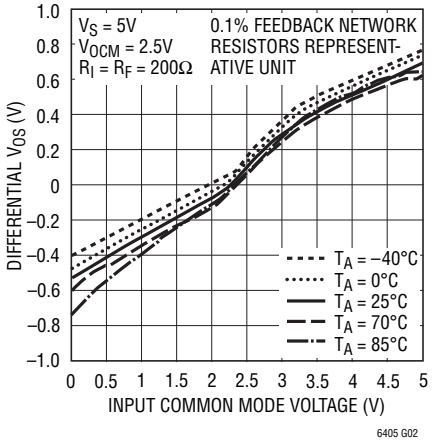
Note 13: QFN package only—refer to datasheet curves for MSOP package numbers.

TYPICAL PERFORMANCE CHARACTERISTICS

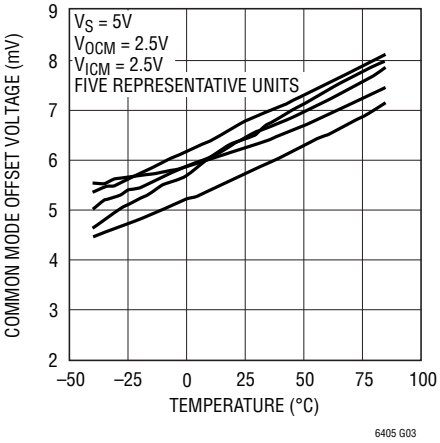
Differential Input Referred Offset Voltage vs Temperature



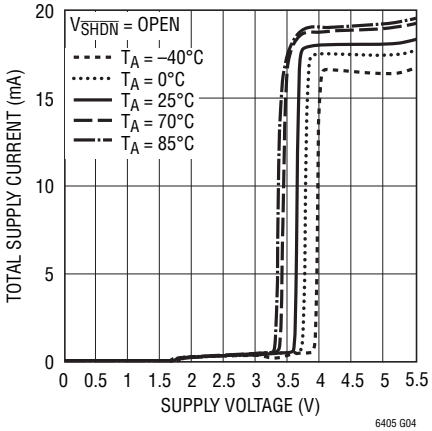
Differential Input Referred Offset Voltage vs Input Common Mode Voltage



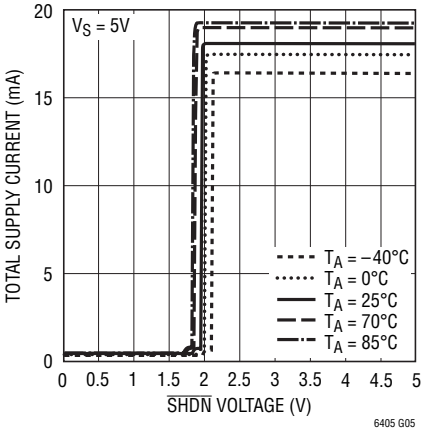
Common Mode Offset Voltage vs Temperature



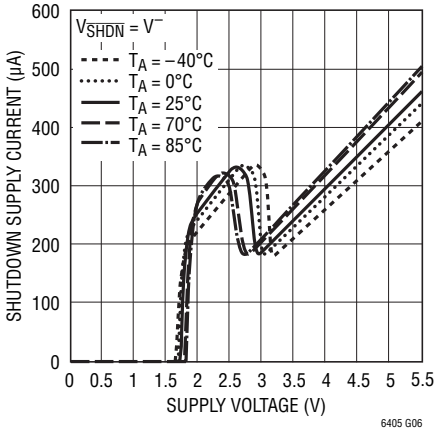
Supply Current vs Supply Voltage



Supply Current vs $\overline{SHDN}$ Voltage

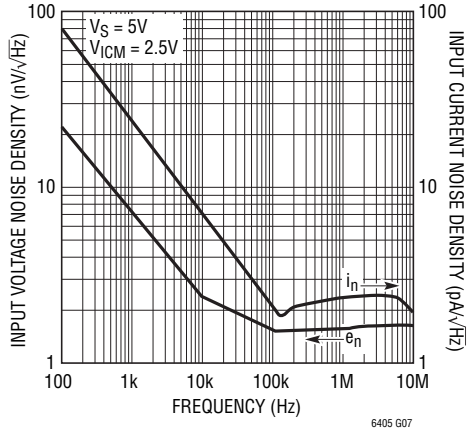


Shutdown Supply Current vs Supply Voltage

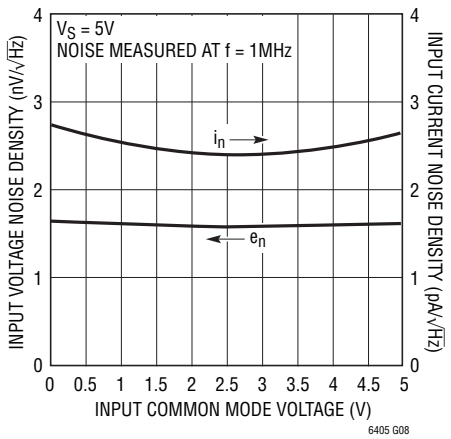


TYPICAL PERFORMANCE CHARACTERISTICS

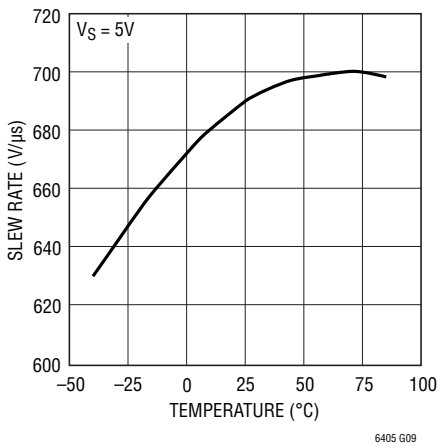
Input Noise Density vs Frequency



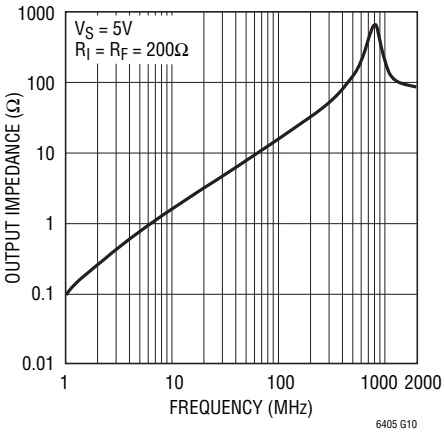
Input Noise Density vs Input Common Mode Voltage



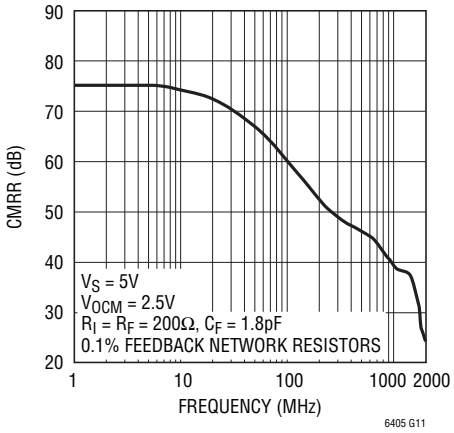
Differential Slew Rate vs Temperature



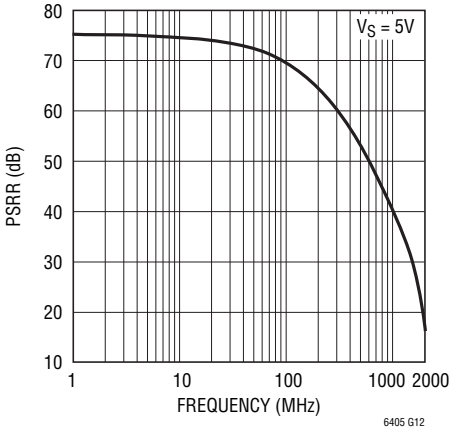
Differential Output Impedance vs Frequency



CMRR vs Frequency

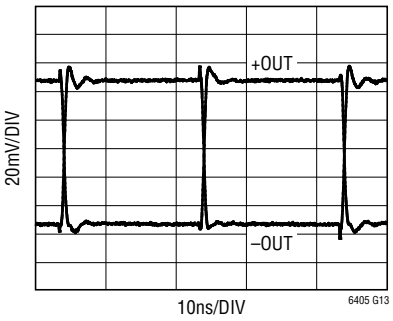


Differential PSRR vs Frequency



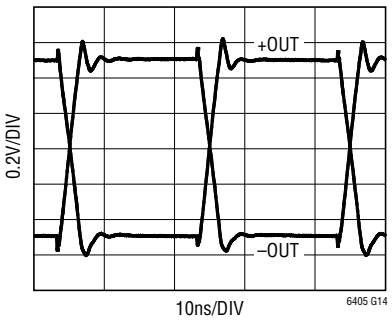
TYPICAL PERFORMANCE CHARACTERISTICS (QFN Package)

Small Signal Step Response



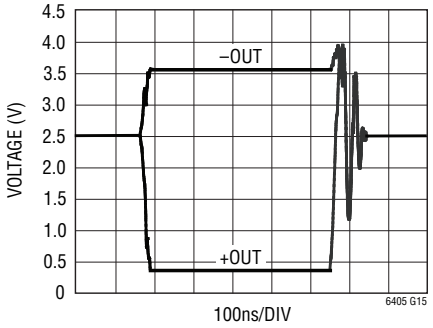
V_S = 5V
$V_{OCM} = V_{ICM}$ = 2.5V
R_{LOAD} = 400Ω
$R_I = R_F$ = 200Ω
C_F = 1.8pF
C_L = 0pF

Large Signal Step Response



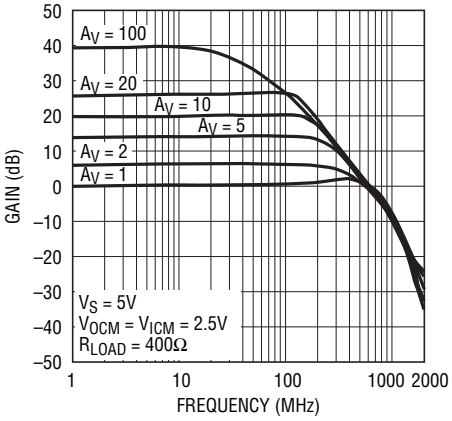
V_S = 5V
R_{LOAD} = 400Ω
V_{IN} = 2V_{P-P}, DIFFERENTIAL

Overdriven Output Transient Response



V_S = 5V
V_{OCM} = 2.5V
R_{LOAD} = 400Ω TO GROUND PER OUTPUT

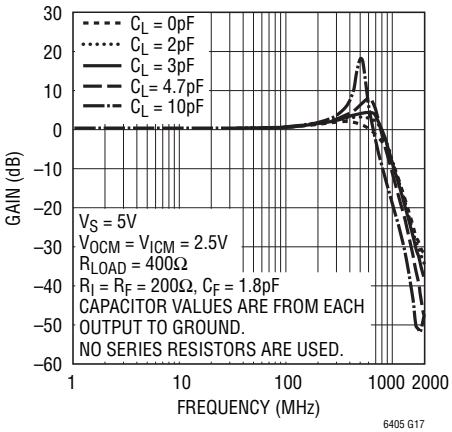
Frequency Response vs Closed Loop Gain



A_V (V/V)	R_I (Ω)	R_F (Ω)	C_F (pF)
1	200	200	1.8
2	200	400	1.5
5	200	1k	0.6
10	200	2k	0.2
20	200	4k	0
100	200	20k	0

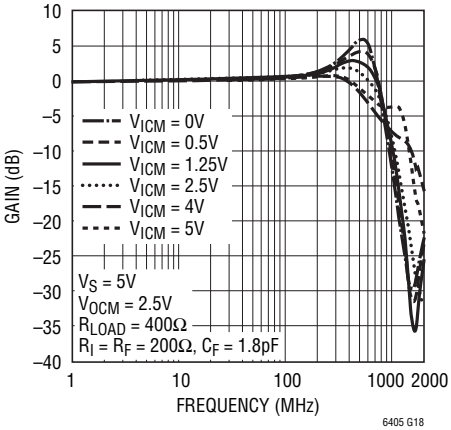
6405 G16

Frequency Response vs Load Capacitance



6405 G17

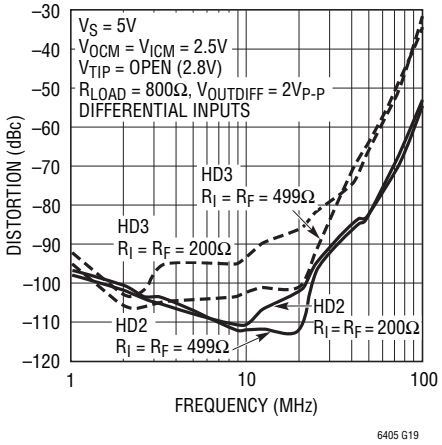
Frequency Response vs Input Common Mode Voltage



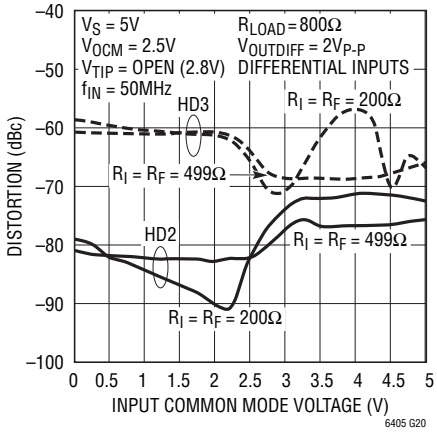
6405 G18

TYPICAL PERFORMANCE CHARACTERISTICS (QFN Package)

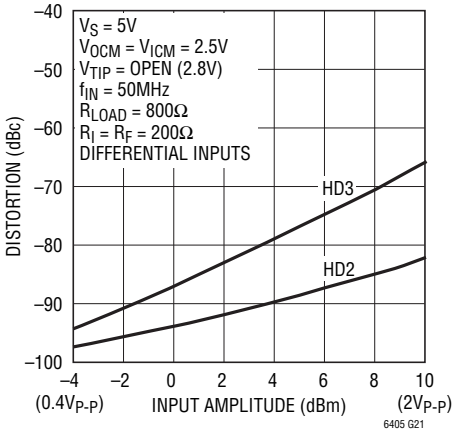
Harmonic Distortion vs Frequency



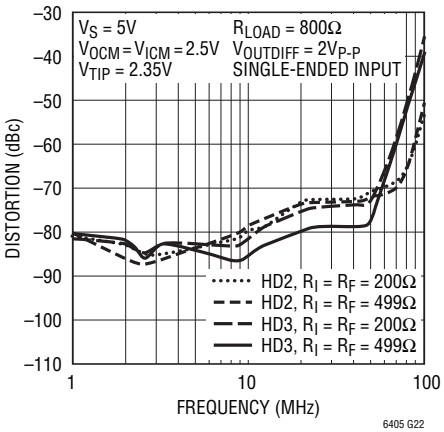
Harmonic Distortion vs Input Common Mode Voltage



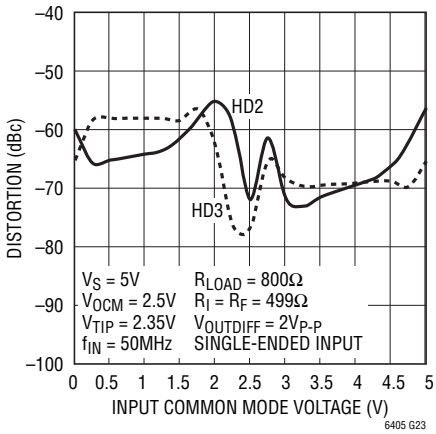
Harmonic Distortion vs Input Amplitude



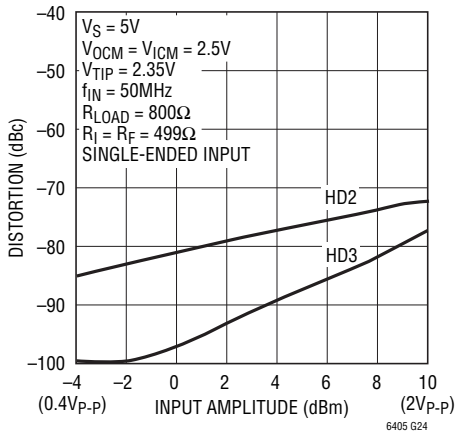
Harmonic Distortion vs Frequency



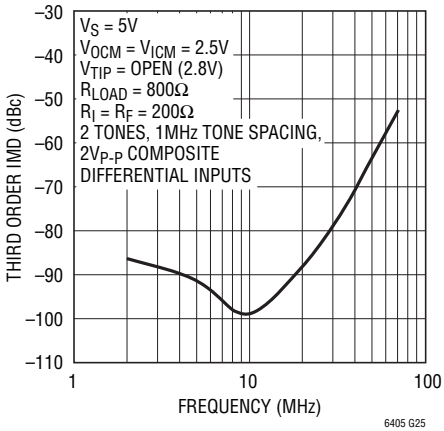
Harmonic Distortion vs Input Common Mode Voltage



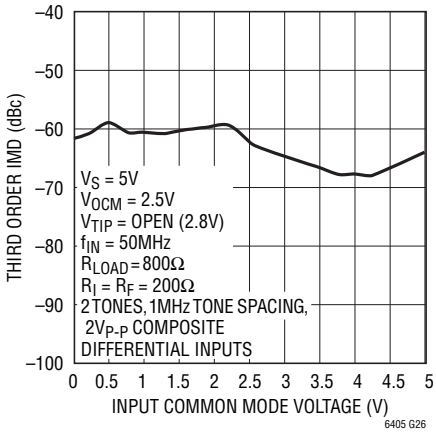
Harmonic Distortion vs Input Amplitude



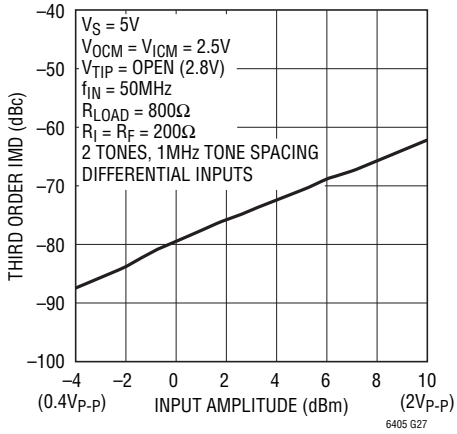
Intermodulation Distortion vs Frequency



Intermodulation Distortion vs Input Common Mode Voltage

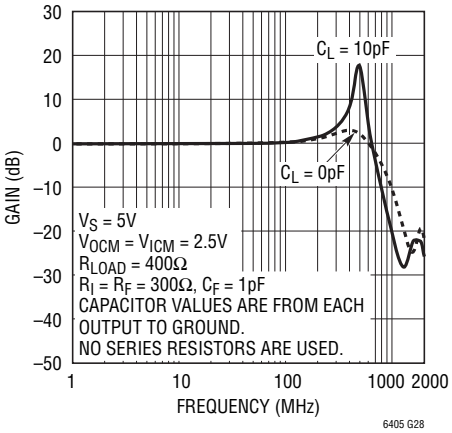


Intermodulation Distortion vs Input Amplitude

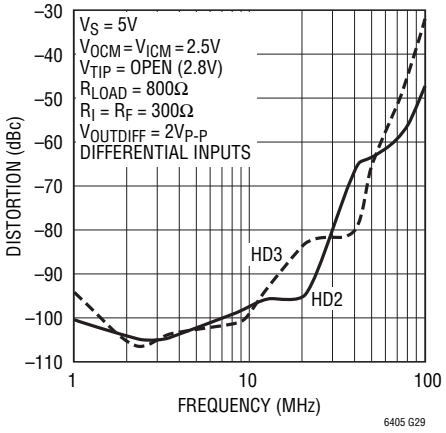


TYPICAL PERFORMANCE CHARACTERISTICS (MSOP Package)

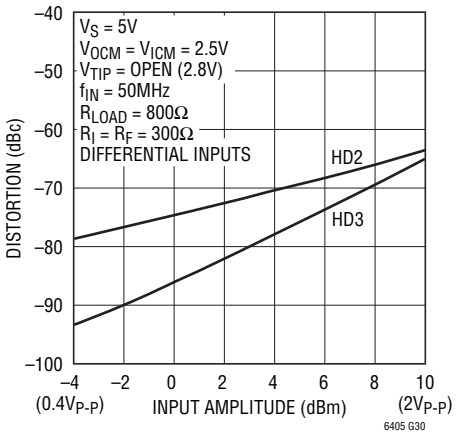
Frequency Response vs Load Capacitance



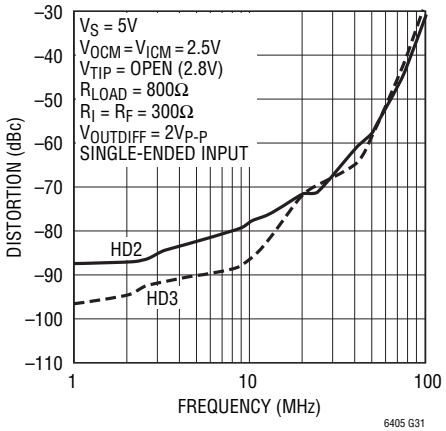
Harmonic Distortion vs Frequency



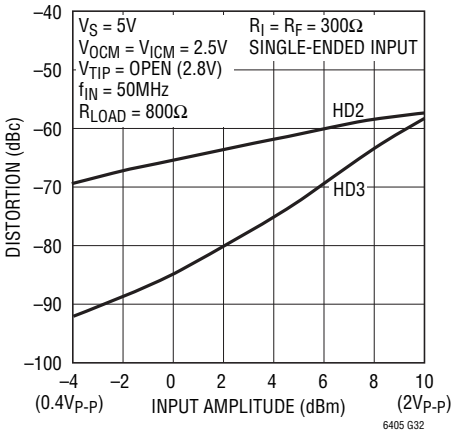
Harmonic Distortion vs Input Amplitude



Harmonic Distortion vs Frequency



Harmonic Distortion vs Input Amplitude



PIN FUNCTIONS (MSOP/QFN)

V_{OCM} (Pin 2/Pin 4): Output Common Mode Reference Voltage. The voltage on V_{OCM} sets the output common mode voltage level (which is defined as the average of the voltages on the +OUT and –OUT pins). The V_{OCM} voltage is internally set by a resistive divider between the supplies, developing a default voltage potential of 2.5V with a 5V supply. The V_{OCM} pin can be over-driven by an external voltage capable of driving the 19kΩ Thevenin equivalent impedance presented by the pin. The V_{OCM} pin should be bypassed with a high quality ceramic bypass capacitor of at least 0.01µF, to minimize common mode noise from being converted to differential noise by impedance mismatches both externally and internally to the IC.

V^+ (Pin 3/Pins 2, 10, 11):

V^- (Pin 6/Pins 3, 9, 12):

Power Supply Pins. It is critical that close attention be paid to supply bypassing. For single supply applications, it is recommended that a high quality 0.1µF surface mount ceramic bypass capacitor be placed between V^+ and V^- with direct short connections. In addition, V^- should be tied directly to a low impedance ground plane with minimal routing. For dual (split) power supplies, it is recommended that additional high quality, 0.1µF ceramic capacitors are used to bypass V^+ to ground and V^- to ground, again with minimal routing. For driving large loads (<200Ω), additional bypass capacitance may be needed for optimal performance. Keep in mind that small geometry (e.g., 0603 or smaller) surface mount ceramic capacitors have a much higher self resonant frequency than do leaded capacitors, and perform best in high speed applications.

+OUT, –OUT (Pins 4, 5/Pins 7, 14): Unfiltered Output Pins. Besides driving the feedback network, each pin can drive an additional 50Ω to ground with typical short circuit current limiting of ±60mA. Each amplifier output is designed to drive a load capacitance of 5pF. Larger capacitive loads should be decoupled with at least 15Ω resistors from each output.

V_{TIP} (Pin 5) QFN Only: This pin can normally be left floating. It determines which pair of input transistors (NPN or PNP or both) is sensing the input signal. The V_{TIP} pin is set by an internal resistive divider between the supplies, developing a default 2.8V voltage with a 5V supply. V_{TIP} has a Thevenin equivalent resistance of approximately 17k and can be over-driven by an external voltage. The V_{TIP} pin should be bypassed with a high quality ceramic bypass capacitor of at least 0.01µF. See the Applications Information section for more details.

$\overline{SHDN}$ (Pin 7/Pin 1): When $\overline{SHDN}$ is floating or directly tied to V^+, the LTC6405 is in the normal (active) operating mode. When the $\overline{SHDN}$ pin is connected to V^-, the LTC6405 enters into a low power shutdown state with Hi-Z outputs.

+IN, –IN (Pins 8, 1/Pins 15, 6): Noninverting and Inverting Input Pins of the Amplifier, Respectively. For best performance, it is highly recommended that stray capacitance be kept to an absolute minimum by keeping printed circuit connections as short as possible.

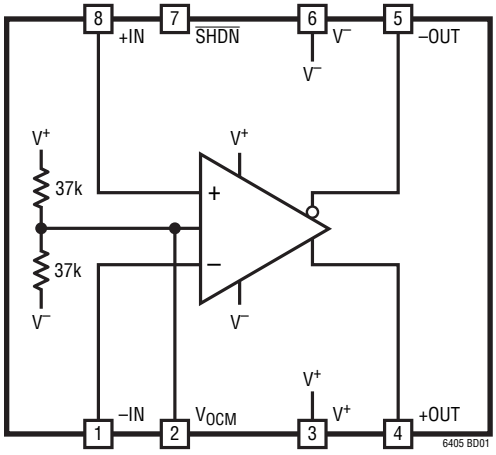
+OUTF, –OUTF (Pins 8, 13) QFN Only: Filtered Output Pins. These pins have a series RC network (R = 50Ω, C = 3.75pF) connected between the filtered and unfiltered outputs. See the Applications Information section for more details.

NC (Pin 16) QFN Only: No Connection. This pin is not connected internally.

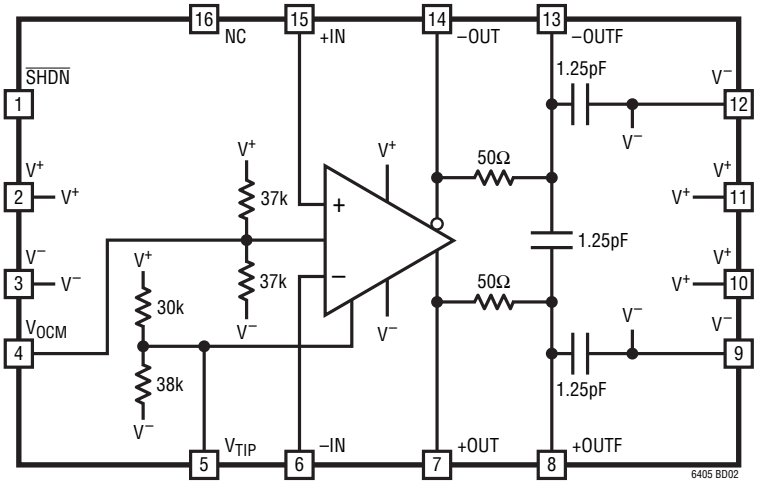
Exposed Pad (Pin 9/Pin 17): Tie the bottom pad to V^-. If split supplies are used, DO NOT tie the pad to ground.

BLOCK DIAGRAMS

LTC6405 Block Diagram/Pinout in MSOP Package



LTC6405 Block Diagram/Pinout in QFN Package



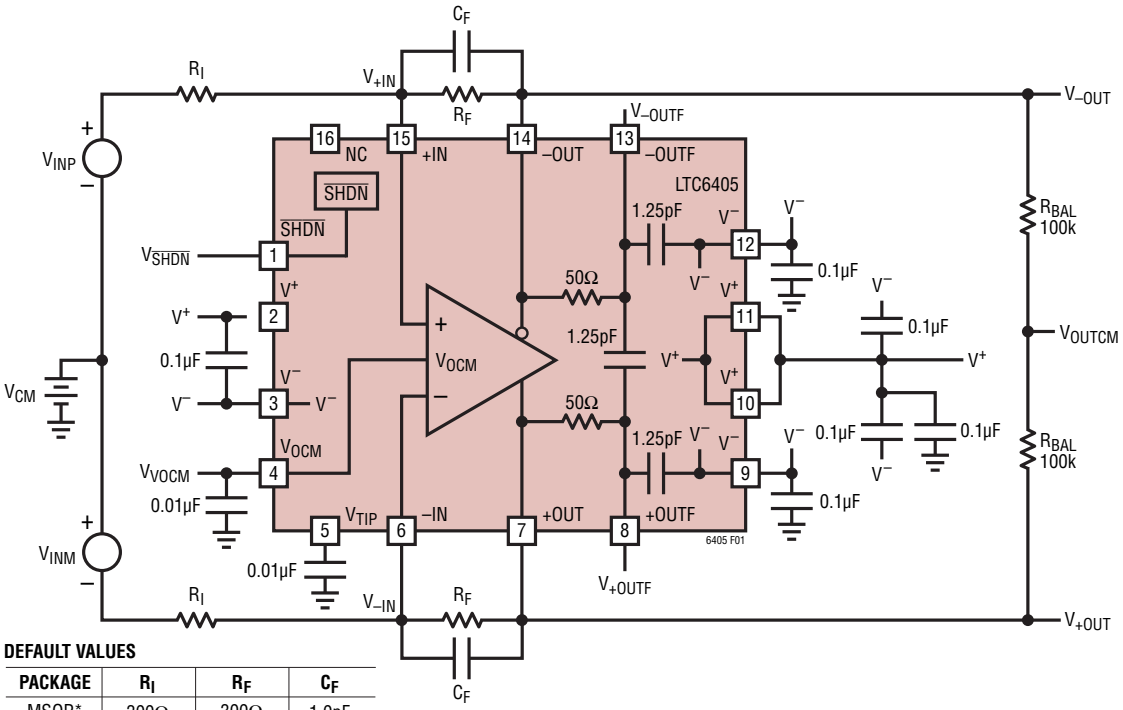
APPLICATIONS INFORMATION

Functional Description

The LTC6405 is a small outline, wideband, low noise, and low distortion fully-differential amplifier with accurate output phase balancing. The LTC6405 is optimized to drive low voltage, single-supply, differential input analog-to-digital converters (ADCs). The LTC6405 input common mode range is rail-to-rail, while the output common mode voltage is independently adjustable by applying a voltage on the V_{OCM} pin. The output voltage swing extends from near-ground to 4V, to be compatible with a wide range of ADC converter input requirements. This makes the LTC6405 ideal for level shifting signals with a wide common mode range for driving 12-bit to 16-bit single supply, differential input ADCs. The differential output allows for twice the signal swing in low voltage systems when compared to single-ended output amplifiers. The balanced differential nature of the amplifier also provides even-order harmonic distortion cancellation, and less susceptibility to common mode noise (like power supply noise). The LTC6405 can be used as a single ended input to differential output amplifier, or as a differential input to differential output amplifier.

The LTC6405 output common mode voltage, defined as the average of the two output voltages, is independent of the input common mode voltage, and is adjusted by applying a voltage on the V_{OCM} pin. If the pin is left open, there is an internal resistive voltage divider, which develops a potential of 2.5V (if the supply is 5V). It is recommended that a high quality ceramic cap is used to bypass the V_{OCM} pin to a low impedance ground plane. The LTC6405's internal common mode feedback path forces accurate output phase balancing to reduce even order harmonics, and centers each individual output about the potential set by the V_{OCM} pin.

$$V_{OUTCM} = V_{OCM} = \frac{V_{+OUT} + V_{-OUT}}{2}$$



DEFAULT VALUES

PACKAGE	R_I	R_F	C_F
MSOP*	300Ω	300Ω	1.0pF
QFN	200Ω	200Ω	1.8pF

(R_I, R_F: 0.1% RESISTORS)

*TO OPTIMIZE THE HIGH FREQUENCY PERFORMANCE FOR THE PIN CONFIGURATION OF THE LTC6405 IN THE SMALL MSOP PACKAGE, A FEEDBACK RESISTANCE OF AT LEAST 300Ω IS RECOMMENDED.

Figure 1. DC Test Circuit

APPLICATIONS INFORMATION

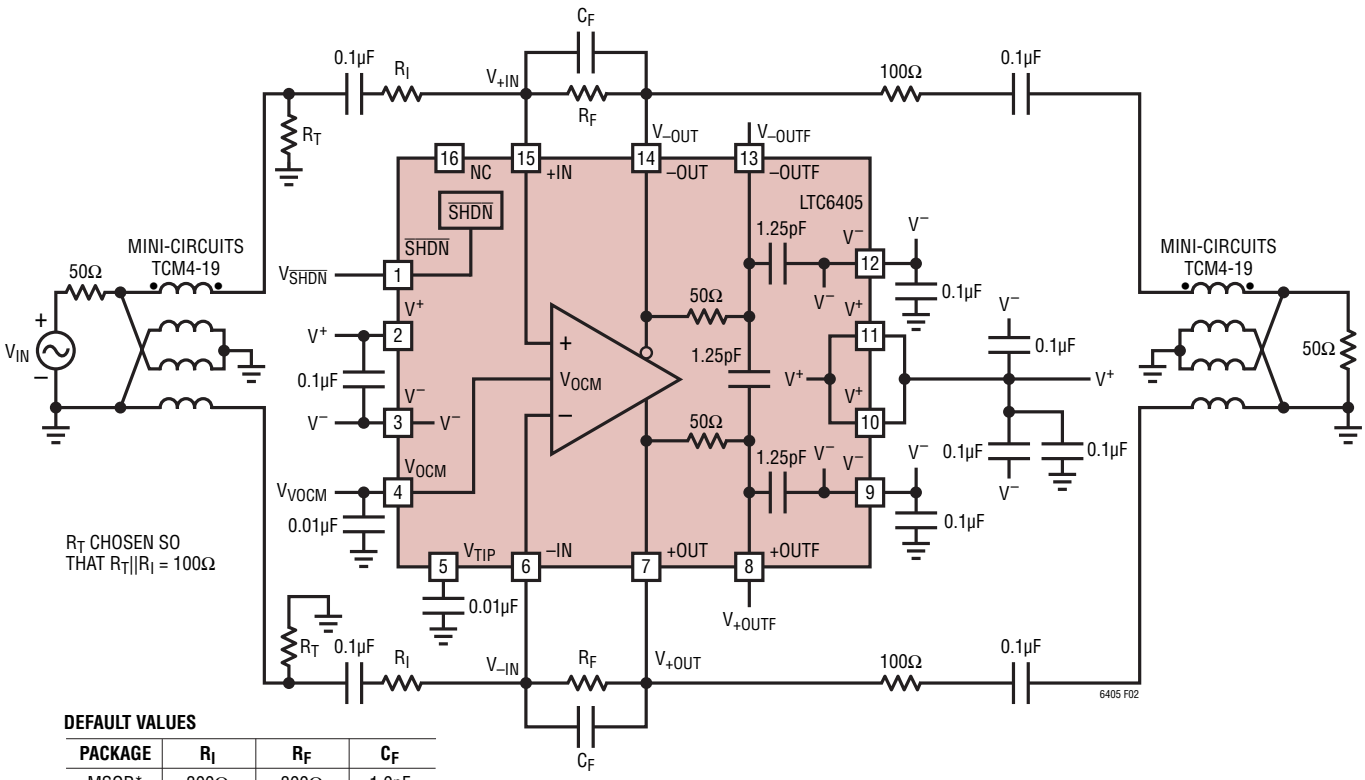
The outputs (+OUT and –OUT) of the LTC6405 are capable of swinging from close-to-ground to typically 1V below V^+. They can source or sink up to approximately 60mA of current. Each output is designed to directly drive up to 5pF to ground. Higher load capacitances should be decoupled with at least 15Ω of series resistance from each output.

Input Pin Protection

The LTC6405 input stage is protected against differential input voltages which exceed 1.4V by two pairs of series diodes connected back to back between +IN and –IN. In addition, the input pins have clamping diodes to either power supply. If the input pins are over-driven, the current should be limited to under 10mA to prevent damage to the IC. The LTC6405 also has clamping diodes to either power supply on the V_{OCM}, V_{TIP} and $\overline{SHDN}$ pins and if driven to voltages which exceed either supply, they too, should be current limited to under 10mA.

$\overline{SHDN}$ Pin

The $\overline{SHDN}$ pin is a CMOS logic input with a 50k internal pull-up resistor. If the pin is driven low, the LTC6405 powers down with Hi-Z outputs. If the pin is left unconnected or driven high, the part is in normal active operation. Some care should be taken to control leakage currents at this pin to prevent inadvertently putting the LTC6405 into shutdown. The turn-on and turn-off time between the shutdown and active states are typically less than 1µs.



DEFAULT VALUES

PACKAGE	R_I	R_F	C_F
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QFN	200Ω	200Ω	1.8pF

(R_I, R_F: 0.1% RESISTORS)

*TO OPTIMIZE THE HIGH FREQUENCY PERFORMANCE FOR THE PIN CONFIGURATION OF THE LTC6405 IN THE SMALL MSOP PACKAGE, A FEEDBACK RESISTANCE OF AT LEAST 300Ω IS RECOMMENDED.

Figure 2. AC Test Circuit (–3dB BW Testing)

APPLICATIONS INFORMATION

General Amplifier Applications

As levels of integration have increased and correspondingly, system supply voltages decreased, there has been a need for ADCs to process signals differentially in order to maintain good signal to noise ratios. These ADCs are typically supplied from a single supply voltage which can be as low as 3V, and will have an optimal common mode input range of 1.25V or 1.5V. The LTC6405 makes interfacing to these ADCs easy, by providing both single-ended to differential conversion as well as common mode level shifting. The gain to $V_{OUTDIFF}$ from V_{INM} and V_{INP} is:

$$V_{OUTDIFF} = V_{+OUT} - V_{-OUT} \approx \frac{R_F}{R_I} \bullet (V_{INP} - V_{INM})$$

Note from the above equation, the differential output voltage ($V_{+OUT} - V_{-OUT}$) is completely independent of input and output common mode voltages, or the voltage at the common mode pin. This makes the LTC6405 ideally suited for pre-amplification, level shifting and conversion of single ended signals to differential output signals in preparation for driving differential input ADCs.Δ

Effects of Resistor Pair Mismatch

Figure 3 shows a circuit diagram which takes into consideration that real world resistors will not match perfectly. Assuming infinite open loop gain, the differential output relationship is given by the equation:

$$V_{OUTDIFF} = V_{+OUT} - V_{-OUT} \cong \frac{R_F}{R_I} \bullet V_{INDIFF} + \frac{\Delta\beta}{\beta_{AVG}} \bullet V_{ICM} - \frac{\Delta\beta}{\beta_{AVG}} \bullet V_{OCM}$$

where:

R_F is the average of R_{F1}, and R_{F2}, and R_I is the average of R_{I1}, and R_{I2}.

β_{AVG} is defined as the average feedback factor from the outputs to their respective inputs:

$$\beta_{AVG} = \frac{1}{2} \bullet \left(\frac{R_{I1}}{R_{I1} + R_{F1}} + \frac{R_{I2}}{R_{I2} + R_{F2}} \right)$$

$\Delta\beta$ is defined as the difference in feedback factors:

$$\Delta\beta = \frac{R_{I2}}{R_{I2} + R_{F2}} - \frac{R_{I1}}{R_{I1} + R_{F1}}$$

V_{ICM} is defined as the average of the two input voltages V_{INP} and V_{INM} (also called the input common mode voltage):

$$V_{ICM} = \frac{1}{2} \bullet (V_{INP} + V_{INM})$$

and V_{INDIFF} is defined as the difference of the input voltages:

$$V_{INDIFF} = V_{INP} - V_{INM}$$

V_{OCM} is defined as the average of the two output voltages V_{+OUT} and V_{-OUT}:

$$V_{OCM} = \frac{V_{+OUT} + V_{-OUT}}{2}$$

When the feedback ratios mismatch ($\Delta\beta$), common mode to differential conversion occurs.

Setting the differential input to zero ($V_{INDIFF} = 0$), the degree of common mode to differential conversion is given by the equation:

$$V_{OUTDIFF} = V_{+OUT} - V_{-OUT} \approx (V_{ICM} - V_{OCM}) \bullet \frac{\Delta\beta}{\beta_{AVG}}$$

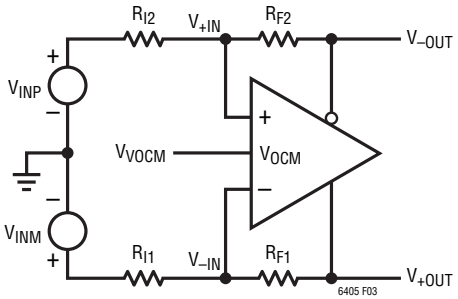


Figure 3. Real-World Application with Feedback Resistor Pair Mismatch

APPLICATIONS INFORMATION

In general, the degree of feedback pair mismatch is a source of common mode to differential conversion of both signals and noise. Using 1% resistors or better will mitigate most problems, and will provide about 34dB worst case of common mode rejection. Using 0.1% resistors will provide about 54dB of common mode rejection. A low impedance ground plane should be used as a reference for both the input signal source and the V_{OCM} pin. Bypassing the V_{OCM} with a high quality 0.1µF ceramic capacitor to this ground plane will further help prevent common mode signals from being converted to differential signals.

There may be concern on how feedback factor mismatch affects distortion. Feedback factor mismatch from using 1% resistors or better, has a negligible effect on distortion. However, in single supply level shifting applications where there is a voltage difference between the input common mode voltage and the output common mode voltage, resistor mismatch can make the apparent voltage offset of the amplifier appear worse than specified.

The apparent input referred offset induced by feedback factor mismatch is derived from the above equation:

$$V_{OSDIFF(APPARENT)} \approx (V_{ICM} - V_{OCM}) \bullet \Delta\beta$$

Using the LTC6405 in a single supply application on a single 5V supply with 1% resistors, and the input common mode grounded, with the V_{OCM} pin biased at 2.5V, the worst case DC offset can induce 25mV of apparent offset voltage. With 0.1% resistors, the worst case apparent offset reduces to 2.5mV.

Input Impedance and Loading Effects

The input impedance looking into the V_{INP} or V_{INM} input of Figure 1 depends on whether or not the sources V_{INP} and V_{INM} are fully differential or not. For balanced input sources ($V_{INP} = -V_{INM}$), the input impedance seen at either input is simply:

$$R_{INP} = R_{INM} = R_I$$

For single ended inputs, because of the signal imbalance at the input, the input impedance actually increases over the balanced differential case. The input impedance looking into either input is:

$$R_{INP} = R_{INM} = \frac{R_I}{\left(1 - \frac{1}{2} \bullet \left(\frac{R_F}{R_I + R_F}\right)\right)}$$

Input signal sources with non-zero output impedances can also cause feedback imbalance between the pair of feedback networks. For the best performance, it is recommended that the input source output impedance be compensated for. If input impedance matching is required by the source, a termination resistor R1 should be chosen (see Figure 4):

$$R1 = \frac{R_{INM} \bullet R_S}{R_{INM} - R_S}$$

According to Figure 4, the input impedance looking into

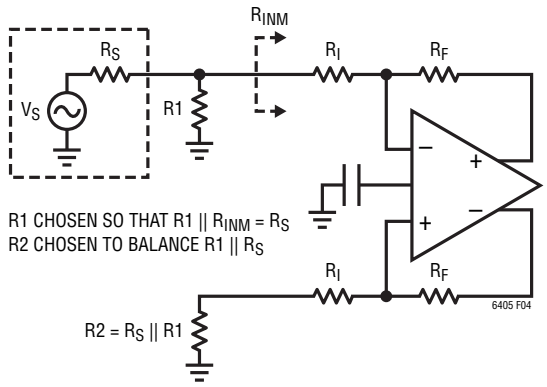


Figure 4. Optimal Compensation for Signal Source Impedance

the differential amp (R_{INM}) reflects the single ended source case, thus:

$$R_{INM} = \frac{R_I}{\left(1 - \frac{1}{2} \bullet \left(\frac{R_F}{R_I + R_F}\right)\right)}$$

R2 is chosen to equal R1 || R_S:

$$R2 = \frac{R1 \bullet R_S}{R1 + R_S}$$

APPLICATIONS INFORMATION

Input Common Mode Voltage Range

The LTC6405's input common mode voltage (V_{ICM}) is defined as the average of the two input voltages, V_{+IN}, and $V_{–IN}$. At the inputs to the actual op amp, the range extends from $V^–$ to V^+. This makes it easy to interface to a wide range of common mode signals, from ground referenced to V_{CC} referenced signals. Moreover, due to external resistive divider action of the gain and feedback resistors, the effective range of signals that can be processed is even wider. The input common mode range at the op amp inputs depends on the circuit configuration (gain), V_{OCM} and V_{CM} (refer to Figure 5). For fully differential input applications, where $V_{INP} = –V_{INM}$, the common mode input is approximately:

$$V_{ICM} = \frac{V_{+IN} + V_{–IN}}{2} \approx V_{OCM} \bullet \left(\frac{R_I}{R_I + R_F} \right) + V_{CM} \bullet \left(\frac{R_F}{R_F + R_I} \right)$$

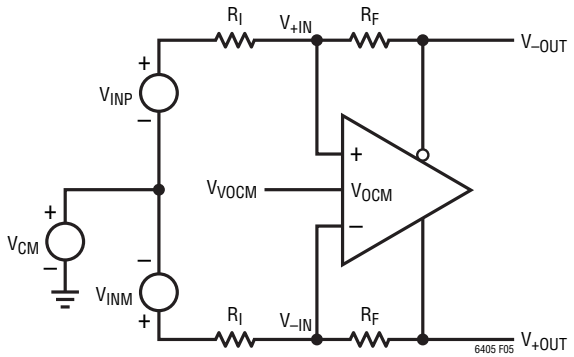


Figure 5. Circuit for Common Mode Range

With single ended inputs, there is an input signal component to the input common mode voltage. Applying only V_{INP} (setting V_{INM} to zero), the input common voltage is approximately:

$$V_{ICM} = \frac{V_{+IN} + V_{–IN}}{2} \approx V_{OCM} \bullet \left(\frac{R_I}{R_I + R_F} \right) + V_{CM} \bullet \left(\frac{R_F}{R_F + R_I} \right) + \frac{V_{INP}}{2} \bullet \left(\frac{R_F}{R_F + R_I} \right)$$

Use the equations above to check that the V_{ICM} at the op amp inputs is within range ($V^–$ to V^+).

Manipulating the Rail-to-Rail Input Stage with V_{TIP}

To achieve rail-to-rail input operation, the LTC6405 features an NPN input stage in parallel with a PNP input stage. When the input common mode voltage is near V^+, the NPNs are active while the PNPs are off. When the input common mode is near $V^–$, the PNPs are active while the NPNs are off. At some range in the middle, both input stages are active. This 'hand-off' operation happens automatically.

In the QFN package, a special pin, V_{TIP}, is made available that can be used to manipulate the 'hand-off' operation between the NPN and PNP input stages. By default, the V_{TIP} pin is internally biased by an internal resistive divider between the supplies, developing a default 2.8V voltage with a 5V supply. If desired, V_{TIP} can be over-driven by an external voltage (the Thevenin equivalent resistance is approximately 17k).

If V_{TIP} is pulled closer to $V^–$, the range over which the NPN input pair remains active is increased, while the range over which the PNP input pair is active is reduced. In applications where the input common mode does not come close to $V^–$, this mode can be used to further improve linearity beyond the specified performance (see Figure 6).

If V_{TIP} is pulled closer to V^+, the range over which the PNP input pair remains active is increased, while the range over which the NPN input pair is active is reduced. In applications where the input common mode does not come close to V^+, this mode can be used to further improve linearity beyond the specified performance.

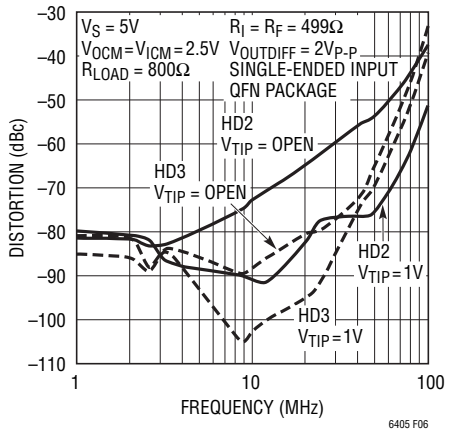


Figure 6. Manipulating V_{TIP} to Improve Harmonic Distortion

APPLICATIONS INFORMATION

Output Common Mode Voltage Range

The output common mode voltage is defined as the average of the two outputs:

$$V_{OUTCM} = V_{OCM} = \frac{V_{+OUT} + V_{-OUT}}{2}$$

The V_{OCM} pin sets this average by an internal common mode feedback loop which internally forces $V_{OUTCM} = V_{OCM}$. The output common mode range extends from 0.5V above V^- to typically 1V below V^+. The V_{OCM} voltage is internally set by a resistive divider between the supplies, developing a default voltage potential of 2.5V with a 5V supply.

In single supply applications, where the LTC6405 is used to interface to an ADC, the optimal common mode input range to the ADC is often determined by the ADC's reference. If the ADC makes a reference available for setting the input common mode voltage, it can be directly tied to the V_{OCM} pin (as long as it is able to drive the 19kΩ Thevenin equivalent input impedance presented by the V_{OCM} pin).

The V_{OCM} pin should be bypassed with a high quality ceramic bypass capacitor of at least 0.01µF to filter any common mode noise rather than being converted to differential noise and to prevent common mode signals on this pin from being inadvertently converted to differential signals by impedance mismatches both externally and internally to the IC.

Output Filter Considerations and Use

Filtering at the output of the LTC6405 is often desired to provide anti-aliasing or to improve signal to noise ratio. To simplify this filtering, the LTC6405 in the QFN package includes an additional pair of differential outputs (+OUTF and –OUTF) which incorporate an internal lowpass RC network with a –3dB bandwidth of 850MHz (Figure 7).

These pins each have an output resistance of 50Ω (tolerance ±12%). Internal capacitances are 1.25pF (tolerance ±15%) to V^- on each filtered output, plus an additional 1.25pF (tolerance ±15%) capacitor connected between the two filtered outputs. This resistor/capacitor combination creates filtered outputs that look like a series 50Ω resistor with a 3.75pF capacitor shunting each filtered output to AC ground, providing a –3dB bandwidth of 850MHz, and a noise bandwidth of 1335MHz. The filter cutoff frequency is easily modified with just a few external components. To increase the cutoff frequency, simply add two equal value resistors, one between +OUT and +OUTF and the other between –OUT and –OUTF (Figure 8). These resistors, in parallel with the internal 50Ω resistors, lower the overall resistance and therefore increase filter bandwidth. For example, to double the filter bandwidth, add two external 50Ω resistors to lower the series filter resistance to 25Ω. The 3.75pF of capacitance remains unchanged, so filter bandwidth doubles. Keep in mind, the series resistance also serves to decouple the outputs from load capaci-

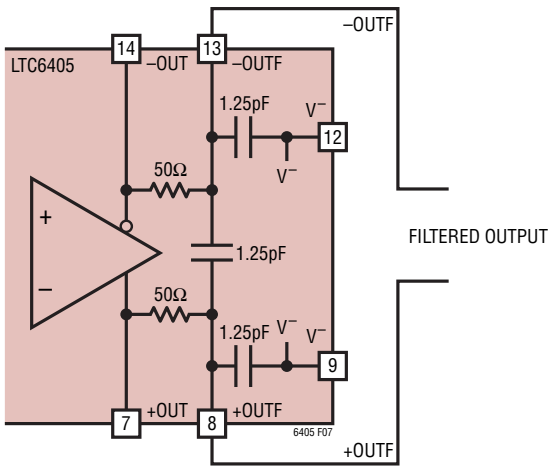


Figure 7. LTC6405 Internal Filter Topology

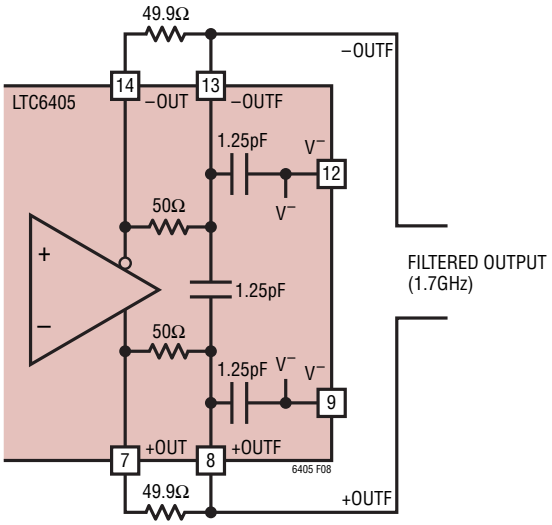


Figure 8. LTC6405 Filter Topology Modified for 2x Filter Bandwidth (Two External Resistors)

APPLICATIONS INFORMATION

tance. The outputs of the LTC6405 are designed to drive 5pF to ground, so care should be taken to not lower the effective impedance between +OUT and +OUTF or –OUT and –OUTF below 15Ω.

To decrease filter bandwidth, add two external capacitors, one from +OUTF to ground, and the other from –OUTF to ground. A single differential capacitor connected between +OUTF and –OUTF can also be used, but since it is being driven differentially it will appear at each filtered output as a single-ended capacitance of twice the value. To halve the filter bandwidth, for example, two 3.9pF capacitors could be added (one from each filtered output to ground). Alternatively, one 1.8pF capacitor could be added between the filtered outputs, which also halves the filter bandwidth. Combinations of capacitors could be used as well; a three capacitor solution of 1.2pF from each filtered output to ground plus a 1.2pF capacitor between the filtered outputs would also halve the filter bandwidth (Figure 9).

Noise Considerations

The LTC6405's input referred voltage noise is 1.6nV/√Hz. Its input referred current noise is 2.4pA/√Hz. In addition to the noise generated by the amplifier, the surrounding feedback resistors also contribute noise. A noise model is shown in Figure 10. The output noise generated by both the amplifier and the feedback components is governed by the equation:

$$e_{no} = \sqrt{\left(e_{ni} \bullet \left(1+\frac{R_F}{R_I}\right)\right)^2 + 2 \bullet \left(I_n \bullet R_F\right)^2 + 2 \bullet \left(e_{nRI} \bullet \left(\frac{R_F}{R_I}\right)\right)^2 + 2 \bullet e_{nRF}^{\ 2}}$$

A plot of this equation, and a plot of the noise generated by the feedback components for the LTC6405 is shown in Figure 11.

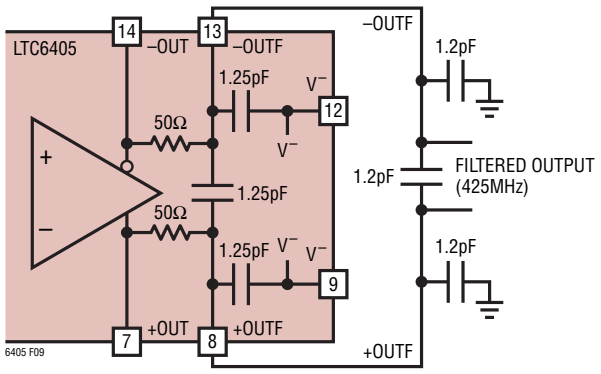


Figure 9. LTC6405 Filter Topology Modified for 1/2x Filter Bandwidth (Three External Capacitors)

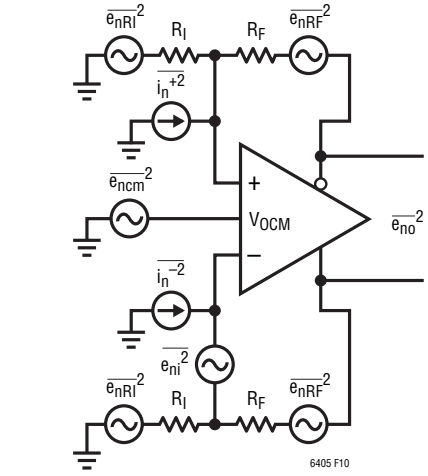


Figure 10. Noise Model of the LTC6405

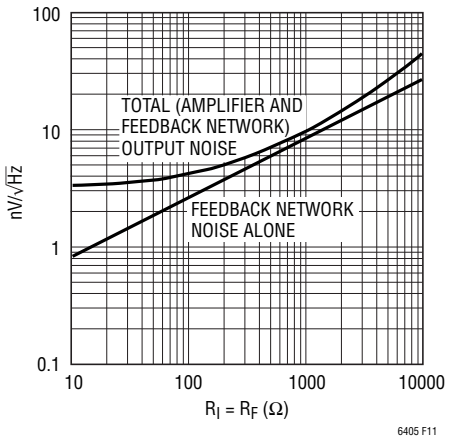


Figure 11. LTC6405 Output Spot Noise vs Spot Noise Contributed by Feedback Network Alone

APPLICATIONS INFORMATION

The LTC6405's input referred voltage noise contributes the equivalent noise of a 155Ω resistor. When the feedback network is comprised of resistors whose values are less than this, the LTC6405's output noise is voltage noise dominant (see Figure 11):

$$e_{no} \approx e_{ni} \bullet \left(1+\frac{R_F}{R_I}\right)$$

Feedback networks consisting of resistors with values greater than about 200Ω will result in output noise which is resistor noise and amplifier current noise dominant.

$$e_{no} \approx \sqrt{2} \bullet \sqrt{\left(I_n \bullet R_F\right)^2 + \left(1+\frac{R_F}{R_I}\right) \bullet 4 \bullet k \bullet T \bullet R_F}$$

Lower resistor values (<100Ω) always result in lower noise at the penalty of increased distortion due to increased loading of the feedback network on the output. Higher resistor values (but still less than <500Ω) will result in higher output noise, but typically improved distortion due to less loading on the output. The optimal feedback resistance for the LTC6405 runs in between 100Ω to 500Ω.

The differential filtered outputs +OUTF and –OUTF will have a little higher noise than the unfiltered outputs (due to the two 50Ω resistors which contribute 0.9nV/$\sqrt{Hz}$ each), but can provide superior signal-to-noise due to the output noise filtering.

Layout Considerations

Because the LTC6405 is a very high speed amplifier, it is sensitive to both stray capacitance and stray inductance. In the QFN package, three pairs of power supply pins are provided to keep the power supply inductance as low as possible to prevent any degradation of amplifier 2nd harmonic performance. It is critical that close attention be paid to supply bypassing. For single supply applications it is recommended that high quality 0.1µF surface mount ceramic bypass capacitor be placed directly between each V^+ and $V^–$ pin with direct short connections. The $V^–$ pins should be tied directly to a low impedance ground plane with minimal routing. For dual (split) power supplies, it is recommended that additional high quality, 0.1µF ceramic capacitors are used to bypass V^+ to ground and $V^–$ to ground, again with minimal routing. For driving large loads (<200Ω), additional bypass capacitance may be needed for optimal performance. Keep in mind that small geometry (e.g., 0603) surface mount ceramic capacitors have a much higher self resonant frequency than do leaded capacitors, and perform best in high speed applications.

Any stray parasitic capacitances to ground at the summing junctions, +IN and –IN, should be minimized. This becomes especially true when the feedback resistor network uses resistor values >500Ω in circuits with $R_F = R_I$. Always keep in mind the differential nature of the LTC6405, and that it is critical that the load impedances seen by both outputs (stray or intended), should be as balanced and symmetric as possible. This will help preserve the natural balance of the LTC6405, which minimizes the generation of even order harmonics, and improves the rejection of common mode signals and noise.

It is highly recommended that the V_{OCM} pin be bypassed to ground with a high quality ceramic capacitor whose value exceeds 0.01µF. This will help stabilize the common mode feedback loop as well as prevent thermal noise from the internal voltage divider and other external sources of noise from being converted to differential noise due to divider mismatches in the feedback networks. It is also recommended that the resistive feedback networks be comprised of 1% resistors (or better) to enhance the output common mode rejection. This will also prevent V_{OCM} input referred common mode noise of the common mode amplifier path (which cannot be filtered) from being converted to differential noise, degrading the differential noise performance.

Feedback factor mismatch has a weak effect on distortion. Using 1% or better resistors will limit any mismatch from impacting amplifier linearity. However, in single supply level shifting applications where there is a voltage difference between the input common mode voltage and the output common mode voltage, resistor mismatch can make the apparent voltage offset of the amplifier appear worse than specified.

APPLICATIONS INFORMATION

Interfacing the LTC6405 to A/D Converters

Rail-to-rail input and fast settling time make the LTC6405 ideal for interfacing to low voltage, single supply, differential input ADCs. The sampling process of ADCs create a sampling glitch caused by switching in the sampling capacitor on the ADC front end which momentarily "shorts" the output of the amplifier as charge is transferred between the amplifier and the sampling capacitor. The amplifier must recover and settle from this load transient before this acquisition period ends for a valid representation of the input signal. In general, the LTC6405 will settle much more quickly from these periodic load impulses than from a 2V input step, but it is a good idea to place an R-C filter network between the differential outputs of the LTC6405 and the input of the ADC to help absorb the charge injection that comes out of the ADC from the sampling process. The capacitance of the filter network serves as a charge reservoir to provide high frequency charging during the sampling process, while the resistors of the filter network are used to dampen and attenuate any charge kickback from the ADC. The selection of the R-C time constant is trial and error for a given ADC, but the following guidelines are recommended: Choosing too large of a resistor in the decoupling network leaving insufficient settling time will create a voltage divider between the dynamic input impedance of the ADC and the decoupling resistors. Choosing too small of a resistor will possibly prevent the resistor from properly dampening the load transient caused by the sampling process, prolonging the time required for settling. In 16-bit applications, this will typically require a minimum of 11 R-C time constants. It is recommended that the capacitor chosen have a high quality dielectric (such as C0G multilayer ceramic).

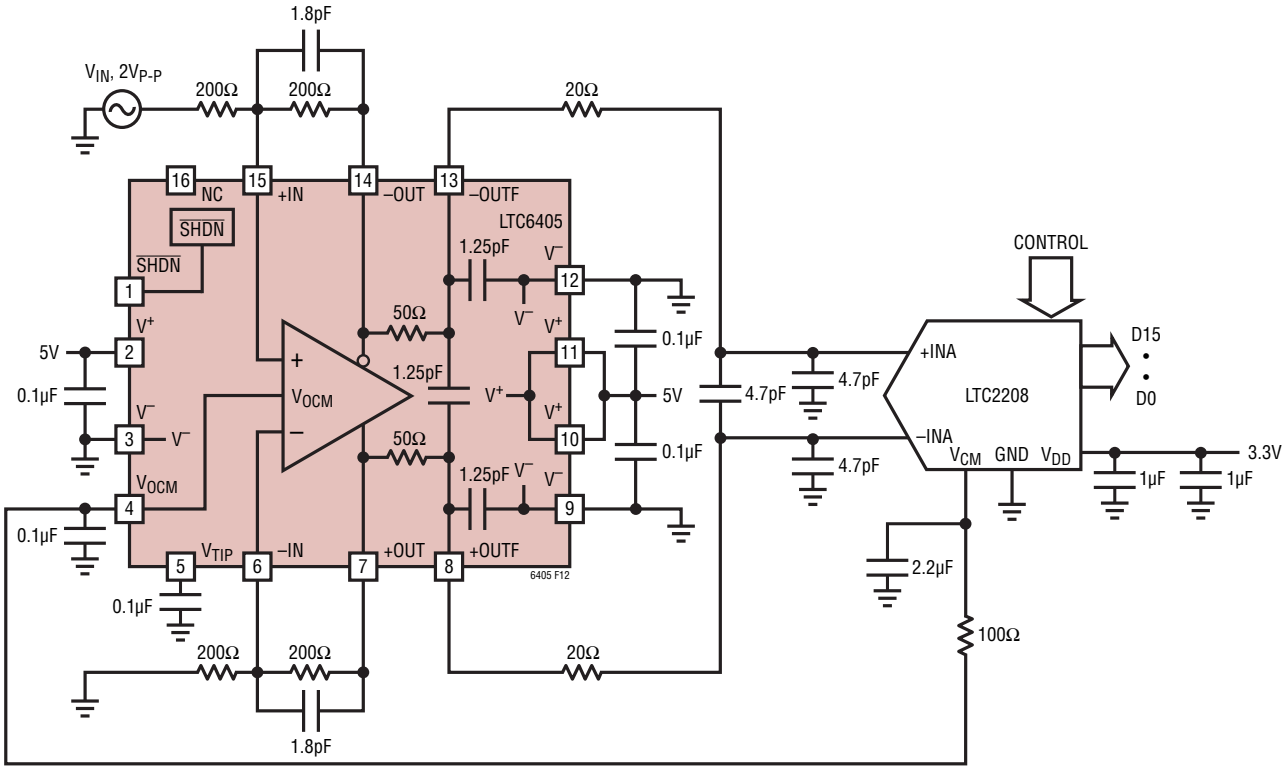
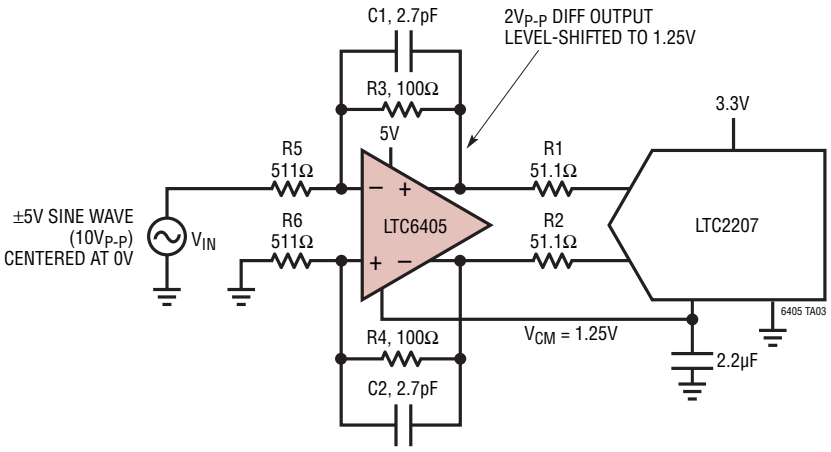


Figure 12. Interfacing the LTC6405 to an ADC

TYPICAL APPLICATION

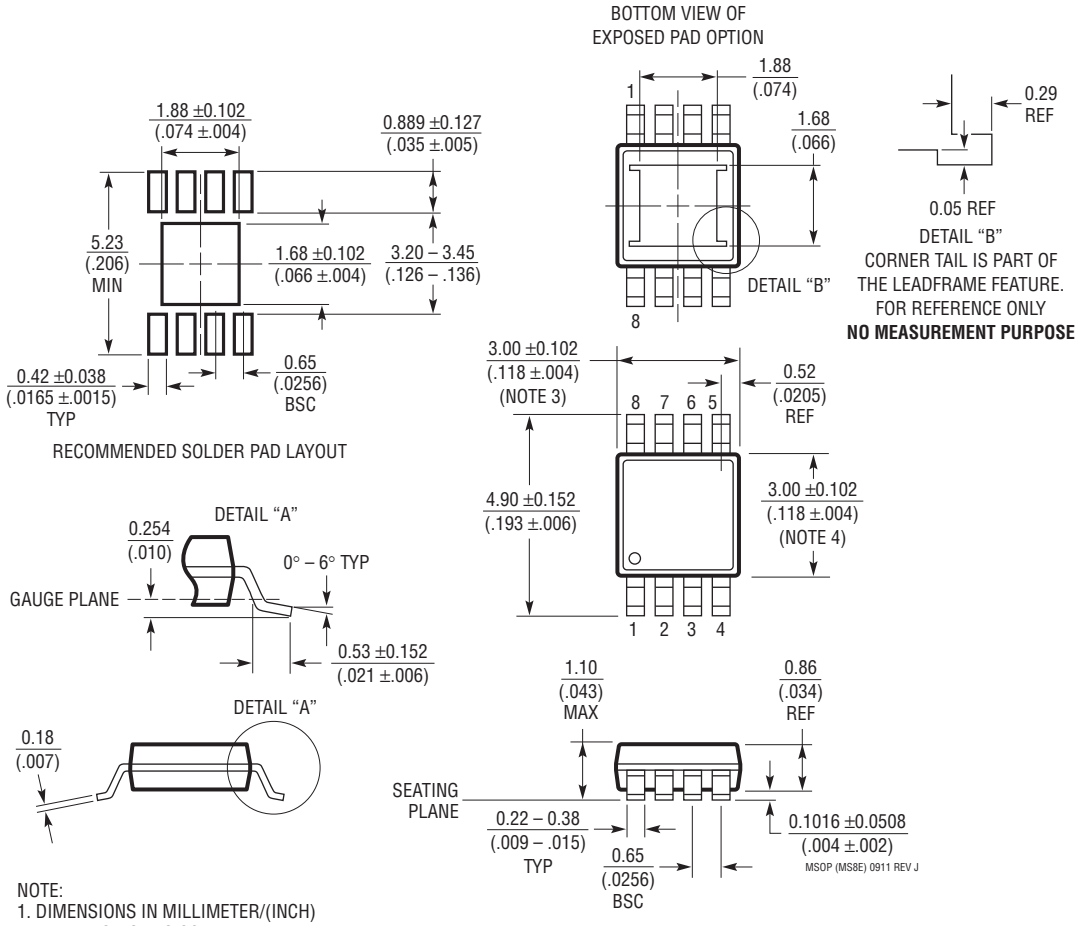
Attenuating and Level Shifting a Single-Ended ±5V Signal to a Differential $2V_{P-P}$ Signal at a 1.25V Common Mode



PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

MS8E Package
8-Lead Plastic MSOP, Exposed Die Pad
(Reference LTC DWG # 05-08-1662 Rev J)

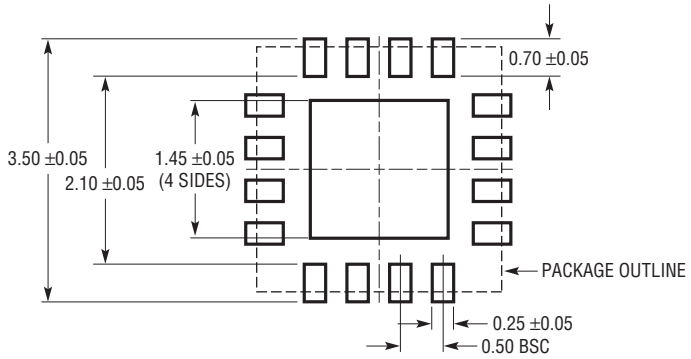


NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX
6. EXPOSED PAD DIMENSION DOES INCLUDE MOLD FLASH. MOLD FLASH ON E-PAD
   SHALL NOT EXCEED 0.254mm (.010") PER SIDE.

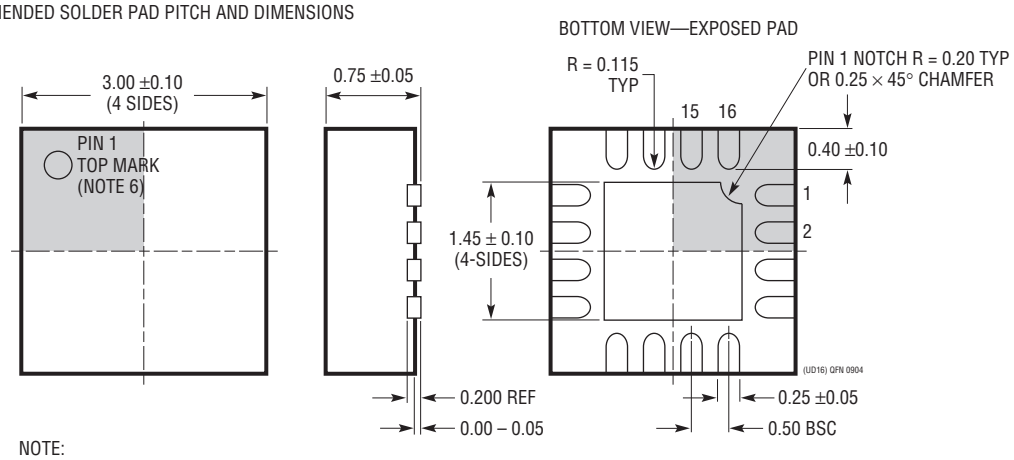
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

UD Package
16-Lead Plastic QFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1691 Rev Ø)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



NOTE:
1. DRAWING CONFORMS TO JEDEC PACKAGE OUTLINE MO-220 VARIATION (WEED-2)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

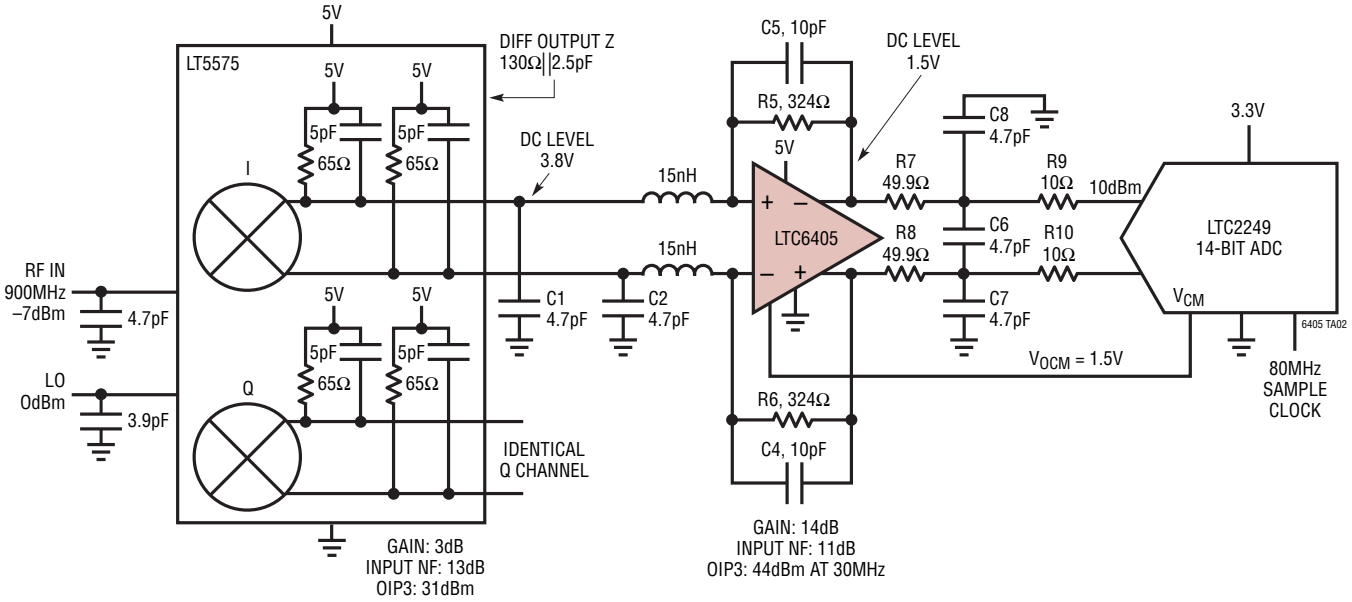
REVISION HISTORY (Revision history begins at Rev B)

REV	DATE	DESCRIPTION	PAGE NUMBER
B	02/13	Changed operating voltage upper range from 5.5V to 5.25V	1, 3, 4
		Changed voltage max spec from 0.4V to 0.45V	3

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

TYPICAL APPLICATION

DC-Coupled Level Shifting of Demodulator Output



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1993-2/LT1993-4/ LT1993-10	800MHz/900MHz/700MHz Low Distortion, Low Noise Differential Amplifier/ADC Driver	A_V = 2V/V / A_V = 4V/V / A_V = 10V/V, NF = 12.3dB/14.5dB/ 12.7dB, OIP3 = 38dBm/40dBm/40dBm at 70MHz
LT1994	Low Noise, Low Distortion Fully differential Input/Output Amplifier/Driver	Low Distortion, $2V_{P-P}$, 1MHz: –94dBc, 13mA, Low Noise: $3nV/\sqrt{Hz}$
LTC6400-8/LTC6400-14/ LTC6400-20/LTC6400-26	1.8GHz Low Noise, Low Distortion, Differential ADC Driver	300MHz IF Amplifier, A_V = 20dB/26dB
LTC6401-8/LTC6401-14/ LTC6401-20/LTC6401-26	1.3GHz Low Noise, Low Distortion, Differential ADC Driver	140MHz IF Amplifier, A_V = 20dB/26dB
LT6402-6/LT6402-12/ LT6402-20	300MHz/300MHz/300MHz Low Distortion, Low Noise Differential Amplifier/ADC Driver	A_V = 6dB/A_V = 12dB/A_V = 20dB, NF = 18.6dB/15dB/12.4dB, OIP3 = 49dBm/43dBm/51dBm at 20MHz
LTC6404-1/ LTC6404-2/ LTC6404-4	600MHz Low Noise, Low Distortion, Differential ADC Driver	$1.5nV/\sqrt{Hz}$ Noise, –90dBc Distortion at 10MHz
LTC6406	3GHz Low Noise, 3V, Rail-to-Rail Input Differential Amplifier/ Driver	$1.6nV/\sqrt{Hz}$ Noise, –70dBc Distortion at 50MHz, 18mA, 3V Supply
LTC6411	Low Power Differential ADC Driver/Dual Selectable Gain Amplifier	16mA Supply Current, IMD3 = –83dBC at 70MHz, A_V = 1, –1, or 2
LT6600-2.5/LT6600-5/ LT6600-10/LT6600-20	Very Low Noise, Fully Differential Amplifier and 4th Order Filter	2.5MHz/5MHz/10MHz/20MHz Integrated Filter, 3V Supply, SO-8 Package
LTC6403-1	200MHz Low Noise, Low Power Differential ADC Driver	–95dBc Distortion at 3MHz, 10.8mA Supply Current

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