Precision, Low Power Rail-to-Rail Input/Output Differential Op Amp/SAR ADC Driver

FEATURES

- **1mA Supply Current**
- **Single 2.8V to 5.25V supply**
- **Fully Differential Input and Output**
- **200µV Max Offset Voltage**
- **260nA Max Input Bias Current**
- **Fast Settling: 550ns to 18-Bit, 8V$_{P-P}$ Output**
- Low Distortion: –116dBc at 1kHz, 8V$_{P-P}$
- Rail-to-Rail Inputs and Outputs
- 3.9nV/√Hz Input-Referred Noise
- 180MHz Gain-Bandwidth Product
- 34MHz –3dB Bandwidth
- Low Power Shutdown: 70µA
- 8-Lead MSOP and 3mm × 3mm 8-Lead DFN Packages

APPLICATIONS

- 16-Bit and 18-Bit SAR ADC Drivers
- Single-Ended-to-Differential Conversion
- Low Power Pipeline ADC Driver
- Differential Line Drivers
- Battery-Powered Instrumentation

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DESCRIPTION

The LTC®6362 is a low power, low noise differential op amp with rail-to-rail input and output swing that has been optimized to drive low power SAR ADCs. The LTC6362 draws only 1mA of supply current in active operation, and features a shutdown mode in which the current consumption is reduced to 70µA.

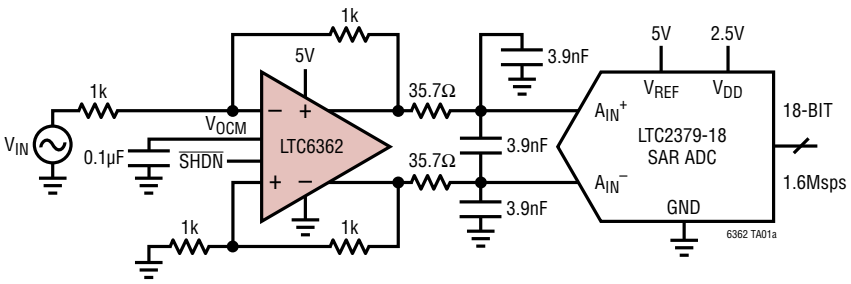
The amplifier may be configured to convert a single-ended input signal to a differential output signal, and is capable of being operated in an inverting or noninverting configuration.

Low offset voltage, low input bias current, and a stable high impedance configuration make this amplifier suitable for use not only as an ADC driver but also earlier in the signal chain, to convert a precision sensor signal to a balanced (differential) signal for processing in noisy industrial environments.

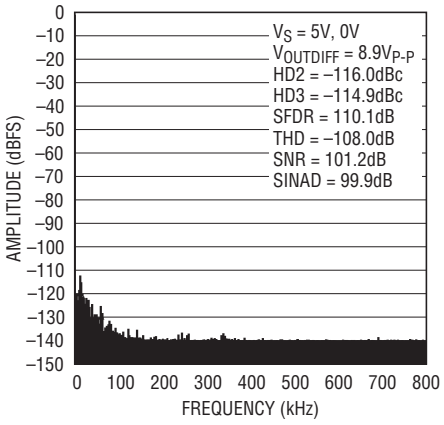
The LTC6362 is available in an 8-lead MSOP package and also in a compact 3mm × 3mm 8-pin leadless DFN package, and operates with guaranteed specifications over a –40°C to 125°C temperature range.

TYPICAL APPLICATION

DC-Coupled Interface from a Ground-Referenced Single-Ended Input to an LTC2379-18 SAR ADC



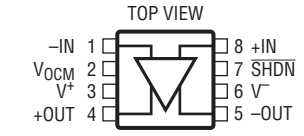
LTC6362 Driving LTC2379-18
f_{IN} = 2kHz, –1dBFS, 16384-Point FFT



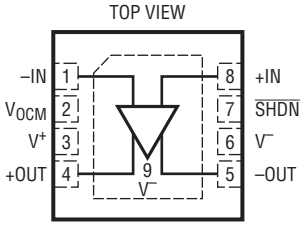
ABSOLUTE MAXIMUM RATINGS (Note 1)

Total Supply Voltage ($V^+ – V^–$) 5.5V
Input Current (+IN, –IN, V_{OCM}, $\overline{SHDN}$) (Note 2) ... ±10mA
Output Short-Circuit Duration (Note 3) ..... Indefinite
Operating Temperature Range (Note 4)
LTC6362C/LTC6362I.....–40°C to 85°C
LTC6362H.....–40°C to 125°C
Specified Temperature Range (Note 5)
LTC6362C..... 0°C to 70°C
LTC6362I .....–40°C to 85°C
LTC6362H..... –40°C to 125°C
Maximum Junction Temperature ..... 150°C
Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



MS8 PACKAGE
8-LEAD PLASTIC MSOP
T_{JMAX} = 150°C, θ_{JA} = 273°C/W, θ_{JC} = 45°C/W



DD PACKAGE
8-LEAD (3mm × 3mm) PLASTIC DFN
T_{JMAX} = 150°C, θ_{JA} = 39.7°C/W, θ_{JC} = 45°C/W
EXPOSED PAD (PIN 9) IS $V^–$, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE
LTC6362CMS8#PBF	LTC6362CMS8#TRPBF	LTGCN	8-Lead Plastic MSOP	0°C to 70°C
LTC6362IMS8#PBF	LTC6362IMS8#TRPBF	LTGCN	8-Lead Plastic MSOP	–40°C to 85°C
LTC6362HMS8#PBF	LTC6362HMS8#TRPBF	LTGCN	8-Lead Plastic MSOP	–40°C to 125°C
LTC6362CDD#PBF	LTC6362CDD#TRPBF	LGCM	8-Lead (3mm × 3mm) Plastic DFN	0°C to 70°C
LTC6362IDD#PBF	LTC6362IDD#TRPBF	LGCM	8-Lead (3mm × 3mm) Plastic DFN	–40°C to 85°C
LTC6362HDD#PBF	LTC6362HDD#TRPBF	LGCM	8-Lead (3mm × 3mm) Plastic DFN	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V^+ = 5V, V^- = 0V, V_{CM} = V_{OCM} = V_{ICM} = 2.5V, $V_{\overline{SHDN}}$ = open. V_S is defined as ($V^+ - V^-$). V_{OUTCM} is defined as ($V_{+OUT} + V_{-OUT}$)/2. V_{ICM} is defined as ($V_{+IN} + V_{-IN}$)/2. $V_{OUTDIFF}$ is defined as ($V_{+OUT} - V_{-OUT}$).

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OSDIFF} (Note 6)	Differential Offset Voltage (Input Referred)	V_S = 3V					
		V_{ICM} =1.5V			50	200	µV
			●			350	µV
		V_{ICM} = 2.75V			65	250	µV
			●			600	µV
		V_S = 5V					
		V_{ICM} = 2.5V			50	200	µV
			●			350	µV
		V_{ICM} = 4.5V			75	260	µV
			●			600	µV
$\Delta V_{OSDIFF}/\Delta T$ (Note 7)	Differential Offset Voltage Drift (Input Referred)	V_S = 3V	●		0.9	2.5	µV/°C
		V_S = 5V	●		0.9	2.5	µV/°C
I_B (Note 8)	Input Bias Current	V_S = 3V					
		V_{ICM} =1.5V			±100	±350	nA
			●			±500	nA
		V_{ICM} = 2.5V			±75	±350	nA
			●			±850	nA
		V_S = 5V					
		V_{ICM} = 2.5V			±75	±260	nA
			●			±460	nA
		V_{ICM} = 4.5V			±75	±350	nA
			●			±850	nA
$\Delta I_B/\Delta T$	Input Bias Current Drift	V_S = 3V	●		1.1		nA/°C
		V_S = 5V	●		0.9		nA/°C
I_{OS} (Note 8)	Input Offset Current	V_S = 3V					
		V_{ICM} =1.5V			±75	±325	nA
			●			±650	nA
		V_{ICM} = 2.5V			±125	±425	nA
			●			±1200	nA
		V_S = 5V					
		V_{ICM} =2.5V			±75	±325	nA
			●			±500	nA
		V_{ICM} = 4.5V			±125	±425	nA
			●			±1200	nA
R_{IN}	Input Resistance	Common Mode			14		MΩ
		Differential Mode			32		kΩ
C_{IN}	Input Capacitance	Differential Mode			2		pF
e_n	Differential Input Noise Voltage Density	f = 100kHz, Not Including R_I/R_F Noise			3.9		nV/√Hz
i_n	Input Noise Current Density	f = 100kHz, Not Including R_I/R_F Noise			0.8		pA/√Hz
e_{nvocm}	Common Mode Noise Voltage Density	f = 100kHz			14.3		nV/√Hz
V_{ICMR} (Note 9)	Input Common Mode Range	V_S = 3V	●	0		3	V
		V_S = 5V	●	0		5	V
CMRRI (Note 10)	Input Common Mode Rejection Ratio (Input Referred) $\Delta V_{ICM}/\Delta V_{OSDIFF}$	V_S = 3V, V_{ICM} from 0V to 3V	●	70	95		dB
		V_S = 5V, V_{ICM} from 0V to 5V	●	73	98		dB
CMRRIO (Note 10)	Output Common Mode Rejection Ratio (Input Referred) $\Delta V_{OCM}/\Delta V_{OSDIFF}$	V_S = 3V, V_{OCM} from 0.5V to 2.5V	●	75	100		dB
		V_S = 5V, V_{OCM} from 0.5V to 4.5V	●	55	90		dB
PSRR (Note 11)	Differential Power Supply Rejection ($\Delta V_S/\Delta V_{OSDIFF}$)	V_S = 2.8V to 5.25V	●	80	105		dB
PSRRCM (Note 11)	Output Common Mode Power Supply Rejection ($\Delta V_S/\Delta V_{OSCM}$)	V_S = 2.8V to 5.25V	●	58	72		dB

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V^+ = 5V, V^- = 0V, V_{CM} = V_{OCM} = V_{ICM} = 2.5V, $V_{\overline{SHDN}}$ = open. V_S is defined as ($V^+ – V^-$). V_{OUTCM} is defined as ($V_{+OUT} + V_{–OUT}$)/2. V_{ICM} is defined as ($V_{+IN} + V_{–IN}$)/2. $V_{OUTDIFF}$ is defined as ($V_{+OUT} – V_{–OUT}$).

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
GCM	Common Mode Gain ($\Delta V_{OUTCM}/\Delta V_{OCM}$)	V_S = 3V, V_{OCM} from 0.5V to 2.5V V_S = 5V, V_{OCM} from 0.5V to 4.5V	● ●		1 1		V/V V/V
ΔGCM	Common Mode Gain Error 100 • (GCM – 1)	V_S = 3V, V_{OCM} from 0.5V to 2.5V V_S = 5V, V_{OCM} from 0.5V to 4.5V	● ●		±0.07 ±0.07	±0.16 ±0.4	% %
BAL	Output Balance ($\Delta V_{OUTCM}/\Delta V_{OUTDIFF}$)	$\Delta V_{OUTDIFF}$ = 2V Single-Ended Input Differential Input	 ● ●		 –57 –57	 –35 –35	 dB dB
A_{VOL}	Open-Loop Voltage Gain				95		dB
V_{OSCM}	Common Mode Offset Voltage ($V_{OUTCM} – V_{OCM}$)	V_S = 3V V_S = 5V	● ●		±6 ±6	±30 ±30	mV mV
$\Delta V_{OSCM}/\Delta T$	Common Mode Offset Voltage Drift		●		45		µV/°C
V_{OUTCMR} (Note 9)	Output Signal Common Mode Range (Voltage Range for the V_{OCM} Pin)	V_{OCM} Driven Externally, V_S = 3V V_{OCM} Driven Externally, V_S = 5V	● ●	0.5 0.5		2.5 4.5	V V
V_{OCM}	Self-Biased Voltage at the V_{OCM} Pin	V_{OCM} Not Connected, V_S = 3V V_{OCM} Not Connected, V_S = 5V	● ●	1.475 2.475	1.5 2.5	1.525 2.525	V V
R_{INVOCM}	Input Resistance, V_{OCM} Pin		●	110	170	230	kΩ
V_{OUT}	Output Voltage, High, Either Output Pin	I_L= 0mA, V_S = 3V I_L = –5mA, V_S = 3V	● ●	2.85 2.75	2.93 2.85		V V
		I_L= 0mA, V_S = 5V I_L = –5mA, V_S = 5V	● ●	4.8 4.7	4.93 4.85		V V
	Output Voltage, Low , Either Output Pin	I_L= 0mA, V_S = 3V I_L = 5mA, V_S = 3V	● ●		0.05 0.13	0.15 0.3	V V
		I_L= 0mA, V_S = 5V I_L = 5mA, V_S = 5V	● ●		0.05 0.13	0.2 0.4	V V
I_{SC}	Output Short-Circuit Current, Either Output Pin	V_S = 3V V_S = 5V	● ●	13 15	25 35		mA mA
SR	Slew Rate	Differential 8V_{P-P} Output			45		V/µs
GBWP	Gain-Bandwidth Product	f_{TEST} = 200kHz	 ●	145 90	180		MHz MHz
$f_{–3dB}$	–3dB Bandwidth	R_I = R_F = 1k			34		MHz
HD2/HD3	2nd/3rd Order Harmonic Distortion Single-Ended Input	f = 1kHz, V_{OUT} = 8V_{P-P} f = 10kHz, V_{OUT} = 8V_{P-P} f = 100kHz, V_{OUT} = 8V_{P-P}			–120/–116 –106/–103 –84/–76		dBc dBc dBc
t_s	Settling Time to a 2V_{P-P} Output Step	0.1% 0.01% 0.0015% (16-Bit) 4ppm (18-Bit)			160 180 230 440		ns ns ns ns
	Settling Time to a 8V_{P-P} Output Step	0.1% 0.01% 0.0015% (16-Bit) 4ppm (18-Bit)			230 300 460 550		ns ns ns ns
V_S (Note 12)	Supply Voltage Range		●	2.8		5.25	V
I_S	Supply Current	V_S = 3V, Active	 ●		0.9	0.96 1.05	mA mA
		V_S = 3V, Shutdown	●		55	130	µA
		V_S = 5V, Active	 ●		1	1.06 1.18	mA mA
		V_S = 5V, Shutdown	●		70	140	µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V^+ = 5V, V^- = 0V, V_{CM} = V_{OCM} = V_{ICM} = 2.5V, $V_{\overline{SHDN}}$ = open. V_S is defined as ($V^+ – V^-$). V_{OUTCM} is defined as ($V_{+OUT} + V_{–OUT}$)/2. V_{ICM} is defined as ($V_{+IN} + V_{–IN}$)/2. $V_{OUTDIFF}$ is defined as ($V_{+OUT} – V_{–OUT}$).

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IL}	$\overline{SHDN}$ Input Logic Low		●			0.8	V
V_{IH}	$\overline{SHDN}$ Input Logic High		●	2			V
t_{ON}	Turn-On Time				2		µs
t_{OFF}	Turn-Off Time				2		µs

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Input pins (+IN, –IN, V_{OCM} and $\overline{SHDN}$) are protected by steering diodes to either supply. If the inputs should exceed either supply voltage, the input current should be limited to less than 10mA. In addition, the inputs +IN, –IN are protected by a pair of back-to-back diodes. If the differential input voltage exceeds 1.4V, the input current should be limited to less than 10mA.

Note 3: A heat sink may be required to keep the junction temperature below the absolute maximum rating when the output is shorted indefinitely.

Note 4: The LTC6362C and LTC6362I are guaranteed functional over the operating temperature range of –40°C to 85°C. The LTC6362H is guaranteed functional over the operating temperature range of –40°C to 125°C.

Note 5: The LTC6362C is guaranteed to meet specified performance from 0°C to 70°C.The LTC6362I is guaranteed to meet specified performance from –40°C to 85°C. The LTC6362C is designed, characterized and expected to meet specified performance from –40°C to 85°C, but is not tested or QA sampled at these temperatures. The LTC6362H is guaranteed to meet specified performance from –40°C to 125°C.

Note 6: Differential input referred offset voltage includes offset due to input offset current across 1k source resistance.

Note 7: Maximum differential input referred offset voltage drift is determined by a large sampling of typical parts. Drift is not guaranteed by test or QA sampled at this value.

Note 8: Input bias current is defined as the maximum of the input currents flowing into either of the input pins (–IN and +IN). Input Offset current is defined as the difference between the input currents ($I_{OS} = I_B^+ – I_B^-$).

Note 9: Input common mode range is tested by verifying that at the limits stated in the Electrical Characteristics table, the differential offset (V_{OSDIFF}) and common mode offset (V_{OSCM}) have not deviated by more than ±1mV and ±35mV respectively compared to the V_{ICM} = 2.5V (at V_S = 5V) and V_{ICM} = 1.5V (at V_S = 3V) cases.

Output common mode range is tested by verifying that at the limits stated in the Electrical Characteristics table, the common mode offset (V_{OSCM}) has not deviated by more than ±15mV compared to the V_{OCM} = 2.5V (at V_S = 5V) and V_{OCM} = 1.5V (at V_S = 3V) cases.

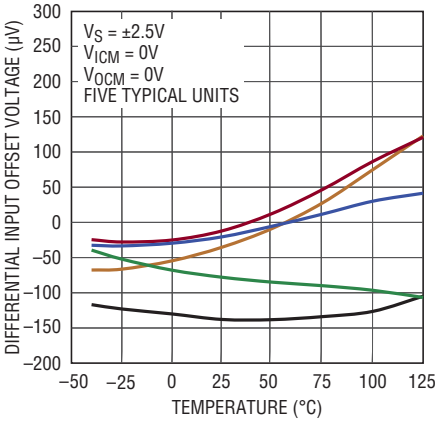
Note 10: Input CMRR is defined as the ratio of the change in the input common mode voltage at the pins +IN or –IN to the change in differential input referred offset voltage. Output CMRR is defined as the ratio of the change in the voltage at the V_{OCM} pin to the change in differential input referred offset voltage. This specification is strongly dependent on feedback ratio matching between the two outputs and their respective inputs and it is difficult to measure actual amplifier performance (see Effects of Resistor Pair Mismatch in the Applications Information section of this data sheet). For a better indicator of actual amplifier performance independent of feedback component matching, refer to the PSRR specification.

Note 11: Differential power supply rejection (PSRR) is defined as the ratio of the change in supply voltage to the change in differential input referred offset voltage. Common mode power supply rejection (PSRRCM) is defined as the ratio of the change in supply voltage to the change in the common mode offset voltage.

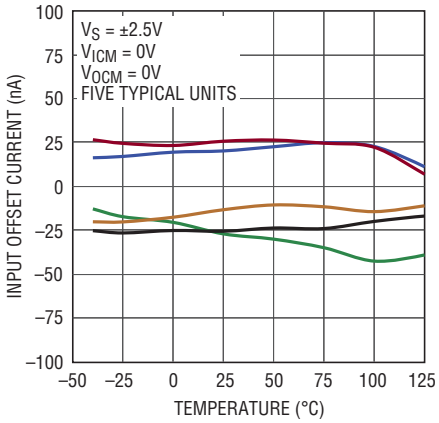
Note 12: Supply voltage range is guaranteed by power supply rejection ratio test.

TYPICAL PERFORMANCE CHARACTERISTICS

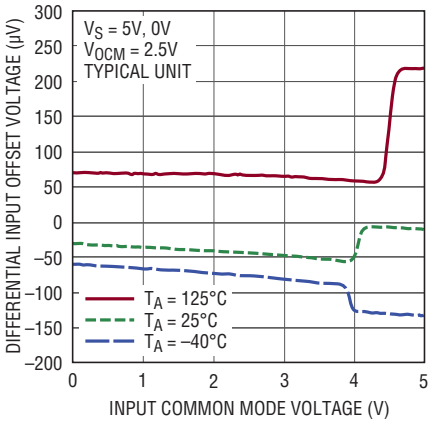
Differential Input Offset Voltage vs Temperature



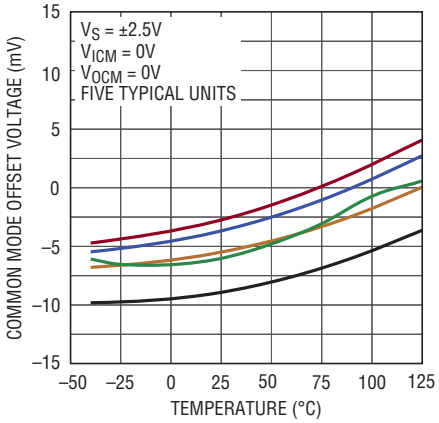
Input Offset Current vs Temperature



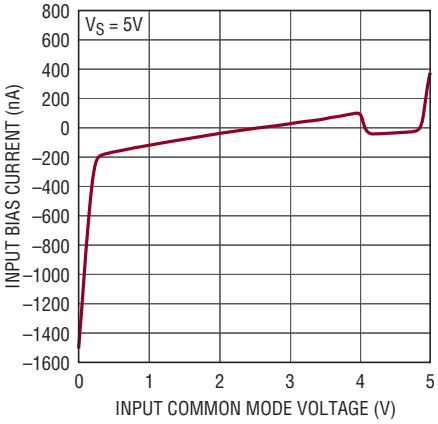
Differential Input Offset Voltage vs Input Common Mode Voltage



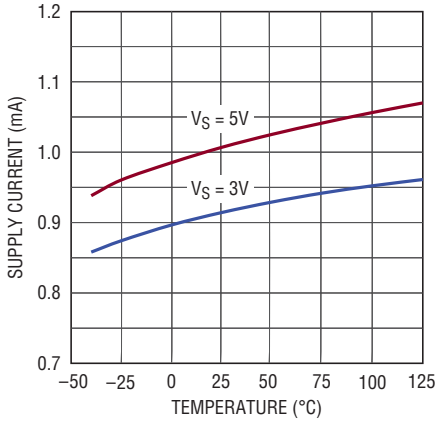
Common Mode Offset Voltage vs Temperature



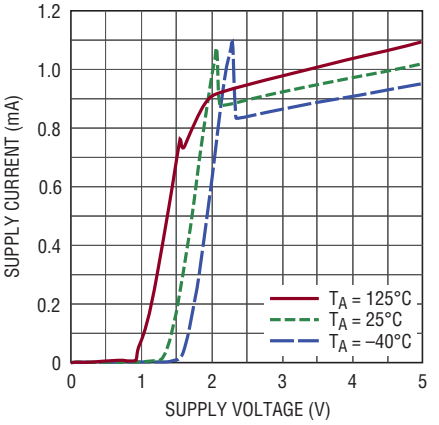
Input Bias Current vs Input Common Mode Voltage



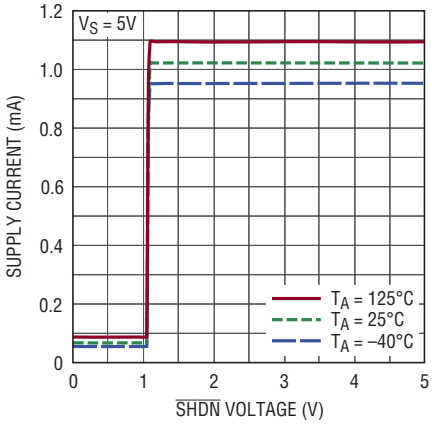
Supply Current vs Temperature



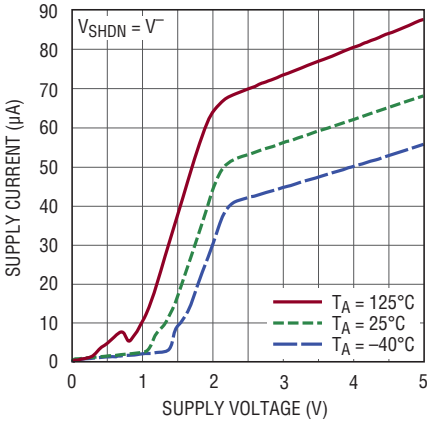
Supply Current vs Supply Voltage



Supply Current vs $\overline{SHDN}$ Voltage

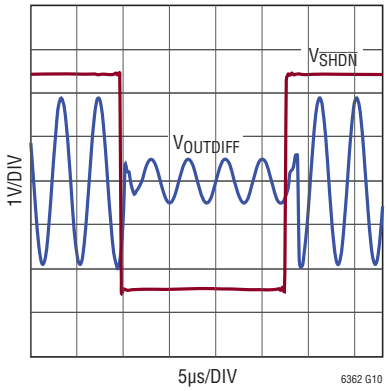


Shutdown Supply Current vs Supply Voltage

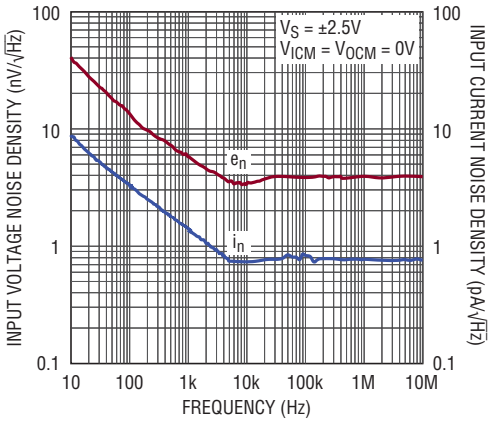


TYPICAL PERFORMANCE CHARACTERISTICS

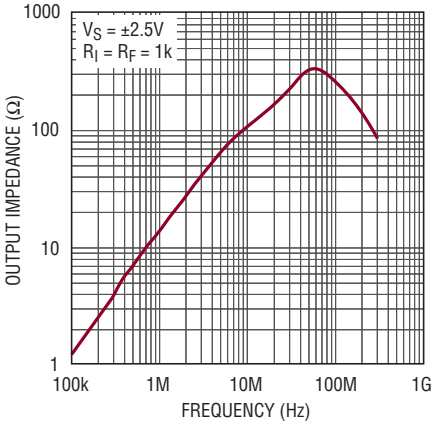
Turn-On and Turn-Off Transient Response



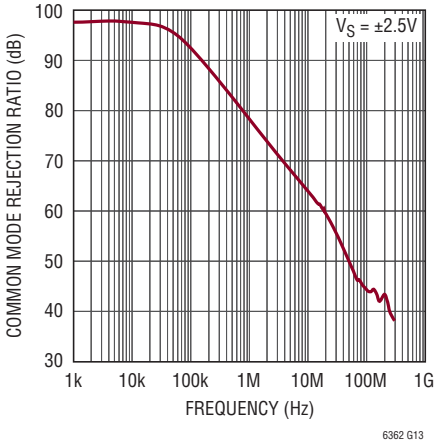
Input Noise Density vs Frequency



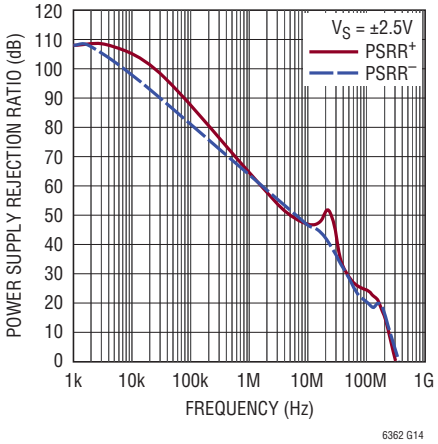
Differential Output Impedance vs Frequency



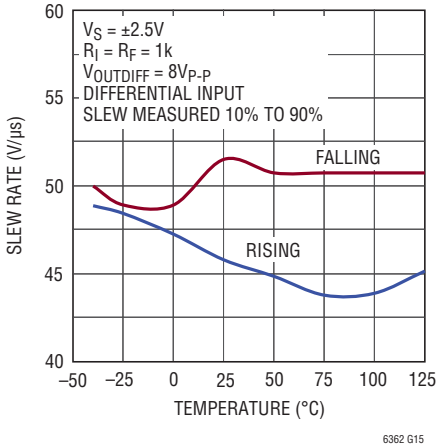
Common Mode Rejection Ratio vs Frequency



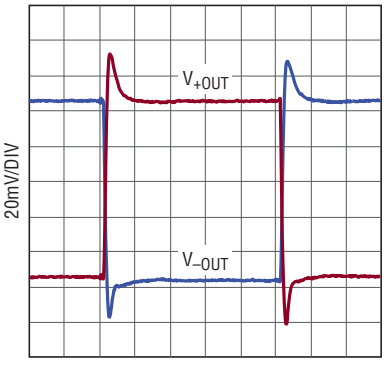
Differential Power Supply Rejection Ratio vs Frequency



Slew Rate vs Temperature

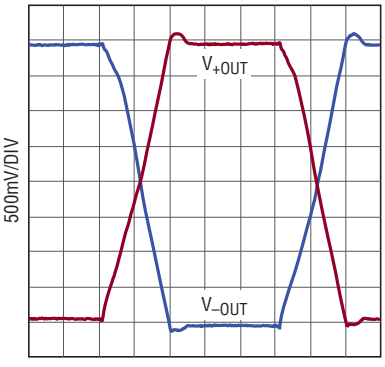


Small-Signal Step Response



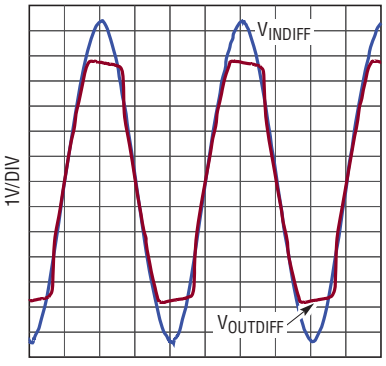
V_S = ±2.5V 100ns/DIV
V_{INDIFF} = 200mV_{P-P}
$R_I = R_F$ = 1k
R_{LOAD} = 1k

Large-Signal Step Response



V_S = ±2.5V 100ns/DIV
V_{INDIFF} = 8V_{P-P}
R_{LOAD} = 1k

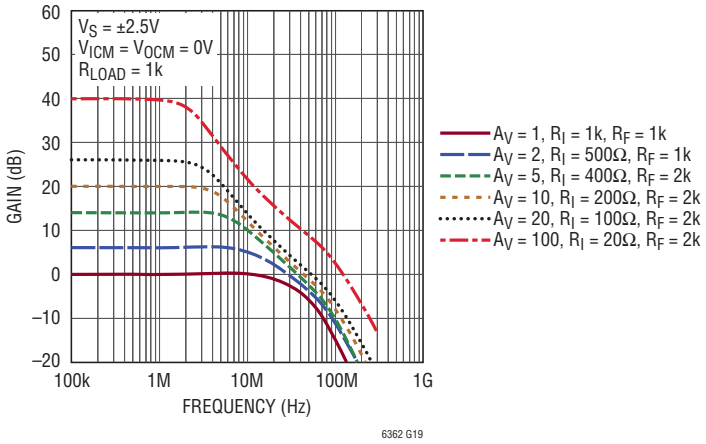
Overdriven Output Transient Response



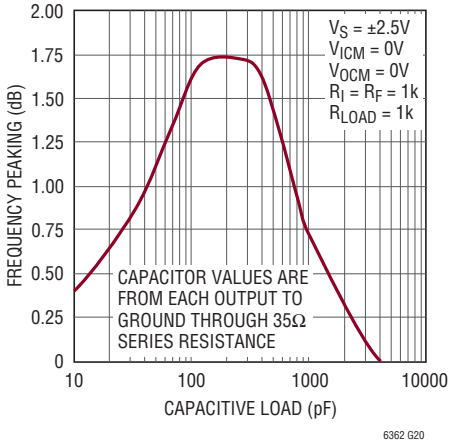
V_S = ±2.5V 1µs/DIV
V_{INDIFF} = 13V_{P-P}
R_{LOAD} = 1k

TYPICAL PERFORMANCE CHARACTERISTICS

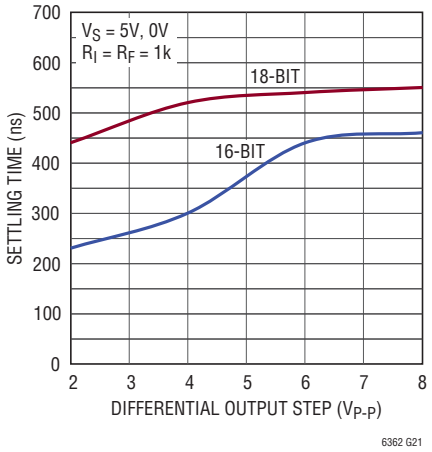
Frequency Response vs Closed-Loop Gain



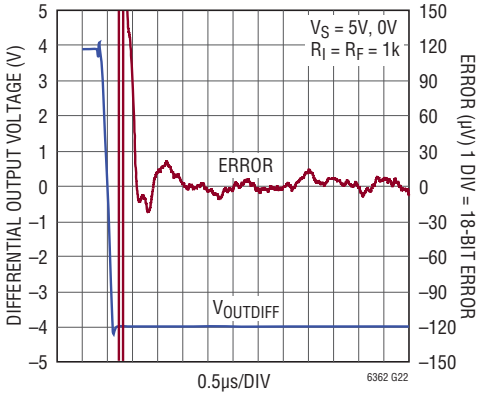
Frequency Peaking vs Load Capacitance



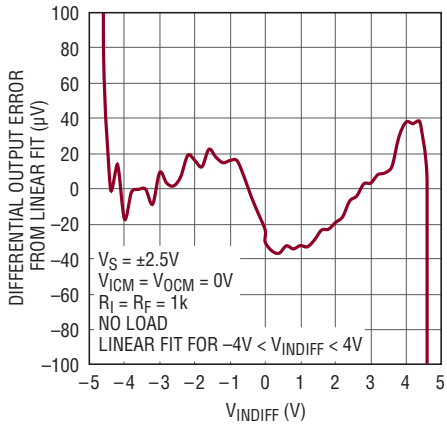
Settling Time vs Output Step



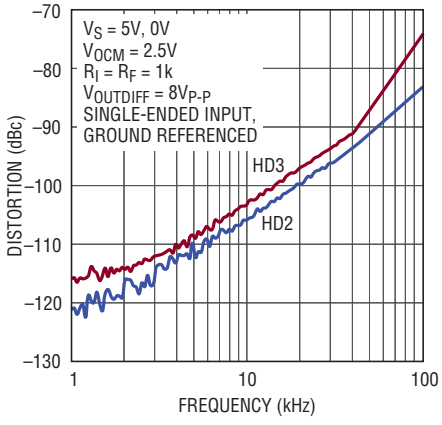
Settling Time to 8V_{P-P} Output Step



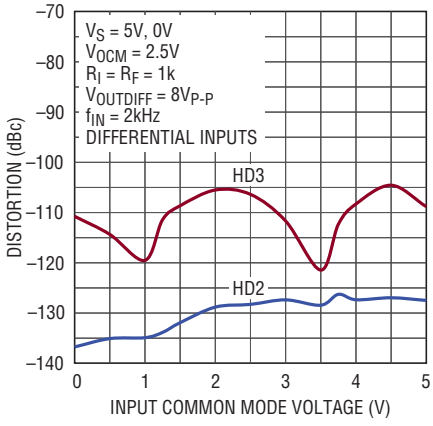
DC Linearity



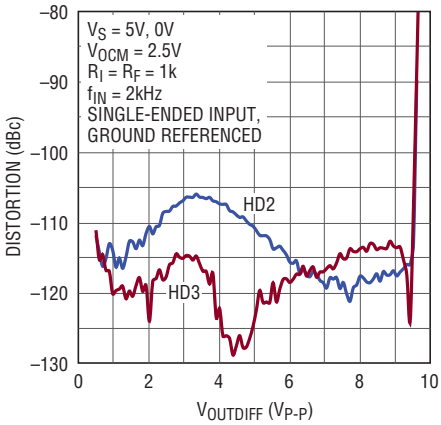
Harmonic Distortion vs Frequency



Harmonic Distortion vs Input Common Mode Voltage



Harmonic Distortion vs Output Amplitude



PIN FUNCTIONS

–IN (Pin 1): Inverting Input of Amplifier. Valid input range is from V^- to V^+.

V_{OCM} (Pin 2): Output Common Mode Reference Voltage. The voltage on this pin sets the output common mode voltage level. If left floating, an internal resistor divider develops a default voltage of 2.5V with a 5V supply.

V^+ (Pin 3): Positive Power Supply. Operational supply range is 2.8V to 5.25V when V^- = 0V.

+OUT (Pin 4): Positive Output Pin. Output capable of swinging rail-to-rail.

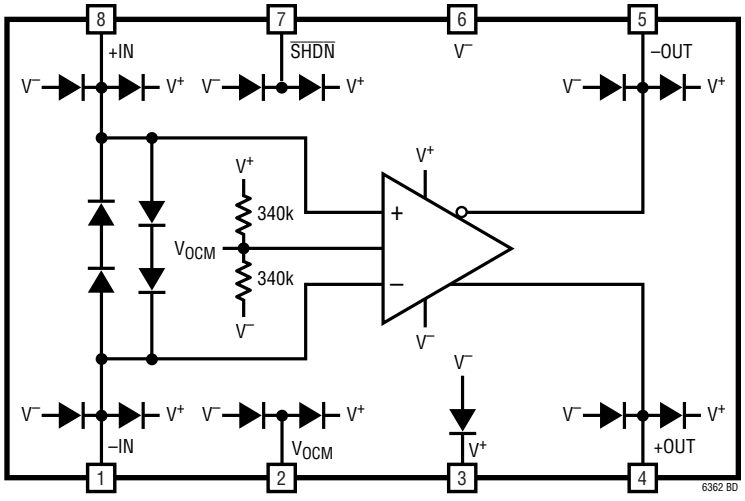
–OUT (Pin 5): Negative Output Pin. Output capable of swinging rail-to-rail.

V^- (Pin 6/Exposed Pad Pin 9): Negative Power Supply, Typically 0V. Negative supply can be negative as long as $2.8V \le (V^+ – V^-) \le 5.25V$ still holds.

$\overline{SHDN}$ (Pin 7): When $\overline{SHDN}$ is floating or directly tied to V^+ the LTC6362 is in the normal (active) operating mode. When the $\overline{SHDN}$ pin is connected to V^-, the part is disabled and draws approximately 70µA of supply current.

+IN (Pin 8): Noninverting Input of Amplifier. Valid input range is from V^- to V^+.

BLOCK DIAGRAM



APPLICATIONS INFORMATION

Functional Description

The LTC6362 is a low power, low noise, high DC accuracy fully differential operational amplifier/ADC driver. The amplifier is optimized to convert a fully differential or single-ended signal to a low impedance, balanced differential output suitable for driving high performance, low power differential successive approximation register (SAR) ADCs. The balanced differential nature of the amplifier also provides even-order harmonic distortion cancellation, and low susceptibility to common mode noise (like power supply noise).

The outputs of the LTC6362 are capable of swinging rail-to-rail and can source or sink up to 35mA of current. The LTC6362 is optimized for high bandwidth and low power applications. Load capacitances above 10pF to ground or 5pF differentially should be decoupled with 10Ω to 100Ω of series resistance from each output to prevent oscillation or ringing. Feedback should be taken directly from the amplifier output. Higher voltage gain configurations tend to have better capacitive drive capability than lower gain configurations due to lower closed-loop bandwidth.

Input Pin Protection

The LTC6362 input stage is protected against differential input voltages which exceed 1.4V by two pairs of series diodes connected back-to-back between +IN and –IN. Moreover, all pins have clamping diodes to both power supplies. If any pin is driven to voltages which exceed either supply, the current should be limited to under 10mA to prevent damage to the IC.

$\overline{SHDN}$ Pin

The LTC6362 has a $\overline{SHDN}$ pin which when driven to within 0.8V above the negative rail, will shut down amplifier operation such that only 70µA is drawn from the supplies. Pull-down circuitry should be capable of sinking at least 4µA to guarantee complete shutdown across all conditions. For normal operation, the $\overline{SHDN}$ pin should be left floating or tied to the positive rail.

General Amplifier Applications

In Figure 1, the gain to $V_{OUTDIFF}$ from V_{INP} and V_{INM} is given by:

$$V_{OUTDIFF} = V_{+OUT} - V_{-OUT} \approx \left(\frac{R_F}{R_I}\right) \bullet \left(V_{INP} - V_{INM}\right)$$

Note from the previous equation, the differential output voltage (V_{+OUT} – V_{-OUT}) is completely independent of input and output common mode voltages, or the voltage at the common mode pin. This makes the LTC6362 ideally suited for pre-amplification, level shifting and conversion of single-ended signals to differential output signals for driving differential input ADCs.

Output Common Mode and V_{OCM} Pin

The output common mode voltage is defined as the average of the two outputs:

$$V_{OUTCM} = V_{OCM} = \left(\frac{V_{+OUT} + V_{-OUT}}{2}\right)$$

As the equation shows, the output common mode voltage is independent of the input common mode voltage, and is instead determined by the voltage on the V_{OCM} pin, by means of an internal common mode feedback loop.

If the V_{OCM} pin is left open, an internal resistor divider develops a default voltage of 2.5V with a 5V supply. The V_{OCM} pin can be overdriven to another voltage if desired. For example, when driving an ADC, if the ADC makes a reference available for setting the common mode voltage, it can be directly tied to the V_{OCM} pin, as long as the ADC is capable of driving the 170k input resistance presented by the V_{OCM} pin. The Electrical Characteristics table specifies the valid range that can be applied to the V_{OCM} pin (V_{OUTCMR}).

APPLICATIONS INFORMATION

Input Common Mode Voltage Range

The LTC6362's input common mode voltage (V_{ICM}) is defined as the average of the two input pins, V_{+IN} and $V_{–IN}$. The inputs of the LTC6362 are capable of swinging rail-to-rail and as such the valid range that can be used for V_{ICM} is $V^–$ to V^+. However, due to external resistive divider action of the gain and feedback resistors, the effective range of signals that can be processed is even wider. The input common mode range at the op amp inputs depends on the circuit configuration (gain), V_{OCM} and V_{CM} (refer to Figure 1). For fully differential input applications, where $V_{INP} = –V_{INM}$, the common mode input is approximately:

$$V_{ICM} = \frac{V_{+IN} + V_{–IN}}{2} \approx V_{OCM} \bullet \frac{R_I}{R_I + R_F} + V_{CM} \bullet \frac{R_F}{R_I + R_F}$$

With single-ended inputs, there is an input signal component to the input common mode voltage. Applying only V_{INP} (setting V_{INM} to zero), the input common voltage is approximately:

$$V_{ICM} = \frac{V_{+IN} + V_{–IN}}{2}$$

$$\approx V_{OCM} \bullet \frac{R_I}{R_I + R_F} + V_{CM} \bullet \frac{R_F}{R_I + R_F} + \frac{V_{INP}}{2} \bullet \frac{R_F}{R_I + R_F}$$

This means that if, for example, the input signal (V_{INP}) is a sine, an attenuated version of that sine signal also appears at the op amp inputs.

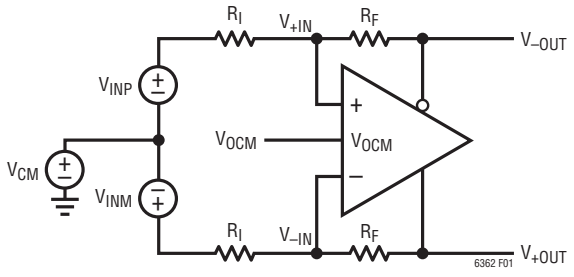


Figure 1. Definitions and Terminology

Input Bias Current

Input bias current varies according to V_{ICM}. For common mode voltages ranging from 0.2V above the negative supply to 1.1V below the positive supply, input bias current follows $\Delta I_B/\Delta V_{ICM} = 75nA/V$, with I_B at $V_{ICM} = 2.5V$ typically below 75nA on a 5V supply. For common mode voltages ranging from 1.1V below the positive supply to 0.2V below the positive supply, input bias current follows $\Delta I_B/\Delta V_{ICM} = 25nA/V$, with I_B at $V_{ICM} = 4.5V$ typically below 75nA on a 5V supply. Operating within these ranges allows the amplifier to be used in applications with high source resistances where errors due to voltage drops must be minimized. For applications where V_{ICM} is within 0.2V of either rail, input bias current may reach values over 1µA.

Input Impedance and Loading Effects

The low frequency input impedance looking into the V_{INP} or V_{INM} input of Figure 1 depends on how the inputs are driven. For fully differential input sources ($V_{INP} = –V_{INM}$), the input impedance seen at either input is simply:

$$R_{INP} = R_{INM} = R_I$$

For single-ended inputs, because of the signal imbalance at the input, the input impedance actually increases over the balanced differential case. The input impedance looking into either input is:

$$R_{INP} = R_{INM} = \frac{R_I}{1 – \left(\frac{1}{2}\right) \bullet \left(\frac{R_F}{R_I + R_F}\right)}$$

Input signal sources with non-zero output impedances can also cause feedback imbalance between the pair of feedback networks. For the best performance, it is recommended that the input source output impedance be compensated. If input impedance matching is required by the source, a termination resistor R1 should be chosen (see Figure 2) such that:

$$R1 = \frac{R_{INM} \bullet R_S}{R_{INM} – R_S}$$

According to Figure 2, the input impedance looking into the differential amp (R_{INM}) reflects the single-ended source case, given above. Also, R2 is chosen as:

$$R2 = R1 || R_S = \frac{R1 \bullet R_S}{R1 + R_S}$$

APPLICATIONS INFORMATION

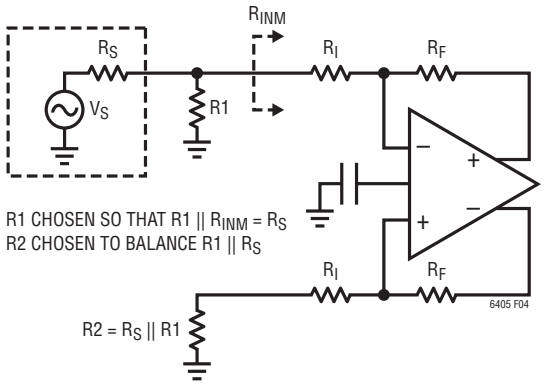


Figure 2. Optimal Compensation for Signal Source Impedance

Effects of Resistor Pair Mismatch

Figure 3 shows a circuit diagram which takes into consideration that real world resistors will not match perfectly. Assuming infinite open-loop gain, the differential output relationship is given by the equation:

$$V_{OUT(DIFF)} = V_{+OUT} - V_{-OUT}$$

$$\approx V_{INDIFF} \bullet \frac{R_F}{R_I} + V_{CM} \bullet \frac{\Delta\beta}{\beta_{AVG}} - V_{OCM} \bullet \frac{\Delta\beta}{\beta_{AVG}}$$

where R_F is the average of R_{F1} and R_{F2}, and R_I is the average of R_{I1} and R_{I2}.

β_{AVG} is defined as the average feedback factor from the outputs to their respective inputs:

$$\beta_{AVG} = \frac{1}{2} \bullet \left(\frac{R_{I1}}{R_{I1}+R_{F1}} + \frac{R_{I2}}{R_{I2}+R_{F2}} \right)$$

$\Delta\beta$ is defined as the difference in the feedback factors:

$$\Delta\beta = \frac{R_{I2}}{R_{I2}+R_{F2}} - \frac{R_{I1}}{R_{I1}+R_{F1}}$$

Here, V_{CM} and V_{INDIFF} are defined as the average and the difference of the two input voltages V_{INP} and V_{INM}, respectively:

$$V_{CM} = \frac{V_{INP} + V_{INM}}{2}$$

$$V_{INDIFF} = V_{INP} - V_{INM}$$

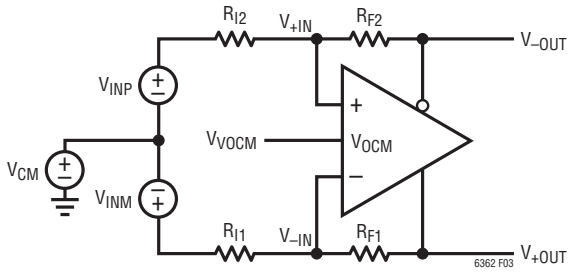


Figure 3. Real-World Application with Feedback Resistor Pair Mismatch

When the feedback ratios mismatch ($\Delta\beta$), common mode to differential conversion occurs. Setting the differential input to zero ($V_{INDIFF} = 0$), the degree of common mode to differential conversion is given by the equation:

$$V_{OUTDIFF} \approx (V_{CM} - V_{OCM}) \bullet \Delta\beta/\beta_{AVG}$$

In general, the degree of feedback pair mismatch is a source of common mode to differential conversion of both signals and noise. Using 0.1% resistors or better will mitigate most problems. A low impedance ground plane should be used as a reference for both the input signal source and the V_{OCM} pin.

Noise

The LTC6362's differential input referred voltage and current noise densities are 3.9nV/$\sqrt{Hz}$ and 0.8pA/$\sqrt{Hz}$, respectively. In addition to the noise generated by the amplifier, the surrounding feedback resistors also contribute noise. A simplified noise model is shown in Figure 4. The output noise generated by both the amplifier and the feedback components is given by the equation:

$$e_{no} = \sqrt{\left[e_{ni} \bullet \left(1 + \frac{R_F}{R_I} \right) \right]^2 + 2 \bullet \left(i_n \bullet R_F \right)^2 + 2 \bullet \left[e_{nRI} \bullet \frac{R_F}{R_I} \right]^2 + 2 \bullet e_{nRF}^{\,2}}$$

For example, if $R_F = R_I = 1k$, the output noise of the circuit e_{no} = 12nV/$\sqrt{Hz}$.

If the circuits surrounding the amplifier are well balanced, common mode noise (e_{nvocm}) does not appear in the differential output noise equation given above.

APPLICATIONS INFORMATION

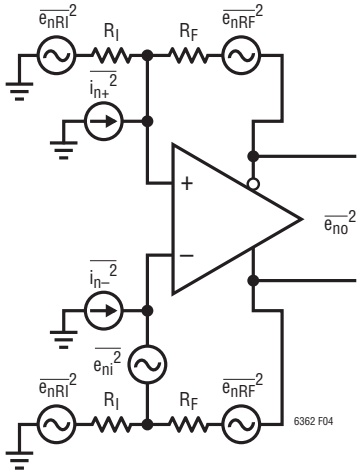


Figure 4. Simplified Noise Model

The LTC6362's input referred voltage noise contributes the equivalent noise of a 920Ω resistor. When the feedback network is comprised of resistors whose values are larger than this, the output noise is resistor noise and amplifier current noise dominant. For feedback networks consisting of resistors with values smaller than 920Ω, the output noise is voltage noise dominant.

Lower resistor values always result in lower noise at the penalty of increased distortion due to increased loading of the feedback network on the output. Higher resistor values will result in higher output noise, but typically improved distortion due to less loading on the output. For this reason, when LTC6362 is configured in a differential gain of 1, using feedback resistors of at least 1k is recommended.

GBW vs $f_{–3dB}$

Gain-bandwidth product (GBW) and –3dB frequency ($f_{–3dB}$) have been specified in the Electrical Characteristics table as two different metrics for the speed of the LTC6362. GBW is obtained by measuring the open-loop gain of the amplifier at a specific frequency (f_{TEST}), then calculating gain • f_{TEST}. GBW is a parameter that depends only on the internal design and compensation of the amplifier and is a suitable metric to specify the inherent speed capability of the amplifier.

$f_{–3dB}$, on the other hand, is a parameter of more practical interest in different applications and is by definition the frequency at which the closed-loop gain is 3dB lower than its low frequency value. The value of $f_{–3dB}$ depends on the speed of the amplifier as well as the feedback factor. Since the LTC6362 is designed to be stable in a differential signal gain of 1 (where $R_I = R_F$ or $\beta = 1/2$), the maximum $f_{–3dB}$ is obtained and measured in this gain setting, as reported in the Electrical Characteristics table.

In most amplifiers, the open-loop gain response exhibits a conventional single-pole roll-off for most of the frequencies before the unity-gain crossover frequency, and the GBW and unity-gain frequency are close to each other. However, the LTC6362 is intentionally compensated in such a way that its GBW is significantly larger than its $f_{–3dB}$. This means that at lower frequencies where the amplifier inputs generally operate, the amplifier's gain and thus the feedback loop gain is larger. This has the important advantage of further linearizing the amplifier and improving distortion at those frequencies.

Feedback Capacitors

In cases where the LTC6362 is connected such that the combination of parasitic capacitances (device + PCB) at the inverting input forms a pole whose frequency lies within the closed-loop bandwidth of the amplifier, a capacitor (C_F) can be added in parallel with the feedback resistor (R_F) to cancel the degradation on stability. C_F should be chosen such that it generates a zero at a frequency close to the frequency of the pole.

In general, a larger value for C_F reduces the peaking (overshoot) of the amplifier in both frequency and time domains, but also decreases the closed-loop bandwidth ($f_{–3dB}$).

Board Layout and Bypass Capacitors

For single supply applications, it is recommended that high quality 0.1µF ceramic bypass capacitors be placed directly between the V^+ and the $V^–$ pin with short connections. The $V^–$ pins (including the exposed pad in the DD8 package) should be tied directly to a low impedance ground plane with minimal routing. For dual (split) power supplies, it is recommended that additional high quality 0.1µF ceramic capacitors be used to bypass V^+ to ground and $V^–$ to ground, again with minimal routing. Small geometry (e.g., 0603) surface mount ceramic capacitors have a much higher self-resonant frequency than leaded capacitors, and perform best with LTC6362.

APPLICATIONS INFORMATION

To prevent degradation in stability response, it is highly recommended that any stray capacitance at the input pins, +IN and –IN, be kept to an absolute minimum by keeping printed circuit connections as short as possible.

At the output, always keep in mind the differential nature of the LTC6362, because it is critical that the load impedances seen by both outputs (stray or intended), be as balanced and symmetric as possible. This will help preserve the balanced operation of the LTC6362 that minimizes the generation of even-order harmonics and maximizes the rejection of common mode signals and noise.

The V_{OCM} pin should be bypassed to the ground plane with a high quality 0.1µF ceramic capacitor. This will prevent common mode signals and noise on this pin from being inadvertently converted to differential signals and noise by impedance mismatches both externally and internally to the IC.

Interfacing to ADCs

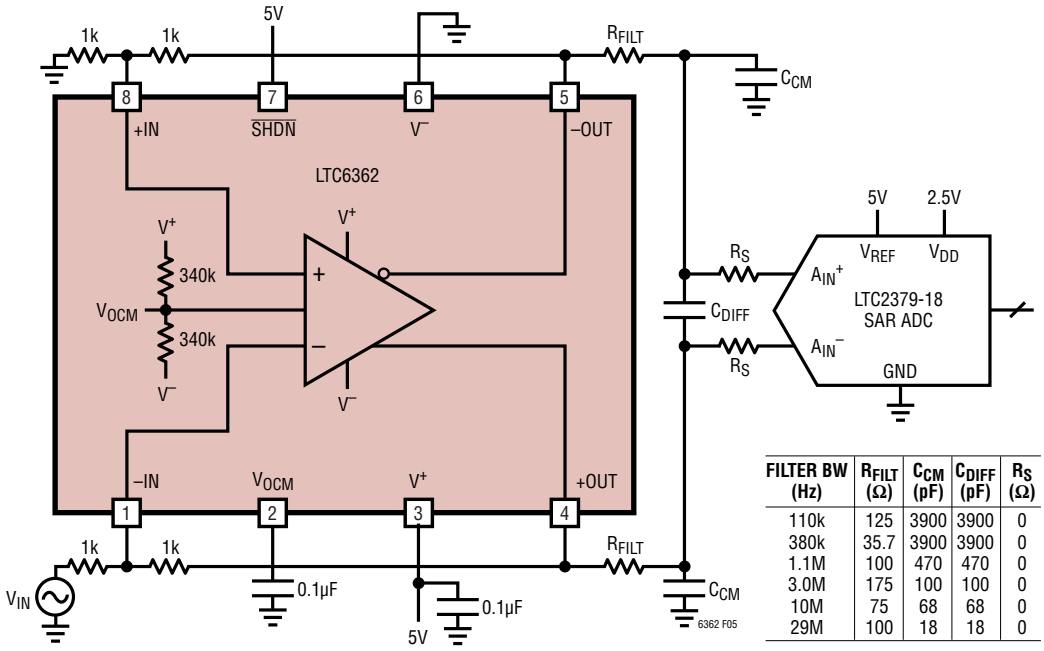
When driving an ADC, an additional passive filter should be used between the outputs of the LTC6362 and the inputs of the ADC. Depending on the application, a single-pole RC filter will often be sufficient. The sampling process of ADCs creates a charge transient that is caused by the switching in of the ADC sampling capacitor. This momentarily "shorts" the output of the amplifier as charge is transferred between amplifier and sampling capacitor. The amplifier must recover and settle from this load transient before the acquisition period has ended, for a valid representation of the input signal. The RC network between the outputs of the driver and the inputs of the ADC decouples the sampling transient of the ADC (see Figure 5). The capacitance serves to provide the bulk of the charge during the sampling process, while the two resistors at the outputs of the LTC6362 are used to dampen and attenuate any charge injected by the ADC. The RC filter gives the additional benefit of band limiting broadband output noise.

The selection of an appropriate filter depends on the specific ADC, however the following procedure is suggested for choosing filter component values. Begin by selecting an appropriate RC time constant for the input signal. Generally, longer time constants improve SNR at the expense of settling time. Output transient settling to 18-bit accuracy will typically require over twelve RC time constants. To select the resistor value, remember the resistors in the decoupling network should be at least 10Ω. Keep in mind that these resistors also serve to decouple the LTC6362 outputs from load capacitance. Too large of a resistor will leave insufficient settling time. Too small of a resistor will not properly dampen the load transient of the sampling process, prolonging the time required for settling. For lowest distortion, choose capacitors with low dielectric absorption (such as a C0G multilayer ceramic capacitor). In general, large capacitor values attenuate the fixed nonlinear charge kickback, however very large capacitor values will detrimentally load the driver at the desired input frequency and thus cause driver distortion. Smaller input swings will in general allow for larger filter capacitor values due to decreased loading demands on the driver. This property however may be limited by the particular input amplitude dependence of differential nonlinear charge kickback for the specific ADC used.

In some applications, placing series resistors at the inputs of the ADC may further improve distortion performance. These series resistors function with the ADC sampling capacitor to filter potential ground bounce or other high speed sampling disturbances. Additionally the resistors limit the rise time of residual filter glitches that manage to propagate to the driver outputs. Restricting possible glitch propagation rise time to within the small signal bandwidth of the driver enables less disturbed output settling.

For the specific application of LTC6362 driving the LTC2379-18 SAR ADC in a gain of $A_V = –1$ configuration, the recommended component values of the RC filter for varying filter bandwidths are provided in Figure 5. These component values are chosen for optimal distortion performance. Broadband output noise will vary with filter bandwidth.

APPLICATIONS INFORMATION

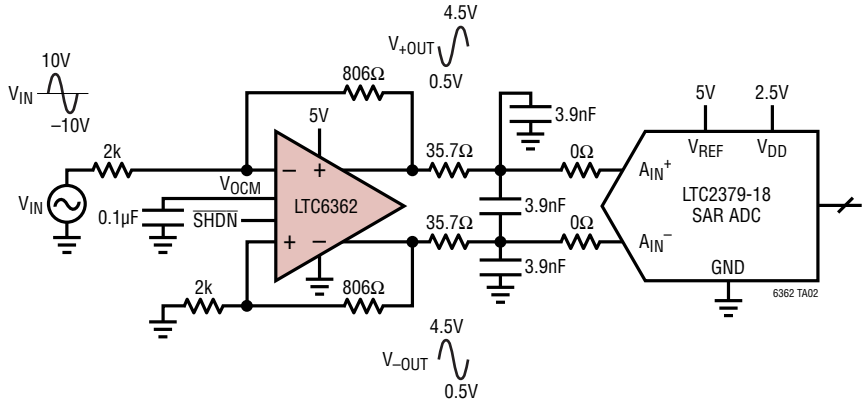


FILTER BW (Hz)	R_{FILT} (Ω)	C_{CM} (pF)	C_{DIFF} (pF)	R_S (Ω)
110k	125	3900	3900	0
380k	35.7	3900	3900	0
1.1M	100	470	470	0
3.0M	175	100	100	0
10M	75	68	68	0
29M	100	18	18	0

Figure 5. Recommended Interface Solutions for Driving the LTC2379-18 SAR ADC

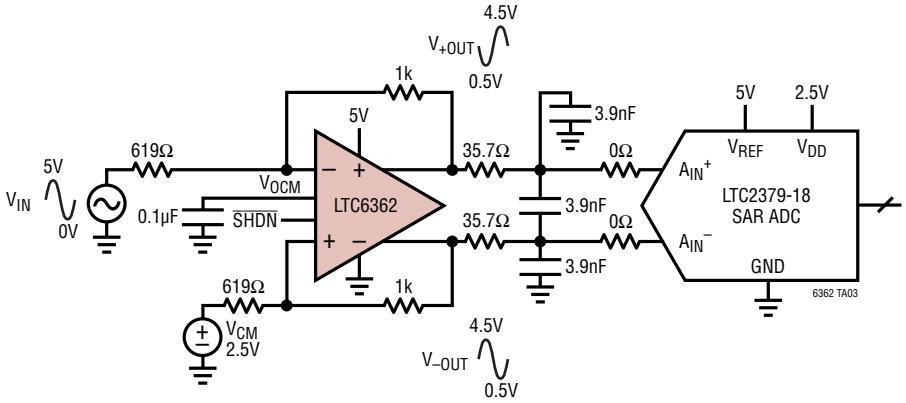
TYPICAL APPLICATIONS

Single-Ended-to-Differential Conversion of a 20V_{P-P} Ground-Referenced Input with Gain of A_V = –0.4 to Drive an ADC

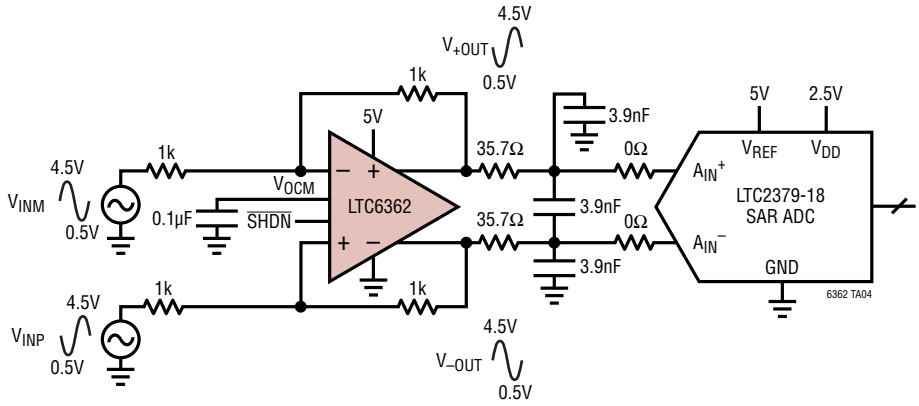


TYPICAL APPLICATIONS

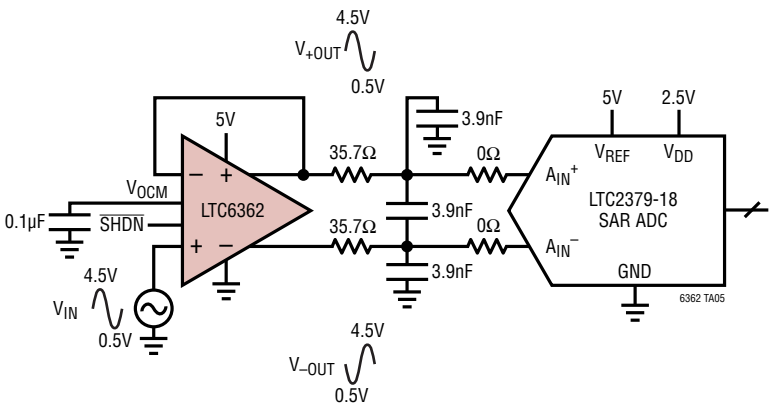
Single-Ended-to-Differential Conversion of a $5V_{P-P}$, 2.5V Referenced Input with Gain of $A_V = -1.6$ to Drive an ADC



Differentially Driving an ADC with $\Delta V_{IN} = 8V_{P-P}$ and Gain of $A_V = 1$

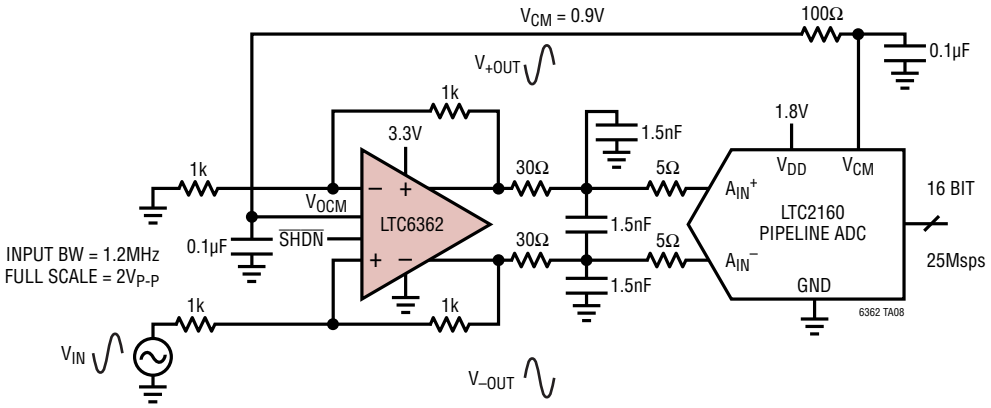


Single-Ended-to-Differential Conversion of a $4V_{P-P}$ Input with Gain of $A_V = 2$ to Drive an ADC for Applications Where the Importance of High Input Impedance Justifies Some Degradation in Distortion, Noise, and DC Accuracy. Input Is True High Impedance, However Common Mode Noise and Offset Are Present on the Output. Additionally, When the Input Signal Exceeds $2.8V_{P-P}$, a Step in Input Offset Will Occur That Will Degrade Distortion Performance



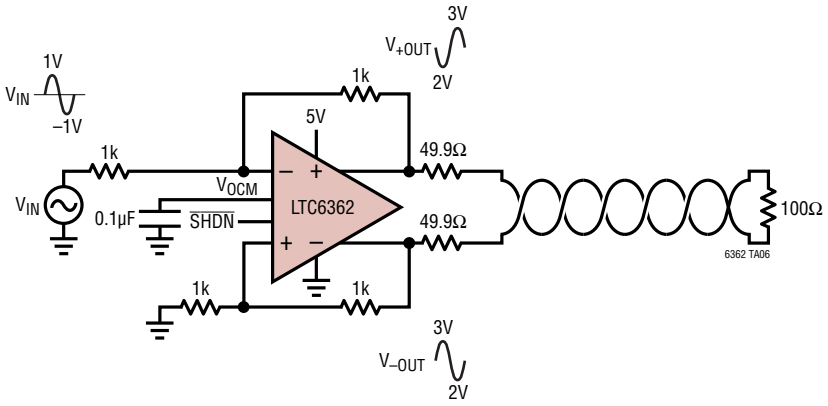
TYPICAL APPLICATIONS

Differentially Driving a Pipeline ADC with $A_V = 1$



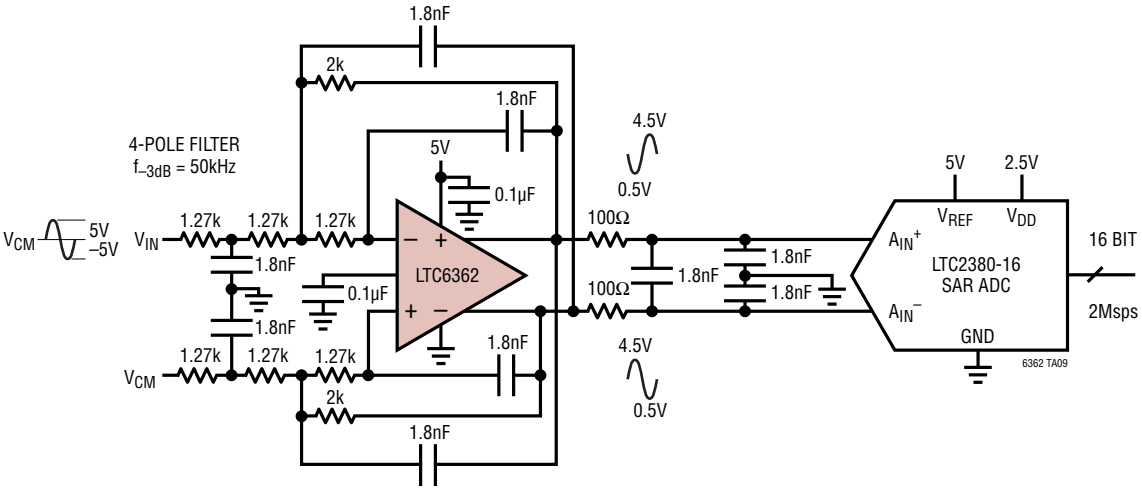
MEASURED PERFORMANCE FOR LTC6362 DRIVING LTC2160:
INPUT: f_{IN} = 2kHz, –1dBFS
SNR: 77.0dB
HD2: –98.9dBc
HD3: –102.3dBc
THD: –96.3dB

Differential Line Driver Connected in Gain of $A_V = -1$

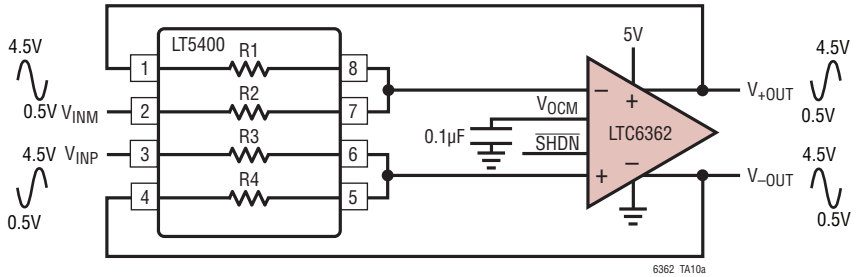


TYPICAL APPLICATIONS

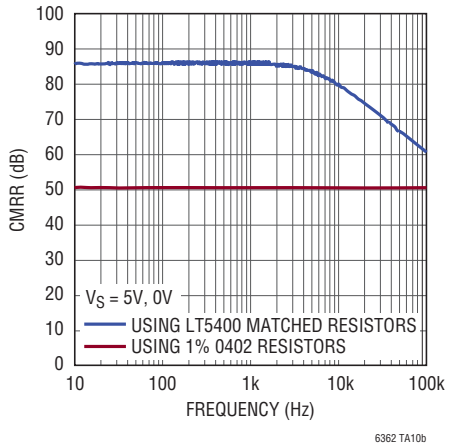
LTC6362 Used as Lowpass Filter/Driver with 10V_{P-P} Singled-Ended Input, Driving a SAR ADC



Differential A_V = 1 Configuration Using an LT®5400 Quad-Matched Resistor Network



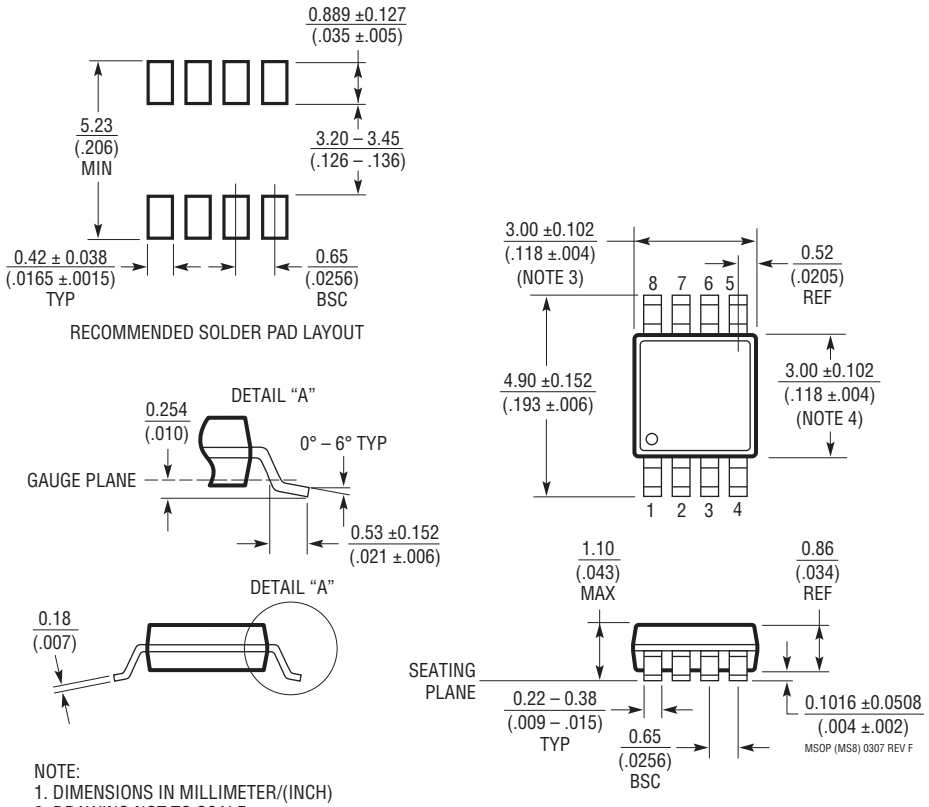
CMRR Comparison Using the LT5400 and 1% 0402 Resistors



PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

MS8 Package
8-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1660 Rev F)

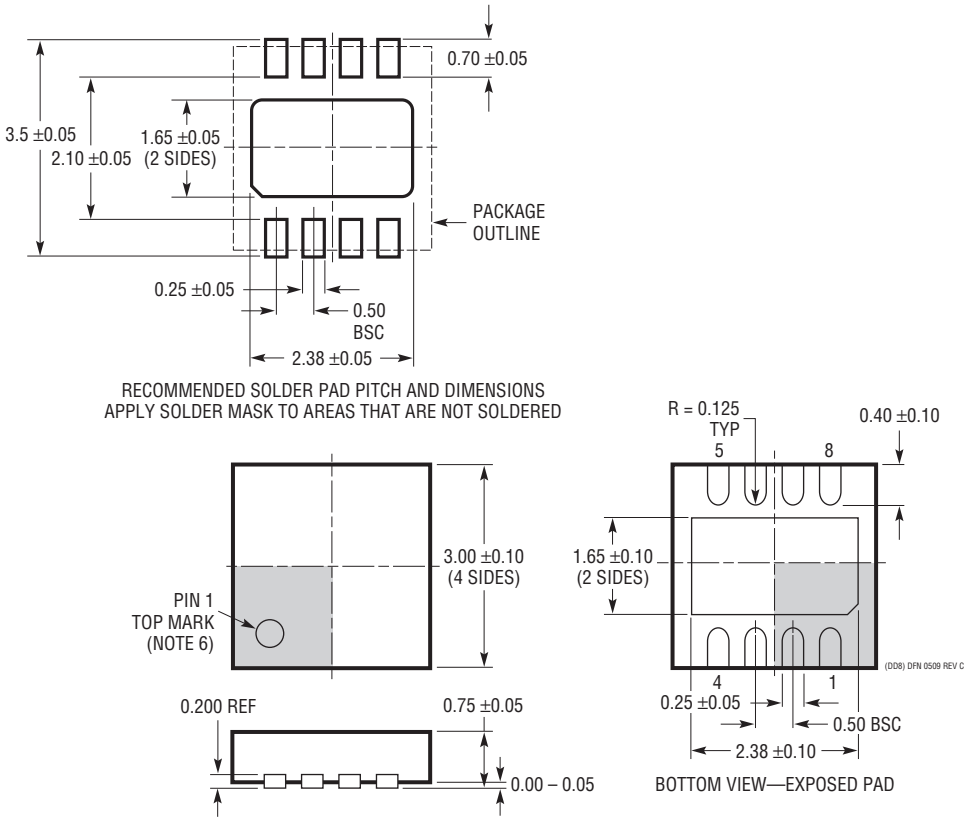


NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

DD Package
8-Lead Plastic DFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1698 Rev C)



NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-1)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON TOP AND BOTTOM OF PACKAGE

REVISION HISTORY

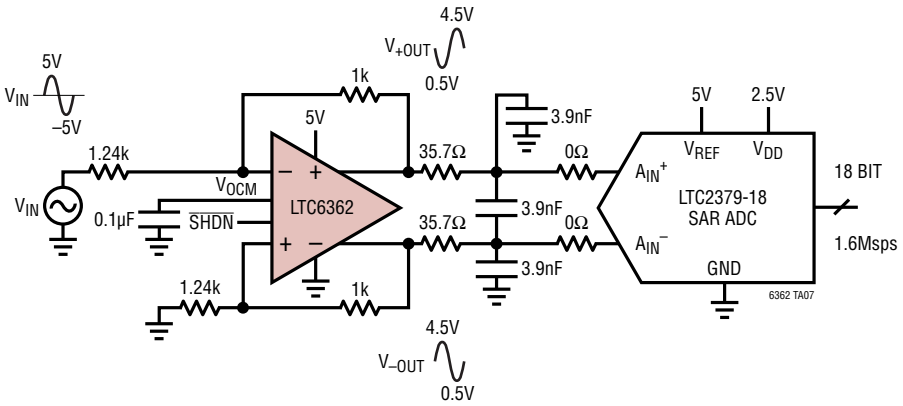
REV	DATE	DESCRIPTION	PAGE NUMBER
A	05/12	Added DFN package	1, 2, 9, 13, 20
		Added typical spec for $2V_{P-P}$ t_S	4

LINEAR TECHNOLOGY

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

TYPICAL APPLICATION

Single-Ended-to-Differential Conversion of a 10V_{P-P} Ground-Referenced Input with Gain of A_V = –0.8 to Drive a 5V Reference SAR ADC



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
Operational Amplifiers		
LT6350	Low Noise, Single-Ended to Differential Converter/ ADC Driver	4.8mA, –97dBc Distortion at 100kHz, 4V_{P-P} Output
LTC6246/LTC6247/ LTC6248	Single/Dual/Quad 180MHz Rail-to-Rail Low Power Op Amps	1mA/Amplifier, 4.2nV/$\sqrt{Hz}$
LTC6360	1GHz Very Low Noise Single-Ended SAR ADC Driver with True Zero Output	13.6mA, HD2/HD3 = –103dBc/–109dBc at 40kHz, 4V_{P-P} Output
LTC1992/LTC1992-X	3MHz to 4MHz Fully Differential Input/Output Amplifiers	Internal Feedback Resistors Available (G =1, 2, 5,10)
LT1994	70MHz Low Noise, Low Distortion Fully Differential Input/Output Amplifier/Driver	13mA, –94dBc Distortion at 1MHz, 2V_{P-P} Output
ADCs		
LTC2379-18/LTC2378-18 LTC2377-18/LTC2376-18	18-Bit, 1.6Msps/1Msps/500ksps/250ksps Serial, Low Power ADC	2.5V Supply, Differential Input, 101.2dB SNR, ±5V Input Range, DGC, Pin Compatible Family in MSOP-16 and 4mm × 3mm DFN-16 Packages
LTC2380-16/LTC2378-16 LTC2377-16/LTC2376-16	16-Bit, 2Msps/1Msps/500ksps/250ksps Serial, Low Power ADC	2.5V Supply, Differential Input, 96.2dB SNR, ±5V Input Range, DGC, Pin Compatible Family in MSOP-16 and 4mm × 3mm DFN-16 Packages
LTC2383-16/LTC2382-16/ LTC2381-16	16-Bit, 1Msps/500ksps/250ksps Serial, Low Power ADC	2.5V Supply, Differential Input, 92dB SNR, ±2.5V Input Range, Pin Compatible Family in MSOP-16 and 4mm × 3mm DFN-16 Packages
LTC2393-16/LTC2392-16/ LTC2391-16	16-Bit, 1Msps/500ksps/250ksps Parallel/Serial ADC	5V Supply, Differential Input, 94dB SNR, ±4.096V Input Range, Pin Compatible Family in 7mm × 7mm LQFP-48 and QFN-48 Packages
LTC2355-14/LTC2356-14	14-Bit, 3.5Msps Serial ADC	3.3V Supply, 1-Channel, Unipolar/Bipolar, 18mW, MSOP-10 Package
LTC2366	12-Bit, 3Msps Serial ADC	2.35V to 3.6V Supply 6- and 8-Lead TSOT-23 Packages
LTC2162/LTC2161/ LTC2160	16-Bit, 65/40/25Msps Low Power ADC	1.8V Supply, Differential Input, 77dB SNR, 2V_{P-P} Input Range, Pipeline Converter in 7mm × 7mm QFN-48 Package

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