Dual/Quad 18MHz, Low Noise, Rail-to-Rail, CMOS Op Amps

FEATURES

- **0.1Hz to 10Hz Noise: 550nV$_{P-P}$**
- **Input Bias Current: 1pA (Typ at 25°C)**
- **Low Offset Voltage: 125µV Max**
- Low Offset Drift: 2.5µV/°C Max
- Voltage Gain: 124dB Typ
- Gain Bandwidth Product: 18MHz
- Output Swings Rail-to-Rail
- Supply Operation:
  2.8V to 6V LTC6241/LTC6242
  2.8V to ±5.5V LTC6241HV/LTC6242HV
- Low Input Capacitance
- Dual LTC6241 in 8-Pin SO and Tiny DFN Packages
- Quad LTC6242 in 16-Pin SSOP and 5mm × 3mm DFN Packages

APPLICATIONS

- Photo Diode Amplifiers
- Charge Coupled Amplifiers
- Low Noise Signal Processing
- Active Filters
- Medical Instrumentation
- High Impedance Transducer Amplifier

DESCRIPTION

The LTC®6241/LTC6242 are dual and quad low noise, low offset, rail-to-rail output, unity gain stable CMOS op amps that feature 1pA of input bias current. The 0.1Hz to 10Hz noise of only 550nV$_{P-P}$, along with an offset of just 125µV make them uncommon among traditional CMOS op amps. Additionally, noise is guaranteed to be less than 10nV/$\sqrt{Hz}$ at 1kHz. An 18MHz gain bandwidth, and 10V/µs slew rate, along with the wide supply range and low input capacitance, make them perfect for use as fast signal processing amplifiers.

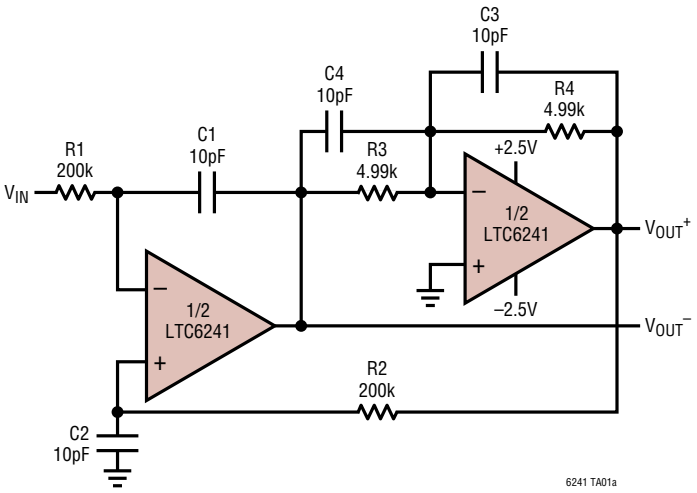
These op amps have an output stage that swings within 30mV of either supply rail to maximize the signal dynamic range in low supply applications. The input common mode range extends to the negative supply. They are fully specified on 3V and 5V, and an HV version guarantees operation on supplies up to ±5.5V.

The LTC6241 is available in the 8-pin SO, and for compact designs it is packaged in the tiny dual fine pitch leadless (DFN) package. The LTC6242 is available in the 16-Pin SSOP as well as the 5mm × 3mm DFN package.

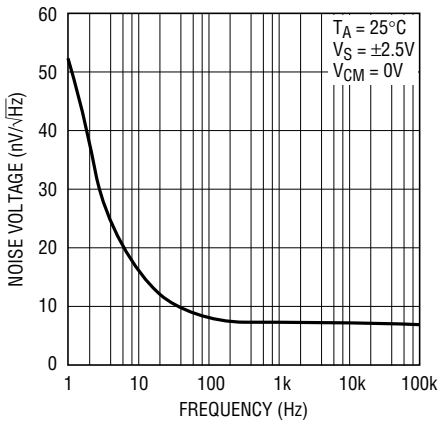
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TYPICAL APPLICATION

Low Noise Single-Ended Input to Differential Output Amplifier



Noise Voltage vs Frequency



ABSOLUTE MAXIMUM RATINGS

(Note 1)

Total Supply Voltage (V^+ to V^-)
- LTC6241/LTC6242 ..... 7V
- LTC6241HV/LTC6242HV 12V

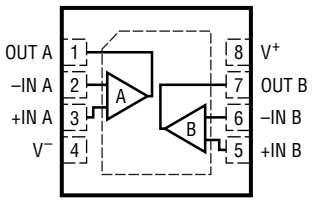
Input Voltage..... (V^+ + 0.3V) to (V^- – 0.3V)
Input Current..... ±10mA
Output Short Circuit Duration (Note 2) ..... Indefinite
Operating Temperature Range (Note 3) ... –40°C to 85°C
Specified Temperature Range (Note 4) .... –40°C to 85°C
Junction Temperature ..... 150°C
- DHC, DD Package ..... 125°C

Storage Temperature Range.....–65°C to 150°C
- DHC, DD Package .....–65°C to 125°C

Lead Temperature (Soldering, 10 sec) ..... 300°C

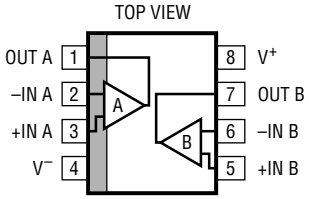
PACKAGE/ORDER INFORMATION

TOP VIEW



DD PACKAGE
8-LEAD (3mm × 3mm) PLASTIC DFN
T_{JMAX} = 125°C, θ_{JA} = 43°C/W
UNDERSIDE METAL CONNECTED TO V^-
(PCB CONNECTION OPTIONAL)

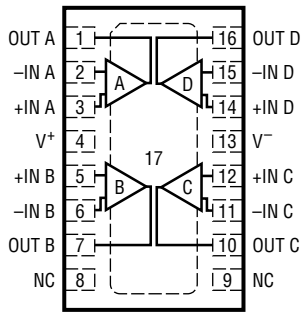
TOP VIEW



S8 PACKAGE
8-LEAD PLASTIC SO
T_{JMAX} = 150°C, θ_{JA} = 190°C/W

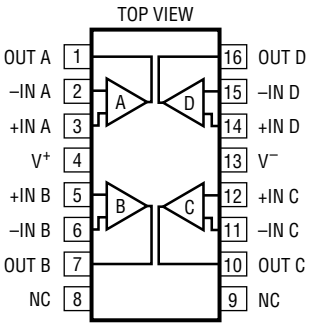
ORDER PART NUMBER	DD PART MARKING*
LTC6241CDD LTC6241HVCDD LTC6241IDD LTC6241HVIDD	LBPD LBRR LBPD LBRR
ORDER PART NUMBER	**S8 PART MARKING**
LTC6241CS8 LTC6241HVCS8 LTC6241IS8 LTC6241HVIS8	6241 6241HV 6241I 241HVI

TOP VIEW



DHC16 PACKAGE
16-LEAD (5mm × 3mm) PLASTIC DFN
T_{JMAX} = 125°C, θ_{JA} = 43°C/W
UNDERSIDE METAL CONNECTED TO V^-

TOP VIEW



GN PACKAGE
16-LEAD PLASTIC SSOP
T_{JMAX} = 150°C, θ_{JA} = 135°C/W

ORDER PART NUMBER	DHC PART MARKING*
LTC6242CDHC LTC6242HVCDHC LTC6242IDHC LTC6242HVIDHC	6242 6242HV 6242 6242HV
ORDER PART NUMBER	**GN PART MARKING**
LTC6242CGN LTC6242HVCGN LTC6242IGN LTC6242HVIGN	6242 6242HV 6242I 242HVI

Order Options Tape and Reel: Add #TR
Lead Free: Add #PBF Lead Free Tape and Reel: Add #TRPBF
Lead Free Part Marking: http://www.linear.com/leadfree/

*The temperature grade is identified by a label on the shipping container. Consult LTC Marketing for parts specified with wider operating temperature ranges.

AVAILABLE OPTIONS

PART NUMBER	AMPS/PACKAGE	SPECIFIED TEMP RANGE	SPECIFIED SUPPLY VOLTAGE	PACKAGE	PART MARKING
LTC6241CS8	2	0°C to 70°C	3V, 5V	SO-8	6241
LTC6241CDD	2	0°C to 70°C	3V, 5V	DD	LBPD
LTC6241HVCS8	2	0°C to 70°C	3V, 5V, ±5V	SO-8	6241HV
LTC6241HVCDD	2	0°C to 70°C	3V, 5V, ±5V	DD	LBRR
LTC6241IS8	2	–40°C to 85°C	3V, 5V	SO-8	6241I
LTC6241IDD	2	–40°C to 85°C	3V, 5V	DD	LBPD
LTC6241HVIS8	2	–40°C to 85°C	3V, 5V, ±5V	SO-8	241HVI
LTC6241HVIDD	2	–40°C to 85°C	3V, 5V, ±5V	DD	LBRR
LTC6242CGN	4	0°C to 70°C	3V, 5V	GN	6242
LTC6242CDHC	4	0°C to 70°C	3V, 5V	DHC	6242
LTC6242HVCGN	4	0°C to 70°C	3V, 5V, ±5V	GN	6242HV
LTC6242HVCDHC	4	0°C to 70°C	3V, 5V, ±5V	DHC	6242HV
LTC6242IGN	4	–40°C to 85°C	3V, 5V	GN	6242I
LTC6242IDHC	4	–40°C to 85°C	3V, 5V	DHC	6242
LTC6242HVIGN	4	–40°C to 85°C	3V, 5V, ±5V	GN	242HVI
LTC6242HVIDHC	4	–40°C to 85°C	3V, 5V, ±5V	DHC	6242HV

ELECTRICAL CHARACTERISTICS

(LTC6241/LTC6241HV, LTC6242/LTC6242HV) The ● denotes the specifications which apply over the specified temperature range, otherwise specifications are at T_A = 25°C. V_S = 5V, 0V, V_{CM} = 2.5V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage (Note 5)	SO-Package			40	125	µV
		0°C to 70°C	●			250	µV
		–40°C to 85°C	●			300	µV
		GN Package			50	150	µV
		0°C to 70°C	●			275	µV
		–40°C to 85°C	●			300	µV
		DD, DHC Packages			100	550	µV
		0°C to 70°C	●			650	µV
		–40°C to 85°C	●			725	µV
	V_{OS} Match Channel-to-Channel (Note 6)	SO-8 Package			40	160	µV
		0°C to 70°C	●			300	µV
		–40°C to 85°C	●			375	µV
		GN Package			50	185	µV
		0°C to 70°C	●			325	µV
		–40°C to 85°C	●			400	µV
		DD, DHC Packages			150	650	µV
		0°C to 70°C	●			700	µV
		–40°C to 85°C	●			750	µV
TC V_{OS}	Input Offset Voltage Drift (Note 7)		●		0.7	2.5	µV/°C
I_B	Input Bias Current (Notes 5, 8)				1		pA
			●			75	pA

ELECTRICAL CHARACTERISTICS

(LTC6241/LTC6241HV, LTC6242/LTC6242HV) The ● denotes the specifications which apply over the specified temperature range, otherwise specifications are at T_A = 25°C. V_S = 5V, 0V, V_{CM} = 2.5V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_{OS}	Input Offset Current (Notes 5, 8)				0.5		pA
			●			75	pA
	Input Noise Voltage	0.1Hz to 10Hz			550		nV_{P-P}
e_n	Input Noise Voltage Density	f = 1kHz			7	10	$nV/\sqrt{Hz}$
i_n	Input Noise Current Density (Note 9)				0.56		$fA/\sqrt{Hz}$
R_{IN}	Input Resistance	Common Mode			10^{12}		Ω
C_{IN}	Input Capacitance	f = 100kHz (See Typical Characteristic Curves)					
	Differential Mode				0.5		pF
	Common Mode				3		pF
V_{CM}	Input Voltage Range	Guaranteed by CMRR	●	0		3.5	V
CMRR	Common Mode Rejection	0V ≤ V_{CM} ≤ 3.5V	●	80	105		dB
	CMRR Match Channel-to-Channel (Note 6)		●	76	95		dB
A_{VOL}	Large Signal Voltage Gain	V_O = 1V to 4V, R_L = 10k to V_S/2		425	1600		V/mV
		0°C to 70°C	●	300			V/mV
		–40°C to 85°C	●	200			V/mV
		V_O = 1.5V to 3.5V, R_L = 1k to V_S/2		90	215		V/mV
		0°C to 70°C	●	60			V/mV
		–40°C to 85°C	●	50			V/mV
V_{OL}	Output Voltage Swing Low (Note 10)	No Load	●		7	30	mV
		I_{SINK} = 1mA	●		40	75	mV
		I_{SINK} = 5mA	●		190	325	mV
V_{OH}	Output Voltage Swing High (Note 10)	No Load	●		11	30	mV
		I_{SOURCE} = 1mA	●		45	75	mV
		I_{SOURCE} = 5mA	●		190	325	mV
PSRR	Power Supply Rejection	V_S = 2.8V to 6V, V_{CM} = 0.2V	●	80	104		dB
	PSRR Match Channel-to-Channel (Note 6)		●	74	100		dB
	Minimum Supply Voltage (Note 11)		●	2.8			V
I_{SC}	Short-Circuit Current		●	15	30		mA
I_S	Supply Current per Amplifier				1.8	2.2	mA
		0°C to 70°C	●			2.3	mA
		–40°C to 85°C	●			2.4	mA
GBW	Gain Bandwidth Product	Frequency = 20kHz, R_L = 1kΩ	●	13	18		MHz
SR	Slew Rate (Note 12)	A_V = –2, R_L = 1kΩ	●	5	10		V/µs
FPBW	Full Power Bandwidth (Note 13)	V_{OUT} = $3V_{P-P}$, R_L = 1kΩ	●	0.53	1.06		MHz
t_s	Settling Time	V_{STEP} = 2V, A_V = –1, R_L = 1kΩ, 0.1%			1100		ns

ELECTRICAL CHARACTERISTICS

(LTC6241/LTC6241HV, LTC6242/LTC6242HV) The ● denotes the specifications which apply over the specified temperature range, otherwise specifications are at T_A = 25°C. V_S = 3V, 0V, V_{CM} = 1.5V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage (Note 5)	SO-8 Package			40	175	µV
		0°C to 70°C	●			275	µV
		–40°C to 85°C	●			325	µV
		GN Package			60	200	µV
		0°C to 70°C	●			275	µV
		–40°C to 85°C	●			325	µV
		DD, DHC Packages			100	550	µV
		0°C to 70°C	●			650	µV
		–40°C to 85°C	●			725	µV
	V_{OS} Match Channel-to-Channel (Note 6)	SO-8 Package			40	200	µV
		0°C to 70°C	●			325	µV
		–40°C to 85°C	●			400	µV
		GN Package			60	225	µV
		0°C to 70°C	●			325	µV
		–40°C to 85°C	●			400	µV
		DD, DHC Packages			150	650	µV
		0°C to 70°C	●			700	µV
		–40°C to 85°C	●			750	µV
I_B	Input Bias Current (Notes 5, 8)				1		pA
			●			75	pA
I_{OS}	Input Offset Current (Notes 5, 8)				0.5		pA
			●			75	pA
V_{CM}	Input Voltage Range	Guaranteed by CMRR	●	0		1.5	V
CMRR	Common Mode Rejection	0V ≤ V_{CM} ≤ 1.5V	●	78	100		dB
	CMRR Match Channel-to-Channel (Note 6)		●	76	95		dB
A_{VOL}	Large Signal Voltage Gain	V_O = 1V to 2V					
		R_L = 10k to V_S/2		140	600		V/mV
		0°C to 70°C	●	100			V/mV
		–40°C to 85°C	●	75			V/mV
V_{OL}	Output Voltage Swing Low (Note 10)	No Load	●		3	30	mV
		I_{SINK} = 1mA	●		65	110	mV
V_{OH}	Output Voltage Swing High (Note 10)	No Load	●		4	30	mV
		I_{SOURCE} = 1mA	●		70	120	mV
PSRR	Power Supply Rejection	V_S = 2.8V to 6V, V_{CM} = 0.2V	●	80	104		dB
	PSRR Match Channel-to-Channel (Note 6)		●	74	100		dB
	Minimum Supply Voltage (Note 11)		●	2.8			V
I_{SC}	Short-Circuit Current		●	3	6		mA
I_S	Supply Current per Amplifier				1.4	1.7	mA
		0°C to 70°C	●			1.8	mA
		–40°C to 85°C	●			1.9	mA
GBW	Gain Bandwidth Product	Frequency = 20kHz, R_L = 1kΩ	●	12	17		MHz

ELECTRICAL CHARACTERISTICS

(LTC6241HV/LTC6242HV) The ● denotes the specifications which apply over the specified temperature range, otherwise specifications are at T_A = 25°C. V_S = ±5V, 0V, V_{CM} = 0V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage (Note 5)	SO-8 Package			50	175	µV
		0°C to 70°C	●			275	µV
		–40°C to 85°C	●			325	µV
		GN Package			60	200	µV
		0°C to 70°C	●			275	µV
		–40°C to 85°C	●			325	µV
		DD, DHC Packages			100	550	µV
		0°C to 70°C	●			650	µV
		–40°C to 85°C	●			725	µV
	V_{OS} Match Channel-to-Channel (Note 6)	SO-8 Package			50	200	µV
		0°C to 70°C	●			325	µV
		–40°C to 85°C	●			400	µV
		GN Package			60	225	µV
		0°C to 70°C	●			325	µV
		–40°C to 85°C	●			400	µV
		DD, DHC Packages			150	650	µV
		0°C to 70°C	●			700	µV
		–40°C to 85°C	●			750	µV
TC V_{OS}	Input Offset Voltage Drift (Note 7)		●		0.7	2.5	µV/°C
I_B	Input Bias Current (Notes 5, 8)				1		pA
			●			75	pA
I_{OS}	Input Offset Current (Notes 5, 8)				0.5		pA
			●			75	pA
	Input Noise Voltage	0.1Hz to 10Hz			550		nV_{P-P}
e_n	Input Noise Voltage Density	f = 1kHz			7	10	$nV/\sqrt{Hz}$
i_n	Input Noise Current Density (Note 9)				0.56		$fA/\sqrt{Hz}$
R_{IN}	Input Resistance	Common Mode			10^{12}		Ω
C_{IN}	Input Capacitance	f = 100kHz (See Typical Characteristic Curves)					
	Differential Mode				0.5		pF
	Common Mode				3		pF
V_{CM}	Input Voltage Range	Guaranteed by CMRR	●	–5		3.5	V
CMRR	Common Mode Rejection	$-5V \le V_{CM} \le 3.5V$	●	83	105		dB
	CMRR Match Channel-to-Channel (Note 6)		●	76	95		dB
A_{VOL}	Large Signal Voltage Gain	V_O = –3.5V to 3.5V					
		R_L = 10k		775	2700		V/mV
		0°C to 70°C	●	600			V/mV
		–40°C to 85°C	●	500			V/mV
		R_L = 1k		150	360		V/mV
		0°C to 70°C	●	90			V/mV
		–40°C to 85°C	●	75			V/mV
V_{OL}	Output Voltage Swing Low (Note 10)	No Load	●		15	30	mV
		I_{SINK} = 1mA	●		45	75	mV
		I_{SINK} = 10mA	●		360	550	mV
V_{OH}	Output Voltage Swing High (Note 10)	No Load	●		15	30	mV
		I_{SOURCE} = 1mA	●		45	75	mV
		I_{SOURCE} = 10mA	●		360	550	mV

ELECTRICAL CHARACTERISTICS

(LTC6241HV/LTC6242HV) The ● denotes the specifications which apply over the specified temperature range, otherwise specifications are at T_A = 25°C. V_S = ±5V, 0V, V_{CM} = 0V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
PSRR	Power Supply Rejection	V_S = 2.8V to 11V, V_{CM} = 0.2V	●	85	110		dB
	PSRR Match Channel-to-Channel (Note 6)		●	82	106		dB
	Minimum Supply Voltage (Note 11)		●	2.8			V
I_{SC}	Short-Circuit Current		●	15	35		mA
I_S	Supply Current per Amplifier	 0°C to 70°C –40°C to 85°C	 ● ●		2.5	3.2 3.3 3.7	mA mA mA
GBW	Gain Bandwidth Product	Frequency = 20kHz, R_L = 1kΩ	●	13	18		MHz
SR	Slew Rate (Note 12)	A_V = –2, R_L = 1kΩ	●	5.5	10		V/µs
FPBW	Full Power Bandwidth (Note 13)	V_{OUT} = $3V_{P-P}$, R_L = 1kΩ	●	0.58	1.06		MHz
t_s	Settling Time	V_{STEP} = 2V, A_V = –1, R_L = 1kΩ, 0.1%			900		ns

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: A heat sink may be required to keep the junction temperature below the absolute maximum rating when the output is shorted indefinitely.

Note 3: All versions of the LTC6241/LTC6242 are guaranteed functional over the temperature range of –40°C and 85°C.

Note 4: The LTC6241C/LTC6241HVC, LTC6242C/LTC6242HVC are guaranteed to meet specified performance from 0°C to 70°C. They are designed, characterized and expected to meet specified performance from –40°C to 85°C, but are not tested or QA sampled at these temperatures. The LTC6241I/LTC6241HVI, LTC6242I/LTC6242HVI are guaranteed to meet specified performance from –40°C to 85°C.

Note 5: ESD (Electrostatic Discharge) sensitive device. ESD protection devices are used extensively internal to the LTC6241/LTC6242; however, high electrostatic discharge can damage or degrade the device. Use proper ESD handling precautions.

Note 6: Matching parameters are the difference between the two amplifiers A and D and between B and C of the LTC6242; between the two amplifiers of the LTC6241. CMRR and PSRR match are defined as follows: CMRR and PSRR are measured in µV/V on the matched amplifiers. The difference is calculated between the matching sides in µV/V. The result is converted to dB.

Note 7: This parameter is not 100% tested.

Note 8: This specification is limited by high speed automated test capability. See Typical Characteristics curves for actual typical performance.

Note 9: Current noise is calculated from the formula: $i_n = (2qI_B)^{1/2}$ where $q = 1.6 \times 10^{-19}$ coulomb. The noise of source resistors up to 50GΩ dominates the contribution of current noise. See also Typical Characteristics curve Noise Current vs Frequency.

Note 10: Output voltage swings are measured between the output and power supply rails.

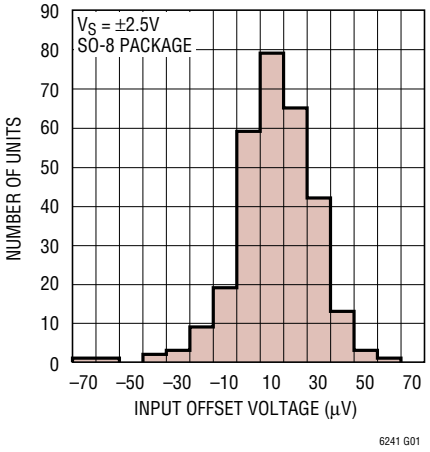
Note 11: Minimum supply voltage is guaranteed by the power supply rejection ratio test.

Note 12: Slew rate is measured in a gain of –2 with R_F = 1k and R_G = 500Ω. On the LTC6241/LTC6242, V_{IN} is ±1V and V_{OUT} slew rate is measured between –1V and +1V. On the LTC6241HV/LTC6242HV, V_{IN} is ±2V and V_{OUT} slew rate is measured between –2V and +2V.

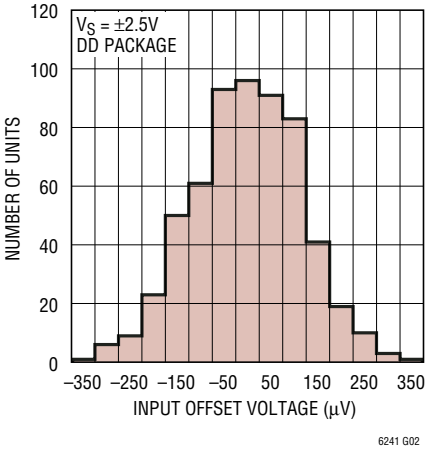
Note 13: Full-power bandwidth is calculated from the slew rate: $FPBW = SR/2\pi V_P$.

TYPICAL PERFORMANCE CHARACTERISTICS

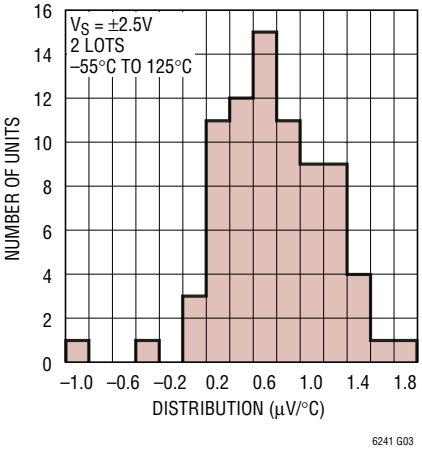
V_{OS} Distribution



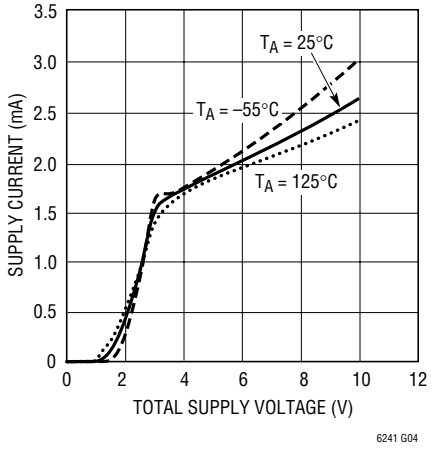
V_{OS} Distribution



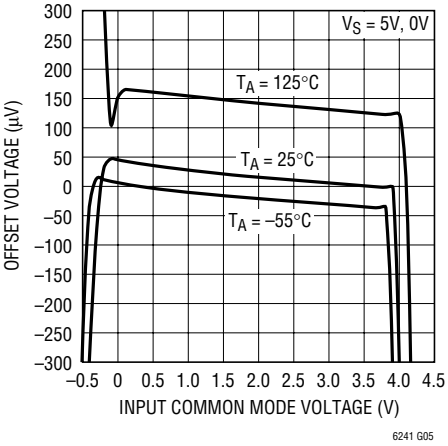
V_{OS} Temperature Coefficient Distribution



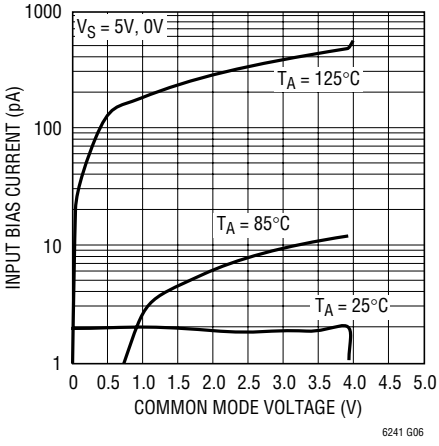
Supply Current vs Supply Voltage



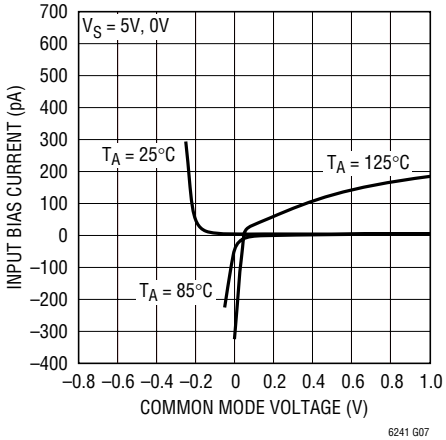
Offset Voltage vs Input Common Mode Voltage



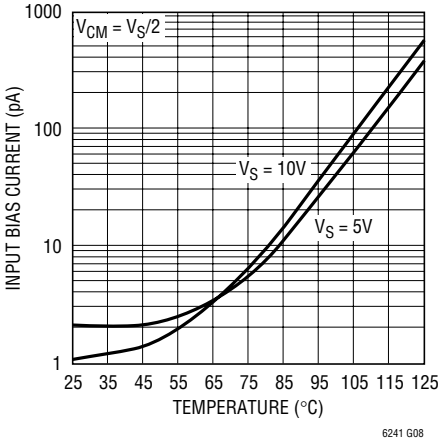
Input Bias Current vs Common Mode Voltage



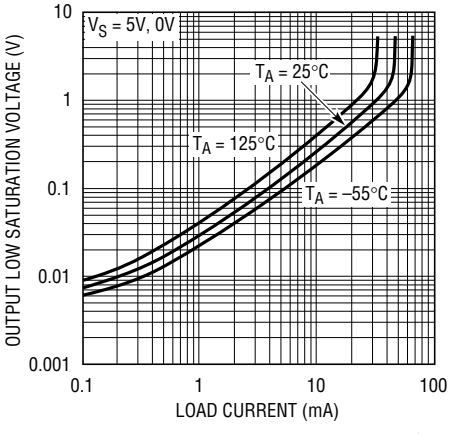
Input Bias Current vs Common Mode Voltage



Input Bias Current vs Temperature

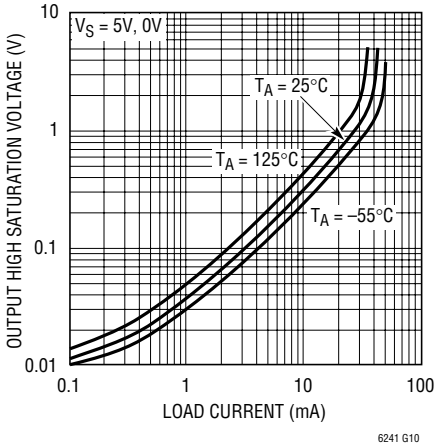


Output Saturation Voltage vs Load Current (Output Low)

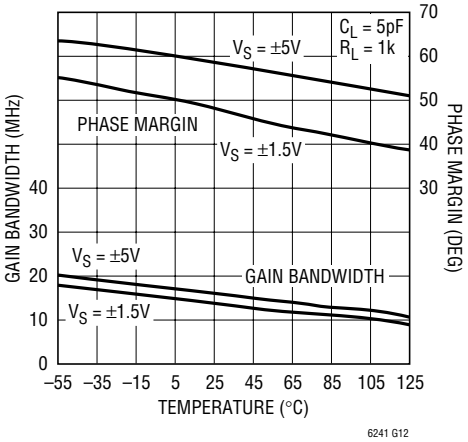


TYPICAL PERFORMANCE CHARACTERISTICS

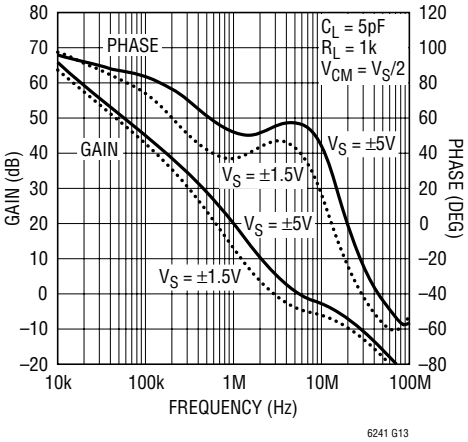
Output Saturation Voltage vs Load Current (Output High)



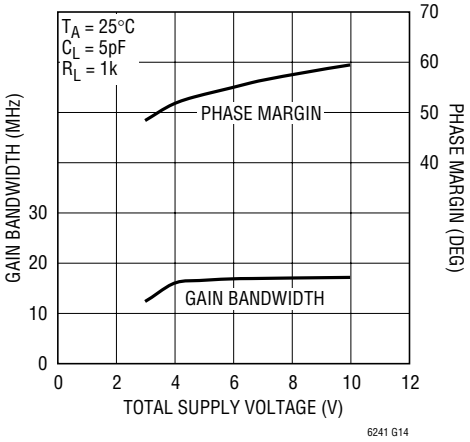
Gain Bandwidth and Phase Margin vs Temperature



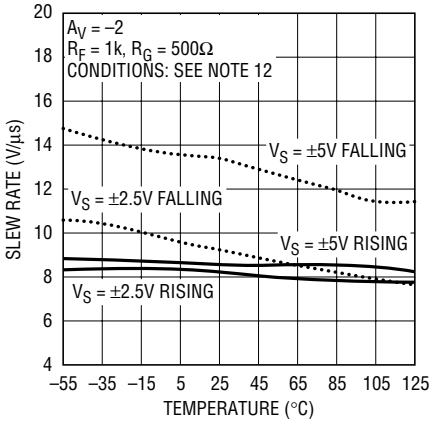
Open Loop Gain vs Frequency



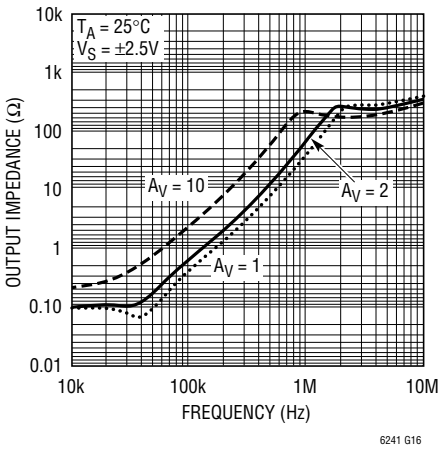
Gain Bandwidth and Phase Margin vs Supply Voltage



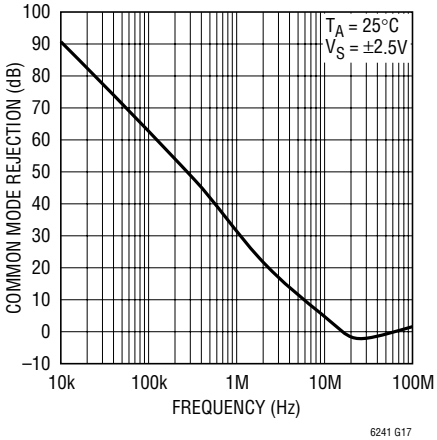
Slew Rate vs Temperature



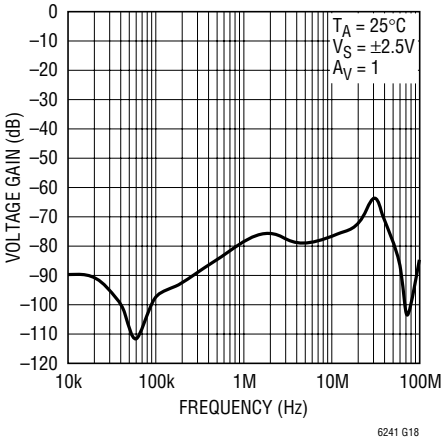
Output Impedance vs Frequency



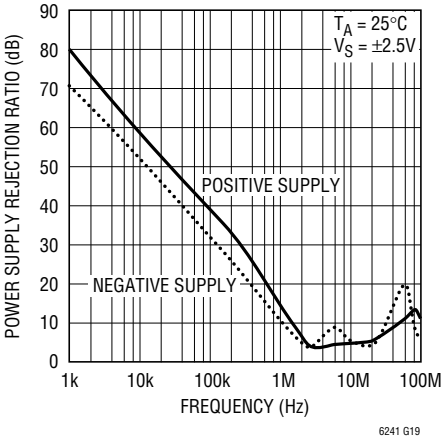
Common Mode Rejection Ratio vs Frequency



Channel Separation vs Frequency

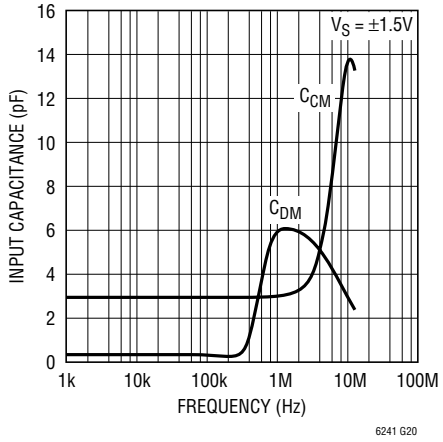


Power Supply Rejection Ratio vs Frequency

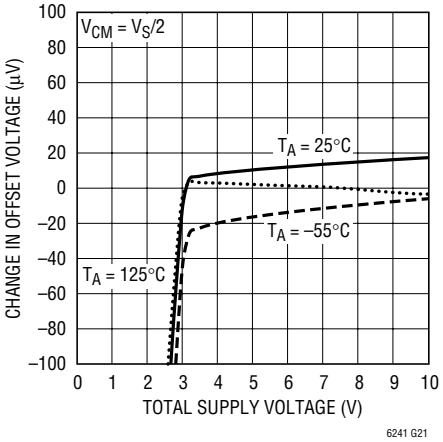


TYPICAL PERFORMANCE CHARACTERISTICS

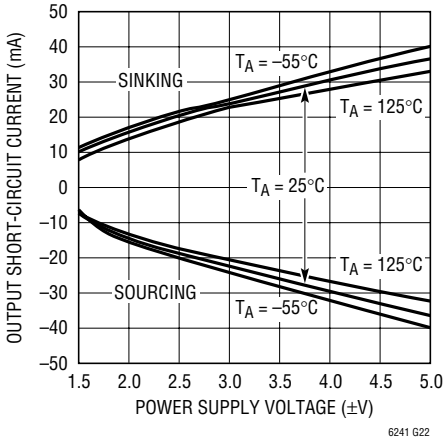
Input Capacitance vs Frequency



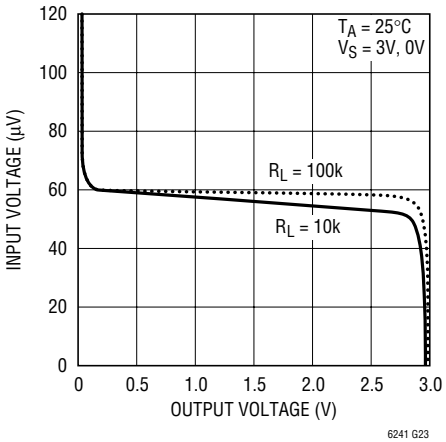
Minimum Supply Voltage



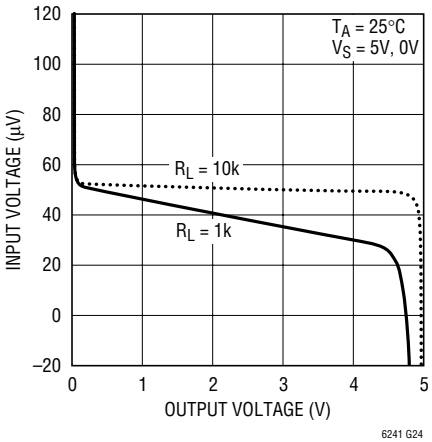
Output Short Circuit Current vs Power Supply Voltage



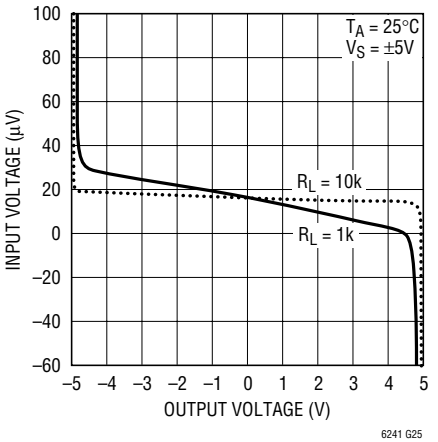
Open Loop Gain



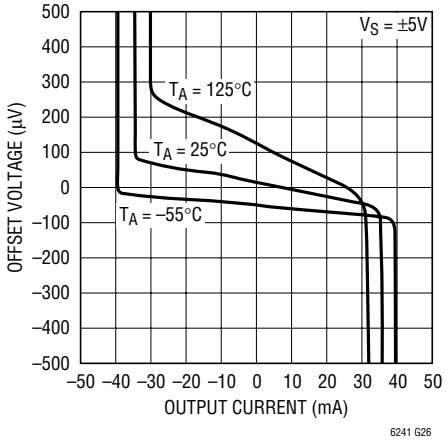
Open Loop Gain



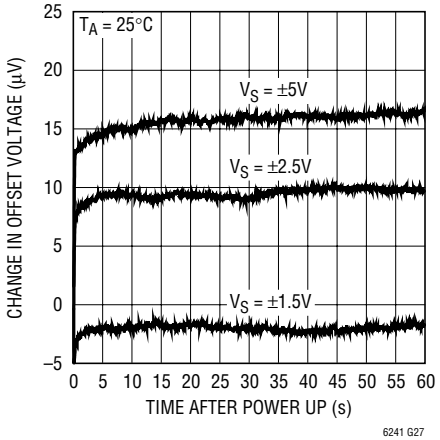
Open Loop Gain



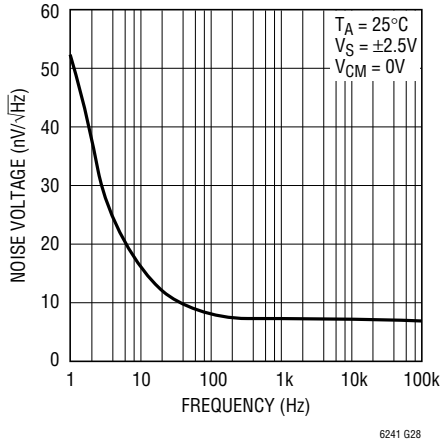
Offset Voltage vs Output Current



Warm-Up Drift vs Time

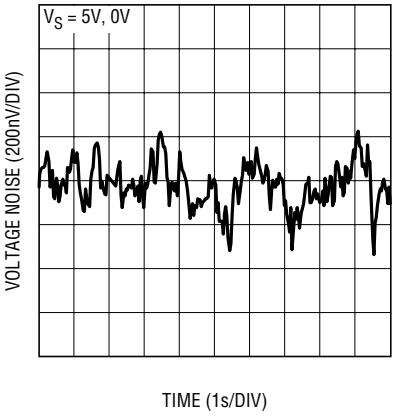


Noise Voltage vs Frequency



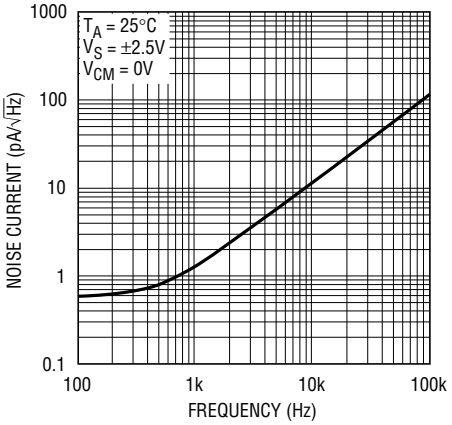
TYPICAL PERFORMANCE CHARACTERISTICS

0.1Hz to 10Hz Voltage Noise



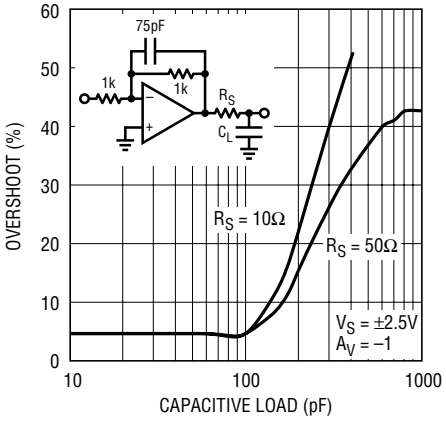
6241 G11

Noise Current vs Frequency



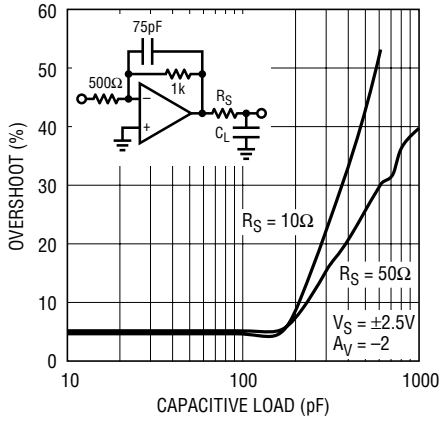
6241 G42

Series Output Resistance and Overshoot vs Capacitive Load



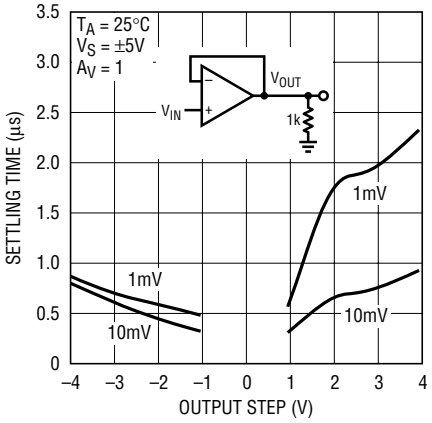
6241 G29

Series Output Resistance and Overshoot vs Capacitive Load



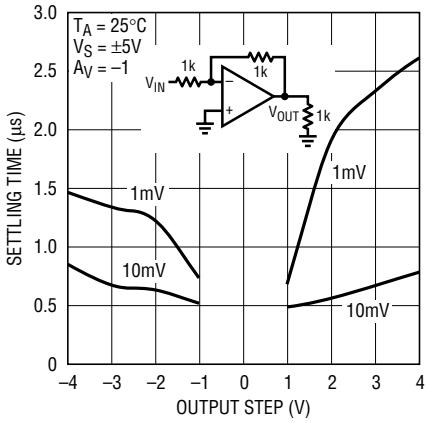
6241 G30

Settling Time vs Output Step (Non-Inverting)



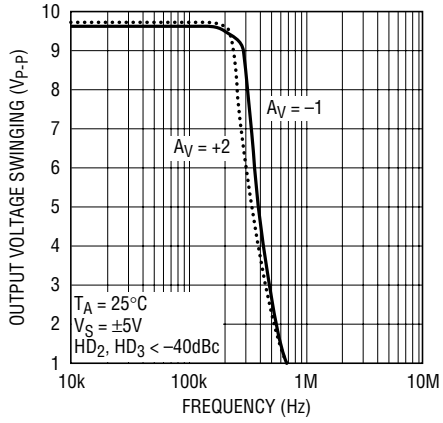
6241 G31

Settling Time vs Output Step (Inverting)



6241 G32

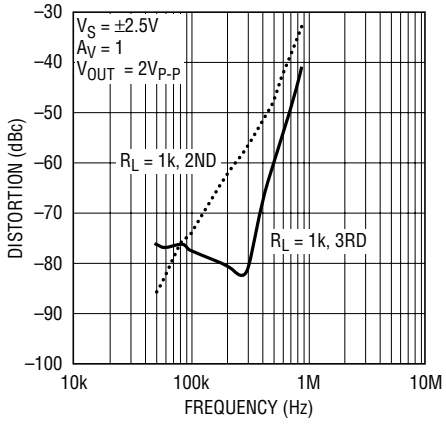
Maximum Undistorted Output Signal vs Frequency



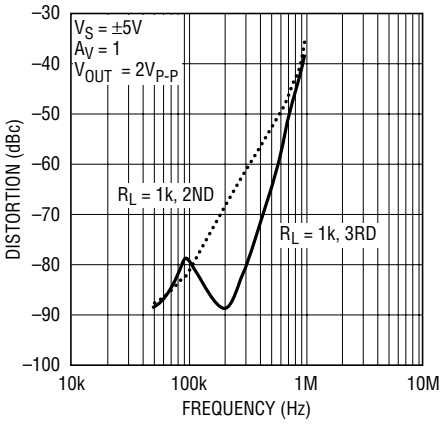
6241 G33

TYPICAL PERFORMANCE CHARACTERISTICS

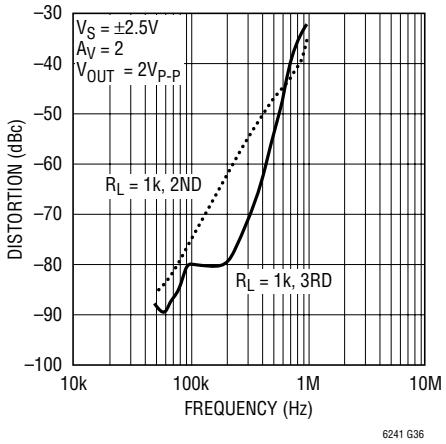
Distortion vs Frequency



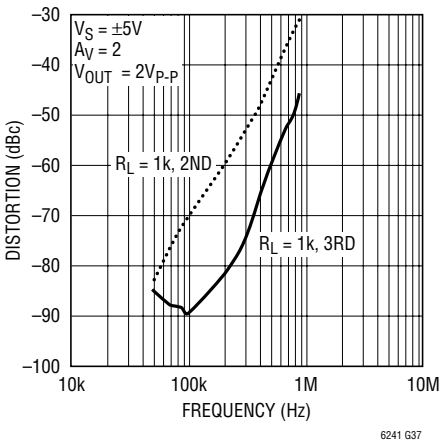
Distortion vs Frequency



Distortion vs Frequency

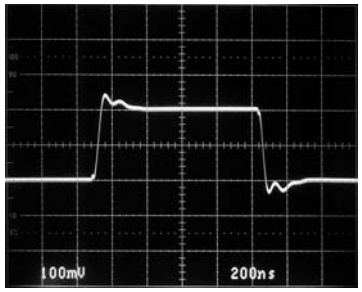


Distortion vs Frequency



TYPICAL PERFORMANCE CHARACTERISTICS

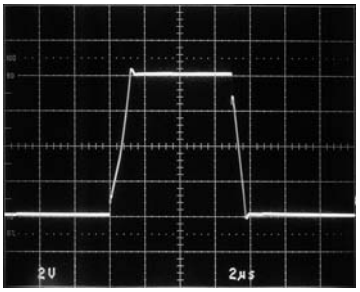
Small Signal Response



6241 G38

$V_S = \pm 2.5V$
$A_V = 1$
$R_L = \infty$

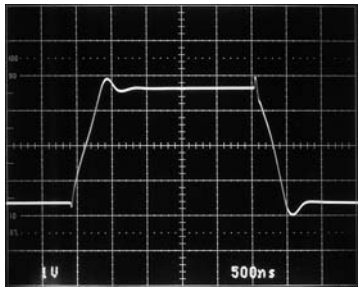
Large Signal Response



6241 G39

$V_S = \pm 5V$
$A_V = 1$
$R_L = \infty$

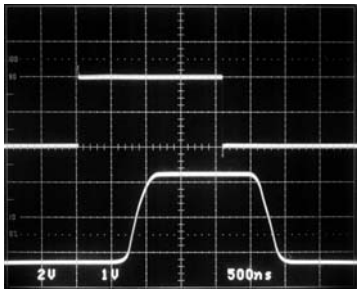
Large Signal Response



6241 G40

$V_S = \pm 2.5V$
$A_V = -1$
$R_L = 1k$

Output Overdrive Recovery



6241 G41

$V_S = \pm 2.5V$ 500ns/DIV
$A_V = 3$
$R_L = \infty$

APPLICATIONS INFORMATION

Amplifier Characteristics

Figure 1 is a simplified schematic of the LTC6241, which has a pair of low noise input transistors M1 and M2. A simple folded cascode Q1, Q2 and R1, R2 allow the input stage to swing to the negative rail, while performing level shift to the Differential Drive Generator. Low offset voltage is accomplished by laser trimming the input stage.

Capacitor C1 reduces the unity cross frequency and improves the frequency stability without degrading the gain bandwidth of the amplifier. Capacitor Cm sets the overall amplifier gain bandwidth. The differential drive generator supplies signals to transistors M3 and M4 that swing the output from rail-to-rail.

The photo of Figure 2 shows the output response to an input overdrive with the amplifier connected as a voltage follower. If the negative going input signal is less than a diode drop below V^-, no phase inversion occurs. For input signals greater than a diode drop below V^-, limit the current to 3mA with a series resistor R_S to avoid phase inversion.

ESD

The LTC6241 has reverse-biased ESD protection diodes on all input and outputs as shown in Figure 1. If these pins are forced beyond either supply, unlimited current will flow through these diodes. If the current is transient and limited to one hundred milliamps or less, no damage to the device will occur.

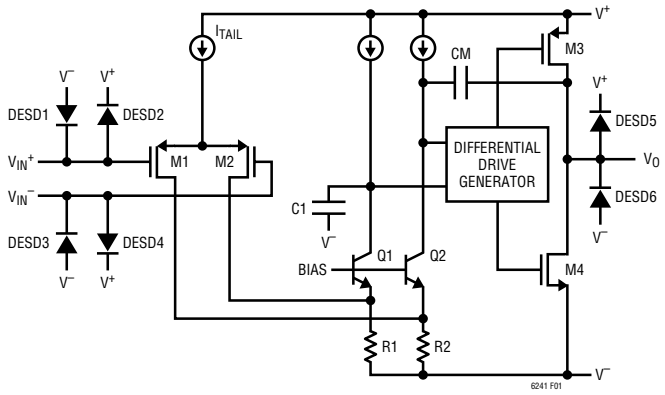


Figure 1. Simplified Schematic

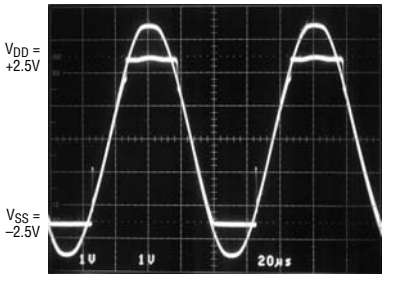
The amplifier input bias current is the leakage current of these ESD diodes. This leakage is a function of the temperature and common mode voltage of the amplifier, as shown in the Typical Performance Curves.

Noise

The LTC6241 exhibits exceptionally low 1/f noise in the 0.1Hz to 10Hz region. This $550nV_{P-P}$ noise allows these op amps to be used in a wide variety of high impedance low frequency applications, where Zero-Drift amplifiers might be inappropriate due to their charge injection.

In the frequency region above 1kHz the LTC6241 also show good noise voltage performance. In this frequency region, noise can easily be dominated by the total source resistance of the particular application. Specifically, these amplifiers exhibit the noise of a 3.1kΩ resistor, meaning it is desirable to keep the source and feedback resistance at or below this value, i.e. $R_S + R_G||R_{FB} \leq 3.1k\Omega$. Above this total source impedance, the noise voltage is not dominated by the amplifier.

Noise current can be estimated from the expression $i_n = \sqrt{2qI_B}$, where $q = 1.6 \bullet 10^{-19}$ coulombs. Equating $\sqrt{4kTR\Delta f}$ and $R\sqrt{2qI_B\Delta f}$ shows that for source resistors below 50GΩ the amplifier noise is dominated by the source resistance. See the Typical Characteristics curve Noise Current vs Frequency.



V_{OUT} AND V_{IN} OF FOLLOWER WITH LARGE INPUT OVERDRIVE

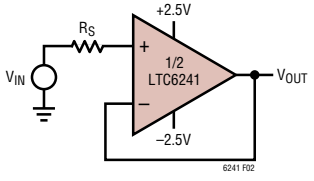


Figure 2. Unity Gain Follower Test Circuit

APPLICATIONS INFORMATION

Proprietary design techniques are used to obtain simultaneous low 1/f noise and low input capacitance. Low input capacitance is important when the amplifier is used with high source and feedback resistors. High frequency noise from the amplifier tail current source, I_{TAIL} in Figure 1, couples through the input capacitance and appears across these large source and feedback resistors. As an example, the photodiode amplifier of Figure 11 on the last page of this data sheet shows the noise results from the LTC6241 and the results of a competitive CMOS amplifier. The LTC6241 output is the ideal noise of a 1MΩ resistor at room temperature, 130nV$\sqrt{Hz}$.

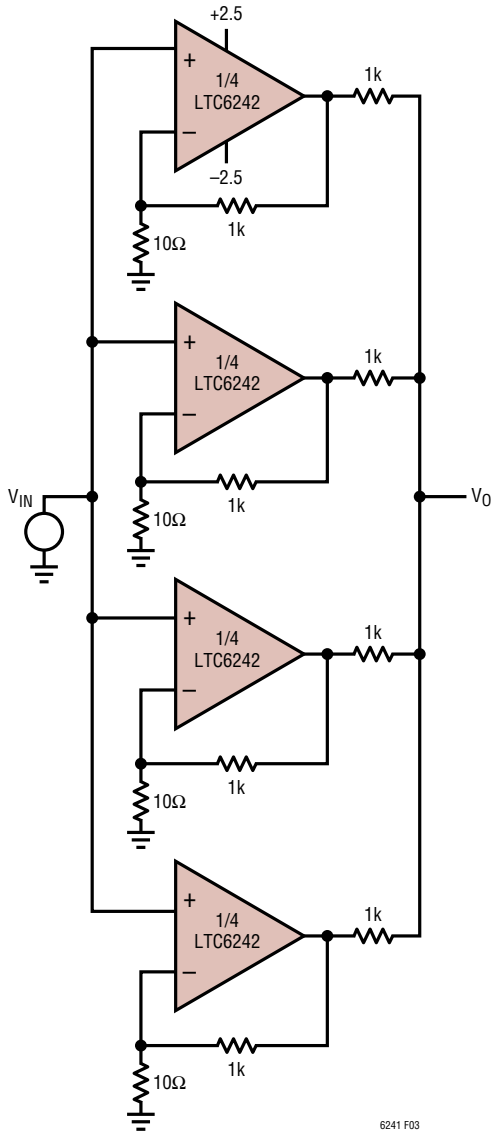


Figure 3. Parallel Amplifier Lowers Noise by 2x

Half the Noise

The circuit shown in Figure 3 can be used to achieve even lower noise voltage. By paralleling 4 amplifiers the noise voltage can be lowered by $\sqrt{4}$, or half as much noise. The $\sqrt{}$ comes about from an RMS summing of uncorrelated noise sources. This circuit maintains extremely high input resistance, and has a 250Ω output resistance. For lower output resistance, a buffer amplifier can be added without influencing the noise.

Stability

The good noise performance of these op amps can be attributed to large input devices in the differential pair. Above several hundred kilohertz, the input capacitance rises and can cause amplifier stability problems if left unchecked. When the feedback around the op amp is resistive (R_F), a pole will be created with R_F, the source resistance, source capacitance (R_S, C_S), and the amplifier input capacitance. In low gain configurations and with R_F and R_S in even the kilohm range (Figure 4), this pole can create excess phase shift and possibly oscillation. A small capacitor C_F in parallel with R_F eliminates this problem.

Low Noise Single-Ended Input to Differential Output Amplifier

The circuit on the first page of the data sheet is a low noise single-ended input to differential output amplifier, with a 200k input impedance. The very low input bias current of the LTC6241 allows for these large input and feedback resistors. The 200k resistors, R1 and R2, along with C1 and C2 set the –3dB bandwidth to 80kHz. Capacitor C3 is used to cancel effects of input capacitance, while C4 adds

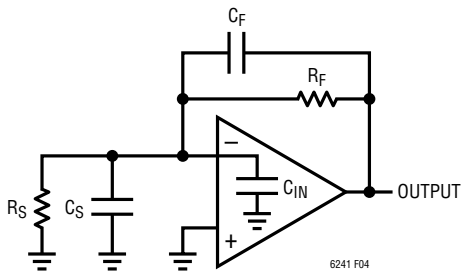


Figure 4. Compensating Input Capacitance

APPLICATIONS INFORMATION

phase lead to compensate the phase lag of the second amplifier. The op amp's good input offset voltage match and low input bias current means that the typical differential output voltage is less than 40µV. A noise spectrum plot of the differential output is shown in Figure 5.

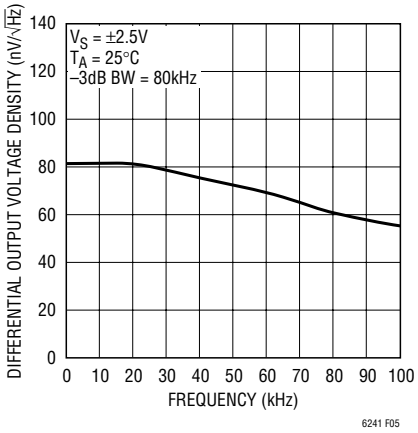


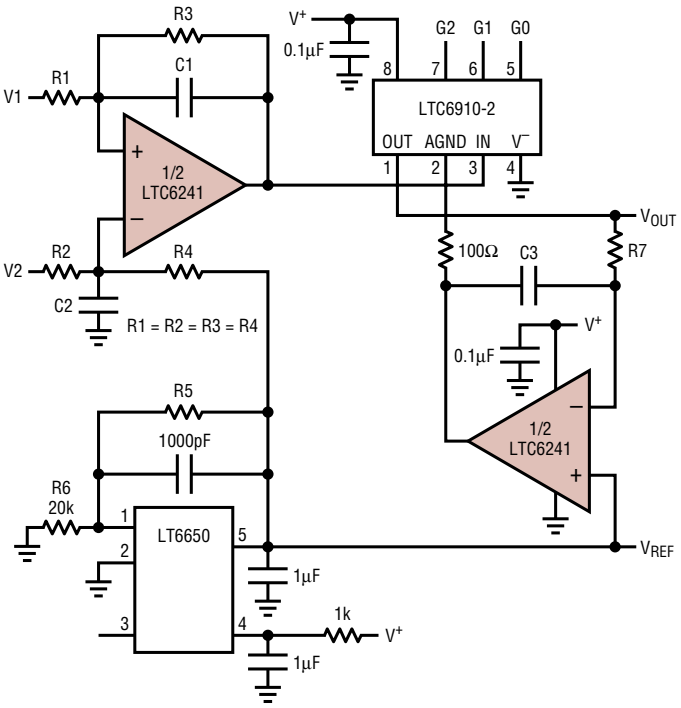
Figure 5. Differential Output Noise

Achieving Low Input Bias Current

The DD package is leadless and makes contact to the PCB beneath the package. Solder flux used during the attachment of the part to the PCB can create leakage current paths and can degrade the input bias current performance of the part. All inputs are susceptible because the backside paddle is connected to V^- internally. As the input voltage changes or if V^- changes, a leakage path can be formed and alter the observed input bias current. For lowest bias current, use the LTC6241 in the SO-8 and provide a guard ring around the inputs that are tied to a potential near the input voltage.

A Digitally Programmable AC Difference Amplifier

The LTC6241 configured as a difference amplifier, can be combined with a programmable gain amplifier (PGA) to obtain a low noise high speed programmable difference amplifier. Figure 6 shows the LTC6241 based as a single-supply AC amplifier. One LTC6241 op amp is used at the circuit's input as a standard four resistor difference amplifier. The low bias current and current noise of the LTC6241 allow the use of high valued input resistors, 100k or greater. Resistors R1, R2, R3 and R4 are equal and the gain of the difference amplifier is one. An LTC6910-2 PGA amplifies the difference amplifier output with inverting gains of –1, –2, –4, –8, –16, –32 and –64. The second LTC6241 op amp is used as an integrator to set the DC output voltage equal to the LT6650 reference voltage V_{REF}. The integrator drives the PGA analog ground to provide a feedback loop, in addition to blocking any DC voltage through the PGA. The reference voltage of the LT6650 can be set to a voltage from 400mV to V^+ – 350mV with resistors R5 and R6. If R6 is 20k or less, the error due to the LT6650 op amp bias current is negligible. The low voltage offset and drift of the LTC6241 integrator will not contribute any significant error to the LT6650 reference voltage. The LT6650 V_{REF} voltage has a maximum error



DIGITAL INPUTS G2	G1	G0	GAIN
0	0	0	0
0	0	1	–1
0	1	0	–2
0	1	1	–4
1	0	0	–8
1	0	1	–16
1	1	0	–32
1	1	1	–64

$V_{OUT} = (V1 - V2)\ GAIN + V_{REF}$

$V_{REF} = 0.4 \bullet \left(\frac{R5}{R6} + 1\right)$

$R5 = 10k \bullet (5 \bullet V_{REF} - 2) \quad R6 = 20k$

$-3d\ BANDWIDTH = (f_{HIGH} - f_{LOW})$

$f_{HIGH} = \frac{1}{2 \bullet \pi \bullet R3 \bullet C1} \quad f_{LOW} = \frac{GAIN}{2 \bullet \pi \bullet R7 \bullet C3}$

6241 F06

Figure 6. Wideband Difference Amplifier with High Input Impedance and Digitally Programmable Gain

APPLICATIONS INFORMATION

of ±2% with 1% resistors. The upper –3dB frequency of the amplifier is set by resistor R3 and capacitor C1 and is limited by the bandwidth of the PGA when operated at a gain of 64. Capacitor C2 is equal to C1 and is added to maintain good common mode rejection at high frequency. The lower –3dB frequency is set by the integrator resistor R7, capacitor C3, and the gain setting of the LTC6910-2 PGA. This lower –3dB zero frequency is multiplied by the PGA gain. The rail-to-rail output of the LTC6910-2 PGA allows for a maximum output peak-to-peak voltage equal to twice the V_{REF} voltage. At the maximum gain setting of 64, the maximum peak-to-peak difference between inputs V1 and V2 is equal to twice V_{REF} divided by 64.

Example Design: Design a programmable gain AC difference amplifier, with a bandwidth 10Hz to 100kHz, an input impedance equal or greater than 100kΩ, and an output DC reference equal to 1V.

a. Select input resistors R1, R2, R3 and R4 equal to 100k.

b. If the upper –3dB frequency is 100kHz then C1 = 1/(2π • R2 • f3dB) = 1/(6.28 • 100kΩ • 100kHz) = 15pF (to the nearest 5% value) and C2 = C1 = 15pF.

c. Select R7 equal to one 1M and set the lower –3dB frequency to 10Hz at the highest PGA gain of 64, then C3 = Gain/(2π • R7 • f3dB) = 64/(6.28 • 100kΩ • 10Hz) = 1uF. Lower gains settings will give a lower f3dB.

d. Calculate the value of R5 to set the LT6650 reference equal to 1V;

   V_{REF} = 0.4(R5/R6 + 1), so R5 = R6(2.5V_{REF} – 1). For R6 = 20kΩ, R5 = 30kΩ

   With V_{REF} = 1V the maximum input difference voltage is equal to 2V/64 = 31.2mV.

40nVpp Noise, 0.05µV/°C Drift, Chopped FET Amplifier

Figure 7's circuit combines the 5V rail-to-rail performance of the LTC6241 with a pair of extremely low noise JFETs configured in a chopper based carrier modulation scheme to achieve an extraordinarily low noise and low DC drift. The performance of this circuit is suited for the demanding transducer signal conditioning situations such as high resolution scales and magnetic search coils.

The LTC1799's output is divided down to form a 2-phase 925Hz square wave clock. This frequency, harmonically unrelated to 60Hz, provides excellent immunity to harmonic beating or mixing effects which could cause instabilities. S1 and S2 receive complementary drive, causing A1 to see a chopped version of the input voltage. A1's square wave output is synchronously demodulated by S3 and S4. Because these switches are synchronously driven with the input chopper, proper amplitude and polarity information is presented to A2, the DC output amplifier. This stage integrates the square wave into a DC voltage, providing the output. The output is divided down (R2 and R1) and fed back to the input chopper where it serves as a zero signal reference. Gain, in this case 1000, is set by the R1-R2 ratio. Because A1 is AC coupled, its DC offset and drift do not affect the overall circuit offset, resulting in the extremely low offset and drift noted. The JFETs have an input RC damper that minimizes offset voltage contribution due to parasitic switch behavior, resulting in the 1µV offset specification.

The noise measured over a 50 second interval, in Figure 8, is 40nV in a 0.1Hz to 10Hz bandwidth. This low noise is attributed to the input JFET's die size and current density.

APPLICATIONS INFORMATION

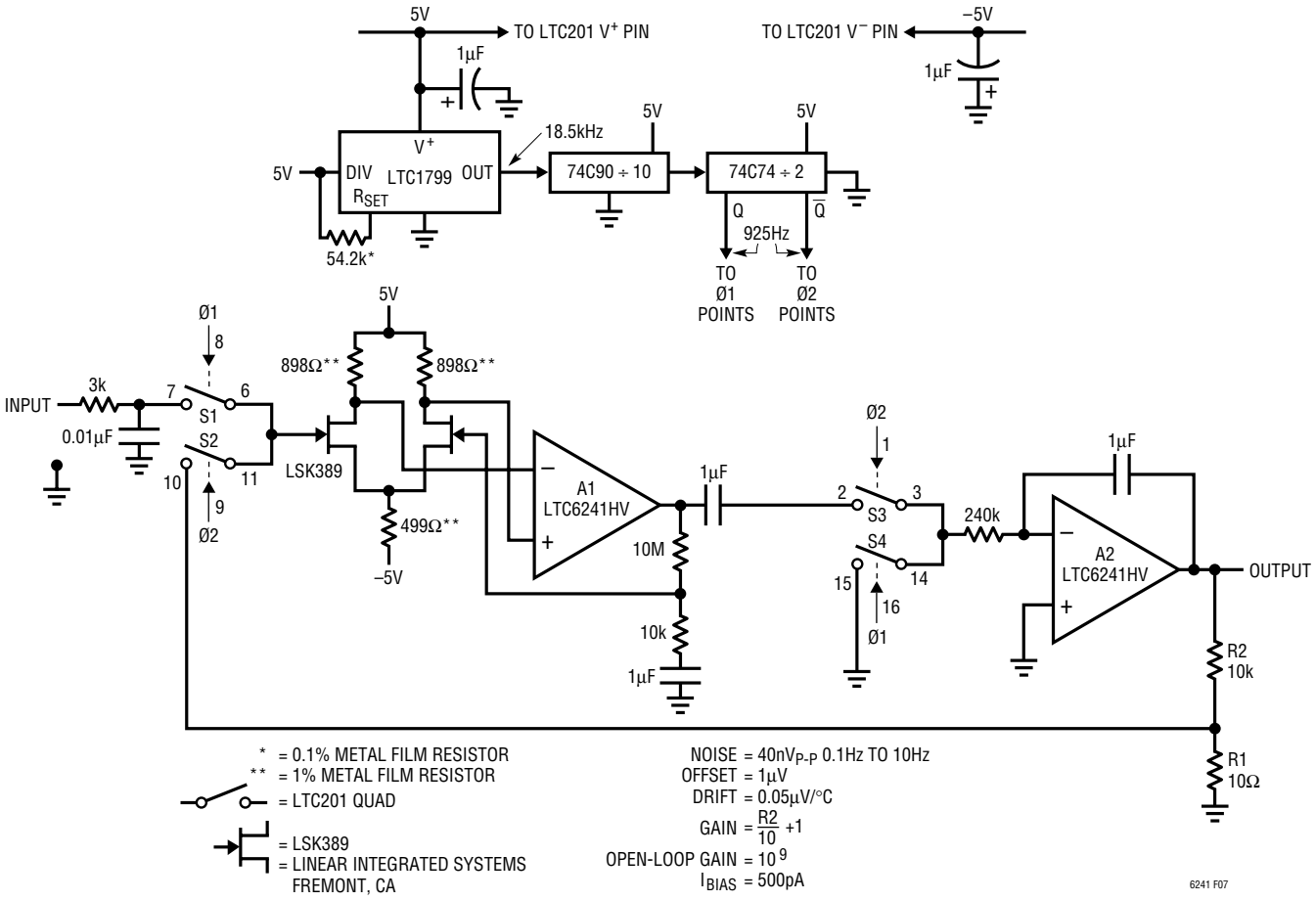


Figure 7. Ultra Low Noise Chopper Amplifier

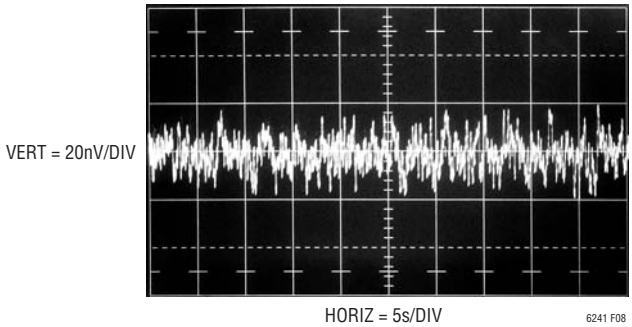


Figure 8. Noise in a 0.1Hz to 10Hz Bandwidth

APPLICATIONS INFORMATION

Low Noise Shock Sensor Amplifiers

Figures 9 and 10 show the LTC6241 realizing two different approaches to amplifying signals from a capacitive sensor. The sensor in both cases is a 770pF piezoelectric shock sensor accelerometer, which generates charge under physical acceleration.

Figure 9 shows the classical "charge amplifier" approach. The LTC6241 is in the inverting configuration so the sensor looks into a virtual ground. All of the charge generated by the sensor is forced across the feedback capacitor by the op amp action. Because the feedback capacitor is 100 times smaller than the sensor, it will be forced to 100 times what would have been the sensor's open circuit voltage. So the circuit gain is 100. The benefit of this approach is that the signal gain of the circuit is independent of any cable capacitance introduced between the sensor and the amplifier. Hence this circuit is favored for remote accelerometers where the cable length may vary. Difficulties with the circuit are inaccuracy of the gain setting with the small capacitor, and low frequency cutoff due to the bias resistor working into the small feedback capacitor.

Figure 10 shows a non-inverting amplifier approach. This approach has many advantages. First of all, the gain is set accurately with resistors rather than with a small capacitor. Second, the low frequency cutoff is dictated by the bias resistor working into the large 770pF sensor, rather than into a small feedback capacitor, for lower frequency response. Third, the non-inverting topology can be paralleled and summed (as shown) for scalable reductions in voltage noise. The only drawback to this circuit is that the parasitic capacitance at the input reduces the gain slightly. This circuit is favored in cases where parasitic input capacitances such as traces and cables will be relatively small and invariant.

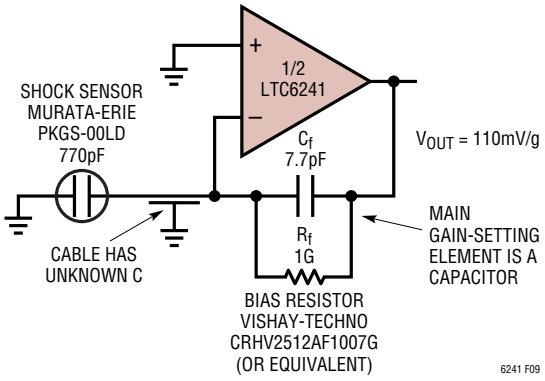


Figure 9. Classical Inverting Charge Amplifier

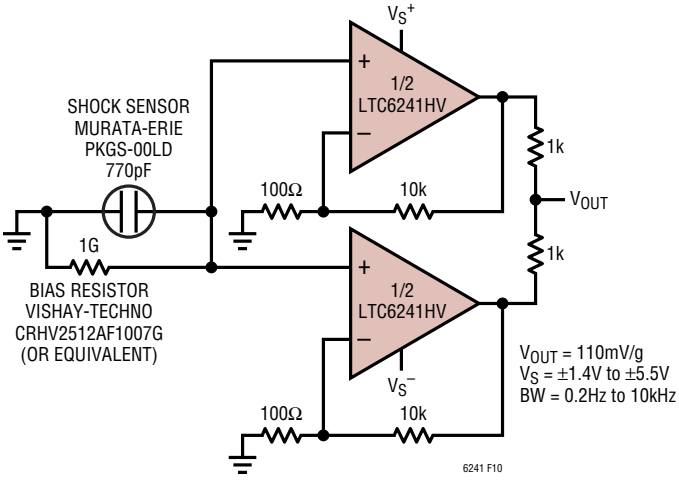
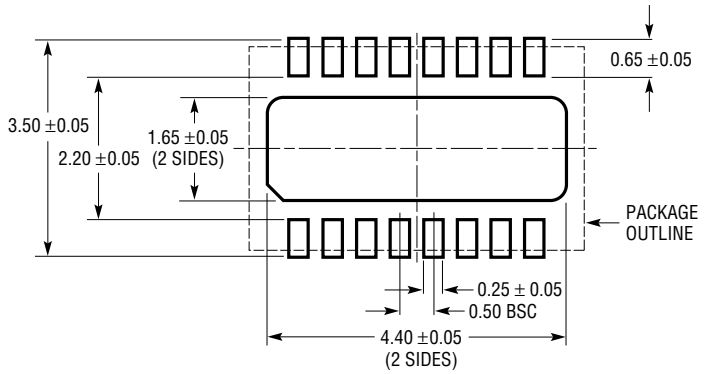


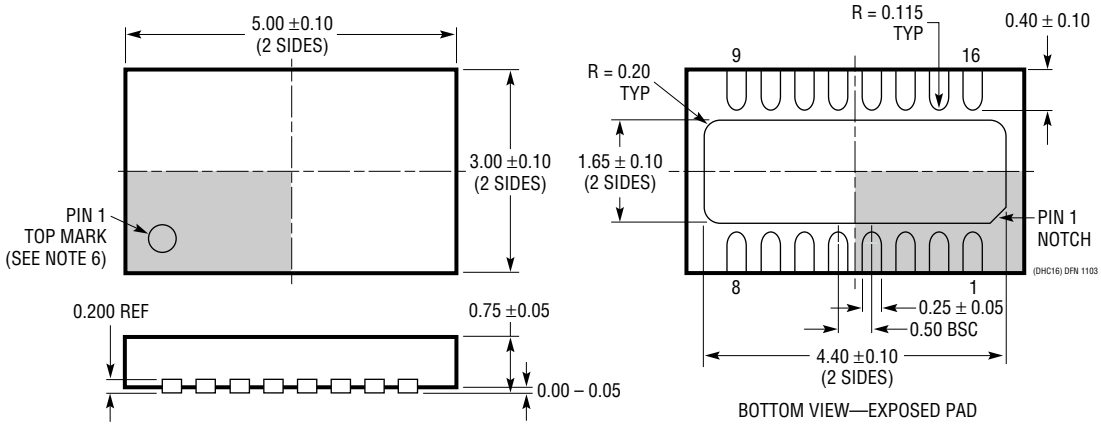
Figure 10. Low Noise Non-Inverting Shock Sensor Amplifier

PACKAGE DESCRIPTION

DHC Package
16-Lead Plastic DFN (5mm × 3mm)
(Reference LTC DWG # 05-08-1706)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS

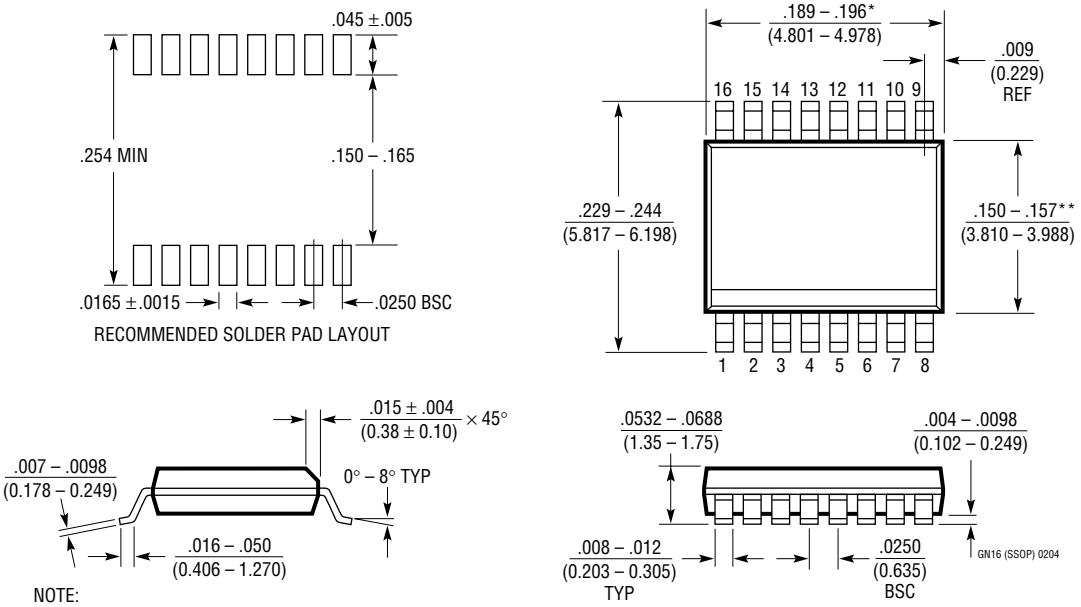


BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING PROPOSED TO BE MADE VARIATION OF VERSION (WJED-1) IN JEDEC PACKAGE OUTLINE MO-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

GN Package
16-Lead Plastic SSOP (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1641)



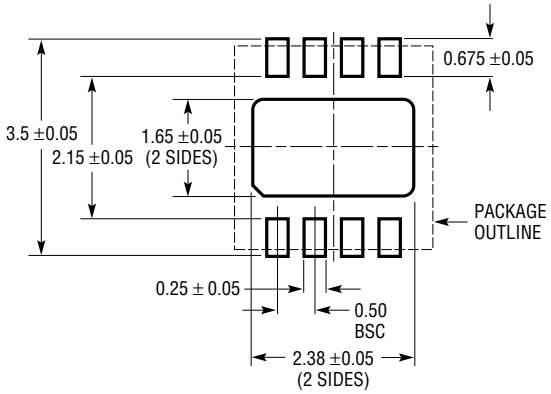
NOTE:
1. CONTROLLING DIMENSION: INCHES
2. DIMENSIONS ARE IN $\frac{\text{INCHES}}{(\text{MILLIMETERS})}$
3. DRAWING NOT TO SCALE

*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

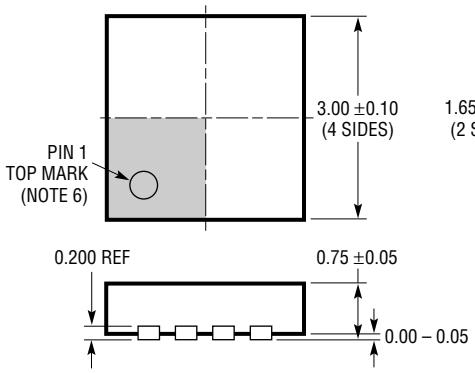
**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

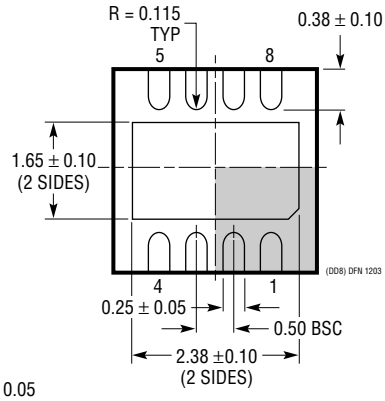
PACKAGE DESCRIPTION

DD Package
8-Lead Plastic DFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1698)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



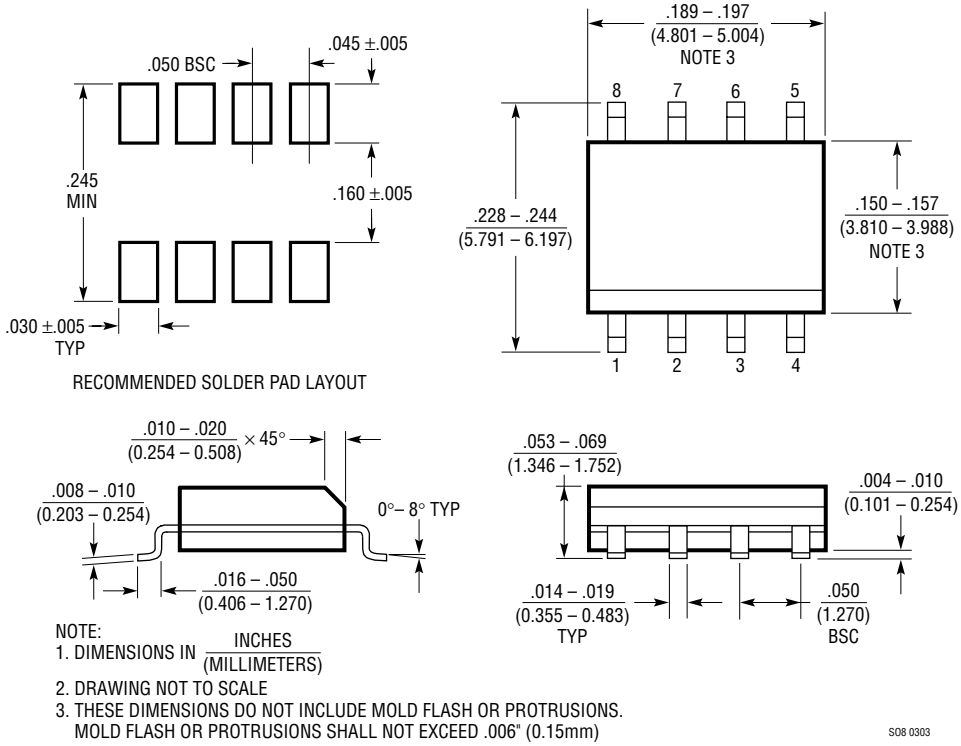


BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-1)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

S8 Package
8-Lead Plastic Small Outline (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1610)



NOTE:
1. DIMENSIONS IN $\frac{\text{INCHES}}{(\text{MILLIMETERS})}$
2. DRAWING NOT TO SCALE
3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
   MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)

SO8 0303

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TYPICAL APPLICATION

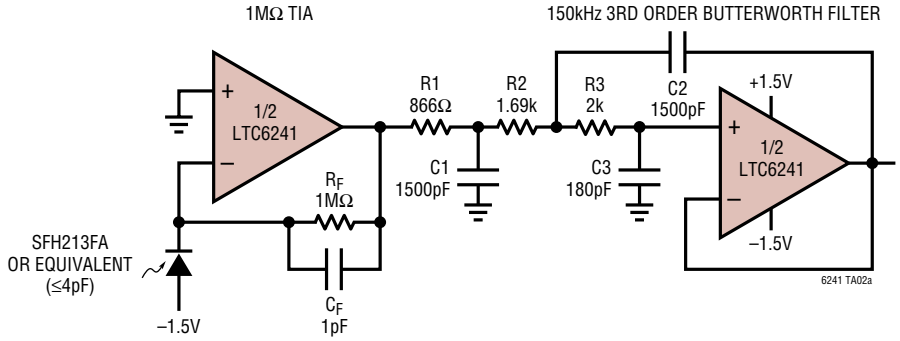
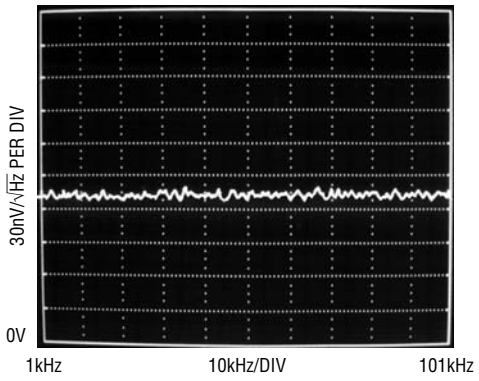
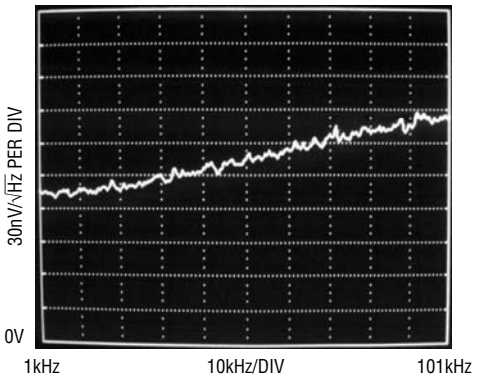


Figure 11. Ultralow Noise 1MΩ 150kHz Photodiode Amplifier

LTC6241 Output Noise Spectrum. 1MΩ Resistor Noise Dominates; Ideal Performance



Competition Output Noise Spectrum. Op Amp Noise Dominates; Performance Compromised



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1151	±15V Zero-Drift Op Amp	Dual High Voltage Operation ±18V
LT1792	Low Noise Precision JFET Op Amp	6nV/√Hz Noise, ±15V Operation
LTC2050	Zero-Drift Op Amp	2.7 Volt Operation, SOT-23
LTC2051/LTC2052	Dual/Quad Zero-Drift Op Amp	Dual/Quad Version of LTC2050 in MS8/GN16 Packages
LTC2054/LTC2055	Single/Dual Zero-Drift Op Amp	Micropower Version of the LTC2050/LTC2051 in SOT-23 and DD Packages

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