Dual SIM/Smart Card Power Supply and Interface

FEATURES

- **Power Management and Signal Level Translators for Two SIM Cards or Smart Cards**
- **Independent 1.8V/3V V_{CC} Control for Both Cards**
- **Automatic Level Translation**
- **ISO7816, ETSI and EMV Compatible**
- Dynamic Pull-Ups Deliver Fast Signal Rise Times*
- Built-In Fault Protection Circuitry
- Automatic Activation/Deactivation Sequencing Circuitry
- Low Operating/Shutdown Current
- >10kV ESD on SIM Card Pins
- Compatible with EMV Fault Tolerance Requirements
- Available in 16-Lead (3mm × 3mm) QFN Package

APPLICATIONS

- GSM and 3G Cellular Phones
- Wireless P.O.S. Terminals
- Multiple SAM Card Interface

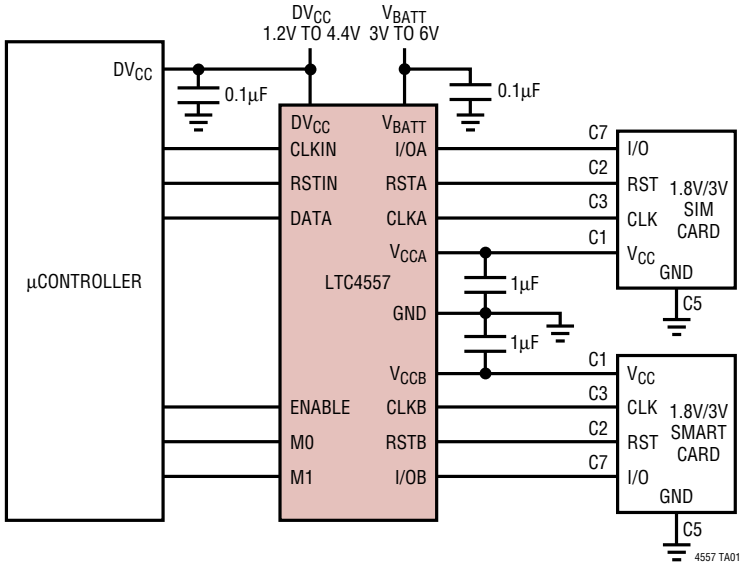
DESCRIPTION

The LTC®4557 provides power conversion and signal level translation needed for 2.5G and 3G cellular telephones to interface with 1.8V or 3V subscriber identity modules (SIMs). The part meets all requirements for 1.8V and 3V SIMs. The part contains LDO regulators to power 1.8V or 3V SIM cards from a 2.7V to 5.5V input. The output voltages can be set using the two voltage selection pins and up to 50mA of load current can be supplied.

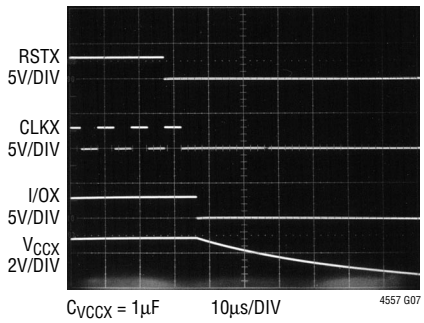
Internal level translators allow controllers operating with supplies as low as 1.2V to interface with 1.8V or 3V smart cards. Battery life is maximized by a low operating current of less than 100µA and a shutdown current of less than 1µA. Board area is minimized by the low profile 3mm × 3mm × 0.75mm leadless QFN package.

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*U.S. Patent No. 6,356,140

TYPICAL APPLICATION



Deactivation Sequence

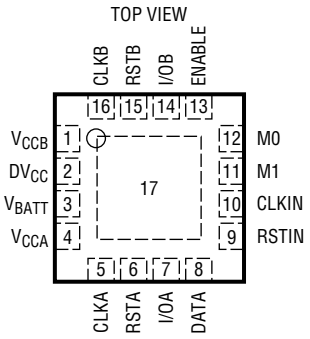


ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{BATT}, DV_{CC}, DATA, RSTIN, CLKIN, ENABLE, M0, M1 to GND ..... −0.3V to 6V
I/OA, CLKA, RSTA ..... −0.3V to V_{CCA} + 0.3V
I/OB, CLKB, RSTB ..... −0.3V to V_{CCB} + 0.3V
$I_{CCA,B}$ (Note 4) 80mA
$V_{CCA,B}$ Short-Circuit Duration ..... Indefinite
Operating Temperature Range (Note 3) .. −40°C to 85°C
Storage Temperature Range ..... −65°C to 125°

PACKAGE/ORDER INFORMATION



UD PACKAGE
16-LEAD (3mm × 3mm) PLASTIC QFN

T_{JMAX} = 125°C, θ_{JA} = 68°C/W, θ_{JC} = 42°C/W
EXPOSED PAD (PIN 17) IS GND
(MUST BE SOLDERED TO PCB)

ORDER PART NUMBER
LTC4557EUD
UD PART MARKING
LAHP

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{BATT} = 3.3V, DV_{CC} = 1.8V, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Power Supply							
	V_{BATT} Operating Voltage		●	2.7		5.5	V
	I_{VBATT} Operating Current	V_{CCA} = 3V, V_{CCB} = 0V, I_{CCA} = I_{CCB} = 0µA V_{CCA} = 1.8V, V_{CCB} = 0V, I_{CCA} = I_{CCB} = 0µA	● ●		65 65	100 100	µA µA
	DV_{CC} Operating Voltage		●	1.2		5.5	V
	I_{DVCC} Operating Current		●		6	10	µA
	I_{DVCC} Shutdown Current		●		0.1	1	µA
	I_{VBATT} Shutdown Current	 DV_{CC} = 0V	● ●		0.4 0.1	2.5 1.0	µA µA
SIM Card Supplies							
	$V_{CCA,B}$ Output Voltage	3V Mode, 0mA < $I_{CCA,B}$ < 50mA 1.8V Mode, 0mA < $I_{CCA,B}$ < 30mA	● ●	2.75 1.65	3.0 1.8	3.25 1.95	V V
	Channel Turn-On Time	$I_{CCA,B}$ = 0mA, ↑ ENABLE to ↑ $I_{OA/B}$	●		1.3	2.5	ms
CLKA, CLKB							
V_{OL}	Low Level Output Voltage	Sink Current = −200µA (Note 2)	●			0.2	V
V_{OH}	High Level Output Voltage	Source Current = 200µA (Note 2)	●	$V_{CCA,B}$ − 0.2			V
	Rise, Fall Time	Loaded with 33pF (10% to 90%) (Note 2)	●			16	ns
	CLKA, CLKB Frequency	(Note 2)	●	10			MHz
RSTA, RSTB							
V_{OL}	Low Level Output Voltage	Sink Current = −200µA (Note 2)	●			0.2	V
V_{OH}	High Level Output Voltage	Source Current = 200µA (Note 2)	●	$V_{CCA,B}$ − 0.2			V
	Rise, Fall Time	Loaded with 33pF (10% to 90%) (Note 2)	●			100	ns

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{BATT} = 3.3V, DV_{CC} = 1.8V, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I/OA, I/OB							
V_{OL}	Low Level Output Voltage	Sink Current = –1mA (V_{DATA} = 0V) (Note 2)	●			0.3	V
V_{OH}	High Level Output Voltage	Source Current = 20µA (V_{DATA} = V_{DVCC}) (Note 2)	●	0.85 • $V_{CCA,B}$			V
	Rise Time	Loaded with 33pF (10% to 90%) (Note 2)	●		200	500	ns
	Short-Circuit Current	V_{DATA} = 0V (Note 2)	●		5	10	mA
DATA							
V_{OL}	Low Level Output Voltage	Sink Current = –500µA ($V_{I/OA,B}$ = 0V)	●			0.3	V
V_{OH}	High Level Output Voltage	Source Current = 20µA ($V_{I/OA,B}$ = $V_{CCA,B}$)	●	0.8 • DV_{CC}			V
	Rise Time	Loaded with 33pF (10% to 90%)	●		200	500	ns
RSTIN, CLKIN, ENABLE, M0, M1							
V_{IL}	Low Input Threshold		●			0.15 • DV_{CC}	V
V_{IH}	High Input Threshold		●	0.85 • DV_{CC}			V
	Input Current (I_{IH}, I_{IL})		●	–1		1	µA

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

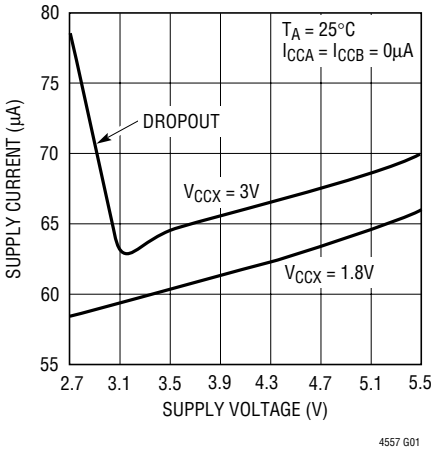
Note 2: This specification applies to both 1.8V and 3V smart cards.

Note 3: The LTC4557E is guaranteed to meet performance specifications from 0°C to 70°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls.

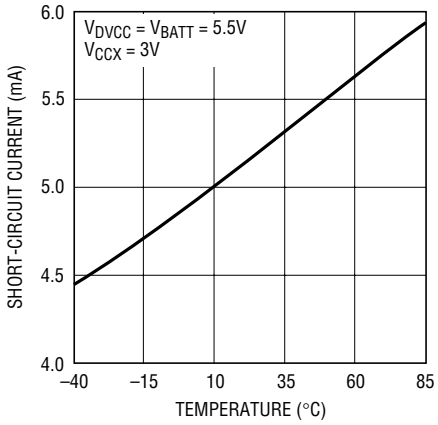
Note 4: Based on long term current density limitations.

TYPICAL PERFORMANCE CHARACTERISTICS

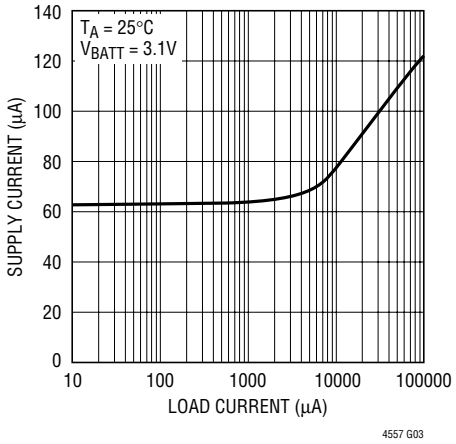
No Load Supply Current vs V_{BATT}



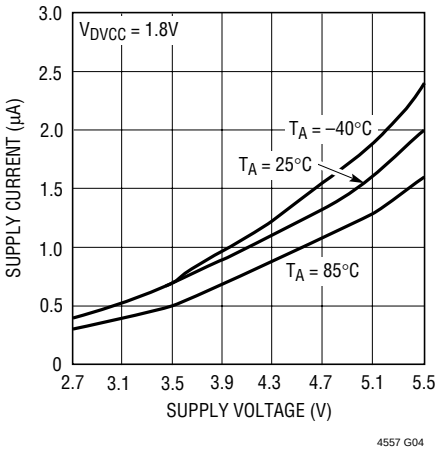
I/O X Short-Circuit Current vs Temperature



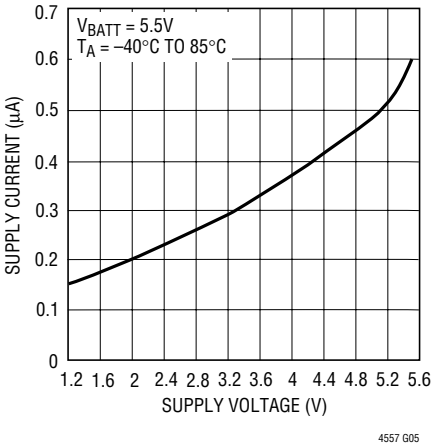
V_{BATT} Quiescent Current ($I_{VBATT} – I_{CC}$) vs Load Current



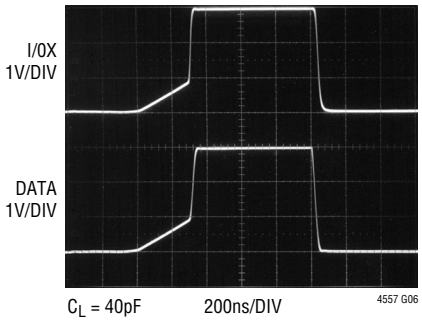
V_{BATT} Shutdown Current vs Supply Voltage



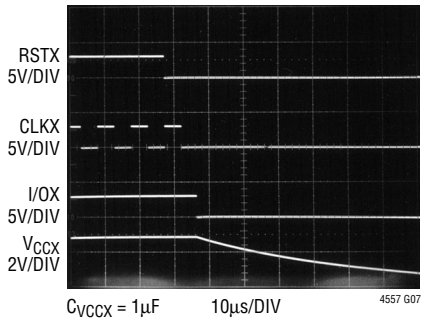
DV_{CC} Shutdown Current vs Supply Voltage



Data – I/O Channel, C_L = 40pF



Deactivation Sequence, C_{VCCX} = 1µF



PIN FUNCTIONS

DV_{CC} (Pin 2): Power. Reference voltage for the control logic.

V_{BATT} (Pin 3): Power. Supply voltage for the analog sections of the LTC4557.

V_{CCA}/V_{CCB} (Pins 4, 1): Card Socket. The V_{CCA}/V_{CCB} pins should be connected to the V_{CC} pins of the respective card sockets. The activation of the V_{CCA}/V_{CCB} pins is controlled by the M0, M1 and ENABLE inputs. They can be set to 0V, 1.8V or 3V. Only one of the two, either V_{CCA} or V_{CCB}, may be active at a time.

CLKA/CLKB (Pins 5, 16): Card Socket. The CLKA/CLKB pins should be connected to the CLK pins of the respective card sockets. The CLKA/CLKB signals are derived from the CLKIN pin. They provide a level shifted CLKIN signal to the selected card. The CLKA/CLKB pins are gated off until V_{CCA}/V_{CCB} attain their correct values.

RSTA/RSTB (Pins 6, 15): Card Socket. The RSTA/RSTB pins should be connected to the RST pins of the respective card sockets. The RSTA/RSTB signals are derived from the RSTIN pin. When a card is selected, its RST pin follows RSTIN. The RSTA/RSTB pins are gated off until V_{CCA}/V_{CCB} attain their correct values.

I/OA, I/OB (Pins 7, 14): Card Socket. The I/OA, I/OB pins connect to the I/O pins of the respective card sockets. When a card is selected, its I/O pin transmits/receives data to/from the DATA pin. The I/OA, I/OB pins are gated off until V_{CCA}/V_{CCB} attain their correct values.

DATA (Pin 8): Input/Output. Microcontroller side data I/O pin. The DATA pin provides the bidirectional communication path to both cards. Only one of the cards may be selected to communicate via the DATA pin. The pin possesses a dynamically activated pull-up current source, allowing the controller to use an open-drain output. The current source maintains a HIGH state. This pin is held HIGH by a weak pull-up when the ENABLE pin is LOW.

RSTIN (Pin 9): Input. The RSTIN pin supplies the reset signal to the cards. It is level shifted and transmitted directly to the RST pin of the selected card.

CLKIN (Pin 10): Input. The CLKIN pin supplies the clock signal to the cards. It is level shifted and transmitted directly to the CLK pin of the selected card.

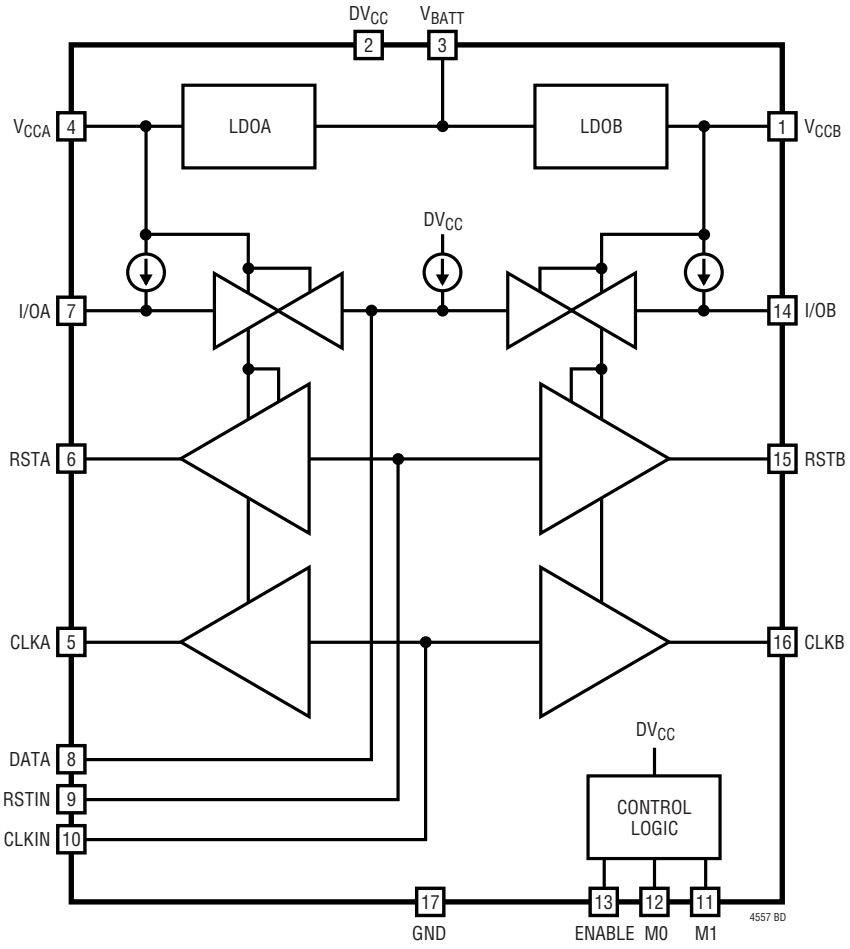
M0/M1 (Pins 12, 11): Inputs. The M0 and M1 pins select which set of SIM/smart card pins are active and at which voltage level they operate. The truth table for these pins follows:

M1	M0	SELECTED CARD/VOLTAGE
0	0	Card A/1.8V
0	1	Card A/3V
1	0	Card B/1.8V
1	1	Card B/3V

ENABLE (Pin 13): Input. The ENABLE pin shuts down the chip when LOW.

EXPOSED PAD (Pin 17): Chip Ground. This ground pad must be soldered directly to a PCB ground plane.

BLOCK DIAGRAM



OPERATION

The LTC4557 features two independent smart card channels. Only one of these channels may operate at a time. Each channel is able to output two voltage levels: 1.8V and 3V. The channel selection and voltage selection are controlled by the ENABLE, M0 and M1 pins as shown in Table 1.

Table 1. Channel and Voltage Truth Table

ENABLE	M1	M0	SELECTED CARD/VOLTAGE
1	0	0	Card A/1.8V
1	0	1	Card A/3V
1	1	0	Card B/1.8V
1	1	1	Card B/3V
0	X	X	A and B Disabled

Bidirectional Channels

The bidirectional channels are level shifted to the appropriate $V_{CCA,B}$ voltages at the I/OA,B pins. An NMOS pass transistor performs the level shifting. The gate of the NMOS transistor is biased such that the transistor is completely off when both sides have relinquished the channel. If one side of the channel asserts a LOW, then the transistor will convey the LOW to the other side. Note that current passes from the receiving side of the channel to the transmitting side. The low output voltage of the receiving side will be dependent upon the voltage at the transmitting side plus the IR drop of the pass transistor.

When a card socket is selected, it becomes a candidate to drive data on the DATA pin and likewise receive data from the DATA pin. When a card socket is deselected, the voltage on its I/OA,B pin will be disabled and set to LOW. If both cards are deselected, a weak pull-up ensures that the DATA pin is held HIGH.

Dynamic Pull-up Current Sources

The current sources on the bidirectional pins (DATA/I/OA,B) are dynamically activated to achieve a fast rise time with a relatively small static current. Once a bidirectional pin is relinquished, a small start-up current begins to charge the node. An edge rate detector determines if the pin is released by comparing its slew rate with an internal reference value. If a valid transition is detected, a large pull-up current enhances the edge rate on the node. The higher slew rate corroborates the decision to charge the node thereby affecting a dynamic form of hysteresis.

Reset Channels

When a card is selected, the reset channel provides a level shifted path from the RSTIN pin to the RSTA,B pin. When a card is deselected its reset pin is pulled LOW.

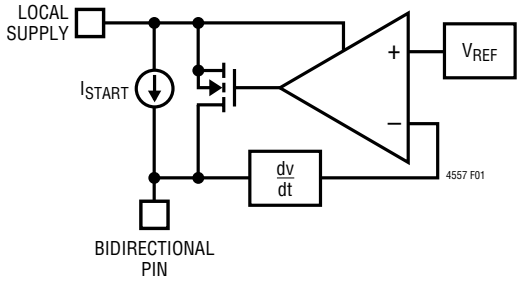


Figure 1. Dynamic Pull-Up Current Source

OPERATION

Activation/Deactivation

Activation and deactivation sequencing is handled by built-in circuitry. The activation sequence is initiated by bringing the ENABLE pin HIGH. The activation sequence is outlined below:

1. The RST, CLK and I/O pins are held LOW.
2. V_{CC} is enabled.
3. After V_{CC} is stable at its selected level, The I/O and RST channels are enabled.
4. The clock channel is enabled on the rising edge of the second clock cycle after the I/O pin is enabled.

The deactivation sequence is initiated by bringing the ENABLE pin LOW. The deactivation sequence is outlined below:

1. The reset channel is disabled and RST is brought LOW.
2. The clock channel is disabled and the CLK pin is brought LOW two clock cycles after ENABLE is brought LOW. If the clock is not running, the clock channel will be disabled approximately 9µs after the ENABLE pin is brought LOW.
3. The I/O channel is disabled and the I/O pin is brought LOW approximately 9µs after the ENABLE is brought LOW.
4. V_{CC} will be depowered after the I/O pin is brought LOW.

The activation or deactivation sequences will take place every time a card socket is enabled or disabled.

Fault Protection

The V_{CC}, I/O, RST and CLK pins are all protected against short-circuit faults. While there are no logic outputs to indicate that a fault has occurred, these pins will be able to tolerate the fault condition until it has been removed.

The $V_{CCA,B}$, I/OA,B, and RSTA,B pins possess fault protection circuitry which will limit the current available to the pins. Each V_{CC} pin is capable of supplying approximately 90mA (typ) before the output voltage is reduced.

The CLKA,B pins are designed to tolerate faults by reducing the current drive capability of their output stages. After a fault is detected by the internal fault detection logic, the logic waits for a fault detection delay to elapse before reducing the current drive capability of the output stage.

APPLICATIONS INFORMATION

10kV ESD Protection

All smart card pins (CLKA,B, RSTA,B, I/OA,B, $V_{CCA,B}$ and GND) can withstand over 10kV of human body model ESD in-situ. In order to ensure proper ESD protection, careful board layout is required. The GND pad should be tied directly to a ground plane. The $V_{CCA,B}$ capacitors should be located very close to the $V_{CCA,B}$ pins and tied immediately to the ground plane.

Capacitor Selection

A total of four capacitors are required for proper bypassing of the LTC4557. An input bypass capacitor is required at V_{BATT} and DV_{CC}. Output bypass capacitors are required on each of the smart card $V_{CCA,B}$ pins. Due to their extremely low equivalent series resistance (ESR), only multilayer ceramic chip capacitors should be used to ensure proper stability and ESD protection.

There are several types of ceramic capacitors available each having considerably different characteristics. For example, X7R/X5R ceramic capacitors have excellent voltage and temperature stability but relatively low packing density. Y5V ceramic capacitors have apparently higher packing density but poor performance over their rated voltage or temperature ranges. Under certain voltage and temperature conditions Y5V and X7R/X5R ceramic capacitors can be compared directly by case size rather than specified value for a desired minimum capacitance.

The $V_{CCA,B}$ outputs should be bypassed to GND with a 1µF capacitor. V_{BATT} should be bypassed with a 0.1µF ceramic capacitor. Capacitors should be placed as close to the LTC4557 as possible for improved ESD tolerance.

The following capacitors are recommended for use with the LTC4557:

	TYPE	VALUE	CASE SIZE	MURATA PART NUMBER
C_{VCC}, $V_{CCA/B}$	X5R	1µF	0603	GRM188R60J105KA01
C_{DVCC}, DV_{CC}	X5R	0.1µF	0402	GRM155R61A104KA01

Compliance Testing

Inductance due to long leads on type approval equipment can cause ringing and overshoot that leads to testing problems. Small amounts of capacitance and damping resistors can be included in the application without compromising the normal electrical performance of the LTC4557 or smart card system. Generally a 100Ω resistor and a 20pF capacitor will accomplish this as shown in Figure 2.

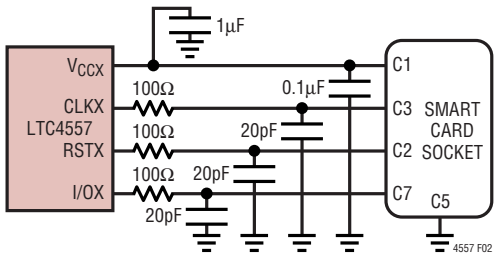


Figure 2. Additional Components for Improved Compliance Testing

APPLICATIONS INFORMATION

Shutdown Modes

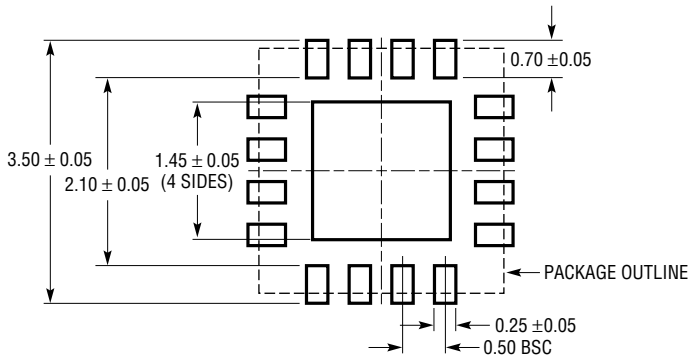
The LTC4557 can enter a low current shutdown mode by one of two methods. First, the ENABLE pin can be brought LOW by the controller to directly shut down the part. The other way is to lower DV_{CC} below 1.2V, at which point the power-on-reset circuit automatically puts the part into shutdown mode.

Ultralow Shutdown Current

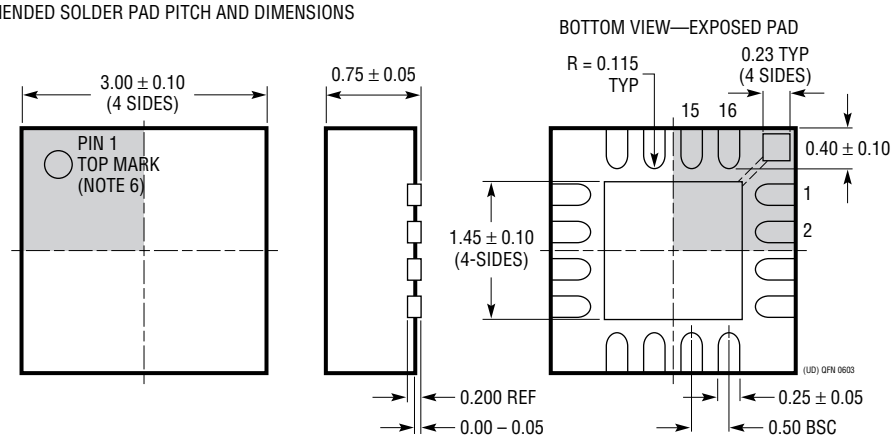
In either of the two shutdown modes, the shutdown current is less than 1μA. For applications that require virtually zero shutdown current, the DV_{CC} pin can be grounded. This will reduce the V_{BATT} current to well under a single microampere.

PACKAGE DESCRIPTION

UD Package
16-Lead Plastic QFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1691)



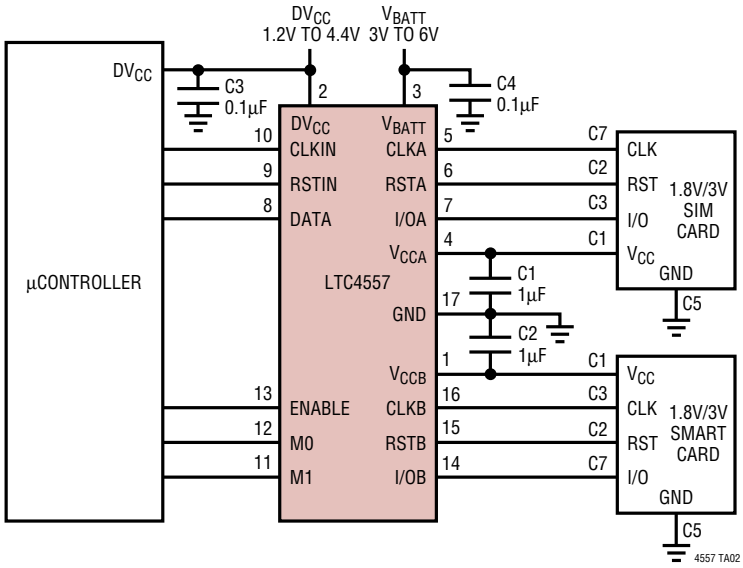
RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



NOTE:
1. DRAWING CONFORMS TO JEDEC PACKAGE OUTLINE MO-220 VARIATION (WEED-2)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

TYPICAL APPLICATION



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1514	50mA, 650kHz, Step-Up/Down Charge Pump with Low-Battery Comparator	V_{IN}: 2.7V to 10V, V_{OUT} = 3V/5V, I_Q = 60µA, I_{SD} = 10µA, SO-8
LTC1515	50mA, 650kHz, Step-Up/Down Charge Pump with Power On Reset	V_{IN}: 2.7V to 10V, V_{OUT} = 3.3V or 5V, I_Q = 60µA, I_{SD} < 1µA, SO-8
LTC1555/LTC1556	SIM Power Supply and Level Translator for 3V/5V SIM Cards	V_{IN}: 2.7V to 10V, V_{OUT} = 3V/5V, Frequency = 650kHz, I_Q = 60µA, I_{SD} < 1µA, SSOP16, SSOP20
LTC1555L	SIM Power Supply and Level Translator for 3V/5V SIM Cards	V_{IN}: 2.6V to 6.6V, V_{OUT} = 3V/5V, Frequency = 1MHz, I_Q = 40µA, I_{SD} < 1µA, SSOP16
LTC1555L-1.8	SIM Power Supply and Level Translator for 1.8V/3V/5V SIM Cards	V_{IN}: 2.6V to 6.6V, V_{OUT} = 1.8V/3V/5V, Frequency = 1MHz, I_Q = 32µA, I_{SD} < 1µA, SSOP16
LTC1755/LTC1756	Smart Card Interface with Serial Control for 3V/5V Smart Card Applications	V_{IN}: 2.7V to 7V, V_{OUT} = 3V/5V, I_Q = 60µA, I_{SD} < 1µA, SSOP16, SSOP24
LTC1955	Dual Smart Card Interface with Serial Control for 1.8V/3V/5V Smart Card Applications	V_{IN}: 3V to 6V, V_{OUT} = 1.8V/3V, I_Q = 200µA, I_{SD} < 1µA, QFN32
LTC1986	SIM Power Supply for 3V/5V SIM Cards	V_{IN}: 2.6V to 4.4V, V_{OUT} = 3V/5V, Frequency = 900kHz, I_Q = 14µA, I_{SD} < 1µA, ThinSOT
LTC3250-1.5	250mA, 1.5MHz, High Efficiency Step-Down Charge Pump	85% Efficiency, V_{IN}: 3.1V to 5.5V, V_{OUT} = 1.2V/1.5V, I_Q = 35µA, I_{SD} < 1µA, ThinSOT
LTC3251	500mA, 1MHz to 16MHz, Spread Spectrum Step-Down Charge Pump	85% Efficiency, V_{IN}: 3.1V to 5.5V, V_{OUT}: 0.9V to 1.6V, 1.2V/1.5V, I_Q = 9µA, I_{SD} < 1µA, MS10
LTC4555	SIM Power Supply and Level Translator for 1.8V/3V SIM Cards	V_{IN}: 3V to 6V, V_{OUT} = 1.8V/3V, I_Q = 40µA, I_{SD} < 1µA, QFN16
LTC4556	Smart Card Interface with Serial Control for 1.8V/3V/5V	V_{IN}: 2.7V to 5.5V, V_{OUT} = 1.8V/3V/5V, I_Q = 250µA, I_{SD} < 1µA, QFN24

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