Dual 4A Ideal Diodes with Adjustable Current Limit

FEATURES

- **Dual 50mΩ Monolithic Ideal Diodes**
- **1.7V to 5.5V Operating Range**
- **Up to 4A Adjustable Current Limit for Each Diode**
- **Low Reverse Leakage Current (1µA Max)**
- **15mV Forward Drop in Regulation**
- **Smooth Switchover in Diode ORing**
- Load Current Monitor
- Precision Enable Thresholds to Set Switchover
- Soft-Start to Limit Inrush Current on Start-Up
- Status Pins to Indicate Forward Diode Conduction
- Current and Thermal Limit with Warning
- Thermally Enhanced 16-Lead MSOP and DFN (3mm × 5mm) Packages

APPLICATIONS

- High Current PowerPath™ Switch
- Battery and Wall Adapter Diode ORing
- Backup Battery Diode ORing
- Logic Controlled High Current Power Switch
- Supercapacitor ORing
- Multiple Battery Sharing

DESCRIPTION

The LTC®4415 contains two monolithic PowerPath ideal diodes, each capable of supplying up to 4A with typical forward conduction resistance of 50mΩ. The diode voltage drops are regulated to 15mV during forward conduction at low currents, extending the power supply operating range and ensuring no oscillations during supply switchover. Less than 1µA of reverse current flows from OUT to IN making this device well suited for power supply ORing applications.

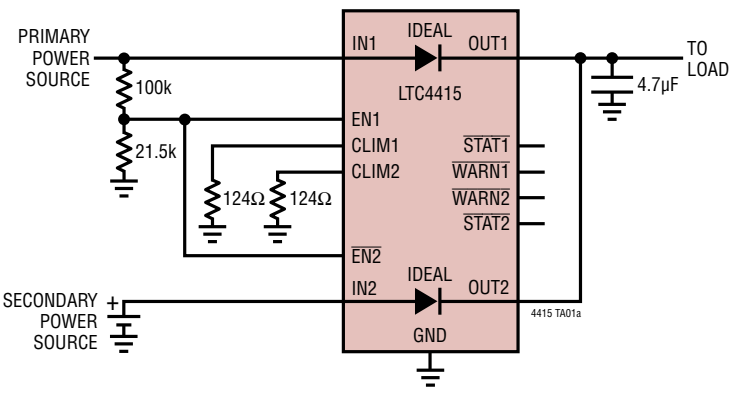
The two ideal diodes are independently enabled and prioritized using inputs EN1 and $\overline{EN2}$. The output current limits can be adjusted independently from 0.5A to 4A using resistors on the CLIM pins. Furthermore, the ideal diode currents can be monitored via CLIM pin voltages.

Open-drain status pins indicate when the ideal diodes are forward conducting. When the die temperature approaches thermal shutdown, or if the output load exceeds the current limit threshold, the corresponding warning pins are pulled low.

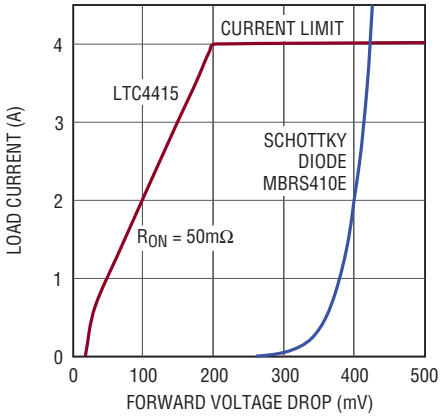
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TYPICAL APPLICATION

Prioritized Power Supply ORing



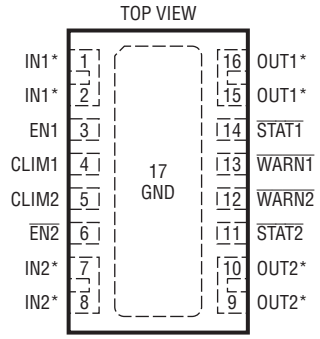
Forward Characteristics of LTC4415 vs MBRS410E Schottky



ABSOLUTE MAXIMUM RATINGS (Note 1)

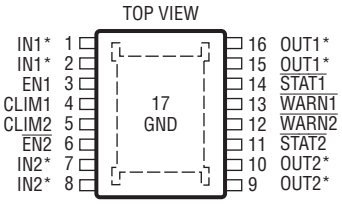
IN1, IN2, OUT1, OUT2, CLIM1, CLIM2, $\overline{STAT1}$, $\overline{STAT2}$, $\overline{WARN1}$, $\overline{WARN2}$ Voltage ..... –0.3V to 6V
EN1, $\overline{EN2}$ Voltage ..... –0.3V to Max (V_{INx}, V_{OUTx})
Operating Junction Temperature Range
(Notes 3, 4) ..... –40°C to 125°C
Storage Temperature Range ..... –65°C to 150°C
Peak Reflow Temperature ..... 260°C

PIN CONFIGURATION



DHC PACKAGE
VARIATION A
16-LEAD (5mm × 3mm) PLASTIC DFN

T_{JMAX} = 125°C, θ_{JA} = 43°C/W
EXPOSED PAD (PIN 17) IS GND, MUST BE SOLDERED TO PCB
*ADJACENT PINS ON THE FOUR CORNERS ARE FUSED TOGETHER



MSE PACKAGE
16-LEAD PLASTIC MSOP

T_{JMAX} = 125°C, θ_{JA} = 35°C/W TO 40°C/W
EXPOSED PAD (PIN 17) IS GND, MUST BE SOLDERED TO PCB
*ADJACENT PINS ON THE FOUR CORNERS ARE FUSED TOGETHER INTERNALLY.

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC4415EDHC#PBF	LTC4415EDHC#TRPBF	4415	16-Lead (5mm × 3mm) Plastic DFN	–40°C to 125°C
LTC4415IDHC#PBF	LTC4415IDHC#TRPBF	4415	16-Lead (5mm × 3mm) Plastic DFN	–40°C to 125°C
LTC4415EMSE#PBF	LTC4415EMSE#TRPBF	4415	16-Lead Plastic MSOP	–40°C to 125°C
LTC4415IMSE#PBF	LTC4415IMSE#TRPBF	4415	16-Lead Plastic MSOP	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C (Notes 2, 3). V_{IN1} = V_{IN2} = 3.6V, R_{CLIM} = 250Ω, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN1}, V_{OUT1}, V_{IN2}, V_{OUT2}	Operating Supply Range	At Least One Input/Output Must Be in This Range	●	1.7		5.5	V
V_{UVLO}	Undervoltage Lockout	V_{INx} Rising Hysteresis	●		1.63 55	1.7	V mV
I_{QF}	Quiescent Current In Forward Regulation (Note 5)	V_{IN1} = V_{EN1} = $V_{\overline{EN2}}$ = 3.6V, I_{OUT1} = –1mA, V_{IN2} = V_{OUT2} = 0V, Measured Through GND Pin	●		44	80	µA
I_{QOFF}	Quiescent Current In Shutdown	V_{IN1} = V_{IN2} = $V_{\overline{EN2}}$ = 3.6V, V_{EN1} = 0V, V_{OUT1} = V_{OUT2} = 0V, Measured Through GND Pin	●		13	28	µA
$I_{QR(OUT)}$	Reverse Turn-Off Current: OUT1 OUT2	V_{IN1} = 3.6V, V_{OUT1} = 3.7V, V_{IN2} = 3.5V, V_{OUT2} = 3.6V (V_{OUT1} > V_{OUT2})	● ●		18 5	40 11	µA µA
$I_{QR(IN)}$	INx Pin Current In Reverse Turn-Off	V_{OUT1} = V_{OUT2} = 5.5V	●		4	10	µA
$I_{LEAK(IN)}$	INx Pin Leakage Current	V_{IN1} = V_{IN2} = 0V, V_{OUT1} = V_{OUT2} = 5.5V		–1		1	µA
V_{FR}	Forward Regulation Voltage (V_{INx} – V_{OUTx})	I_{OUTx} = –1mA	●	5	15	25	mV
V_{RTO}	Reverse Turn-Off Voltage (V_{INx} – V_{OUTx})		●	–50	–30	–10	mV
R_{FR}	Forward Dynamic Resistance in Regulation	I_{OUTx} = –100mA to –300mA			18	30	mΩ
R_{ON}	On-Resistance in Constant Resistance Mode	I_{OUTx} = –1A			50	70	mΩ
t_{ON}	PowerPath Turn-On Time (Notes 6, 7)	Before Enable V_{OUT1} = 1.5V, Diode 1 Before Enable V_{OUT2} = 1.5V, Diode 2 Before Enable V_{OUTx} = 0V			10 23 250		µs µs µs
$t_{ON(SD)}$	PowerPath Turn-On from Shutdown (Note 7)	Both Diodes Disabled and V_{OUTx} = 1.5V Before Enable Both Diodes Disabled and V_{OUTx} = 0V Before Enable			70 320		µs µs
t_{SWITCH}	PowerPath Switchover Time	V_{INx} ↑ (2.6V to 4.6V) to V_{OUTx} Starts Rising, Both Diodes Enabled, OUT1 and OUT2 Tied Together			9		µs
t_{OFF}	PowerPath Turn-Off Time	Disable to I_{IN} Falling from 100mA to 1mA			2		µs
t_{SS}	Soft-Start Duration (Note 8)	V_{OUTx} = 0V			2		ms
Current Monitor							
	Current Monitor Ratio	I_{CLIMx}/I_{OUTx} When I_{OUTx} = –4A I_{CLIMx}/I_{OUTx} When I_{OUTx} = –2A		0.9 0.8	1 1	1.1 1.2	mA/A mA/A
Current Limit							
V_{CLIM}	CLIM Clamp Voltage	In Current Limit			0.5		V
$I_{LIM(ADJ)}$	Current Limit Adjustability		●	0.5		4	A
	Accuracy of Adjustable Current Limit Threshold	V_{OUTx} = V_{INx} – 0.5V, Current Limit = 4A V_{OUTx} = V_{INx} – 0.5V, Current Limit = 2A	● ●			±8 ±15	% %
$I_{LIM(INT)}$	Internal Current Limit	R_{CLIMx} = 0Ω, V_{OUTx} = 0V	●	4	6	9	A
T_{WARN}	Thermal Warning Threshold	Rising Temperature Hysteresis			130 15		°C °C
T_{SD}	Thermal Shutdown Threshold	Rising Temperature Hysteresis			160 20		°C °C
Open-Drain Status Outputs ($\overline{STAT1}$, $\overline{WARN1}$, $\overline{STAT2}$, $\overline{WARN2}$)							
V_{OL}	Open-Drain Output Low Voltage	Current Into Open-Drain Output = 3mA	●		0.05	0.4	V
	Open-Drain Output High Leakage Current	Open-Drain Output Voltage = 5.5V	●		0	1	µA
$t_{STAT(ON)}$	$\overline{STAT}$ Turn-On Time (Note 6)	$\overline{EN1}$ Rising to $\overline{STAT1}$ Pull-Down $\overline{EN2}$ Falling to $\overline{STAT2}$ Pull-Down			5 18		µs µs

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C (Notes 2, 3). V_{IN1} = V_{IN2} = 3.6V, R_{CLIM} = 250Ω, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$t_{STAT(OFF)}$	$\overline{STAT}$ Turn-Off Time	Disable to $\overline{STAT}$ Pull-Up			2		µs
$t_{WARN(ON)}$	$\overline{WARN}$ Turn-On Time	Current Limit to $\overline{WARN}$ Pull-Down			500		µs
$t_{WARN(OFF)}$	$\overline{WARN}$ Turn-Off Time	Out of Current Limit to $\overline{WARN}$ Pull-Up			5		µs
Enable Inputs (EN1, $\overline{EN2}$)							
V_{ENTH}	EN1 Rising and $\overline{EN2}$ Falling Thresholds		●	760	800	840	mV
V_{ENHYST}	EN1 and $\overline{EN2}$ Hysteresis				55		mV
	Enable Pin Current When Pulled High	V_{EN1} = $V_{\overline{EN2}}$ = 3.6V	●		0	1	µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Unless otherwise specified, current into a pin is positive and current out of a pin is negative.

Note 3: The LTC4415 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC4415E is guaranteed to meet performance specifications from 0°C to 85°C. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC4415I is guaranteed over the full –40°C to 125°C operating junction temperature range.

The junction temperature (T_J in °C) is calculated from the ambient temperature (T_A in °C) and power dissipation (P_D in Watts) according to the formula:

$$T_J = T_A + (P_D \bullet \theta_{JA})$$

Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors.

Note 4: The LTC4415 includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

Note 5: One channel enabled. Quiescent current is identical for each channel.

Note 6: Enable inputs are driven to supply levels. Other diode is already enabled so the chip bias circuits are active.

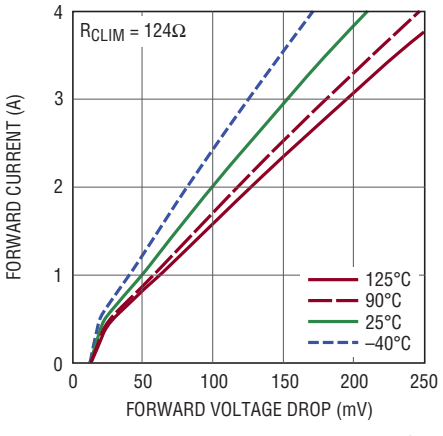
Note 7: Turn-on time is measured from enable to I_{OUTx} rising through 1mA. When the output voltage is more than 1.2V, soft-start is disabled and turn-on is faster.

Note 8: Current ramps from zero to the current limit during the soft-start duration. Soft-start is measured from 10% to 90% of the current limit. If the load condition is such that the current does not need to go up to the current limit during start-up, the output voltage may reach steady state sooner.

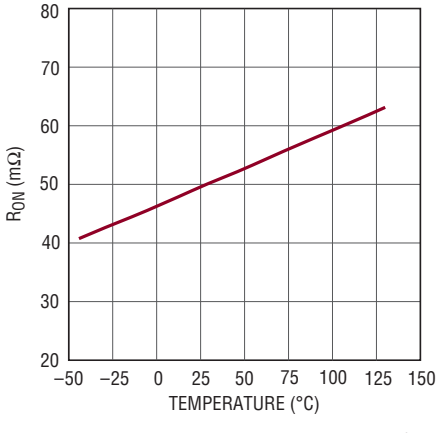
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{IN1} = V_{IN2} = 3.6V, R_{CLIM} = 250Ω unless otherwise noted.

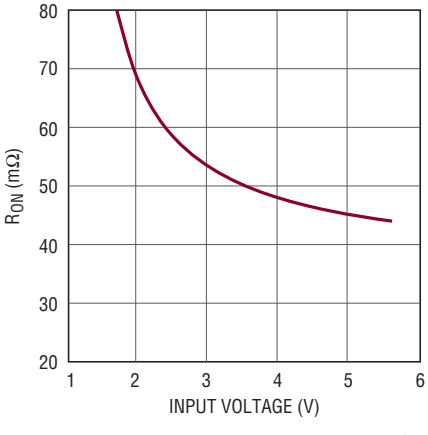
I-V Characteristics



On-Resistance vs Temperature



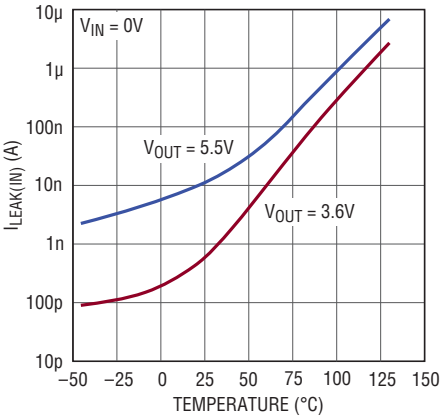
On-Resistance vs V_{IN}



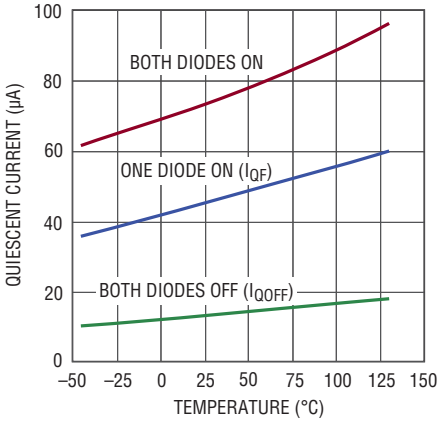
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{IN1} = V_{IN2} = 3.6V, R_{CLIM} = 250Ω unless otherwise noted.

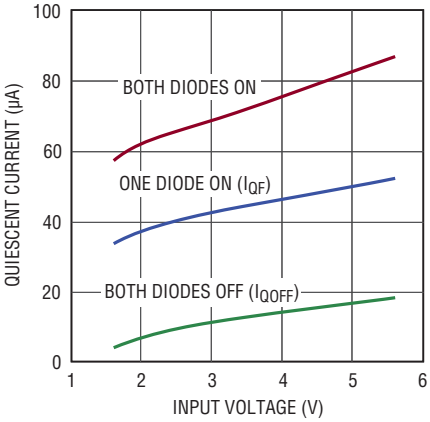
Reverse Leakage Current vs Temperature



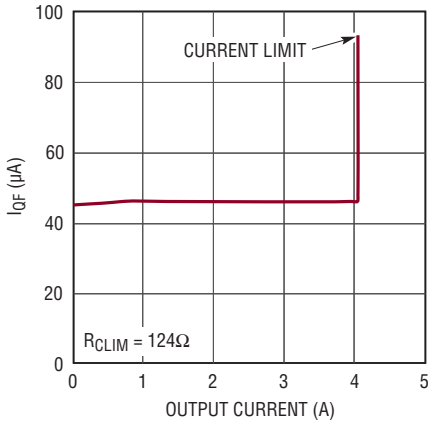
Quiescent Current vs Temperature



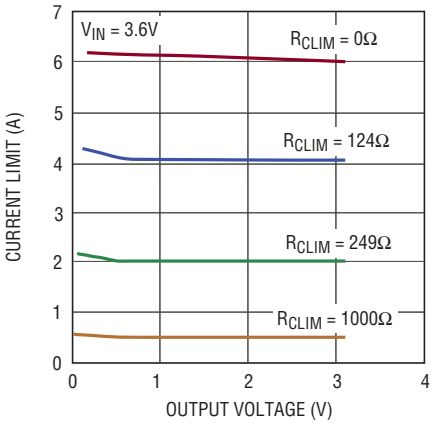
Quiescent Current vs V_{IN}



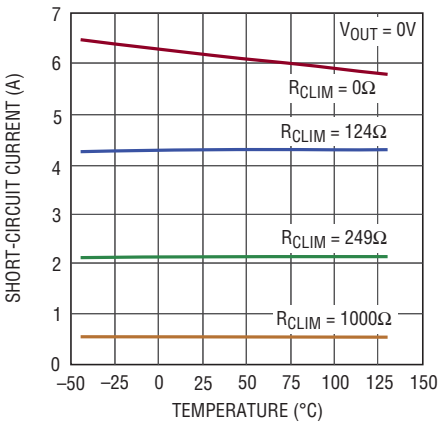
Quiescent Current vs Output Current



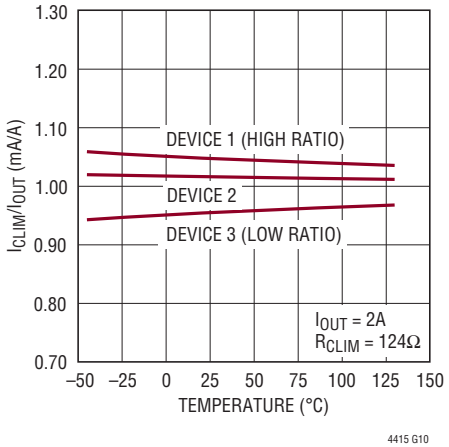
Current Limit vs Output Voltage



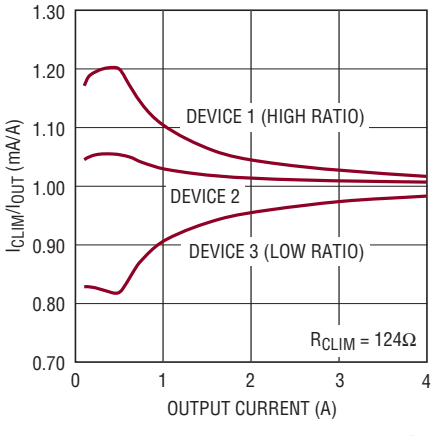
Short-Circuit Current vs Temperature



Current Monitor Ratio vs Temperature



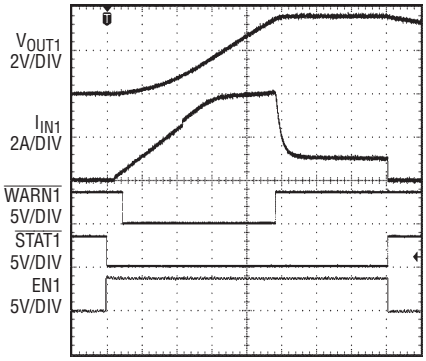
Current Monitor Ratio vs I_{OUT}



TYPICAL PERFORMANCE CHARACTERISTICS

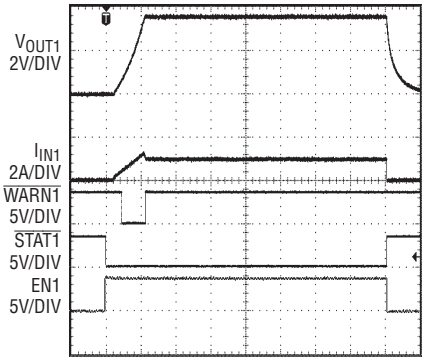
T_A = 25°C, V_{IN1} = V_{IN2} = 3.6V, R_{CLIM} = 250Ω unless otherwise noted.

Enable and Disable Response for Large Load Capacitor



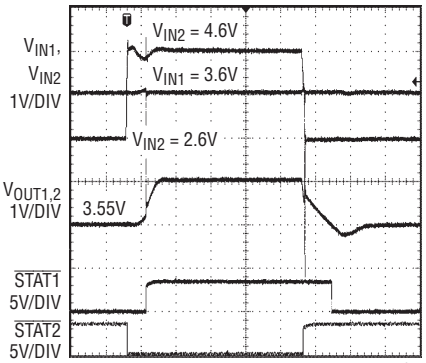
C_{OUT1} = 1200µF 1ms/DIV
R_{LOAD1} = 8Ω

Enable and Disable Response for Small Load Capacitor



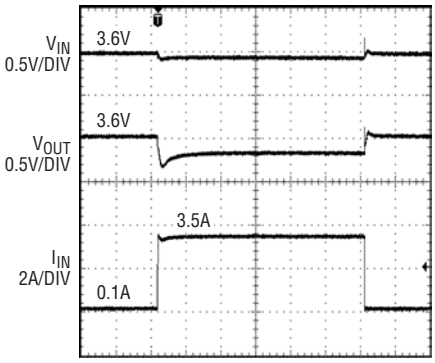
C_{OUT1} = 47µF 1ms/DIV
R_{LOAD1} = 8Ω

Switchover in Diode-OR Application



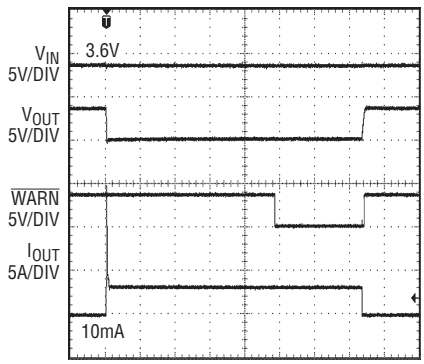
C_{OUT} = 47µF 20µs/DIV
R_{LOAD} = 3.6Ω
V_{OUT1} = V_{OUT2} (SHORTED)

Load Step Response



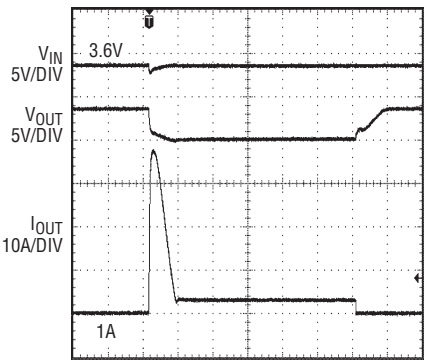
C_{OUT} = 47µF 40µs/DIV
R_{LOAD} = 8Ω
R_{CLIM} = 124Ω

Short-Circuit Response



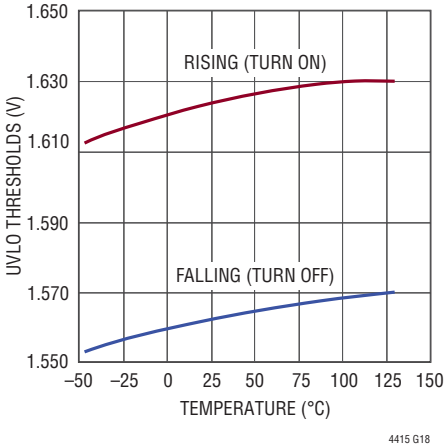
C_{OUT} = 4.7µF 100µs/DIV
R_{CLIM} = 167Ω

Short-Circuit Response at Heavy Load

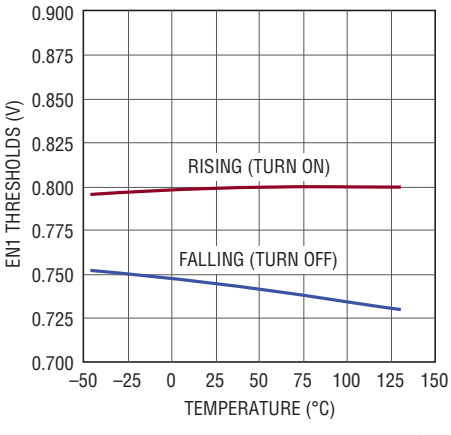


C_{OUT} = 4.7µF 40µs/DIV
R_{CLIM} = 167Ω

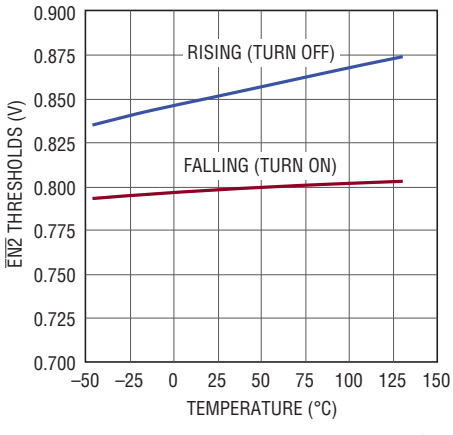
UVLO Thresholds vs Temperature



EN1 Thresholds vs Temperature



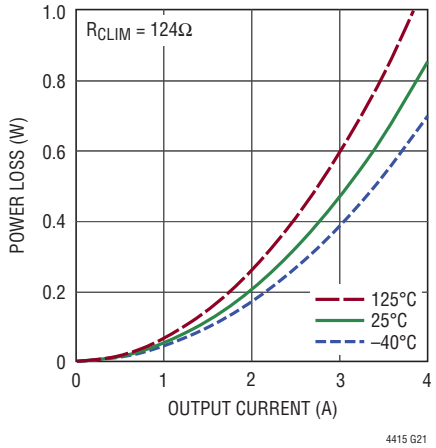
$\overline{EN2}$ Thresholds vs Temperature



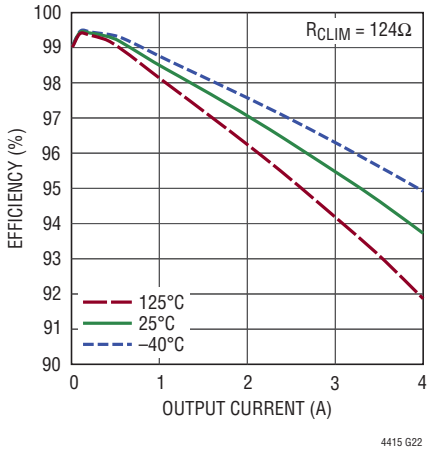
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{IN1} = V_{IN2} = 3.6V, R_{CLIM} = 250Ω unless otherwise noted.

Power Loss vs Output Current



Efficiency vs Output Current



PIN FUNCTIONS

IN1 (Pins 1, 2): Diode 1 Anode and Positive Power Supply for LTC4415. Bypass IN1 with a ceramic capacitor of at least 4.7µF. Pins 1 and 2 are fused together on the package. These pins can be grounded when not used.

EN1 (Pin 3): Enable Input for Diode 1. A high signal greater than V_{ENTH} enables Diode 1.

CLIM1 (Pin 4): Current Limit Adjust and Monitor Pin for Diode 1. Connect a resistor from CLIM1 to ground to set the current limit; the diode 1 current can then be monitored by measuring the voltage on CLIM1 pin. A fixed 6A internal current limit is active when this pin is shorted to ground. Do not leave this pin open. Minimize stray capacitance on this pin to generally less than 200pF (see Applications Information for more details).

CLIM2 (Pin 5): Current Limit Adjust and Monitor Pin for Diode 2. Connect a resistor from CLIM2 to ground to set the current limit; the diode 2 current can then be monitored by measuring the voltage on CLIM2 pin. A fixed 6A internal current limit is active when this pin is shorted to ground. Do not leave this pin open. Minimize stray capacitance on this pin to generally less than 200pF (see Applications Information for more details).

$\overline{EN2}$ (Pin 6): Enable Input for Diode 2. A low signal less than V_{ENTH} enables Diode 2.

IN2 (Pins 7, 8): Diode 2 Anode and Positive Power Supply for LTC4415. Bypass IN2 with a ceramic capacitor of at least 4.7µF. Pins 7 and 8 are fused together on the package. These pins can be grounded when not used.

OUT2 (Pins 9, 10): Diode 2 Cathode and Output of LTC4415. Bypass OUT2 with a ceramic capacitor of at least 4.7µF. Pins 9 and 10 are fused together on the package. Leave these pins open when not used.

$\overline{STAT2}$ (Pin 11): Status Indicator for Diode 2. Open-drain output pulls down during forward diode conduction. This pin can be left open or grounded when not used.

$\overline{WARN2}$ (Pin 12): Overcurrent and Thermal Warning Indicator for Diode 2. Open-drain output pulls down when diode 2 current exceeds its current limit or die temperature is close to thermal shutdown.

$\overline{WARN1}$ (Pin 13): Overcurrent and Thermal Warning Indicator for Diode 1. Open-drain output pulls down when diode 1 current exceeds its current limit or die temperature is close to thermal shutdown.

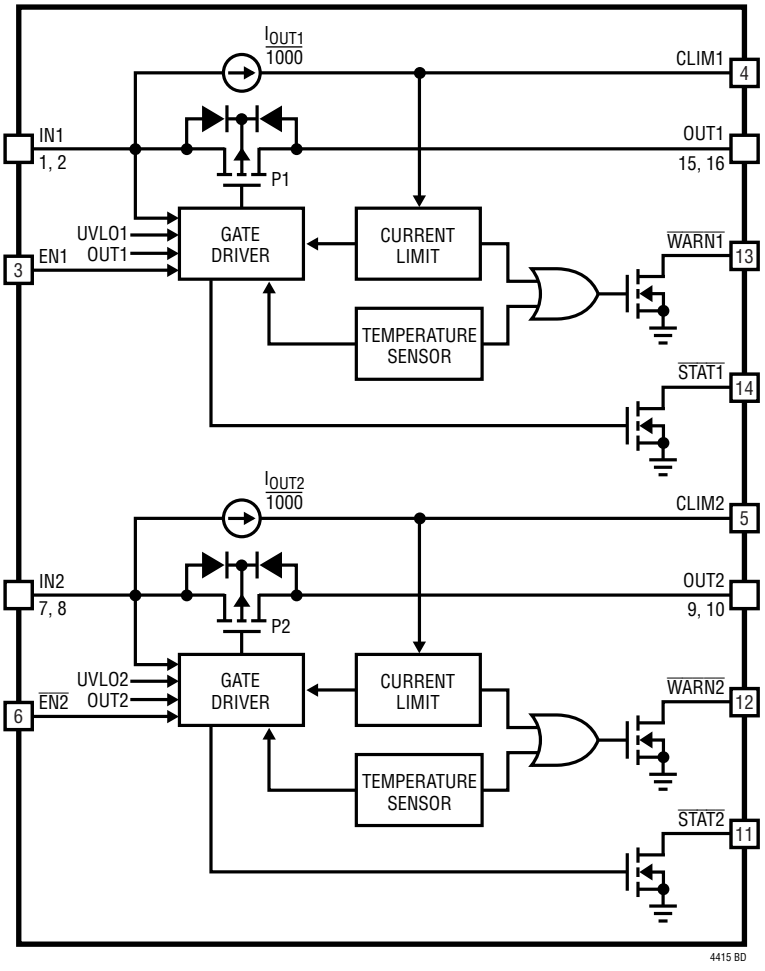
PIN FUNCTIONS

$\overline{\text{STAT1}}$ (Pin 14): Status Indicator for Diode 1. Open-drain output pulls down during forward diode conduction. This pin can be left open or grounded when not used.

OUT1 (Pins 15, 16): Diode 1 Cathode and Output of LTC4415. Bypass OUT1 with a ceramic capacitor of at least 4.7µF. Pins 15 and 16 are fused together on the package. Leave these pins open when not used.

GND (Exposed Pad Pin 17): Device Ground. The exposed pad must be soldered to PCB ground to provide both electrical connection to ground and good thermal conductivity to PCB.

BLOCK DIAGRAM



OPERATION

The LTC4415 consists of two PowerPath ideal diode circuits within a single package. Each diode in the LTC4415 is capable of supplying a maximum rated output current of 4A from its input supply with typical forward conduction resistance of 50mΩ.

The diodes are enabled using level-sensitive enable inputs EN1 and $\overline{EN2}$ with opposite polarity to achieve a prioritizer function with minimal quiescent current during diode-OR implementation. The enable threshold on the enable pins (V_{ENTH}) is 800mV (typical) with one-sided hysteresis of 55mV (typical). For rising voltage on the EN1 pin, Diode 1 is enabled when V_{EN1} > 800mV (typical), and on the falling edge it is disabled when V_{EN1} < 745mV (typical). For falling voltage on the $\overline{EN2}$ pin, Diode 2 is enabled when $V_{\overline{EN2}}$ < 800mV (typical), and on the rising edge it is disabled when V_{EN1} > 855mV (typical). EN1 or $\overline{EN2}$ pin voltages should not exceed the highest voltage on the input (IN1, IN2) or output (OUT1, OUT2) pins.

Forward conduction of the LTC4415 diodes has three operating ranges as a function of the load current, as shown in Figure 1 and described below:

1. For small load current, a low forward voltage drop (V_{FR} = 15mV typical) is maintained by modulating the series resistance offered by the PFETs (P1/P2) in the current paths as shown in the Block Diagram. This operating mode is referred to as constant V_{FR} regulation. In battery-powered and low headroom applications, the low forward drop of the ideal diodes extend the operating range beyond that of Schottky diodes.
2. At higher load currents, the LTC4415 gate driver can no longer modulate the series resistance of the PFETs (P1/P2) to maintain constant forward drop. This transition occurs when the gate voltage of the series PFETs (P1/P2) has been brought down to GND. The ideal diodes subsequently operate with constant resistance, R_{ON}, between inputs and outputs, IN1/IN2 and OUT1/OUT2, respectively.
3. As the load current exceeds the current limit, the series PFETs offer higher resistance between IN1/IN2 and OUT1/OUT2 by reducing the gate drive in order to limit the load current; so the forward voltage drop increases rapidly. This operating mode is referred to as constant current operation.

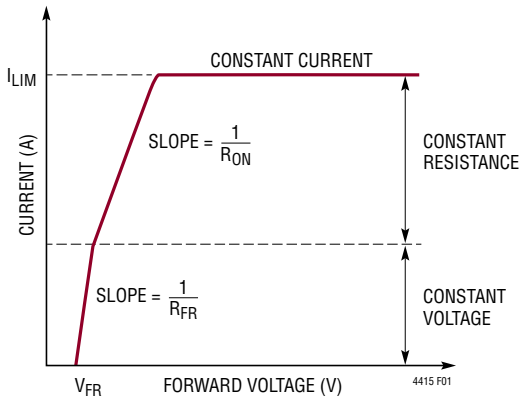


Figure 1. Forward Characteristics of LTC4415

When the output of either diode is driven higher than its input by an alternate supply, conduction through that diode is suspended to prevent reverse conduction from OUT1/OUT2 to IN1/IN2. This function allows implementation of a power supply OR function by simply tying the outputs OUT1 and OUT2 together.

Current Limit Setting

The output current limit of each diode can be set independently by connecting resistors from the current limit adjust pins CLIM1 and CLIM2 to ground. The current out of the CLIM1 and CLIM2 pins are 1/1000 of the ideal diode output currents I_{OUT1} and I_{OUT2} respectively. When the load currents increase so that the CLIM1 or CLIM2 pin voltages exceeds 0.5V, the LTC4415 detects an overcurrent condition and regulates the current to a fixed value. The required value of resistor R_{CLIM} for output current limit of I_{LIM} is calculated as follows:

$$R_{CLIM} = 1000 \bullet \frac{0.5V}{I_{LIM}}$$

The allowed range of R_{CLIM} is 125Ω to 1000Ω unless the CLIM1/CLIM2 pins are shorted to GND, in which case the LTC4415 limits the load current using a fixed internal current limit of 6A.

Overcurrent Status

When either of the ideal diodes is operating in current limit, the corresponding warning pin, $\overline{WARN1}$/$\overline{WARN2}$, is pulled low by an open-drain NFET after a 500µs delay. Normal operation resumes and the warning pin is released

OPERATION

when the load current decreases below the current limit. Power consumption in LTC4415 increases during operation in current limit due to the large voltage drop across the PFET devices (P1 or P2).

Load Current Monitor

The current limit pins output 1/1000th of the ideal diode output current. The voltage across the current limit resistor can be measured to monitor the current through each ideal diode as follows:

$$I_{OUT} = 1000 \bullet \frac{V_{CLIM}}{R_{CLIM}}$$

Note that the current monitor function via V_{CLIM} is not available when CLIM pins are grounded to use the fixed internal current limit.

Soft-Start

An internal soft-start is included for each ideal diode to minimize the start-up inrush current. When either of the diodes start forward conduction, the load current ramps from zero to the set current limit over a period of 2ms. The soft-start can be monitored by observing the CLIM1 and CLIM2 pin voltages when they are connected to grounded resistors. Soft-start duration is reduced to 0.5ms (typical) when the CLIM pins are grounded. In order to minimize output droop during switchover between input sources in power supply ORing applications, soft-start is disabled when the output voltage is above 1.2V.

Forward Conduction Status Monitor

Active low open-drain output status signals, $\overline{STAT1}$ and $\overline{STAT2}$, indicate the forward conduction status of each ideal diode. With resistor pull-ups on these status pins, a low voltage indicates forward conduction from input to output, IN1/IN2 to OUT1/OUT2, respectively. The status pins go to high impedance when the respective ideal diodes are disabled, during reverse turn-off conditions, or during thermal shutdown.

Thermal Warning and Shutdown

Thermal sensors within the LTC4415 monitor the die temperature when either of the diodes are enabled. When the die temperature exceeds the warning threshold (130°C), the $\overline{WARN1}/\overline{WARN2}$ pins are pulled down with open-drain NFETs while the LTC4415 continues to operate normally. This gives some time for the user to reduce the load current to avoid thermal shutdown. The warning signal is deasserted when the die temperature cools down below 115°C.

Thermal shutdown is triggered when the internal die temperature increases beyond the fault threshold (160°C). Status pins, $\overline{STAT1}/\overline{STAT2}$, are deasserted during thermal shutdown to indicate the interruption in forward condition. Normal operation resumes when the die temperature cools below 140°C. Note that prolonged operation at the overtemperature condition degrades device reliability.

Figure 2 shows $\overline{WARN}$ followed by thermal shutdown caused by an output short-circuit to ground. Time to thermal shutdown varies depending on power dissipation, ambient temperature and board layout. The output current ramps up after the device cools down below 140°C, but shuts down repeatedly as the device overheats due to persistent short.

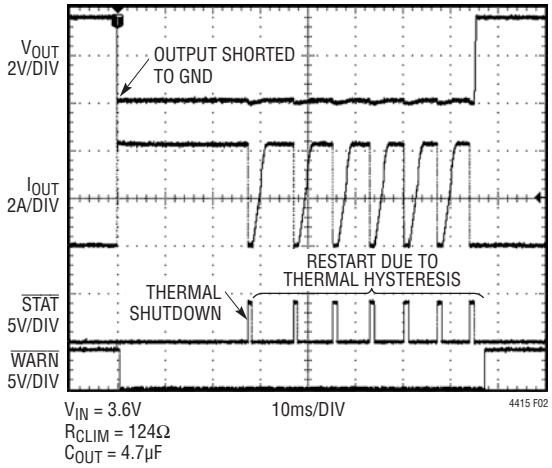


Figure 2. Current Limit Warning and Thermal Shutdown on Output Short Circuit

The thermal sensors are independent for each diode to warn of, or shut down the heat generating path so that it does not hinder the normal operation of the other path. Depending on the amount of heat generated, the whole die may still heat up and eventually shut down the other channel.

OPERATION

Undervoltage Lockout

Each ideal diode contains an independent UVLO control circuit so that one input experiencing undervoltage lockout does not hinder normal operation of the other channel. The diode conduction path is turned off and the status signal, $\overline{STAT1}/\overline{STAT2}$, is deasserted during an undervoltage condition.

APPLICATIONS INFORMATION

Stability Considerations

Any capacitance on the CLIM pins adds a pole to the current control loop. Therefore, stray capacitance on these pins must be kept to a minimum. Although the maximum allowed value of the current limit adjust resistor is 1000Ω, any additional capacitance on these pins reduces the maximum allowed resistance, consequently increasing the minimum allowed current limit. For stable operation, the pole frequency at the CLIM pins should be kept above 800kHz. Therefore, if the CLIM pin parasitic capacitance is C_P, the following equation should be used to calculate the maximum allowed resistor R_{CLIM}:

$$R_{CLIM} \leq \frac{1}{2\pi \bullet 800kHz \bullet C_P}$$

When the voltage at the CLIM pins are monitored using a long cable, such as an oscilloscope probe, decouple the parasitic capacitance of the probe and the monitor system using a series resistor as shown in Figure 3, where a 20k resistor has been added between the CLIM pin and the probe to ensure stable operation.

Input and Output Capacitors

High current transients through parasitic inductance on the input and output sides of the ideal diodes can cause voltage spikes on the IN1/IN2/OUT1/OUT2 pins. These current transients can occur on power plug-in, load disconnect or switching, disable, or even thermal shutdown. Limit inductance and/or increase bypass capacitors to prevent pin voltages from exceeding the absolute maximum rating of 6V. Some ESR in these capacitors may be helpful in dampening the resonances and minimizing the ringing caused by hot plugging or load switching. Refer to Application Note 88, entitled, "Ceramic Input Capacitors Can Cause Overvoltage Transients" for a detailed discussion and mitigation of this phenomenon.

The values of the input and output decoupling capacitors also depends on the maximum allowable droop during switchover in power supply ORing applications. Typical duration for LTC4415 ideal diodes to switchover from reverse turn-off to forward conduction, t_{SWITCH}, is 9µs. Therefore, the minimum decoupling capacitance, C, required for a specified maximum output voltage droop, ΔV, when one of the input voltages drops, can be calculated as follows:

$$C = \frac{I_{LOAD} \bullet t_{SWITCH}}{\Delta V}$$

where I_{LOAD} is the load current at the time of switchover.

For example, the required value of output capacitance for a 100mV maximum droop in the output voltage during quick switchover at 1A load would be 100µF. Note that both supplies share the load during switchover, and therefore reduce the droop, when the voltage on the falling supply pin changes slowly.

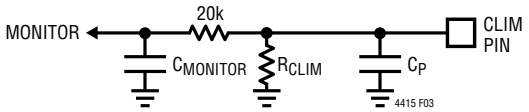


Figure 3. Current Monitor with High Capacitance Probe/Instrument

APPLICATIONS INFORMATION

Board Layout Considerations

When laying out the printed circuit board, the following checklist should be followed to ensure proper operation of the LTC4415:

1. Connect the exposed pad of the package (Pin 17) directly to a large PC board ground to minimize thermal impedance. Correctly soldered to a 2500mm^2 double-sided 1oz copper board, the DFN package has a thermal resistance (θ_{JA}) of approximately 43°C/W. Failure to make good contact between the exposed pad on the backside of the package and an adequately sized ground plane results in much larger thermal resistance, raising the die temperature for given power dissipation. An example layout for double layer board is given in Figure 4. Via holes are used in the board under and near the device to conduct heat away from the device to the bottom layer.
2. The traces to the input supplies, outputs and their decoupling capacitors should be short and wide to minimize the impact of parasitic inductance. Connect the GND side of the capacitors directly to the ground plane of the board. The decoupling capacitors provide the transient current to the internal power MOSFETs and their drivers.
3. Minimize the parasitic capacitance on CLIM1 and CLIM2 pins for stable operation.

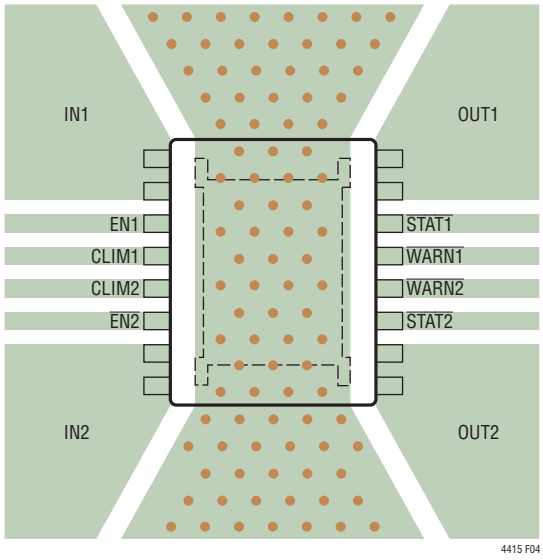


Figure 4. Example Board Layout for a Double-Sided PCB

TYPICAL APPLICATIONS

Precision enable inputs and independent status outputs provide flexibility in power supply back up and load share applications using the two high current ideal diode circuits in the LTC4415, as shown in the following examples. The features shown in these application circuits can be combined in custom applications as needed.

Prioritized Switchover to a Backup Battery

The application circuit, Figure 5, illustrates switchover from a primary power source to backup power at a precise input voltage using the prioritized power supply-OR application circuit. Diode 2 is enabled when the primary power source voltage on diode 1 input falls below the threshold given as follows:

$$V_{IN1} < 0.8V \bullet \left(1 + \frac{R1+R2}{R3}\right)$$

As V_{IN1} falls further, diode 1 is disabled when the primary power source voltage falls below the threshold determined by the resistor divider on enable pin EN1:

$$V_{IN1} < (0.8V - V_{ENHYST}) \bullet \left(1 + \frac{R1}{R2+R3}\right)$$

The built-in hysteresis on the enable pins in the LTC4415 provides some overlap of diode enables around the switchover of power supplies. Resistor R2 can be optionally used for additional overlap between the two supplies. The additional overlap is given by:

$$V_{OVERLAP} \approx V_{ENTH} \bullet \frac{R2}{R3} \text{ when } \frac{R2}{R3} << 1$$

The enable overlap minimizes the load voltage droop during switchover. Both input power supplies provide power to the load during the overlap. The status output pins can be pulled up to the output voltage or to a logic power supply.

Automatic Switchover to a Backup Battery and Keep-Alive Power Source

Figure 6 illustrates an application circuit for automatic switchover to the backup battery if the primary power source voltage falls below the backup battery voltage. The wired-AND of the status outputs is used to drive the gate of a pair of back-to-back connected external NMOS (M1 and M2) when both primary and backup power sources are absent or below UVLO or during thermal shutdown of LTC4415. Under these conditions, the keep-alive source supplies power to critical components of the system. At the same time, the wired-AND status output turns off

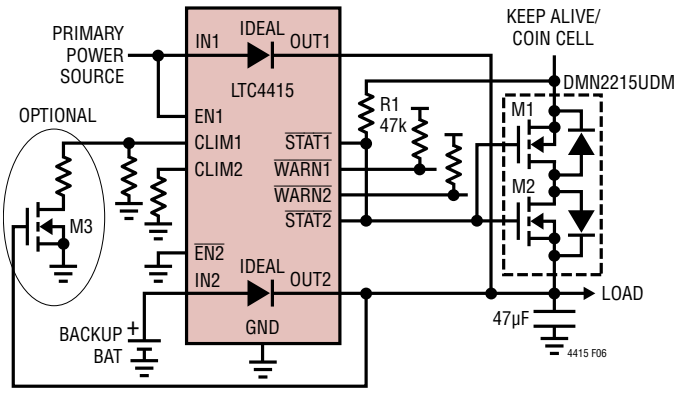


Figure 6. Automatic Switchover to a Backup Battery with Provision for Keep-Alive Power to the Load When Both Are Absent

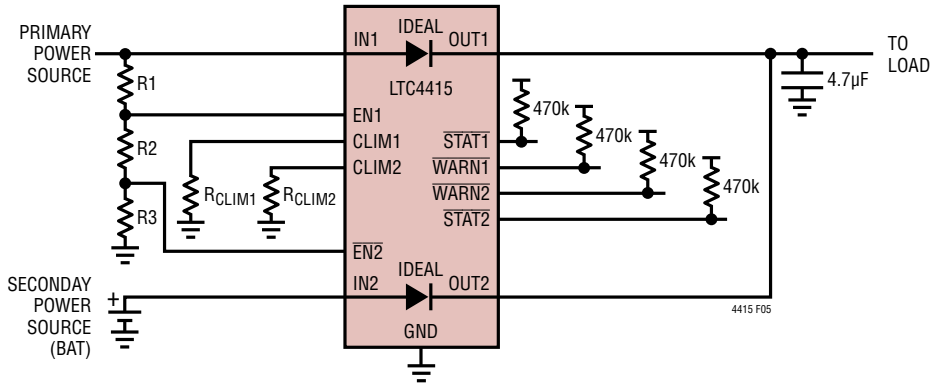


Figure 5. Prioritized Power Supply ORing

TYPICAL APPLICATIONS

non-critical high current loads. If the status resistors are pulled up through the keep-alive power source itself as shown in Figure 6, the output voltage is limited to:

$$V_{OUT} = V_{KEEP_ALIVE} - V_{gs(M1,2)}$$

where $V_{gs(M1,2)}$ is the voltage drop from gate to source of the composite NMOS device (M1 and M2). The pull-up resistor, R1, consumes power from the keep-alive source when the primary or backup sources supply power to the load. The primary power source or backup battery supplies power to the load when either of them are higher than the output voltage.

Current limit on any of the diode power paths can be set to automatically fold back as the output voltage drops (to reduce power consumption), by switching out a resistor on the CLIM pin, as shown in Figure 6 for diode 1. The gate of NMOS M3 can optionally be fed from a resistor divided output voltage to adjust the output voltage threshold of current foldback.

Multiple Battery Charging

Figure 7 illustrates an application circuit for automatic dual battery charging from a single charger. The battery with lower voltage receives larger charging current until both battery voltages are equal, then both are charged. While both batteries are charging simultaneously, the higher capacity battery gets proportionally higher current from the charger. For Li-Ion batteries, both batteries achieve the charger float voltage minus the forward regulation voltage of 15mV. This concept can be extended to more than two batteries using additional LTC4415. The $\overline{STAT1}$, $\overline{STAT2}$ pins provide information as to when the batteries are being charged. For intelligent control, the EN1/$\overline{EN2}$ input pins can be used with a microcontroller as shown in Figure 9 later in this section.

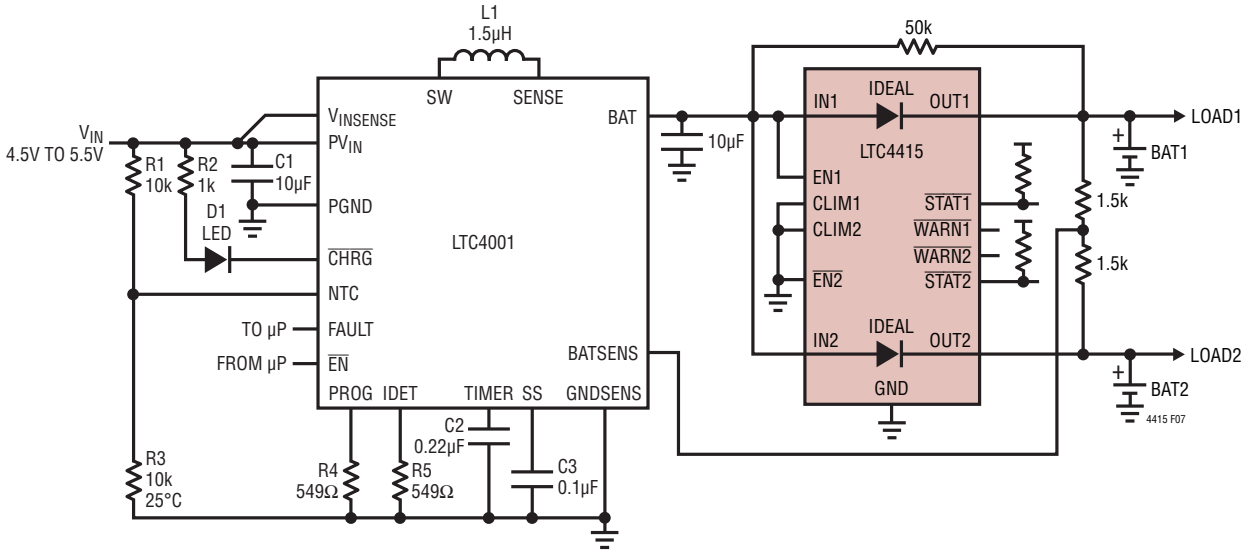


Figure 7. Dual Battery Charging from a Single Charger

TYPICAL APPLICATIONS

Load Sharing by Multiple Batteries and Automatic Switchover to a Preferred Power Supply (Such as a Wall Adapter)

An application circuit for dual battery load sharing with automatic switchover to a wall adapter (when present) is shown in Figure 8. In the absence of the wall adapter, the higher voltage battery provides the load current until it has discharged to the voltage of the other battery. The load is then shared between the two batteries according to their capacities, the higher capacity battery providing proportionally higher current to the load unless limited by its current limit.

When a wall adapter is applied, the output voltage rises as the body diode of PFET MP1 conducts and both of the ideal diode paths in the LTC4415 stop conducting due to reverse turn-off. At this time, the wired-OR status signal pulls up the gate voltage of NFET MN1, pulling down the gate voltage of power PFET MP1, turning it on. The wired-OR status signal indicates whether the wall adapter or either of the two batteries is supplying the load current. The two application circuits described in Figure 7 and Figure 8 can be cascaded for dual battery charging and load sharing.

Microcontrolled Power Switch with Reverse Blocking, Selectable Current Limit, Soft-Start and Monitoring

Figure 9 illustrates an application circuit for microcontroller monitoring and control of two power sources. The microcontroller monitors the input supply voltages and commands the LTC4415 through EN1/$\overline{EN2}$ inputs.

Currents through the ideal diodes are monitored by the microcontroller measuring CLIM1/CLIM2 pin voltages using ADCs. The current limit can be adjusted for either diode using an external FET as shown in this application for diode 1 with MN1. The two ideal diode outputs are connected together for power source ORing, or they may feed different loads.

Parallel Diodes for Lower Resistance or Higher Current Output

The two ideal diodes in the LTC4415 can be connected in parallel as shown in Figure 10 to achieve a low resistance PowerPath. The master enable input, $\overline{ENABLE}$, turns on diode 2. EN1 is tied to the output so that diode 1 conducts only after the output has charged up (by diode 2 according to its current limit setting). Diode 1 is disabled when the

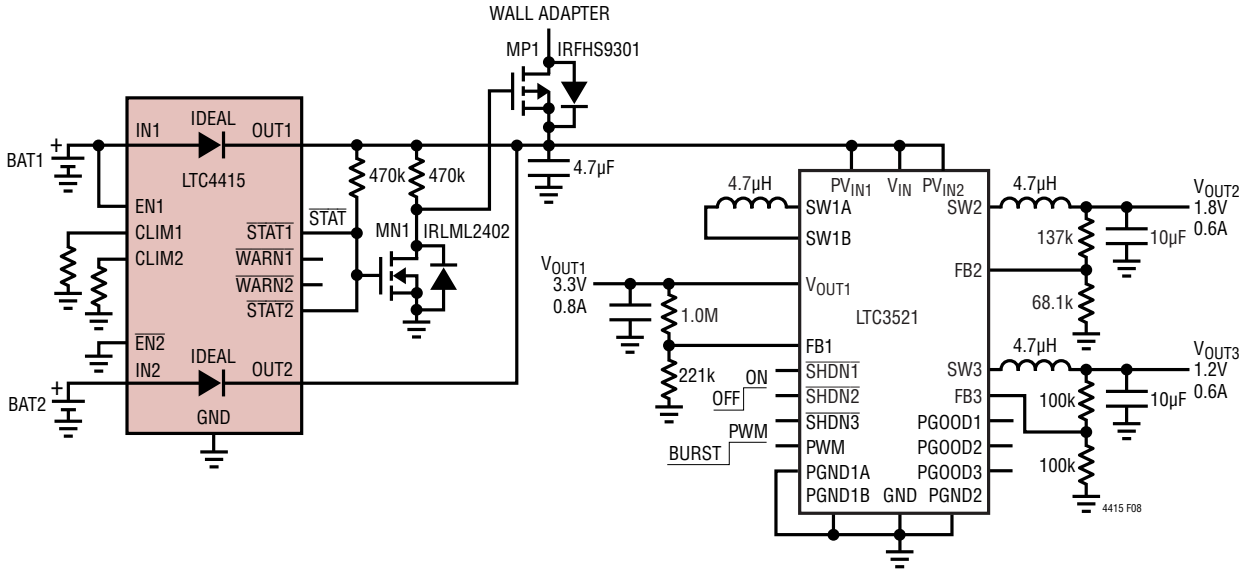


Figure 8. Dual Battery Load Sharing with Automatic Switchover to a Wall Adapter

TYPICAL APPLICATIONS

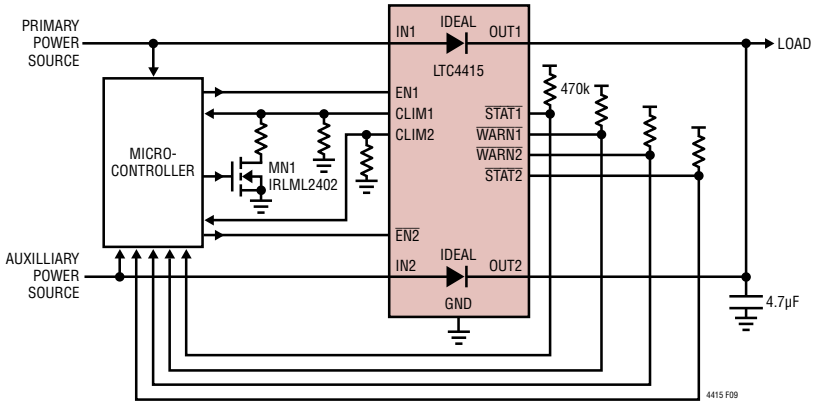


Figure 9. Microcontrolled PowerPath Monitoring and Control

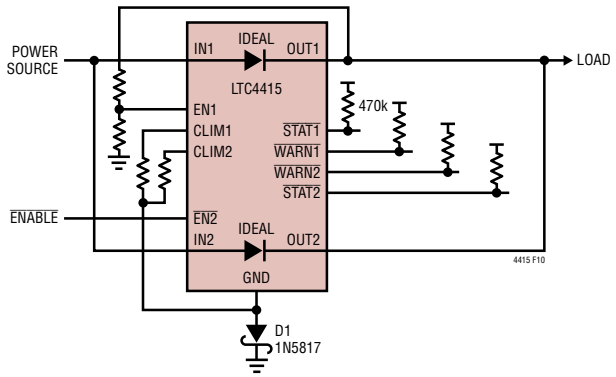


Figure 10. Parallel Diodes with Current Limit Foldback and Reverse Polarity Protection

output falls below a threshold set by the resistor divider on EN1 pin. This arrangement results in current limit foldback, reducing the current limit of the parallel diodes to that of only diode 2 when the output voltage falls, thus controlling power dissipation.

An optional Schottky diode can be inserted in series with the chip ground as shown in Figure 10 to protect LTC4415 against input power source reverse polarity. The presence of the Schottky shifts the UVLO and enable pin thresholds by a voltage equal to the forward voltage drop of the Schottky diode.

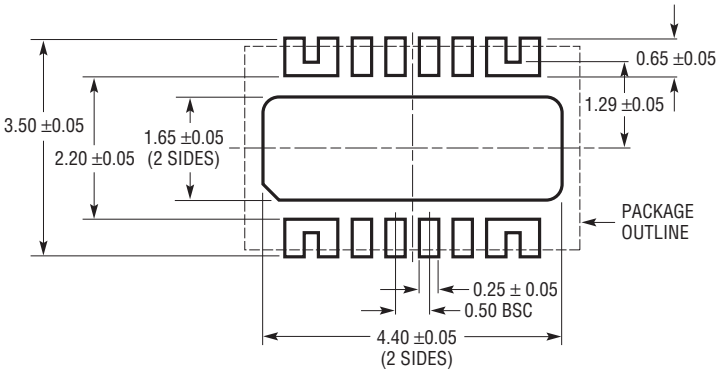
Power Backup Using Supercapacitors and Optional Keep-Alive Cell

An application of dual backup power is shown on the last page of this data sheet. Diode 2 provides power to the triple DC/DC converter (LTC3521) when the primary input power (V_{DD}) is available, possibly from a wall adapter. When the input power falls below the supercapacitor voltage, the supercapcitor provides power to the LTC3521. The supercapacitor charger (LTC3625) provides a power failure comparator output signal ($\overline{PFO}$) when its input voltage falls below a preset voltage defined by the resistive divider on the PFI input. The $\overline{PFO}$ signal is available to start the shutdown of high current applications. When the supercapacitor discharges to a voltage level determined by the resistor divider on EN1 input of LTC4415, the wired-AND status signal of LTC4415 pulls up because neither of the diode paths in LTC4415 are conducting and the coin cell provides power through a back-to-back connected pair of NFETs, M1 and M2. The wired-AND status signal is available to signal that only low current circuits such as real-time clock or memory remain enabled while operating from the coin cell.

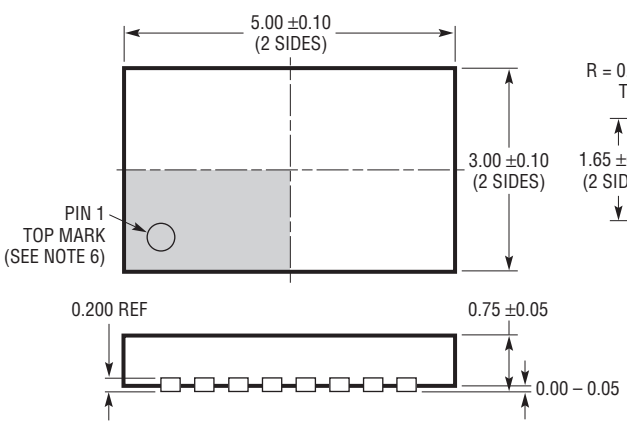
PACKAGE DESCRIPTION

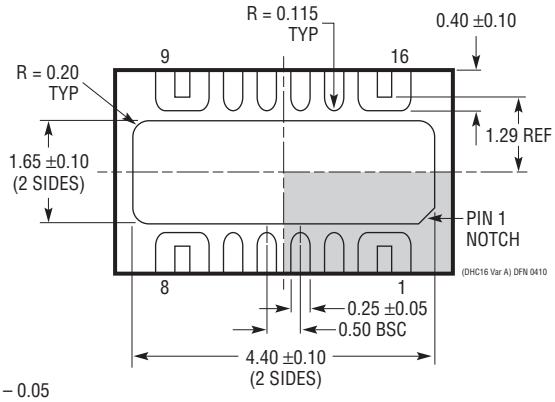
Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

DHC Package
16-Lead Plastic DFN (5mm × 3mm)
(Reference LTC DWG # 05-08-1872 Rev Ø)
Variation A



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS





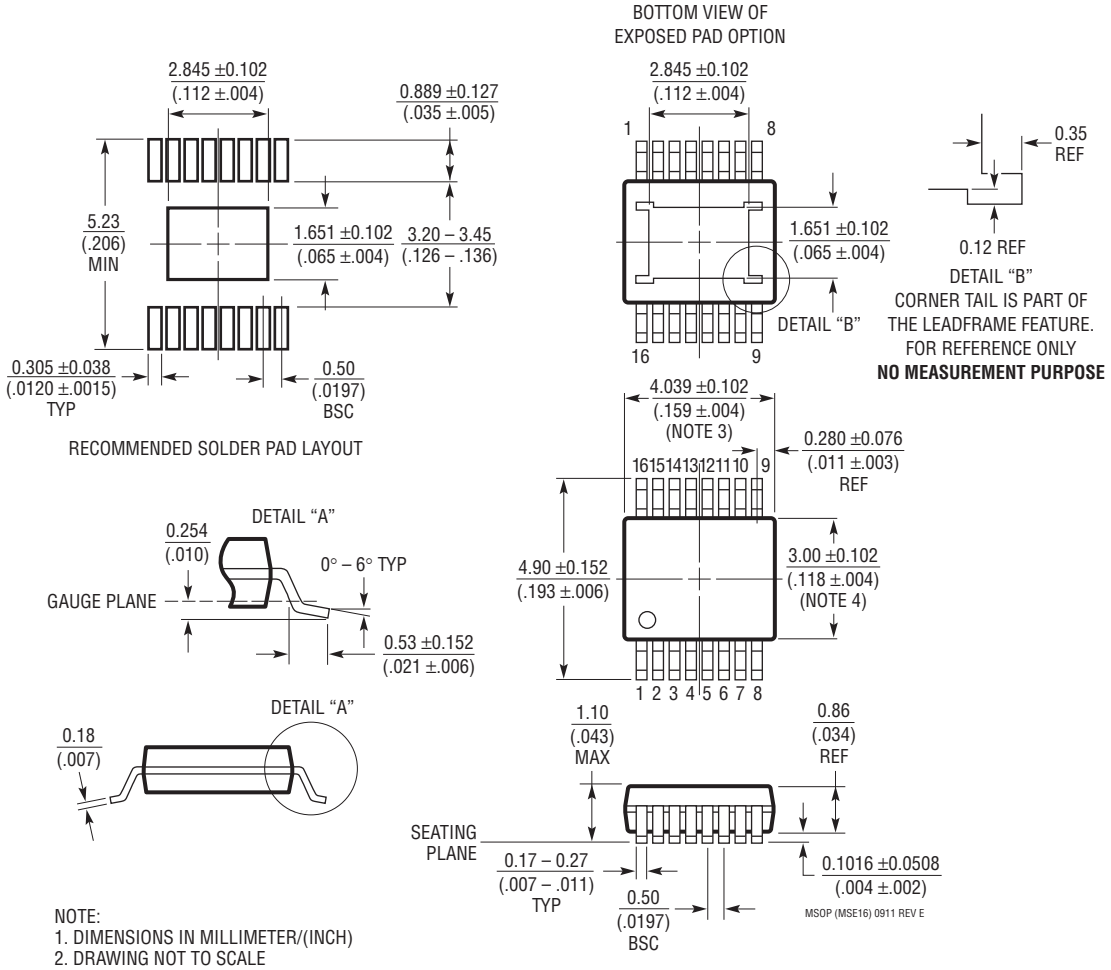
BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING PROPOSED TO BE MADE VARIATION OF VERSION (WJED-1) IN JEDEC PACKAGE OUTLINE MO-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

MSE Package
16-Lead Plastic MSOP, Exposed Die Pad
(Reference LTC DWG # 05-08-1667 Rev E)



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX
6. EXPOSED PAD DIMENSION DOES INCLUDE MOLD FLASH. MOLD FLASH ON E-PAD SHALL
   NOT EXCEED 0.254mm (.010") PER SIDE.

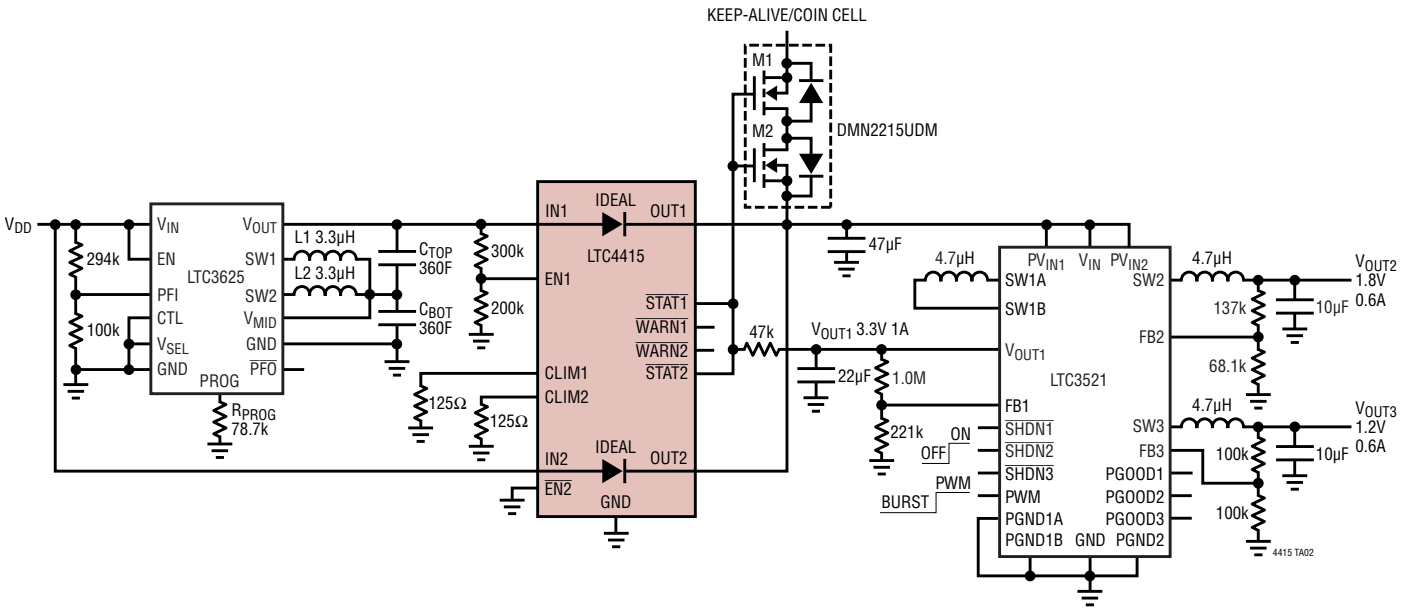
REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	4/12	Clarified footnotes and added new Note 5 for quiescent current	3, 4
		Changed FET MP1 part number on Figure 8	15

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

TYPICAL APPLICATION

Power Backup Using Supercapacitors and Optional Keep-Alive Cell



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC4411	2.6A Low Loss Ideal Diode	Monolithic Low Loss PowerPath, ThinSOT Package
LTC4412	PowerPath Controller	3V to 28V Input Voltage Range, ThinSOT Package
LTC4413-1/ LTC4413-2	Dual 2.6A, 2.5V to 5.5V, Ideal Diodes in 3mm × 3mm DFN	140mΩ On-Resistance, Overvoltage Protection Sensor with Drive Output
LTC4414	36V, Low Loss PowerPath Controller for Large PFETs	Drives Large Q_G PFETs, 3.5V to 36V
LTC4416	36V, Low Loss Dual PowerPath Controllers	Designed to Drive Large and Small Q_G PFETs, 3.5V to 36V
LTC4352	Low Voltage Ideal Diode Controller With Monitoring	Controls Single N-Channel MOSFET, Input Supply Monitors, 2.9V to 18V
LTC4354	Negative High Voltage Diode-OR Controller and Monitor	Controls Two N-Channel MOSFETs, 4.5V to 80V
LTC4355	Positive High Voltage Diode-OR Controller and Monitor	Controls Two N-Channel MOSFETs, 9V to 80V
LTC4357	Positive High Voltage Ideal Diode Controller	Controls Single N-Channel MOSFET, 9V to 80V
LTC4358	5A Monolithic Ideal Diode	20mΩ N-Channel MOSFET, 9V to 26.5V
LTC4066	USB Power Controller and Li-Ion Linear Charger with Low Loss Ideal Diode	Seamless Transition Between Input Power Sources: Li-Ion Battery, USB and 5V Wall Adapter
LTC4425	Linear Supercapacitor Charger with Current-Limited Ideal Diode and V/I Monitor	50mΩ On-Resistance, 2.7V to 5.5V, Programmable Current Limit, Programmable Output Voltage Mode
LTC2952	Pushbutton Ideal Diode PowerPath Controller with Supervisor	Controls Two P-Channel MOSFETs, 2.7V to 28V

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408) 432-1900 • FAX: (408) 434-0507 • www.linear.com
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