Dual I²C/SMBus Address Translator

FEATURES

- **Allows Multiple Slaves with the Same Address to Coexist on the Same Bus**
- **Resistor Configurable Address Translation**
- **No Software Programming Required**
- Compatible with SMBus, I²C and I²C Fast Mode
- Pass-Through Mode Allows General Call Addressing
- ±4kV HBM ESD Ruggedness
- Level Translation for 2.5V, 3.3V and 5V Buses
- Stuck Bus Timeout
- Prevents SDA and SCL Corruption During Live Board Insertion and Removal
- Support Bus Hot Swap
- 20-Lead QFN 4mm × 4mm Package

APPLICATIONS

- I²C, SMBus Address Expansion
- Address Translation
- Servers
- Telecom

DESCRIPTION

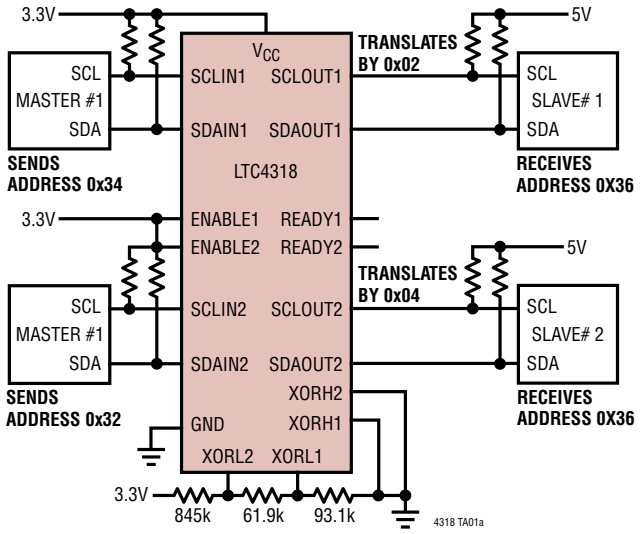
The LTC®4318 enables the hardwired address of one or more I²C or SMBus slave devices to be translated to a different address. This allows slaves with the same hard-wired address to coexist on the same bus. Only discrete resistors are needed to select the new address and no software programming is required. Up to 127 different address translations are available.

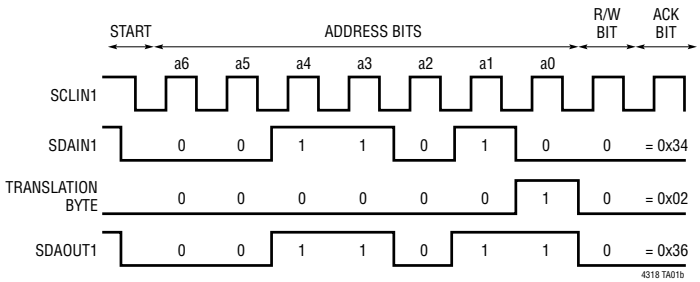
The LTC4318 incorporates a pass-through mode which disables the address translations and allows general call addressing by the master. The LTC4318 is designed to automatically recover from abnormal bus conditions like bus stuck low or premature STOP bits.

PART NUMBER	NUMBER OF INPUT CHANNELS	NUMBER OF OUTPUT CHANNELS
LTC4316	1	1
LTC4317	1	2
LTC4318	2	2

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TYPICAL APPLICATION



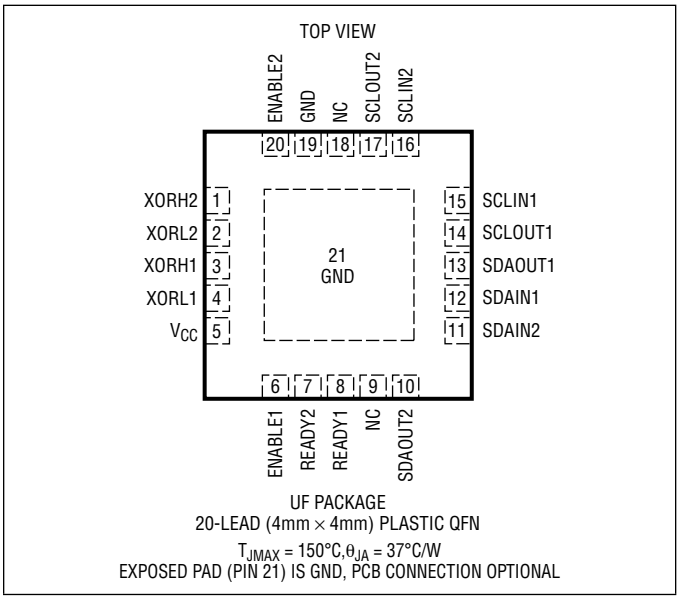


ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

Input Supply Voltage V_{CC} ..... –0.3V to 6V
Input Voltages
ENABLEn..... –0.3V to 6V
XORLn, XORHn .....–0.3V to V_{CC} + 0.3V
Output Voltages
READYn ..... –0.3V to 6V
Output Currents
READYn, SDAOUTn.....50mA
Input/Output Voltages
SCLINn, SCLOUTn, SDAINn, SDAOUTn ..... –0.3V to 6V
Operating Temperature Range
LTC4318C ..... 0°C to 70°C
LTC4318I ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



UF PACKAGE
20-LEAD (4mm × 4mm) PLASTIC QFN
T_{JMAX} = 150°C, θ_{JA} = 37°C/W
EXPOSED PAD (PIN 21) IS GND, PCB CONNECTION OPTIONAL

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC4318CUF#PBF	LTC4318CUF#TRPBF	4318	20-Lead (4mm × 4mm) Plastic QFN	0°C to 70°C
LTC4318IUF#PBF	LTC4318IUF#TRPBF	4318	20-Lead (4mm × 4mm) Plastic QFN	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 3.3V, unless otherwise specified.

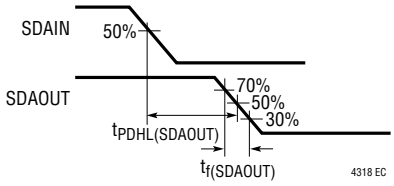
SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Supply							
V_{CC}	Input Supply Range		●	2.25		5.5	V
I_{CC}	Input Supply Current	ENABLE = 3.3V, SCLIN = SDAIN = 0V	●		0.8	2	mA
		ENABLE = 0V, SCLIN = SDAIN = 0V	●		350	800	µA
$V_{CC(UVLO)}$	V_{CC} Supply Undervoltage Lockout	V_{CC} Rising	●	1.9	2.1	2.2	V
$V_{CC(HYST)}$	V_{CC} Supply Undervoltage Lockout Hysteresis				100		mV
ENABLE and READY							
$V_{ENABLE(TH)}$	ENABLE Threshold Voltage	Enable Rising	●	1	1.4	1.8	V
$V_{ENABLE(HYST)}$	ENABLE Hysteresis				50		mV
$I_{ENABLE(LEAK)}$	ENABLE Input Current		●			±1	µA
$V_{READY(OL)}$	READY Output Low Voltage	I = 3mA	●			0.4	V
$I_{READY(OH)}$	READY Off Leakage Current	V_{CC} = V_{READY} = 5.5V	●			±5	µA
SCLIN, SDAIN, SCLOUT, SDAOUT							
$V_{SCL,SDA(TH)}$	Threshold Voltage	SDA, SCL Pins Rising	●	1.5	1.8	2.0	V
$V_{SCL,SDA(HYST)}$	Hysteresis				50		mV
$I_{SCL,SDA(LEAK)}$	Leakage Current	SDA, SCL Pins = 5.5V, 0V, V_{CC} = 5.5V,0V	●			±10	µA
$I_{SCL,SDA(LEAK-INOUT)}$	Input to Output Leakage Current	SDAIN, SCLIN Pins = 5.5V, V_{CC} = 5.5V, SDAOUT, SCLOUT Pins = 4.5V	●			±10	µA
$C_{SCL,SDA}$	Pin Capacitance	Note 3	●			10	pF
$V_{SCL,SDA(PRE)}$	Precharge Voltage		●	0.8	1	1.2	V
$V_{SDAOUT(OL)}$	SDAOUT Output Low Voltage	I = 4mA	●			0.4	V
$R_{DS(ON)}$	Pass Switch On Resistance	V_{CC} = 2.25V, SCLIN = SDAIN = 0.4V	●		3	12	Ω
		V_{CC} = 3.3V, SCLIN = SDAIN = 0.4V	●		2.2	8	Ω
		V_{CC} = 5V, SCLIN = SDAIN = 0.4V	●		1.8	6	Ω
XORH, XORL							
$I_{XORH/XORL}$	XORH and XORL Input Current		●			±100	nA
I²C Interface Timing							
$f_{SCL(MAX)}$	Maximum SCLIN Clock Frequency	Note 3	●	400			kHz
$t_{PDHL(SDAOUTn)}$	SDAOUT Fall Delay	C = 100pF, R_{PULLUP} = 10k	●		170	300	ns
$t_{f(SDAOUTn)}$	SDAOUT Fall Time	C = 100pF, R_{PULLUP} = 10k	●	20	60	300	ns
$t_{TIMEOUT}$	Stuck Bus Timeout	SCLIN Held Low or High	●	25	30	35	ms
t_{IDLE}	Bus Idle Time		●	80	120	160	µs
t_{GLITCH}	SCLIN and SDAIN Glitch Filter		●	50	100		ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All currents into pins are positive and all voltages are referenced to GND unless otherwise indicated.

Note 3: Guaranteed by design and not tested.

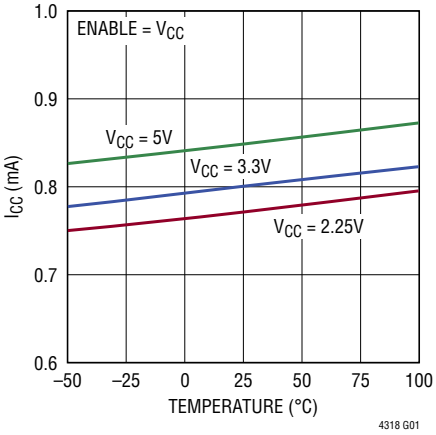
TIMING DIAGRAM



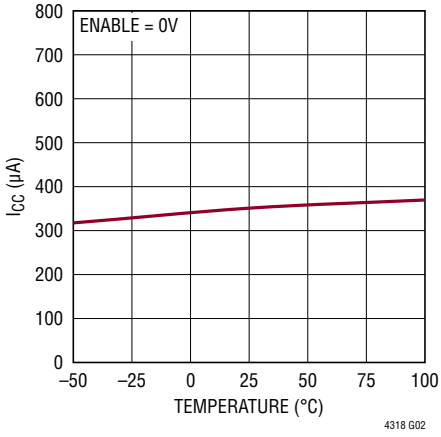
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{CC} = 3.3V unless otherwise noted.

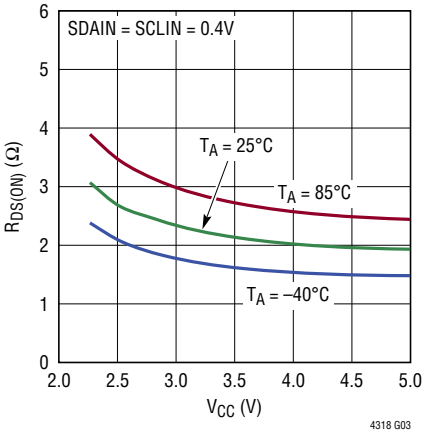
Supply Current vs Temperature



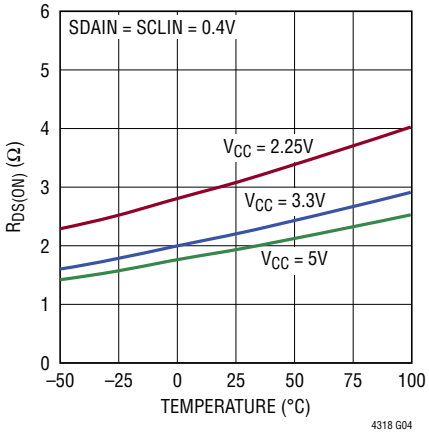
Standby Supply Current vs Temperature



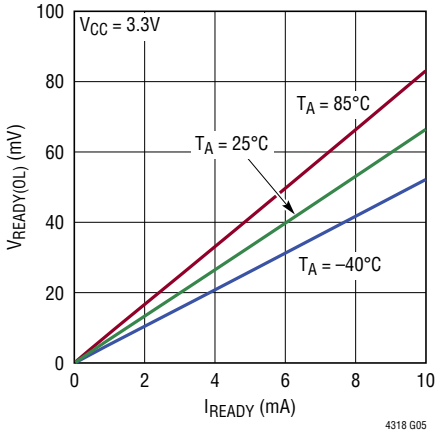
Pass Switch-On Resistance vs V_{CC}



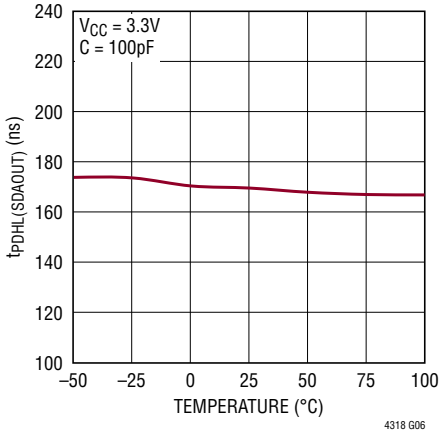
Pass Switch-On Resistance vs Temperature



READY Output Low Voltage vs Current



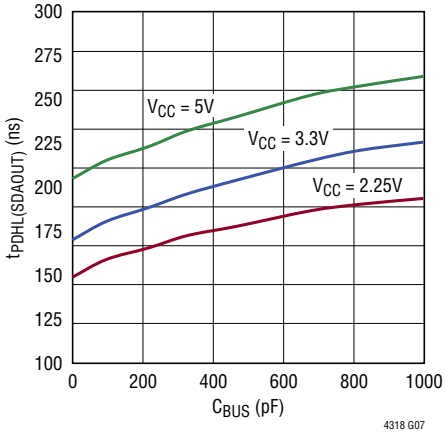
SDAOUT Fall Delay vs Temperature



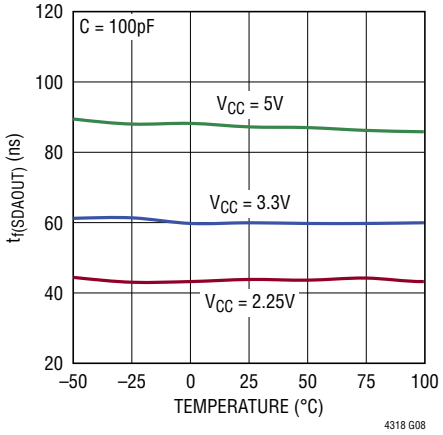
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{CC} = 3.3V unless otherwise noted.

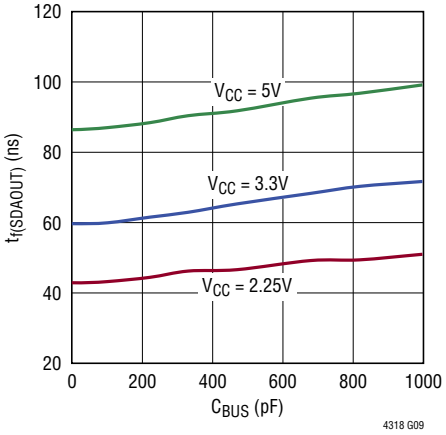
SDAOUT Fall Delay vs Bus Capacitance



SDAOUT Fall Time vs Temperature



SDAOUT Fall Time vs Bus Capacitance



PIN FUNCTIONS

XORL1/XORL2: Translator XOR Lower Nibble Configuration Input. The DC voltage at this pin configures the lower 4-bit nibble of the address translation byte. Tie the pin to an external resistive divider connected between V_{CC} and GND to set the desired DC voltage.

XORH1/XORH2: Translator XOR Upper Nibble Configuration Input. The DC voltage at this pin configures the upper 3-bit nibble of the address translation byte. Tie the pin to an external resistive divider connected between V_{CC} and GND to set the desired DC voltage. Connect this pin to V_{CC} to activate pass-through mode. See Application Information section for more details.

ENABLE1/ENABLE2: Enable Input. If ENABLE pin is low, the address translation is disabled, SDAIN is disconnected from SDAOUT, and SCLIN is disconnected from SCLOUT. A low to high transition on ENABLE restarts the configuration of the address translation byte and also enables the address translation. Connect to V_{CC} if unused.

Exposed Pad: Exposed pad may be left open or connected to device GND.

GND: Device Ground.

READY1/READY2: Ready Status Output. This is an open drain output to indicate that the device is ready for address translation. The pin releases high when the LTC4318 has completed configuration of the address translation byte, SDAIN is connected to SDAOUT and SCLIN is connected to SCLOUT. Connect a pull-up resistor, typically 10k, from this pin to the bus pull-up supply. Leave open or tie to GND if unused.

SCLIN1/SCLIN2: Input Bus Clock Input and Output. Connect this pin to the SCL line on the master side. An external pull-up resistor or current source is required. Connect to V_{CC} through a pull-up resistor if unused.

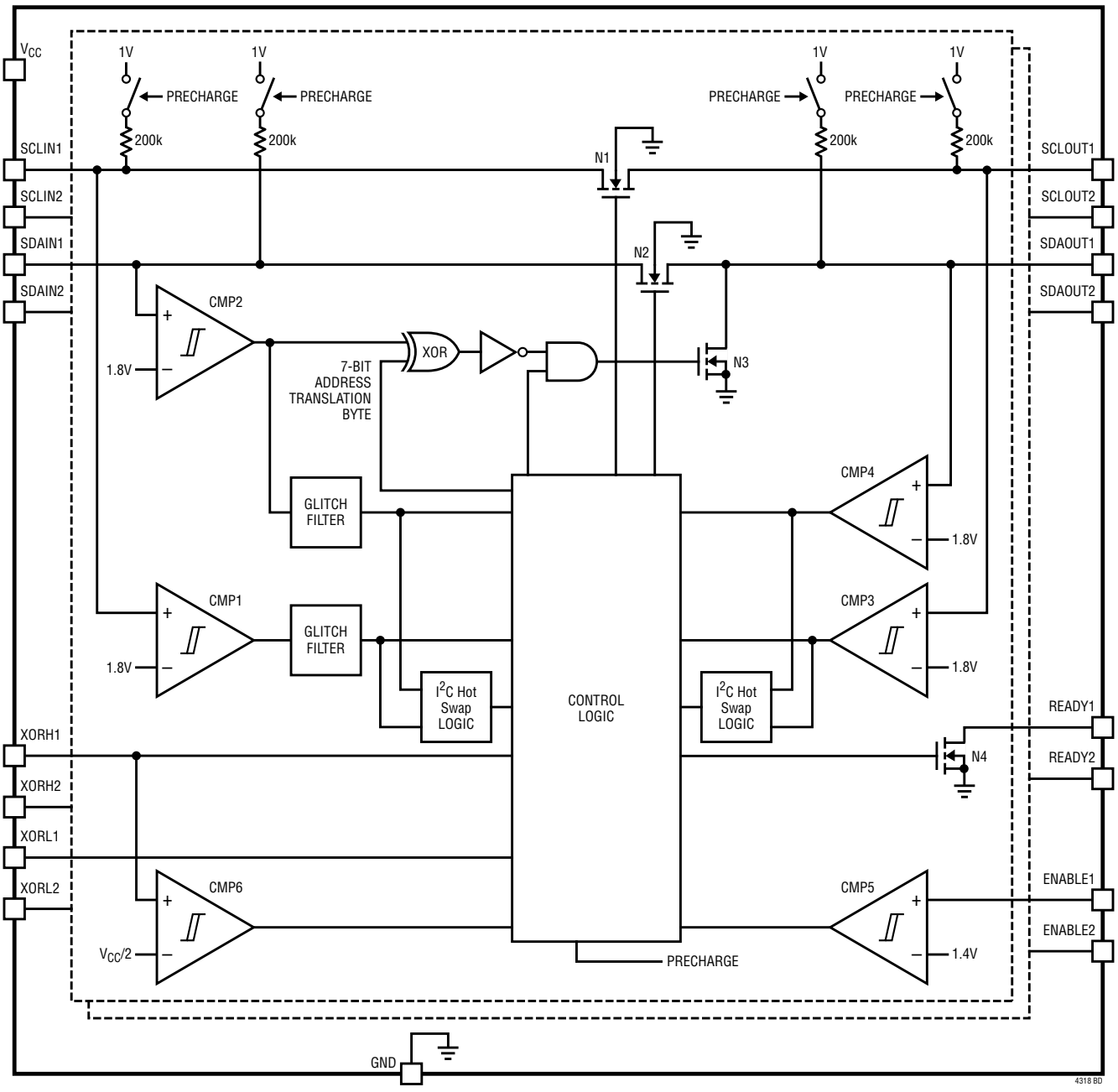
SCLOUT1/SCLOUT2: Output Bus Clock Input and Output. Connect this pin to the SCL line on the slave side. An external pull-up resistor or current source is required. Connect to V_{CC} through a pull-up resistor if unused.

SDAIN1/SDAIN2: Input Bus Data Input and Output. Connect this pin to the SDA line on the master side. An external pull-up resistor or current source is required. Connect to V_{CC} through a pull-up resistor if unused.

SDAOUT1/SDAOUT2: Output Bus Data Input and Output. Connect this pin to the SDA line on the slave side. An external pull-up resistor or current source is required. Connect to V_{CC} through a pull-up resistor if unused.

V_{CC}: Power Supply Input (2.25V to 5.5V). If the supply voltages for the input and output buses are different, connect this pin to the lower supply. If the input and output supplies have the same nominal value and with tolerance less than or equal to ±10%, connect V_{CC} to either supply. Bypass with at least 0.1µF to GND.

BLOCK DIAGRAM



OPERATION

The LTC4318 is an I²C/SMBus address translator. It bridges two segments of an I²C bus, reading incoming addresses on the master side and retransmitting them to the slave side with the 7-bit I²C addresses translated in real time. This allows multiple I²C devices with the same address to be connected to the same bus without interference. The translated addresses are configured with external resistors, and no extra software is required. An ENABLE pin allows bus segments to be enabled and disabled, and the LTC4318 allows hot swapping isolated bus segments together.

Figure 1 shows an I²C master connected to the input bus of the LTC4318 (SCLIN and SDAIN). The slave devices requiring address translation are connected to the output bus of the LTC4318 (SCLOUT and SDAOUT). Any other slave devices that do not require address translation are placed together with the master on the input bus of the LTC4318. Two switches (N1 and N2) inside the LTC4318 connect the input bus to the output bus. N1 connects SCLIN to SCLOUT while N2 connects SDAIN to SDAOUT. In most conditions, N1 and N2 stay on so that the input and output buses are connected.

Translation starts when the master issues a START bit (SDAIN goes low while SCLIN is high). The LTC4318 turns off N2 to disconnect SDAIN from SDAOUT. As the master sends the address byte, the LTC4318 translates the incoming address at the SDAIN pin to a new address at the SDAOUT pin by XORing each incoming bit with a user-configurable translation byte, one bit at a time. N3 turns on and off to send out the new address to the SDAOUT pin. Once all 7 bits of the address are processed, the LTC4318 turns on N2 again to reconnect SDAIN to SDAOUT. The master then transmits the R/W bit directly to the slave. If the new, translated address on SDAOUT matches the slave's address, the slave pulls SDAOUT low to acknowledge (ACK bit). N2 remains on and the rest of the data bytes are transmitted unmodified between the master and slave. The address translation process restarts when the master issues a new START bit.

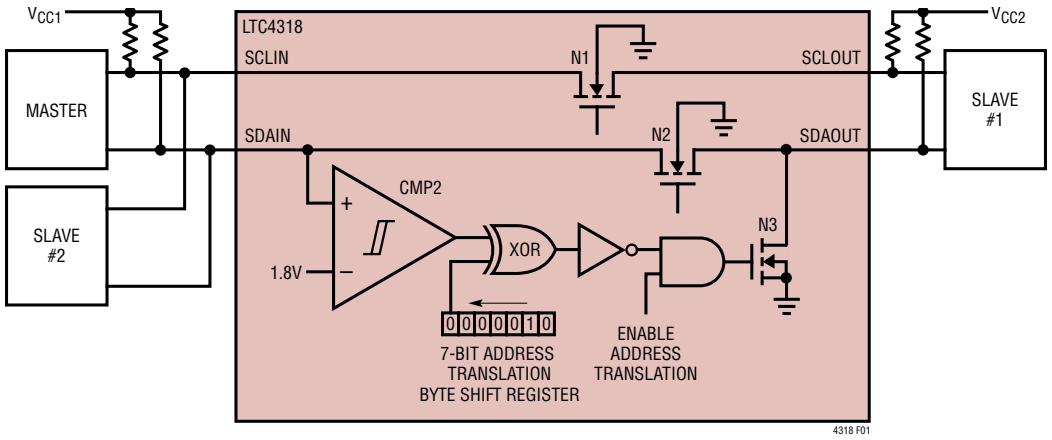


Figure 1. Basic Functions of the LTC4318

OPERATION

Figure 2 shows typical waveforms for the circuit on the front page. In this example, the master transmits address 0x34 while the slave is configured to respond to address 0x36. The resistive dividers at the XORL and XORH pins are configured to generate an address translation byte of 0x02.

Note that in this example, the 8-bit hexadecimal address format (with R/W = 0) is used. 7-bit addresses are also commonly found in I^{2}C device documentation. Make sure to use the correct format when calculating the address translation byte. Table 1 shows examples of both formats.

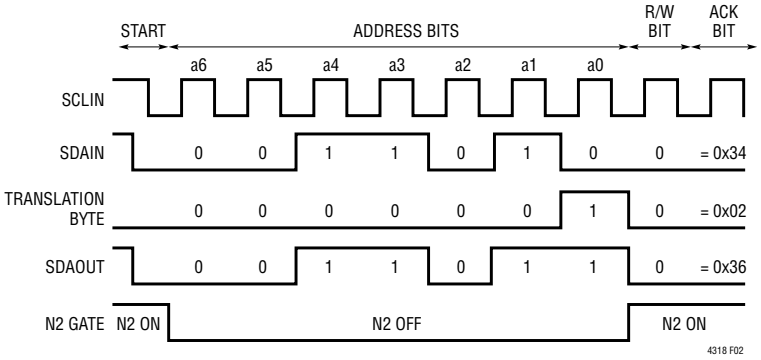


Figure 2. Basic Address Translation Waveforms

Table 1.

DESCRIPTION	BINARY ADDRESS								7-BIT HEX ADDRESS WITHOUT R/W	8-BIT HEX ADDRESS WITH R/W = 0
	a6	a5	a4	a3	a2	a1	a0	R/W		
Input Address from SDAIN	0	0	1	1	0	1	0	0	0x1A	0x34
Translation Byte	0	0	0	0	0	0	1	0	0x01	0x02
Output Address to SDAOUT	0	0	1	1	0	1	1	0	0x1B	0x36

OPERATION

System Configurations

There are several ways that individual slaves or banks of slaves can be connected to an LTC4318. In Figure 3, each slave is paired with one channel of the LTC4318. This configuration allows for maximum flexibility in allocating the bus addresses. Both read and write operations and all protocols supported by the LTC4318 are allowed. Figure 4 shows two slaves with different hardwired addresses translated to two different addresses using one channel of the LTC4318 and a common translation byte. A program is available to help the user visualize an I^2C bus with the LTC4318; this program can be found in the following link:

www.linear.com/TranslatorTool

Setting the Translation Byte

When the LTC4318 is first powered up or any time a rising edge is detected on the ENABLE pin, the LTC4318 reads the voltages at the XORH and XORL pins to determine the 7-bit translation byte. These voltages are referenced to V_{CC} so a resistive divider at each of these pins is the most convenient way to set the voltages. The required translation byte can be determined by taking the bitwise XOR of the slave's original address and the desired input address.

The voltages at the XORH and XORL pins configure the translation byte. The XORL voltage configures the lower 4 translation bits (excluding the R/W bit), while the XORH voltage configures the upper 3 translation bits. Tables 2 and 3 show the recommended resistive divider values. R_{LT} and R_{LB} are the top and bottom resistors connected to XORL, while R_{HT} and R_{HB} are the top and bottom resistors connected to XORH (Figure 5). Use 1% tolerance resistors for R_{LT}, R_{LB}, R_{HT} and R_{HB}.

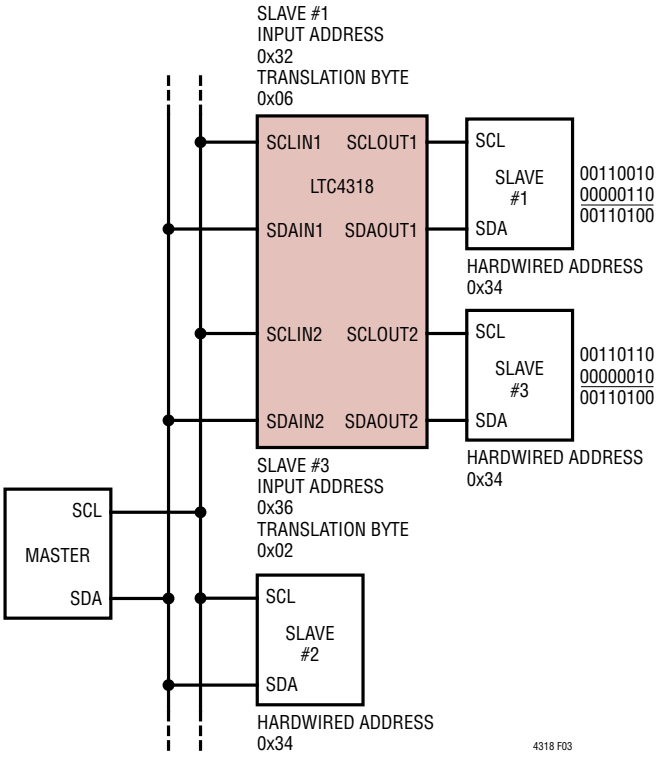


Figure 3. Two Independent Address Translation

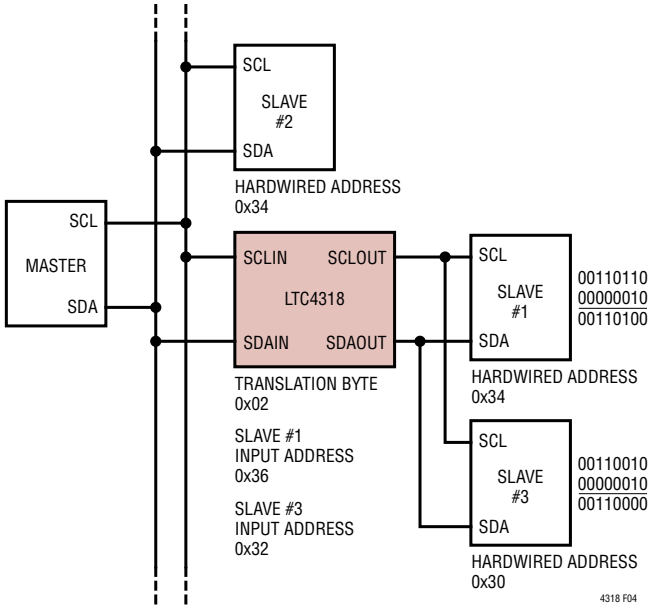


Figure 4. Two Slaves Sharing One Channel of LTC4318

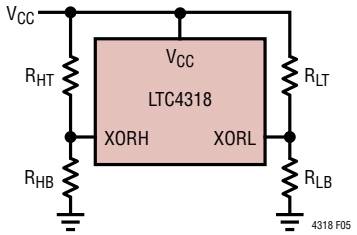


Figure 5. Address Translation Byte Configuration Resistors

OPERATION

Table 2. Setting the Resistive Divider at XORL

LOWER 4-BIT OF TRANSLATION BYTE						
a3	a2	a1	a0	V_{XORL}/V_{CC}	RECOMMENDED R_{LT} [kΩ]	RECOMMENDED R_{LB} [kΩ]
0	0	0	0	≤ 0.03125	Open	Short
0	0	0	1	0.09375 ±0.015	976	102
0	0	1	0	0.15625 ±0.015	976	182
0	0	1	1	0.21875 ±0.015	1000	280
0	1	0	0	0.28125 ±0.015	1000	392
0	1	0	1	0.34375 ±0.015	1000	523
0	1	1	0	0.40625 ±0.015	1000	681
0	1	1	1	0.46875 ±0.015	1000	887
1	0	0	0	0.53125 ±0.015	887	1000
1	0	0	1	0.59375 ±0.015	681	1000
1	0	1	0	0.65625 ±0.015	523	1000
1	0	1	1	0.71875 ±0.015	392	1000
1	1	0	0	0.78125 ±0.015	280	1000
1	1	0	1	0.84375 ±0.015	182	976
1	1	1	0	0.90625 ±0.015	102	976
1	1	1	1	≥ 0.96875	Short	Open

Table 3. Setting the Resistive Divider at XORH

UPPER 3-BIT OF TRANSLATION BYTE					
a6	a5	a4	V_{XORH}/V_{CC}	RECOMMENDED R_{HT} [kΩ]	RECOMMENDED R_{HB} [kΩ]
0	0	0	≤ 0.03125	Open	Short
0	0	1	0.09375 ±0.015	976	102
0	1	0	0.15625 ±0.015	976	182
0	1	1	0.21875 ±0.015	1000	280
1	0	0	0.28125 ±0.015	1000	392
1	0	1	0.34375 ±0.015	1000	523
1	1	0	0.40625 ±0.015	1000	681
1	1	1	0.46875 ±0.015	1000	887

For example, if R_{LT} = 976k, R_{LB} = 102k, R_{HT} = 1000k, and R_{HB} = 280k, the lower 4 translation bits are 0001b and the upper 3 bits are 011b. The 8-bit hexadecimal address translation byte is obtained by adding a 0 as the LSB, which gives 0110 0010b or 0x62. If the configuration voltages at XORL and XORH pins are the same, they can be tied together and connected to a single resistive divider. Alternatively, three resistors can be used to configure the XORL and XORH pins (Figure 6). Use the following procedure to calculate the value of the three resistors:

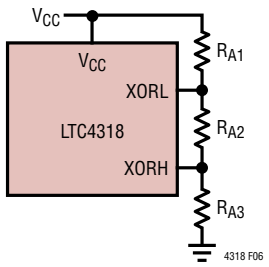


Figure 6. Address Translation Byte Configuration Using Three Resistors

First choose a total resistance value R_{TOTAL}

$R_{A3} = R_{TOTAL} \bullet (V_{XORH}/V_{CC})$

$R_{A2} = (R_{TOTAL} \bullet V_{XORL}/V_{CC}) - R_{A3}$

$R_{A1} = R_{TOTAL} - R_{A3} - R_{A2}$

Use 1% tolerance resistors for R_{A1}, R_{A2} and R_{A3}.

Once the XORL and XORH pins are read, the LTC4318 turns on switches N1 and N2, connecting the input and output, and the READY pin goes high to indicate that the LTC4318 is ready to start address translation.

The address translation byte can be changed during operation by changing the XORH and XORL voltages and toggling the ENABLE pin (high-low-high). This triggers the LTC4318 to re-read the XORL and XORH voltages.

Enable/UVLO

If the ENABLE pin is driven below 1.4V or if V_{CC} is below the UVLO threshold, the LTC4318 shuts down. The internal shift register storing the address translation byte is cleared, address translation is disabled, switches N1, N2 and N3 are off, the READY pin is pulled low and the quiescent current drops to 350µA.

OPERATION

Precharge and Hot Swap

When the LTC4318 is first powered on, switches N1 and N2 are initially off. This allows a LTC4318 and its connected slaves to be hot swapped onto an active I²C bus. Internal precharge circuitry initially sets the bus lines to 1V through a 200k resistor, minimizing disturbance to an active bus when the LTC4318 is connected. The LTC4318 keeps N1 and N2 off until ENABLE goes high, the XORL/XORH pins are read, and both sides of the I²C bus are idle (indicated either by a STOP bit or all bus pins high for longer than 120µs). Once these conditions are met, N1 and N2 turn on, and the READY pin goes high to indicate that the LTC4318 is ready to start address translation.

Pass-Through Mode

If the master wants to communicate with the slave using the general call address, it can temporarily disable address translation by pulling XORH high. This disables address translation and keeps N1 and N2 on regardless of the activity on the buses. Any translation that may be in progress is stopped immediately when XORH goes high.

Extra Transitions on SDAOUT

In an I²C/SMBus system, the master changes the state of the SDA line when SCL is low. The LTC4318 also advances the address translation byte shift register when the SCLIN is low. The translation byte transitions occur approximately 100ns after the falling edge of SCLIN. If the SDAIN transitions sent by the master do not coincide exactly with the LTC4318 address translation bit transitions, an extra transition on SDAOUT may appear (Figure 7). These extra SDA transitions are like glitches similar to those occurring during normal Acknowledge bit transitions and do not pose problems in the system because devices on the bus latch SDA data only when SCL is high.

Level Translation and Supply Voltage Matching

The LTC4318 can operate with different supply voltages on the input and output bus, and it will level shift the voltages on the SCLIN, SDAIN, SCLOUT, and SDAOUT pins to match the supply voltage at each side. V_{CC} must be powered from the lower of the two supply voltages

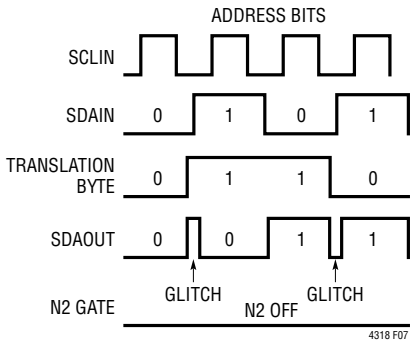


Figure 7. Extra Transitions on SDAOUT While SCL Is Low

for level shifting to operate correctly. For example, if the input bus is powered by a 5V supply and the output bus is powered by a 3.3V supply, the LTC4318 V_{CC} pin must be connected to the 3.3V supply as shown in Figure 8.

If the LTC4318 supply pin is connected to the higher bus supply, current may flow through the switches N1 and

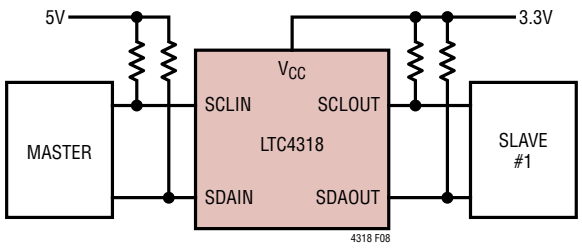


Figure 8. A 5V to 3.3V Level Translation Application

N2 to the bus with lower supply. If the voltage difference is less than 1V, this current is limited to less than 10µA. This allows the input and output buses to be connected to nominally identical supplies that may have up ±10% tolerance, and the LTC4318 V_{CC} pin can be connected to either supply.

Extra START and STOP Bits

During normal operation, an I²C master should not issue a START or STOP bit within a data byte. I²C slave behavior when such a command is received can be unpredictable. The LTC4318 will recover automatically when an unexpected START or STOP is received during the address byte; however, depending on the state of the translating bits, it may convert START bits to STOP bits and vice versa, causing unexpected slave behavior.

OPERATION

If a START bit is received during the address byte when the active translating bit is a "1", the slave device will see a STOP bit. This will typically reset the slave and cause it to miss the remainder of the transmission. If the START bit is received while the active translating bit is a "0", the START passes through the LTC4318 unchanged. The slave will react in the same way it would if the LTC4318 was not present, and will typically reset when the master next issues a STOP bit. In both cases, the LTC4318 automatically resets at the next STOP bit and the next message will be transmitted normally.

If a STOP bit is received during the address byte, the LTC4318 will abort the address translation and ensure that a STOP bit is issued at SDAOUT to reset the slave. If the active translating bit is a "0" when the STOP arrives, it is not modified, and the slave will see the STOP and typically reset. If the active translating bit is a "1" when the STOP arrives, the slave device will see a START bit. This might leave the slave in an indeterminate state, so the LTC4318 briefly disconnects the slave from the master, adds a short delay, and then generates a STOP bit at the SDAOUT pin (Figure 9). It then reconnects the busses and waits for a START bit to begin the next transmission. Again, in both cases, the LTC4318 automatically resets and the next message will be transmitted normally.

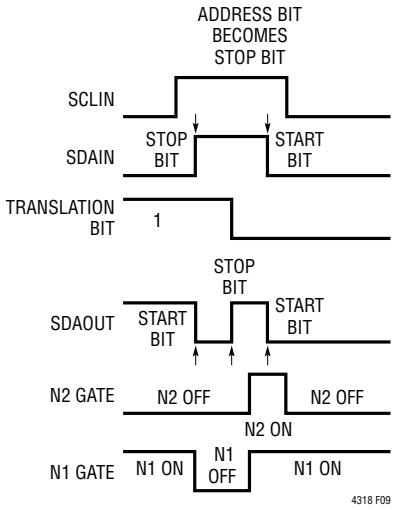


Figure 9. Stop Bit within Address Byte when Address Translation Byte Is 1

Stuck Bus Timeout

During the address translation, if SCLIN stays low or high for more than 30ms without any transitions, the LTC4318 will abort the address translation and reconnect SDAIN to SDAOUT. It will then wait for a START bit to start a new address translation. This prevents any bus stuck low/high conditions from permanently disconnecting SDAIN from SDAOUT.

Supported Protocols

The LTC4318 is designed to support most I²C and SMBus message protocols. The only exceptions are protocols that use pre-assigned addresses on the slave side of the bus.

Supported I²C and SMBus Protocols:

Send/Receive Byte

Write Byte/Word

Read Byte/Word

Process Call

Block Write/Read

Block Write-Block Read Process Call

Extended Read and Write Commands

General Call (I²C Only)

Start Byte (I²C Only)

PMBus (without PEC)

Unsupported I²C Protocols:

10-Bit Addressing

Device ID

Ultra Fast-Mode I²C Bus Protocol

Unsupported SMBus Protocols:

SMBus Host Notify

Address Resolution Protocol (ARP)

Parity Error Code (PEC)

Alert Response Address (ARA)

PMBus (with PEC)

TYPICAL APPLICATIONS

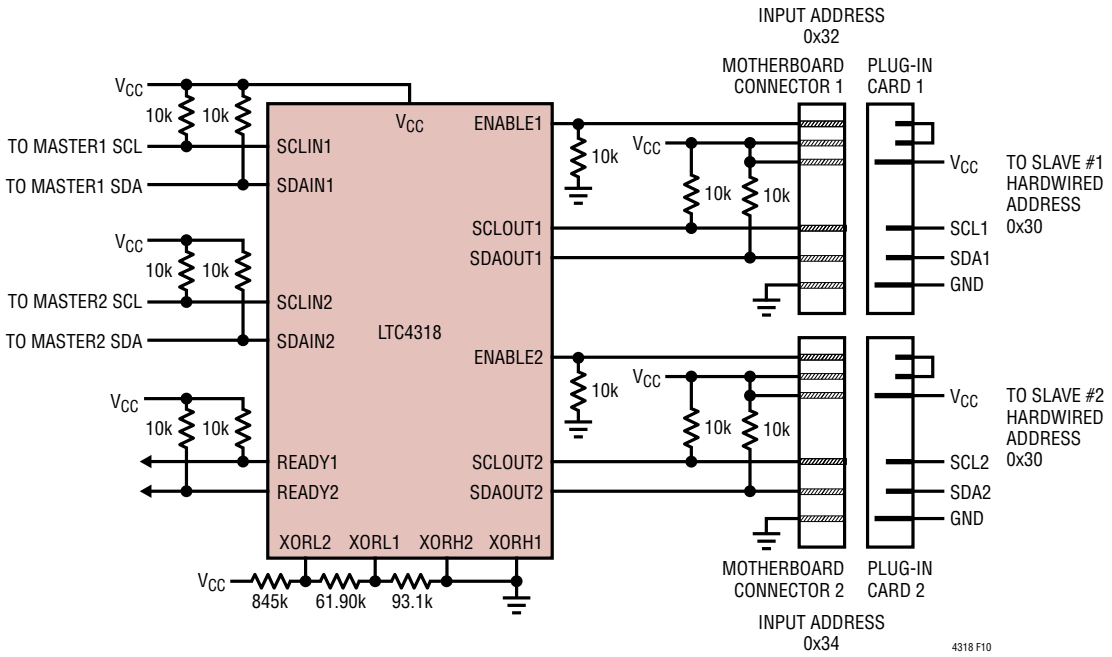
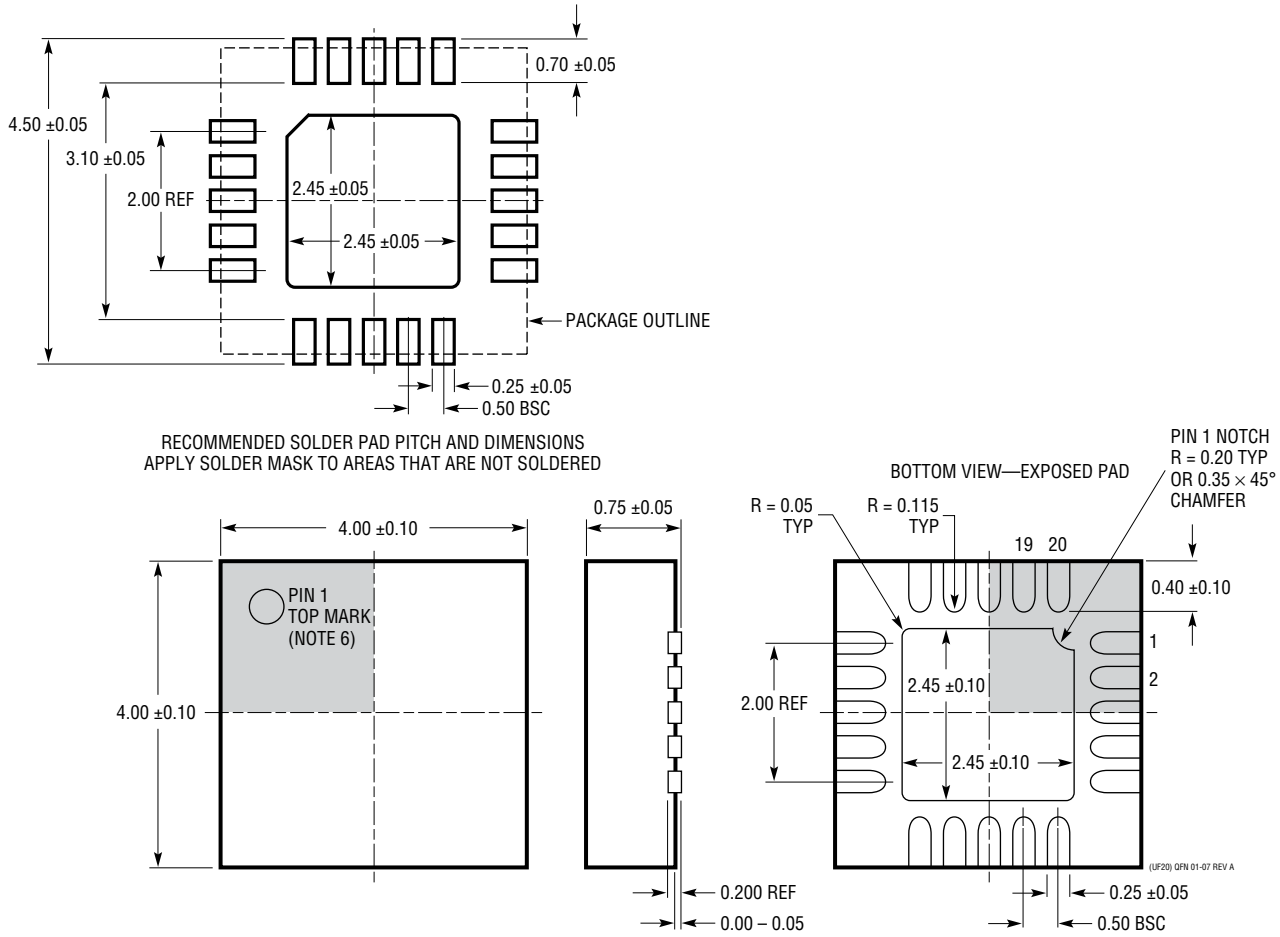


Figure 10. LTC4318 with Address Translation Byte of 0x02 and 0x04

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LTC4318#packaging for the most recent package drawings.

UF Package
20-Lead Plastic QFN (4mm × 4mm)
(Reference LTC DWG # 05-08-1710 Rev A)



NOTE:
1. DRAWING IS PROPOSED TO BE MADE A JEDEC PACKAGE OUTLINE MO-220 VARIATION (WGGD-1)—TO BE APPROVED
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	10/15	Minor edits	4, 5

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TYPICAL APPLICATION

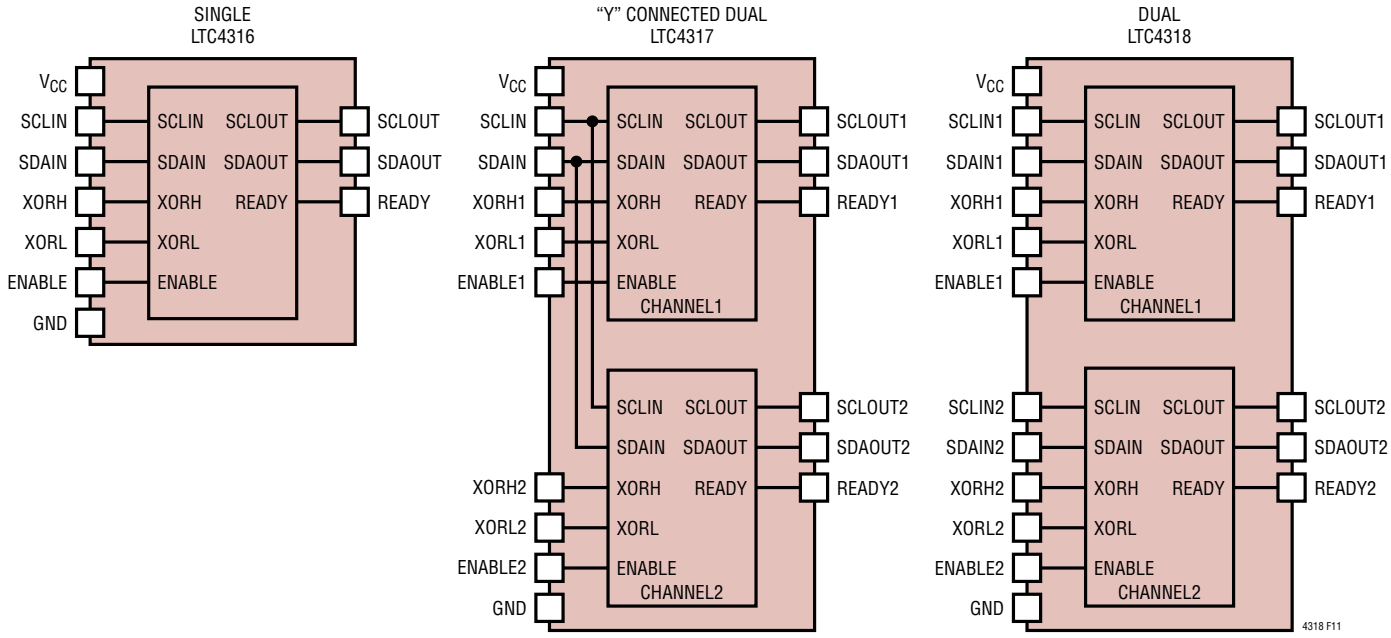


Figure 11. Comparison Between LTC4316/LTC4317/LTC4318

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC4300A-1/ LTC4300A-2/ LTC4300A-3	Hot Swappable 2-Wire Bus Buffers	LTC4300A-1: Bus Buffer with READY and ENABLE LTC4300A-2: Dual Supply Buffer with ACC LTC4300A-3: Dual Supply Buffer and ENABLE
LTC4302-1/ LTC4302-2	Addressable 2-Wire Bus Buffer	Address Expansion, GPIO, Software Controlled
LTC4303/ LTC4304	Hot Swappable 2-Wire Bus Buffer with Stuck Bus Recovery	Provides Automatic Clocking to Free Stuck I^2C Busses
LTC4305/ LTC4306	2- or 4-Channel, 2-Wire Bus Multiplexers with Capacitance Buffering	Two or Four Software Selectable Downstream Busses, Stuck Bus Disconnect, Rise Time Accelerators, Fault Reporting, ±10kV HBM ESD
LTC4307	Low Offset, Hot Swappable 2-Wire Bus Buffer with Stuck Bus Recovery	60mV Buffer Offset, 30ms Stuck Bus Disconnect and Recovery, Rise Time Accelerators, ±5kV HBM ESD
LTC4307-1	High Definition Multimedia Interface (HDMI) Level Shifting 2-Wire Bus Buffer	60mV Buffer Offset, 3.3V to 5V Level Shifting, ±5kV HBM ESD
LTC4308	Low Voltage, Level Shifting Hot Swappable 2-Wire Bus Buffer with Stuck Bus Recovery	Bus Buffer with 1V Precharge, ENABLE and READY, 0.9V to 5.5V Level Translation, 30ms Stuck Bus Disconnect and Recovery, Output Side Rise Time Accelerators, ±6kV HBM ESD
LTC4309	Low Offset Hot Swappable 2-Wire Bus Buffer with Stuck Bus Recovery	60mV Buffer Offset, 30ms Stuck Bus Disconnect and Recovery, Rise Time Accelerators, ±5kV HBM ESD, 1.8V to 5.5V Level Translation
LTC4310-1/ LTC4310-2	Hot Swappable I^2C Isolators	Bidirectional I^2C Communication Between Two Isolated Busses, LTC4310-1: 100kHz Bus, LTC4310-2: 400kHz Bus
LTC4311	Hot Swappable I^2C/SMBus Accelerator	Rise Time Acceleration with ENABLE, ±8kV HBM ESD
LTC4312/ LTC4314	2- or 4-Channel, Hardware Selectable 2-Wire Bus Multiplexers with Capacitance Buffering	Two or Four Pin Selectable Downstream Busses, V_{IL} Up to 0.3V • V_{CC}, Rise Time Accelerators, 45ms Stuck Bus Disconnect and Recovery, ±4kV HBM ESD
LTC4313-1/ LTC4313-2/ LTC4313-3	High Noise Margin 2-Wire Bus Buffers	V_{IL} = 0.3V • V_{CC}, Rise Time Accelerators, Stuck Bus Disconnect and Recovery, 1V Precharge, ±4kV HBM ESD

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