Level Shifting Low Offset Hot Swappable 2-Wire Bus Buffer with Stuck Bus Recovery

FEATURES

- **Bidirectional Buffer Increases Fanout**
- **60mV Buffer Offset Independent of Load**
- **Optional Disconnect when Bus is Stuck Low**
- **Prevents SDA and SCL Corruption During Live Board Insertion and Removal from Backplane**
- **Level Shift 2.5V, 3.3V and 5V Busses**
- **Compatible with Non-Compliant V_{OL} I^2C Devices**
- **±6kV Human Body Model ESD Ruggedness**
- Isolates Input SDA and SCL Lines from Output
- Compatible with I^2C™, I^2C Fast-Mode and SMBus
- READY Open Drain Output
- $\overline{\text{FAULT}}$ Open Drain Output
- 1V Precharge on All SDA and SCL Lines
- Optional Rise Time Accelerators
- High Impedance SDA, SCL Pins for V_{CC} = 0
- Available in Small 12-Pin DFN (4mm x 3mm) and 16-Lead SSOP Packages

APPLICATIONS

- Live Board Insertion
- Servers
- Capacitance Buffer/Bus Extender
- RAID Systems
- ATCA

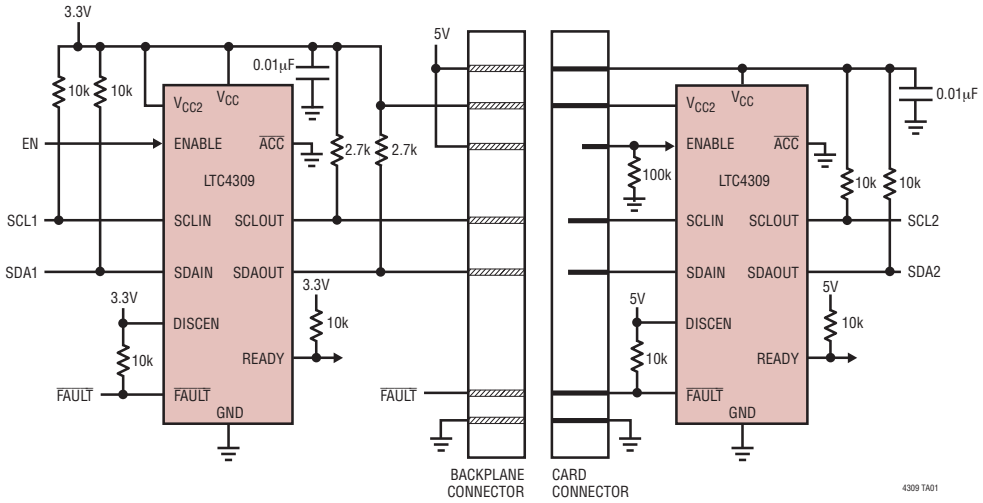
DESCRIPTION

The LTC®4309 hot swappable 2-wire bus buffer allows I/O card insertion into a live backplane without corruption of the data and clock busses. The LTC4309 provides bidirectional buffering, keeping the backplane and card capacitances isolated. Low offset and high V_{OL} tolerance allows cascading of multiple devices on the clock and data busses. If SDAOUT or SCLOUT are low for 30ms, $\overline{\text{FAULT}}$ will pull low indicating a stuck bus low condition. If DISCEN is tied high, the LTC4309 will automatically break the bus connection and generate up to 16 clock pulses and a stop bit in an attempt to free the bus. A connection will resume if the stuck bus is cleared. If DISCEN is connected to GND, the busses will remain connected with no clock or stop bit generation. $\overline{\text{ACC}}$ input enables rise-time accelerators for high capacitively loaded busses.

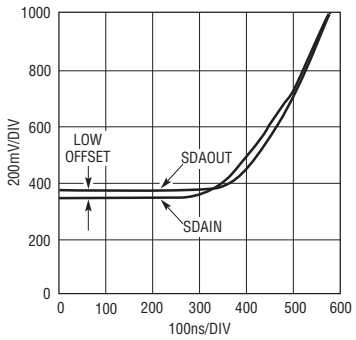
During insertion, the SDA and SCL lines are precharged to 1V to minimize bus disturbances. When driven high, the ENABLE input allows the LTC4309 to connect after a stop bit or bus idle. Driving ENABLE low breaks the connection between SDAIN and SDAOUT, SCLIN and SCLOUT. READY is an open drain output which indicates that the backplane and card sides are connected.

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TYPICAL APPLICATION



Rising Edge from Asserted Low

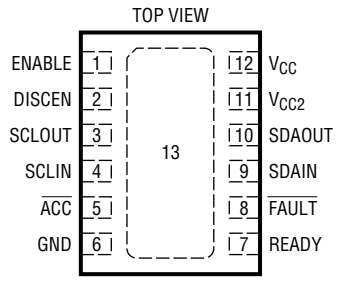


ABSOLUTE MAXIMUM RATINGS (Note 1, 6)

V_{CC}, V_{CC2} to GND .....–0.3 to 6V
SDAIN, SCLIN, SDAOUT, SCLOUT, READY,
ENABLE, $\overline{FAULT}$, $\overline{ACC}$, DISCEN .....–0.3 to 6V
Maximum Sink Current (SDA, SCL, $\overline{FAULT}$, READY)
I_{SINK} 50mA

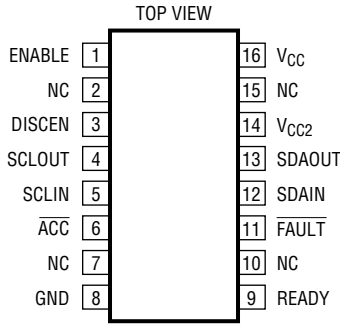
Operating Temperature
LTC4309C ..... 0°C to 70°C
LTC4309I..... –40°C to 85°C
Storage Temperature Range (DE)..... –65°C to 125°C
Storage Temperature Range (GN) ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)
GN Package ..... 300°C

PIN CONFIGURATION



DE12 PACKAGE
12-LEAD (4mm × 3mm) PLASTIC DFN

T_{JMAX} = 125°C, θ_{JA} = 43°C/W
EXPOSED PAD (PIN 13) PCB CONNECTION TO GND IS OPTIONAL



GN PACKAGE
16-LEAD NARROW PLASTIC SSOP

T_{JMAX} = 150°C, θ_{JA} = 110°C/W

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC4309CDE#PBF	LTC4309CDE#TRPBF	4309	12-Lead (4mm × 3mm) Plastic DFN	0°C to 70°C
LTC4309IDE#PBF	LTC4309IDE#TRPBF	4309	12-Lead (4mm × 3mm) Plastic DFN	–40°C to 85°C
LTC4309CGN#PBF	LTC4309CGN#TRPBF	4309	16-Lead Plastic SSOP	0°C to 70°C
LTC4309IGN#PBF	LTC4309IGN#TRPBF	4309I	16-Lead Plastic SSOP	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 3.3V, V_{CC2} = 3.3V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CC}	Positive Supply Voltage		●	2.3		5.5	V
V_{CC2}	Input Side Accelerator Supply Voltage		●	1.8		5.5	V
I_{CC}	V_{CC} Input Supply Current Enabled	V_{CC} = V_{CC2} = 5.5V, V_{SDAIN} = V_{SCLIN} = 0V (Note 2)	●		7	11	mA
I_{SD}	V_{CC} Input Supply Current Disabled	V_{CC} = V_{CC2} = 5.5V, SDA = SCL = 5.5V, ENABLE = 0V	●		900	1400	µA
I_{CC2}	V_{CC2} Input Supply Current Enabled	V_{CC} = V_{CC2} = 5.5V, V_{SDAIN} = V_{SCLIN} = 0V (Note 2)	●		190	250	µA
I_{SD2}	V_{CC2} Input Supply Current Disabled	V_{CC} = V_{CC2} = 5.5V, SDA = SCL = 5.5V, ENABLE = 0V	●		140	180	µA
Propagation Delay and Rise Time Accelerators							
t_{PHL}	SDA/SCL Propagation Delay High to Low	C_{LOAD} = 50pF, 2.7k to V_{CC} on SDA, SCL, (Note 3, 4), (Figure 1)			85		ns
t_{PLH}	SDA/SCL Propagation Delay Low to High	C_{LOAD} = 50pF, 2.7k to V_{CC} on SDA, SCL, (Note 3, 4), (Figure 1)			10		ns
t_{RISE}	SDA/SCL Rise Time	C_{LOAD} = 100pF, 10k to V_{CC} on SDA, SCL, V_{CC} = 5V V_{CC2} = 5V, (Note 3, 5), (Figure 1)			30	300	ns
t_{FALL}	SDA/SCL Fall Time	C_{LOAD} = 100pF, 10k to V_{CC} on SDA, SCL, V_{CC} = 5V (Note 3, 5), (Figure 1)			30	300	ns
$I_{PULLUPAC}$	Transient Boosted Pull-up Current	Positive Transition > 0.8V/µS on SDA, SCL, V_{CC} = 3.3V (Note 7)		5	8		mA
Start-Up Circuitry							
V_{PRE}	Precharge Voltage	SDA, SCL Open	●	0.8	1.0	1.2	V
t_{IDLE}	Bus Idle Time		●	55	95	175	µs
V_{THR_EN}	ENABLE Threshold Voltage	ENABLE Rising Edge	●	0.8	1.4	2	V
$V_{THR_EN(HYST)}$	ENABLE Threshold Voltage Hysteresis	(Note 3)			100		mV
V_{THR_CTRL}	$\overline{ACC}$, DISCEN Threshold Voltage			0.5	0.7	1	V
I_{CTRL}	ENABLE, $\overline{ACC}$, DISCEN Input Currents	ENABLE, $\overline{ACC}$, DISCEN from 0 to V_{CC}	●		0.1	±5	µA
t_{PLH_EN}	ENABLE Delay Off-On	(Figure 1)			95		µs
t_{PHL_EN}	ENABLE Delay On-Off	(Note 3), (Figure 1)			10		ns
t_{PLH_READY}	READY Delay On-Off	(Note 3), (Figure 1)			10		ns
t_{PHL_READY}	READY Delay Off-On	(Note 3), (Figure 1)			10		ns
V_{OL_READY}	READY Output Low Voltage	I_{READY} = 3mA, V_{CC} = 2.3V	●			0.4	V
I_{OFF_READY}	READY Off Leakage Current	V_{CC} = READY = 5.5V	●		0.1	±5	µA
Timing Characteristics							
$f_{I2C, MAX}$	I^2C Maximum Operating Frequency	(Note 3)		400	600		kHz
t_{BUF}	Bus Free Time Between Stop and Start Condition	(Note 3)				1.3	µs
$t_{HD, STA}$	Hold Time After (Repeated) Start Condition	(Note 3)				100	ns
$t_{SU, STA}$	Repeated Start Condition Set-Up Time	(Note 3)				0	ns
$t_{SU, STO}$	Stop Condition Set-Up Time	(Note 3)				0	ns
$t_{HD, DATI}$	Data Hold Time Input	(Note 3)				0	ns
$t_{SU, DAT}$	Data Set-Up Time	(Note 3)				100	ns
Input-Output Connection							
V_{OS}	Input-Output Offset Voltage	2.7k to V_{CC2} on SDA, SCL, Driven SDA, SCL = 0.2V	●	20	60	100	mV
V_{THR}	SDA, SCL Logic Input Threshold Voltage	V_{CC} ≥ 2.9V V_{CC} < 2.9V		1.4 1.1	1.65 1.35	1.9 1.6	V V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 3.3V, V_{CC2} = 3.3V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$V_{THR(HYST)}$	SDA, SCL Logic Input Threshold Voltage Hysteresis	(Note 3)			50		mV
C_{IN}	Digital Input Capacitance SDAIN, SDAOUT, SCLIN, SCLOUT	(Note 3)				10	pF
I_{LEAK}	Input Leakage Current	SDA, SCL, $\overline{ACC}$, DISCEN Pins	●			±5	µA
V_{OL}	Output Low Voltage	SDA, SCL Pins, I_{SINK} = 4mA, Driven SDA/SCL = 0.2V, V_{CC} = V_{CC2} = 2.7V	●	0		0.4	V
		2.7k to V_{CC} on SDA, SCL, Driven SDA/SCL = 0.1V, V_{CC} = V_{CC2} = 3.3V	●	120	170	205	mV
V_{ILMAX}	Buffer Input Logic Low Voltage		●			1.2	V
Bus Stuck Low Timeout							
$t_{TIMEOUT}$	Bus Stuck Low Timer	SDAOUT, SCLOUT = 0V	●	25	30	35	ms
$V_{OL_\overline{FAULT}}$	$\overline{FAULT}$ Output Low Voltage	$I_{\overline{FAULT}}$ = 3mA	●			0.4	V
$I_{OFF_\overline{FAULT}}$	$\overline{FAULT}$ Off Leakage Current		●		0.1	±5	µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Test performed with connection circuity active.

Note 3: Determined by design, not subject to test.

Note 4: For larger equivalent bus capacitance, the skew increases, and setup and hold times must be adjusted accordingly. Please see the Operation Section of the datasheet.

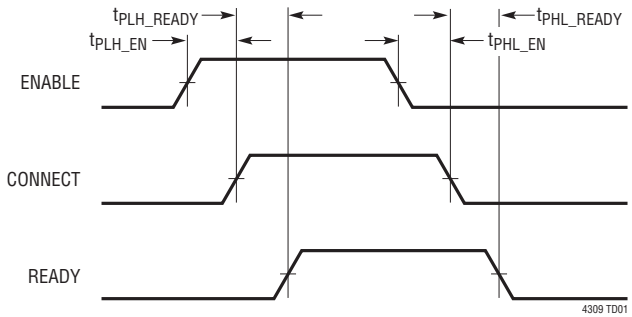
Note 5: Measure points are 0.3 • V_{CC} and 0.7 • V_{CC}.

Note 6: All currents into pins are positive, all voltages are referenced to GND, unless otherwise specified.

Note 7: $I_{PULLUPAC}$ varies with temperature and V_{CC} voltage as shown in the Typical Performance Characteristics section.

TIMING DIAGRAMS

ENABLE and READY Timing



SDA/SCL Propagation Delays, Rise and Fall Times

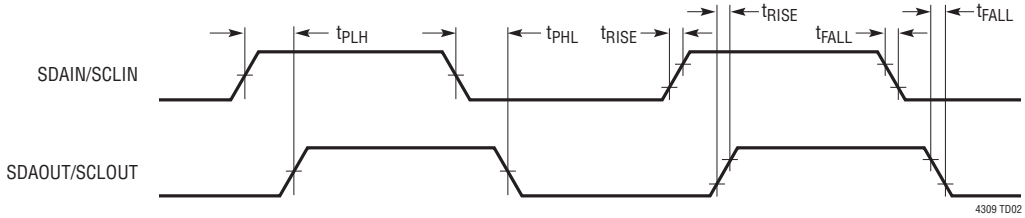
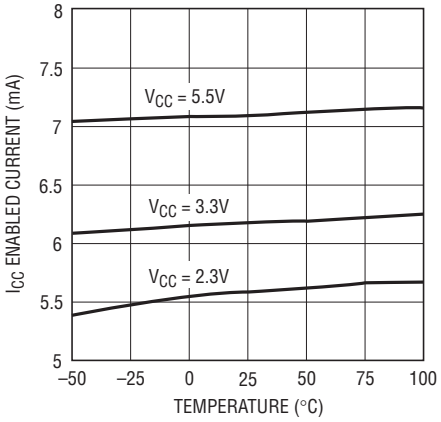


Figure 1. Timing Diagrams

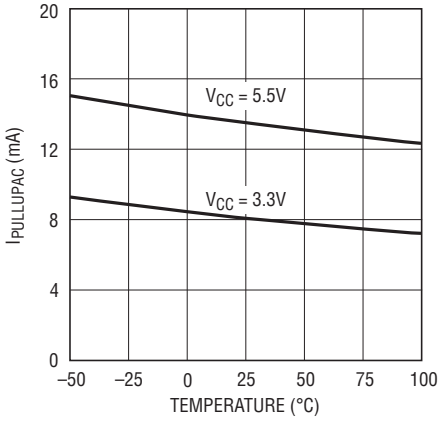
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{CC} = 3.3V, V_{CC2} = 3.3V unless otherwise noted.

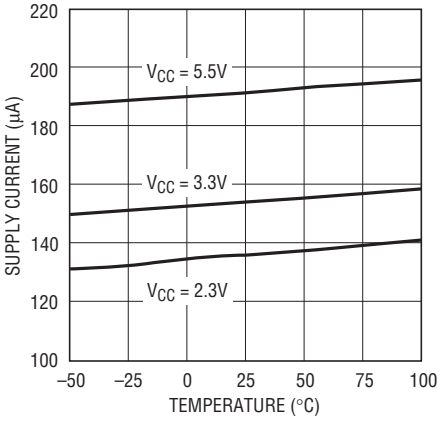
I_{CC} Enabled Current vs Temperature



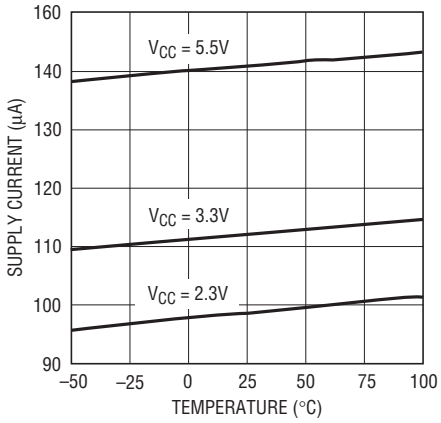
I_{CC} Disabled Current vs Temperature



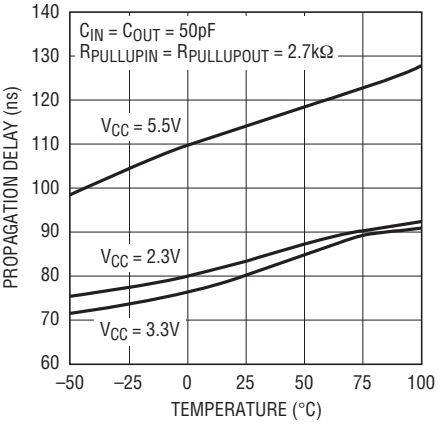
I_{CC2} Enabled Current vs Temperature



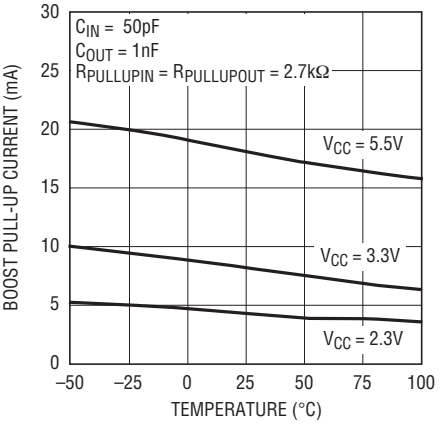
I_{CC2} Disabled Current vs Temperature



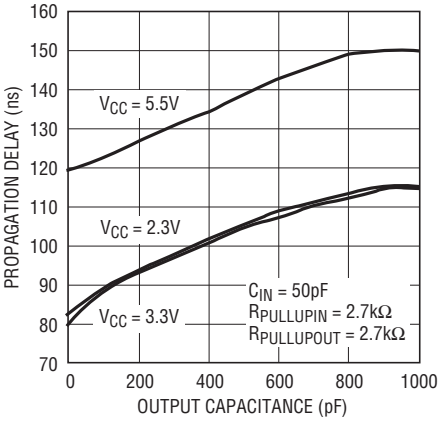
Input-Output High to Low Propagation Delay vs Temperature



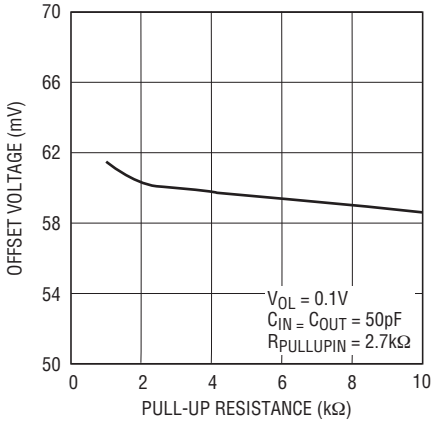
Boost Pull-Up Current vs Temperature



Input-Output High to Low Propagation Delay vs Output Capacitance



Offset Voltage vs Pull-Up Resistance



PIN FUNCTIONS (DE12/GN16)

ENABLE (Pin 1/Pin1): Connection Enable Input. This 1.4V digital threshold input pin enables or disables the LTC4309. For normal operation pull or connect ENABLE high. Driving ENABLE below the 0.8V threshold isolates SDAIN from SDAOUT, SCLIN from SCLOUT, asserts READY low, and prohibits automatic clock and stop bit generation during a fault condition. A rising edge on ENABLE after a fault has occurred forces a connection between SDAIN, SDAOUT and SCLIN, SCLOUT. Connect to V_{CC} if unused.

DISCEN (Pin 2/Pin 3): Bus Stuck Low Disconnect Enable Input. This pin, when high, allows the stuck low bus timeout circuitry to disconnect the bus in a fault condition. When connected to GND, this pin disables the circuitry that disconnects the bus under a fault condition; however, the $\overline{FAULT}$ pin will still go low.

SCLOUT (Pin 3/Pin 4): Serial Clock Output. Connect this pin to a SCL bus segment where bus stuck low recovery is desired. If the output rise time accelerators are enabled, a pull-up resistor should be connected between this pin and a bus supply greater than or equal to V_{CC}. Bus supplies can be lower than V_{CC} if the output rise time accelerators are disabled. See Application Information section for detailed bus pull-up supply options.

SCLIN (Pin 4/Pin 5): Serial Clock Input. Connect this pin to a SCL bus segment where isolation from bus stuck low issues is desired. If the input rise time accelerator is enabled, a pull-up resistor should be connected between this pin and a bus supply greater than or equal to V_{CC2}. Bus supplies can be lower than V_{CC2} if the input rise time accelerators are disabled. See Application Information section for detailed bus pull-up supply options.

$\overline{ACC}$ (Pin 5/Pin 6): Rise Time Accelerator Control Input. This nominal 0.7V threshold input pin enables and disables all rise time accelerators on the SDA and SCL pins. Connect $\overline{ACC}$ to GND to enable all four rise time accelerators or connect $\overline{ACC}$ to V_{CC} to disable all four rise time accelerators. Connect $\overline{ACC}$ to V_{CC2} to GND to enable the accelerators on SDAOUT and SCLOUT only.

GND (Pin 6/Pin 8): Device Ground. Connect this pin to a ground plane for best results.

READY (Pin 7/Pin 9): Connection Ready Status Output. This open-drain N-channel MOSFET pin pulls low when ENABLE is low, when the start-up and connection sequence described in the Operation section has not been completed, or when the LTC4309 disconnects the input and output pins due to a bus stuck low condition. READY goes high when ENABLE is high and connection is made between the input and output pins. Connect a pull-up resistor, typically 10k, from this pin to the bus pull-up supply. This pin can be left open if unused.

$\overline{FAULT}$ (Pin 8/Pin 11): Bus Stuck Low Timeout Output. This open drain N-channel MOSFET output pulls low after 30ms when there is a bus stuck low condition on the output pins of the LTC4309. In normal operation $\overline{FAULT}$ is high. Connect a pull-up resistor, typically 10k, from this pin to the bus pull-up supply. This pin can be left open if unused.

SDAIN (Pin 9/Pin 12): Serial Clock Input. Connect this pin to a SDA bus segment where isolation from bus stuck low issues is desired. If the input accelerator is enabled, a pull-up resistor should be connected between this pin and a bus supply greater than or equal to V_{CC2}. Bus supplies can be lower than V_{CC2} if the input rise time accelerators are disabled. See Application Information section for detailed bus pull-up supply options.

SDAOUT (Pin 10/Pin 13): Serial Clock Output. Connect this pin to a SCL bus segment where bus stuck low recovery is desired. If the output rise time accelerators are enabled, a pull-up resistor should be connected between this pin and a bus supply greater than or equal to V_{CC}. Bus supplies can be lower than V_{CC} if the output rise time accelerators are disabled. See Application Information section for detailed bus pull-up supply options.

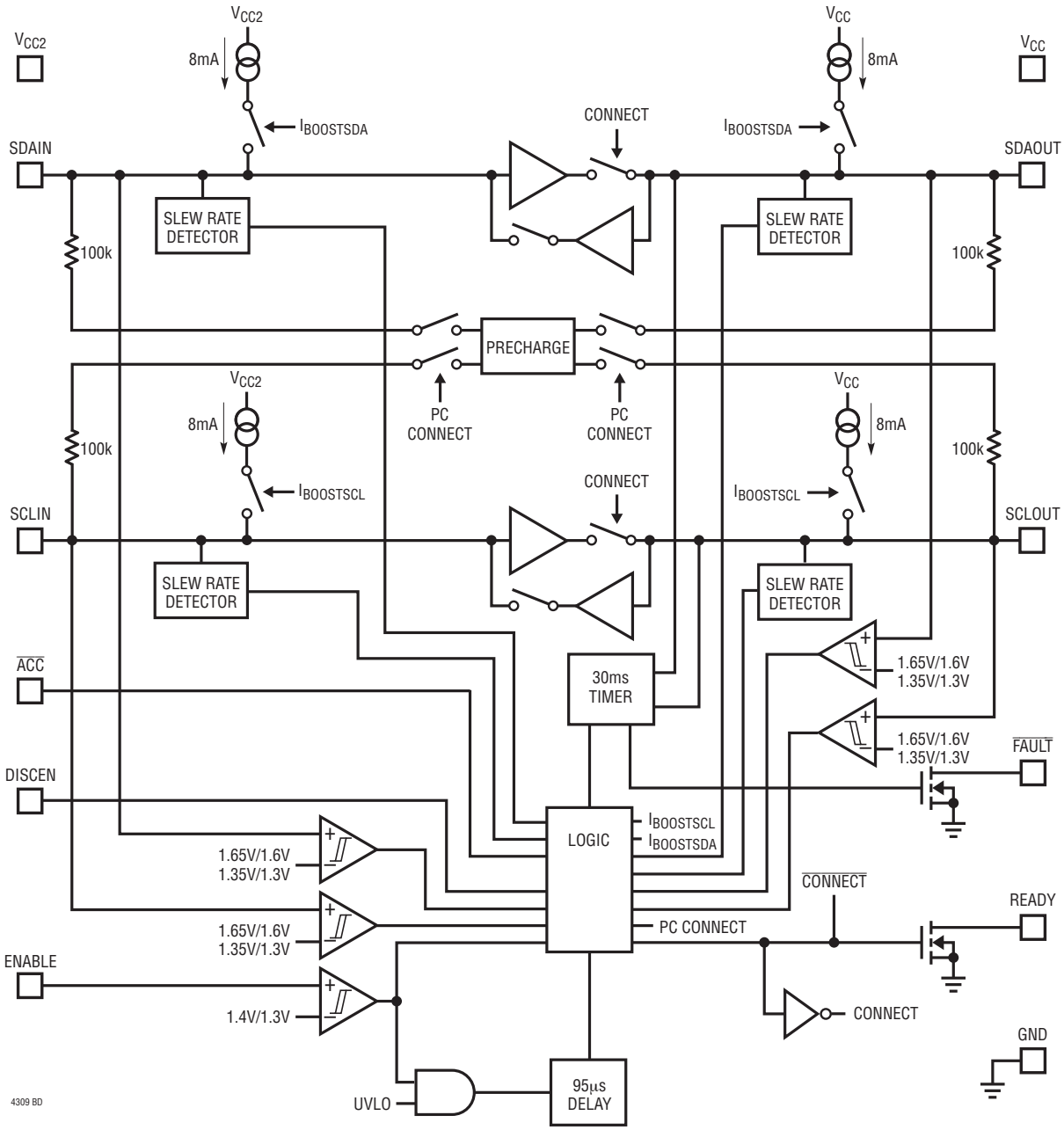
V_{CC2} (Pin 11/Pin 14): Supply Voltage Input for SDAIN and SCLIN Rise Time Accelerator Circuitry. V_{CC2} supplies the rise time accelerator circuitry on the input side. Bypass this pin to GND with a capacitor of at least 0.01µF and place close to V_{CC2} for best results. If V_{CC2} is connected to GND, the input side rise time accelerator circuitry is disabled, regardless of $\overline{ACC}$.

PIN FUNCTIONS (DE12/GN16)

V_{CC} (Pin 12/Pin 16): Supply Voltage Input. Bypass this pin to GND with a capacitor of at least 0.01µF and place close to V_{CC} for best results.

EXPOSED PAD (Pin 13 DE12 Package Only): Exposed Pad may be left open or connected to device ground.

BLOCK DIAGRAM



OPERATION

Start-Up

When the LTC4309 first receives power on its V_{CC} pin, either during power up or live insertion, it starts in an under voltage lockout (UVLO) state, ignoring any activity on the SDA or SCL pins until V_{CC} rises above 2V. This ensures the LTC4309 does not try to function until enough supply voltage is present.

During this time, the 1V precharge circuitry is actively forcing 1V through 100k nominal resistors to the SDA and SCL pins. Because the I/O card is being plugged into a live backplane, the voltage on the backplane SDA and SCL busses may be anywhere between 0V and V_{CC}. Precharging the SCL and SDA pins to 1V minimizes the worst-case voltage differential these pins will see at the moment of contact, therefore minimizing the amount of disturbance caused by the I/O card.

Once the LTC4309 exits from UVLO, it monitors both the input and output pins for either a stop bit or a bus idle condition to indicate the completion of data transactions. When both sides are idle or one side has a stop bit while the other is idle, the connection circuitry is activated, joining the SDA and SCL busses on the input side with those on the output side.

Rise Time Accelerators

Once connection has been established if $\overline{ACC}$ is connected to ground and V_{CC2} is powered from a supply voltage greater than or equal to 1.8V, the rise time accelerator circuits on all four SDA and SCL pins are enabled. During positive bus transitions of at least 0.8V/µs, the rise time accelerators provide strong, slew-limited pull-up currents to force the bus voltage to rise at a rate of 100V/µs. Enabling the rise time accelerators allows users to choose larger bus pull-up resistors, reducing power consumption and improving logic low noise margins, or design with bus capacitances beyond those specified in the I^2C specifications.

To ensure the rise time accelerators are properly activated when the rise time accelerators are enabled, users should choose bus pull-up resistors that guarantee the bus will rise on its own at a rate of at least 0.8V/µs. See the Application Information section for determining the correct pull-up resistor size.

All four rise time accelerators can be disabled by connecting $\overline{ACC}$ to V_{CC}. To activate the rise time accelerators on only SDAOUT and SCLOUT, connect both $\overline{ACC}$ and V_{CC2} to ground. The rise time accelerators are also internally disabled until the sequence of events described in the start-up section have been completed, as well as during automatic clocking and stop bit generation for a bus stuck low recovery event.

Connection Circuitry

Once the connection circuitry is activated, the functionality of the input and output bus of the respective SDA or SCL pins are identical. A low forced on either output or input pin at any time results in both pin voltages forced low. The LTC4309 is tolerant of I^2C bus DC logic low voltages up to the V_{IL} specification of $0.3 \bullet V_{CC}$.

When the LTC4309 senses a rising edge on the bus, with a slew rate greater than 0.8V/µs, the internal pull-down device for the respective bus is deactivated at bus voltages as low as 0.48V. This methodology maximizes the effectiveness of the rise time accelerator circuitry and maintains compatibility with other devices in the LTC4300 bus buffer family. Care must be taken to ensure devices participating in clock stretching or arbitration are capable of forcing logic low voltages below 0.48V at the LTC4309's SDA and SCL pins.

A high occurs when all devices on the input and output pins release high. These important features ensures the I^2C specification protocols such as clock stretching, clock synchronization, arbitration, and acknowledge function seamlessly in all cases as specified, regardless of how the devices in the system are connected to the LTC4309.

Another key feature provided by the connection circuitry is input and output bus capacitance isolation through bidirectional buffering. Because of this isolation, the waveforms on the input busses look slightly different than the corresponding output bus waveforms, as described below.

Input to Output Offset Voltage

When a logic low voltage is driven on any of the LTC4309's data or clock pins, the LTC4309 regulates the voltage on the other side of the device to a slightly higher voltage,

OPERATION

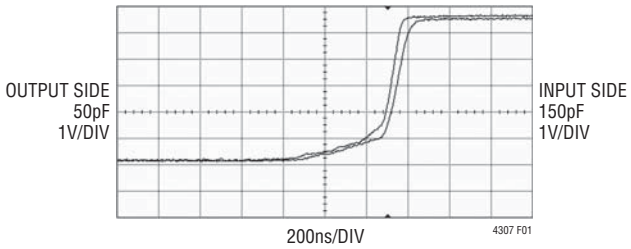


Figure 2. Input-Output Rising Edge Waveforms

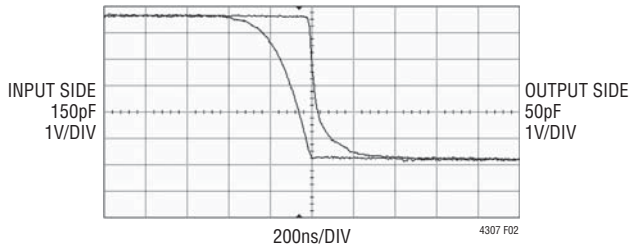


Figure 3. Input-Output Falling Edge Waveforms

typically 60mV. This offset is nearly independent of pull-up current. (See Typical Performance curves.)

Propagation Delays

During a rising edge, the rise time on each side is determined by the bus pull-up resistor and the equivalent capacitance on the line. If the pull-up resistors are the same, a difference in rise time occurs which is directly proportional to the difference in capacitance between the two sides. This effect is displayed in Figure 2 for V_{CC} and V_{CC2} = 5.5V and a 10k pull-up resistor on each side (50pF on one side and 150pF on the other). Since the output side has less capacitance than the input, it rises faster and the effective propagation delay is negative.

There is a finite propagation delay through the connection circuitry for falling waveforms. Figure 3 shows the falling edge waveforms for the same pull-up resistors and equivalent capacitance conditions as used in Figure 2. An external N-channel MOSFET device pulls down the voltage on the side with 150pF capacitance; LTC4309 pulls down the voltage on the opposite side, with a delay of 85ns. This delay is always positive and is a function of supply voltage, temperature and the pull-up resistors and equivalent bus capacitances on both sides of the bus.

The Typical Performance Characteristics section shows Propagation Delay as a function of temperature and voltage for 2.7k pull-up resistors and 50pF equivalent capacitance on both sides of the part. Also, the Propagation Delay as a function of Output Capacitance curve shows that larger output capacitances translate to longer delays. Users must quantify the difference in propagation times for a rising edge versus a falling edge in their systems and adjust setup and hold times accordingly.

Bus Stuck Low Timeout

When SDAOUT or SCLOUT is low, an internal timer is started. The timer is only reset by the respective pin going high. If the bus stuck low does not go high within 30ms (typical), the $\overline{FAULT}$ pin pulls low indicating a bus stuck low condition. If DISCEN is connected to V_{CC}, the connection circuitry is disabled, breaking the connection between the respective input and output pins. In addition, after at least 40µs, up to 16 clock pulses at 8.5kHz (typical) is generated on the SCLOUT pin by the LTC4309 in an attempt to free the stuck low bus. Once the clock pulses have completed, a stop bit is generated on the SCLOUT and SDAOUT pins to reset all devices on the bus.

If the stuck low SDAOUT or SCLOUT recovers to a logic high, the $\overline{FAULT}$ flag clears, and the LTC4309 waits for either a stop bit or a bus idle condition to activate the connection circuitry to reconnect the input and output busses.

If DISCEN is connected to GND, the $\overline{FAULT}$ pin will pull low, but the connection circuitry will not be disabled, leaving the input and output busses connected. Also, no clock or stop bit is generated.

When powering up into a bus stuck low condition, the connection circuitry connecting the SDA and SCL busses on the I/O card with those on the backplane is not activated. 30ms after UVLO, the $\overline{FAULT}$ pin pulls low indicating a bus stuck low condition and automatic clocking and stop bit generation takes place as described above.

READY Digital Output

This pin provides a digital flag which is low when either ENABLE is low, the start-up sequence described earlier in this section has not been completed, or the LTC4309

OPERATION

has disconnected the input and output busses due to a bus stuck low condition. READY goes high when ENABLE is high and start-up is complete. The pin is driven by an open drain pull-down device capable of sinking 3mA while holding 0.4V on the pin. Connect a resistor to the bus pull-up supply to provide the pull-up.

$\overline{\text{FAULT}}$ Digital Output

This pin provides a digital flag which is low when SDA or SCL is low for 30ms (typical). The pin is driven by an open drain pull-down capable of sinking 3mA while holding 0.4V on the pin. Connect a resistor from $\overline{\text{FAULT}}$ to the bus pull-up supply to provide the pull-up.

ENABLE

When the ENABLE pin is driven below 0.8V with respect to the LTC4309's ground, the input pin is disconnected from the output pin and the READY pin is internally pulled low. When the pin is driven above 2V, the part waits for data transactions on both the input and output pins to be complete (as described in the Start-Up section) before connecting the two sides. At this time the internal pull-down on READY releases.

A rising edge on ENABLE after a fault has occurred forces a connection between SDAIN, SDAOUT and SCLIN, SCLOUT, even if the bus stuck low conditions has not been cleared. At this time, the 30ms timer is reset, but not disabled.

APPLICATIONS INFORMATION

Live Insertion and Capacitance Buffering Application

Figures 4 and 5 illustrate applications of the LTC4309 that take advantage of the LTC4309's Hot Swap™, capacitance buffering and precharge features. If the I/O cards were plugged directly into the backplane without the LTC4309 buffer, all of the backplane and card capacitances would add directly together, making rise time and fall time requirements difficult to meet. Placing an LTC4309 on the edge of each card, however, isolates the card capacitance from the backplane. For a given I/O card, the LTC4309 drives the capacitance of everything on the card and the backplane must drive only the capacitance of the LTC4309, which is less than 10pF.

Figure 4 shows the LTC4309 used in the typical staggered connector application, where V_{CC} and GND are the longest "early power" pins. The "early power" pins ensure the LTC4309 is initially powered and forcing a 1V precharge voltage on the medium length SDA and SCL pins before they contact to the backplane busses. Coupled with ENABLE as the shortest pin, passively pulled to ground by a resistor, the staggered approach provides additional time for transients associated with live insertion to settle before the LTC4309 can be enabled.

Figure 5 shows the LTC4309 in an application where all of the pins have the same length. In this application, a resistor is used to hold the ENABLE pin low during live insertion, until the backplane control circuitry can enable the device.

Repeater/Bus Extender Applications

Users who wish to connect two 2-wire systems separated by a distance can do so by connecting two LTC4309s back-to-back, as shown in Figure 6. The I^2C specification allows for 400pF maximum bus capacitance, severely limiting the length of the bus. The SMBus specification places no restriction on bus capacitance, but the limited impedances of devices connected to the bus require systems to remain small if rise time and fall time specifications are to be met. In this situation, the differential ground voltage between the two systems may limit the allowed distance, because a valid logic low voltage with respect to the ground at one end of the system may violate the allowed V_{OL} specification with respect to the ground at the other end. In addition, the connection circuitry offset voltages of the back-to-back LTC4309s add together, directly contributing to the same problem.

Figure 7 further illustrates a repeater application. In AdvancedTCA applications, the bus pull-up resistance can be quite small. Since there is no effect on the offset due

Hot Swap is a trademark of Linear Technology Corporation.

APPLICATIONS INFORMATION

to the pull-up impedance, multiple LTC4309 buffers can be used in a single system. This allows the user to divide the line and device capacitances into more sections with buffering and meet rise and fall times.

The LTC4309 disconnects when both bus I/O's are above 0.48V and rising. In systems with large ground bounce, if many devices are cascaded, the 0.48V threshold can be exceeded, and the transients associated with the ground bounce can appear to be a rising edge. Under this condition, the LTC4309 with inputs above 0.48V may disconnect.

Level Shifting Applications

Systems requiring different supply voltages for the backplane side and the card side can use the LTC4309 for bidirectional level shifting, as shown in Figure 6. The LTC4309 can level shift between bus pull-up supplies as low as 1.7V, with the accelerators disabled, to as high as 5.5V. Level shifting allows newer designs that require low voltage supplies, such as EEPROMs and microcontrollers, the capability to interface with legacy backplanes which may be operating at higher supply voltages.

Systems with Supply Voltage Droop

In large 2-wire systems, the supply voltages seen by devices at various points in the system can differ by a few hundred millivolts or more. For proper operation, make sure that the $V_{CC2(LTC4309)}$ is ≥ 1.8V, and $V_{CC(LTC4309)}$ ≥ 2.3V.

Additional Pull-Up Supply Options

In typical applications, a pull-up resistor connected from the LTC4309's bus output pins to V_{CC} and bus input pins to V_{CC2} or V_{CC}, if V_{CC2} is grounded, is sufficient. However, for unique applications, additional flexibility is available for bus pull-up supplies other than V_{CC} or V_{CC2}. One example is shown in Figure 8. The expanded bus pull-up range is dependent on the user configuration of the rise time accelerators and the supply voltage, V_{CC}.

If the rise time accelerators are enabled, the bus pull-up supply can be greater than or equal to V_{CC} for the output busses and accordingly, the input pull-up supply can be greater than or equal to V_{CC2} for the input busses. This ensures the LTC4309's rise time accelerators do not source current through the pull-up resistors into the pull-up supply. If the rise time accelerator circuitries are disabled, the bus pull-up supply can be as low as 2V for $V_{CC} \geq 2.9V$ and for $V_{CC} < 2.9V$, the bus pull-up supply can be as low as 1.7V. The bound on the lower supply limit exists to ensure the bus signal range exceeds the logic input threshold voltage, V_{THR}.

Resistor Pull-Up Value Selection

To guarantee the rise time accelerators are activated during a rising edge, the bus must rise on its own with a positive slew rate of at least 0.8V/µs. To achieve this, choose a maximum resistor value R_{PULLUP} using the formula:

$$R_{PULLUP} \leq \frac{(V_{BUS(MIN)} - 0.8V) \bullet 1250 \frac{ns}{V}}{C_{BUS}}$$

Where R_{PULLUP} is the pull-up resistor value in kilo ohms, $V_{BUS(MIN)}$ is the minimum bus pull-up supply voltage and C_{BUS} is the equivalent bus capacitance in pico-Farads (pF).

To estimate the value of C_{BUS}, use a general rule of 20pF of capacitance per device on the bus (10pF for the device and 10pF for interconnect).

In addition, R_{PULLUP} must be strong enough to overcome the precharge voltage and provide logic highs on SDAOUT and SCLOUT for the start-up and connection circuitry to connect the backplane to the card. Regardless of the bus capacitance, always choose

$$R_{PULLUP} \leq \frac{V_{BUS(MAX)} - V_{THR}}{100\mu A}$$

APPLICATIONS INFORMATION

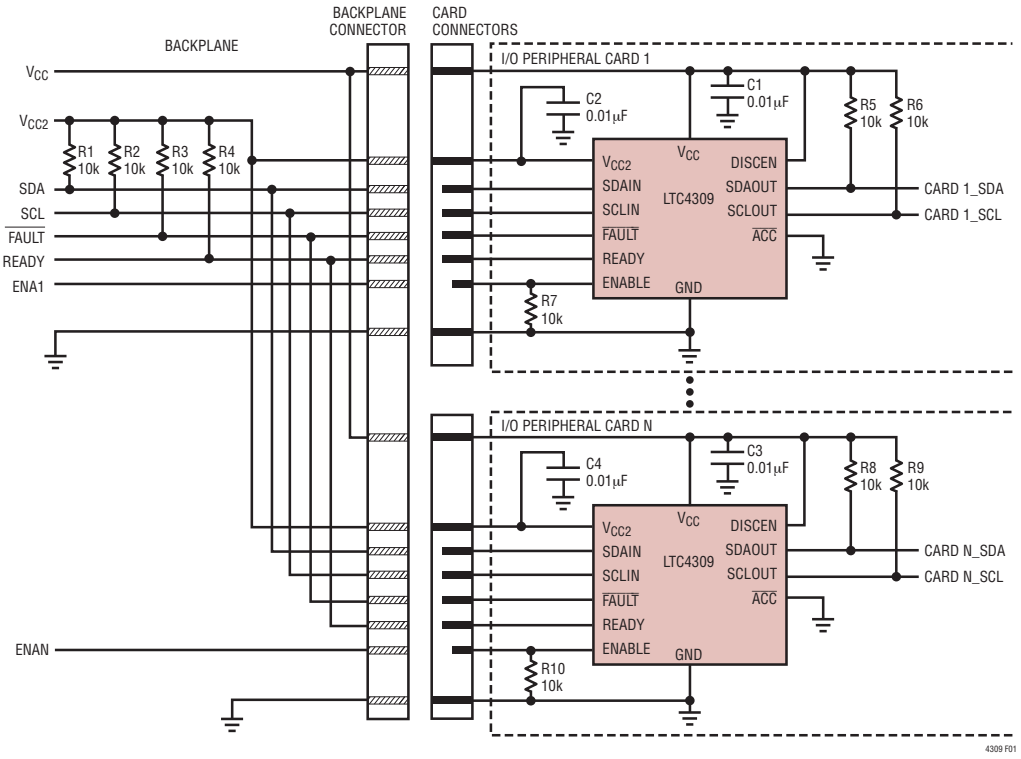


Figure 4. The LTC4309 in an Application with a Staggered Connector.

APPLICATIONS INFORMATION

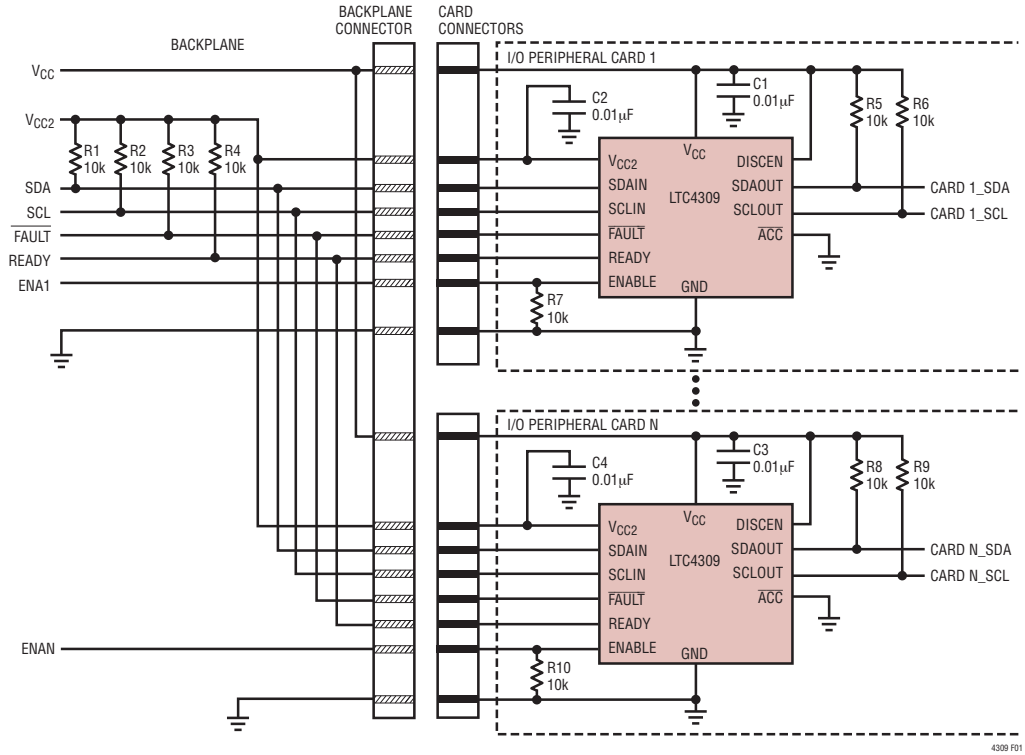


Figure 5. The LTC4309 in an Application Where All the Pins Have the Same Length.

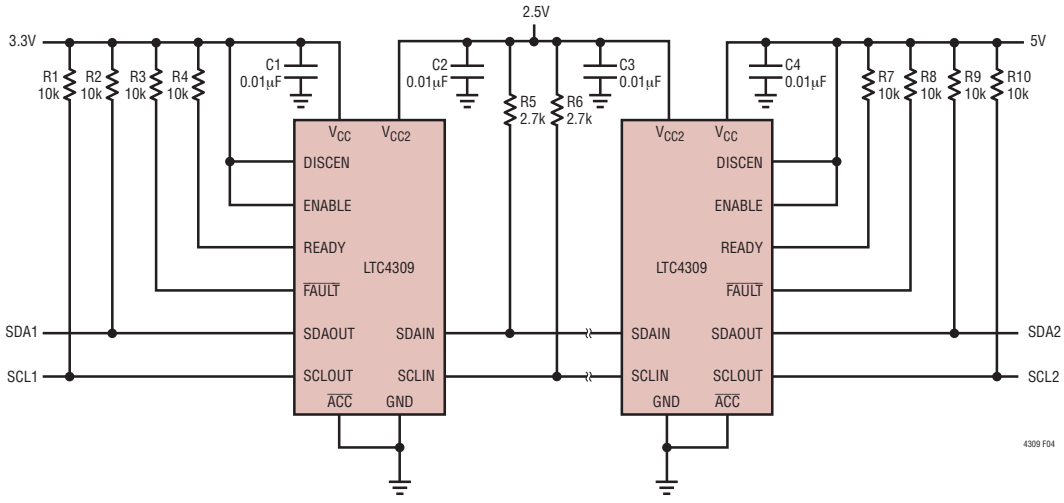


Figure 6. The LTC4309 in a Level Shifting Repeater/Bus Extender Application.

APPLICATIONS INFORMATION

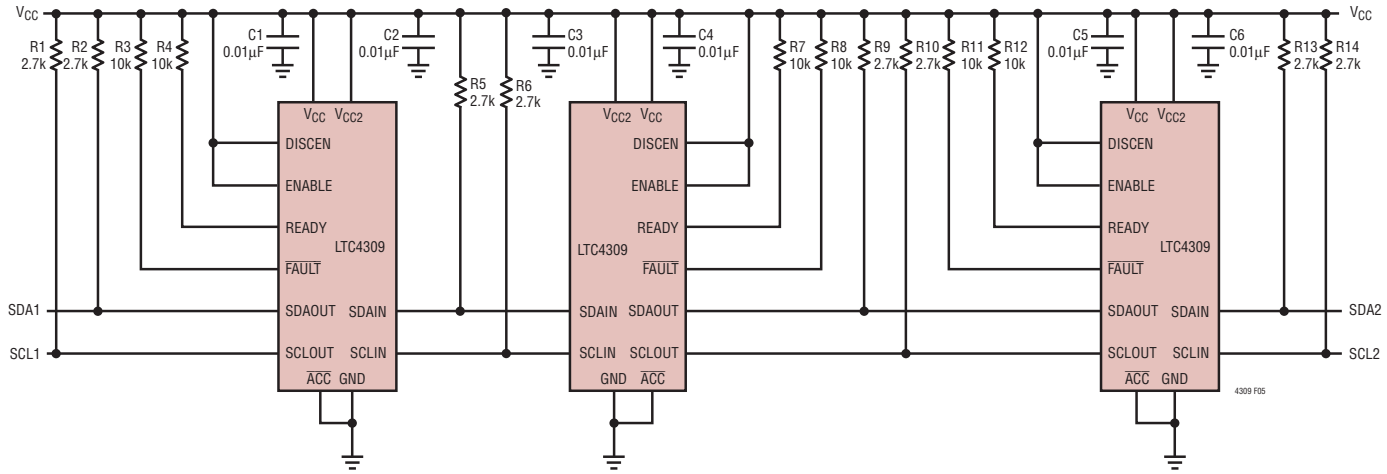


Figure 7. The LTC4309 in a Repeater Application. The LTC4309's Low Offset Allows Cascading of Multiple Devices.

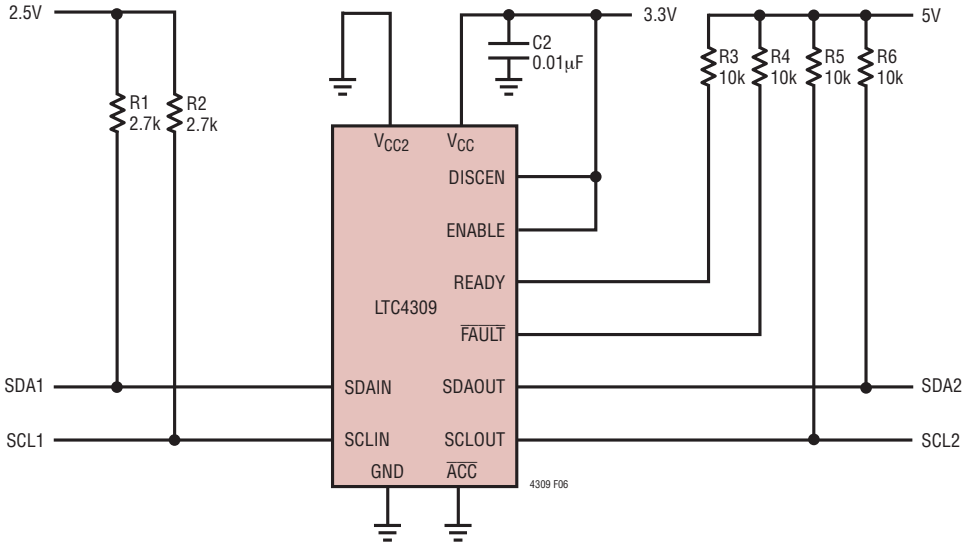
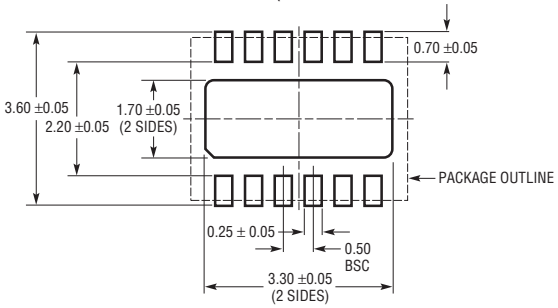


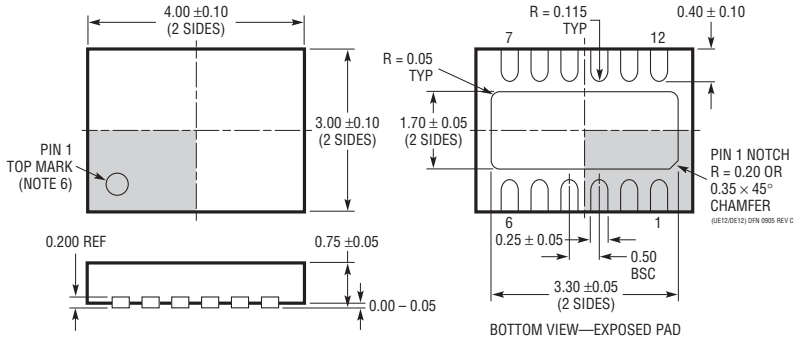
Figure 8. The LTC4309 in a level shifting application where the bus supplies are different from V_{CC}.

PACKAGE DESCRIPTION

DE/UE Package
12-Lead Plastic DFN (4mm x 3mm)
(Reference LTC DWG # 05-08-1695)



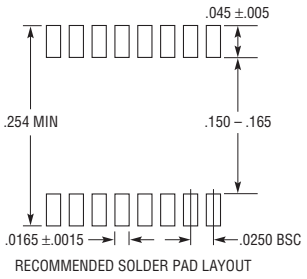
RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



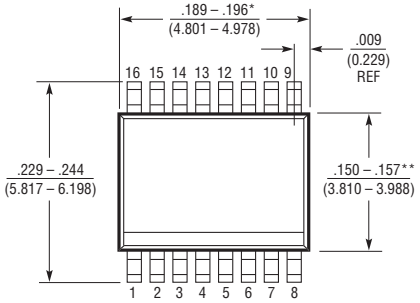
BOTTOM VIEW—EXPOSED PAD

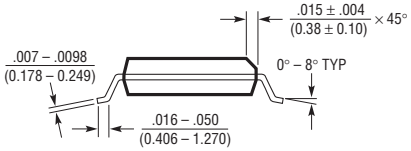
NOTE:
1. DRAWING PROPOSED TO BE A VARIATION OF VERSION (WGED) IN JEDEC PACKAGE OUTLINE M0-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

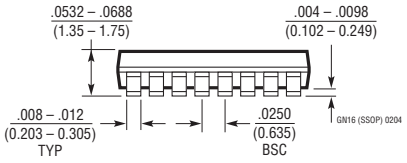
GN Package
16-Lead Plastic SSOP (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1641)



RECOMMENDED SOLDER PAD LAYOUT







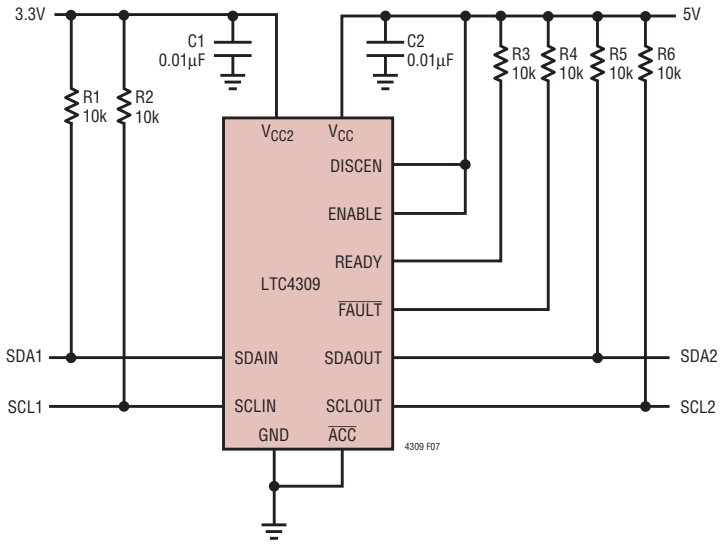
NOTE:
1. CONTROLLING DIMENSION: INCHES
2. DIMENSIONS ARE IN INCHES (MILLIMETERS)
3. DRAWING NOT TO SCALE

*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE
**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

TYPICAL APPLICATION

5V to 3.3V Level Translator



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1380/LTC1393	Single-Ended 8-Channel/Differential 4-Channel Analog MUX with SMBus Interface	Low R_{ON}: 35Ω Single Ended/70Ω Differential, Expandable to 32 Single or 16 Differential Channels
LTC1427-50	Micropower, 10-Bit Current Output DAC with SMBus Interface	Precision 50uA+/–2.5% Tolerance Over Temperature, 4 Selectable SMBus Addresses, DAC Powers up at Zero or Midscale
LTC1623	Dual High Side Switch Controller with SMBus Interface	8 Selectable Addresses/16 Channel Capability
LTC1663	SMBus Interface 10-Bit Rail to Rail Micropower DAC	DNL < 0.75 LSB Max, 5-Lead SOT-23 Package
LTC1694/LTC1694-1	SMBus Accelerator	Improved SMBus/I^{2}C Rise-Time, Ensures Data Integrity with Multiple SMBus/I^{2}C Devices
LTC1695	SMBus/I^{2}C Fan Speed Controller in ThinSOT™	0.75Ω PMOS 180mA Regulator, 6-Bit DAC
LT1786F	SMBus Controlled CCFL Switching Regulator	1.25A, 200kHz, Floating or Grounded Lamp Configurations
LTC1840	Dual I^{2}C Fan Speed Controller	Two 100µA 8-Bit DACs, Two Tach Inputs, Four GPIO
LTC4300A-1/ LTC4300A-2/ LTC4300A-3	Hot Swappable 2-Wire Bus Buffers	–1: Bus Buffer with READY, ACC and ENABLE –2: Dual Supply Bus Buffer with READY and ACC –3: Dual Supply Bus Buffer with READY and ENABLE
LTC4301	Supply Independent Hot Swappable 2-Wire Bus Buffer	Supply Independent
LTC4301L	Hot Swappable 2-Wire Bus Buffer with Low Voltage Level Translation	Allows Bus Pull-Up Voltages as Low as 1V on SDA_{IN} and SCL_{IN}
LTC4302-1/ LTC4302-2	Addressable 2-Wire Bus Buffer	Address Expansion, GPIO, Software Controlled
LTC4303 LTC4304	Hot Swappable 2-Wire Bus Buffer with Stuck Bus Recovery	Provides Automatic Clocking to Free Stuck I^{2}C Busses
LTC4305 LTC4306	2 or 4-Channel, 2 Wire Bus Multiplexers with Capacitance Buffering	2 or 4 Selectable Downstream Busses, Stuck Bus Disconnect, Rise Time Accelerators, Fault Reporting, ± 10kV HBM ESD Tolerance
LTC4307	Low Offset Hot Swappable 2-Wire Bus Buffer with Stuck Bus Recovery	60mV Buffer Offset, 30ms Stuck Bus Disconnect and Recovery, Rise Time Accelerators, ± 5kV HBM ESD Tolerance
LTC4307-1	High Definition Multimedia Interface (HDMI) Level Shifting 2-Wire Bus Buffer	60mV Buffer Offset, 3.3V to 5V Level Shifting, ± 5kV HBM ESD Tolerance

ThinSOT is a trademark of Linear Technology Corporation

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