# USB Power Manager with High Voltage Switching Charger

## FEATURES

- **Seamless Transition Between Power Sources: Li-Ion Battery, USB, and 6V to 36V External Supply**
- **High Efficiency 1.2A Charger from 6V to 36V Input with Adaptive Output Control**
- **3.95V Float Voltage Improves Battery Lifespan and High Temperature Safety Margin**
- **Load Dependent Charging from USB Input Guarantees Current Compliance**
- **215mΩ Internal Ideal Diode plus Optional External Ideal Diode Controller Provides Low Loss Power Path When External Supply/USB Not Present**
- Constant-Current/Constant-Voltage Operation with Thermal Feedback to Maximize Charging Rate without Risk of Overheating
- Selectable 100% or 20% Current Limit (e.g., 500mA/100mA) from USB Input
- Preset 3.95V Charge Voltage with ±0.8% Accuracy
- C/10 Charge Current Detection Output
- NTC Thermistor Input for Temperature Qualified Charging
- Tiny (6mm × 3mm × 0.75mm) 22-Lead DFN Package

## APPLICATIONS

- Portable USB Devices—GPS Receivers, Cameras, MP3 Players, PDAs

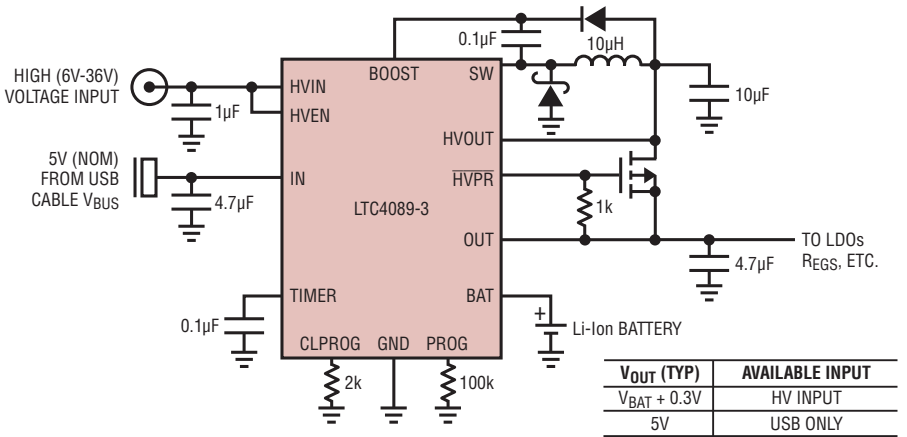
## DESCRIPTION

The LTC®4089-3 is a USB power manager plus high voltage Li-Ion battery charger. This device controls the total current used by the USB peripheral for operation and battery charging. Battery charge current is automatically reduced such that the sum of the load current and the charge current does not exceed the programmed input current limit. The LTC4089-3 also accommodates high voltage power supplies, such as 12V AC/DC wall adapters, Firewire, or automotive power.

The LTC4089-3 provides an adaptive output that tracks the battery voltage for high efficiency charging from the high voltage input. This 3.95V version of the the standard LTC4089 is intended for applications which have extended battery lifetime requirements or those that require high temperature (approximately >60°C) operation or storage. Under these conditions, a reduced float voltage will trade-off initial cell capacity for the benefit of increased capacity retention over the life of the battery. The charge current is programmable and an end-of-charge status output ($\overline{CHRG}$) indicates full charge. Also featured are programmable total charge time, an NTC thermistor input used to monitor battery temperature while charging and automatic recharging of the battery.

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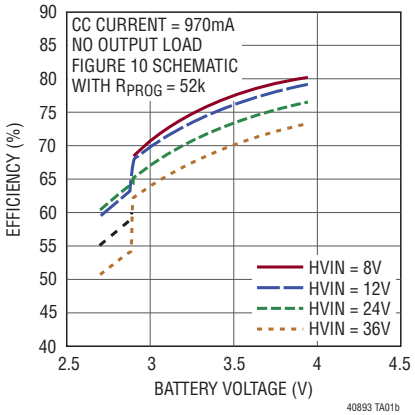
## TYPICAL APPLICATION




| $V_{OUT}$ (TYP) | AVAILABLE INPUT |
|---|---|
| $V_{BAT}$ + 0.3V | HV INPUT |
| 5V | USB ONLY |
| $V_{BAT}$ | BAT ONLY |

40893 TA01a

**LTC4089 High Voltage Battery Charger Efficiency**



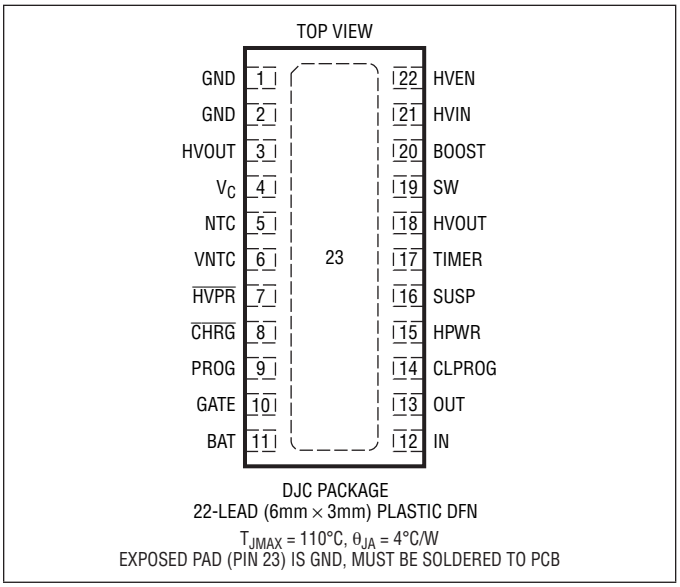

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## ABSOLUTE MAXIMUM RATINGS

**(Notes 1, 2, 3, 4, 5)**

Terminal Voltage
BOOST ..... –0.3V to 50V
BOOST above SW ..... 25V
HVIN, HVEN ..... –0.3V to 40V
IN, OUT, HVOUT
  t < 1ms and Duty Cycle < 1% ..... –0.3V to 7V
  DC ..... –0.3V to 6V
BAT ..... –0.3V to 6V
NTC, TIMER, PROG, CLPROG ..... –0.3V to ($V_{CC}$ + 0.3V)
$\overline{CHRG}$, HPWR, SUSP, $\overline{HVPR}$ ..... –0.3V to 6V
Pin Current, DC
IN, OUT, BAT (Note 6) ..... 2.5A
Operating Temperature Range ..... –40°C to 85°C
Maximum Operating Junction Temperature ..... 110°C
Storage Temperature Range ..... –65°C to 150°C

## PIN CONFIGURATION




DJC PACKAGE
22-LEAD (6mm × 3mm) PLASTIC DFN
$T_{JMAX}$ = 110°C, $\theta_{JA}$ = 4°C/W
EXPOSED PAD (PIN 23) IS GND, MUST BE SOLDERED TO PCB

## ORDER INFORMATION

http://www.linear.com/product/LTC4089-3#orderinfo

| LEAD FREE FINISH | TAPE AND REEL | PART MARKING | PACKAGE DESCRIPTION | TEMPERATURE RANGE |
|---|---|---|---|---|
| LTC4089EDJC-3#PBF | LTC4089EDJC-3#TRPBF | 40893 | 22-Lead (6mm × 3mm) Plastic DFN | –40°C to 85°C |

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

## LTC4089 OPTIONS

| PART NUMBER | FLOAT VOLTAGE | NTC HOT THRESHOLD | Bat-Track™ ADAPTIVE HV OUTPUT |
|---|---|---|---|
| LTC4089 | 4.2V | 29% $V_{VNTC}$ | Yes |
| LTC4089-1 | 4.1V | 32.6% $V_{VNTC}$ | No |
| LTC4089-3 | 3.95V | 32.6% $V_{VNTC}$ | Yes |
| LTC4089-5 | 4.2V | 29% $V_{VNTC}$ | No |

## ELECTRICAL CHARACTERISTICS

**The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C. HVIN = 12V, BOOST = 17V, $V_{IN}$ = 5V, $V_{BAT}$ = 3.7V, HVEN = 12V, HPWR = 5V, $R_{PROG}$ = 100k, $R_{CLPROG}$ = 2k, SUSP = 0V, unless otherwise noted.**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **USB Input Current Limit** | | | | | | | |
| $V_{IN}$ | USB Input Supply Voltage | IN | ● | 4.35 | | 5.5 | V |
| $I_{IN}$ | Input Bias Current | $I_{BAT}$ = 0 (Note 7)<br>Suspend Mode; SUSP = 5V | ●<br>● | | 0.5<br>50 | 1<br>100 | mA<br>µA |

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| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $I_{LIM}$ | Current Limit | $R_{CLPROG}$ = 2k, HPWR = 5V<br>$R_{CLPROG}$ = 2k, HPWR = 0V | ●<br>● | 475<br>90 | 500<br>100 | 525<br>110 | mA<br>mA |
| $I_{IN(MAX)}$ | Maximum Input Current Limit | (Note 8) | | | 2.4 | | A |
| $R_{ON}$ | ON Resistance $V_{IN}$ to $V_{OUT}$ | $I_{OUT}$ = 80mA Load | | | 0.215 | | Ω |
| $V_{CLPROG}$ | CLPROG Pin Voltage | $R_{CLPROG}$ = 2k<br>$R_{CLPROG}$ = 1k | ●<br>● | 0.98<br>0.98 | 1.00<br>1.00 | 1.02<br>1.02 | V<br>V |
| $I_{SS}$ | Soft-Start Inrush Current | IN | | | 5 | | mA/µs |
| $V_{CLEN}$ | Input Current Limit Enable Threshold Voltage ($V_{IN}$ – $V_{OUT}$) | ($V_{IN}$ – $V_{OUT}$) $V_{IN}$ Rising<br>($V_{IN}$ – $V_{OUT}$) $V_{IN}$ Falling | | 20<br>–80 | 50<br>–50 | 80<br>–20 | mV<br>mV |
| $V_{UVLO}$ | Input Undervoltage Lockout | $V_{IN}$ Powers Part, Rising Threshold | ● | 3.6 | 3.8 | 4 | V |
| $dV_{UVLO}$ | Input Undervoltage Lockout Hysteresis | $V_{IN}$ Rising – $V_{IN}$ Falling | | | 130 | | mV |
| **High Voltage Regulator** | | | | | | | |
| $V_{HVIN}$ | HVIN Supply Voltage | | | 6 | | 36 | V |
| $I_{HVIN}$ | HVIN Bias Current | Not Switching<br>Shutdown; HVEN = 0V | | | 1.9<br>0.01 | 2.5<br>2 | mA<br>µA |
| $V_{OUT}$ | Output Voltage with HVIN Present | Assumes HVOUT to OUT Connection | | 3.45 | $V_{BAT}$+0.3 | 4.6 | V |
| $V_{HVUVLO}$ | High Voltage Input Undervoltage Lockout | $V_{HVIN}$ Rising | | | 4.7 | 5 | V |
| $f_{SW}$ | Switching Frequency | $V_{HVOUT}$ > 3.95V<br>$V_{HVOUT}$ = 0V | | 685 | 750<br>35 | 815 | kHz<br>kHz |
| $DC_{MAX}$ | Maximum Duty Cycle | | ● | 88 | 95 | | % |
| $I_{SW(MAX)}$ | Switch Current Limit | (Note 9) | | 1.5 | 1.95 | 2.3 | A |
| $V_{SAT}$ | Switch $V_{CESAT}$ | $I_{SW}$ = 1A | | | 330 | | mV |
| $I_{LK}$ | Switch Leakage Current | | | | | 2 | µA |
| $V_{SWD}$ | Minimum Boost Voltage Above SW | $I_{SW}$ = 1A | | | 1.85 | 2.2 | V |
| $I_{BST}$ | BOOST Pin Current | $I_{SW}$ = 1A | | | 30 | 50 | mA |
| **Battery Management** | | | | | | | |
| $V_{BAT}$ | Input Voltage | BAT | | | | 4.3 | V |
| $I_{BAT}$ | Battery Drain Current | $V_{BAT}$ = 4.05V, Charging Stopped<br>Suspend Mode; SUSP = 5V<br>$V_{HVIN}$ = $V_{IN}$ = 0V, BAT Powers OUT, No Load | ●<br>●<br>● | | 15<br>22<br>60 | 27<br>35<br>100 | µA<br>µA<br>µA |
| $V_{FLOAT}$ | Regulated Output Voltage | $I_{BAT}$ = 2mA<br>$I_{BAT}$ = 2mA; (0°C – 85°C) | | 3.915<br>3.910 | 3.95<br>3.95 | 3.985<br>3.990 | V<br>V |
| $I_{CHG}$ | Current Mode Charge Current | $R_{PROG}$ = 100k, No Load<br>$R_{PROG}$ = 50k, No Load; (0°C – 85°C) | ● | 465<br>900 | 500<br>1000 | 535<br>1080 | mA<br>mA |
| $I_{CHG(MAX)}$ | Maximum Charge Current | (Note 8) | | | 1.2 | | A |
| $V_{PROG}$ | PROG Pin Voltage | $R_{PROG}$ = 100k<br>$R_{PROG}$ = 50k | ●<br>● | 0.98<br>0.98 | 1.00<br>1.00 | 1.02<br>1.02 | V<br>V |
| $k_{EOC}$ | Ratio of End-of-Charge Current to Charge Current | $V_{BAT}$ = $V_{FLOAT}$ (3.95V) | ● | 0.085 | 0.1 | 0.11 | mA/mA |
| $I_{TRIKL}$ | Trickle Charge Current | $V_{BAT}$ = 2V, $R_{PROG}$ = 100k | | 35 | 50 | 60 | mA |
| $V_{TRIKL}$ | Trickle Charge Threshold Voltage | | ● | 2.75 | 2.9 | 3 | V |
| $V_{CEN}$ | Charger Enable Threshold Voltage | ($V_{OUT}$ – $V_{BAT}$) Falling; $V_{BAT}$ = 4V<br>($V_{OUT}$ – $V_{BAT}$) Rising; $V_{BAT}$ = 4V | | | 55<br>80 | | mV<br>mV |
| $V_{RECHRG}$ | Recharge Battery Threshold Voltage | $V_{FLOAT}$ – $V_{RECHRG}$ | ● | 60 | 95 | 130 | mV |
| $t_{TIMER}$ | TIMER Accuracy | $V_{BAT}$ = 4.05V | | –10 | | 10 | % |
| | Recharge Time | Percent of Total Charge Time | | | 50 | | % |

## ELECTRICAL CHARACTERISTICS

**The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C. HVIN = 12V, BOOST = 17V, $V_{IN}$ = 5V, $V_{BAT}$ = 3.7V, HVEN = 12V, HPWR = 5V, $R_{PROG}$ = 100k, $R_{CLPROG}$ = 2k, SUSP = 0V, unless otherwise noted.**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| | Low Battery Trickle Charge Time | Percent of Total Charge Time, $V_{BAT}$ < 2.8V | | | 25 | | % |
| $T_{LIM}$ | Junction Temperature in Constant Temperature Mode | | | | 105 | | °C |
| **Internal Ideal Diode** | | | | | | | |
| $R_{FWD}$ | Incremental Resistance, $V_{ON}$ Regulation | $I_{BAT}$ = 100mA | | | 125 | | mΩ |
| $R_{DIO(ON)}$ | ON Resistance $V_{BAT}$ to $V_{OUT}$ | $I_{BAT}$ = 600mA | | | 215 | | mΩ |
| $V_{FWD}$ | Voltage Forward Drop ($V_{BAT}$ - $V_{OUT}$) | $I_{BAT}$ = 5mA<br>$I_{BAT}$ = 100mA<br>$I_{BAT}$ = 600mA | ● | 10 | 30<br>55<br>160 | 50 | mV<br>mV<br>mV |
| $V_{OFF}$ | Diode Disable Battery Voltage | | | | 2.8 | | V |
| $I_{FWD}$ | Load Current Limit, for $V_{ON}$ Regulation | | | | 550 | | mA |
| $I_{D(MAX)}$ | Diode Current Limit | | | | 2.2 | | A |
| **External Ideal Diode** | | | | | | | |
| $V_{FWD(EXT)}$ | External Diode Forward Voltage | | | | 20 | | mV |
| **Logic** | | | | | | | |
| $V_{OL}$ | Output Low Voltage ($\overline{CHRG}$, $\overline{HVPR}$) | $I_{SINK}$ = 5mA | ● | | 0.1 | 0.4 | V |
| $V_{IH}$ | Input High Voltage | HVEN, SUSP, HPWR Pin Low to High | | 2.3 | | | V |
| $V_{IL}$ | Input Low Voltage | HVEN, SUSP, HPWR Pin High to Low | | | | 0.3 | V |
| $I_{PULLDN}$ | Logic Input Pull Down Current | SUSP, HPWR | | | 2 | | µA |
| $I_{HVEN}$ | HVEN Pin Bias Current | $V_{HVEN}$ = 2.3V<br>$V_{HVEN}$ = 0V | | | 6<br>0.01 | 20<br>0.1 | µA<br>µA |
| $V_{CHG(SD)}$ | Charger Shutdown Threshold Voltage on TIMER | | ● | 0.14 | | 0.4 | V |
| $I_{CHG(SD)}$ | Charger Shutdown Pull-Up Current on TIMER | $V_{TIMER}$ = 0V | ● | 5 | 14 | | µA |
| **NTC** | | | | | | | |
| $I_{VNTC}$ | VNTC Pin Current | $V_{VNTC}$ = 2.5V | | 1.4 | 2.5 | 3.5 | mA |
| $V_{VNTC}$ | VNTC Bias Voltage | $I_{VNTC}$ = 500µA | ● | 4.4 | 4.85 | | V |
| $I_{NTC}$ | NTC Input Leakage Current | $V_{NTC}$ = 1V | | | 0 | ±1 | µA |
| $V_{COLD}$ | Cold Temperature Fault Threshold Voltage | Rising Threshold<br>Hysteresis | | | 0.738•$V_{VNTC}$<br>0.018•$V_{VNTC}$ | | V<br>V |
| $V_{HOT}$ | Hot Temperature Fault Threshold Voltage | Falling Threshold<br>Hysteresis | | | 0.326•$V_{VNTC}$<br>0.015•$V_{VNTC}$ | | V<br>V |
| $V_{DIS}$ | NTC Disable Voltage | NTC Input Voltage to GND (Falling)<br>Hysteresis | ● | 75 | 100<br>35 | 125 | mV<br>mV |

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** $V_{CC}$ is the greater of $V_{IN}$, $V_{OUT}$ or $V_{BAT}$

**Note 3:** All voltage values are with respect to GND.

**Note 4:** This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperatures will exceed 110°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may result in device degradation or failure.

**Note 5:** The LTC4089-3 is guaranteed to meet specified performance from 0°C to 85°C and are designed, characterized and expected to meet these extended temperature limits, but are not tested at –40°C and 85°C.

**Note 6:** Guaranteed by long term current density limitations.

**Note 7:** Total input current is equal to this specification plus 1.002 • $I_{BAT}$ where $I_{BAT}$ is the charge current.

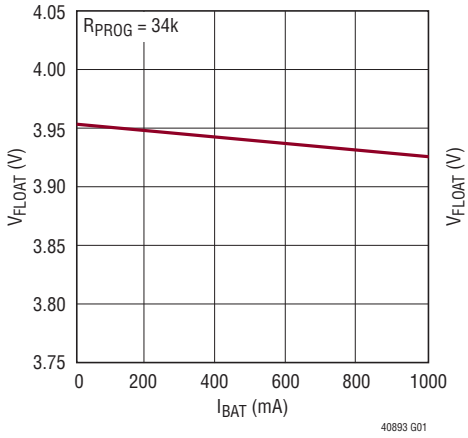
**Note 8:** Accuracy of programmed current may degrade for currents greater than 1.5A.

**Note 9:** Current limit guaranteed by design and/or correlation to static test. Slope compensation reduces current limit at high duty cycle.

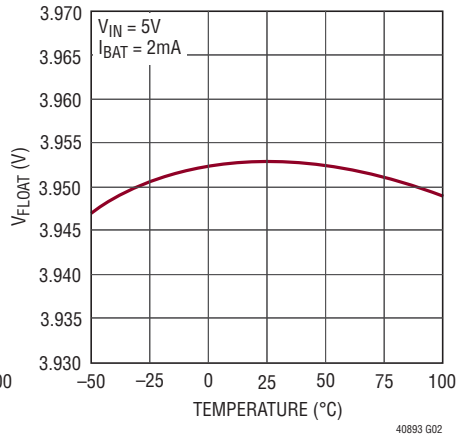
## TYPICAL PERFORMANCE CHARACTERISTICS

$T_A$ = 25°C, unless otherwise specified.

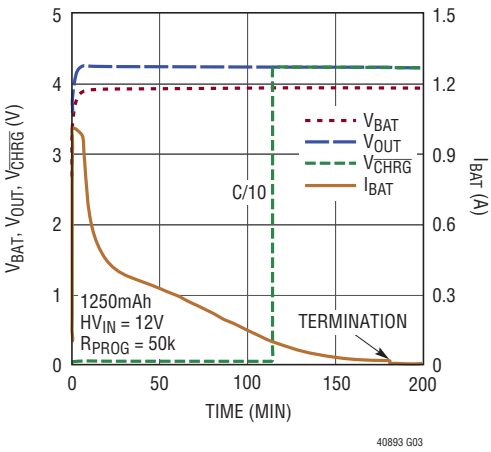
### $V_{FLOAT}$ Load Regulation



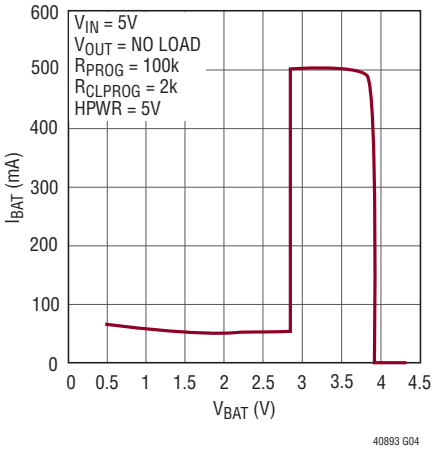

### Battery Regulation (Float) Voltage vs Temperature



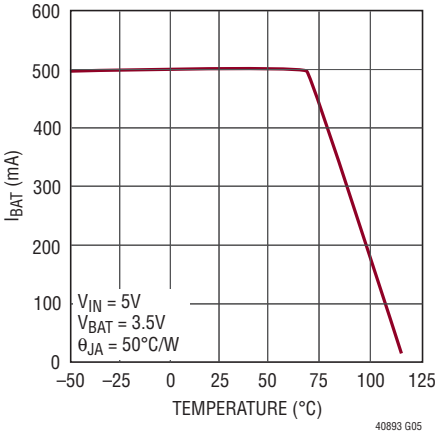

### Battery Current and Voltage vs Time



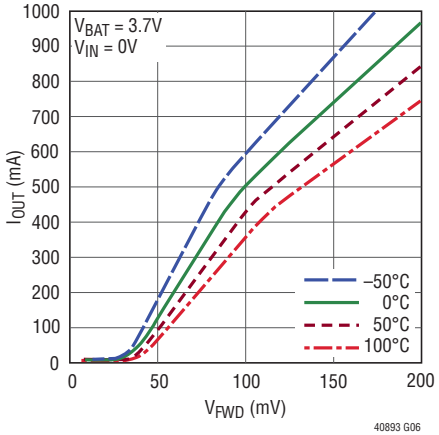

### Charging from USB, $I_{BAT}$ vs $V_{BAT}$



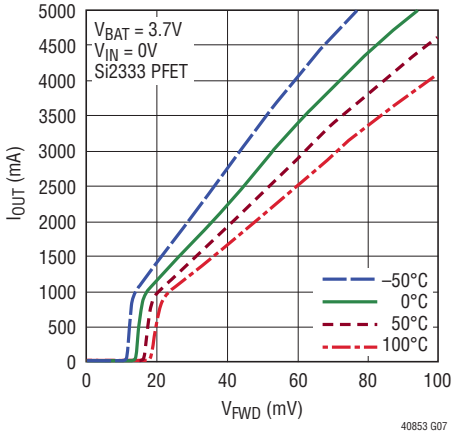

### Charge Current vs Temperature (Thermal Regulation)



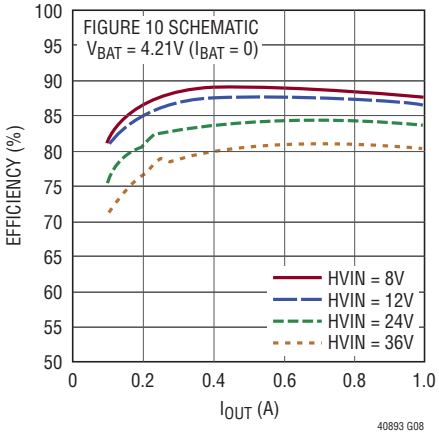

### Ideal Diode Current vs Forward Voltage and Temperature (No External Device)




### Ideal Diode Current vs Forward Voltage and Temperature with External Device

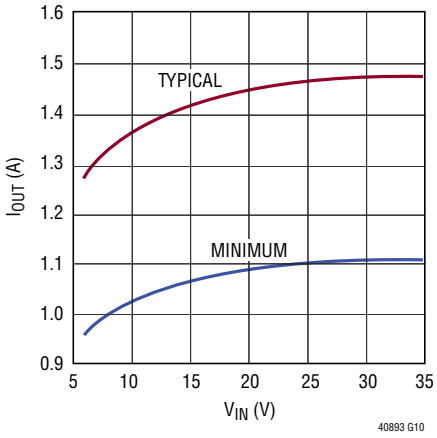



### High Voltage Regulator Efficiency vs Output Load

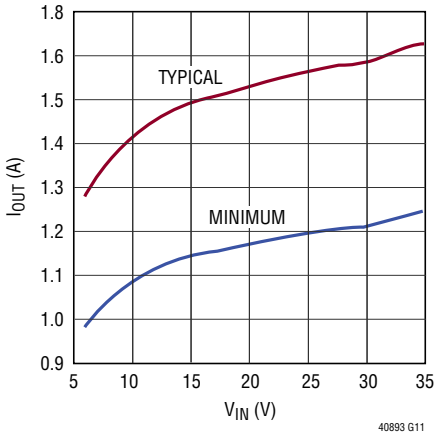


## TYPICAL PERFORMANCE CHARACTERISTICS $T_A$ = 25°C, unless otherwise specified.

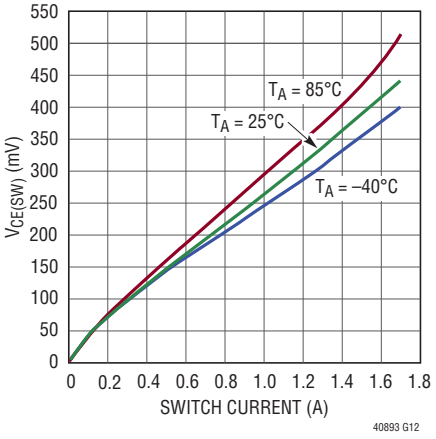
### High Voltage Regulator Maximum Load Current, L = 10µH



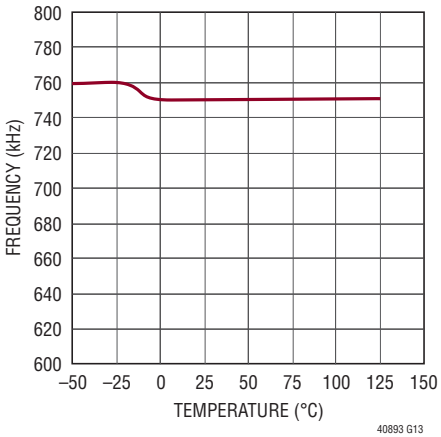

### High Voltage Regulator Maximum Load Current, L = 33µH



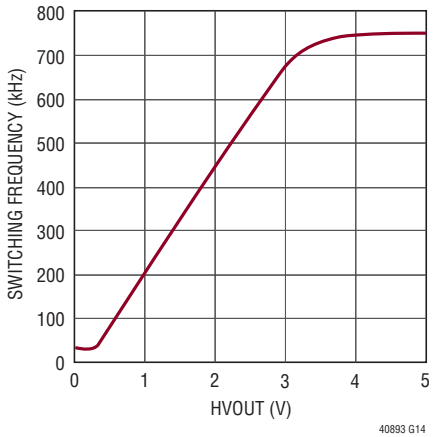

### High Voltage Regulator Switch Voltage Drop



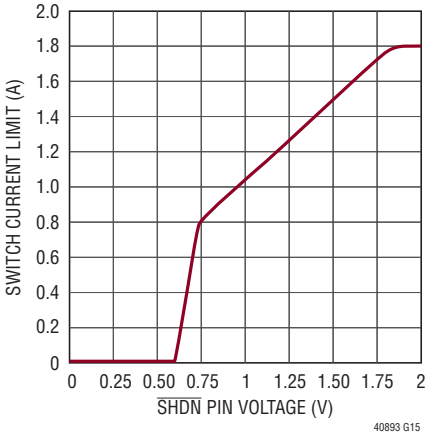

### High Voltage Regulator Switch Frequency



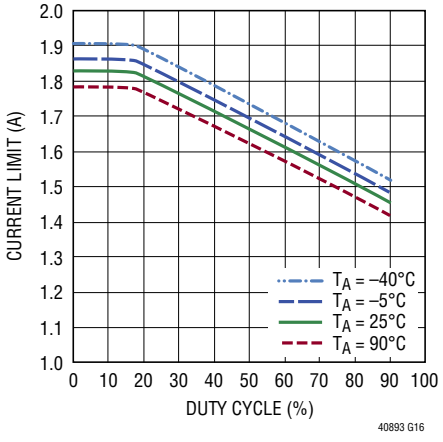

### High Voltage Regulator Frequency Foldback



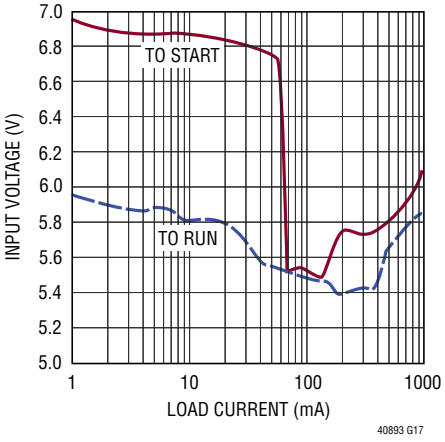

### High Voltage Regulator Soft-Start




### High Voltage Switch Current Limit

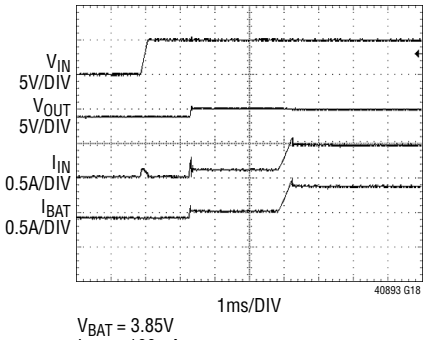



### High Voltage Regulator Typical Minimum Input Voltage



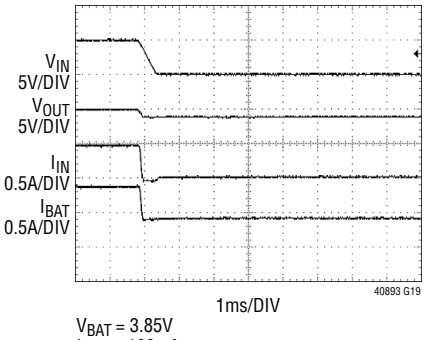
## TYPICAL PERFORMANCE CHARACTERISTICS $T_A$ = 25°C, unless otherwise specified.

### Input Connect Waveforms



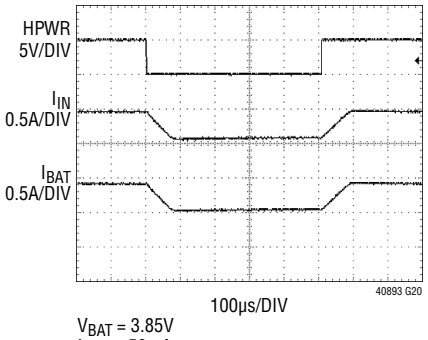

$V_{BAT}$ = 3.85V
$I_{OUT}$ = 100mA

### Input Disconnect Waveforms



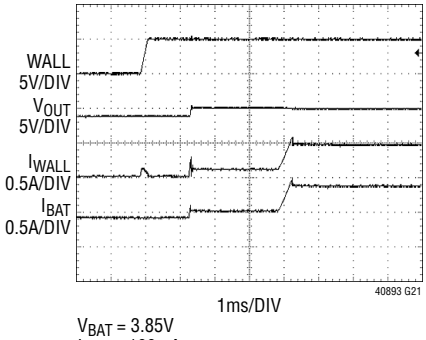

$V_{BAT}$ = 3.85V
$I_{OUT}$ = 100mA

### Response to HPWR



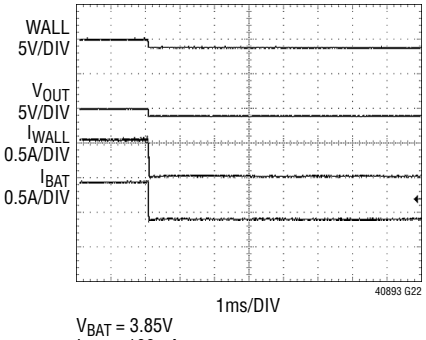

$V_{BAT}$ = 3.85V
$I_{OUT}$ = 50mA

### Wall Connect Waveforms



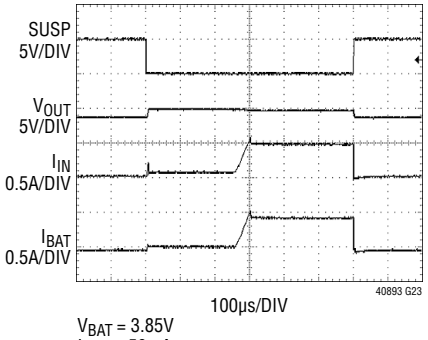

$V_{BAT}$ = 3.85V
$I_{OUT}$ = 100mA
$R_{PROG}$ = 100k

### Wall Disconnect Waveforms



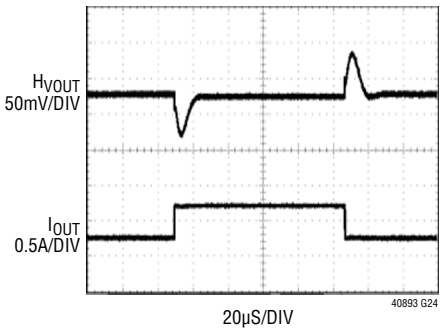

$V_{BAT}$ = 3.85V
$I_{OUT}$ = 100mA
$R_{PROG}$ = 100k

### Response to Suspend

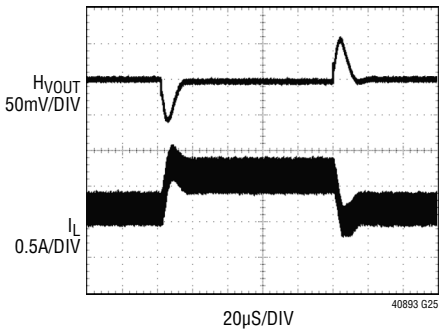



$V_{BAT}$ = 3.85V
$I_{OUT}$ = 50mA

### High Voltage Regulator Load Transient




### High Voltage Regulator Load Transient



## PIN FUNCTIONS

**GND (Pins 1, 2, Exposed Pad Pin 23):** Ground. Tie the GND pin to a local ground plane below the LTC4089-3 and the circuit components. The exposed package pad is ground and must be soldered to the PC board for proper functionality and for maximum heat transfer (use several vias directly under the LTC4089-3).

**HVOUT (Pins 3, 18)**: Voltage Output of the High Voltage Regulator. When sufficient voltage is present at HVOUT, the low voltage power path from IN to OUT will be disconnected and the $\overline{HVPR}$ pin will be pulled low to indicate that a high voltage wall adapter has been detected. The LTC4089-3 high voltage regulator will maintain just enough differential voltage between HVOUT and BAT to keep the battery charger MOSFET out of dropout (typically 300mV from OUT to BAT). HVOUT should be bypassed with at least 10µF to GND. **Connect Pins 3 and 18 with a resistance no greater than 1Ω.**

**$V_C$ (Pin 4):** Leave the $V_C$ pin floating or bypass to ground with a 10pF capacitor. This optional 10pF capacitor reduces HVOUT ripple in discontinuous mode.

**NTC (Pin 5):** Input to the NTC Thermistor Monitoring Circuit. The NTC pin connects to a negative temperature coefficient thermistor which is typically co-packaged with the battery pack to determine if the battery is too hot or too cold to charge. If the battery temperature is out of range, charging is paused until the battery temperature re-enters the valid range. A low drift bias resistor is required from IN to NTC and a thermistor is required from NTC to ground. To disable the NTC function, the NTC pin should be grounded.

Connect the NTC pin to ground to disable this feature. This will disable all of the LTC4089-3 NTC functions.

**VNTC (Pin 6):** Output Bias Voltage for NTC. A resistor from this pin to the NTC pin will bias the NTC thermistor.

**$\overline{HVPR}$ (Pin 7):** High Voltage Present Output. Active low open-drain output pin. A low on this pin indicates that the high voltage regulator has sufficient voltage to charge the battery. This feature is disabled if no power is present on HVIN, IN or BAT (i.e., below UVLO thresholds).

**$\overline{CHRG}$ (Pin 8):** Open-Drain Charge Status Output. When the battery is being charged, the $\overline{CHRG}$ pin is pulled low by an internal N-channel MOSFET. When the timer runs out or the charge current drops below 10% of the programmed charge current or the input supply is removed, the $\overline{CHRG}$ pin is forced to a high impedance state.

**PROG (Pin 9):** Charge Current Program. Connecting a resistor, $R_{PROG}$, to ground programs the battery charge current. The battery charge current is programmed as follows:

$$I_{CHG}(A) = \frac{50,000V}{R_{PROG}}$$

**GATE (Pin 10):** External Ideal Diode Gate Pin. This pin can be used to drive the gate of an optional external PFET connected between BAT (drain) and OUT (source). By doing so, the impedance of the ideal diode between BAT and OUT can be reduced. When not in use, this pin should be left floating. It is important to maintain a high impedance on this pin and minimize all leakage paths.

**BAT (Pin 11):** Connect to a single cell Li-Ion battery. This pin is used as an output when charging the battery and as an input when supplying power to OUT. When the OUT pin potential drops below the BAT pin potential, an ideal diode function connects BAT to OUT and prevents $V_{OUT}$ from dropping more than 100mV below $V_{BAT}$. A precision internal resistor divider sets the final float (charging) potential on this pin. The internal resistor divider is disconnected when IN and HVIN are in undervoltage lockout.

**IN (Pin 12):** Input Supply. Connect to USB supply, $V_{BUS}$. Input current to this pin is limited to either 20% or 100% of the current programmed by the CLPROG pin as determined by the state of the HPWR pin. Charge current (to the BAT pin) supplied through the input is set to the current programmed by the PROG pin but will be limited by the input current limit if charge current is set greater than the input current limit.

## PIN FUNCTIONS

**OUT (Pin 13):** Voltage Output. This pin is used to provide controlled power to a USB device from either USB $V_{BUS}$ (IN), an external high voltage supply (HVIN), or the battery (BAT) when no other supply is present. The high voltage supply is prioritized over the USB $V_{BUS}$ input. OUT should be bypassed with at least 4.7µF to GND.

**CLPROG (Pin 14):** Current Limit Program and Input Current Monitor. Connecting a resistor, $R_{CLPROG}$, to ground programs the input to output current limit. The current limit is programmed as follows:

$$I_{CL}(A) = \frac{1000V}{R_{CLPROG}}$$

In USB applications, the resistor $R_{CLPROG}$ should be set to no less than 2.1k. The voltage on the CLPROG pin is always proportional to the current flowing through the IN to OUT power path. This current can be calculated as follows:

$$I_{IN}(A) = \frac{V_{CLPROG}}{R_{CLPROG}} \bullet 1000$$

**HPWR (Pin 15):** High Power Select. This logic input is used to control the input current limit. A voltage greater than 2.3V on the pin will set the input current limit to 100% of the current programmed by the CLPROG pin. A voltage less than 0.3V on the pin will set the input current limit to 20% of the current programmed by the CLPROG pin. A 2µA pull-down current is internally connected to this pin to ensure it is low at power up when the pin is not being driven externally.

**SUSP (Pin 16):** Suspend Mode Input. Pulling this pin above 2.3V will disable the power path from IN to OUT. The supply current from IN will be reduced to comply with the USB specification for suspend mode. Both the ability to charge the battery from HVIN and the ideal diode function (from BAT to OUT) will remain active. Suspend mode will reset the charge timer if $V_{OUT}$ is less than $V_{BAT}$ while in suspend mode. If $V_{OUT}$ is kept greater than $V_{BAT}$, such as when the high voltage input is present, the charge timer will not be reset when the part is put in suspend. A 2µA pull-down current is internally applied to this pin to ensure it is low at power-up when the pin is not being driven externally.

**TIMER (Pin 17):** Timer Capacitor. Placing a capacitor, $C_{TIMER}$, to GND sets the timer period. The timer period is:

$$t_{TIMER}(hours) = \frac{C_{TIMER} \bullet R_{PROG} \bullet 3hours}{0.1\mu F \bullet 100k}$$

Charge time is increased if charge current is reduced due to undervoltage current limit, load current, thermal regulation and current limit selection (HPWR).

Shorting the TIMER pin to GND disables the battery charging functions.

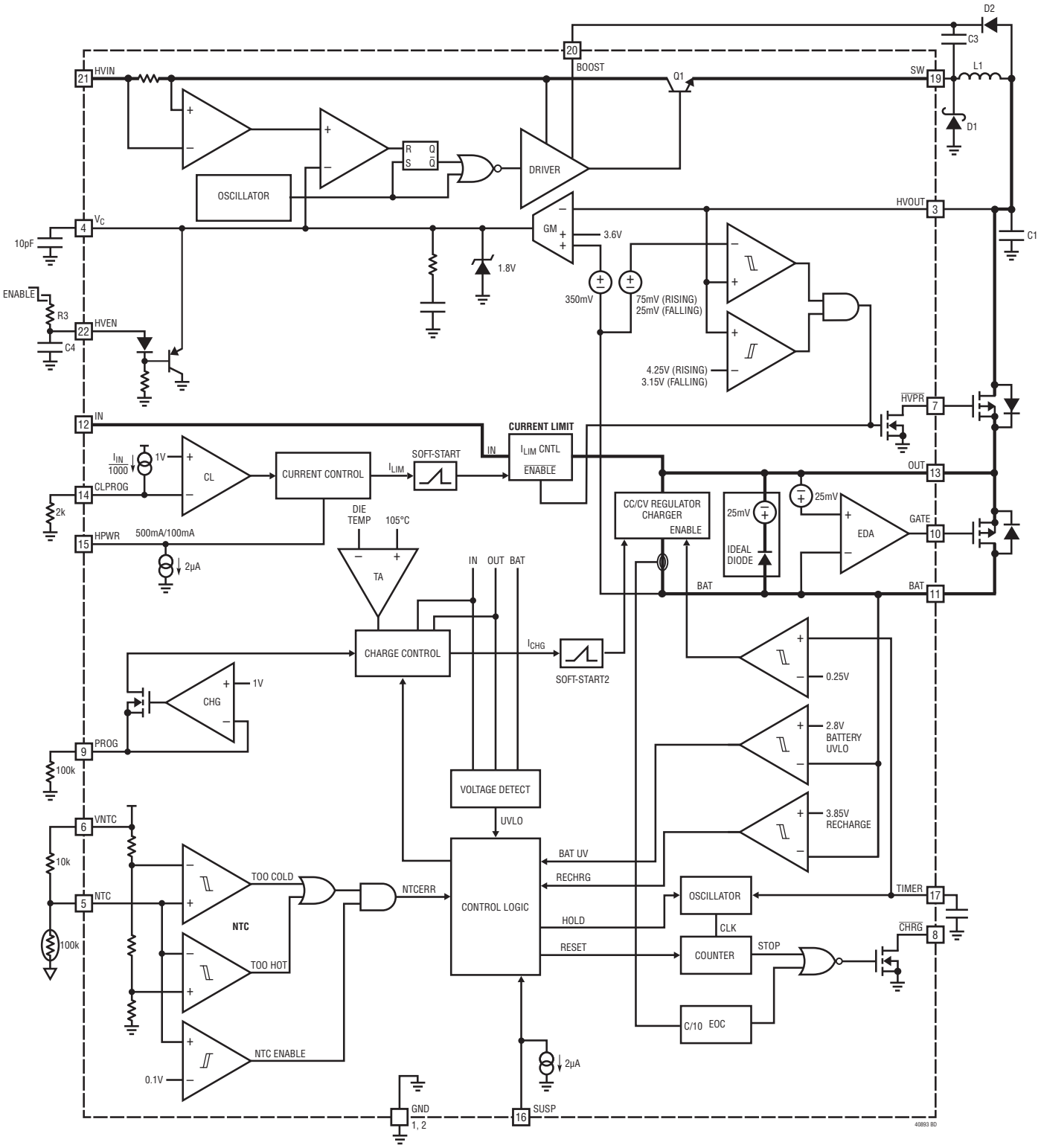
**SW (Pin 19):** The SW pin is the output of the internal high voltage power switch. Connect this pin to the inductor, catch diode and boost capacitor.

**BOOST (Pin 20):** The BOOST pin is used to provide a drive voltage, higher than the input voltage, to the internal bipolar NPN power switch.

**HVIN (Pin 21):** The HVIN pin supplies current to the internal high voltage regulator and to the internal high voltage power switch. The presence of a high voltage input takes priority over the USB $V_{BUS}$ input (i.e., when a high voltage input supply is detected, the USB IN to OUT path is disconnected). This pin must be locally bypassed.

**HVEN (Pin 22):** The HVEN pin is used to disable the high voltage input path. Tie to ground to disable the high voltage input or tie to at least 2.3V to enable the high voltage path. If this feature is not used, tie to the HVIN pin. This pin can also be used to soft-start the high voltage regulator; see the Applications Information section.

## BLOCK DIAGRAM



## OPERATION (Refer to Block Diagram)

The LTC4089-3 is a complete PowerPath™ controller for battery-powered USB applications. The LTC4089-3 is designed to receive power from a low voltage source (e.g., USB or 5V wall adapter), a high voltage source (e.g., Firewire/IEEE1394, automotive battery, 12V wall adapter, etc.), and a single-cell Li-Ion battery. It can then deliver power to an application connected to the OUT pin and a battery connected to the BAT pin (assuming that an external supply other than the battery is present). Power supplies that have limited current resources (such as USB $V_{BUS}$ supplies) should be connected to the IN pin which has a programmable current limit. Battery charge current will be adjusted to ensure that the sum of the charge current and load current does not exceed the programmed input current limit (see Figure 1).

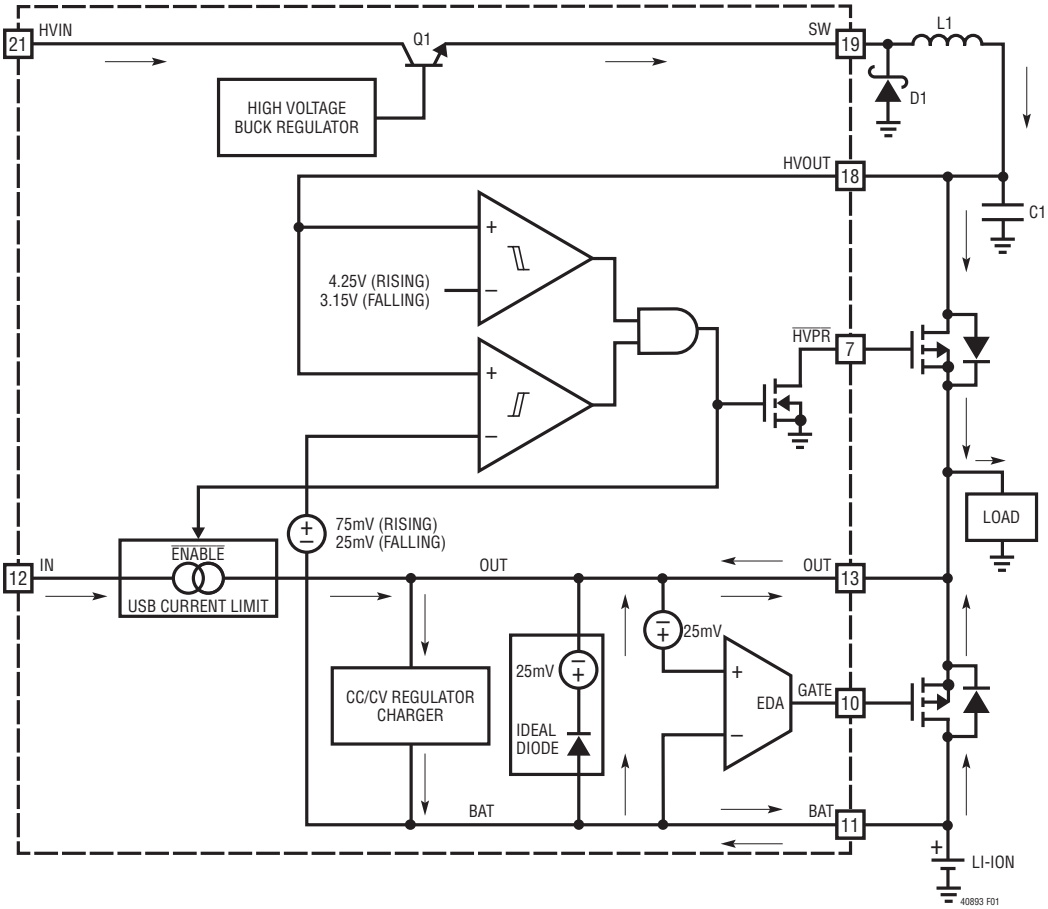



**Figure 1. Simplified PowerPath Block Diagram**

## OPERATION

An ideal diode function provides power from the battery when output / load current exceeds the input current limit or when input power is removed. Powering the load through the ideal diode instead of connecting the load directly to the battery allows a fully charged battery to remain fully charged until external power is removed. Once external power is removed the output drops until the ideal diode is forward biased. The forward biased ideal diode will then provide the output power to the load from the battery.

The LTC4089-3 also includes a high voltage switching regulator which has the ability to receive power from a high voltage input. This input takes priority over the USB $V_{BUS}$ input (i.e., if both HVIN and IN are present, load current and charge current will be delivered via the high voltage path). When enabled, the high voltage regulator regulates the HVOUT voltage using a 750kHz constant frequency, current mode regulator. An external PFET between HVOUT (drain) and OUT (source) is turned on via the $\overline{HVPR}$ pin allowing OUT to charge the battery and/or supply power to the application. The LTC4089-3 maintains approximately 300mV between the OUT pin and the BAT pin.

### Input Current Limit

Whenever the input power path is enabled (i.e., SUSP = 0V and HVIN = 0V) and power is available at IN, power is delivered to OUT. The current limit and charger control circuits of the LTC4089-3 are designed to limit input current as well as control battery charge current as a function of $I_{OUT}$. The input current limit, $I_{CL}$, can be programmed using the following formula:

$$I_{CL} = \left[\frac{1000}{R_{CLPROG}} \bullet V_{CLPROG}\right] = \frac{1000V}{R_{CLPROG}}$$

where $V_{CLPROG}$ is the CLPROG pin voltage (typically 1V) and $R_{CLPROG}$ is the total resistance from the CLPROG pin to ground. For best stability over temperature and time, 1% metal film resistors are recommended.

The programmed battery charge current, $I_{CHG}$, is defined as:

$$I_{CHG} = \left[\frac{50,000}{R_{PROG}} \bullet V_{PROG}\right] = \frac{50,000V}{R_{PROG}}$$

Input current, $I_{IN}$, is equal to the sum of the BAT pin output current and the OUT pin output current. $V_{CLPROG}$ will typically servo to 1V, however, if $I_{OUT} + I_{BAT} < I_{CL}$ then $V_{CLPROG}$ will track the input current according to the following equation:

$$I_{IN} = I_{OUT} + I_{BAT} = \frac{V_{CLPROG}}{R_{CLPROG}} \bullet 1000$$

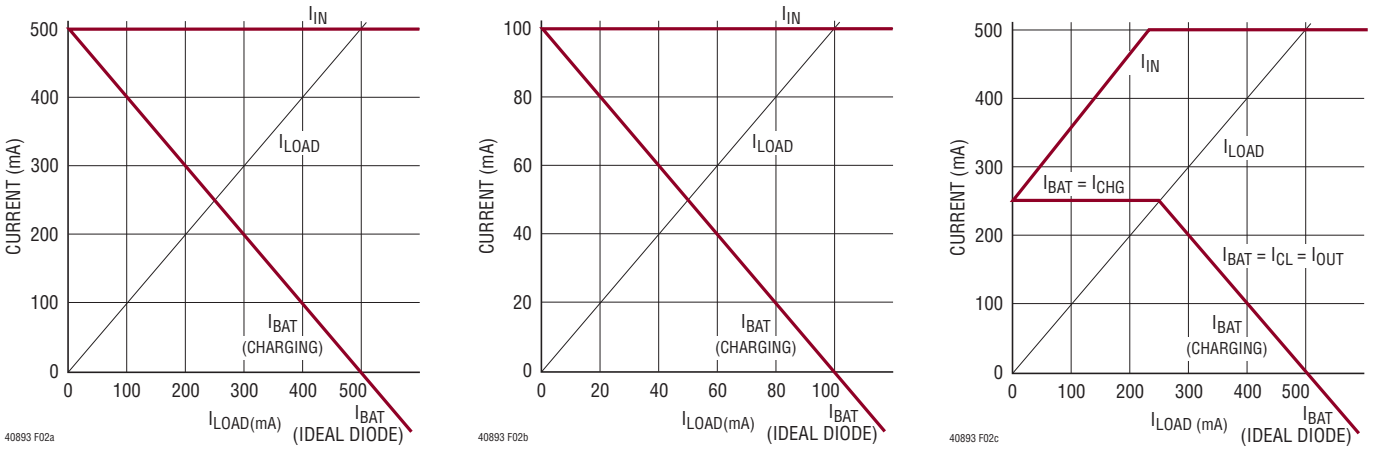
## OPERATION

The current limiting circuitry in the LTC4089-3 can and should be configured to limit current to 500mA for USB applications (selectable using the HPWR pin and programmed using the CLPROG pin).

The LTC4089-3 reduces battery charge current such that the sum of the battery charge current and the load current does not exceed the programmed input current limit (one-fifth of the programmed input current limit when HPWR is low, see Figure 2). The battery charge current goes to zero when load current exceeds the programmed input current limit (one-fifth of the limit when HPWR is low). Even if the battery charge current is set to exceed the allowable USB current, the USB specification will not be violated. The battery charger will reduce its current as needed to ensure that the USB specification is not exceeded. If the load current is greater than the current limit, the output voltage will drop to just under the battery voltage where the ideal diode circuit will take over and the excess load current will be drawn from the battery.

In USB applications, the minimum value for $R_{CLPROG}$ should be 2.1k. This will prevent the input current from exceeding 500mA due to LTC4089-3 tolerances and quiescent currents. A 2.1k CLPROG resistor will give a typical current limit of 476mA in high power mode (HPWR = 1) or 95mA in low power mode (HPWR = 0).

When SUSP is driven to a logic high, the input power path is disabled and the ideal diode from BAT to OUT will supply power to the application.




**(a) High Power Mode/Full Charge $R_{PROG}$ = 100k and $R_{CLPROG}$ = 2k**

**(b) Low Power Mode/Full Charge $R_{PROG}$ = 100k and $R_{CLPROG}$ = 2k**

**(c) High Power Mode with $I_{CL}$ = 500mA and $I_{CHG}$ = 250mA $R_{PROG}$ = 200k and $R_{CLPROG}$ = 2k**

**Figure 2. Input and Battery Currents as a Function of Load Current**

## OPERATION

### High Voltage Step Down Regulator

The power delivered from HVIN to HVOUT is controlled by a 750kHz constant frequency, current mode step down regulator. An external P-channel MOSFET directs this power to OUT and prevents reverse conduction from OUT to HVOUT (and ultimately HVIN).

A 750kHz oscillator enables an RS flip-flop, turning on the internal 1.95A power switch Q1. An amplifier and comparator monitor the current flowing between the HVIN and SW pins, turning the switch off when this current reaches a level determined by the voltage at $V_C$. An error amplifier servos the $V_C$ node to maintain approximately 300mV between OUT and BAT. By keeping the voltage across the battery charger low, efficiency is optimized because power lost to the battery charger is minimized and power available to the external load is maximized. If the BAT pin voltage is less than approximately 3.3V, then the error amplifier will servo the $V_C$ node to provide a constant HVOUT output voltage of about 3.6V. An active clamp on the $V_C$ node provides current limit. The $V_C$ node is also clamped to the voltage on the HVEN pin; soft-start is implemented by a voltage ramp at the HVEN pin using an external resistor and capacitor.

An internal regulator provides power to the control circuitry. This regulator includes an undervoltage lockout to prevent switching when HVIN is less than about 4.7V. The HVEN pin is used to disable the high voltage regulator. HVIN input current is reduced to less than 2µA and the external P-channel MOSFET disconnects HVOUT from OUT when the high voltage regulator is disabled.

The switch driver operates from either the high voltage input or from the BOOST pin. An external capacitor and diode are used to generate a voltage at the BOOST pin that is higher than the input supply. This allows the driver to fully saturate the internal bipolar NPN power switch for efficient operation.

When HVOUT is below 3.95V the operating frequency is reduced. This frequency foldback helps to control the regulator output current during start-up and overload.

### Ideal Diode from BAT to OUT

The LTC4089-3 has an internal ideal diode as well as a controller for an optional external ideal diode. If a battery is the only power supply available, or if the load current exceeds the programmed input current limit, then the battery will automatically deliver power to the load via an ideal diode circuit between the BAT and OUT pins. The ideal diode circuit (along with the recommended 4.7µF capacitor on the OUT pin) allows the LTC4089-3 to handle large transient loads and wall adapter or USB $V_{BUS}$ connect/disconnect scenarios without the need for large bulk capacitors. The ideal diode responds within a few microseconds and prevents the OUT pin voltage from dropping significantly below the BAT pin voltage. A comparison of the I-V curve of the ideal diode and a Schottky diode can be seen in Figure 3.

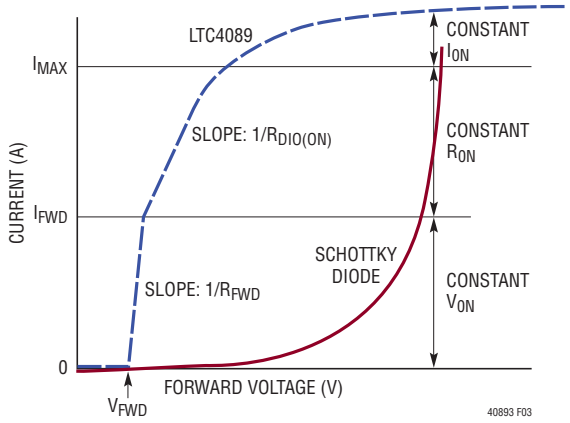



**Figure 3. LTC4089-3 Versus Schottky Diode Forward Voltage Drop**

## OPERATION

If the input current increases beyond the programmed input current limit additional current will be drawn from the battery via the internal ideal diode. Furthermore, if power to IN (USB $V_{BUS}$) or HVIN (high voltage input) is removed, then all of the application power will be provided by the battery via the ideal diode. A 4.7µF capacitor at OUT is sufficient to keep a transition from input power to battery power from causing significant output voltage droop. The ideal diode consists of a precision amplifier that enables a large P-channel MOSFET transistor whenever the voltage at OUT is approximately 20mV ($V_{FWD}$) below the voltage at BAT. The resistance of the internal ideal diode is approximately 200mΩ. If this is sufficient for the application then no external components are necessary. However, if more conductance is needed, an external P-channel MOSFET can be added from BAT to OUT. The GATE pin of the LTC4089-3 drives the gate of the PFET for automatic ideal diode control. The source of the external MOSFET should be connected to OUT and the drain should be connected to BAT. In order to help protect the external MOSFET in over-current situations, it should be placed in close thermal contact to the LTC4089-3.

### Battery Charger

The battery charger circuits of the LTC4089-3 are designed for charging single-cell lithium-ion batteries. Featuring an internal P-channel power MOSFET, the charger uses a constant-current/constant-voltage charge algorithm with programmable current and a programmable timer for charge termination. Charge current can be programmed up to 1.2A. The final float voltage accuracy is ±0.8% typical. No blocking diode or sense resistor is required when powering either the IN or the HVIN pins. The $\overline{CHRG}$ open-drain status output provides information regarding the charging status of the LTC4089-3 at all times. An NTC input provides the option of charge qualification using battery temperature.

An internal thermal limit reduces the programmed charge current if the die temperature attempts to rise above a preset value of approximately 105°C. This feature protects the LTC4089-3 from excessive temperature, and allows the user to push the limits of the power handling capability of a given circuit board without risk of damaging the LTC4089-3. Another benefit of the LTC4089-3 thermal limit is that charge current can be set according to typical, not worst-case, ambient temperatures for a given application with the assurance that the charger will automatically reduce the current in worst-case conditions.

The charge cycle begins when the voltage at the OUT pin rises above the battery voltage and the battery voltage is below the recharge threshold. No charge current actually flows until the OUT voltage is 100mV above the BAT voltage. At the beginning of the charge cycle, if the battery voltage is below 2.8V, the charger goes into trickle charge mode to bring the cell voltage up to a safe level for charging. The charger goes into the fast charge constant-current mode once the voltage on the BAT pin rises above 2.8V. In constant-current mode, the charge current is set by $R_{PROG}$. When the battery approaches the final float voltage, the charge current begins to decrease as the LTC4089-3 switches to constant-voltage mode. When the charge current drops below 10% of the programmed charge current while in constant-voltage mode the $\overline{CHRG}$ pin assumes a high impedance state.

An external capacitor on the TIMER pin sets the total minimum charge time. When this time elapses the charge cycle terminates and the $\overline{CHRG}$ pin assumes a high impedance state, if it has not already done so. While charging in constant-current mode, if the charge current is decreased by thermal regulation or in order to maintain the programmed input current limit the charge time is automatically increased. In other words, the charge time is extended inversely proportional to the actual charge current delivered to the battery. For Li-Ion and similar batteries that require accurate final float potential, the internal bandgap reference, voltage amplifier and the resistor divider provide regulation with ±0.8% accuracy.

## OPERATION

### Trickle Charge and Defective Battery Detection

At the beginning of a charge cycle, if the battery voltage is low (below 2.8V) the charger goes into trickle charge reducing the charge current to 10% of the full-scale current. If the low battery voltage persists for one quarter of the total charge time, the battery is assumed to be defective, the charge cycle is terminated and the $\overline{CHRG}$ pin output assumes a high impedance state. If for any reason the battery voltage rises above ~2.8V the charge cycle will be restarted. To restart the charge cycle (i.e., when the dead battery is replaced with a discharged battery), simply remove the input voltage and reapply it or cycle the TIMER pin to 0V.

### Programming Charge Current

The formula for the battery charge current is:

$$I_{CHG} = I_{PROG} \bullet 50,000 = \frac{V_{PROG}}{R_{PROG}} \bullet 50,000$$

where $V_{PROG}$ is the PROG pin voltage and $R_{PROG}$ is the total resistance from the PROG pin to ground. Keep in mind that when the LTC4089-3 is powered from the IN pin, the programmed input current limit takes precedent over the charge current. In such a scenario, the charge current cannot exceed the programmed input current limit.

For example, if typical 500mA charge current is required, calculate:

$$R_{PROG} = \frac{1V}{500mA} \bullet 50,000 = 100k$$

For best stability over temperature and time, 1% metal film resistors are recommended. Under trickle charge conditions, this current is reduced to 10% of the full-scale value.

### The Charge Timer

The programmable charge timer is used to terminate the charge cycle. The timer duration is programmed by an external capacitor at the TIMER pin. The charge time is typically:

$$t_{TIMER}(hours) = \frac{C_{TIMER} \bullet R_{PROG} \bullet 3hours}{0.1\mu F \bullet 100k}$$

The timer starts when an input voltage greater than the undervoltage lockout threshold level is applied or when leaving shutdown and the voltage on the battery is less than the recharge threshold. At power-up or exiting shutdown with the battery voltage less than the recharge threshold the charge time is a full cycle. If the battery is greater than the recharge threshold the timer will not start and charging is prevented. If after power-up the battery voltage drops below the recharge threshold, or if after a charge cycle the battery voltage is still below the recharge threshold, the charge time is set to one-half of a full cycle.

The LTC4089-3 has a feature that extends charge time automatically. Charge time is extended if the charge current in constant-current mode is reduced due to load current or thermal regulation. This change in charge time is inversely proportional to the change in charge current. As the LTC4089-3 approaches constant-voltage mode the charge current begins to drop. This change in charge current is due to normal charging operation and does not affect the timer duration.

Consider, for example, a USB charge condition where $R_{CLPROG}$ = 2k, $R_{PROG}$ = 100k and $C_{TIMER}$ = 0.1µF. This corresponds to a three hour charge cycle. However, if the HPWR input is set to a logic low, then the input current limit will be reduced from 500mA to 100mA. With no additional system load, this means the charge current will

## OPERATION

be reduced to 100mA. Therefore, the termination timer will automatically slow down by a factor of five until the charger reaches constant-voltage mode (i.e., $V_{BAT}$ = 4.2V) or HPWR is returned to a logic high. The charge cycle is automatically lengthened to account for the reduced charge current. The exact time of the charge cycle will depend on how long the charger remains in constant-current mode and/or how long the HPWR pin remains a logic low.

Once a timeout occurs and the voltage on the battery is greater than the recharge threshold, the charge current stops, and the $\overline{CHRG}$ output assumes a high impedance state if it has not already done so.

Connecting the TIMER pin to ground disables the battery charger.

### $\overline{CHRG}$ Status Output Pin

When the charge cycle starts, the $\overline{CHRG}$ pin is pulled to ground by an internal N-channel MOSFET capable of driving an LED. When the charge current drops below 10% of the programmed full charge current while in constant-voltage mode, the pin assumes a high impedance state, but charge current continues to flow until the charge time elapses. If this state is not reached before the end of the programmable charge time, the pin will assume a high impedance state when a timeout occurs. The $\overline{CHRG}$ current detection threshold can be calculated by the following equation:

$$I_{DETECT} = \frac{0.1V}{R_{PROG}} \bullet 50,000 = \frac{5000V}{R_{PROG}}$$

For example, if the full charge current is programmed to 500mA with a 100k PROG resistor the $\overline{CHRG}$ pin will change state at a battery charge current of 50mA.

Note: The end-of-charge (EOC) comparator that monitors the charge current latches its decision. Therefore, the first time the charge current drops below 10% of the programmed full charge current while in constant-voltage mode, it will toggle $\overline{CHRG}$ to a high impedance state. If, for some reason the charge current rises back above the threshold, the $\overline{CHRG}$ pin will not resume the strong pull-down state. The EOC latch can be reset by a recharge cycle (i.e., $V_{BAT}$ drops below the recharge threshold) or toggling the input power to the part.

### NTC Thermistor—Battery Temperature Charge Qualification

The battery temperature is measured by placing a negative temperature coefficient (NTC) thermistor close to the battery pack. The NTC circuitry is shown in Figure 4.

To use this feature, connect the NTC thermistor ($R_{NTC}$) between the NTC pin and ground and a resistor ($R_{NOM}$) from the NTC pin to VNTC. $R_{NOM}$ should be a 1% resistor with a value equal to the value of the chosen NTC thermistor at 25°C (this value is 10k for a Vishay NTHS0603N02N1002J thermistor). The LTC4089-3 goes into hold mode when the resistance ($R_{HOT}$) of the NTC thermistor drops to 0.48 times the value of $R_{NOM}$, or approximately 4.8k, which should be at 45°C. The hold mode freezes the timer and stops the charge cycle until the thermistor indicates a return to a valid temperature. As the temperature drops, the resistance of the NTC thermistor rises. The LTC4089-3 is designed to go into hold mode when the value of the NTC thermistor increases to 2.82 times the value of $R_{NOM}$. This resistance is $R_{COLD}$.

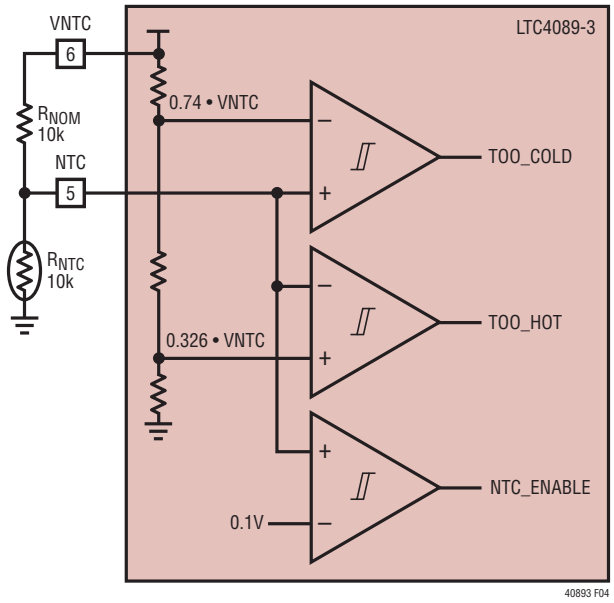



**Figure 4. NTC Circuit**

## OPERATION

For a Vishay NTHS0603N02N1002J thermistor, this value is 28.2k which corresponds to approximately 0°C. The hot and cold comparators each have approximately 2°C of hysteresis to prevent oscillation about the trip point. Grounding the NTC pin will disable the NTC function.

### Current Limit Undervoltage Lockout

An internal undervoltage lockout circuit monitors the input voltage and disables the input current limit circuits until $V_{IN}$ rises above the undervoltage lockout threshold. The current limit UVLO circuit has a built-in hysteresis of 125mV. Furthermore, to protect against reverse current in the power MOSFET, the current limit UVLO circuit disables the current limit (i.e., forces the input power path to a high impedance state) if $V_{OUT}$ exceeds $V_{IN}$. If the current limit UVLO comparator is tripped, the current limit circuits will not come out of shutdown until $V_{OUT}$ falls 50mV below the $V_{IN}$ voltage.

### Charger Undervoltage Lockout

An internal undervoltage lockout circuit monitors the $V_{OUT}$ voltage and disables the battery charger circuits until $V_{OUT}$ rises above the undervoltage lockout threshold. The battery charger UVLO circuit has a built-in hysteresis of 125mV. Furthermore, to protect against reverse current in the power MOSFET, the charger UVLO circuit keeps the charger shut down if $V_{BAT}$ exceeds $V_{OUT}$. If the charger UVLO comparator is tripped, the charger circuits will not come out of shutdown until $V_{OUT}$ exceeds $V_{BAT}$ by 50mV.

### Suspend

The LTC4089-3 can be put in suspend mode by forcing the SUSP pin greater than 2.3V. In suspend mode, the ideal diode function from BAT to OUT is kept alive. If power is applied to the HVIN pin, then charging will be unaffected. Current drawn from the IN pin is reduced to 50µA. Suspend mode is intended to comply with the USB power specification mode of the same name.

# APPLICATIONS INFORMATION

## USB and 5V Wall Adapter Power

Although the LTC4089-3 is designed to draw power from a USB port, a higher power 5V wall adapter can also be used to power the application and charge the battery (higher voltage wall adapters can be connected directly to HVIN). Figure 5 shows an example of combining a 5V wall adapter and a USB power input. With its gate grounded by 1k, P-channel MOSFET MP1 provides USB power to the LTC4089-3 when 5V wall power is not available. When 5V wall power is available, D1 both supplies power to the LTC4089-3, pulls the gate of MN1 high to increase the charge current (by increasing the input current limit), and pulls the gate of MP1 high to disable it and prevent conduction back to the USB port.

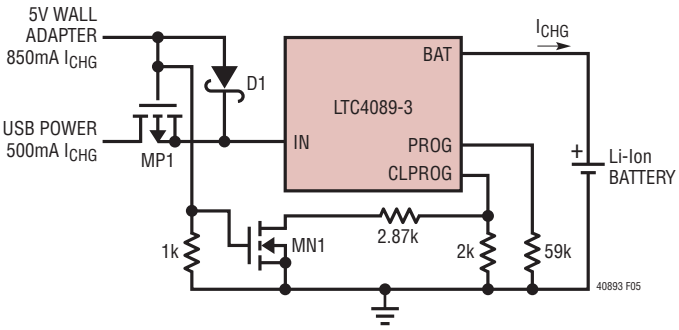



**Figure 5. USB or 5V Wall Adapter Power**

## Inductor Selection and Maximum Output Current

A good choice for the inductor value is L = 10µH. With this value the maximum load current will be 1A. The RMS current rating of the inductor must be greater than the maximum load current and its saturation current should be about 30% higher. Note that the maximum load current will be the programmed charge current plus the largest expected application load current. For robust operation in fault conditions, the saturation current should be ~2.3A. To keep efficiency high, the series resistance (DCR) should be less than 0.1Ω. Table 1 lists several vendors and types that are suitable.

**Table 1. Inductor Vendors**

| VENDOR | URL | PART SERIES | INDUCTANCE (µH) | SIZE (mm) |
|---|---|---|---|---|
| Sumida | www.sumida.com | CDRH5D28 | 8.2, 10 | 6 × 6 × 3 |
| | | CDRH6D38 | 10 | 7 × 7 × 4 |
| TDK | www.tdk.com | SLF6028T | 10 | 6 × 6 × 2.8 |
| Toko | www.toko.com | D63LCB | 10 | 6.3 × 6.3 × 3 |

## Catch Diode

Depending on load current, a 1A to 2A Schottky diode is recommended for the D1 catch diode. The diode must have a reverse voltage rating equal to, or greater than, the maximum input voltage. The ON Semiconductor MBRM140 and the Diodes Inc. DFLS140/160/240 are good choices.

## High Voltage Regulator Capacitor Selection

Bypass the HVIN pin of the LTC4089-3 circuit with a 1µF, or higher value ceramic capacitor of X7R or X5R type. Y5V types have poor performance over temperature and applied voltage and should not be used. A 1µF ceramic is adequate to bypass the high voltage input and will easily handle the ripple current. However, if the input power source has high impedance, or there is significant inductance due to long wires or cables, additional bulk capacitance may be necessary. This can be provided with a low performance electrolytic capacitor.

## APPLICATIONS INFORMATION

The high voltage regulator output capacitor controls output ripple, supplies transient load currents, and stabilizes the regulator control loop. Ceramic capacitors have very low equivalent series resistance (ESR) and provide the best ripple performance. A good value is 10µF. Use X5R or X7R types, and note that a ceramic capacitor biased with $V_{HVOUT}$ will have less than its nominal capacitance. Table 2 lists several capacitor vendors.

**Table 2. Capacitor Vendors**

| VENDOR | PHONE | URL | PART SERIES | COMMENTS |
|---|---|---|---|---|
| Panasonic | (714) 373-7366 | www.panasonic.com | Ceramic, Polymer, Tantalum | EEF Series |
| Kemet | (864) 963-6300 | www.kemet.com | Ceramic, Tantalum | T494, T495 |
| Sanyo | (408) 749-9714 | www.sanyovideo.com | Ceramic, Polymer, Tantalum | POSCAP |
| Murata | (404) 436-1300 | www.murata.com | Ceramic | |
| AVX | | www.avxcorp.com | Ceramic, Tantalum | TPS Series |
| Taiyo Yuden | (864) 963-6300 | www.taiyo-yuden.com | Ceramic | |

### BOOST Pin Considerations

Capacitor C3 and diode D2 (see Block Diagram) are used to generate a boost voltage that is higher than the input voltage. In most cases, a 0.1µF capacitor and fast-switching diode (such as the 1N4148 or 1N914) will work well. The BOOST pin must be at least 2.2V above the SW pin for proper operation.

### High Voltage Regulator Soft-Start

The HVEN pin can be used to soft-start the high voltage regulator and reduce the maximum input current during start-up. A voltage ramp at the HVEN pin can be created by driving the pin through an external RC filter (see Figure 6).

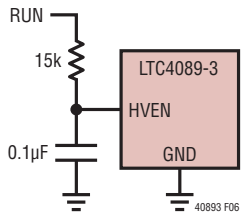



**Figure 6. Using the HVEN Pin to Soft-Start the High Voltage Regulator.**

By choosing a large RC time constant, the peak start-up current will not overshoot the current that is required to regulate the output. Choose the value of the resistor so that it can supply 20µA when the HVEN pin reaches 2.3V.

### Alternate NTC Thermistors

The LTC4089-3 NTC trip points were designed to work with thermistors whose resistance-temperature characteristics follow Vishay Dale's "R-T Curve 2." The Vishay NTHS0603N02N1002J is an example of such a thermistor. However, Vishay Dale has many thermistor products that follow the "R-T Curve 2" characteristic in a variety of sizes. Furthermore, any thermistor whose ratio of $R_{COLD}$ to $R_{HOT}$ is about 6.0 will also work (Vishay Dale R-T Curve 2 shows a ratio of 2.815/0.4839 = 5.82).

Power conscious designs may want to use thermistors whose room temperature value is greater than 10k. Vishay Dale has a number of values of thermistor from 10k to 100k that follow the "R-T Curve 2." Using these as indicated in the NTC Thermistor section will give temperature trip points of approximately 3°C and 42°C, a delta of 39°C. This delta in temperature can be moved in either direction by changing the value of $R_{NOM}$ with respect to $R_{NTC}$. Increasing $R_{NOM}$ will move both trip points to lower temperatures. Likewise, a decrease in $R_{NOM}$ with respect to $R_{NTC}$ will move the trip points to higher temperatures.

## APPLICATIONS INFORMATION

To calculate $R_{NOM}$ for a shift to lower temperature, for example, use the following equation:

$$R_{NOM} = \frac{R_{COLD}}{2.816} \bullet R_{NTC} \text{ at } 25°C$$

where $R_{COLD}$ is the resistance ratio of $R_{NTC}$ at the desired cold temperature trip point. To shift the trip points to higher temperatures use the following equation:

$$R_{NOM} = \frac{R_{HOT}}{0.484} \bullet R_{NTC} \text{ at } 25°C$$

where $R_{HOT}$ is the resistance ratio of $R_{NTC}$ at the desired hot temperature trip point.

The following example uses a 100K R-T Curve 1 Thermistor from Vishay Dale. The difference between the trip points is 39°C, from before—and the desired cold trip point of 0°C, would put the hot trip point at 39°C. The $R_{NOM}$ needed is calculated as follows:

$$R_{NOM} = \frac{R_{COLD}}{2.816} \bullet R_{NTC} \text{ at } 25°C$$

$$= \frac{3.266}{2.816} \bullet 100k\Omega = 116k\Omega$$

The nearest 1% value for $R_{NOM}$ is 115k. This is the value used to bias the NTC thermistor to get cold and hot trip points of approximately 0°C and 44°C, respectively. To extend the delta between the cold and hot trip points, a resistor (R1) can be added in series with $R_{NTC}$ (see Figure 7). The values of the resistors are calculated as follows:

$$R_{NOM} = \frac{R_{COLD} - R_{HOT}}{2.816 - 0.484}$$

$$R1 = \left[\frac{0.484}{2.816 - 0.484}\right] \bullet \left[R_{COLD} - R_{HOT}\right] - R_{HOT}$$

where $R_{NOM}$ is the value of the bias resistor, $R_{HOT}$ and $R_{COLD}$ are the values of $R_{NTC}$ at the desired temperature trip points. Continuing the aforementioned example with a desired hot trip point of 50°C:

$$R_{NOM} = \frac{R_{COLD} - R_{HOT}}{2.816 - 0.484}$$

$$= \frac{100k \bullet (3.266 - 0.3602)}{2.816 - 0.484}$$

$$= 124.6k, 124k \text{ nearest } 1\%$$

$$R1 = 100k \bullet \left[\left(\frac{0.484}{2.816 - 0.484}\right) \bullet \left(3.266 - 0.3602\right) - 0.3602\right]$$

$$= 24.3k$$

The final solution is shown in Figure 7, where $R_{NOM}$ = 124k, R1 = 24.3k and $R_{NTC}$ = 100k at 25°C

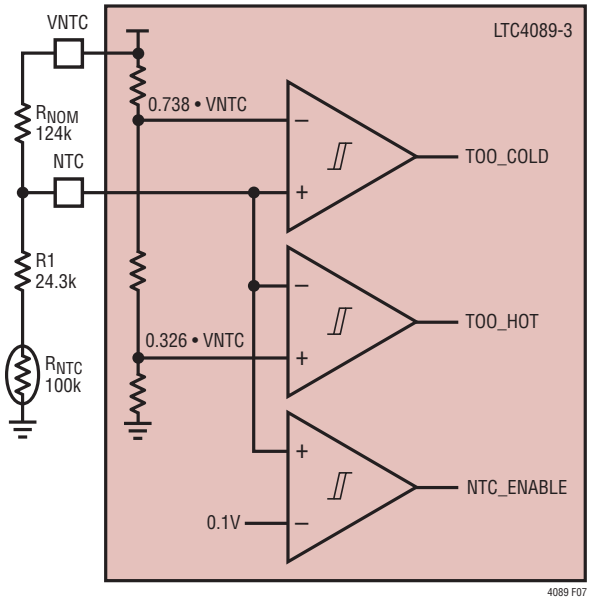



**Figure 7. Modified NTC Circuit**

## APPLICATIONS INFORMATION

### Power Dissipation and High Temperature Considerations

The die temperature of the LTC4089-3 must be lower than the maximum rating of 110°C. This is generally not a concern unless the ambient temperature is above 85°C. The total power dissipated inside the LTC4089-3 depends on many factors, including input voltage (IN or HVIN), battery voltage, programmed charge current, programmed input current limit, and load current.

In general, if the LTC4089-3 is being powered from IN the power dissipation can be calculated as follows:

$$P_D = (V_{IN} – V_{BAT}) • I_{BAT} + (V_{IN} – V_{OUT}) • I_{OUT}$$

where $P_D$ is the power dissipated, $I_{BAT}$ is the battery charge current, and $I_{OUT}$ is the application load current. For a typical application, an example of this calculation would be:

$$P_D = (5V – 3.7V) • 0.4A + (5V – 4.75V) • 0.1A = 545mW$$

This example assumes $V_{IN}$ = 5V, $V_{OUT}$ = 4.75V, $V_{BAT}$ = 3.7V, $I_{BAT}$ = 400mA, and $I_{OUT}$ = 100mA resulting in slightly more than 0.5W total dissipation.

If the LTC4089-3 is being powered from HVIN, the power dissipation can be estimated by calculating the regulator power loss from an efficiency measurement, and subtracting the catch diode loss.

$$P_D = (1-\eta) • (V_{HVOUT} • (I_{BAT} + I_{OUT})) – V_D • \left(1 – \frac{V_{HVOUT}}{V_{HVIN}}\right) • (I_{BAT} + I_{OUT}) + 0.3V • I_{BAT}$$

where $\eta$ is the efficiency of the high voltage regulator and $V_D$ is the forward voltage of the catch diode at $I = I_{BAT} + I_{OUT}$. The first term corresponds to the power lost in converting $V_{HVIN}$ to $V_{HVOUT}$, the second term subtracts the catch diode loss, and the third term is the power dissipated in the battery charger. For a typical application, an example of this calculation would be:

$$P_D = (1-0.87) • [4V • (0.7A + 0.3A)] – 0.4V • \left(1 – \frac{4V}{12V}\right) • (0.7A + 0.3A) + 0.3V • 0.7A$$
$$= 463mW$$

This example assumes 87% efficiency, $V_{HVIN}$ = 12V, $V_{BAT}$ = 3.7V ($V_{HVOUT}$ is about 4V), $I_{BAT}$ = 700mA, $I_{OUT}$ = 300mA resulting in less than 0.5W total dissipation.

To prevent power dissipation of this magnitude from causing high die temperature, it is important to solder the exposed backside of the package to a ground plane. This ground should be tied to other copper layers below with thermal vias; these layers will spread the heat dissipated by the LTC4089-3v. Additional vias should be placed near the catch diodes. Adding more copper to the top and bottom layers, and tying this copper to the internal planes with vias, can reduce thermal resistance further. With these steps, the thermal resistance from die (i.e., junction) to ambient can be reduced to $\theta_{JA}$ = 40°C/W.

The power dissipation in the other power components—catch diodes, MOSFETs, boost diodes and inductors—causes additional copper heating and can further increase the “ambient” temperature of the IC.

### Board Layout Considerations

As discussed in the previous section, it is critical that the exposed metal pad on the backside of the LTC4089-3 package be soldered to the PC board ground. Furthermore, proper operation and minimum EMI requires a careful printed circuit board (PCB) layout. Note that large, switched currents flow in the power switch (between the HVIN and SW pins), the catch diode and the HVIN input capacitor. These components, along with the inductor and output capacitor, should be placed on the same side of the circuit board, and their connections should be made on that layer. Place a local, unbroken ground plane below these components. The loop formed by these components should be as small as possible. Additionally, the SW and BOOST nodes should be kept as small as possible. Figure 8 shows the recommended component placement with trace and via locations.

## APPLICATIONS INFORMATION

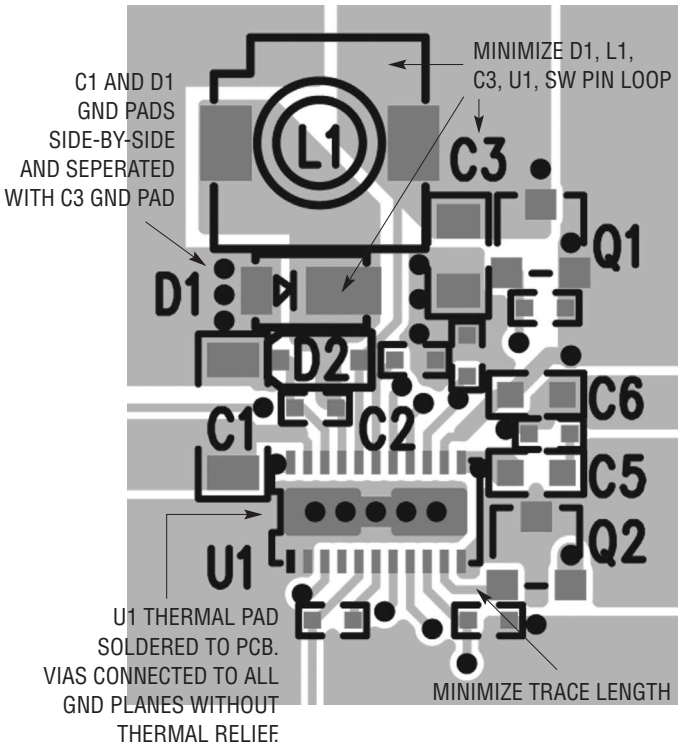



**Figure 8. Suggested Board Layout**

High frequency currents, such as the high voltage input current of the LTC4089, tend to find their way along the ground plane on a mirror path directly beneath the incident path on the top of the board. If there are slits or cuts in the ground plane due to other traces on that layer, the current will be forced to go around the slits. If high frequency currents are not allowed to flow back through their natural least-area path, excessive voltage will build up and radiated emissions will occur. See Figure 9.

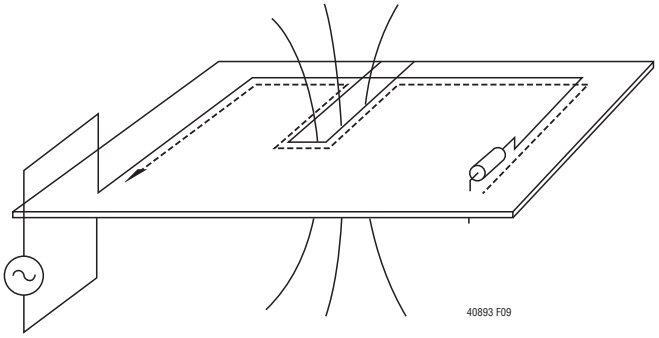



**Figure 9. Ground Currents Follow Their Incident Path at High Speed. Slices in the Ground Plane Cause High Voltage and Increased Emissions**

### $V_{IN}$ and $V_{HVIN}$ Bypass Capacitor

Many types of capacitors can be used for input bypassing, however, caution must be exercised when using multilayer ceramic capacitors. Because of the self-resonant and high Q characteristics of some types of ceramic capacitors, high voltage transients can be generated under some start-up conditions, such as from connecting the charger input to a hot power source. For more information, refer to Application Note 88.

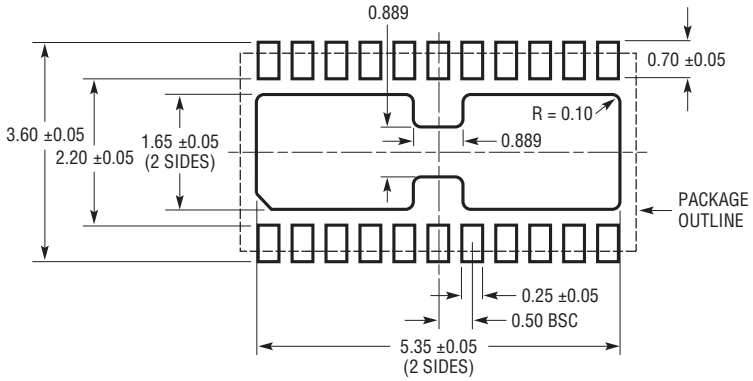
### Battery Charger Stability Considerations

The constant-voltage mode feedback loop is stable without any compensation when a battery is connected with low impedance leads. Excessive lead length, however, may add enough series inductance to require a bypass capacitor of at least 1µF from BAT to GND. Furthermore, a 4.7µF capacitor with a 0.2Ω to 1Ω series resistor to GND is recommended at the BAT pin to keep ripple voltage low when the battery is disconnected.

# PACKAGE DESCRIPTION

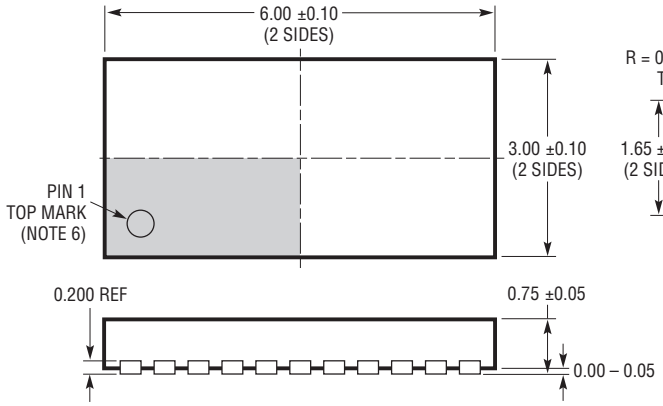
**Please refer to http://www.linear.com/product/LTC4089-3#packaging for the most recent package drawings.**

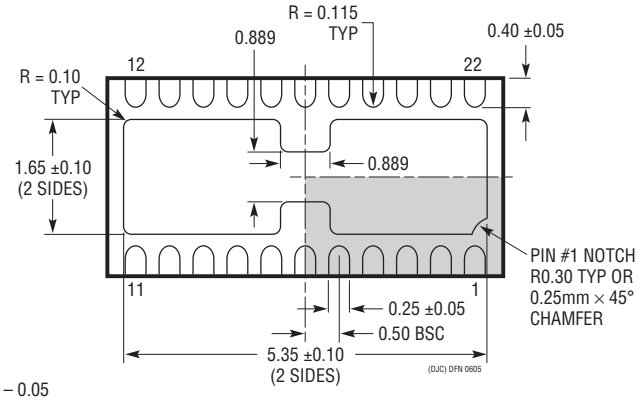
**DJC Package**
**22-Lead Plastic DFN (6mm × 3mm)**
(Reference LTC DWG # 05-08-1714 Rev Ø)




RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS

NOTE:
1. DIMENSIONS ARE IN MILLIMETERS
2. APPLY SOLDER MASK TO AREAS THAT
   ARE NOT SOLDERED
3. DRAWING IS NOT TO SCALE




BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING PROPOSED TO BE MADE VARIATION OF VERSION (WXXX)
   IN JEDEC PACKAGE OUTLINE M0-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE
   MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION
   ON TOP AND BOTTOM OF PACKAGE

# REVISION HISTORY

| REV | DATE | DESCRIPTION | PAGE NUMBER |
|---|---|---|---|
| A | 07/17 | Modified $I_{VNTC}$ specification. | 4 |



Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

## APPLICATIONS INFORMATION

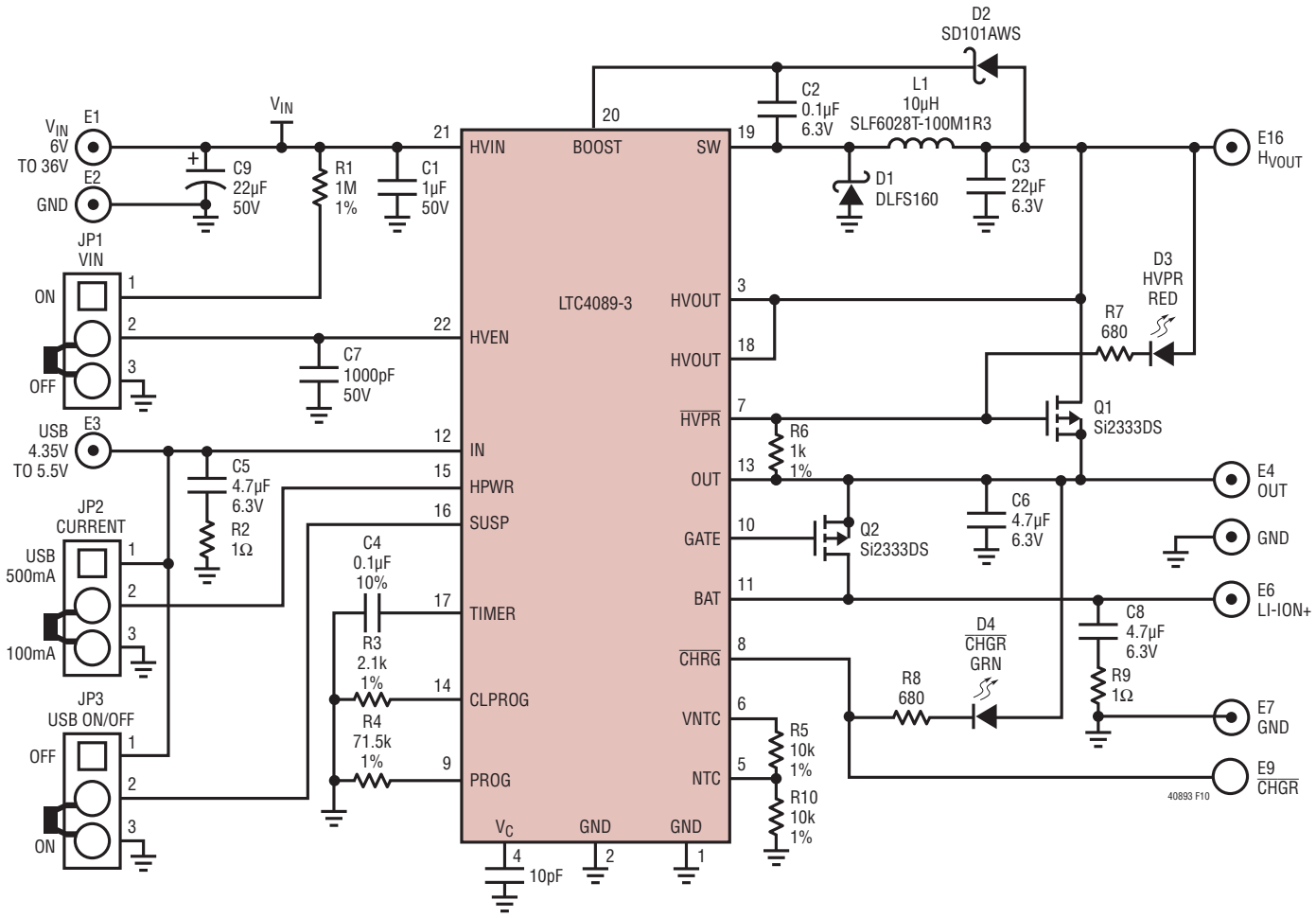



**Figure 10. Typical Application Diagram**

## RELATED PARTS

| PART NUMBER | DESCRIPTION | COMMENTS |
|---|---|---|
| **Power Management** | | |
| LTC3455 | Dual DC/DC Converter with USB Power Manager and Li-Ion Battery Charger | Seamless Transition Between Power Sources: USB, Wall Adapter and Battery; 95% Efficient DC/DC Conversion |
| LTC4055 | USB Power Controller and Battery Charger | Charges Single Cell Li-Ion Batteries Directly from a USB Port, Thermal Regulation, 200mΩ Ideal Diode, 4mm × 4mm QFN16 Package |
| LTC4066 | USB Power Controller and Li-Ion Battery Charger with Low-Loss Ideal Diode | Charges Single Cell Li-Ion Batteries Directly from a USB Port, Thermal Regulation, 50mΩ Ideal Diode, 4mm × 4mm QFN24 Package |
| LTC4085 | USB Power Manager with Ideal Diode Controller and Li-Ion Charger | Charges Single Cell Li-Ion Batteries Directly from a USB Port, Thermal Regulation, 200mΩ Ideal Diode with <50mΩ Option, 4mm × 3mm DFN14 Package |



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