2.5A Supercapacitor Backup Power Manager

FEATURES

- **2.5A Step-Down Supercapacitor Charger and 2.5A Step-Up Backup Supply**
- **6.5A Switches for 2.5A Backup from One Supercapacitor or Two in Series**
- **Input Current Limit Prioritizes Load over Charge Current**
- **Input Disconnect Switch Isolates Input During Backup**
- **Automatic Seamless Switch-Over to Backup Mode**
- Internal Supercapacitor Balancer (No External Resistors)
- Programmable Charge Current and Charge Voltage
- Input Power Fail Indicator
- System Power Good Indicator
- Optional OVP Circuitry Protects Device to >60V
- Constant Frequency Operation
- Thermally Enhanced 24-Lead 4mm × 5mm QFN Package

APPLICATIONS

- Ride-Through "Dying Gasp" Supplies
- High Current Ride-Through 3V to 5V UPS
- Power Meters/Industrial Alarms
- Servers/Solid State Drives

DESCRIPTION

The LTC®4041 is a complete supercapacitor backup system for 2.9V to 5.5V supply rails. It contains a high current step-down DC/DC converter to charge a single supercapacitor or two supercapacitors in series. When input power is unavailable, the step-down regulator operates in reverse as a step-up regulator to backup the system output from the supercapacitor(s).

The LTC4041's adjustable input current limit function reduces charge current to protect the input supply from overload while an external disconnect switch isolates the input supply during backup. When the input supply drops below the adjustable PFI threshold, the 2.5A boost regulator delivers power from the supercapacitor to the system output.

An optional input overvoltage protection (OVP) circuit protects the LTC4041 from high voltage damage at the V_{IN} pin. An internal supercapacitor balancing circuit maintains equal voltages across each supercapacitor and limits the maximum voltage of each supercapacitor to a pre-determined value. The LTC4041 is available in a low profile (0.75mm) 24-Lead 4mm × 5mm QFN package.

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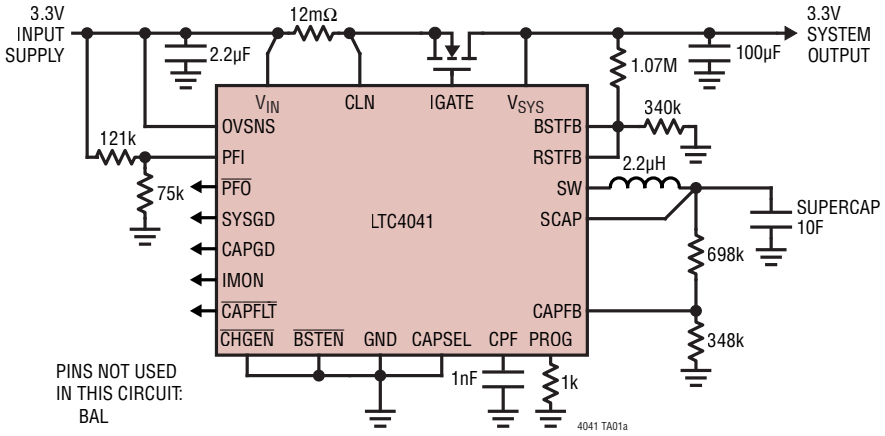
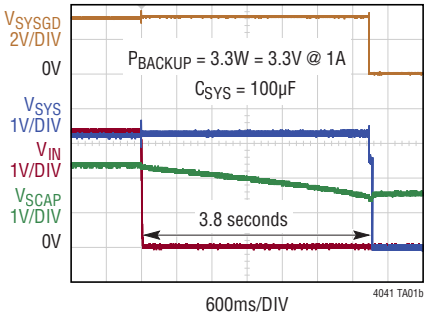
TYPICAL APPLICATION

Single Supercapacitor 3.3V Backup Application



Complete Backup Event with a Single 10F Supercapacitor

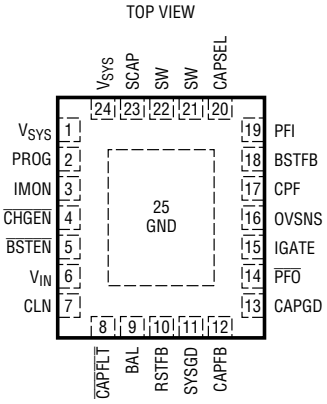


ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN} (Transient) t < 1ms, Duty Cycle < 1% ..... –0.3V to 7V
V_{IN} (Steady State), SCAP, BAL, CLN, V_{SYS}, BSTFB, PFI, CPF, CAPFB, $\overline{CAPFLT}$, $\overline{PFO}$, SYSGD, OVSNS, IMON.....–0.3V to 6V
$\overline{BSTEN}$, $\overline{CHGEN}$, CAPGD, RSTFB, CAPSEL..... –0.3V to [Max (V_{IN}, V_{SCAP}, V_{SYS}) +0.3V]
I_{OVSNS} ..... ±10mA
I_{CAPGD}, $I_{\overline{PFO}}$, I_{SYSGD} 10mA
I_{PROG} .....–1.1mA
Operating Junction Temperature Range (Notes 2, 3) ..... –40°C to 125°C
Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



UFD PACKAGE
24-LEAD (4mm × 5mm) PLASTIC QFN
T_{JMAX} = 125°C, θ_{JA} = 43°C/W, θ_{JC} = 3.4°C/W
EXPOSED PAD (PIN 25) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC4041EUFD#PBF	LTC4041EUFD#TRPBF	4041	24-Lead (4mm × 5mm × 0.75mm) Plastic QFN	–40°C TO 125°C
LTC4041IUFD#PBF	LTC4041IUFD#TRPBF	4041	24-Lead (4mm × 5mm × 0.75mm) Plastic QFN	–40°C TO 125°C

Consult ADI Marketing for parts specified with wider operating temperature ranges.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating temperature range, otherwise specifications are at T_A = 25°C. (Note 3) V_{IN} = V_{SYS} = 5V, V_{SCAP} = 2.5V, R_{PROG} = 2k, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Input Voltage Range		●	2.9		5.5	V
V_{SCAP}	Supercapacitor Voltage Range (Backup Boost Input)		●			5.4	V
	Quiescent Current in Charger Mode with Charging Complete and Backup Boost Active (CAPSEL = 1)	V_{IN} and V_{SYS} Total Quiescent Current			800	1600	µA
		SCAP Quiescent Current			13	26	µA
	Quiescent Current in Charger Mode with Charging Complete and Backup Boost in Sleep (CAPSEL = 1)	V_{IN} and V_{SYS} Total Quiescent Current			275	550	µA
		SCAP Quiescent Current			13	26	µA
	Quiescent Current in Backup Mode with Backup Boost in Sleep (V_{IN} = 0V, CAPSEL = 1)	V_{SYS} Quiescent Current	●		75	150	µA
		SCAP Quiescent Current	●		1	2	µA
	Quiescent Current in Shutdown ($\overline{CHGEN}$ = $\overline{BSTEN}$ = CAPSEL = 1, V_{SYS} = 0V)	V_{IN} Quiescent Current			5.5	11	µA
		SCAP Quiescent Current	●		0	1	µA
Buck Supercapacitor Charger							
V_{CAPFB}	CAPFB Pin Servo Voltage		●	0.788	0.80	0.812	V
I_{CAPFB}	CAPFB Pin Input Leakage Current			–50	0	50	nA
I_{CHG}	Regulated Supercapacitor Charge Current	R_{PROG} = 2k, V_{SCAP} >1V		950	1000	1050	mA
	V_{SYS}-to-V_{SCAP} Differential Undervoltage Lockout Threshold	(V_{SYS} – V_{SCAP}) Falling (V_{SYS} – V_{SCAP}) Rising		30 100	50 150	70 200	mV mV
V_{PROG}	PROG Pin Servo Voltage				800		mV
h_{PROG}	Ratio of Charge Current to PROG Pin Current				2500		mA/mA
	Input Current Limit Threshold Voltage	V_{IN} – V_{CLN}	 ●	23.5 22	25 25	26.5 28	mV mV
A_{IMON}	Input Current Limit Amplifier Gain	Ratio of V_{IMON} to (V_{IN} – V_{CLN})			32		V/V
	CLN Input Bias Current	V_{CLN} = V_{IN}				300	nA
V_{RECHRG}	Recharge Threshold Voltage	As a Percentage of the Regulated V_{SCAP}		96.2	97.5	98.8	%
	End-of-Charge Indication	PROG Pin Average Voltage			100		mV
	CAPGD Rising Threshold	As a Percentage of the Regulated V_{SCAP}		90	92.5	95	%
	Hysteresis	As a Percentage of the Regulated V_{SCAP}			2.5		%
$f_{OSC(BUCK)}$	Step-Down Converter Switching Frequency	V_{SCAP}>1V		2.0	2.25	2.5	MHz
$R_{P(BUCK)}$	High Side Switch On-Resistance				130		mΩ
$R_{N(BUCK)}$	Low Side Switch On-Resistance				120		mΩ
$I_{LIM(BUCK)}$	PMOS Switch Current Limit			3	4.3		A
Supercapacitor Balancer							
V_{BAL}	Supercapacitor Balance Point	As a Percentage of V_{SCAP}, V_{SCAP} = 5V		49	50	51	%
I_{SOURCE}	Balancer Source Current	V_{SCAP} = 5V, V_{BAL} = 2.4V			50		mA
I_{SINK}	Balancer Sink Current	V_{SCAP} = 5V, V_{BAL} = 2.6V			50		mA
	Top/Bottom Supercapacitor Overvoltage Threshold	(V_{SCAP} – V_{BAL}) and/or V_{BAL} Rising, CAPSEL = 1	●		2.7	2.8	V
	Hysteresis				55		mV
	Top/Bottom Supercapacitor Undervoltage Threshold	(V_{SCAP} – V_{BAL}) and/or V_{BAL} Falling, CAPSEL = 1	●	–50	–20		mV
	Hysteresis				30		mV

ELECTRICAL CHARACTERISTICS

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SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Backup Boost Switching Regulator							
V_{BSTFB}	BSTFB Pin Servo Voltage		●	0.78	0.8	0.82	V
I_{BSTFB}	BSTFB Pin Input Leakage Current	V_{BSTFB} = 0.9V		–20		20	nA
$V_{SYS-BACKUP}$	Programmed Boost Output Voltage Range			2.7		5	V
$f_{OSC(BST)}$	Step-Up Converter Switching Frequency			1.0	1.125	1.25	MHz
$I_{LIM(BST)}$	NMOS Switch Current Limit			5.5	6.5	7.5	A
$R_{P(BST)}$	High Side Switch On-Resistance				75		mΩ
$R_{N(BST)}$	Low Side Switch On-Resistance				70		mΩ
	V_{SYS} Overvoltage Shutdown Threshold	V_{SYS} Rising		5.3	5.5	5.7	V
	Hysteresis				100		mV
	Boost Undervoltage Lockout	Max(V_{SYS}, V_{SCAP}) Falling			2.5		V
	Hysteresis				150		mV
D_{MAX}	Maximum Boost Duty Cycle				88		%
	NMOS Switch Leakage Current	$\overline{BSTEN}$ = 1, $\overline{CHGEN}$ = 1			0	1	µA
	PMOS Switch Leakage Current	$\overline{BSTEN}$ = 1, $\overline{CHGEN}$ = 1			0	1	µA
$t_{MIN-BACKUP}$	Minimum Backup Time	C_{CPF} = 1nF			2.2		ms
SYSGD Comparator							
	RSTFB Threshold	V_{RSTFB} Falling	●	0.72	0.74	0.76	V
	Hysteresis				20		mV
I_{RSTFB}	RSTFB Pin Input Leakage Current	V_{RSTFB} = 0.9V		–50	0	50	nA
	SYSGD Delay	V_{RSTFB} Rising & Falling			100		µs
Power-Fail Comparator							
	PFI Input Threshold	V_{PFI} Falling	 ●	1.17 1.16	1.19 1.19	1.21 1.22	V V
	Hysteresis				40		mV
	PFI Pin Leakage Current	V_{PFI} = 1.3V		–100	0	100	nA
	PFI Delay to $\overline{PFO}$	V_{PFI} Falling			0.5		µs
	$\overline{PFO}$ Pin Leakage Current	$V_{\overline{PFO}}$ = 5V			0	1	µA
	$\overline{PFO}$ Pin Output Low Voltage	$I_{\overline{PFO}}$ = 5mA			65	200	mV
Logic Input ($\overline{BSTEN}$, $\overline{CHGEN}$, CAPSEL, $\overline{CAPFLT}$)							
V_{IL}	Logic Low Input Voltage		●			0.4	V
V_{IH}	Logic High Input Voltage		●	1.2			V
I_{IL}	Logic Low Input Leakage Current	$\overline{BSTEN}$, $\overline{CHGEN}$			0	1	µA
I_{IH}	Logic High Input Leakage Current	$\overline{BSTEN}$, $\overline{CHGEN}$			0	1	µA
	CAPSEL Pin Leakage Current	CAPSEL = 1				10	µA

ELECTRICAL CHARACTERISTICS

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SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Open-Drain Output (SYSGD, CAPGD)							
	Pin Leakage Current	5V at Pin			0	1	µA
	Pin Output Low Voltage	5mA Into Pin			65	200	mV
$\overline{\text{CAPFLT}}$ Status Pin							
	$\overline{\text{CAPFLT}}$ Pin Pull-Down Current	$V_{\overline{\text{CAPFLT}}}$ = 200mV			10		µA
	Pin Leakage Current	5V at Pin			0	1	µA
Overvoltage Protection							
$V_{OV(CUTOFF)}$	Overvoltage Protection Threshold	V_{OVSNS} Rising, R_{OVSNS} = 6.2k		6.0	6.4	6.8	V
V_{OVGT}	IGATE Output Voltage Active	V_{IN} = V_{OVSNS} = 5V			9.4	12	V
$V_{OVGT(LOAD)}$	IGATE Voltage Under Load	5V Through 6.2k Into OVSNS, I_{IGATE} = 1µA		8	8.6		V
I_{OVSNSQ}	OVSNS Quiescent Current	V_{OVSNS} = 5V			40		µA
	OVSNS Quiescent Current in Shutdown	$\overline{\text{BSTEN}}$ = 1, $\overline{\text{CHGEN}}$ = 1			25		µA
	IGATE Time to Reach Regulation	C_{IGATE} = 2.2nF			3.5		ms
Overtemperature (OT) Protection							
	Overtemperature Shutdown	Temperature Rising			160		°C
	Hysteresis				15		°C

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

Note 3: The LTC4041E is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC4041E is guaranteed to meet performance specifications from 0°C to 85°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process control. The LTC4041I is guaranteed over the full –40°C to 125°C operating junction temperature range. The junction temperature (T_J in °C) is calculated from the ambient temperature (T_A, in °C) and power dissipation (P_D, in watts) according to the formula:

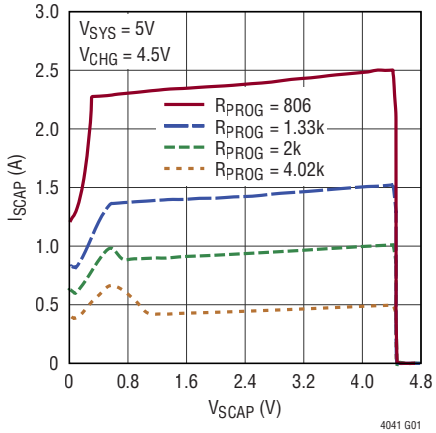
$$T_J = T_A + (P_D \bullet \theta_{JA})$$

where the package thermal impedance θ_{JA} = 43°C/W.

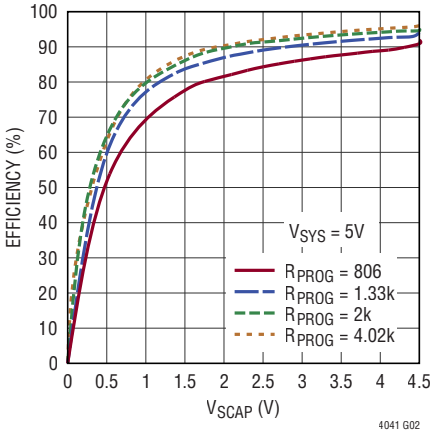
Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance and other environmental factors.

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

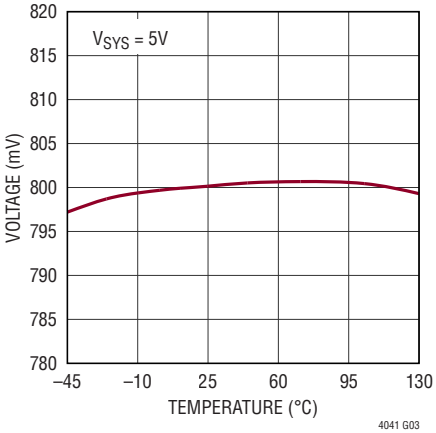
I_{SCAP} vs V_{SCAP} with Different PROG Resistor Values



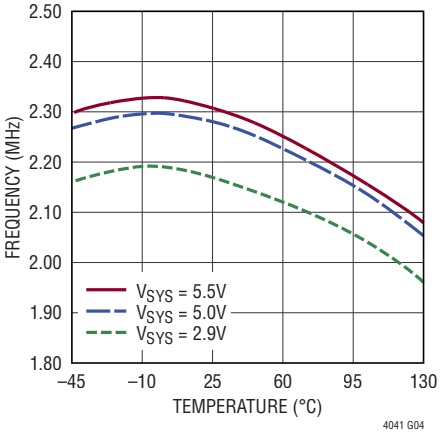
Step-Down Charger Efficiency vs V_{SCAP}



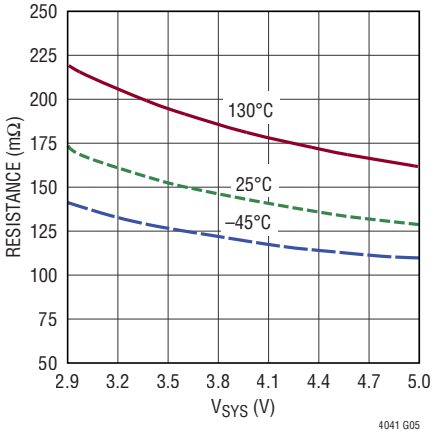
V_{CAPFB} vs Temperature



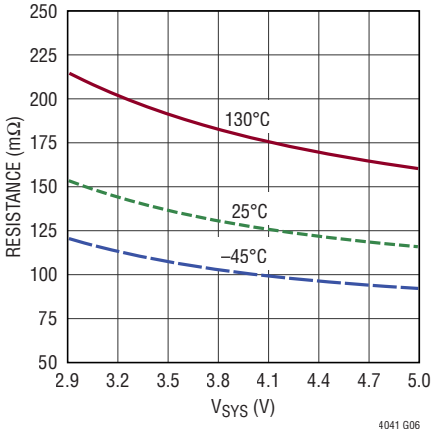
Step-Down Charger Oscillator Frequency vs Temperature



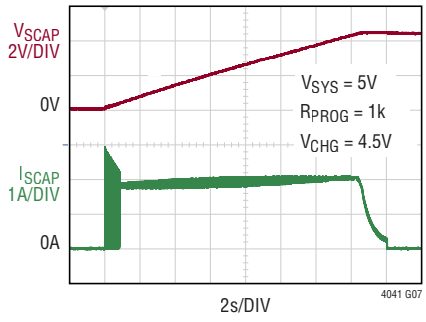
Step-Down Charger PMOS On-Resistance vs V_{SYS}



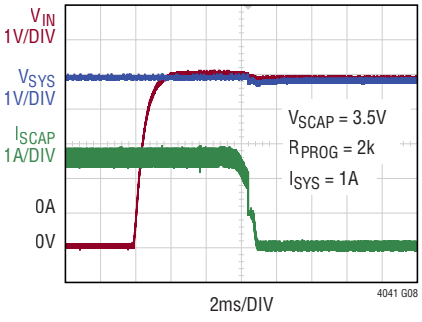
Step-Down Charger NMOS On-Resistance vs V_{SYS}



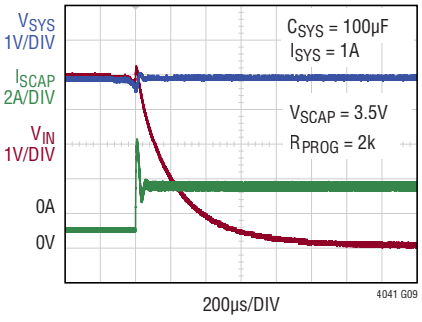
Charging Profile: Two 10F Supercapacitors In Series



Backup to Normal Mode Transition Waveform

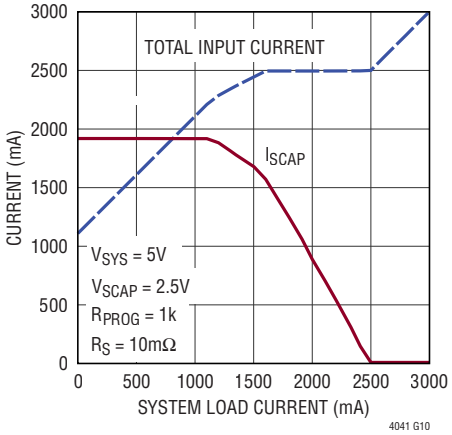


Normal to Backup Mode Transition Waveform

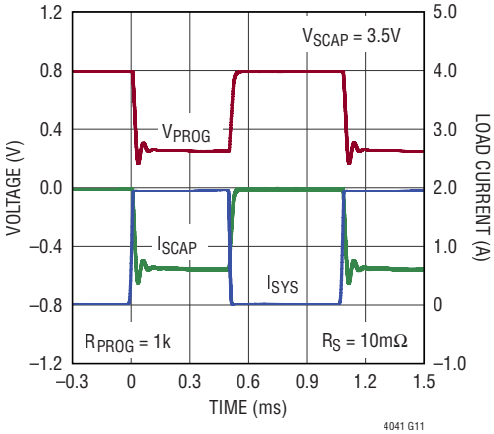


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

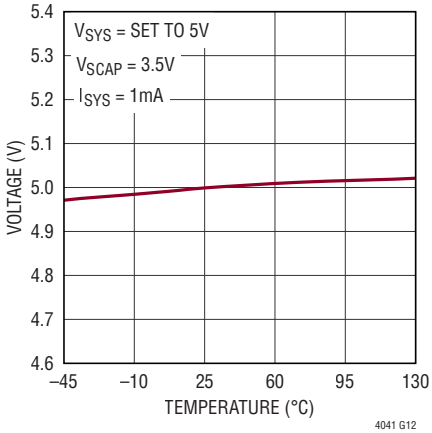
Charge Current Reduction Due to Input Current Limit



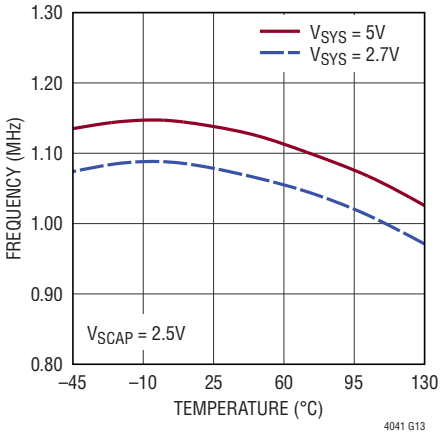
PROG Voltage Transient Response To System Step Load



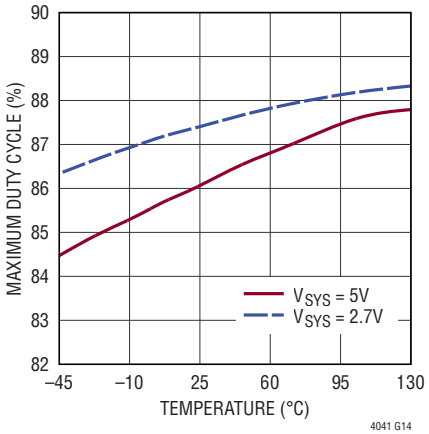
Backup Boost Output Voltage (V_{SYS}) vs Temperature



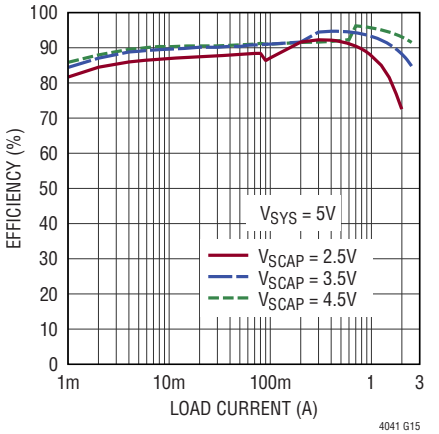
Backup Boost Oscillator Frequency vs Temperature



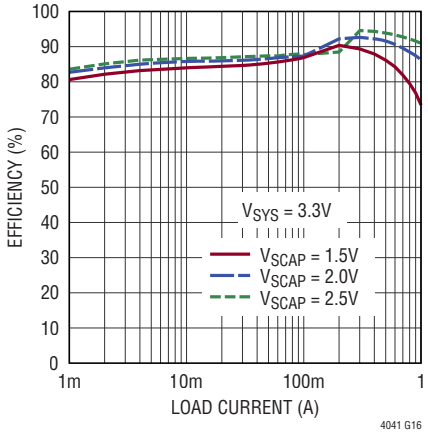
Backup Boost Maximum Duty Cycle vs Temperature



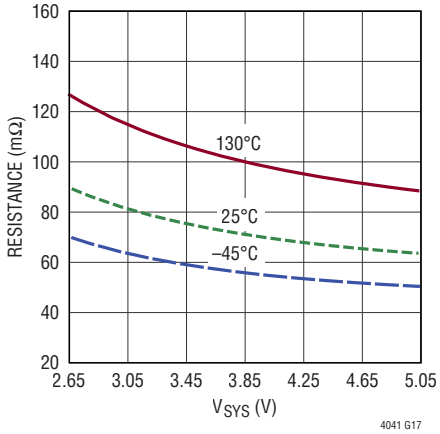
Backup Boost Efficiency vs Load Current for V_{SYS} = 5V



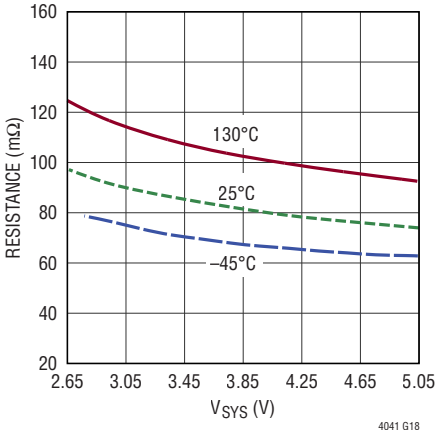
Backup Boost Efficiency vs Load Current for V_{SYS} = 3.3V



Backup Boost NMOS On-Resistance vs V_{SYS}

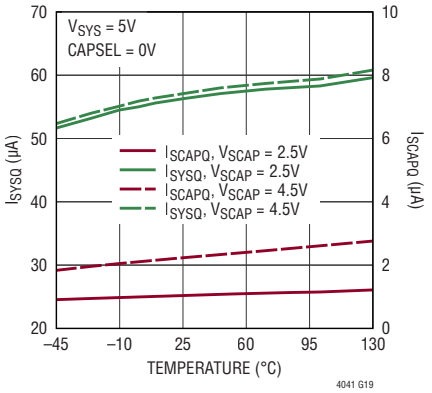


Backup Boost PMOS On-Resistance vs V_{SYS}

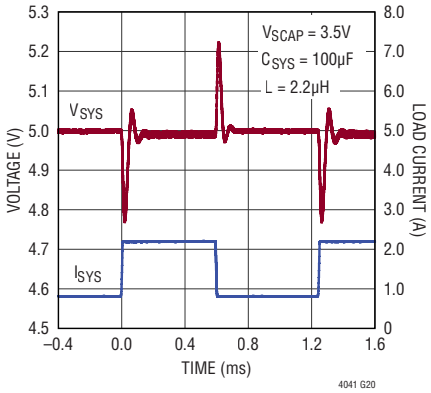


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

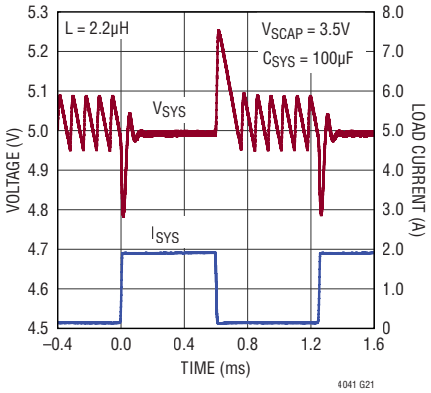
Boost Sleep Mode I_{SYSQ} and I_{SCAPQ} vs Temperature



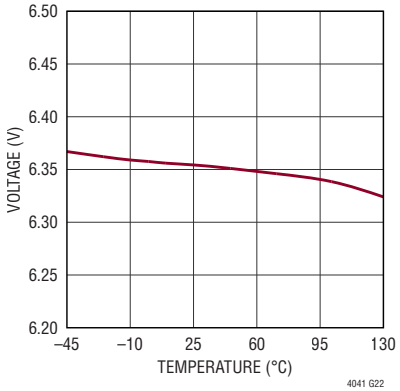
Backup Boost Transient Response to Load Step



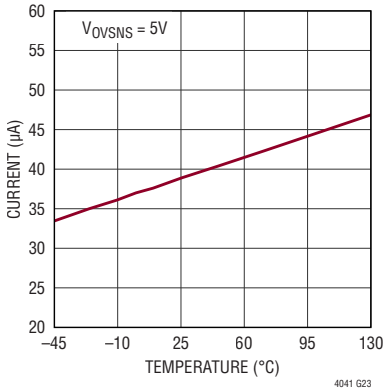
Burst Mode to Constant Frequency Mode Transition Waveform



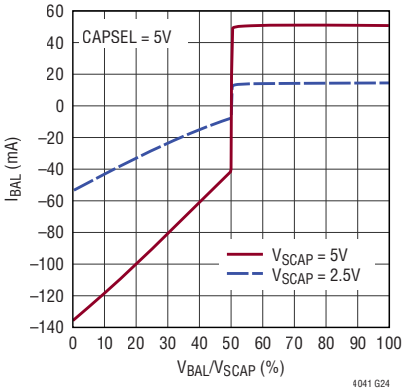
OVP Module Shutdown Voltage (Through 6.2k) vs Temperature



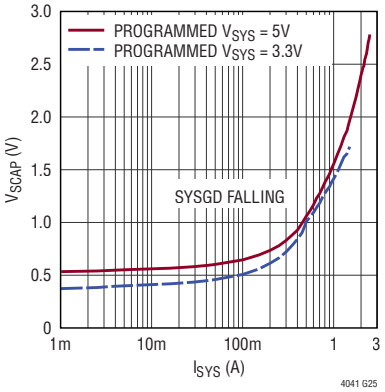
OVSNS Pin Quiescent Current vs Temperature



Supercapacitor Balancer Source/Sink Current



Minimum V_{SCAP} to Maintain Boost Regulation vs I_{SYS}



PIN FUNCTIONS

V_{SYS} (Pins 1, 24): System Voltage Output Pin. This pin is used to provide power to an external load from either the primary input supply or from the backup supercapacitor if the primary input supply is not available. In addition to supplying power to the load, this pin provides power to charge the supercapacitor when input power is available. V_{SYS} should be bypassed with a low ESR ceramic capacitor of at least 100µF to GND.

PROG (Pin 2): Charge Current Program Pin. An external resistor from the PROG pin to GND programs the full-scale charge current. At full scale, the PROG pin servos to 0.8V. The ratio of the SCAP pin current to the PROG pin current is internally set to 2500.

IMON (Pin 3): V_{SYS} Current Monitoring Pin. The ratio between the IMON pin voltage and the differential voltage between V_{IN} and CLN is internally set to 32. Charge current is reduced when the IMON pin voltage reaches 0.8V.

$\overline{\text{CHGEN}}$ (Pin 4): Disable Pin for the Supercapacitor Charger. Tie this pin to GND to enable the charger or to a voltage above 1.2V to disable it. Do not leave this pin unconnected.

$\overline{\text{BSTEN}}$ (Pin 5): Disable Pin for the Backup Boost Converter. Tie this pin to GND to enable the boost backup or to a voltage above 1.2V to disable backup. Do not leave this pin unconnected.

V_{IN} (Pin 6): Input Pin. Power can be applied directly to this pin if the optional overvoltage protection (OVP) feature is not used. For applications where the OVP feature is required, connect an external N-channel FET between the input supply V_{PWR} and this pin.

CLN (Pin 7): Negative terminal pin for an external current limit sense resistor connected between V_{IN} and this pin. This resistor is used to monitor the current from V_{IN} to V_{SYS}. The LTC4041 reduces charge current in order to maintain 25mV across this sense resistor. However, it does not limit the system current if the drop exceeds 25mV.

$\overline{\text{CAPFLT}}$ (Pin 8): Open-Drain Supercapacitor Fault Status Output. In charger mode, if the voltage of any single supercapacitor exceeds 2.7V, this pin is pulled low and charging is disabled. In backup mode, if the voltage of any single supercapacitor falls below –20mV, the $\overline{\text{CAPFLT}}$ pin is pulled low and the backup boost is disabled. To keep charging or backup enabled under any supercapacitor fault condition, tie this pin high. The current pull-down capability of the $\overline{\text{CAPFLT}}$ is 10µA.

BAL (Pin 9): Supercapacitor Balance Point. Connect the common node of a stack of two supercapacitors to this pin. An internal supercapacitor balancer drives this node to a voltage that is half of V_{SCAP}. Leave this pin open if only one supercapacitor is used.

RSTFB (Pin 10): SYSGD Comparator Input. High impedance input to an accurate comparator with a 0.74V falling threshold and 20mV hysteresis. This pin controls the state of the SYSGD output pin. An external resistor divider is used between V_{SYS}, RSTFB and GND. It can be the same resistor divider as the BSTFB divider to monitor the system output voltage V_{SYS}. See the Applications Information section.

SYSGD (Pin 11): Open-Drain Status Output of the SYSGD Comparator. This pin is pulled to GND by an internal N-channel MOSFET whenever the RSTFB pin falls below 0.74V.

CAPFB (Pin 12): Supercapacitor (Single or a Stack of Two) Feedback Pin. An external divider between the SCAP pin and GND with the center tap connected to the CAPFB pin programs the final supercapacitor (or stack) voltage(V_{CHG}). The voltage on this pin nominally servos to 0.8V.

CAPGD (Pin 13): Supercapacitor Power Good Indicator Pin. The open-drain output is pulled low until CAPFB rises to 92.5% of its regulation point.

$\overline{\text{PFO}}$ (Pin 14): Open-Drain Power-Fail Status Output. This pin is pulled to GND by an internal N-channel MOSFET when the PFI input is below the falling threshold of the power-fail comparator. Once the PFI input rises above the rising threshold, this pin becomes high impedance.

PIN FUNCTIONS

IGATE (Pin 15): Gate Pin for the External N-Channel FET(s). This pin is driven by an internal charge pump to develop sufficient overdrive to fully enhance the pass transistors. The first pass transistor, connected between the input power supply and V_{IN}, is a part of the optional overvoltage protection module. The second pass transistor, connected between V_{IN} and V_{SYS}, is mandatory and is used to disconnect the system from the input supply during backup mode.

OVSNS (Pin 16): Overvoltage Protection Sense Input. If the overvoltage feature is used, the OVSNS pin should be connected through a 6.2k resistor to the input power supply and the drain of an N-channel MOS pass transistor. If not, this pin should be shorted to V_{IN}. When voltage is detected on OVSNS, it draws a small amount of current to power a charge pump which then provides gate drive to IGATE to energize the external transistor(s). When the voltage on this pin exceeds 6V (typical), IGATE is pulled to GND to disable the pass transistor and protect the LTC4041 from high voltage.

CPF (Pin 17): Minimum Backup Time ($t_{MIN\text{-}BACKUP}$) Program Pin. Connect a capacitor to this pin to set $t_{MIN\text{-}BACKUP}$. When backup mode is initiated, the LTC4041's backup boost converter stays on for at least $t_{MIN\text{-}BACKUP}$ to prevent any unwanted mode switching. The output of the power-fail comparator is ignored during this time. Do not tie this pin to GND or leave it unconnected.

BSTFB (Pin 18): Feedback Input for the Backup Boost Regulator. During backup operation, the voltage on this pin servos to 0.8V.

PFI (Pin 19): Power-Fail Input. High impedance input to an accurate comparator (power-fail) with a 1.19V falling threshold and 40mV hysteresis. PFI controls the state of the $\overline{PFO}$ output pin and sets the input voltage threshold below which the boost backup is initiated. This threshold voltage also represents the minimum voltage above which the step-down supercapacitor charger is enabled and power is allowed to flow from the input to the output through the external pass transistor(s).

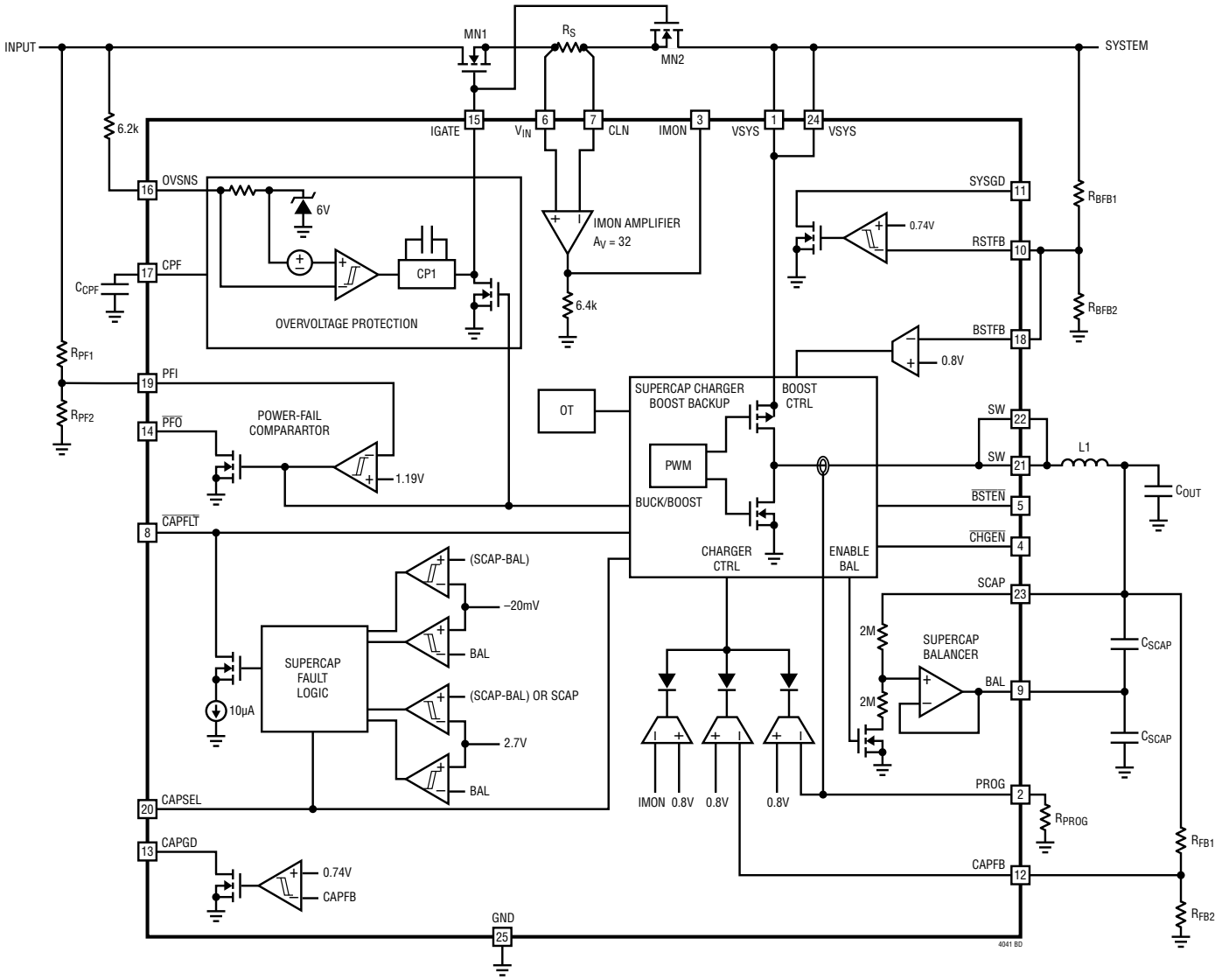
CAPSEL (Pin 20): Supercapacitor Stack Selector Pin. Tie this pin to a voltage higher than 1.2V if a stack of two supercapacitors is connected to the SCAP pin or to GND if a single supercapacitor is connected to the SCAP pin. Do not leave this pin unconnected.

SW (Pins 21, 22): Switch Pins for the Buck Charger and the Boost Backup Converter. A 1µH to 2.2µH inductor should be connected from SW to SCAP.

SCAP (Pin 23): Supercapacitor Pin. Connect a single supercapacitor or the top of a two-supercapacitor stack to this pin. Depending on the availability of input power, the supercapacitor (or the stack) will either deliver power to V_{SYS} via the boost converter or be charged from V_{SYS} via the buck charger.

GND (Exposed Pad Pin 25): The exposed pad must be soldered to the PCB to provide a low electrical and thermal impedance connection to the printed circuit board's ground. A continuous ground plane on the second layer of a multilayer printed circuit board is strongly recommended.

BLOCK DIAGRAM



OPERATION

The LTC4041 is a complete supercapacitor backup system manager for a 2.9V to 5.5V supply rail. The system has three principal circuit components: a full-featured step-down (buck) supercapacitor charger, a step-up (boost) backup converter to deliver power to the system load when external input power is lost, and a power-fail comparator to decide which one to activate. The LTC4041 has several other auxiliary components: an input current limit (IMON) amplifier, an optional input overvoltage protection (OVP) circuit, and a system power good (SYSGD) comparator.

The LTC4041 has three modes of operation: normal, backup and shutdown. If the input supply is above an externally programmable PFI threshold voltage, the LTC4041 is considered to be in normal mode. In this normal mode power flows from input to output (V_{SYS}) while the step-down switching regulator charges a supercapacitor or a stack of supercapacitors to a charge voltage programmed by an external resistor divider connected at the CAPFB pin. Refer to the Block Diagram.

The total system load is monitored by the IMON amplifier via an external series resistor, R_S, connected between the V_{IN} and CLN pins. This amplifier can reduce the charge current from its programmed value (set by the PROG pin external resistor R_{PROG}) if the external load demand increases beyond the level set by R_S.

When the input supply falls below the PFI threshold, backup mode disconnects the switches (MN1 and MN2) to isolate the system (V_{SYS}) from the input, and the boost converter powers the system load from the supercapacitor using the external inductor, L1.

THE SUPERCAPACITOR CHARGER

The LTC4041 includes a full-featured constant-current (CC)/ constant-voltage (CV) supercapacitor charger with programmable charge current and charge voltage, automatic recharge, supercapacitor good indicator, supercapacitor overvoltage detection, and an internal balancer. The charger is a high efficiency, constant frequency (2.25MHz) synchronous buck converter used to charge SCAP from V_{SYS} via the SW pin. It is capable of directly charging the supercapacitor to its charge voltage with an externally programmable charge current up to 2.5A from an input supply as high as 5.5V. A zero current comparator monitors the inductor current and shuts off the NMOS synchronous rectifier once the current reduces to approximately 250mA. This prevents the inductor current from reversing and improves efficiency for low charging currents. The charger can be disabled by pulling the $\overline{CHGEN}$ pin above 1.2V.

Constant-Current Mode Charging

In constant-current (CC) mode, the average current delivered to the supercapacitor can reach 2000V/ R_{PROG}. Depending on the external load condition, the supercapacitor charger may or may not be able to charge at the full programmed rate. The external load will always be prioritized over the supercapacitor charge current. The charger will charge at the full programmed rate only if the sum of the external load and the charger input current is less than or equal to the input current limit set by R_S.

If the buck charger is operating at very low duty cycles (i.e. if the supercapacitor voltage is very low), the actual average charge current delivered to the supercapacitor could vary by as much as 50% of the programmed value. At low duty cycles, the measurement accuracy of the inductor current sensing circuitry in the CC servo loop is low. As a result, the average charge current could overshoot or undershoot. When the supercapacitor (or a stack of supercapacitors) is charged from 0V, the low accuracy of the inductor current sensing causes the buck to operate in discontinuous mode. As the SCAP voltage increases the buck will try to servo the average charge current to the programmed value. When the SCAP voltage is about 1V, the buck exits discontinuous mode and the average charge current will be at the programmed level. During this discontinuous mode of operation, the V_{SYS} voltage ripple is still well-controlled despite the large inductor current ripple because the buck is running at a low duty cycle.

OPERATION

Figure 1 shows the buck charger operating in discontinuous mode. The supercapacitor voltage is at 0V and the charge current is programmed to 500mA. The V_{SYS} voltage ripple, which is also shown in the same figure, is about 14mV in this example.

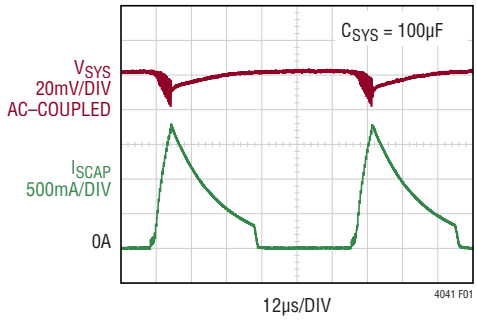


Figure 1. Charge Current Waveform for V_{SCAP} <1V

Charge Termination

The charge voltage of the supercapacitor (or the stack) is set by an external resistor divider connected between the SCAP pin and ground with its midpoint connected to the CAPFB pin. As the voltage on the supercapacitor reaches the pre-set charge voltage, the constant-voltage (CV) loop of the buck charger starts to regulate the supercapacitor voltage and the charge current decreases naturally. Once the charge current drops to 12.5% of the programmed charge current, the buck charger is disabled and no charge current will be delivered to the supercapacitor. To enable the buck charger and resume charging, the supercapacitor voltage has to fall below the automatic recharge threshold.

Automatic Recharge

Once the supercapacitor charger terminates, it remains off drawing only microamperes of current from the supercapacitor. To ensure that the supercapacitor is always topped off, a charge cycle automatically begins when the supercapacitor voltage falls below V_{RECHRG} (typically 97.5%). To prevent brief excursions below V_{RECHRG} from enabling/disabling the buck charger unnecessarily, the supercapacitor voltage must be below V_{RECHRG} for at least 5ms (typical) for the charger to be re-enabled.

Supercapacitor Charge Status Indication via the CAPGD Pin

The CAPGD pin is an open-drain output used to indicate that the supercapacitor (or the stack) voltage has reached 92.5% of its regulation point. The CAPGD pin is pulled low until the supercapacitor voltage is above 92.5% of the final charge voltage at which point the CAPGD pin becomes high impedance. The supercapacitor voltage has to fall below 90% of the regulation point to pull the CAPGD pin low again. The CAPGD pin requires an external pull-up resistor to either the V_{SYS} pin or to another appropriate power source. When the charger is disabled, the CAPGD pin is pulled low.

Supercapacitor Balancer

The LTC4041 has an internal balancer that servos the midpoint of a stack of two supercapacitors, i.e. the BAL pin voltage, to half the stack voltage (V_{SCAP}). To activate the balancer, tie the CAPSEL pin high to indicate that a stack of two supercapacitors is connected to the SCAP pin with the midpoint of the stack connected to the BAL pin. The source/sink capability of the internal balancer is typically ±50mA with V_{SCAP} at 5V. The balancer will try to balance the stack of supercapacitors even after charging is completed. The balancer circuitry is disabled if the charger is disabled. The balancer is also disabled if the CAPSEL pin is low. When a single supercapacitor is connected to the SCAP pin, tie the CAPSEL pin low and float the BAL pin.

Differential Undervoltage Lockout

An undervoltage lockout circuit monitors the differential voltage between V_{SYS} and SCAP and shuts off the charger if the SCAP voltage reaches within 50mV of the V_{SYS} voltage. Charging does not resume until this difference increases to 150mV.

OPERATION

Input Current Limit and IMON Monitor

The LTC4041 contains an input current limit circuit which monitors the total system current (the external load plus the charger input current) via an external series resistor, R_S, connected between the V_{IN} and CLN pins. The LTC4041 does not actually limit the external load but as the external load demand increases, it reduces charge current, if necessary, in an attempt to maintain a maximum of 25mV across the V_{IN} and CLN pins. Refer to Programming the Input Current Limit and IMON Monitor section in Applications Information. However, if the external load demand exceeds the limit set by R_S, the LTC4041 does not reduce the load current but the charge current will drop to zero. In all scenarios, the voltage on the IMON pin will correctly represent the total system current. 800mV on the IMON pin represents the full-scale current set by the external series resistor, R_S.

SUPERCAPACITOR FAULT INDICATION VIA THE $\overline{\text{CAPFLT}}$ PIN

The LTC4041 is equipped with comparators to detect if the voltage on the supercapacitor (or either supercapacitor in the stack) has exceeded the overvoltage (OV) threshold (2.7V typical) or has fallen below the undervoltage (UV) threshold (–20mV typical). Overvoltage detection is enabled only during charging and undervoltage detection is enabled only during backup. Undervoltage detection is also disabled if a single supercapacitor is used (CAPSEL pin is set to low).

The $\overline{\text{CAPFLT}}$ pin is an open-drain output pin with a 10µA (typical) pull-down current source. If the supercapacitor is not under any fault conditions, the $\overline{\text{CAPFLT}}$ pin is high impedance. If the supercapacitor is in an OV/UV condition, the $\overline{\text{CAPFLT}}$ pin is pulled low and charging or backup is disabled. To ignore the fault condition (and continue charging or backup), tie the $\overline{\text{CAPFLT}}$ pin high.

BACKUP BOOST CONVERTER

To supply the system load from the supercapacitor in backup mode, the LTC4041 contains a 1.125MHz constant-frequency current-mode synchronous boost switching regulator with output disconnect and automatic Burst Mode features. The regulator can provide a maximum load of 2.5A from a supercapacitor (or a stack of two supercapacitors) and the system output voltage (V_{SYS}) can be programmed up to a maximum of 5V via the BSTFB pin. See the Applications Information section for details. The converter can be disabled by pulling the $\overline{\text{BSTEN}}$ pin high. The boost regulator includes safety features like short-circuit current protection, input undervoltage lockout, and output overvoltage protection.

Zero Current Comparator

The LTC4041 boost converter includes a zero current comparator which monitors the inductor current and shuts off the PMOS synchronous rectifier once the current drops to approximately 250mA. This prevents the inductor current from reversing in polarity thereby improving efficiency at light loads.

PMOS Synchronous Rectifier

To prevent the inductor current from running away, the PMOS synchronous rectifier is only enabled when $V_{SYS} > (V_{SCAP} – 200mV)$. Additionally, if the current through the synchronous FET (PMOS) ever exceeds 8A, the converter skips the next two clock cycles so that the inductor current has a chance to discharge safely below this level.

Short-Circuit Protection

The output disconnect feature enables the LTC4041 boost converter to survive a short circuit at its output. It incorporates internal features such as current limit foldback and thermal shutdown for protection from excessive power dissipation during short circuit.

Max(V_{SYS},V_{SCAP}) Undervoltage Lockout

The LTC4041 incorporates an undervoltage lockout circuit which shuts down the boost regulator when max(V_{SYS}, V_{SCAP}) drops below 2.5V. This is to ensure that the boost regulator has enough supply voltage to function properly.

OPERATION

Boost Overvoltage Protection

If the BSTFB node were inadvertently shorted to ground, the boost converter output voltage (V_{SYS}) would increase indefinitely with the maximum current that could be sourced from the supercapacitor. The LTC4041 protects against this by shutting off both switches if the output voltage exceeds 5.5V.

Burst Mode Operation

The LTC4041 boost converter provides automatic Burst Mode operation which increases the efficiency of power conversion at very light loads. Burst Mode operation is initiated if the output load current falls below an internally set threshold. Once Burst Mode operation is initiated, only the circuitry required to monitor the output and the supercapacitor undervoltage comparators (if CAPSEL = H) are kept alive. This is referred to as the sleep state in which the backup boost consumes only 75µA (typical, CAPSEL = H) from the system output and 1µA (typical) from the supercapacitor(s). When the V_{SYS} pin voltage drops by about 1% from its nominal value, the boost converter wakes up and commences normal PWM operation. The output capacitor recharges and causes the LTC4041 to re-enter the sleep state if the output load remains less than the Burst Mode threshold. The frequency of this intermittent PWM or Burst Mode operation depends on the load current. As the load current drops below the burst threshold, the boost converter turns on less frequently. When the load current increases above the burst threshold, the converter seamlessly resumes continuous PWM operation. Thus, Burst Mode operation maximizes the efficiency at very light loads by minimizing switching and quiescent losses. However, the output ripple typically increases to about 2% peak-to-peak. Burst Mode ripple can be reduced in some circumstances by placing a small phase-lead capacitor (C_{PL}) between the V_{SYS} and BSTFB pins. However, this may adversely affect the efficiency and the quiescent current at light loads. Typical values of C_{PL} range from 15pF to 100pF.

V_{SCAP} > V_{SYS} Operation

The LTC4041 boost converter will maintain voltage regulation even if its input voltage is above the output voltage. This is achieved by terminating the switching of the synchronous PMOS and applying V_{SCAP} voltage statically on its gate. This ensures that the slope of the inductor current reverses during the time current is flowing to the output. Since the PMOS no longer acts as a low impedance switch in this mode, there will be more power dissipation within the IC. This will cause a sharp drop in the efficiency. The maximum output current should be limited in order to maintain an acceptable junction temperature.

SYSGD COMPARATOR

The LTC4041 contains a SYSGD comparator which monitors V_{SYS} under all operating modes via the RSTFB pin and reports the status via an open-drain NMOS transistor on the SYSGD pin. At any time, if V_{SYS} falls 7.5% from its programmed value, the SYSGD pin pulls low after a 100µs (typical) delay. The comparator also waits 100µs (typical) after V_{SYS} rises above the threshold before making the SYSGD pin high impedance. Refer to Programming the SYSGD Comparator section in Applications Information.

POWER-FAIL COMPARATOR AND MODE SWITCHING

The LTC4041 contains a fast power-fail comparator which switches the LTC4041 from normal to backup mode in the event the input supply voltage falls below an externally programmed threshold voltage. This threshold voltage is programmed by an external resistor divider via the PFI pin. See the Applications Information section for details on how to choose values for the resistor divider. The output of the power-fail comparator also directly drives the gate of an open-drain NMOS to report the status of the availability of input power via the $\overline{PFO}$ pin. If input power is available, the $\overline{PFO}$ pin is high impedance; otherwise, the pin is pulled down to ground.

OPERATION

At the onset of backup mode, the supercapacitor charger shuts off and the external NMOS pass transistors (MN1 and MN2 in the Block Diagram) are quickly turned off by discharging the IGATE pin to ground, thereby disconnecting the system output V_{SYS} from the input and activating the backup boost converter to promptly deliver load from the supercapacitor. Although the power-fail comparator has a hysteresis of approximately 40mV, it may not be able to overcome the input voltage spike resulting from the sudden collapse of the forward current from the input to V_{SYS}. To prevent repetitive mode switching, the backup boost stays on for at least the minimum backup time ($t_{MIN-BACKUP}$) once activated. The minimum backup time is programmed by connecting an external capacitor between the CPF pin and ground. Refer to Programming the Minimum Backup Time section in the Applications Information. During this time, the power-fail comparator output is ignored and an internal switch of approximately 270Ω pulls down the OVSNS pin to help discharge the input. After the minimum backup time has elapsed, if the power-fail comparator output indicates that power is still not available, the backup boost continues to deliver the load but the pull-down on the OVSNS pin is released. When the power-fail comparator detects that input power is available, the OVP charge pump starts to charge up the IGATE pin but the backup boost converter continues to deliver system load until IGATE is approximately 8V. This ensures that the forward conduction path through the external NMOS pass transistors has been established. At this point, the backup boost gets deactivated and the charger turns back on to charge the supercapacitor while the system load gets delivered directly from the input to V_{SYS} through the pass transistors.

OPTIONAL INPUT OVERVOLTAGE PROTECTION (OVP)

The LTC4041 can protect itself from the inadvertent application of excessive voltage with just two external components: an N-channel FET (MN1) and a 6.2k resistor as shown in the Block Diagram. The maximum safe overvoltage magnitude is determined by the choice of external NMOS and its associated drain breakdown voltage.

The optional overvoltage protection (OVP) module consists of two pins. The first, OVSNS, is used to measure the applied voltage through an external resistor. The second, IGATE, is an output used to drive the gate pins of two external N-channel FETs, MN1 and MN2 (Block Diagram). The voltage at the OVSNS pin will be lower than the OVP input voltage by about 250mV due to the OVP circuit's quiescent current flowing through the OVSNS resistor. When OVSNS is below 6V, an internal charge pump drives IGATE to approximately $1.88 \bullet V_{OVSNS}$. This enhances the N-channel FETs providing a low impedance connection to V_{SYS} and power to the LTC4041. If OVSNS rises above 6V due to a fault, IGATE is pulled down to ground, disabling the external FETs to protect downstream circuitry. At the same time, the backup boost converter activates to supply the system load from the supercapacitor. When the voltage drops below 6V again, the external FETs are re-enabled. If the OVP feature is not desired, remove MN1, short OVSNS to V_{IN}, and apply external power directly to V_{IN}.

SHUTDOWN MODE OPERATION

The LTC4041 can be shutdown almost entirely by pulling both $\overline{CHGEN}$ and $\overline{BSTEN}$ pin above 1.2V. In this mode, the internal charge pump is shutdown and IGATE is pulled to ground disconnecting the forward path from input to output via the external FETs. Only the internal OVP shunt regulator remains active to monitor the input supply for any possible overvoltage condition and consuming about 25µA via the OVSNS pin. Total current draw from the SCAP pin drops to below 1µA (V_{SCAP} = 2.5V) in shutdown.

Overtemperature (OT) Protection

When the LTC4041 die temperature exceeds 160°C (typical), the buck charger and backup boost are shut down to prevent any thermal damage and remain in shutdown until the die temperature falls to 145°C (typical). In OT, the forward path from V_{IN} to V_{SYS} is disconnected by pulling the gate voltage of the external FET(s) to ground.

APPLICATIONS INFORMATION

Programming the Supercapacitor Charge Voltage

The charge voltage for a supercapacitor or a stack of supercapacitors is set by an external resistor divider as shown in Figure 2. The charge voltage is given by the following equation:

$$V_{CHG} = 0.8V \bullet \left(1 + \frac{R_{FB1}}{R_{FB2}}\right)$$

where 0.8V is the typical CAPFB pin servo voltage (V_{CAPFB}). Typical values for R_{FB1} and R_{FB2} are in the range of 40k to 2MΩ. Small resistor values result in higher leakage current that will discharge the supercapacitor. If the resistor values are too large, the parasitic capacitance on the CAPFB pin could create an additional pole and cause loop instability.

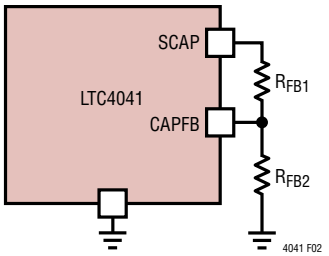


Figure 2. Programming the Charge Voltage

Programming the Input Voltage Threshold for the Power-Fail Comparator

The input voltage threshold below which the power-fail status pin $\overline{PFO}$ indicates a power-fail condition and the LTC4041 activates the backup boost operation can be programmed by using a resistor divider from the supply to GND via the PFI pin such that:

$$V_{IN(PF)} = 1.19V \bullet \left(1 + \frac{R_{PF1}}{R_{PF2}}\right)$$

where 1.19V is the typical power fail threshold voltage (V_{PFI}). See Block Diagram. The power fail threshold voltage should be set to a level between 200mV to 300mV below the nominal input supply voltage so that supply transients do not trip the comparator. On the other hand, it should be set high enough so that the V_{SYS} voltage does not drop enough to trip the SYSGD comparator during the transition to backup mode. For applications using the overvoltage protection (OVP) module, select a value greater than 35k for R_{PF1}.

Programming the Supercapacitor Charge Current

Supercapacitor charge current is programmed using a single resistor from the PROG pin to ground. To set a charge current of I_{CHG}, the PROG pin resistor value can be determined using the following equation:

$$R_{PROG} = 2500 \bullet \frac{0.8V}{I_{CHG}} = \frac{2000V}{I_{CHG}}$$

where 0.8V is the typical PROG pin servo voltage (V_{PROG}). For example, to set the charge current to 1A, the value of the PROG pin resistor should be 2k. The minimum recommended charge current is 500mA, below which the accuracy of the charge current suffers. This corresponds to a maximum R_{PROG} resistor of 4k. The maximum charge current is 2.5A.

Programming the Input Current Limit and IMON Monitor

The input current limit is programmed by connecting a series resistor between the V_{IN} and CLN pins. To limit the total system current to I_{SYSLIM}, the value of the required resistor can be calculated using the following equation:

$$R_S = \frac{25mV}{I_{SYSLIM}}$$

For example, to set the current limit to 2A, the series resistor should be 12.5mΩ. As discussed in the Operation section, the LTC4041 does not limit the system current but reduces the charge current to zero in the event the system load exceeds this limit.

APPLICATIONS INFORMATION

The voltage on the IMON pin always represents the total system current I_{SYS} through the external series resistance, R_S. A voltage of 800mV on IMON represents the full-scale current set by R_S. The system current can be calculated from the IMON pin voltage by using the following equation:

$$I_{SYS} = \frac{V_{IMON}}{32 \bullet R_S}$$

For example, if the IMON pin voltage is 600mV and R_S is 12.5mΩ, then the total system current is 1.5A. As shown in the block diagram, the IMON pin is not buffered internally, so it is important to isolate this pin before connecting to an ADC or any other monitoring device. Failure to do so can degrade the accuracy of this circuit.

Programming the Boost Output Voltage

The boost converter output voltage in backup mode can be programmed for any voltage from 2.7V to 5V by using a resistor divider from the V_{SYS} pin to GND via the BSTFB pin such that:

$$V_{SYS} = 0.8V \bullet \left(1 + \frac{R_{BFB1}}{R_{BFB2}}\right)$$

where 0.8V is the typical BSTFB pin servo voltage (V_{BSTFB}). See the Block Diagram. Typical values for R_{BFB1} and R_{BFB2} are in the range of 40k to 2M. Too small a resistor results in a large quiescent current whereas too large a resistor coupled with any parasitic BSTFB pin capacitance creates an additional pole and may cause loop instability.

Programming the SYSGD Comparator

The threshold for the SYSGD comparator can be programmed by using a resistor divider from the V_{SYS} pin to GND via the RSTFB pin such that:

$$V_{SYS(SYSGD)} = 0.74V \bullet \left(1 + \frac{R_{BFB1}}{R_{BFB2}}\right)$$

where 0.74V is the typical SYSGD pin (falling) threshold voltage (V_{RSTFB}). See the Block Diagram. Typical value for R_{BFB1} and R_{BFB2} are in the range of 40k to 2M. In most applications, the BSTFB and RSTFB pins can be shorted together and only one resistor divider between V_{SYS} and GND is needed to set the V_{SYS} voltage during backup mode and the SYSGD threshold 7.5% below the V_{SYS} programmed voltage.

Programming the Minimum Backup Time

The minimum backup time can be programmed by connecting an external capacitor between the CPF pin and ground. For a given capacitor (C_{CPF}), $t_{MIN\text{-}BACKUP}$ can be calculated by the following equation:

$$t_{MIN\text{-}BACKUP}\ (ms) = 2.2 \bullet C_{CPF}\ (nF)$$

It is recommended to set $t_{MIN\text{-}BACKUP}$ in the range of 1ms to 0.5s. If $t_{MIN\text{-}BACKUP}$ is too short, the LTC4041 could oscillate between charging and backup unnecessarily. If the minimum backup time is too long, the amount of energy drained from the supercapacitor on any single backup event may be more than necessary.

Note: When the LTC4041 is powered on, the C_{CPF} capacitor is pre-charged by the internal circuitry to 1V (typical) with a 1µA current source. The time taken for the initial pre-charge is given by:

$$t_{PRE\text{-}CHARGE}\ (ms) = 1 \bullet C_{CPF}\ (nF)$$

If a backup event occurs during this pre-charge time, the total minimum backup duration will be longer than the programmed value.

Choosing the External Resistor for the Overvoltage Protection (OVP) Module

When overvoltage protection is activated, the OVSNS pin is clamped at 6V. The external 6.2k resistor must be sized appropriately to dissipate the resultant power. For example, a 1/8W, 6.2k resistor can have at most $\sqrt{P_{MAX}} \bullet 6.2k\Omega$ = 28V applied across its terminals. With 6V at OVSNS, the maximum overvoltage magnitude that this resistor can withstand is 34V. A 0.25W, 6.2k resistor raises the value to 45V. The OVSNS pin's absolute maximum current rating of 10mA imposes an upper limit of 68V protection.

APPLICATIONS INFORMATION

Choosing the External Transistors (MN1 and MN2) for the OVP Module and the Input-to-Output Disconnect Switch

The LTC4041 uses a weak internal charge pump to pump IGATE above the input voltage so that the N-channel external FETs can be used as pass transistors. However, these transistors should be carefully chosen so that they are fully enhanced with a V_{GS} of 3V. Since one of these pass transistors is the OVP FET, its breakdown voltage (BV_{DSS}) determines the maximum voltage the LTC4041 can withstand at its input. Also, care must be taken to avoid any leakage on the IGATE pin, as it may adversely affect the FET operation. See Table 1 for a list of recommended transistors.

Table 1. Recommended NMOS FETs for Overvoltage Protection and Disconnect Switch

NMOS FET	BVDSS	R_{ON}
SIR424DP (Vishay)	20V	7.4mΩ
SiS488DN (Vishay)	40V	7.5mΩ
SiS424DN (Vishay)	20V	8.9mΩ

Choosing the Inductor for the Switching Regulators

Since the same inductor is used to charge the supercapacitor in normal mode and to deliver the system load in backup mode, its inductance should be low enough so that the inductor current can reverse quickly as soon as backup mode is initiated. On the other hand, the inductance should not be so low that the inductor current is discontinuous at the lowest charge current setting since charge current accuracy suffers greatly if the inductor current is discontinuous. Inductor current ripple (ΔI_L) can be computed using the following equation:

$$\Delta I_L = V_{SCAP} \bullet \left(1 - \frac{V_{SCAP}}{V_{SYS}}\right) \bullet \frac{1}{L \bullet f_{OSC}}$$

Since the lowest recommended charge current setting is 500mA, inductor current will be discontinuous if the ripple is more than twice that amount, i.e, 1A. For V_{SYS} = 5V, V_{SCAP} = 3.2V, f_{OSC} = 2.25MHz (buck mode), and ΔI_L = 1A, the theoretical minimum inductor size to avoid discontinuous operation can be computed using the above equation to be 0.5µH. To account for inaccuracies in the system and component values, the practical lower limit should be 1µH. Since the backup boost operates at half the frequency (1.125MHz), the inductor current ripple with a 1µH inductor using the same equation will be approximately 1A in backup mode. If this is excessive, inductors up to 2.2µH can be used to lower the inductor current ripple.

The other considerations when choosing an inductor are the maximum DC current (IDC) and the maximum DC resistance (DCR) rating as shown in Table 2. The chosen inductor should have a max IDC rating which is greater than the current limit specification of the LTC4041 in order to prevent an inductor current runaway situation. For the LTC4041, the maximum current that the inductor can experience is approximately 8A in backup mode. It is also important to keep the max DCR as low as possible in order to minimize conduction loss to and help improve the converter's efficiency.

Table 2. Recommended Inductors for the LTC4041

PART NUMBER	L (µH)	MAX IDC (A)	MAX DCR (mΩ)	SIZE IN mm (L × W × H)	MANUFACTURER
XAL-5020-122	1.2	8.3	20.5	5.68 × 5.68 × 2	Coilcraft www.coilcraft.com
XAL-6030-122	1.2	10.8	7.5	6.76 × 6.76 × 3.1	Coilcraft www.coilcraft.com
XAL-6020-132	1.3	9	15.4	6.76 × 6.76 × 2.1	Coilcraft www.coilcraft.com
XAL-6030-182	1.8	14	10.52	6.76 × 6.76 × 3.1	Coilcraft www.coilcraft.com
XAL-5030-222	2.2	9.2	14.5	5.3 × 5.5 × 3.1	Coilcraft www.coilcraft.com
XAL-6030-222	2.2	15.9	13.97	6.38 × 6.58 × 3.1	Coilcraft www.coilcraft.com
831532200	2.2	14	15.3	6.5 × 7 × 3	Wurth Electronics www.we-online.com

Choosing the V_{SYS} Capacitor

The worst-case delay for the backup boost converter to meet the system load demand occurs when the PFI input falls below the externally set threshold at a time when the buck charger is charging at the highest setting of

APPLICATIONS INFORMATION

2.5A and the system load is also very high, e.g., 2.5A. Under this scenario, as soon as the LTC4041 initiates backup mode, the inductor current has to reverse from 2.5A (from SW to SCAP) to as high as the boost current limit of approximately 6.5A (from SCAP to SW). That is a 9A current change in the inductor with a slope of V_{SCAP}/L. At a low supercapacitor voltage of 3.2V, this would take almost 3µs even with a 1µH inductor. During this transition, C_{SYS}, the capacitor on the V_{SYS} pin, has to deliver the shortfall until the inductor current catches up with the system load demand, and the capacitor will deplete according to the following equation:

$$C_{SYS} = I_{LOAD} \bullet \frac{\Delta t}{\Delta V}$$

The size of the capacitor should be big enough to hold the system voltage, V_{SYS}, up above the SYSGD threshold during this transition. For a system load I_{LOAD} = 2.5A and transition time Δt = 3µs, if the maximum droop ΔV allowed in the system output is 100mV, the required capacitance at the V_{SYS} pin should be at least 75µF. The other consideration for choosing the V_{SYS} capacitor size is the maximum acceptable output voltage ripple during steady-state backup boost operation. For a given duty cycle D and load I_{LOAD}, the output ripple V_{RIP} of a boost converter is calculated using the following equation:

$$V_{RIP} = \frac{I_{LOAD}}{C_{SYS}} \bullet D \bullet \frac{1}{f_{OSC}}$$

If the maximum allowable ripple is 20mV under 2.5A steady-state load while boosting from 3.2V to 5V (D = 36%), the required capacitance at V_{SYS} is calculated to be at least 40µF using the above equation. Refer to Table 3 for recommended ceramic capacitor manufacturers.

Table 3. Recommended Ceramic Capacitor Manufacturers

AVX	www.avx.com
Murata	www.murata.com
Taiyo Yuden	www.t-yuden.com
Vishay Siliconix	www.vishay.com
TDK	www.tdk.com

Choosing a Supercapacitor

The backup energy requirement is the main consideration when selecting a supercapacitor. The capacitance per cell and the number of cells (maximum of two) needed depends on the system load (I_{SYS}), system voltage (V_{SYS}), backup boost efficiency (η), supercapacitor charge voltage (V_{CHG}) and the duration of the backup (t_{BACKUP}). The following equation can be used to estimate the amount of capacitance required for a given backup application:

$$C_{SCAP} = \frac{V_{SYS} \bullet I_{SYS} \bullet t_{BACKUP}}{\eta \bullet (V_{CHG})^2}$$

Another factor to be considered is the current rating of the supercapacitor. With the LTC4041, the supercapacitor could be charged with a current as high as 2.5A. During a backup event, the supercapacitor could be discharged at a current level as high as 7.5A. It is also important to select a supercapacitor with low ESR to minimize power losses in the supercapacitor during charging or backup. Other factors to be considered are the lifetime of the supercapacitor at the charge voltage, and the capacitance degradation over time.

The internal balancer of the LTC4041 is designed to balance supercapacitors with capacitances greater than 100mF per cell. For lower capacitances, the balancer servo loop could be unstable.

A list of supercapacitor suppliers is provided in Table 4.

Table 4. Supercapacitor Suppliers

AVX	www.avx.com
Bussman	www.cooperbussman.com
CAP-XX	www.cap-xx.com
Illinois Capacitor	www.illcap.com
Maxwell	www.maxwell.com
Murata	www.murata.com
NESS CAP	www.nesscap.com
Tecate Group	www.tecategroup.com

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Supercapacitor Charger Stability Considerations

The LTC4041's switching supercapacitor charger contains three control loops: constant-voltage, constant-current, and input current limit loop, all of which are internally compensated. However, various external variables like load and component values may interfere with the internal compensation and cause instability.

In constant-current mode, the PROG pin is in the feedback loop rather than the SCAP pin. Because of the additional pole created by any PROG pin capacitance, capacitance on this pin must be kept to a minimum. For the constant-current loop to be stable, the pole frequency at the PROG pin should be kept above 1MHz. Therefore, if the PROG pin has a parasitic capacitance, C_{PROG}, the following equation should be used to calculate the maximum resistance value for R_{PROG}:

$$R_{PROG} \leq \frac{1}{2\pi \bullet 1MHz \bullet C_{PROG}}$$

Alternatively, for R_{PROG} = 4k (500mA setting), the maximum allowable capacitance on the PROG pin is 40pF. If any measuring device is attached to the PROG pin for monitoring the charge current, a 1M isolation resistor should be inserted between the PROG pin and the device.

Backup Boost Stability Considerations

The LTC4041's backup boost converter is internally compensated. However, system capacitance less than 100µF or over 1000µF will adversely affect the phase margin and hence the stability of the converter. Also, if the right-half-plane (RHP) zero moves down in frequency due to external load conditions or the choice of the inductor value, the phase margin may be reduced to a point which causes instability. If the output power is P_{OUT}, inductor value is L, efficiency is η, and the input to the boost converter is V_{SCAP}, the RHP zero frequency can be expressed as follows:

$$f_{RHP} = \frac{(V_{SCAP})^2}{2 \bullet \pi \bullet L \bullet P_{OUT}} \bullet \eta$$

For the LTC4041's backup boost to be able to supply 12.5W of output power (2.5A at 5V) from a stack of supercapacitors charged to 3.2V, the maximum inductor size should not exceed 2.2µH because of the RHP zero consideration. Also, too much resistance between the supercapacitor and the SCAP pin can lower the effective input voltage of the boost converter causing the RHP zero to shift lower in frequency and thus causing instability. This is why it is important to minimize the lead resistance and place the supercapacitor as close to the SCAP pin as possible.

PCB Layout Considerations

Since the LTC4041 includes a high-current high-frequency switching converter, the following guidelines should be followed in the printed circuit board (PCB) layout in order to achieve optimum performance and minimum electromagnetic interference (EMI).

1. Even though the converter can operate in both step-down (buck) and step-up (boost) mode, there is only one hot-loop containing high-frequency switching currents. The simplified diagram in Figure 3 can be used to explain the hot-loop in the LTC4041 switching converter. Current follows the blue loop when the switch S2 (NMOS) is closed and the red loop when switch S1 (PMOS) is closed. So it is evident that the current in the C_{SCAP} capacitor is continuous whereas the C_{SYS} current is discontinuous forming a hot loop with the V_{SYS} pins and GND as indicated by the green loop. Since the amount of EMI is directly proportional to the area of this loop, the V_{SYS} capacitor, prioritized over all else, should be placed as close to the V_{SYS} pins as possible and the ground side of the capacitor should return to the ground plane through an array of vias.

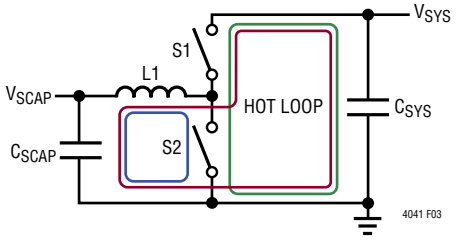

Figure 3. Hot-Loop Illustration for the LTC4041 Switching Converter

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2. To minimize parasitic inductance, the ground plane should be as close as possible to the top plane of the PC board (Layer 2). High frequency currents in the hot loop tend to flow along a mirror path on the ground plane which is directly beneath the incident path on the top plane of the board as illustrated in Figure 4. If there are slits or cuts or drill-holes in this mirror path on the ground plane due to other traces, the current will be forced to go around the slits. When high frequency currents are not allowed to flow back through their natural least-area path, excessive voltage will build up and radiated emissions will occur. So every effort should be made to keep the hot-loop current path as unbroken as possible.

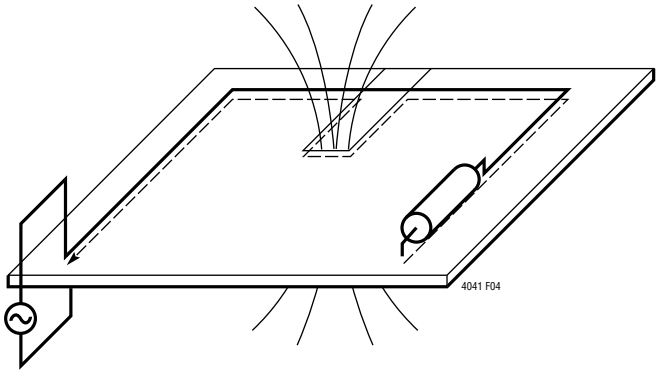
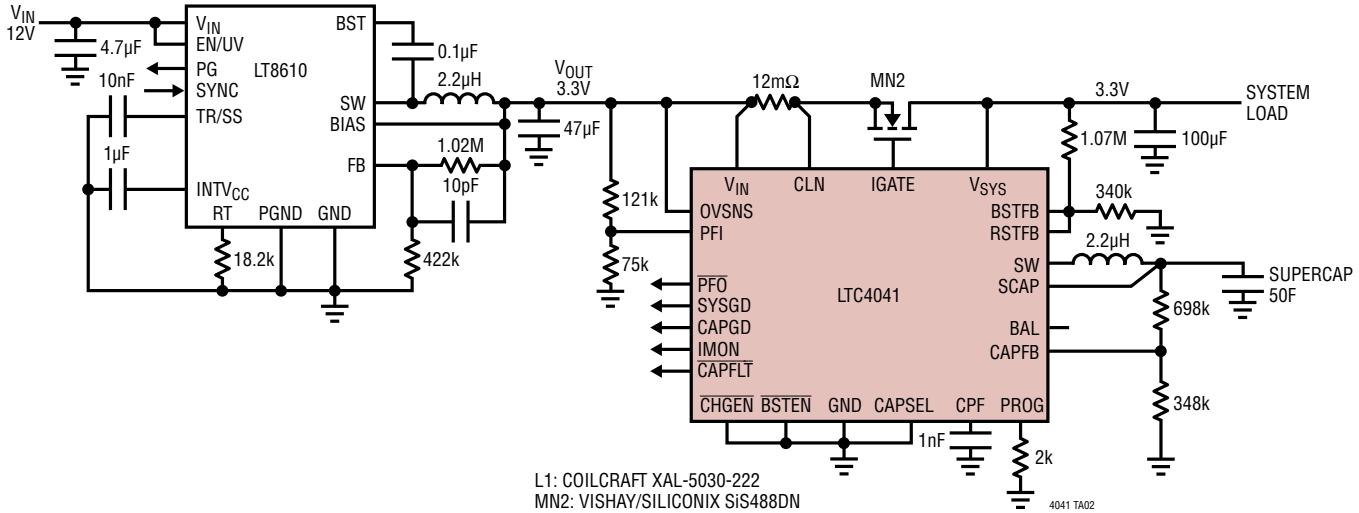


Figure 4. High Frequency Ground Currents Follow Their Incident Path. Slices in the Ground Plane Cause High Voltage and Increased EMI

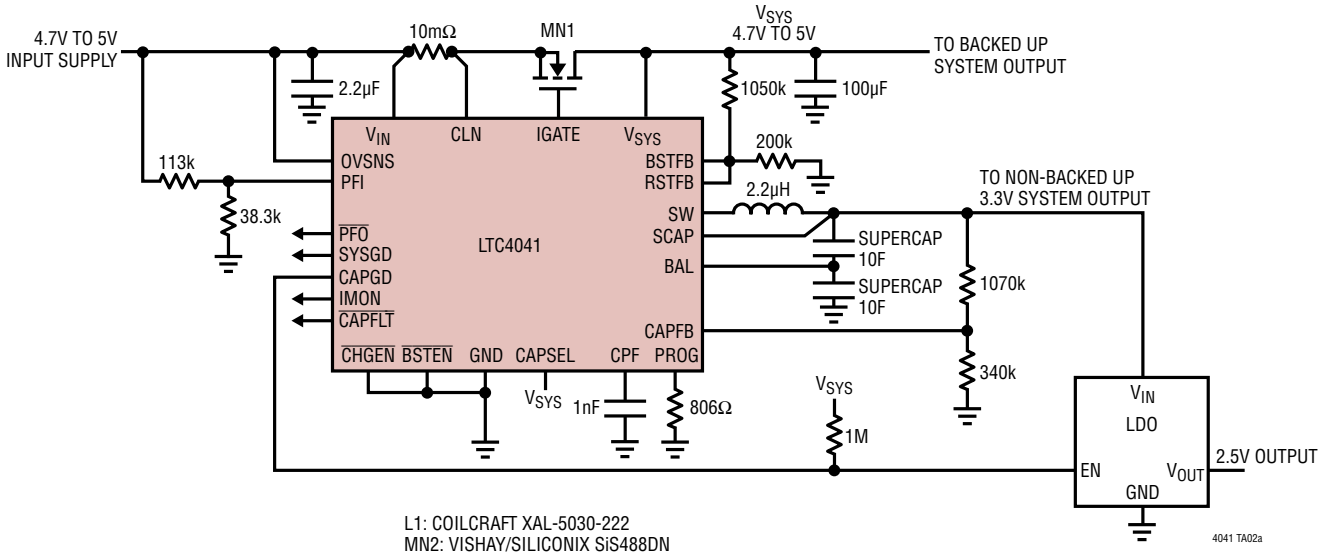
3. The other important components that need to be placed close to the pins are the supercapacitor (connected to the SCAP pin) and the inductor L1. Even though the current through these components is continuous, they can change very abruptly due to a sudden change in load demand. Also, their traces should be wide enough to handle currents as high as the NMOS current limit (typical 6.5A) in backup boost mode.
4. Locate the V_{SYS} dividers for BSTFB and RSTFB near the IC but away from the switching components. Kelvin the top of the resistor dividers to the positive terminal of C_{SYS}. The bottom of the resistor dividers should return to the ground plane away from the hot-loop current path. The same is true for the PFI divider and the CAPFB divider.
5. The exposed pad on the backside of the LTC4041 package must be securely soldered to the PC board ground and also must have a group of vias connecting it to the ground plane for optimum thermal performance. Also this is the only ground pin in the package, and it serves as the return path for both the control circuitry and the switching converter.
6. The IGATE pin for controlling the gates of the external pass transistors has extremely limited drive current. Care must be taken to minimize leakage to adjacent PC board traces. To minimize leakage, the trace can be guarded on the PC board by surrounding it with V_{SYS} connected metal.

TYPICAL APPLICATIONS

3.3V Backup System with 12V Buck for Automotive Application
(Charge Current Setting: 1A, Input Current Limit Setting: 2A)

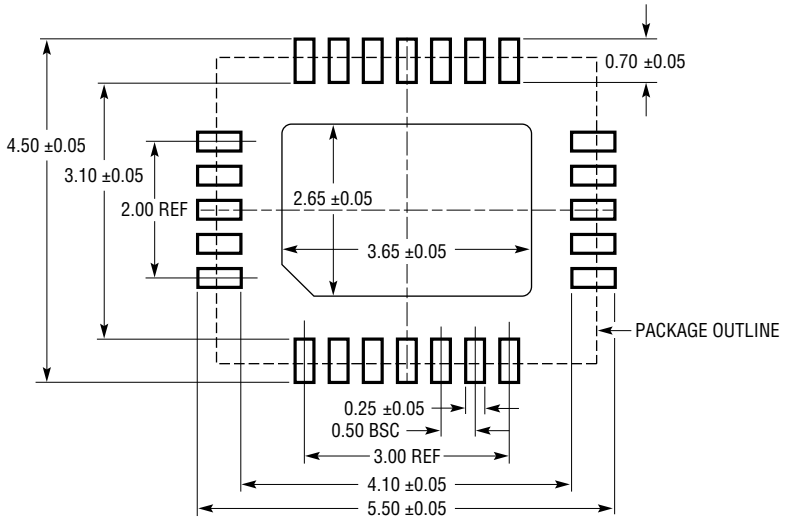


5V Backup Application with Non-Backed Up 3.3V Load Option
(Charge Current Setting: 2.5A, Input Current Limit Setting: 2.5A)

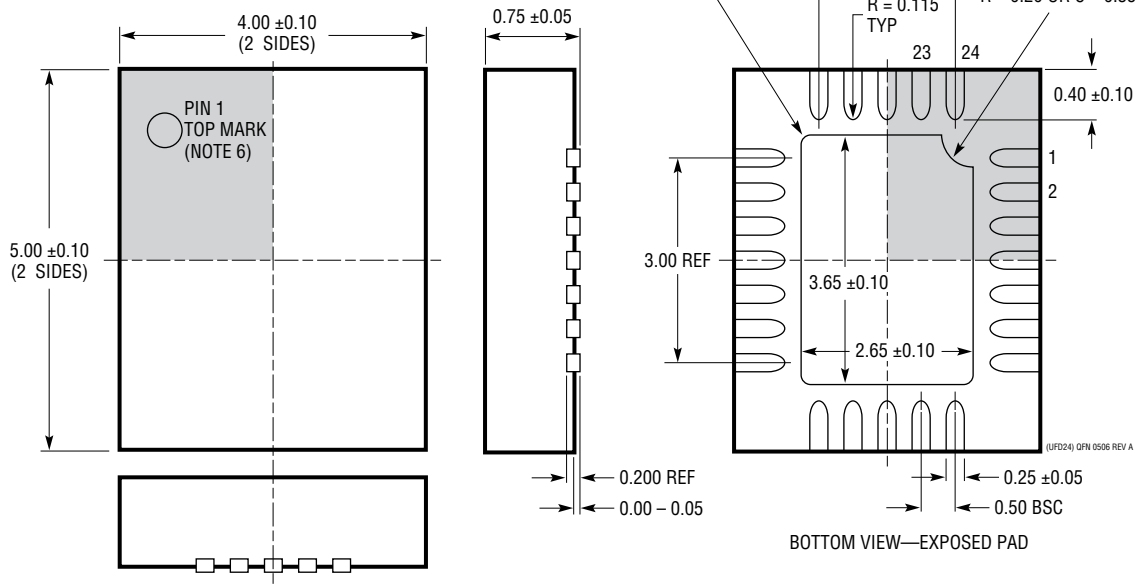


PACKAGE DESCRIPTION

UFD Package
24-Lead Plastic QFN (4mm × 5mm)
(Reference LTC DWG # 05-08-1696 Rev A)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING PROPOSED TO BE MADE A JEDEC PACKAGE OUTLINE MO-220 VARIATION (WXXX-X).
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE
   MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION
   ON THE TOP AND BOTTOM OF PACKAGE

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	01/19	Add Condition to I_{BSTFB} spec	4
		Modified Block Diagram pin numbering	11
		Modified Backup Boost Stability Considerations section	21

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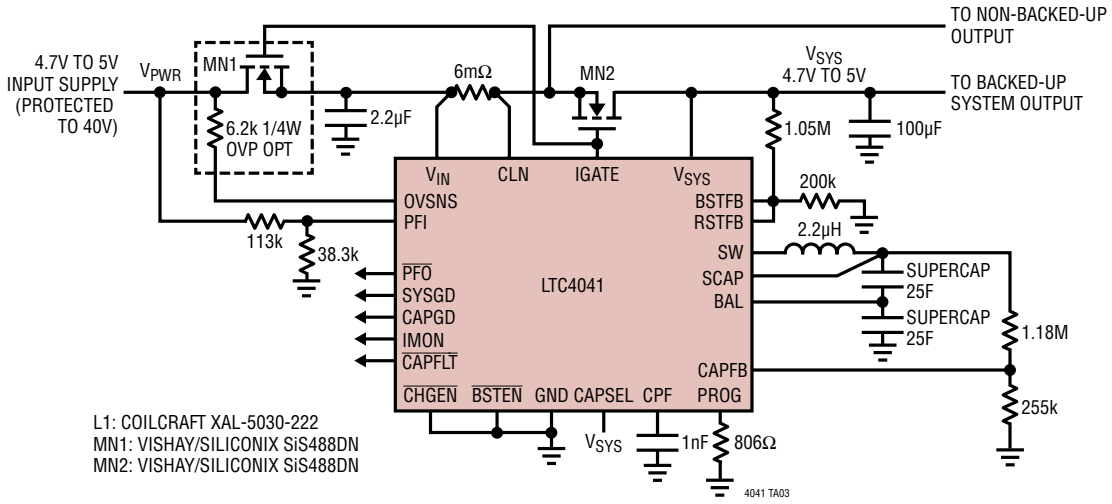
TYPICAL APPLICATION

5V Backup Application with OVP Protection and Non-Backed Up Load Option (Charge Current Setting: 2.5A, Input Current Limit Setting: 4A)



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC3226	2-Cell Supercapacitor Charger with Backup PowerPath™ Controller	1×/2× Multimode Charge Pump Supercapacitor Charger, Internal 2A LDO Backup Supply, PowerPath, Automatic Main/Backup Switchover, Automatic Cell Balancing, Input Voltage Range: 2.5V-5V, 16-Lead 3mm × 3mm QFN Package.
LTC3350/LTC3351	High Current Supercapacitor Backup Controller and System Monitor	High Efficiency Synchronous Step-Down CC-CV Charging of 1-4 Series Supercapacitors, 14-Bit ADC for Monitoring System Voltage/Currents, Capacitance and ESR, Programmable Input Current Limit, V_{IN}: 4.5V to 35V, 38-Lead 5mm × 7mm QFN Package. LTC3351 is Also a Hot Swap Controller.
LTC3355	20V, 1A Buck DC/DC with Integrated SCAP Charger and Backup Regulator	1A Main Buck Regulator, 5A Boost Backup Regulator Powered from Single Supercapacitor, Overvoltage Protection, V_{IN}: 3V to 20V, V_{OUT}: 2.7V to 5V, 20-Lead 4mm × 4mm QFN Package.
LTC4040	2.5A Battery Backup Power Manager	3.5V to 5.5V Supply Rail Battery Backup System, 2.5A Backup from 3.2V Battery, Input Current Limit Prioritizer, Pin Selectable Battery, 24-Lead 4mm × 5mm QFN Package.
LTC4089	USB Power Manager with High Voltage Switching Charger	1.2A Charger for Li-Ion from 6V to 86V Supply , Seamless Transition Between Power Sources, Load Dependent Charging from USB Input, 215mΩ Internal Ideal Diode plus Optional External Ideal Diode Controller, Thermal Regulation, 22-Lead 6mm × 3mm DFN Package
LTC4090	USB Power Manager with 2A High Voltage Bat-Track™ Buck Regulator	Full Featured Li-Ion Battery Charger, 1.5A Maximum Charge Current with Thermal Limiting, NTC Thermistor Input for Temperature Qualified Charging, 22-Lead 3mm × 6mm DFN Package.
LTC4110	Battery Backup System Manager	Complete Manager for Li-Ion/Polymer, Lead Acid, NiMH/NiCd Batteries and Supercapacitors, Input Supply Range: 4.5V to 19V, Programmable Charge Current up to 3A, 38-Lead 5mm × 7mm QFN Package.
LTC4155/LTC4156	Dual Input Power Manager/3.5A Li-Ion Battery Charger with I^2C Control and USB OTG	3.5A Charge Current for Li-Ion/Polymer, LTC4156 for LiFePO4 Batteries, Dual Input Overvoltage Protection Controller, Instant-On Operation with Low Battery, Priority Multiplexing for Multiple Outputs, 28-Lead 4mm × 5mm QFN Package
LTC4160	Switching Power Manager with USB On-The-Go and Overvoltage Protection	USB-OTG 5V Output, Overvoltage Protection, Maximizes Available Power from USB Port, Bat-Track, Instant-On Operation, 1.2A Max Charge Current with Thermal Limiting, 1.2A Max Input Current Limit, 20-Lead 3mm × 4mm QFN Package

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