Secondary Side Synchronous Driver for Push-Pull and Full-Bridge Converters

FEATURES

- **N-Channel Synchronous MOSFET Driver**
- **Programmable Timeout**
- **Reverse Inductor Current Sense**
- Gate Drive Transformer Synchronization Sequence Monitor
- Wide V_{CC} Supply Range: 4.5V to 11V
- 15ns Rise/Fall Times at V_{CC} = 5V, C_L = 4700pF
- Undervoltage Lockout
- Small 16-Lead SSOP Package

APPLICATIONS

- 48V Input Isolated DC/DC Converters
- Isolated Telecom Power Supplies
- Distributed Power Step-Down Converters
- Industrial Control System Power Supplies
- Automotive and Heavy Equipment

DESCRIPTION

The LTC®3901 is a secondary side synchronous rectifier driver designed to be used in isolated push-pull and full-bridge converter power supplies. The chip drives two external N-channel MOSFETs and accepts a transformer-generated bipolar input to maintain sychronization with the primary side controller.

The LTC3901 provides a full range of protection features for the external MOSFETs. A programmable timeout function is included that disables both drivers when the synchronization signal is missing or incorrect. Additionally, the chip senses the output inductor current through the drain-source resistance of the two MOSFETs, turning off the MOSFETs if the inductor current reverses. The LTC3901 also shuts off the drivers if the supply is low or if the synchronization sequence is incorrect.

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TYPICAL APPLICATION

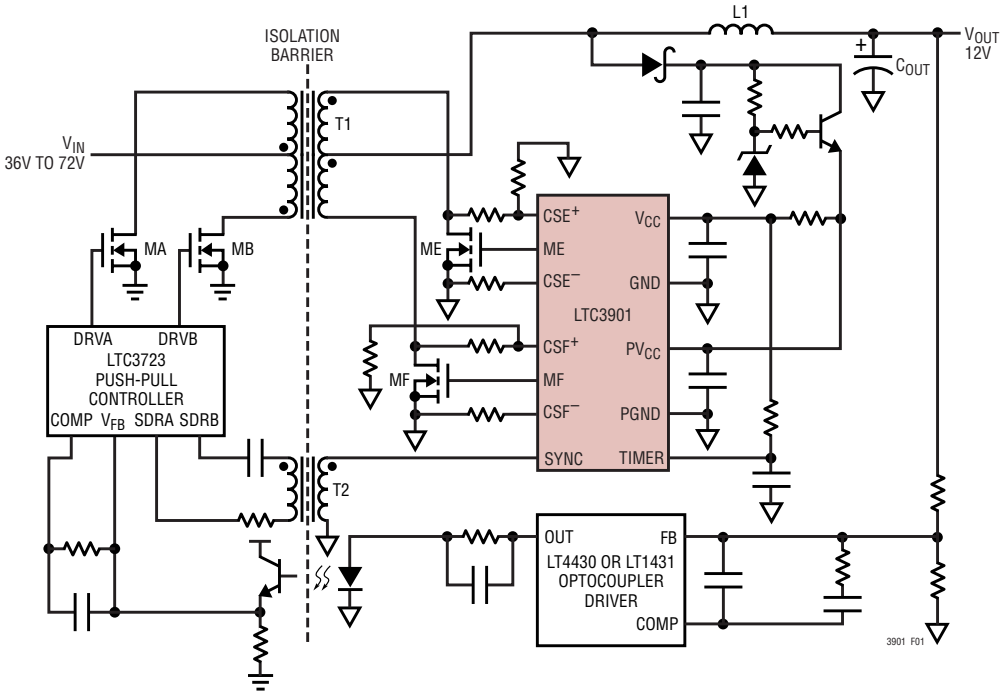


Figure 1. Simplified Isolated Push-Pull Converter

ABSOLUTE MAXIMUM RATINGS

(Note 1)

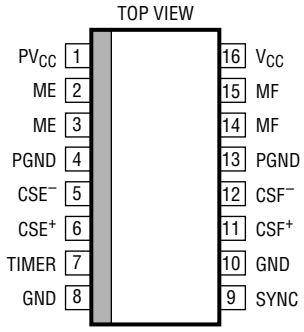
Supply Voltage
- V_{CC}, PV_{CC} 12V

Input Voltage
- CSE^-, CSF^-, TIMER ..... –0.3V to (V_{CC} + 0.3V)
- SYNC ..... –12V to 12V

Input Current
- CSE^+, CSF^+ 15mA

Operating Temperature Range (Note 2) ...–40°C to 85°C
Storage Temperature Range .....–65°C to 150°C
Lead Temperature (Soldering, 10 sec).....300°C

PACKAGE/ORDER INFORMATION



GN PACKAGE
16-LEAD NARROW PLASTIC SSOP
T_{JMAX} = 125°C, θ_{JA} = 130°C/W

ORDER PART NUMBER
LTC3901EGN
GN PART MARKING
3901

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range. V_{CC} = 5V, T_A = 25°C unless otherwise specified. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CC}	Supply Voltage Range		●	4.5	5	11	V
V_{UVLO}	V_{CC} Undervoltage Lockout Threshold V_{CC} Undervoltage Lockout Hysteresis	Rising Edge Rising Edge to Falling Edge	●		4.1 0.5	4.5	V V
I_{VCC}	V_{CC} Supply Current	V_{SYNC} = 0V f_{SYNC} = 100kHz, C_{ME} = C_{MF} = 4700pF (Note 4)	● ●		0.5 7	1 15	mA mA
Timer							
V_{TMR}	Timer Threshold Voltage		●	–10%	V_{CC}/5	10%	V
I_{TMR}	Timer Input Current	V_{TMR} = 0V	●		–6	–10	µA
t_{TMRDIS}	Timer Discharge Time	C_{TMR} = 1000pF, R_{TMR} = 4.7k	●		40	120	ns
V_{TMRMAX}	Timer Pin Clamp Voltage	C_{TMR} = 1000pF, R_{TMR} = 4.7k			2.5		V
Current Sense (Note 5)							
I_{CS+}	CS^+ Input Current	V_{CS+} = 0V	●			±1	µA
$I_{CS–}$	$CS^–$ Input Current	$V_{CS–}$ = 0V	●			±1	µA
V_{CSMAX}	CS^+ Pin Clamp Voltage	I_{IN} = 5mA, Driver Off			11		V
V_{CS}	Current Sense Threshold Voltage	$V_{CS–}$ = 0V (Note 6)	 ●	7.5 3	10.5	13.5 18	mV mV
SYNC Input							
I_{SYNC}	SYNC Input Current	V_{SYNC} = ±10V	●		±1	±10	µA
V_{SYNCP}	SYNC Input Positive Threshold SYNC Positive Input Hysteresis	(Note 7)	●	1.0	1.4 0.2	1.8	V V
V_{SYNCN}	SYNC Input Negative Threshold SYNC Negative Input Hysteresis	(Note 7)	●	–1.8	–1.4 0.2	–1.0	V V
Driver Output							
R_{ONH}	Driver Pull-Up Resistance	I_{OUT} = –100mA	 ●		0.9	1.2 1.6	Ω
R_{ONL}	Driver Pull-Down Resistance	I_{OUT} = 100mA	 ●		0.8	1.2 1.6	Ω
I_{PK}	Driver Peak Output Current	(Note 7)			2		A

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range. V_{CC} = 5V, T_A = 25°C unless otherwise specified. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Switching Characteristics (Note 8)							
t_d	SYNC Input to Driver Output Delay	C_{ME} = C_{MF} = 4700pF, V_{SYNC} = ±5V	●		60	120	ns
t_r, t_f	Driver Rise/Fall Time	C_{ME} = C_{MF} = 4700pF, V_{SYNC} = ±5V			15		ns

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: The LTC3901E is guaranteed to meet performance specifications from 0°C to 70°C. Specifications over the –40°C to 85°C operating temperature range are assured by design; characterization and correlation with statistical process controls.

Note 3: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.

Note 4: Supply current in normal operation is dominated by the current needed to charge and discharge the external MOSFET gates. This current will vary with supply voltage, switching frequency and the external MOSFETs used.

Note 5: Both CSE^+, CSE^- and CSF^+, CSF^- current sense comparators have the same performance specifications.

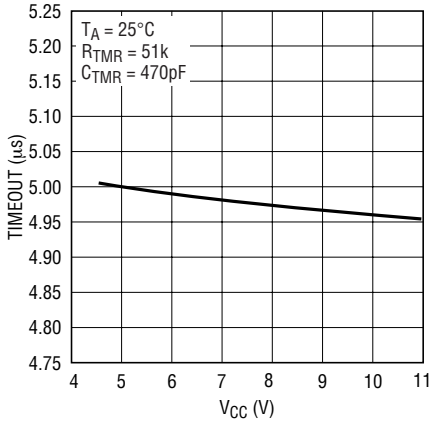
Note 6: The current sense comparator threshold has a 0.33%/°C temperature coefficient (TC) to match the TC of the external MOSFET R_{DSON}.

Note 7: Guaranteed by design, not subject to test.

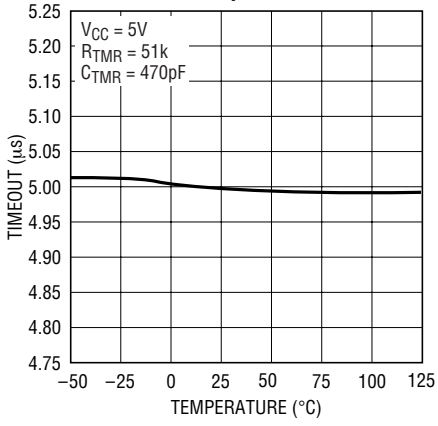
Note 8: Rise and fall times are measured using 10% and 90% levels. Delay times are measured from ±1.4V at SYNC input to 20%/80% levels at the driver output.

TYPICAL PERFORMANCE CHARACTERISTICS

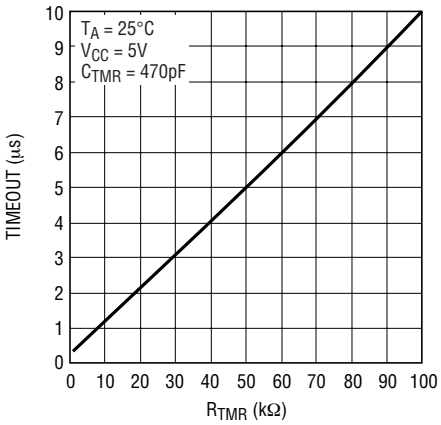
Timeout vs V_{CC}



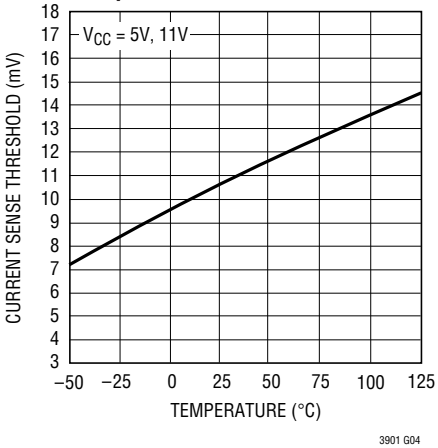
Timeout vs Temperature



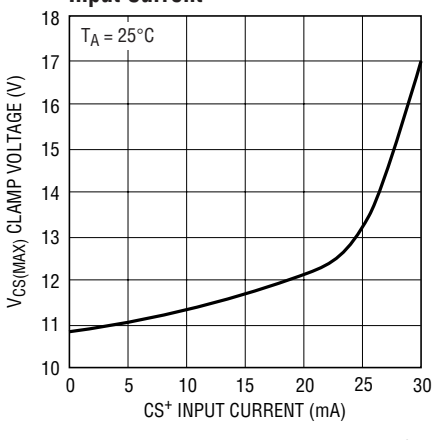
Timeout vs R_{TMR}



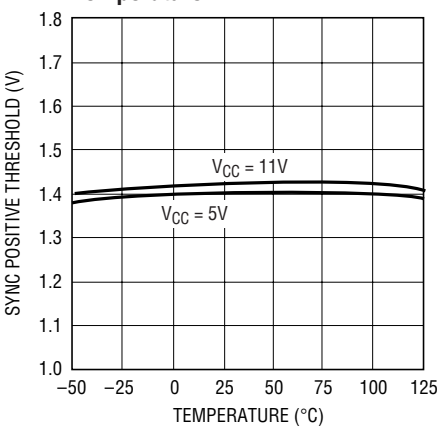
Current Sense Threshold vs Temperature



$V_{CS(MAX)}$ Clamp Voltage vs CS^+ Input Current

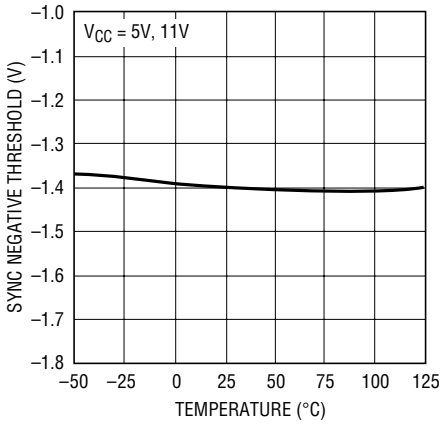


SYNC Positive Threshold vs Temperature

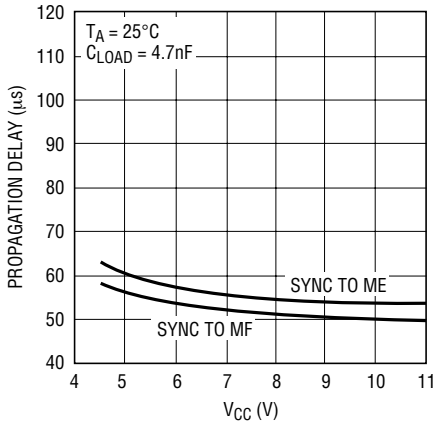


TYPICAL PERFORMANCE CHARACTERISTICS

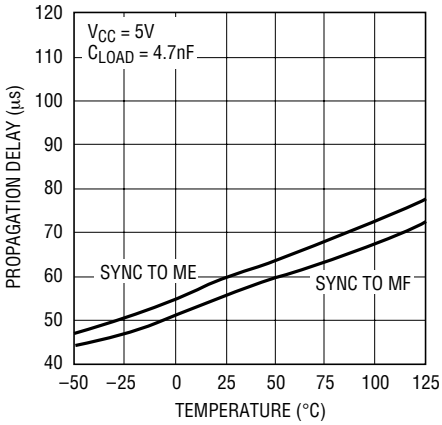
SYNC Negative Threshold vs Temperature



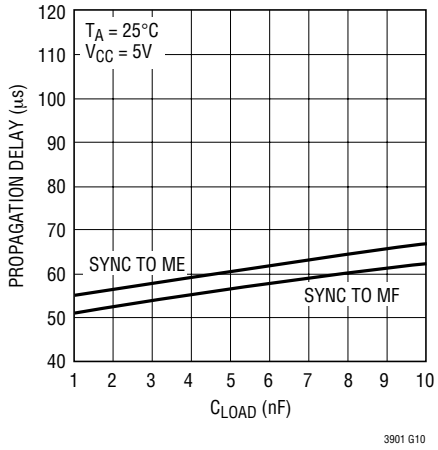
Propagation Delay vs V_{CC}



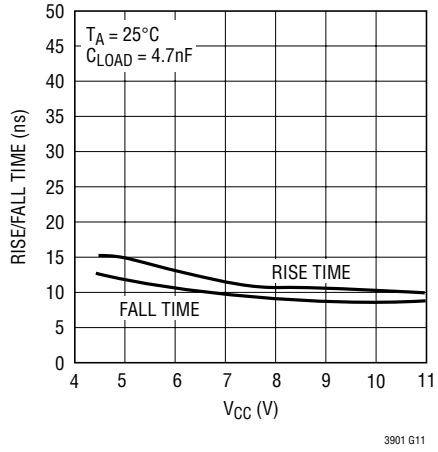
Propagation Delay vs Temperature



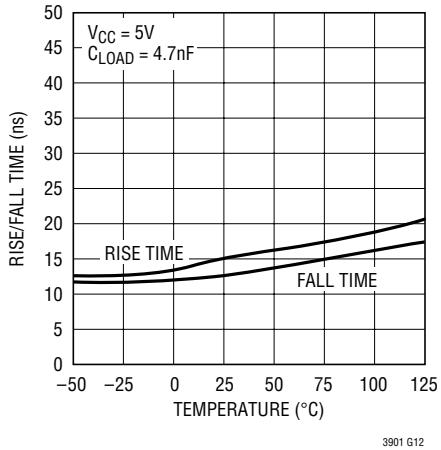
Propagation Delay vs C_{LOAD}



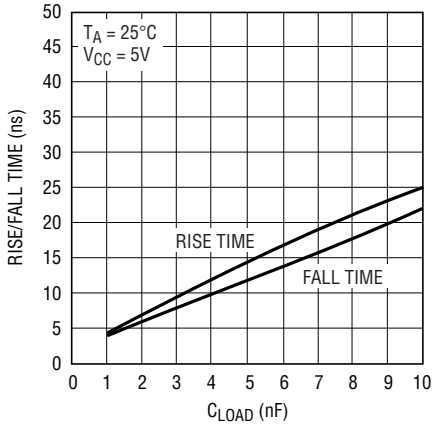
Rise/Fall Time vs V_{CC}



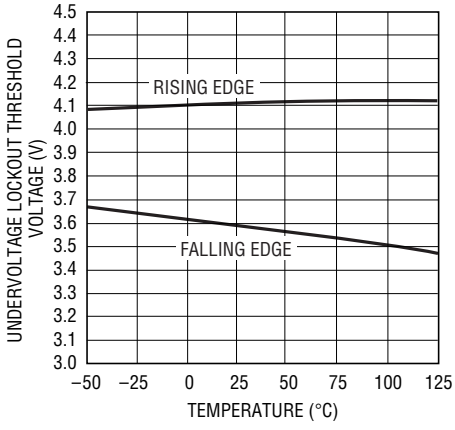
Rise/Fall Time vs Temperature



Rise/Fall Time vs Load Capacitance

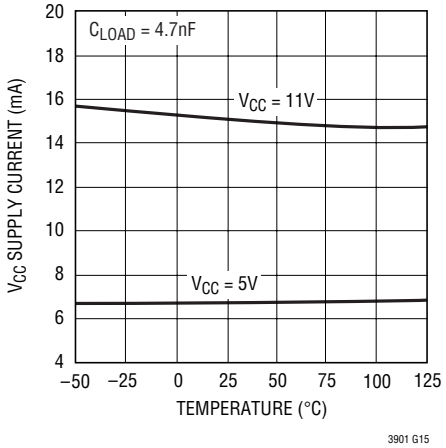


Undervoltage Lockout Threshold Voltage vs Temperature

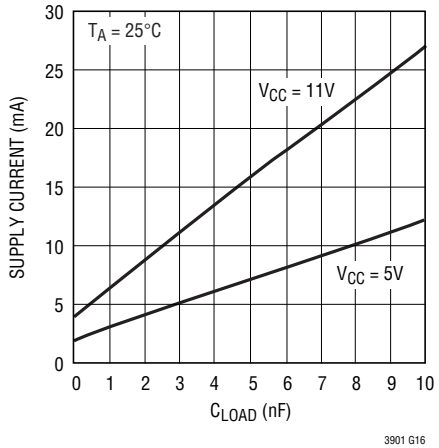


TYPICAL PERFORMANCE CHARACTERISTICS

V_{CC} Supply Current vs Temperature



V_{CC} Supply Current vs Load Capacitance



PIN FUNCTIONS

PV_{CC} (Pin 1): Driver Supply Input. This pin powers the ME and MF drivers. Bypass this pin to PGND using a 4.7µF low ESR capacitor in close proximity to the LTC3901. This pin should be connected to the same supply voltage as the V_{CC} pin.

ME (Pin 2, 3): Driver Output for ME. This pin drives the gate of the external N-channel MOSFET, ME.

PGND (Pin 4,13): Power Ground. Both drivers return to this pin. Connect PGND to a high current ground node in close proximity to the sources of ME and MF.

CSE^+, CSE^- (Pin 6, 5): ME Current Sense Differential Input. Connect CSE^+ through a series resistor to the drain of ME and CSE^- through a series resistor to the source of ME. The LTC3901 monitors the CSE inputs 250ns after ME goes high. If the inductor current reverses and flows into ME causing CSE^+ to rise above CSE^- by more than 10.5mV, the LTC3901 pulls ME low. See the Current Sense section for more details on choosing the resistance values for R_{CSE1} to R_{CSE3}.

TIMER (Pin 7): Timer Input. Connect this pin to an external R-C network to program the timeout period. The LTC3901 resets the timer at every positive and negative transition of the SYNC input. If the SYNC signal is missing or incorrect, the LTC3901 pulls both ME and MF low once the TIMER pin goes above the timeout threshold. See the Timer section for more details on programming the timeout period.

GND (Pin 8,10): Signal Ground. All internal low power circuitry returns to this pin. To minimize differential ground currents, connect GND to PGND right at the LTC3901.

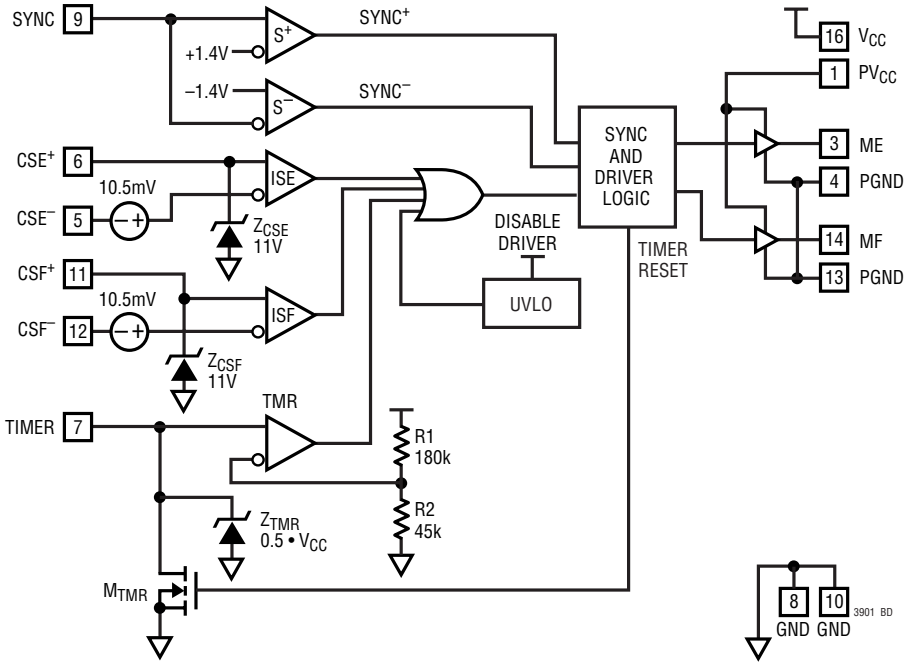
SYNC (Pin 9): Driver Synchronization Input. 0V at this pin forces both ME and MF high after an initial negative pulse. A subsequent positive pulse at SYNC input forces ME to pull low, whereas a negative pulse forces MF to pull low. The SYNC signal should alternate between positive and negative pulses. If the SYNC signal is incorrect, the LTC3901 pulls both MF and ME low.

CSF^+, CSF^- (Pin 11, 12): MF Current Sense Differential Input. Connect CSF^+ through a series resistor to the drain of MF and CSF^- through a series resistor to the source of MF. The LTC3901 monitors the CSF inputs 250ns after MF goes high. If the inductor current reverses and flows into MF causing CSF^+ to rise above CSF^- by more than 10.5mV, the LTC3901 pulls MF low. See the Current Sense section for more details on choosing the resistance values for R_{CSF1} to R_{CSF3}.

MF (Pin 14, 15): Driver Output for MF. This pin drives the gate of the external N-channel MOSFET, MF.

V_{CC} (Pin 16): Power Supply Input. All internal circuits except the drivers are powered from this pin. Bypass this pin to GND using a 1µF capacitor in close proximity to the LTC3901.

BLOCK DIAGRAM



APPLICATIONS INFORMATION

Overview

Push-pull and full bridge converters use power transformers to provide input-to-output isolation and voltage step-up/down. Diodes are used as a simple solution for secondary side rectification. Unfortunately, as output currents increase, the loss associated with diode forward voltage drop results in low overall efficiency. The LTC3901 overcomes this problem by providing control and drive for two external N-channel synchronous MOSFETs. Synchronization to the primary side controller is maintained through a small signal transformer.

Figure 1 shows a simplified push-pull converter application. T1 is the power transformer; MA and MB are the primary side power transistors driven by the LTC3723 controller's DRVA and DRVB outputs. The gate drive transformer T2 is driven by the LTC3723's SDRA and SDRB outputs and provides the synchronization signal to the LTC3901 on the secondary side. When both SDRA and SDRB are high, there is no voltage across the transformer's primary and the LTC3901 SYNC input is approximately 0V. According to the polarity of the transformer: if SDRA goes low while SDRB is high, SYNC is positive; if SDRB goes low while SDRA is high, SYNC is negative. ME and MF are the secondary side synchronous switches driven by the LTC3901's ME and MF output. Inductor L1 and capacitor C_{OUT} form the output filter, providing DC output voltage to the load. The feedback path from V_{OUT} through the optocoupler driver and optocoupler back to the primary side controller is also shown in Figure 1.

Each full cycle of the push-pull converter consists of four distinct periods. Figure 2 shows the push-pull converter waveforms.

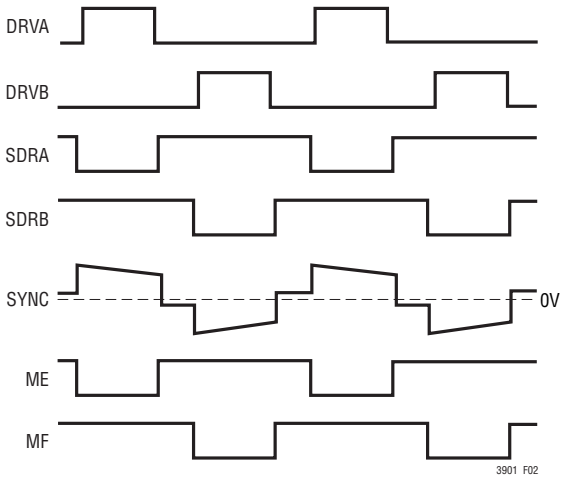


Figure 2. Push-Pull Converter Switching Waveforms

APPLICATIONS INFORMATION

In the first period, SDRA goes low (followed by DRVA going high) and T2 generates a positive voltage at the LTC3901's SYNC input. The LTC3901's ME output then pulls low. Current flows to the load through MOSFET MF, T1's secondary and L1.

In the second period, SDRA goes high and T2 provides approximately 0V at the LTC3901 SYNC input. This causes the LTC3901's ME output to go high and both MOSFET ME and MF to conduct. This is the free-wheeling period with T1 secondary winding shorted.

In the third period, SDRB goes low (followed by DRVB going high) and T2 generates a negative voltage at the LTC3901's SYNC input. The LTC3901's MF output then pulls low. Current flows to the load through MOSFET ME, T1's secondary and L1.

The last period is also a free-wheeling period like the second period. Both SDRA and SDRB are high and the LTC3901 forces both MOSFETs ME and MF to conduct.

External MOSFET Protection

A programmable timer and two differential input current sense comparators are included in the LTC3901 for protection of the external MOSFETs during power down and Burst Mode® operation. The chip also shuts off the MOSFETs if $V_{CC} < 4.1V$ or if the synchronization sequence is incorrect.

When the primary controller is powering down, the LTC3901 continues to operate by drawing power from the V_{CC} bypass cap, C_{VCC}. The primary controller synchronous output stops switching and the LTC3901 SYNC input goes to 0V. Both ME and MF remain on and the decreasing inductor current continues to flow into the load. Once the inductor current decreases to zero, it reverses direction, discharging the output capacitor C_{OUT} to GND through both MOSFETs. At the same time, the C_{VCC} voltage continues to drop. When the voltage drops below 4.1V, the LTC3901 shuts down and pulls both ME and MF low. This causes the inductor current to stop suddenly and the drain voltage of both MOSFETs to fly high, due to the buildup of inductor energy. In the absence of a protection timer, if the inductor energy is high due to a long period of current reversal, the drain voltage can go above the MOSFET's voltage rating and cause damage to the MOSFET.

MOSFETs are also kept on for long periods when the primary controller enters Burst Mode operation. Both ME and MF stop switching until the primary controller exits Burst Mode operation. This would also cause the inductor current to reverse and the drains to fly high.

In both of these situations, the timer and/or current sense comparator shuts off the drivers before or immediately after the inductor current reverses direction. This prevents the buildup of inductor energy.

Timer

The timer circuit (Figure 3) operates by using an external R-C charging network to program the timeout period. On every transition at the SYNC input, the chip generates a 200ns pulse to reset the timer capacitor. If the SYNC signal is missing or incorrect (allowing the timer capacitor voltage to go high) it shuts off both drivers once the voltage reaches the timeout threshold. Figure 4 shows the timer waveforms.

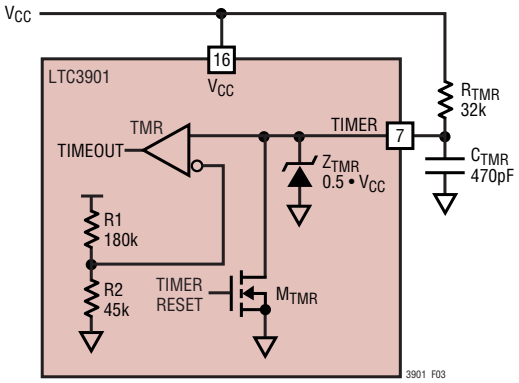


Figure 3. Timer Circuit

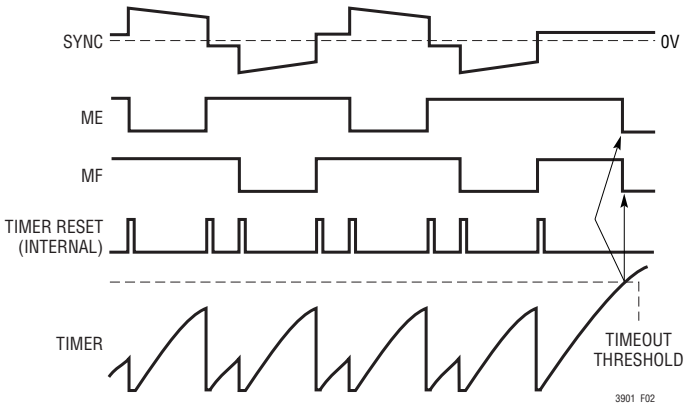


Figure 4. Timer Waveforms

Burst Mode is a registered trademark of Linear Technology Corporation.

APPLICATIONS INFORMATION

The timeout period is determined predominantly by the external R_{TMR} and C_{TMR} values and is independent of the V_{CC} voltage. This independence is achieved by making the timeout threshold a ratio of V_{CC}. The ratio is 0.2x, set internally by R1 and R2 (see Figure 3). The Timeout period should be programmed to around 1 period of the primary switching frequency using the following formula:

$$TIMEOUT = 0.2 \bullet R_{TMR} \bullet C_{TMR} + 0.27E\text{-}06$$

To reduce error in the timeout setting due to the discharge time, select C_{TMR} between 100pF and 1000pF. Start with a C_{TMR} around 470pF and then calculate the required R_{TMR}. C_{TMR} should be placed as close as possible to the LTC3901 with minimum PCB trace between C_{TMR}, the TIMER pin and GND. This is to reduce any ringing caused by the PCB trace inductance when C_{TMR} discharges. This ringing may introduce error to the timeout setting.

The timer input also includes a current sinking clamp circuit (Z_{TMR} in Figure 3) that clamps this pin to about $0.5 \bullet V_{CC}$ if there is missing SYNC/timer reset pulse. This clamp circuit prevents the timer capacitor from getting fully charged up to the rail, which would result in a longer discharge time. The current sinking capability of the circuit is around 1mA.

The timeout function can be disabled by connecting the timer pin to GND.

Synchronization Sequence

A typical push-pull converter cycle always turns off ME and MF alternately. The SYNC input should alternate between a positive and negative pulse. The LTC3901 includes a sequential logic to monitor the SYNC input pulses. If after one positive pulse the SYNC comparator receives another positive pulse, the LTC3901 sequential logic shuts off both drivers until a negative pulse appears. The same applies to double negative pulses; the driver will turn on only after receiving a positive pulse. This is to protect the external components in situations where only one polarity of the SYNC pulse is present and the corresponding driver remains on. Figure 5 shows the SYNC double pulse operation.

The LTC3901 has two separate SYNC comparators (S^+ and S^- in the Block Diagram) to detect the positive and negative pulses. The threshold voltages of both comparators are designed to be of the same magnitude but opposite in polarity. In some situations, for example during power-up or power-down, the SYNC pulse magnitude may be low (slightly higher or lower than the threshold of the comparators). This can cause only one of the SYNC comparators to trip. This also appears as a double pulse to the sequential logic and both drivers will be shut off.

Current Sense

The differential input current sense comparators, ISE and ISF (Figure 6), are used for sensing the voltage across the drain-to-source terminal of the MOSFET through the CSX^+ and CSX^- pins. There are two sets of comparator inputs, one for each MOSFET (ME and MF). If the inductor current reverses into the MOSFET causing CSX^+ to rise above CSX^- by more than 10.5mV, the LTC3901 turns off the respective MOSFET. This comparator is used to prevent inductor reverse current buildup during power-down or Burst Mode operation, which may cause damage to the MOSFETs. The 10.5mV input threshold has a positive temperature coefficient, which closely matches the TC of the external MOSFET $R_{DS(ON)}$. The current sense comparator is only active 250ns after the respective driver

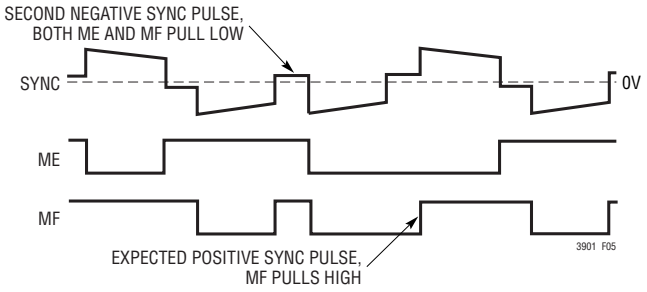


Figure 5. SYNC Double Pulse Operation

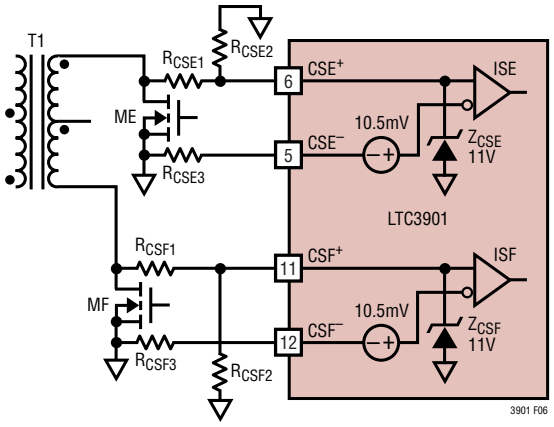


Figure 6. Current Sense Circuit

APPLICATIONS INFORMATION

output goes high; this is to avoid any ringing immediately after the MOSFETs are switched on.

Under no/light load conditions, if the inductor average current is less than half of its peak-to-peak ripple current, the inductor current will reverse into MOSFETs during a portion of the free-wheeling period, forcing CSX+ to rise above CSX–. The current sense comparator input threshold is set at 10.5mV to prevent tripping under this normal no load condition. If at no load, the product of the inductor negative peak current and MOSFET $R_{DS(ON)}$ is higher than 10.5mV; this may trip the comparator and force the LTC3901 to operate in discontinuous mode. Figure 7 shows the LTC3901 operating in discontinuous mode; the driver's output goes low before the next SYNC transition edge when the inductor current goes negative. In push-pull topology, both MOSFETs conduct the same amount of current during the free-wheeling period; this will trip both comparators at the same time. Discontinuous mode is sometimes undesirable because if the load current suddenly increases when the MOSFETs are off, it creates a large output voltage drop. To overcome this, add a resistor divider, R_{CSX1} and R_{CSX2} at the CSX+ pin to increase the 10.5mV threshold so that the LTC3901 operates in continuous mode at no load.

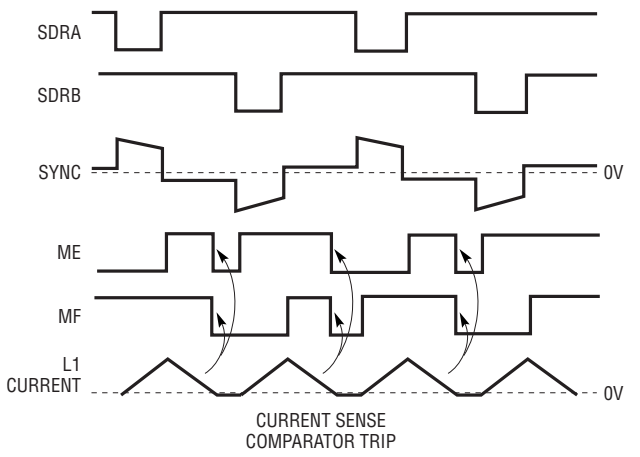


Figure 7a. Discontinuous Mode Operation at No Load

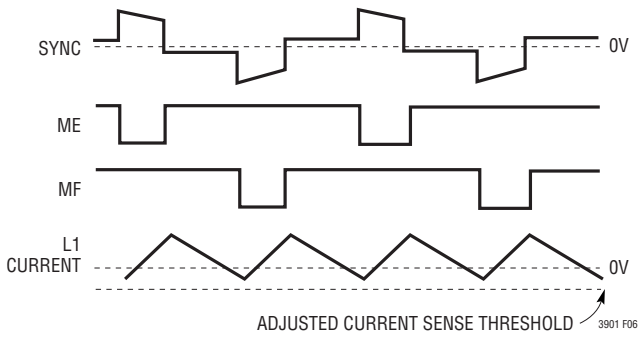


Figure 7b. Continuous Mode Operation with Adjusted Current Sense Threshold

The LTC3901 CSX+ pin has an internal current sinking clamp circuit (Z_{CSX}) that clamps the pin to around 11V. The clamp circuit, together with the external series resistor $R_{CSX}1$, protects the CSX+ pins from the high MOSFET drain voltage in the power delivery cycle. During the power delivery cycle, one of the MOSFETs (ME or MF) is off. The drain voltage of the MOSFET that is off is determined by the primary input voltage and the transformer turn ratio. This voltage can be high and may damage the internal circuit if CSX+ is connected directly to the drain of its MOSFET. The current sinking capability of the clamp circuit is 5mA minimum.

The value of the resistorsR_{CSX1}, R_{CSX2} and R_{CSX3} should be calculated using the following formulas to meet both the clamp and threshold voltage requirements:

$$k = \{48 \bullet I_{RIPPLE} \bullet R_{DS(ON)}\} - 1$$

$$R_{CSX2} = \{200 \bullet V_{IN(MAX)} \bullet N_S/N_P - 2200 \bullet (1 + k)\} / k$$

$$R_{CSX1} = k \bullet R_{CSX2}$$

$$R_{CSX3} = \{R_{CSX1} \bullet R_{CSX2}\} / \{R_{CSX1} + R_{CSX2}\}$$

If k = 0 or less than zero, R_{CSX2} is not needed and $R_{CSX1} = R_{CSX3} = \{V_{IN(MAX)} \bullet (N_S/N_P) - 11V\} / 5mA$

where:

I_{RIPPLE} = Inductor peak-to-peak ripple current

$R_{DS(ON)}$ = On-resistance of MOSFET at $I_{RIPPLE}/2$

$V_{IN(MAX)}$ = Primary side main supply maximum input voltage

N_S/N_P = Power transformer T1, turn ratio

If the LTC3901 still operates in discontinuous mode with the calculated resistance value, increase the value of R_{CSX1} to raise the threshold. The resistors R_{CSX1} and R_{CSX2} and the CSX+ pins input capacitance plus the PCB trace capacitance forms an R-C delay; this slows down the response time of the comparators. The resistors and CSX+ input leakage currents also create an input offset error.

To minimize this delay and error, do not use resistance value higher than required and make the PCB trace from

APPLICATIONS INFORMATION

the resistors to the LTC3901 CSX^+/CSX^- pins as short as possible . Add a series resistor, R_{CSX3}, with value equal to parallel sum of R_{CSX1} and R_{CSX2} to the CSX^- pin and connect the other end of R_{CSX3} directly to the source of the MOSFET.

SYNC Input

Figure 8 shows the external circuit for the LTC3901 SYNC input. The gate drive transformer (T2) should be selected based on the primary switching frequency and SDRA/SDRB output voltage.

The values of the C_{SG} and R_{SYNC} should then be adjusted to obtain a optimum SYNC pulse shape and amplitude. The amplitude of the SYNC pulse should be much higher than the LTC3901 SYNC threshold of ±1.4V. Amplitudes greater than ±5V will help to speed up the SYNC comparator and reduce the propagation delay from SYNC to the drivers. When SDRA and SDRB lines go low, the resulting undershoot or overshoot must not exceed the minimum SYNC threshold of ±1V.

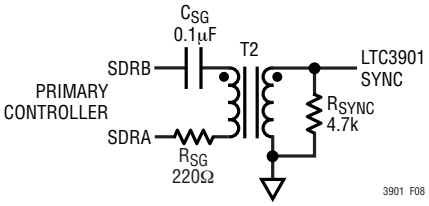


Figure 8. SYNC Input Circuit

V_{CC}/PV_{CC} Regulator

The V_{CC}/PV_{CC} supply for the LTC3901 can be generated by peak rectifying the transformer secondary winding as shown in Figure 9. The Zener diode D_Z sets the output voltage (V_Z – 0.7V). Resistor R_B (on the order of a few hundred ohms), in series with the base of Q_{REG}, may be required to surpress high frequency oscillations depending on Q_{REG}'s selection. A power MOSFET can also be used by increasing the zener diode value to offset the drop of the gate-to-source voltage. The V_{CC} input is separated from the PV_{CC} input through a 100Ω resistor. This lowers the driver switching feedthrough. Connect a 1µF bypass capacitor for the V_{CC} supply. PV_{CC} supply current varies linearly with the supply voltage, driver load and clock frequency. A 4.7µF bypass capacitor for the PV_{CC} supply is sufficient for most applications. Alternatively, the LTC3901 can be powered directly by V_{OUT} if the voltage is

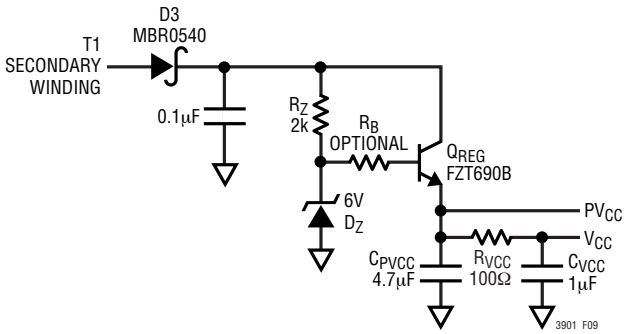


Figure 9. V_{CC}/PV_{CC} Regulator

higher than 4.5V. This reduces the number of external components needed.

The LTC3901 has an UVLO detector that pulls the drivers' output low if V_{CC} < 4.1V. The output remains off from V_{CC} = 1V to 4.1V. The UVLO detector has 0.5V of hysteresis to prevent chattering.

In a typical push-pull converter, the secondary side circuits have no power until the primary side controller starts operating. Since power for the LTC3901 is derived from the power transformer T1, the LTC3901 will initially remain off. During this period (V_{CC} < 4.1V), the synchronous MOSFETs ME and MF will remain off and the MOSFETs' body diodes will conduct. The MOSFETs may experience very high power dissipation due to a high voltage drop in the body diodes. To prevent MOSFET damage, a V_{CC} voltage greater than 4.1V should be provided quickly. The V_{CC} supply circuit in Figure 9 will provide power for the LTC3901 within the first few switching pulses of the primary controller, preventing overheating of the MOSFETs.

Full-Bridge Converter Application

The LTC3901 can be used in full-bridge converter applications. Figure 10 shows a simplified full-bridge converter circuit. The LTC3901 circuit and operation is the same as in the push-pull application (refer to Figure 1). On the primary side there are four power MOSFETs, MA to MD, driven by the respective outputs of the primary controller. Transformer T3 and T4 step up the gate drives for MA and MC.

Each full cycle of the full-bridge converter includes four distinct periods which are similar to those found in the push-pull application. Figure 11 shows the full-bridge converter switching waveforms. The shaded areas correspond to power delivery periods.

APPLICATIONS INFORMATION

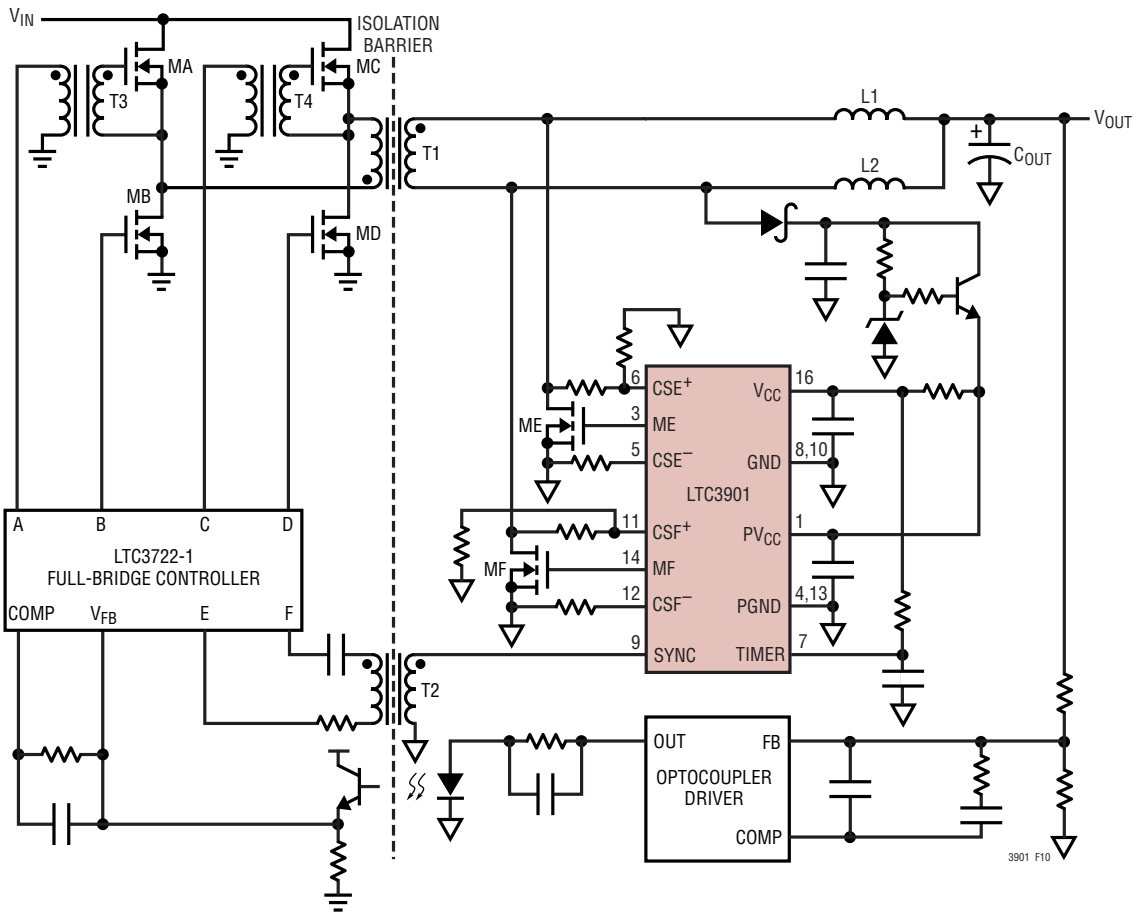


Figure 10. Simplified Isolated Full-Bridge Converter

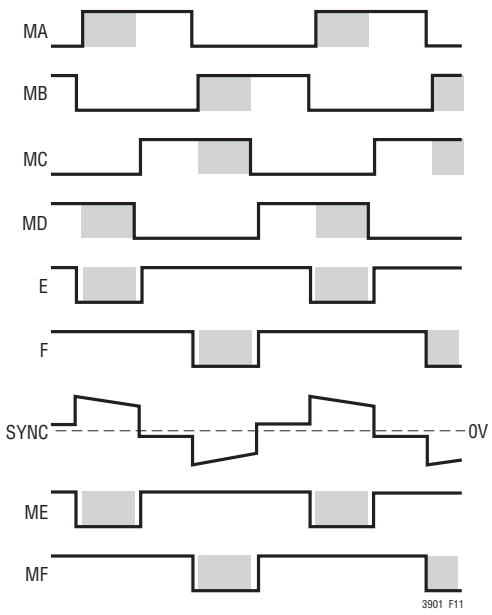


Figure 11. Full-Bridge Converter Switching Waveforms

In the first period, MB turns off, E goes low (followed by MA turning on), and the LTC3901 forces ME to turn off. The primary side delivers power to the load through MOSFET MF, T1 and L1.

In the second period, MA remains on, MD turns off, and MC turns on. E goes high and the LTC3901 forces both ME and MF to conduct. This is the free-wheeling period with the T1 secondary output shorted.

In the third period, MA turns off, F goes low (followed by MB turning on), and the LTC3901 forces MF to turn off. The primary side delivers power to the load through MOSFET ME, T1 and L2.

Like the second period, the last period is a free-wheeling period. MB remains on, MC turns off, MD turns on, F goes high, and the LTC3901 forces both ME and MF to conduct. The timeout and current sense operations are the same as in the push-pull application.

APPLICATIONS INFORMATION

MOSFET Selection

The required MOSFET $R_{DS(ON)}$ should be determined based on allowable power dissipation and maximum required output current.

The MOSFETs body diodes conduct during the power-up phase, when the LTC3901 V_{CC} supply is ramping up. The ME and MF signals stay low and the inductor current flows through the body diodes. The body diodes must be able to handle the load current during start-up until V_{CC} reaches 4.1V.

The LTC3901 drivers dissipate power while the MOSFETs are switching. The power dissipation increases with switching frequency, PV_{CC}, and size of the MOSFETs. To calculate the driver dissipation, the total gate charge Q_G is used. This parameter is found on the MOSFET manufacturers' data sheets.

The power dissipated in each LTC3901 MOSFET driver is:

$$P_{DRIVER} = Q_G \bullet PV_{CC} \bullet f_{SW}$$

where f_{SW} is the switching frequency of the converter.

PC Board Layout Checklist

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the LTC3901:

1. Connect the 1µF C_{VCC} bypass capacitor as close as possible to the V_{CC} and GND pins. Connect the 4.7µF C_{PVCC} bypass capacitor as close as possible to the PV_{CC} and PGND pins.

2. Connect the two MOSFET drain terminals directly to the transformer. The two MOSFET sources should be as close together as possible.

3. Keep the timer, SYNC and V_{CC} regulator circuit away from the high current path of ME, MF and T1.

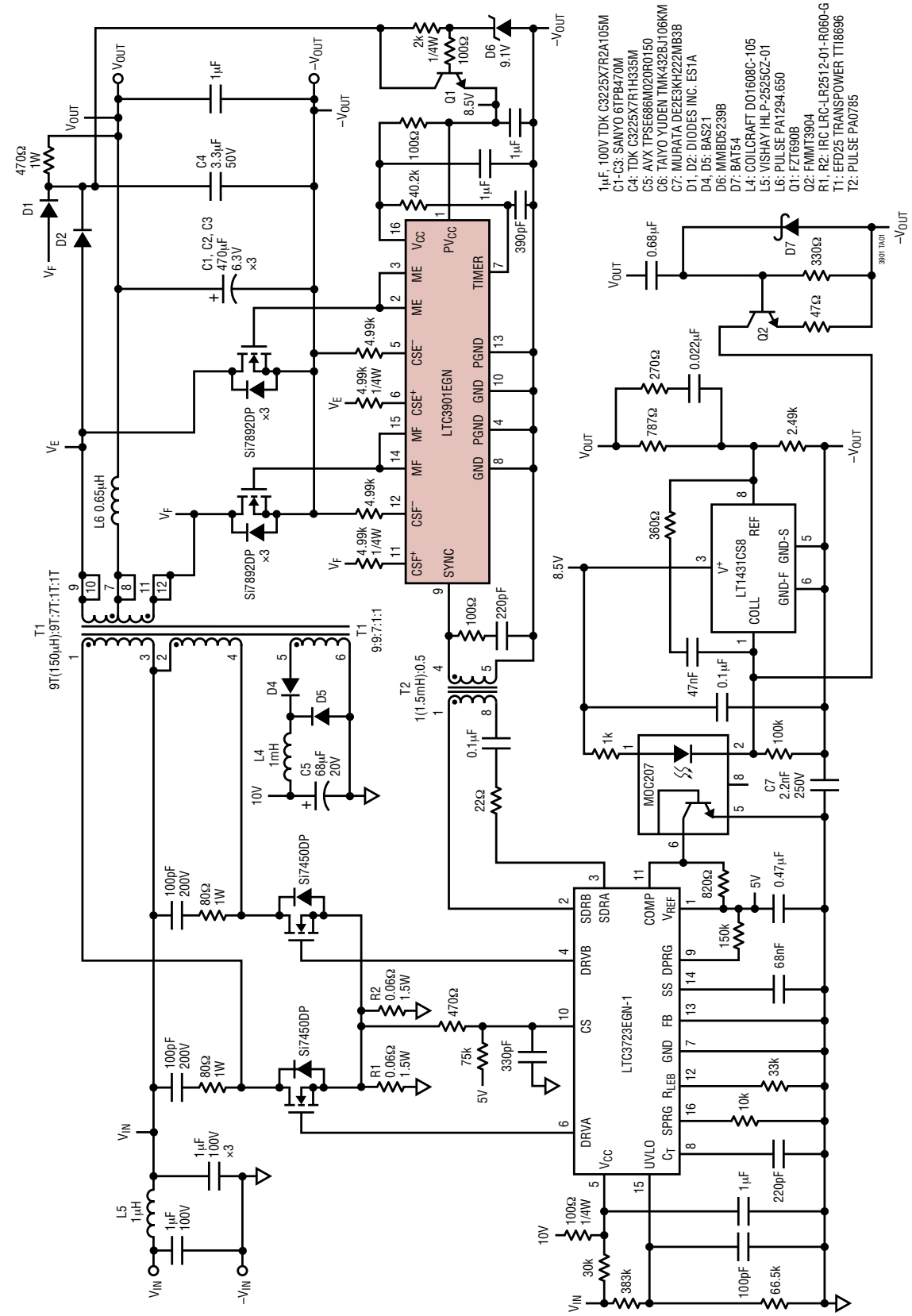
4. Place the timer capacitor, C_{TMR} as close as possible to the LTC3901.

5. Keep the PCB trace from the resistors R_{CSX1}, R_{CSX2} and R_{CSX3} to the LTC3901 CSX^+/CSX^- pins as short as possible. Connect the other ends of the resistors directly to the drain and source of the MOSFET.

6. Make the connection between GND and PGND right at the LTC3901 pins.

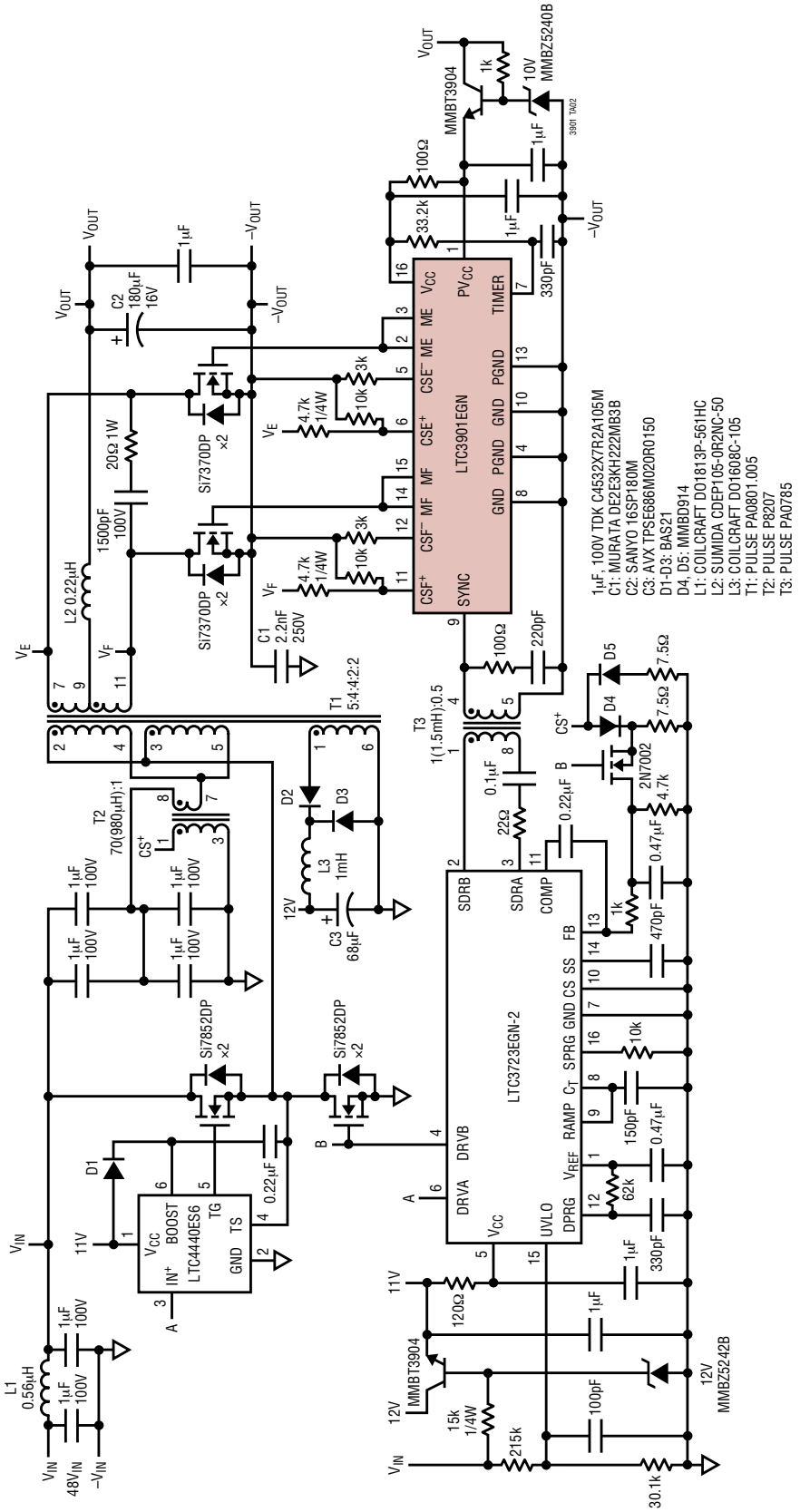
TYPICAL APPLICATIONS

165W 36V-72V Input to 3.3V at 50A Isolated Push-Pull Converter



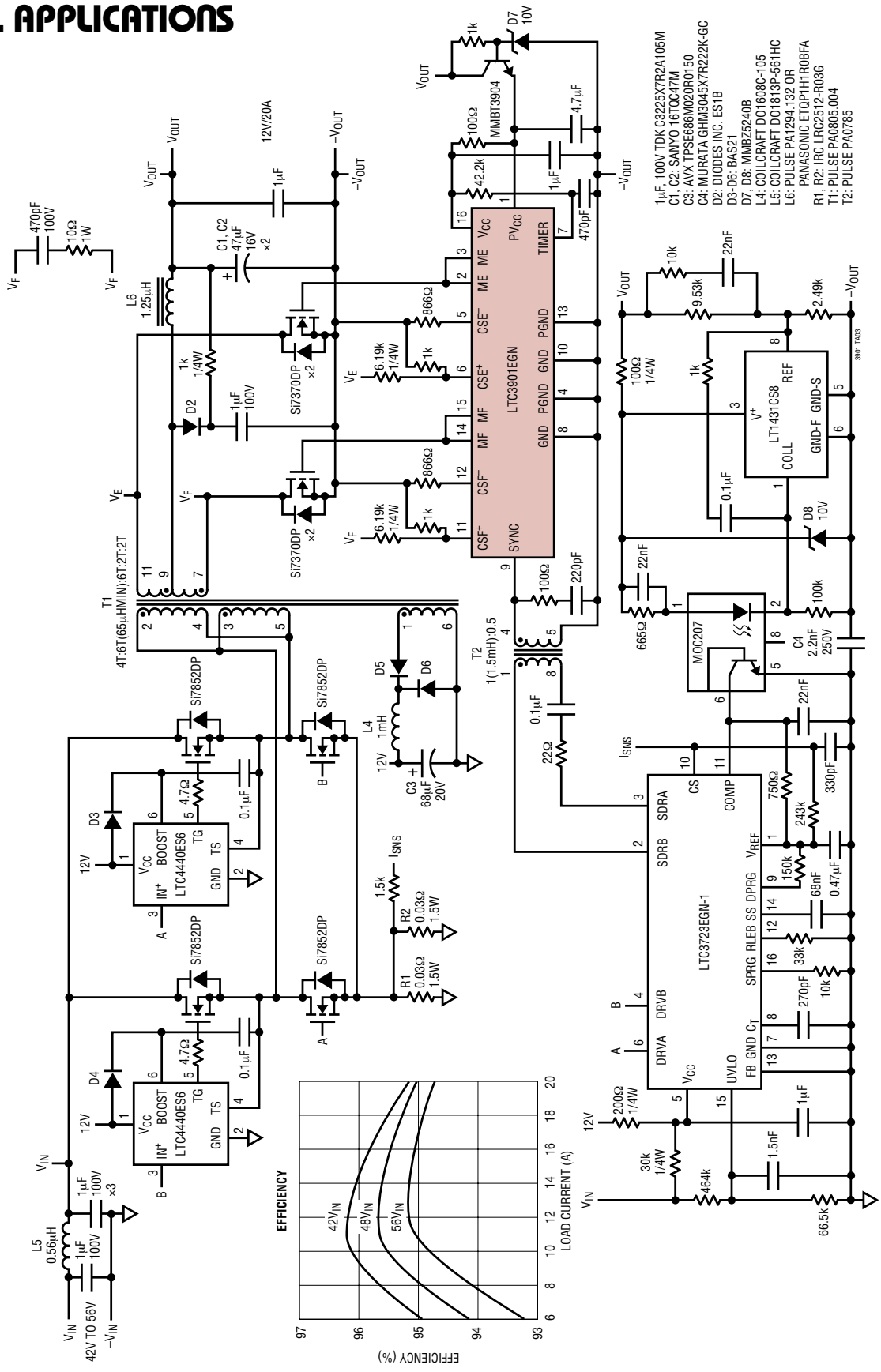
TYPICAL APPLICATIONS

240W 42V-56V Input to Unregulated 12V Half-Bridge Converter



TYPICAL APPLICATIONS

240W 42V-56V Input to 12V at 20A Isolated 1/4 Brick (2.3" × 1.45")



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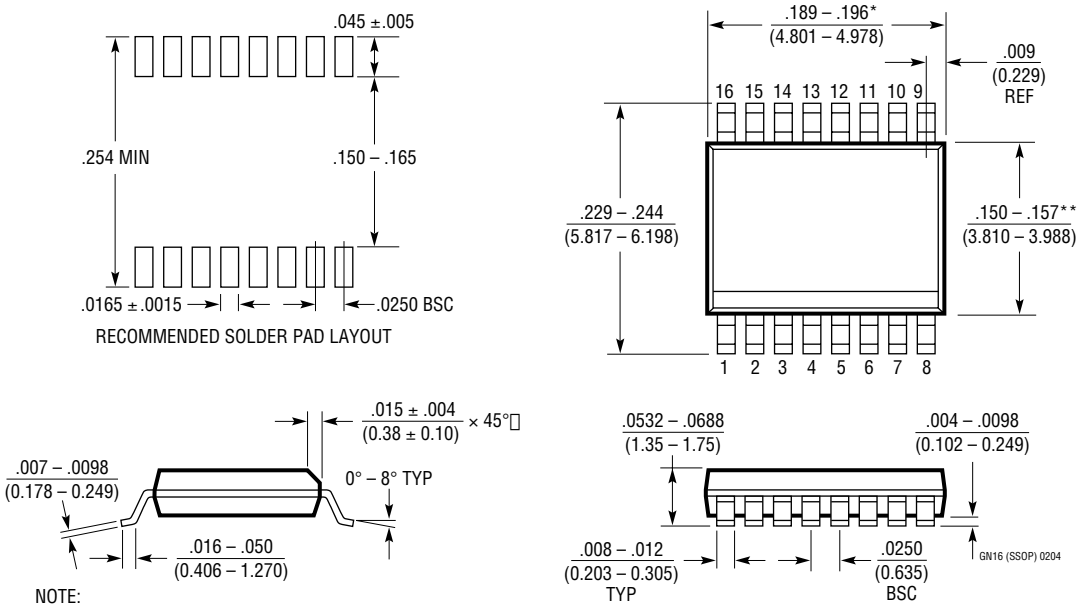
PACKAGE DESCRIPTION

GN Package
16-Lead Plastic SSOP (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1641)



NOTE:
1. CONTROLLING DIMENSION: INCHES
2. DIMENSIONS ARE IN $\frac{\text{INCHES}}{(\text{MILLIMETERS})}$
3. DRAWING NOT TO SCALE

*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1693	High Speed Single/Dual N-Channel MOSFET Drivers	CMOS Compatible Input, V_{CC} Range: 4.5V to 13.2V
LTC1698	Isolated Secondary Synchronous Rectifier Controller	Use with the LT1681, Optocoupler Driver, Pulse Transformer Synchronization
LT1952	Synchronous DC/DC Forward Controller	Programmable Volt-Second Clamp and Slope Compensation
LTC3722	Synchronous Dual Mode Phase Modulated Full-Bridge Controller	50W to 2kW Power Supply Design, Adaptive Direct Sense ZVS
LTC3723	Synchronous Push-Pull Controller	Adjustable Push-Pull Dead Time, High Efficiency
LTC3900	Synchronous Rectifier Driver for Forward Converters	Similar Function to the LTC3901 but for Forward Converter
LTC4441	6A MOSFET Driver	Adjustable Gate Drive Voltage, Programmable Blanking
LT4430	Optocoupler Driver	SOT-23, Prevents Overshoot

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