PolyPhase® Synchronous Boost Controller with Input/Output Protection

FEATURES

- **Input Supply Range: 4.5V to 65V (Up to 75V Surge)**
- **Reverse Input Protection to –40V**
- **Inrush Current Control, Overcurrent Protection and Output Disconnect for Boost Converter**
- **Input Voltage Surge Protection with Adjustable Clamp Voltage**
- **Onboard Ideal Diode Controller**
- **Low Quiescent Current: 55µA**
- **2-Phase Operation Reduces Required Input and Output Capacitance and Noise**
- **Output Voltage Up to 60V**
- **Adjustable Gate Drive Level 5V to 10V (OPTI-DRIVE) for Logic-Level or Standard Threshold FETs**
- **No External Bootstrap Diodes Required**
- 5mm × 9mm QFN-44 Package with High Voltage Pin Spacing

APPLICATIONS

- Industrial
- Automotive
- Military/Avionics
- Telecommunications

DESCRIPTION

The LTC®3897-2 is a synchronous boost DC/DC controller with surge stopper and ideal diode controller.

The boost controller drives two N-channel power MOSFET stages out-of-phase to reduce input and output capacitor requirements, allowing the use of smaller inductors than the single-phase equivalent. Synchronous rectification reduces power loss and eases thermal requirements.

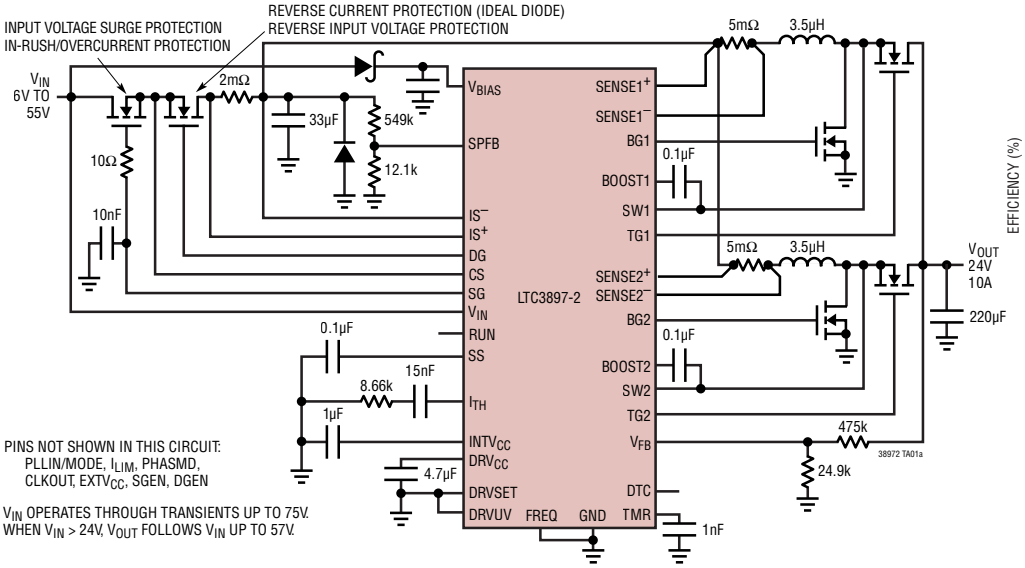
The surge stopper controls the gate of an external N-channel MOSFET to protect against high voltage input transients and provides inrush current control, overcurrent protection and output disconnect for the boost converter. The integrated ideal diode controller drives another N-channel MOSFET to replace a Schottky diode for reverse input protection and voltage holdup or peak detection. It controls the forward voltage drop across the MOSFET and minimizes reverse current flow.

The differences between the LTC3897-2 and LTC3897 are shown in Table 1.

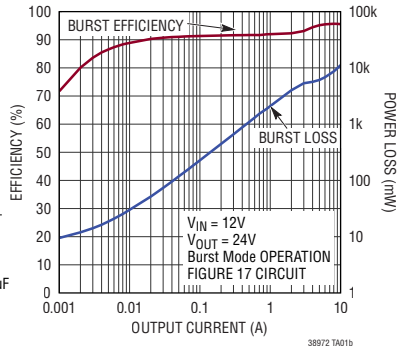
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TYPICAL APPLICATION

24V/10A 2-Phase Synchronous Boost Converter with Surge Protection and Reverse Protection



Efficiency and Power Loss vs Output Current

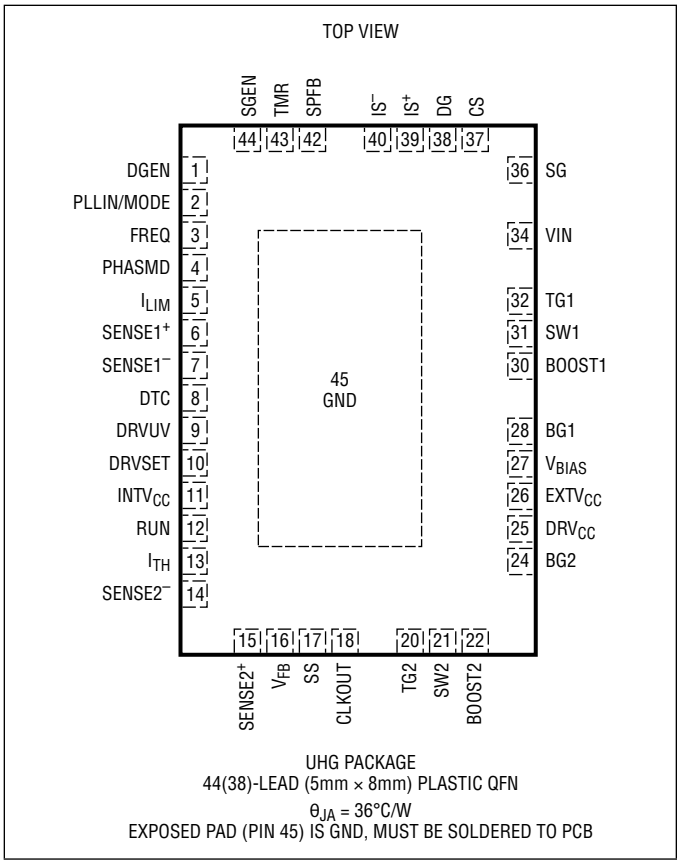


ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN}, SGEN ..... –40V to 76V
V_{BIAS}, IS^+, IS^-, ... 76V
$SENSE1^+$, $SENSE2^+$, $SENSE1^-$, $SENSE2^-$ 65V
CS ..... –40V to 76V
SG, DG (Note 8) ..... CS – 0.3V to CS + 10V
BOOST1 and BOOST2 ..... –0.3V to 71V
SW1 and SW2 ..... –5V to 65V
BG1, BG2, TG1, TG2 ..... (Note 9)
RUN, DGEN ..... –0.3V to 76V
PLLIN/MODE, TMR, V_{FB}, SPFB ..... –0.3V to 6V
$INTV_{CC}$ ..... –0.3V to 6V
$EXTV_{CC}$ ..... –0.3V to 14V
DRV_{CC}, (BOOST1-SW1), (BOOST2-SW2) ..... –0.3V to 11V
($SENSE1^+$-$SENSE1^-$),
($SENSE2^+$-$SENSE2^-$) ..... –0.3V to 0.3V
I_{LIM}, SS, I_{TH}, FREQ,
PHASMD, DTC ..... –0.3V to $INTV_{CC}$ + 0.3V
DRVUV, DRVSET ..... –0.3V to $INTV_{CC}$ + 0.3V
Operating Junction Temperature Range
(Notes 2, 3) ..... –40°C to 150°C
Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



UHG PACKAGE
44(38)-LEAD (5mm × 8mm) PLASTIC QFN
θ_{JA} = 36°C/W
EXPOSED PAD (PIN 45) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3897EUHG-2#PBF	LTC3897EUHG-2#TRPBF	38972	38-Lead (5mm × 8mm) Plastic QFN	–40°C to 125°C
LTC3897IUHG-2#PBF	LTC3897IUHG-2#TRPBF	38972	38-Lead (5mm × 8mm) Plastic QFN	–40°C to 125°C
LTC3897HUHG-2#PBF	LTC3897HUHG-2#TRPBF	38972	38-Lead (5mm × 8mm) Plastic QFN	–40°C to 150°C

Contact the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{IN} = 12V, V_{BIAS} = 12V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage and Operating Current							
V_{BIAS}	Bias Voltage Operating Range			4.5		75	V
	SENSE Pins Common Mode Range (BOOST Converter Input Supply Voltage)			2.3		65	V
V_{IN}	Input Supply Voltage Operating Range			4.2		75	V
	Reverse Input Current	V_{IN} = –30V			0	–10	µA
I_Q	Input DC Supply Current	(Note 5)					
	Pulse-Skipping or Forced Continuous Mode	RUN = 12V, V_{FB} = 1.25V (No Load)			1.32		mA
	Burst Mode (Sleep)	RUN = 12V, DGEN = SGEN = 0V, V_{FB} = 1.25V (No Load), CS = IS^+ = IS^- = V_{SPFB} = 0V			55	90	µA
		RUN = DGEN = 12V, SGEN = 0V, V_{FB} = 1.25V (No Load), CS = 12V, IS^+ = IS^- = CS – 0.1V			125	190	µA
		RUN = 12V, DGEN = 0V, SGEN = 12V, V_{FB} = 1.25V (No Load), CS = IS^+ = IS^- = 12V			260	380	µA
		RUN = DGEN = SGEN = 12V, V_{FB} = 1.25V (No Load), CS = 12V, IS^+ = IS^- = CS – 0.1V			325	450	µA
	Shutdown	RUN = DGEN = SGEN = 0V			15	22	µA
BOOST Controller Main Control Loop							
V_{OUT}	Regulated Boost Output Voltage in Synchronous Configuration					60	V
V_{FB}	Regulated Feedback Voltage	I_{TH} = 1.2 V (Note 4)	●	1.188	1.200	1.212	V
I_{FB}	Feedback Current	(Note 4)			±10	±50	nA
	Reference Line Voltage Regulation	(Note 4) V_{IN} = 6V to 75V			0.002	0.02	%/V
	Output Voltage Load Regulation	(Note 4)					
		(Note 4) Measured in Servo Loop, I_{TH} Voltage = 1V to 0.6V	●		0.01	0.1	%
		(Note 4) Measured in Servo Loop, I_{TH} Voltage = 1V to 1.4V	●		–0.01	–0.1	%
g_m	Error Amplifier Transconductance	I_{TH} = 1.2 V			2		mmho
UVLO	Undervoltage Lockout	DRV_{CC} Ramping Up					
		DRVUV = 0V	●		4.0	4.2	V
		DRVUV = $INTV_{CC}$	●		7.5	7.8	V
		DRV_{CC} Ramping Down					
		DRVUV = 0V	●	3.6	3.8	4.0	V
		DRVUV = $INTV_{CC}$	●	6.4	6.7	7.0	V
V_{RUN}	RUN Pin ON Threshold	V_{RUN} Rising	●	1.18	1.28	1.38	V
	RUN Pin Hysteresis				100		mV
I_{SS}	Soft-Start Charge Current	V_{SS} = GND		7	10	13	µA
$V_{SENSE1,2(MAX)}$	Maximum Current Sense Threshold	V_{FB} = 1.15V, I_{LIM} = $INTV_{CC}$, V_{SENSE}+ = 12V	●	125	140	155	mV
		V_{FB} = 1.15V, I_{LIM} = Float, V_{SENSE}+ = 12V	●	85	95	105	mV
		V_{FB} = 1.15V, I_{LIM} = GND, V_{SENSE}+ = 12V	●	41	48	55	mV
	Matching Between $V_{SENSE1(MAX)}$ and $V_{SENSE2(MAX)}$	V_{FB} = 1.15V, I_{LIM} = $INTV_{CC}$, V_{SENSE}+ = 12V	●	–12	0	12	mV
		V_{FB} = 1.15V, I_{LIM} = Float, V_{SENSE}+ = 12V	●	–10	0	10	mV
		V_{FB} = 1.15V, I_{LIM} = GND, V_{SENSE}+ = 12V	●	–9	0	9	mV

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{IN} = 12V, V_{BIAS} = 12V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	SENSE+ Pin Current	V_{FB} = 1.1V, I_{LIM} = Float			250	350	µA
	SENSE– Pin Current	V_{FB} = 1.1V, I_{LIM} = Float				±2	µA
	Top Gate Pull-Up Resistance	DRV_{CC} = 10V			2.5		Ω
	Top Gate Pull-Down Resistance	DRV_{CC} = 10V			1.5		Ω
	Bottom Gate Pull-Up Resistance	DRV_{CC} = 10V			2.5		Ω
	Bottom Gate Pull-Down Resistance	DRV_{CC} = 10V			1		Ω
BDSW	BOOST to DRV_{CC} Switch On-Resistance	V_{SW} = 0V, V_{DRVSET} = $INTV_{CC}$		2.6	3.7		Ω
	Top Gate Off to Bottom Gate On Switch-On Delay Time	DTC = 0V			55	75	ns
		DTC = Float			90	130	ns
		DTC = $INTV_{CC}$			170	275	ns
	Bottom Gate Off to Top Gate On Switch-On Delay Time	DTC = 0V			55	75	ns
		DTC = Float			90	130	ns
		DTC = $INTV_{CC}$			170	275	ns
	Maximum BG Duty Factor				96		%
$t_{ON(MIN)}$	Minimum BG On-Time	(Note 7) V_{DRVSET} = $INTV_{CC}$			90		ns
DRV_{CC} LDO Regulator							
	DRV_{CC} Voltage from Internal V_{BIAS} LDO	V_{EXTVCC} = 0V 7V < V_{BIAS} < 75V, DRVSET = 0V 11V < V_{BIAS} < 75V, DRVSET = $INTV_{CC}$		 5.8 9.6	 6.0 10.0	 6.2 10.4	 V V
	DRV_{CC} Load Regulation from V_{BIAS} LDO	I_{CC} = 0mA to 50mA, V_{EXTVCC} = 0V, V_{DRVSET} = $INTV_{CC}$			0.7	2	%
	DRV_{CC} Voltage from Internal $EXTV_{CC}$ LDO	7V < V_{EXTVCC} < 13V, DRVSET = 0V 11V < V_{EXTVCC} < 13V, DRVSET = $INTV_{CC}$		5.8 9.6	6.0 10.0	6.2 10.4	V V
	DRV_{CC} Load Regulation from Internal $EXTV_{CC}$ LDO	I_{CC} = 0mA to 50mA, V_{EXTVCC} = 8.5V, V_{DRVSET} = 0V			0.7	2	%
	$EXTV_{CC}$ LDO Switchover Voltage	$EXTV_{CC}$ Ramping Positive DRVUV = 0V DRVUV = $INTV_{CC}$		 4.5 7.4	 4.7 7.7	 4.9 8.0	 V V
	$EXTV_{CC}$ Hysteresis				250		mV
	Programmable DRV_{CC}	R_{DRVSET} = 50kΩ, V_{EXTVCC} = 0V			5.0		V
	Programmable DRV_{CC}	R_{DRVSET} = 70kΩ, V_{EXTVCC} = 0V		6.4	7.0	7.6	V
	Programmable DRV_{CC}	R_{DRVSET} = 90kΩ, V_{EXTVCC} = 0V			9.0		V
Oscillator and Phase-Locked Loop							
	Programmable Frequency	R_{FREQ} = 25k			105		kHz
		R_{FREQ} = 60k		335	400	465	kHz
	Lowest Fixed Frequency	V_{FREQ} = 0V		320	350	380	kHz
	Highest Fixed Frequency	V_{FREQ} = $INTV_{CC}$		488	535	585	kHz
f_{SYNC}	Synchronizable Frequency	PLLIN/MODE = External Clock	●	75		550	kHz
	PLLIN/MODE Input High Level	PLLIN/MODE = External Clock	●	2.5			V
	PLLIN/MODE Input Low Level	PLLIN/MODE = External Clock	●			0.5	V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{IN} = 12V, V_{BIAS} = 12V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
BOOST1 and BOOST2 Charge Pump							
	BOOST Charge Pump Available Output Current	FREQ = 0V, Forced Continuous or Pulse-Skipping Mode $V_{SW1,2}$ = 12V; $V_{BOOST1,2}$ = 16.5V $V_{SW1,2}$ = 12V; $V_{BOOST1,2}$ = 19.5V			 70 30		 µA µA
Surge Stopper							
	SGEN Pin ON Threshold	V_{SGEN} Rising	●	1.16	1.26	1.36	V
	SGEN Pin Hysteresis				100		mV
	SG Pin Output High Voltage (V_{SG} – V_{CS})	V_{IN} = 4.2V, I_{SG} = 0, –1µA, DG – CS = 1V	●	4.5		8	V
		V_{IN} = 8V to 70V, I_{SG} = 0, –1µA	●	10	12	16	V
	SG Pin Pull-Up Current	V_{IN} = SG = DG = CS = 12V	●	–5	–10	–15	µA
	SG Pin Pull-Down Current	Overvoltage: SPFB = 1.5V, SG – CS = 5V	●	50	130		mA
		Overcurrent: ΔV_{IS} = 100mV, SG – CS = 5V	●	50	130		mA
		Shutdown: DGEN = SGEN = 0V, SG – CS = 5V	●	0.4	1		mA
	CS Pin Input Current	V_{IN} = CS = 12V, IS^+ = IS^- = 11.9V, SGEN = Float	●		2	6	µA
		V_{IN} = CS = 12V, SGEN = 0V	●		25	100	µA
		V_{CS} = –30V	●		–2.5	–3.5	mA
V_{SPFB}	Regulated Surge Protection Feedback Voltage		●	1.205	1.235	1.265	V
ΔV_{IS}	Overcurrent Fault Threshold, (V_{IS^+} – V_{IS^-})	IS^- > 2.5V	●	45	50	55	mV
		IS^- = 1.5V	●	21	27	33	mV
	IS^+ Pin Input Current	IS^+ = IS^- = V_{IN} = CS = 12V, SGEN = DGEN = Float	●		35	100	µA
		IS^+ = IS^- = V_{IN} = CS = 12V, SGEN = DGEN = 0V	●		1	15	µA
	SPFB Pin Input Current	SPFB = 1.235V	●		±20	±500	nA
	IS^- Pin Input Current	IS^+ = IS^- = V_{IN} = CS = 12V, SGEN = DGEN = Float	●		20	100	µA
		IS^+ = IS^- = V_{IN} = CS = 12V, SGEN = DGEN = 0V	●		5	15	µA
$I_{TMR,UP}$	TMR Pin Pull-Up Current, Overvoltage	TMR = 1V, SPFB = 1.5V, V_{IN} – V_{IS^-} = 0.5V TMR = 1V, SPFB = 1.5V, V_{IN} – V_{IS^-} = 70V	● ●	–1.5 –43	–2.5 –53	–3.7 –63	µA µA
	TMR Pin Pull-Up Current, Overcurrent	TMR = 1V, ΔV_{IS} = 60mV, V_{IN} – V_{IS^-} = 0.5V TMR = 1V, ΔV_{IS} = 60mV, V_{IN} – V_{IS^-} = 70V	● ●	–6 –210	–10 –250	–16 –290	µA µA
	TMR Pin Pull-Up Current, Warning	TMR = 1.3V, SPFB = 1.5V, V_{IN} – V_{IS^-} = 0.5V	●	–3	–5	–8	µA
	TMR Pin Pull-Up Current, Retry	TMR = 1V, SPFB = 1.5V	●	–1.5	–2.5	–3.7	µA
$I_{TMR,DN}$	TMR Pin Pull-Down Current	TMR = 1V, SPFB = 1.5V, Retry SGEN = 0V	● ●	1.2 0.4	2 0.75	2.8 1.5	µA mA
	Retry Duty Cycle, Overcurrent	ΔV_{IS} = 60mV, V_{IN} – V_{IS^-} = 12V	●	0.06	0.08	0.12	%
	TMR Pin Thresholds	SG Falling, V_{IN} = 4.2V to 70V SG Rising (after 32 cycles), V_{IN} = 4.2V to 70V	● ●	1.31 0.13	1.35 0.15	1.38 0.18	V V
Ideal Diode							
	DGEN Pin ON Threshold	V_{DGEN} Rising	●	1.16	1.26	1.36	V
	DGEN Pin Hysteresis				100		mV
	DG Pin Output High Voltage, (V_{DG} – V_{CS})	V_{IN} = 4.2V, I_{DG} = 0, –1µA, No Fault, SG Open	●	4.5			V
		8V < V_{IN} < 70V, I_{DG} = 0, –1µA, No Fault, SG Open	●	10	12	16	V
	DG Pin Pull-Up Current	DG = CS = V_{IN} = 12V, CS – IS^+ = 0.1V	●	–5	–10	–15	µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{IN} = 12V, V_{BIAS} = 12V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	DG Pin Pull-Down Current	DG = CS + 5V, CS – IS^+ = –0.2V	●	60	130		mA
		DG = CS + 5V, SGEN = DGEN = 0V	●	0.4	1		mA
ΔV_{SD}	Source-Drain Regulation Voltage, (V_{CS} – V_{IS+})	DG – CS = 2.5V, V_{IN} = CS = 4.2V to 70V	●	20	30	40	mV
	DG Turn Off Propagation Delay in Fault Condition	CS – IS^+ = –1V, DG High to Low	●		0.6	2	µS

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC3897-2 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC3897E-2 is guaranteed to meet specifications from 0°C to 85°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3897I-2 is guaranteed over the –40°C to 125°C operating junction temperature range. The LTC3897H-2 is guaranteed over the –40°C to 150°C operating temperature range. High junction temperatures degrade operation lifetime. Operation lifetime is derated for junction temperatures greater than 125°C. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors. The junction temperature (T_J, in °C) is calculated from the ambient temperature (T_A, in °C) and power dissipation (P_D, in watts) according to the formula:

$T_J = T_A + (P_D \bullet \theta_{JA})$, where θ_{JA} = 36°C/W for the QFN package.

Note 3: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. The maximum rated junction temperature will be exceeded when this protection is active. Continuous operation above the specified absolute maximum operating junction temperature may impair device reliability or permanently damage the device.

Note 4: The LTC3897-2 is tested in a feedback loop that servos V_{FB} to the output of the error amplifier while maintaining I_{TH} at the midpoint of the current limit range.

Note 5: Dynamic supply current is higher due to the gate charge being delivered at the switching frequency.

Note 6: Rise and fall times are measured using 10% and 90% levels. Delay times are measured using 50% levels.

Note 7: See Minimum On-Time Considerations in the Applications Information section.

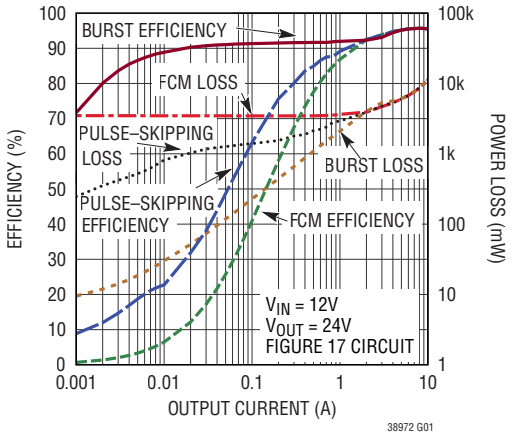
Note 8: Internal clamps limit the SG and DG pins to minimum of 10V above the CS pin. Driving these pins to voltages beyond the clamp may damage the device.

Note 9: Do not apply a voltage or current source to these pins. They must be connected to capacitive loads only, otherwise permanent damage may occur.

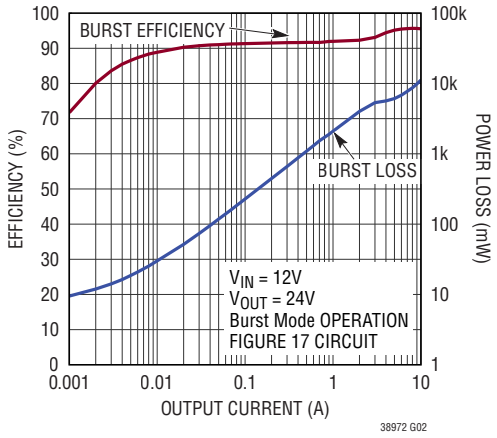
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C unless otherwise noted.

Efficiency and Power Loss vs Output Current

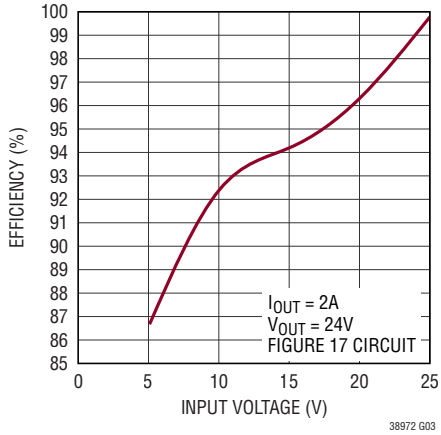


Efficiency and Power Loss vs Output Current

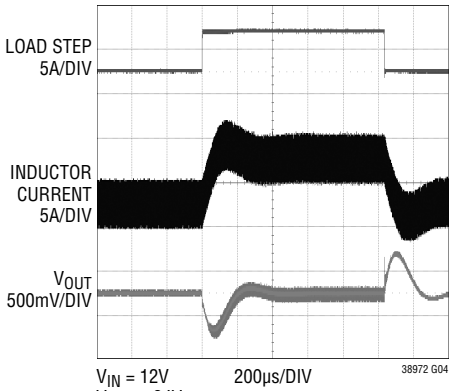


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C unless otherwise noted.

Efficiency vs Input Current

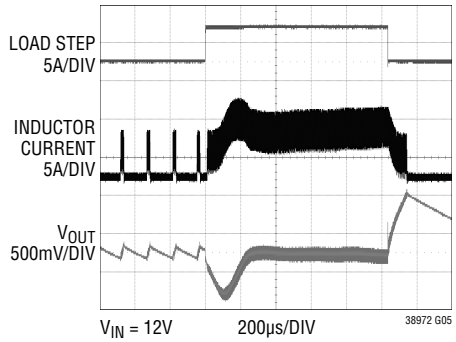


Load Step
Forced Continuous Mode



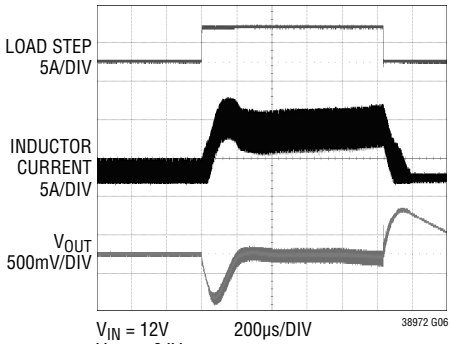
V_{IN} = 12V 200µs/DIV
V_{OUT} = 24V
LOAD STEP FROM 100mA TO 5A
FIGURE 17 CIRCUIT

Load Step
Burst Mode Operation



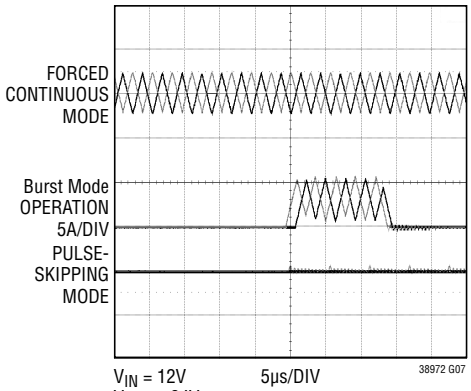
V_{IN} = 12V 200µs/DIV
V_{OUT} = 24V
LOAD STEP FROM 100mA TO 5A
FIGURE 17 CIRCUIT

Load Step
Pulse-Skipping Mode



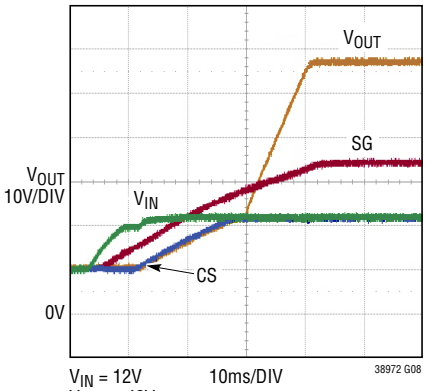
V_{IN} = 12V 200µs/DIV
V_{OUT} = 24V
LOAD STEP FROM 100mA TO 5A
FIGURE 17 CIRCUIT

Inductor Currents at Light Load



V_{IN} = 12V 5µs/DIV
V_{OUT} = 24V
I_{LOAD} = 200µA
FIGURE 17 CIRCUIT

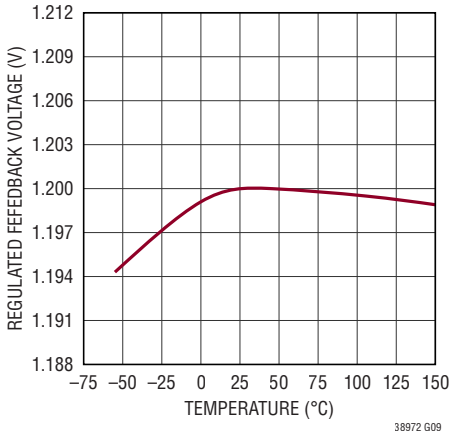
Start-Up



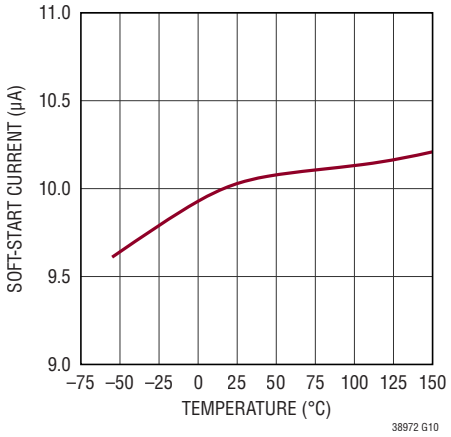
V_{IN} = 12V 10ms/DIV
V_{OUT} = 48V
FIGURE 16 CIRCUIT

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C unless otherwise noted.

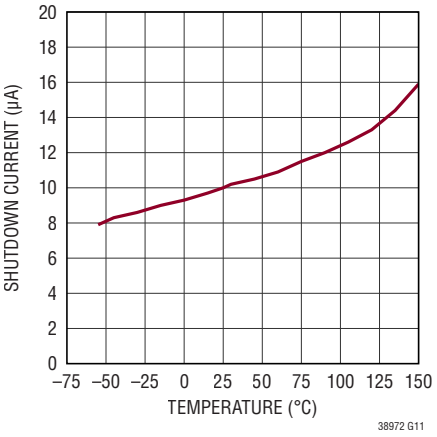
Regulated Feedback Voltage vs Temperature



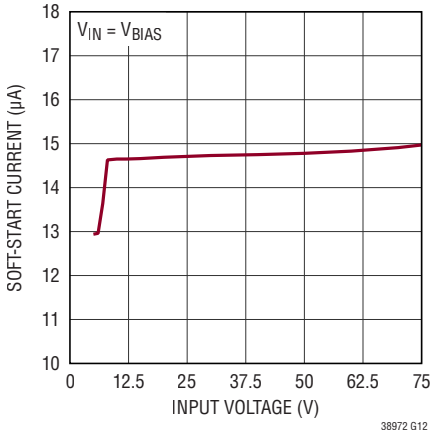
Soft-Start Pull-Up Current vs Temperature



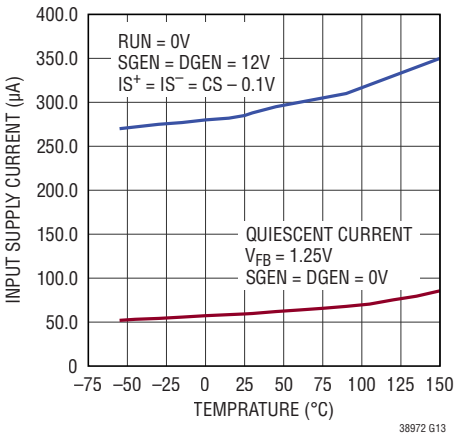
Shutdown Current vs Temperature



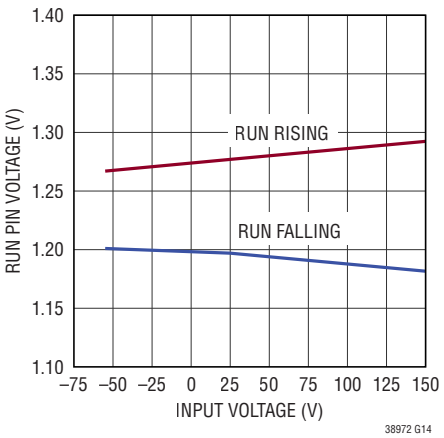
Shutdown Current vs Input Voltage



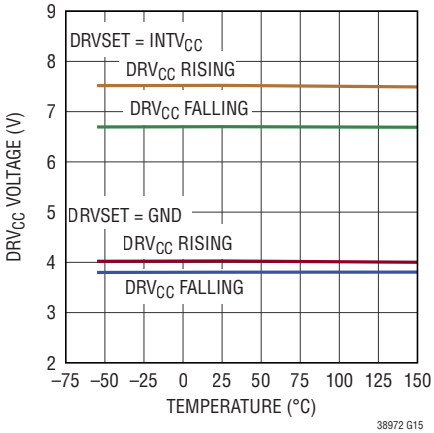
Input Supply Current vs Temperature



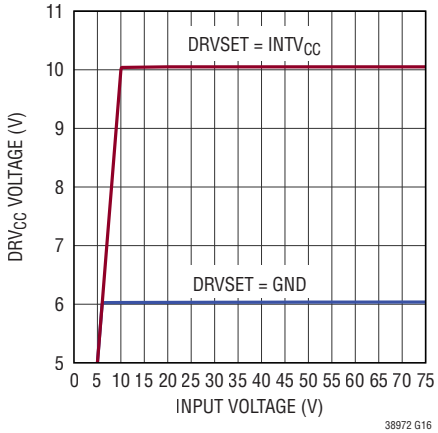
BOOST Shutdown (RUN) Threshold vs Temperature



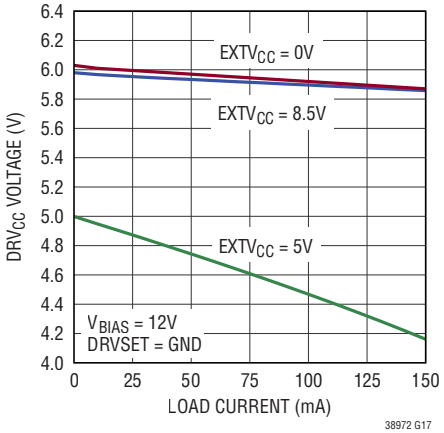
Undervoltage Lockout Threshold vs Temperature



DRV_{CC} Line Regulation



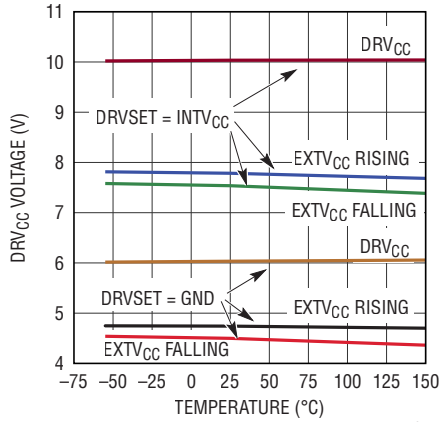
DRV_{CC} and $EXTV_{CC}$ vs Load Current



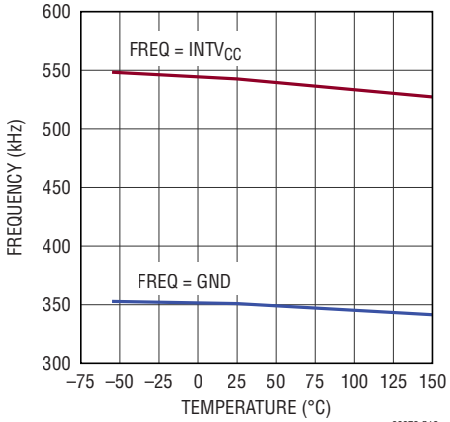
Rev. A

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C unless otherwise noted.

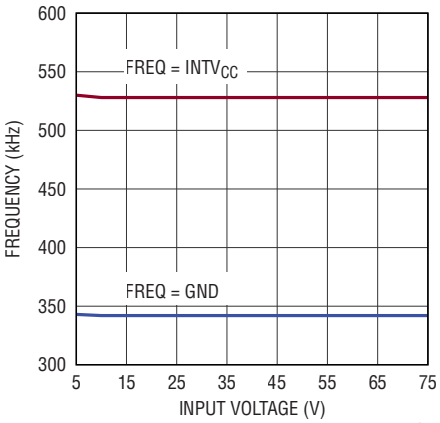
$EXTV_{CC}$ Switchover and DRV_{CC} Voltages vs Temperature



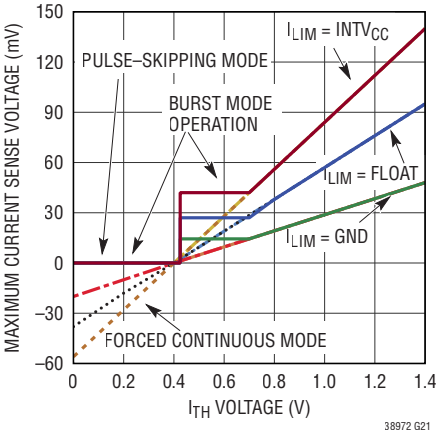
Oscillator Frequency vs Temperature



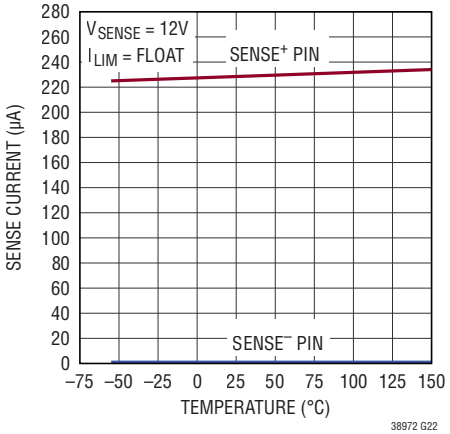
Oscillator Frequency vs Input Voltage



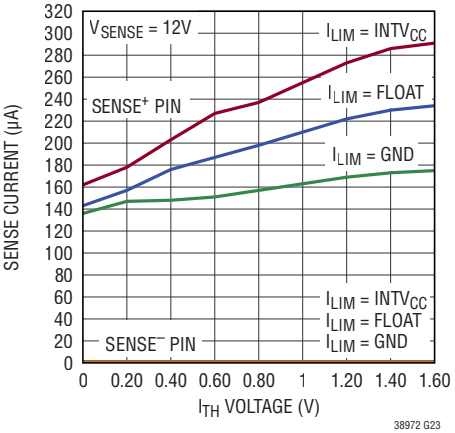
Maximum Current Sense Threshold vs I_{TH} Voltage



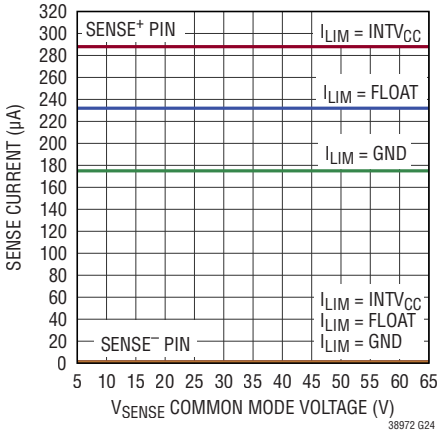
SENSE Pin Input Current vs Temperature



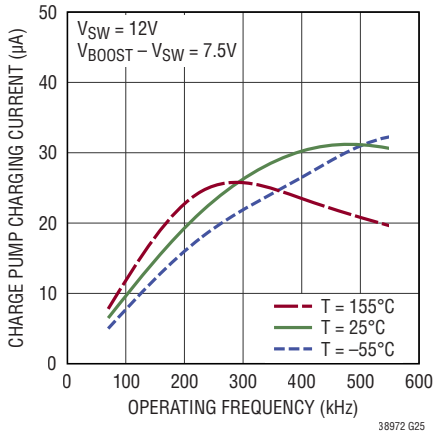
SENSE Pin Input Current vs I_{TH} Voltage



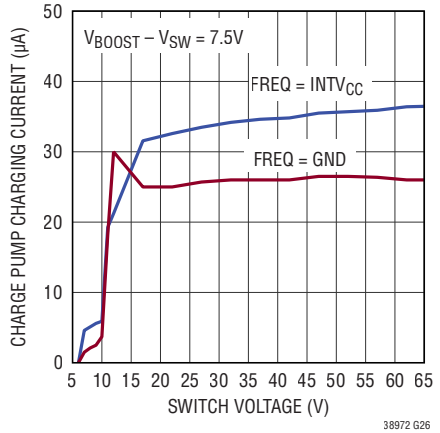
SENSE Pin Input Current vs V_{SENSE} Voltage



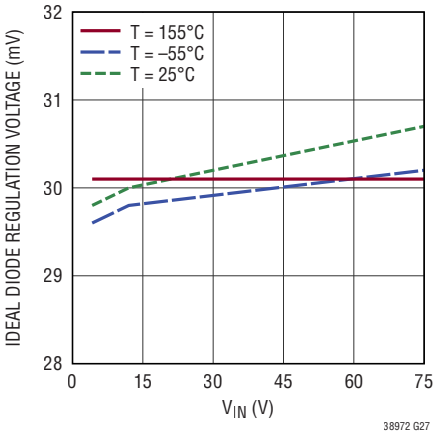
BOOST-SW Charge Pump Charging Current vs Operating Frequency



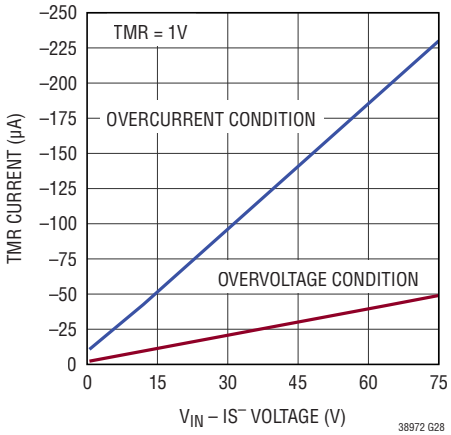
BOOST-SW Charge Pump Charging Current vs Switch Voltage



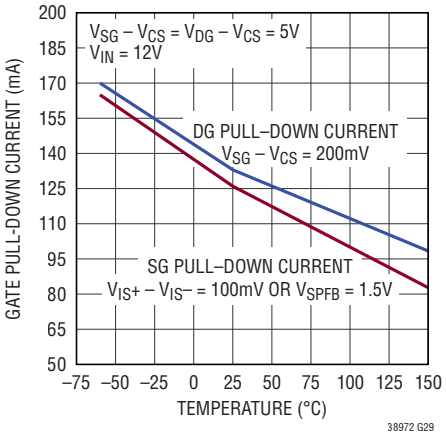
Ideal Diode Regulation Voltage vs V_{IN}



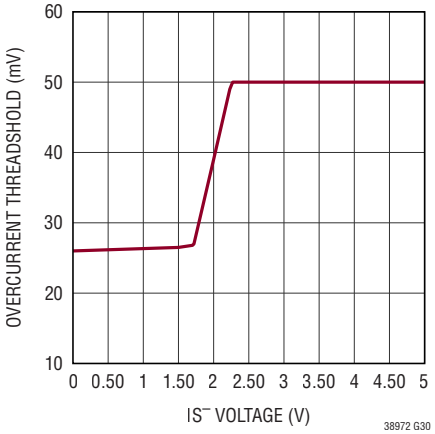
TMR Current vs V_{IN} – IS^- Voltage



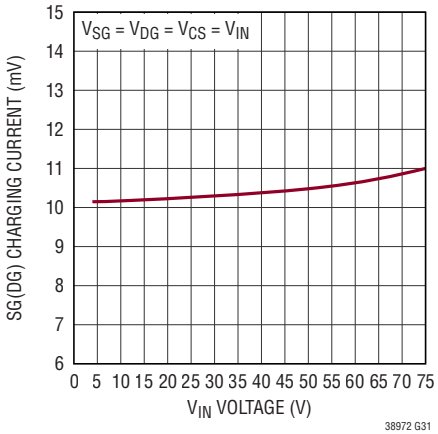
TMR Current vs Temperature



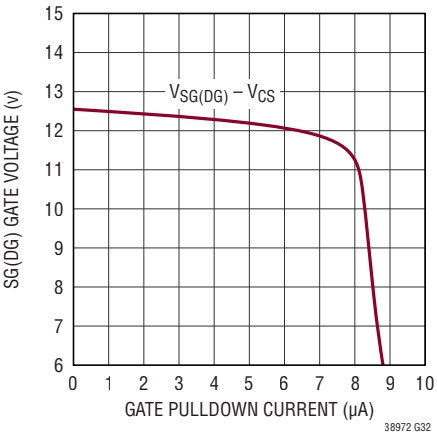
Overcurrent Threshold vs IS^- Voltage



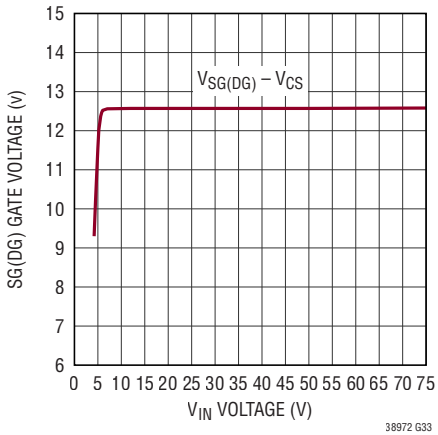
SG(DG) Charging Current vs V_{IN} Voltage



SG(DG) GATE Voltage vs GATE Pull-Down Current



SG(DG) GATE Voltage vs V_{IN} Voltage



PIN FUNCTIONS

DGEN (Pin 1): Ideal Diode Enable Pin. This pin enables regulation for the ideal diode's forward drop. Tying this pin to SGND disables the regulation but still keeps the reverse input voltage protection.

PLLIN/MODE (Pin 2): External Synchronization Input to Phase Detector and Forced Continuous Mode Input. When an external clock is applied to this pin, it will force the controller into pulse-skipping mode of operation and the phase-locked loop will force the rising BG1 signal to be synchronized with the rising edge of the external clock. When not synchronizing to an external clock, this input determines how the LTC3897-2 operates at light loads. Pulling this pin to ground selects Burst Mode operation. An internal 100k resistor to ground also invokes Burst Mode® operation when the pin is floated. Tying this pin to $INTV_{CC}$ forces continuous inductor current operation. Tying this pin to a voltage greater than 1.2V and less than $INTV_{CC}$ – 1.3V selects pulse-skipping operation. This can be done by adding a 100k resistor between the PLLIN/MODE pin and $INTV_{CC}$.

FREQ (Pin 3): The frequency control pin for the internal VCO. Connecting the pin to GND forces the VCO to a fixed low frequency of 350kHz. Connecting the pin to $INTV_{CC}$ forces the VCO to a fixed high frequency of 535kHz. The frequency can be programmed by connecting a resistor from the FREQ pin to GND. The resistor and an internal 20µA source current create a voltage used by the internal oscillator to set the frequency. Alternatively, this pin can be driven with a DC voltage to vary the frequency of the internal oscillator.

PHASMD (Pin 4): This pin can be floated, tied to GND, or tied to $INTV_{CC}$ to program the phase relationship between the rising edges of BG1 and BG2, as well as the phase relationship between BG1 and CLKOUT.

I_{LIM} (Pin 5): Current Comparator Sense Voltage Range Input. This pin is used to set the peak current sense voltage in the current comparator. Connect this pin to GND, open, and $INTV_{CC}$ to set the peak current sense voltage to 48mV, 95mV and 140mV, respectively.

$SENSE1^+$, $SENSE2^+$ (Pins 6, 15): Positive Current Sense Comparator Input for each channel of the boost controller. The (+) input to the Current Comparator is normally connected to the positive terminal of a current sense resistor. This pin also supplies power to the current comparator.

$SENSE1^–$, $SENSE2^–$ (Pins 7, 14): Negative Current Sense Comparator Input for each channel of the boost controller. The (–) input to the Current Comparator is normally connected to the negative terminal of a current sense resistor connected in series with the inductor.

DTC (Pin 8): Dead Time Control. This pin selects different dead times between TG and BG. Floating this pin sets the dead time to 100nS. Tying this pin to GND or $INTV_{CC}$ sets the dead time to 60nS or 200nS, respectively.

DRVUV (Pin 9): Sets the higher or lower DRV_{CC} UVLO and $EXTV_{CC}$ switchover thresholds, as listed on the Electrical Characteristics table. Tying this pin to GND sets the lower thresholds whereas tying this pin to $INTV_{CC}$ sets the higher thresholds. See the Electrical Characteristics table for the rising/falling threshold values and tolerances.

DRVSET (Pin 10): Sets the regulated output voltage of the DRV_{CC} LDO regulator. Tying this pin to GND sets DRV_{CC} to 6.0V. Tying this pin to $INTV_{CC}$ sets DRV_{CC} to 10.0V. Other voltages between 5.0V and 10.0V can be programmed by using a resistor (50k to 100k) between the DRVSET pin and GND. When programming DRVSET with a resistor, do not choose a resistor value less than 50k (unless shorting DRVSET to GND) or higher than 100k.

$INTV_{CC}$ (Pin 11): Output of the Internal 3.5V Low Dropout Regulator. Supply pin for the low voltage analog and digital circuits. A low ESR 0.1µF ceramic bypass capacitor should be connected between $INTV_{CC}$ and GND, as close as possible to the IC. $INTV_{CC}$ should not be used to power or bias any external circuitry other than to configure the FREQ, PHASMD, I_{LIM}, DTC, DRVUV, DRVSET and PLLIN/MODE pins.

PIN FUNCTIONS

RUN (Pin 12): Run Control Input for the boost controller. Forcing this pin below 1.28V shuts down the controller. Forcing this pin as well as the SGEN and DGEN pins below 0.7V shuts down the entire LTC3897-2, reducing quiescent current to approximately 15µA. An external resistor divider connected to V_{BIAS} can set the threshold for converter operation.

I_{TH} (Pin 13): Error Amplifier Outputs and Switching Regulator Compensation Point. The current comparator trip point increases with this control voltage.

V_{FB} (Pin 16): This pin receives the remotely sensed feedback voltage from the external resistive divider across the boost controller output.

SS (Pin 17): Output Soft-Start Input. A capacitor to ground at this pin sets the ramp rate of the output voltage during startup.

CLKOUT (Pin 18): A digital output used for daisy-chaining multiple LTC3897-2 ICs in multi-phase systems. The PHASMD pin voltage controls the relationship between BG1 and CLKOUT. This pin swings between GND and $INTV_{CC}$.

TG2, TG1 (Pins 20, 32): Top Gate. Connect to the gate of the synchronous N-channel MOSFET.

SW2, SW1 (Pins 21, 31): Switch Node. Connect to the source of the synchronous N-channel MOSFET (TG), the drain of the main N-channel MOSFET (BG), and the inductor.

BOOST2, BOOST1 (Pins 22, 30): Floating power supply for the synchronous N-channel MOSFET. Bypass to SW pin with a capacitor.

BG2, BG1 (Pins 24, 28): Bottom Gate. Connect to the gate of the main N-channel MOSFET.

DRV_{CC} (Pin 25): Output of the Internal Low Dropout (LDO) Regulator that powers the boost controller gate drivers. The regulated DRV_{CC} voltage is set by the DRVSET pin. Must be decoupled to ground with a minimum of 4.7µF ceramic or other low ESR capacitor. Do not use the DRV_{CC} pin for any other purpose.

$EXTV_{CC}$ (Pin 26): External Power Input to an Internal LDO Connected to DRV_{CC}. This LDO supplies DRV_{CC} power from $EXTV_{CC}$, bypassing the internal LDO powered from V_{BIAS} whenever $EXTV_{CC}$ is higher than its switchover threshold (4.7V or 7.7V depending on the state of the DRVUV pin). See $EXTV_{CC}$ Connection in the Applications Information section. Do not float or exceed 14V on this pin. Do not connect $EXTV_{CC}$ to a voltage greater than V_{BIAS}. Connect to GND if not used.

V_{BIAS} (Pin 27): Bias Supply Pin. This pin powers most of the chip. When the ideal diode is used at the input to block negative input voltage, connect a Schottky diode from the V_{IN} pin to the V_{BIAS} pin. A bypass capacitor should be tied between this pin and the signal ground pin.

V_{IN} (Pin 34): Input Supply Pin. A bypass capacitor should be tied between this pin and the GND pins. The supply input ranges from 4.2V to 75V for normal operation. It can also be pulled below ground potential by up to 40V during a reverse battery condition, without damaging the part.

SG (Pin 36): N-Channel MOSFET Gate Drive Output for Surge Stopper Controller. The SG pin is pulled up by an internal charge pump current source and clamped to 12V above the CS pin. An external capacitor connected to this pin can provide slew rate and inrush current control. A voltage and current amplifier controls the SG pin to regulate the SPFB pin voltage. When the overcurrent comparator monitoring the IS^+ and IS^- pins is tripped, the SG pin is pulled low, forming an electronic current breaker.

CS (Pin 37): Common Source Input and Gate Drive Return. Connect this pin directly to the sources of the external back-to-back N-Channel MOSFETs and the resistance should be limited to below 10Ω. CS is the anode of the ideal diode and the voltage sensed between this pin and the IS^+ pin is used to control the source-drain voltage across the N-Channel MOSFET (forward voltage of the ideal diode).

PIN FUNCTIONS

DG (Pin 38): N-Channel Gate Drive Output for Ideal Diode Controller. When the load current creates more than 30mV of voltage drop across the MOSFET, the DG pin is pulled high by an internal charge pump current source and clamped to 12V above the CS pin. When the load current is small, the DG pin is actively driven to maintain 30mV across the MOSFET. If reverse current develops, a 100mA fast pull-down circuit quickly connects the DG pin to the CS pin, turning off the MOSFET.

IS^+ (Pin 39): Positive Overcurrent Sense Input. Connect this pin to the input of the overcurrent sense resistor. The current limit circuit pulls the SG pin low if the sense voltage between the IS^+ and IS^- pins exceed 50mV if IS^- is above 2.5V. When IS^- drops below 1.5V, the sense voltage is reduced to 27mV for additional protection during output overcurrent condition. The voltage difference with the IS^- pin must be limited to less than 30V. Connect to the IS^- pin if unused.

IS^- (Pin 40): Negative Overcurrent Sense Input. Connect this pin to the output of the overcurrent sense resistor.

SPFB (Pin 42): Surge Protection Voltage Regulator Feedback Input. Connect this pin to the center tap of the resistive divider connected between the voltage being protected and ground. During an overvoltage condition, the SG pin is servoed to maintain a 1.235V threshold at the SPFB pin. Connect to GND to disable the overvoltage clamp.

TMR (Pin 43): Fault Timer Input for the Surge Stopper. Connect a capacitor between this pin and ground to set the times for fault and cool down periods. When either overvoltage or overcurrent is detected, a current source charges up the TMR pin. The current charging up this pin during the fault conditions depends on the voltage difference between V_{IN} and IS^- pins. When V_{TMR} reaches 1.35V, the pass transistor turns off. As soon as the fault condition disappears, a cool down interval commences while the TMR pin cycles 32 times between 0.15V and 1.35V with 2.5µA charge and 2µA discharge currents. At the end of the cool down period, the SG pin is allowed to pull high turning the pass transistor back on.

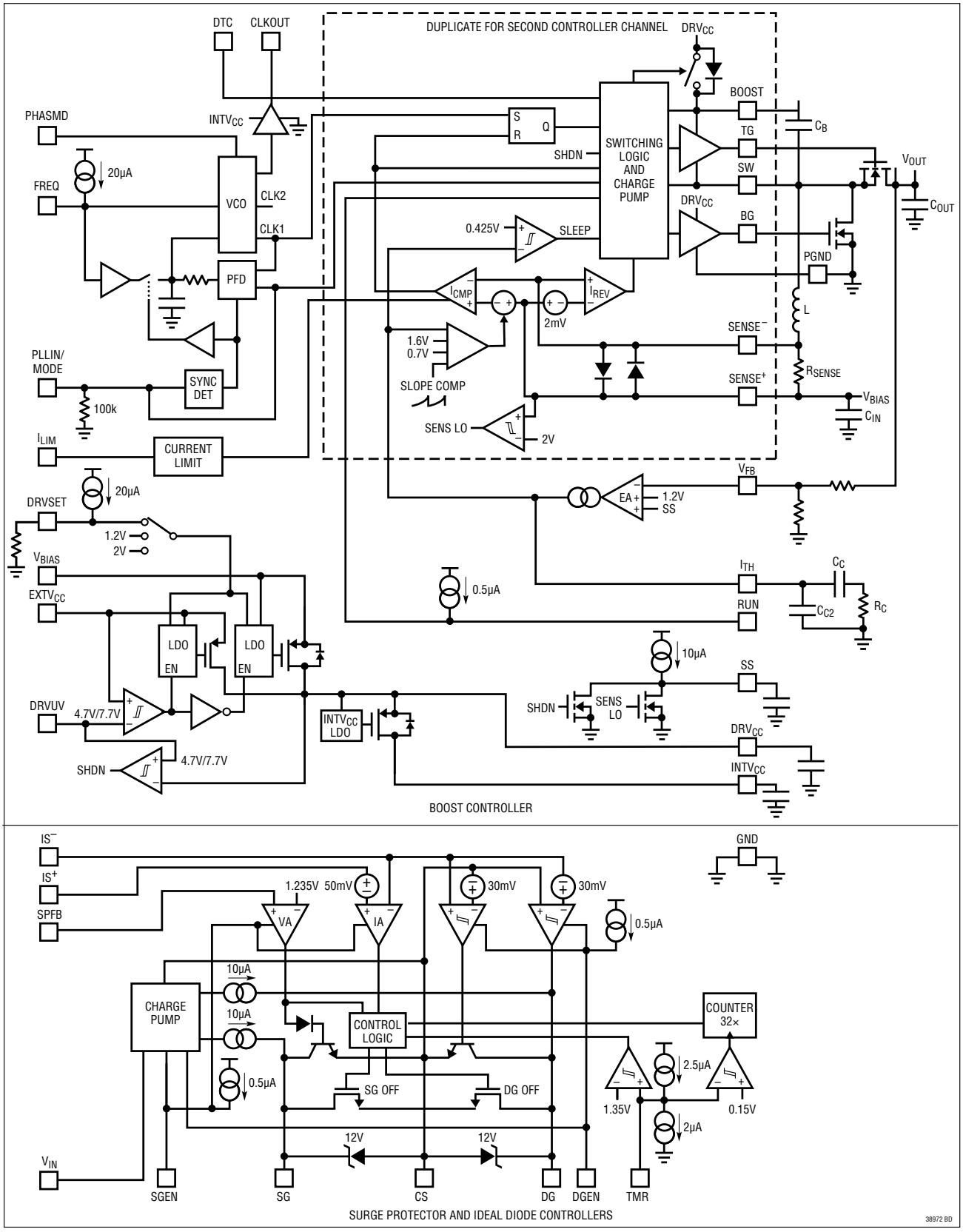
SGEN (Pin 44): Surge Gate Enable Pin. This pin enables the surge stopper controller (voltage clamp and output protection). When SGEN is low, SG is pulled to CS.

GND (Exposed Pad Pin 45): Ground. The exposed pad must be soldered to the PCB for rated electrical and thermal performance.

Table 1. Summary of the Main Differences Between the LTC3897 and the LTC3897-2

	LTC3897-2	LTC3897
Light Load Mode when Synchronized to an External Clock	Pulse Skipping Mode (Discontinuous)	Forced Continuous Mode
Output Overvoltage Protection when V_{FB} > 110% of Regulation	No TG Crowbar	TG Crowbar (TG Forced On)
Programmable Frequency	50kHz to 550kHz	50kHz to 900kHz
Package	5×8 QFN-44(38)	5×7 QFN-38 TSSOP-38

BLOCK DIAGRAM



OPERATION

Overview

The LTC3897-2 includes a polyphase step-up (boost) controller as well as surge stopper and ideal diode controllers to enable input/output protections for the boost controller. All three controllers can be individually enabled or disabled for building different boost converter applications that have a variety of combinations of the protection circuits.

The surge stopper controls the gate of an external N-channel MOSFET to protect against high voltage input transients and provide in-rush current control and output disconnect for the boost converter. The current limited circuit breaker protects against short-circuited boost outputs and other overcurrent events.

The integrated ideal diode controller drives another N-channel MOSFET to replace a Schottky diode for reverse (negative) input protection and voltage holdup or peak detection. It controls the forward voltage drop across the MOSFET and minimizes reverse current transients during power source failure, brownout or input short.

BOOST Controller Main Control Loop

The LTC3897-2's boost controller uses a constant-frequency, current mode step-up architecture with the two controller channels operating out of phase. During normal operation, each external bottom MOSFET is turned on when the clock for that channel sets the RS latch, and is turned off when the main current comparator, ICMP, resets the RS latch. The peak inductor current at which ICMP trips and resets the latch is controlled by the voltage on the I_{TH} pin, which is the output of the error amplifier EA. The error amplifier compares the output voltage feedback signal at the V_{FB} pin (which is generated with an external resistor divider connected across the output voltage, V_{OUT}, to ground), to the internal 1.200V reference voltage. In a boost converter, the required inductor current is determined by the load current, V_{IN} and V_{OUT}. When the load current increases, it causes a slight decrease in V_{FB} relative to the reference, which causes the EA to increase the I_{TH} voltage until the average inductor current in each channel matches the new requirement based on the new load current.

After the bottom MOSFET is turned off each cycle, the top MOSFET is turned on until either the inductor current starts to reverse, as indicated by the current comparator, IR, or the beginning of the next clock cycle.

$DRV_{CC}/EXTV_{CC}/INTV_{CC}$ Power

Power for the top and bottom MOSFET drivers is derived from the DRV_{CC} pin. The DRV_{CC} supply voltage can be programmed from 5V to 10V through control of the DRVSET pin. When the $EXTV_{CC}$ pin is tied to a voltage below its switchover voltage (4.7V or 7.7V depending on the DRVSET voltage), the V_{BIAS} LDO (low dropout linear regulator) supplies the DRV_{CC} voltage set by DRVSET from V_{BIAS} to DRV_{CC}. If $EXTV_{CC}$ is taken above the switchover voltage, the V_{BIAS} LDO is turned off and an $EXTV_{CC}$ LDO is turned on. Once enabled, the $EXTV_{CC}$ LDO supplies the voltage from $EXTV_{CC}$ to DRV_{CC}. Using the $EXTV_{CC}$ pin allows the DRV_{CC} power to be derived from a high efficiency external source, thus removing the power dissipation of the V_{BIAS} LDO.

Each top MOSFET driver is biased from the floating bootstrap capacitor, C_B, which normally recharges during each cycle through an internal switch whenever SW goes low.

The $INTV_{CC}$ supply powers most of the other internal circuits in the LTC3897-2's boost controller. The $INTV_{CC}$ LDO regulates to a fixed value of 3.5V and its power is derived from the DRV_{CC} supply.

Shutdown and Start-Up (RUN, SGEN, DGEN and SS Pins)

The LTC3897-2's boost controller, surge stopper, and ideal diode can be shut down independently using the enable pins, i.e. the RUN pin, the SGEN pin and the DGEN pin. Pulling the RUN pin below 1.28V shuts down the main control loops for both phases of the boost controller. Pulling the RUN pin below 0.7V disables both phases and most internal circuits. If SGEN and DGEN are both low, pulling the RUN pin below 0.7V also disables the DRV_{CC} and $INTV_{CC}$ LDOs. In this state, the LTC3897-2 draws only 15µA of quiescent current.

OPERATION

NOTE: When the input/output protections are not used, do not apply a heavy load for an extended time while the chip is in shutdown. The top MOSFETs will be turned off during shutdown and the output load may cause excessive dissipation in the body diodes.

Releasing any of the enable pins (RUN, SGEN or DGEN) allows a small internal current to pull up the pin to enable the corresponding circuits. The enable pins may be externally pulled up or driven directly by logic. Each of the enable pins can tolerate up to 75V (absolute maximum), so it can be conveniently tied to the supplies in always-on applications where the controllers or the protections are enabled continuously and never shutdown. Note that the SGEN pin can also tolerate negative voltage up to –40V, so it can be tied to the V_{IN} supply directly.

When the input/output protections are enabled, the boost controller is not enabled until IS^- pin is above (V_{IN} – 0.7V). This is to ensure that the external MOSFETs for the input/output protections are fully turned on before the BOOST controller can start operating.

The start-up of the boost controller's output voltage V_{OUT} is controlled by the voltage on the SS pin. When the voltage on the SS pin is less than the 1.2V internal reference, the LTC3897-2 regulates the V_{FB} voltage to the SS pin voltage instead of the 1.2V reference. This allows the SS pin to be used to program a soft-start by connecting an external capacitor from the SS pin to GND. An internal 10µA pull-up current charges this capacitor creating a voltage ramp on the SS pin. As the SS voltage rises linearly from 0V to 1.2V (and beyond up to $INTV_{CC}$), the output voltage rises smoothly to its final value.

Light Load Current Operation—Burst Mode Operation, Pulse-Skipping or Continuous Conduction (PLLIN/MODE Pin)

The LTC3897-2's boost controller can be enabled to enter high efficiency Burst Mode operation, constant-frequency, pulse-skipping mode or forced continuous conduction mode at low load currents. To select Burst Mode operation, tie the PLLIN/MODE pin to ground (e.g., GND). To select forced continuous operation, tie the PLLIN/MODE pin to $INTV_{CC}$. To select pulse-skipping mode, tie the PLLIN/MODE pin to a DC voltage greater than 1.2V and less than $INTV_{CC}$ – 1.3V.

When the controller is enabled for Burst Mode operation, the minimum peak current in the inductor is set to approximately 30% of the maximum sense voltage even though the voltage on the I_{TH} pin indicates a lower value. If the average inductor current is higher than the required current, the error amplifier EA will decrease the voltage on the I_{TH} pin. When the I_{TH} voltage drops below 0.425V, the internal sleep signal goes high (enabling sleep mode) and both external MOSFETs are turned off.

In sleep mode, much of the internal circuitry is turned off and the LTC3897-2 boost controller draws only 55µA of quiescent current when the input/output protections are not used. In sleep mode the load current is supplied by the output capacitor. As the output voltage decreases, the EA's output begins to rise. When the output voltage drops enough, the sleep signal goes low and the controller resumes normal operation by turning on the bottom external MOSFET on the next cycle of the internal oscillator.

When the controller is enabled for Burst Mode operation, the inductor current is not allowed to reverse. The reverse current comparator (IR) turns off the top external MOSFET just before the inductor current reaches zero, preventing it from reversing and going negative. Thus, the controller operates in discontinuous current operation. In forced continuous operation, the inductor current is allowed to reverse at light loads or under large transient conditions. The peak inductor current is determined by the voltage on the I_{TH} pin, just as in normal operation. In this mode, the efficiency at light loads is lower than in Burst Mode operation. However, continuous operation has the advantages of lower output voltage ripple and less interference to audio circuitry, as it maintains constant-frequency operation independent of load current.

When the PLLIN/MODE pin is connected for pulse-skipping mode, or when it is driven by an external clock source to use the phase-locked loop, the LTC3897-2 operates in

OPERATION

PWM pulse-skipping mode at light loads. In this mode, constant-frequency operation is maintained down to approximately 1% of designed maximum output current. At very light loads, the current comparator ICMP may remain tripped for several cycles and force the external bottom MOSFET to stay off for the same number of cycles (i.e., skipping pulses). The inductor current is not allowed to reverse (discontinuous operation). This mode, like forced continuous operation, exhibits low output ripple as well as low audio noise and reduced RF interference as compared to Burst Mode operation. It provides higher low current efficiency than forced continuous mode, but not nearly as high as Burst Mode operation.

Frequency Selection and Phase-Locked Loop (FREQ and PLLIN/MODE Pins)

The selection of switching frequency is a trade-off between efficiency and component size. Low frequency operation increases efficiency by reducing MOSFET switching losses, but requires larger inductance and/or capacitance to maintain low output ripple voltage.

The switching frequency of the LTC3897-2's controllers can be selected using the FREQ pin.

If the PLLIN/MODE pin is not being driven by an external clock source, the FREQ pin can be tied to GND, tied to $INTV_{CC}$, or programmed through an external resistor. Tying FREQ to GND selects 350kHz while tying FREQ to $INTV_{CC}$ selects 535kHz. Placing a resistor between FREQ and GND allows the frequency to be programmed between 50kHz and 550kHz, as shown in Figure 7.

A phase-locked loop (PLL) is available on the LTC3897-2 to synchronize the internal oscillator to an external clock source that is connected to the PLLIN/MODE pin. The LTC3897-2's phase detector adjusts the voltage (through an internal lowpass filter) of the VCO input to align the turn-on of the first controller's external bottom MOSFET to the rising edge of the synchronizing signal. Thus, the turn-on of the second controller's external bottom MOSFET is 180 or 240 degrees out-of-phase to the rising edge of the external clock source.

The VCO input voltage is prebiased to the operating frequency set by the FREQ pin before the external clock is applied. If prebiased near the external clock frequency, the PLL loop only needs to make slight changes to the VCO input in order to synchronize the rising edge of the external clock's to the rising edge of BG1. The ability to prebias the loop filter allows the PLL to lock-in rapidly without deviating far from the desired frequency.

The typical capture range of the LTC3897-2's PLL is from approximately 55kHz to 600kHz, and is guaranteed to lock to an external clock source whose frequency is between 75kHz and 550kHz.

The typical input clock thresholds on the PLLIN/MODE pin are 1.6V (rising) and 1.2V (falling). The recommended maximum amplitude for low level and minimum amplitude for high level of external clock are 0V and 2.5V, respectively.

PolyPhase Applications (CLKOUT and PHASMD Pins)

The LTC3897-2 features two pins, CLKOUT and PHASMD, that allow other controller ICs to be daisy chained with the LTC3897-2 in PolyPhase applications. The clock output signal on the CLKOUT pin can be used to synchronize additional power stages in a multiphase power supply solution feeding a single, high current output or multiple separate outputs. The PHASMD pin is used to adjust the phase of the CLKOUT signal as well as the relative phases between the two internal controllers, as summarized in Table 2. The phases are calculated relative to the zero degrees phase being defined as the rising edge of the bottom gate driver output of controller 1 (BG1). Depending on the phase selection, a PolyPhase application with multiple LTC3897-2s can be configured for 2-, 3-, 4- , 6- and 12-phase operation.

Table 2.

V_{PHASMD}	CONTROLLER 2 PHASE	CLKOUT PHASE
GND	180°	60°
Floating	180°	90°
$INTV_{CC}$	240°	120°

CLKOUT is disabled when the controller is in shutdown or in sleep mode.

OPERATION

Boost Controller Operation When V_{IN} > Regulated V_{OUT}

When the input voltage to the boost channel rises above the regulated V_{OUT} voltage, the boost controller can behave differently depending on the mode, inductor current and V_{IN} voltage. In forced continuous mode, the loop works to keep the top MOSFET on continuously once V_{IN} rises above V_{OUT}. The internal charge pump delivers current to the boost capacitor to maintain a sufficiently high TG voltage. The amount of current the charge pump can deliver is characterized by two curves in the Typical Performance Characteristics section.

In pulse-skipping mode, if V_{IN} is greater than the regulated V_{OUT} voltage, TG turns on if the inductor current rises above a certain threshold and turns off if the inductor current falls below this threshold. This threshold current is set to approximately 6%, 4% or 3% of the maximum I_{LIM} current when the I_{LIM} pin is grounded, floating or tied to $INTV_{CC}$, respectively. If the controller is programmed to Burst Mode operation under this same V_{IN} condition, then TG remains off regardless of the inductor current.

Operation at Low SENSE Pin Common Mode Voltage

The current comparator in the LTC3897-2 is powered directly from the $SENSE^+$ pin. This enables the common mode voltage of the $SENSE^+$ and $SENSE^-$ pins to operate at as low as 2.3V, which is below the UVLO threshold. The figure on the first page shows a typical application in which the controller's V_{BIAS} is powered from V_{OUT} while the V_{IN} supply can go as low as 2.3V. If the voltage on $SENSE^+$ drops below 2.3V, the SS pin will be held low. When the SENSE voltage returns to the normal operating range, the SS pin will be released, initiating a new soft-start cycle.

BOOST Supply Refresh and Internal Charge Pump

Each top MOSFET driver is biased from the floating bootstrap capacitor, C_B, which normally recharges during each cycle through an internal switch when the bottom MOSFET turns on. There are two considerations for keeping the BOOST supply at the required bias level. During start-up, if the bottom MOSFET is not turned on within 100µs after UVLO goes low, the bottom MOSFET will be forced to turn on for ~400ns. This forced refresh generates enough BOOST-SW voltage to allow the top MOSFET ready to be fully enhanced instead of waiting for the initial few cycles to charge up. There is also an internal charge pump that keeps the required bias on BOOST. The charge pump always operates in both forced continuous mode and pulse-skipping mode. In Burst Mode operation, the charge pump is turned off during sleep and enabled when the chip wakes up. The internal charge pump can normally supply a charging current of 30µA.

Surge Stopper and Ideal Diode Controllers

The LTC3897-2 includes input/output protections that are designed to suppress high voltage surges and limit the input voltage of the boost controller and ensure normal operation in high availability power systems. The LTC3897-2 drives an N-channel MOSFET M_{SG} at the SG pin to limit the voltage and current to the boost controller during supply transients or overcurrent events. The LTC3897-2 also drives a second N-channel MOSFET M_{DG} at the DG pin as an ideal diode to protect the boost controller from damage during reverse polarity input conditions, and to block reverse current flow in the event the input collapses.

The LTC3897-2 operates from a wide range of V_{IN} supply voltage, from 4.2V to 75V. With a clamp limiting the V_{IN} supply, the input voltage may be higher than 75V. The input supply can also be pulled below ground potential by up to 40V without damaging the LTC3897-2. The low power supply requirement of 4.2V allows it to operate even during cold cranking conditions in automotive applications.

Normally, the pass device M_{SG} is fully on, supplying current to the load with very little power loss. If the input voltage surges too high, the voltage amplifier (VA) controls the gate of M_{SG} and regulates the voltage at the IS^- pin to a level that is set by an external resistive divider (SFPB pin) from the IS^- pin to ground and the internal 1.235V reference. The LTC3897-2 also detects an overcurrent condition by monitoring the voltage across an external sense resistor placed between the IS^+ and IS^- pins. An active current limit circuit (IA) controls the gate of M_{SG} to limit the sense voltage to 50mV if IS^- is above 2.5V. In the case of a severe output overcurrent that brings IS^- below 1.5V, the sense voltage is reduced to 27mV to reduce the stress on M_{SG}.

OPERATION

During an overvoltage or overcurrent event, a current source starts charging up the capacitor connected at the TMR pin to ground. The pull-up current source in overcurrent condition is 5 times of that in overvoltage to accelerate turn-off. The pass device M_{SG} stays on and the TMR pin is further charged up until it reaches 1.35V, at which point the SG pin pulls low and turns off M_{SG}. The fault timer allows the load to continue functioning during brief transient events while protecting the MOSFET from being damaged by a long period of input overvoltage, such as load dump in vehicles. The fault timer period decreases with the voltage across the MOSFET, to help keep the MOSFET within its safe operating area (SOA). M_{SG} turns back on after a cool down timer cycle.

The source and drain of MOSFET M_{DG} serve as the anode and cathode of the ideal diode. The LTC3897-2 controls the DG pin to maintain a 30mV forward voltage across the drain and source terminals of M_{DG}. It reduces the power dissipation and increases the available supply voltage to the load, as compared to using a discrete blocking diode. If M_{DG} is driven fully on and the load current results in more than 30mV of forward voltage, the forward voltage is equal to $R_{DS(ON)} \bullet I_{LOAD}$.

In the event of an input short or a power supply failure, reverse current temporarily flows through the MOSFET M_{DG} that is on. If the reverse voltage exceeds –30mV, the LTC3897-2 pulls the DG pin low strongly and turns off M_{DG}, minimizing the disturbance at the output.

If the V_{IN} pin drops below the GND pin voltage, the DG pin is pulled to the CS pin voltage, keeping M_{DG} off. When the SG pin pulls low in any fault condition, the DG pin also pulls low, so both pass devices are turned off.

If the IS^+ and $IS^–$ pins (and so the CS pin, through the body diode of M_{DG}) drops below GND, the SG pin is pulled to the CS pin voltage, turning M_{SG} off and shutting down the forward current path.

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The Typical Application on the first page is a basic LTC3897-2 application circuit. The boost controller of the LTC3897-2 can be configured to use either inductor DCR (DC resistance) sensing or a discrete sense resistor (R_{SENSE}) for current sensing. The choice between the two current sensing schemes is largely a design trade-off between cost, power consumption and accuracy. DCR sensing is becoming popular because it does not require current sensing resistors and is more power-efficient, especially in high current applications. However, current sensing resistors provide the most accurate current limits for the controller. Other external component selection is driven by the load requirement, and begins with the selection of R_{SENSE} (if R_{SENSE} is used) and inductor value. Next, the power MOSFETs are selected. Finally, input and output capacitors are selected. Note that the two controller channels of the LTC3897-2 should be designed with the same components.

SENSE+ and SENSE– Pins

The SENSE+ and SENSE– pins are the inputs to the current comparators. The common mode input voltage range of the current comparators is 2.3V to 65V (abs max), allowing the boost controller to operate from inputs over this full range. The current sense resistor is normally placed at the input of the boost controller in series with the inductor. The SENSE+ pin also provides power to the current comparator. It draws ~250µA during normal operation. There is a small base current of less than 1µA that flows into the SENSE– pin. The high impedance SENSE– input to the current comparators allows accurate DCR sensing

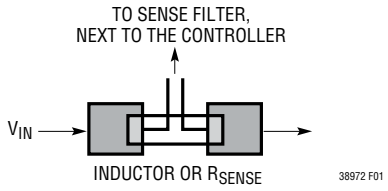
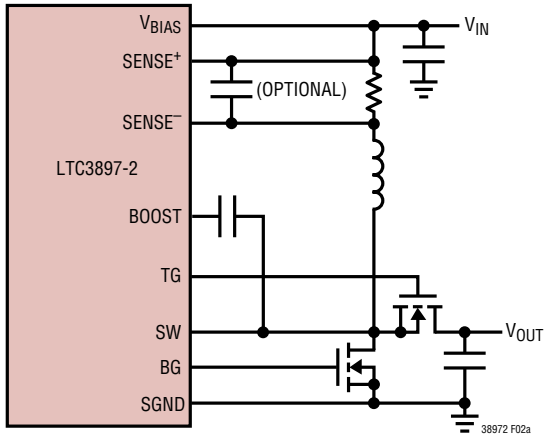


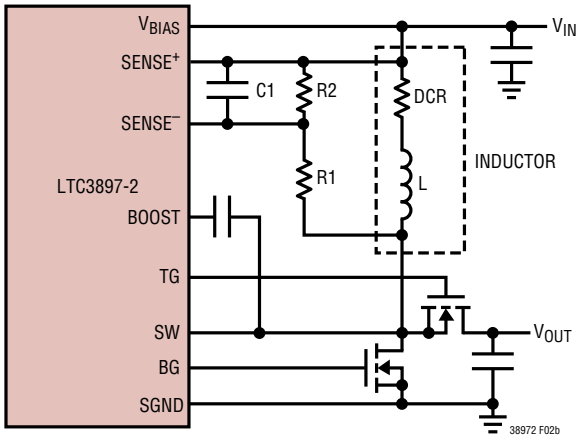
Figure 1. Sense Lines Placement with Inductor or Sense Resistor

Filter components mutual to the sense lines should be placed close to the LTC3897-2, and the sense lines should run close together to a Kelvin connection underneath the current sense element (shown in Figure 1). Sensing current elsewhere can effectively add parasitic inductance and capacitance to the current sense element, degrading the information at the sense terminals and making the programmed current limit unpredictable. If DCR sensing is used (Figure 2b), resistor R1 should be placed close to the switching node, to prevent noise from coupling into sensitive small-signal nodes.

SENSE+ and SENSE– pins are rated at 65V abs max. If input supply is expected to go above 65V, these pins need to be protected using the surge protection voltage regulator (SPFB pin).



(2a) Using a Resistor to Sense Current



PLACE C1 NEAR SENSE PINS $(R1||R2) \bullet C1 = \frac{L}{DCR}$ $R_{SENSE(EQ)} = DCR \bullet \frac{R2}{R1 + R2}$

(2b) Using the Inductor DCR to Sense Current

Figure 2. Two Different Methods of Sensing Current

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Sense Resistor Current Sensing

A typical sensing circuit using a discrete resistor is shown in Figure 2a. R_{SENSE} is chosen based on the required output current.

The current comparator has a maximum threshold $V_{SENSE(MAX)}$. When the I_{LIM} pin is grounded, floating or tied to $INTV_{CC}$, the maximum threshold is set to 48mV, 95mV or 140mV, respectively. The current comparator threshold sets the peak of the inductor current, yielding a maximum average inductor current, I_{MAX}, equal to the peak value less half the peak-to-peak ripple current, ΔI_L. To calculate the sense resistor value, use the equation:

$$R_{SENSE} = \frac{V_{SENSE(MAX)}}{I_{MAX} + \frac{\Delta I_L}{2}}$$

The actual value of I_{MAX} for each channel depends on the required output current $I_{OUT(MAX)}$ and can be calculated using:

$$I_{MAX} = \left(\frac{I_{OUT(MAX)}}{2}\right) \bullet \left(\frac{V_{OUT}}{V_{IN}}\right)$$

When using the controller in low V_{IN} and very high voltage output applications, the maximum inductor current and correspondingly the maximum output current level will be reduced due to the internal compensation required to meet stability criterion for boost regulators operating at greater than 50% duty factor. A curve is provided in the Typical Performance Characteristics section to estimate this reduction in peak inductor current level depending upon the operating duty factor.

Inductor DCR Sensing

For applications requiring the highest possible efficiency at high load currents, the LTC3897-2 is capable of sensing the voltage drop across the inductor DCR, as shown in Figure 2b. The DCR of the inductor can be less than 1mΩ for high current inductors. In a high current application requiring such an inductor, conduction loss through a sense resistor could reduce the efficiency by a few percent compared to DCR sensing.

If the external R1||R2 • C1 time constant is chosen to be exactly equal to the L/DCR time constant, the voltage drop across the external capacitor is equal to the drop across the inductor DCR multiplied by R2/(R1 + R2). R2 scales the voltage across the sense terminals for applications where the DCR is greater than the target sense resistor value. To properly dimension the external filter components, the DCR of the inductor must be known. It can be measured using a good RLC meter, but the DCR tolerance is not always the same and varies with temperature. Consult the manufacturers' data sheets for detailed information.

Using the inductor ripple current value from the inductor value calculation section, the target sense resistor value is:

$$R_{SENSE(EQUIV)} = \frac{V_{SENSE(MAX)}}{I_{MAX} + \frac{\Delta I_L}{2}}$$

To ensure that the application will deliver full load current over the full operating temperature range, choose the minimum value for the maximum current sense threshold ($V_{SENSE(MAX)}$).

Next, determine the DCR of the inductor. Where provided, use the manufacturer's maximum value, usually given at 20°C. Increase this value to account for the temperature coefficient of resistance, which is approximately 0.4%/°C. A conservative value for the maximum inductor temperature ($T_{L(MAX)}$) is 100°C.

To scale the maximum inductor DCR to the desired sense resistor value, use the divider ratio:

$$R_D = \frac{R_{SENSE(EQUIV)}}{DCR_{MAX} \text{ at } T_{L(MAX)}}$$

C1 is usually selected to be in the range of 0.1µF to 0.47µF. This forces R1|| R2 to around 2k, reducing error that might have been caused by the $SENSE^-$ pin's ±1µA current.

The equivalent resistance R1|| R2 is scaled to the room temperature inductance and maximum DCR:

$$R1||R2 = \frac{L}{(DCR \text{ at } 20°C) \bullet C1}$$

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The resistor values are:

$$R1 = \frac{R1||R2}{R_D};\quad R2 = \frac{R1 \bullet R_D}{1-R_D}$$

The maximum power loss in R1 is related to duty cycle, and will occur in continuous mode at $V_{IN} = 1/2V_{OUT}$:

$$P_{LOSS_R1} = \frac{(V_{OUT} - V_{IN}) \bullet V_{IN}}{R1}$$

Ensure that R1 has a power rating higher than this value. If high efficiency is necessary at light loads, consider this power loss when deciding whether to use DCR sensing or sense resistors. Light load power loss can be modestly higher with a DCR network than with a sense resistor, due to the extra switching losses incurred through R1. However, DCR sensing eliminates a sense resistor, reduces conduction losses and provides higher efficiency at heavy loads. Peak efficiency is about the same with either method.

Inductor Value Calculation

The operating frequency and inductor selection are interrelated in that higher operating frequencies allow the use of smaller inductor and capacitor values. Why would anyone ever choose to operate at lower frequencies with larger components? The answer is efficiency. A higher frequency generally results in lower efficiency because of MOSFET gate charge and switching losses. Also, at higher frequency the duty cycle of body diode conduction is higher, which results in lower efficiency. In addition to this basic trade-off, the effect of inductor value on ripple current and low current operation must also be considered.

The inductor value has a direct effect on ripple current. The inductor ripple current ΔI_L decreases with higher inductance or frequency and increases with higher V_{IN}:

$$\Delta I_L = \frac{V_{IN}}{f \bullet L}\left(1 - \frac{V_{IN}}{V_{OUT}}\right)$$

Accepting larger values of ΔI_L allows the use of low inductances, but results in higher output voltage ripple and greater core losses. A reasonable starting point for setting ripple current is $\Delta I_L = 0.3(I_{MAX})$. The maximum ΔI_L occurs at $V_{IN} = 1/2V_{OUT}$.

The inductor value also has secondary effects. The transition to Burst Mode operation begins when the average inductor current required results in a peak current below 25% of the current limit determined by R_{SENSE}. Lower inductor values (higher ΔI_L) will cause this to occur at lower load currents, which can cause a dip in efficiency in the upper range of low current operation. In Burst Mode operation, lower inductance values will cause the burst frequency to decrease. Once the value of L is known, an inductor with low DCR and low core losses should be selected.

Also, for high duty cycle and/or high output voltage applications (particularly those operating near the maximum BG duty factor), it is recommended to keep the operating frequency at 400kHz or less.

Power MOSFET Selection for the BOOST Controller

Two external power MOSFETs must be selected for each phase of the boost controller in the LTC3897-2: one N-channel MOSFET for the bottom (main) switch, and one N-channel MOSFET for the top (synchronous) switch.

The peak-to-peak drive levels are set by the DRV_{CC} voltage. This voltage can range from 5V to 10V depending on configuration of the DRVSET pin. Therefore, both logic-level and standard-level threshold MOSFETs can be used in most applications depending on the programmed DRV_{CC} voltage. Pay close attention to the BV_{DSS} specification for the MOSFETs as well.

The LTC3897-2's unique ability to adjust the gate drive level between 5V to 10V (OPTI-DRIVE) allows an application circuit to be precisely optimized for efficiency. When adjusting the gate drive level, the final arbiter is the total input current for the regulator. If a change is made and the input current decreases, then the efficiency has improved. If there is no change in input current, then there is no change in efficiency.

Selection criteria for the power MOSFETs include the on-resistance $R_{DS(ON)}$, Miller capacitance C_{MILLER}, input voltage and maximum output current. Miller capacitance, C_{MILLER}, can be approximated from the gate charge curve usually provided on the MOSFET manufacturer's data sheet. C_{MILLER} is equal to the increase in gate charge along the horizontal axis while the curve is approximately

APPLICATIONS INFORMATION

flat divided by the specified change in V_{DS}. This result is then multiplied by the ratio of the application applied V_{DS} to the gate charge curve specified V_{DS}. When the IC is operating in continuous mode, the duty cycles for the top and bottom MOSFETs are given by:

$$\text{Main Switch Duty Cycle} = \frac{V_{OUT} - V_{IN}}{V_{OUT}}$$

$$\text{Synchronous Switch Duty Cycle} = \frac{V_{IN}}{V_{OUT}}$$

If the maximum output current is $I_{OUT(MAX)}$ and each channel takes one half of the total output current, the MOSFET power dissipations in each channel at maximum output current are given by:

$$P_{MAIN} = \frac{(V_{OUT} - V_{IN})V_{OUT}}{V^2_{IN}} \bullet \left(\frac{I_{OUT(MAX)}}{2}\right)^2 \bullet (1+\delta)$$

$$\bullet R_{DS(ON)} + k \bullet V_{OUT}{}^3 \bullet \frac{I_{OUT(MAX)}}{2 \bullet V_{IN}}$$

$$\bullet C_{MILLER} \bullet f$$

$$P_{SYNC} = \frac{V_{IN}}{V_{OUT}} \bullet \left(\frac{I_{OUT(MAX)}}{2}\right)^2 \bullet (1+\delta) \bullet R_{DS(ON)}$$

where σ is the temperature dependency of $R_{DS(ON)}$ (approximately 1Ω). The constant k, which accounts for the loss caused by reverse recovery current, is inversely proportional to the gate drive current and has an empirical value of 1.7.

Both MOSFETs have I^2R losses while the bottom N-channel equation includes an additional term for transition losses, which are highest at low input voltages. For high V_{IN} the high current efficiency generally improves with larger MOSFETs, while for low V_{IN} the transition losses rapidly increase to the point that the use of a higher $R_{DS(ON)}$ device with lower C_{MILLER} actually provides higher efficiency. The synchronous MOSFET losses are greatest at high input voltage when the bottom switch duty factor is low or during overvoltage when the synchronous switch is on close to 100% of the period.

The term $(1 + \sigma)$ is generally given for a MOSFET in the form of a normalized $R_{DS(ON)}$ vs Temperature curve, but $\sigma = 0.005/°C$ can be used as an approximation for low voltage MOSFETs.

Boost Converter C_{IN} and C_{OUT} Selection

The input ripple current in a boost converter is relatively low (compared with the output ripple current), because this current is continuous. The voltage rating of the input capacitor C_{IN} at the input end of the boost converter should comfortably exceed the maximum input voltage. Although ceramic capacitors can be relatively tolerant of overvoltage conditions, aluminum electrolytic capacitors are not. Be sure to characterize the input voltage for any possible overvoltage transients that could apply excess stress to the input capacitors.

The value of C_{IN} is a function of the source impedance, and in general, the higher the source impedance, the higher the required input capacitance. The required amount of input capacitance is also greatly affected by the duty cycle. High output current applications that also experience high duty cycles can place great demands on the input supply, both in terms of DC current and ripple current.

In a boost converter, the output has a discontinuous current, so C_{OUT} must be capable of reducing the output voltage ripple. The effects of ESR (equivalent series resistance) and the bulk capacitance must be considered when choosing the right capacitor for a given output ripple voltage. The steady ripple voltage due to charging and discharging the bulk capacitance in a single phase boost converter is given by:

$$V_{RIPPLE} = \frac{I_{OUT(MAX)} \bullet (V_{OUT} - V_{IN(MIN)})}{C_{OUT} \bullet V_{OUT} \bullet f} V$$

where C_{OUT} is the output filter capacitor.

The steady ripple due to the voltage drop across the ESR is given by:

$$\Delta V_{ESR} = I_{L(MAX)} \bullet ESR$$

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The LTC3897-2's boost controller is configured as a 2-phase single output converter where the outputs of the two channels are connected together and both channels have the same duty cycle. With 2-phase operation, the two channels are operated 180 degrees out-of-phase. This effectively interleaves the output capacitor current pulses, greatly reducing the output capacitor ripple current. As a result, the ESR requirement of the capacitor can be relaxed. Because the ripple current in the output capacitor is a square wave, the ripple current requirements for the output capacitor depend on the duty cycle, the number of phases and the maximum output current. Figure 3 illustrates the normalized output capacitor ripple current as a function of duty cycle in a 2-phase configuration. To choose a ripple current rating for the output capacitor, first establish the duty cycle range based on the output voltage and range of input voltage. Referring to Figure 3, choose the worst-case high normalized ripple current as a percentage of the maximum load current.

Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirements. Dry tantalum, special polymer, aluminum electrolytic and ceramic capacitors are all available in surface mount packages. Ceramic capacitors have excellent low ESR characteristics but can have a high voltage coefficient. Capacitors are now available with low ESR and high ripple current ratings (e.g., OS-CON and POSCAP).

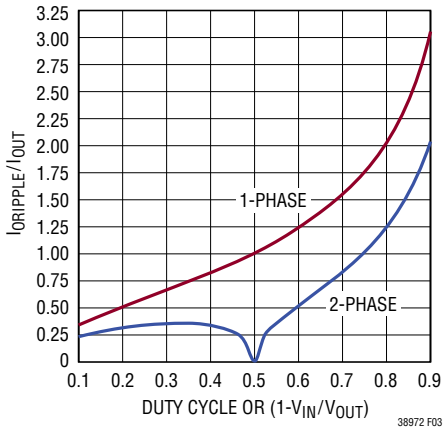


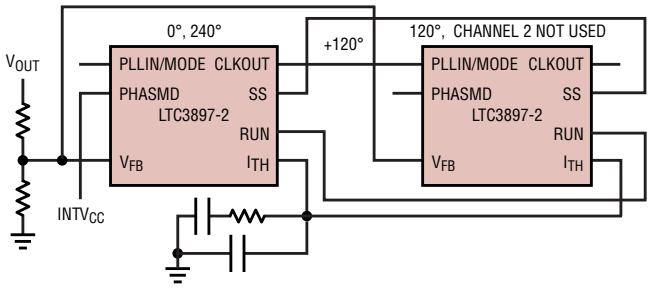
Figure 3. Normalized Output Capacitor Ripple Current (RMS) for a Boost Converter

PolyPhase Operation

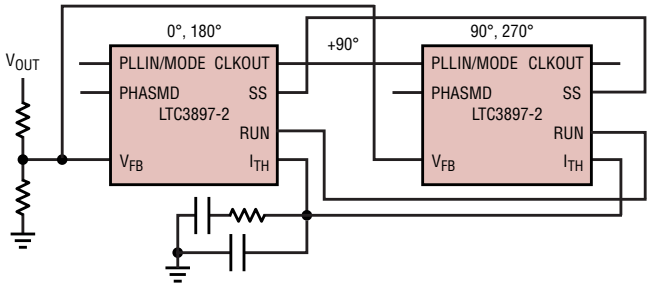
For output loads that demand high current, multiple LTC3897-2s can be cascaded to run out-of-phase to provide more output current and at the same time to reduce input and output voltage ripple. The PLLIN/MODE pin allows the LTC3897-2 to synchronize to the CLKOUT signal of another LTC3897-2. The CLKOUT signal can be connected to the PLLIN/MODE pin of the following LTC3897-2 stage to line up both the frequency and the phase of the entire system.

Tying the PHASMD pin to $INTV_{CC}$, SGND or floating generates a phase difference (between PLLIN/MODE and CLKOUT) of 240°, 60° or 90°, respectively, and a phase difference (between CH1 and CH2) of 120°, 180°or 180°. Figure 4 shows the connections necessary for 3-, 4-, 6- or 12-phase operation. A total of 12 phases can be cascaded to run simultaneously out-of-phase with respect to each other.

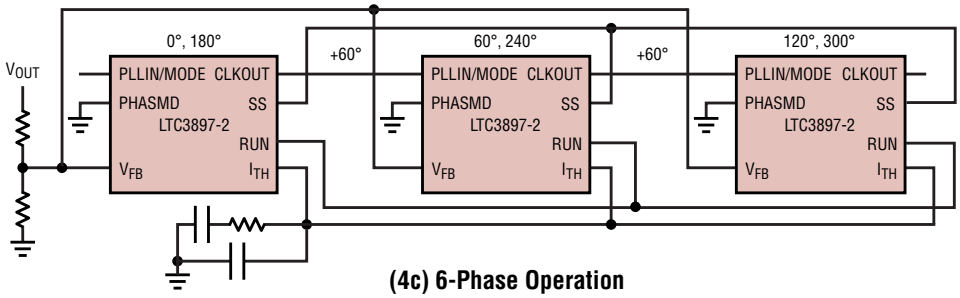
APPLICATIONS INFORMATION



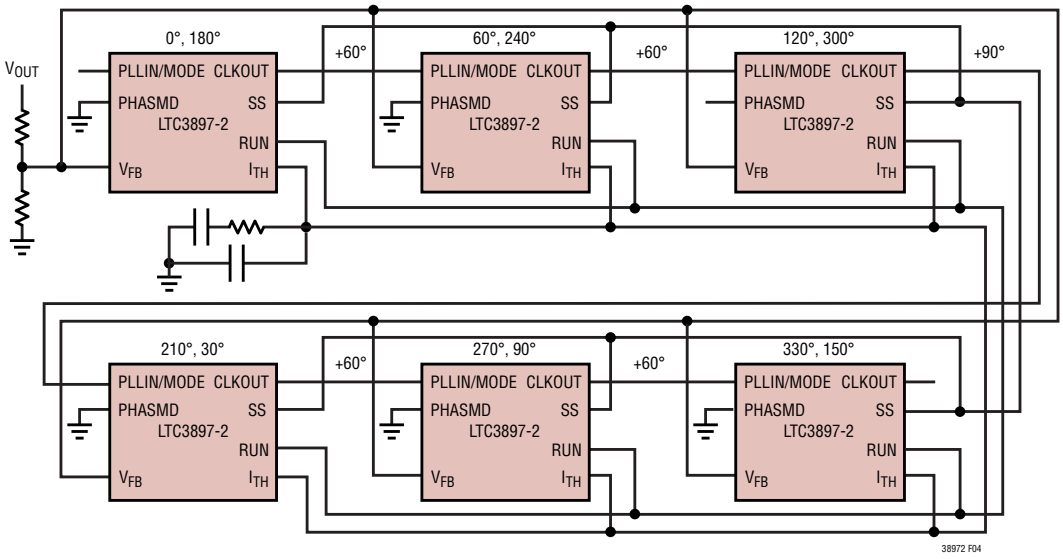
(4a) 3-Phase Operation



(4b) 4-Phase Operation



(4c) 6-Phase Operation



(4d) 12-Phase Operation

Figure 4. PolyPhase Operation

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Setting Output Voltage

The LTC3897-2 output voltage is set by an external feedback resistor divider carefully placed across the output, as shown in Figure 5. The regulated output voltage is determined by:

$$V_{OUT} = 1.2V\left(1+\frac{R_B}{R_A}\right)$$

Great care should be taken to route the V_{FB} line away from noise sources, such as the inductor or the SW line. Also keep the V_{FB} node as small as possible to avoid noise pickup.

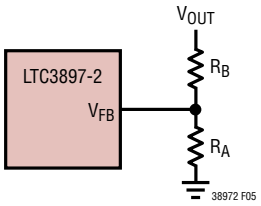


Figure 5. Setting Output Voltage

Soft-Start (SS Pin)

The start-up of V_{OUT} is controlled by the voltage on the SS pin. When the voltage on the SS pin is less than the internal 1.2V reference, the LTC3897-2 regulates the V_{FB} pin voltage to the voltage on the SS pin instead of 1.2V.

Soft-start is enabled by simply connecting a capacitor from the SS pin to ground, as shown in Figure 6. An internal 10µA current source charges the capacitor, providing a linear ramping voltage at the SS pin. The LTC3897-2 will regulate the V_{FB} pin (and hence, V_{OUT}) according to the voltage on the SS pin, allowing V_{OUT} to rise smoothly from V_{IN} to its final regulated value. The total soft-start time will be approximately:

$$t_{SS} = C_{SS} \bullet \frac{1.2V}{10\mu A}$$

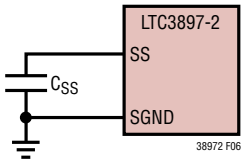


Figure 6. Using the SS Pin to Program Soft-Start

DRV_{CC} and $INTV_{CC}$ Regulators (OPTI-DRIVE)

The LTC3897-2 features two separate internal P-channel low dropout linear regulators (LDO) that supply power at the DRV_{CC} pin from either the V_{BIAS} supply pin or the $EXTV_{CC}$ pin depending on the connections of the $EXTV_{CC}$ and DRVSET pins. A third P-channel LDO supplies power at the $INTV_{CC}$ pin from the DRV_{CC} pin. DRV_{CC} powers the gate drivers whereas $INTV_{CC}$ powers much of the LTC3897-2's internal circuitry. The V_{BIAS} LDO and the $EXTV_{CC}$ LDO regulate DRV_{CC} between 5V to 10V, depending on how the DRVSET pin is set. Each of these LDOs can supply a peak current of at least 50mA and must be bypassed to ground with a minimum of 4.7µF ceramic capacitor. Good bypassing is needed to supply the high transient currents required by the MOSFET gate drivers and to prevent interaction between the channels. The $INTV_{CC}$ supply must be bypassed with a 0.1µF ceramic capacitor.

The DRVSET pin programs the DRV_{CC} supply voltage. Tying the DRVSET pin to $INTV_{CC}$ programs DRV_{CC} to 10V. Tying the DRVSET pin to GND programs DRV_{CC} to 6V. By placing a 50k to 100k resistor between DRVSET and GND the DRV_{CC} voltage can be programmed between 5V to 10V, as shown in Figure 7.

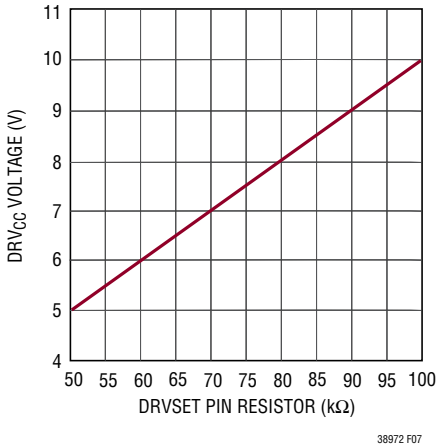


Figure 7. Relationship Between DRV_{CC} Voltage and Resistor Value at DRVSET Pin

APPLICATIONS INFORMATION

High voltage applications in which large MOSFETs are being driven at high frequencies may cause the maximum junction temperature rating for the LTC3897-2 to be exceeded. The DRV_{CC} current, which is dominated by the gate charge current, may be supplied by either the V_{BIAS} LDO or the $EXTV_{CC}$ LDO. When the voltage on the $EXTV_{CC}$ pin is less than its switchover threshold (4.7V or 7.7V as determined by the DRVUV pin), the V_{BIAS} LDO is enabled. Power dissipation for the IC in this case is highest and is equal to $V_{BIAS} \bullet I_{DRVCC}$. The gate charge current is dependent on operating frequency as discussed in the Efficiency Considerations section. The junction temperature can be estimated by using the equations given in Note 2 of the Electrical Characteristics. For example, using the LTC3897-2 in the QFN package and setting DRV_{CC} to 6V, the DRV_{CC} current is limited to less than 47mA from a 40V supply when not using the $EXTV_{CC}$ supply at a 70°C ambient temperature:

$$T_J = 70°C + (47mA)(40V – 6V)(34°C/W) = 125°C$$

In the FE package, , the DRV_{CC} current is limited to less than 57mA from a 40V supply when not using the $EXTV_{CC}$ supply at a 70°C ambient temperature:

$$T_J = 70°C + (57mA)(40V – 6V)(28°C/W) = 125°C$$

To prevent the maximum junction temperature from being exceeded, the V_{BIAS} supply current must be checked while operating in forced continuous mode (PLLIN/MODE = $INTV_{CC}$) at maximum V_{BIAS}.

When the voltage applied to $EXTV_{CC}$ rises above its switchover threshold, the V_{BIAS} LDO is turned off and the $EXTV_{CC}$ LDO is enabled. The $EXTV_{CC}$ LDO remains on as long as the voltage applied to $EXTV_{CC}$ remains above the switchover threshold minus the comparator hysteresis. The $EXTV_{CC}$ LDO attempts to regulate the DRV_{CC} voltage to the voltage as programmed by the DRVSET pin, so while $EXTV_{CC}$ is less than this voltage, the LDO is in dropout and the DRV_{CC} voltage is approximately equal to $EXTV_{CC}$. When $EXTV_{CC}$ is greater than the programmed voltage, up to an absolute maximum of 14V, DRV_{CC} is regulated to the programmed voltage. If more current is required through the $EXTV_{CC}$ LDO than is specified, an external Schottky diode can be added between the $EXTV_{CC}$ and DRV_{CC} pins. In this case, do not apply more than 10V to the $EXTV_{CC}$ pin and make sure that $EXTV_{CC} \leq V_{BIAS}$. Significant thermal gains can be realized by powering DRV_{CC} from an external supply. Tying the $EXTV_{CC}$ pin to an 8.5V supply reduces the junction temperature in the previous example from 125°C to 74°C:

$$T_J = 70°C + (47mA)(8.5V – 6V)(34°C/W) = 74°C$$

and from 125°C to 74°C in an FE package:

$$T_J = 70°C + (57mA)(8.5V – 6V)(34°C/W) = 74°C$$

The following list summarizes two possible connections for $EXTV_{CC}$:

1. $EXTV_{CC}$ grounded. This will cause DRV_{CC} to be powered from the internal V_{BIAS} regulator resulting in an efficiency penalty of up to 10% at high input voltages.
2. $EXTV_{CC}$ connected to an external supply. If an external supply is available in the 5V to 14V range, it may be used to power $EXTV_{CC}$ providing it is compatible with the MOSFET gate drive requirements. Ensure that $EXTV_{CC} \leq V_{BIAS}$.

Topside MOSFET Driver Supply (C_B)

External bootstrap capacitors, C_B, connected to the BOOST pins supply the gate drive voltage for the topside MOSFET. The LTC3897-2 features an internal switch between DRV_{CC} and the BOOST pin for each controller. These internal switches eliminate the need for external bootstrap diodes between DRV_{CC} and BOOST. Capacitor C_B in the Functional Diagram is charged through this internal switch from DRV_{CC} when the SW pin is low. When the topside MOSFET is to be turned on, the driver places the C_B voltage across the gate-source of the MOSFET. This enhances the top MOSFET switch and turns it on. The switch node voltage, SW, rises to V_{IN} and the BOOST pin follows. With the topside MOSFET on, the boost voltage is above the input supply: $V_{BOOST} = V_{IN} + V_{DRVCC}$ ($V_{BOOST} = V_{OUT} + V_{DRVCC}$ for the boost controller). The value of the boost capacitor, C_B, needs to be 100 times that of the total input capacitance of the topside MOSFET(s).

APPLICATIONS INFORMATION

Phase-Locked Loop and Frequency Synchronization

The LTC3897-2 has an internal phase-locked loop (PLL) comprised of a phase frequency detector, a lowpass filter and a voltage-controlled oscillator (VCO). This allows the turn-on of the bottom MOSFET of channel 1 to be locked to the rising edge of an external clock signal applied to the PLLIN/MODE pin. The turn-on of channel 2's bottom MOSFET is thus 180 degrees out-of-phase with the external clock. The phase detector is an edge-sensitive digital type that provides zero degrees phase shift between the external and internal oscillators. This type of phase detector does not exhibit false lock to harmonics of the external clock.

If the external clock frequency is greater than the internal oscillator's frequency, f_{OSC}, then current is sourced continuously from the phase detector output, pulling up the VCO input. When the external clock frequency is less than f_{OSC}, current is sunk continuously, pulling down the VCO input. If the external and internal frequencies are the same but exhibit a phase difference, the current sources turn on for an amount of time corresponding to the phase difference. The voltage at the VCO input is adjusted until the phase and frequency of the internal and external oscillators are identical. At the stable operating point, the phase detector output is high impedance and the internal filter capacitor, C_{LP} , holds the voltage at the VCO input.

Typically, the external clock (on the PLLIN/MODE pin) input high threshold is 1.6V, while the input low threshold is 1.2V.

Note that the LTC3897-2 can only be synchronized to an external clock whose frequency is within range of the LTC3897-2's internal VCO, which is nominally 55kHz to 600kHz. This is guaranteed to be between 75kHz and 550kHz.

Rapid phase locking can be achieved by using the FREQ pin to set a free-running frequency near the desired synchronization frequency. The VCO's input voltage is prebiased at a frequency corresponding to the frequency set by the FREQ pin. Once prebiased, the PLL only needs to adjust the frequency slightly to achieve phase lock and synchronization. Although it is not required that the free-running frequency be near external clock frequency, doing so will prevent the operating frequency from passing through a large range of frequencies as the PLL locks.

Table 3 summarizes the different states in which the FREQ pin can be used.

Table 3.

FREQ PIN	PLLIN/MODE PIN	FREQUENCY
0V	DC Voltage	350kHz
$INTV_{CC}$	DC Voltage	550kHz
Resistor	DC Voltage	50kHz to 550kHz
Any of the Above	External Clock	Phase Locked to External Clock

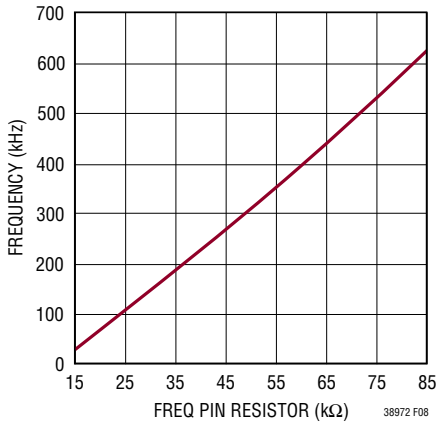


Figure 8. Relationship Between Oscillator Frequency and Resistor Value at the FREQ Pin

Minimum On-Time Considerations

Minimum on-time, $t_{ON(MIN)}$, is the smallest time duration that the LTC3897-2 is capable of turning on the bottom MOSFET. It is determined by internal timing delays and the gate charge required to turn on the top MOSFET. Low duty cycle applications may approach this minimum on-time limit.

In forced continuous mode, if the duty cycle falls below what can be accommodated by the minimum on-time, the controller will begin to skip cycles but the output will continue to be regulated. More cycles will be skipped when V_{IN} increases. Once V_{IN} rises above V_{OUT}, the loop keeps the top MOSFET continuously on. The minimum on-time for the LTC3897-2 is approximately 90ns.

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Efficiency Considerations

The percent efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the greatest improvement. Percent efficiency can be expressed as:

%Efficiency = 100% – (L1 + L2 + L3 + ...)

where L1, L2, etc., are the individual losses as a percentage of input power.

Although all dissipative elements in the circuit produce losses, five main sources usually account for most of the losses in LTC3897-2 circuits: 1) IC V_{BIAS} current, 2) DRV_{CC} regulator current, 3) I^2R losses, 4) bottom MOSFET transition losses, 5) body diode conduction losses.

1. The V_{BIAS} current is the DC supply current given in the Electrical Characteristics table, which excludes MOSFET driver and control currents. V_{BIAS} current typically results in a small (<0.1%) loss.
2. DRV_{CC} current is the sum of the MOSFET driver and control currents. The MOSFET driver current results from switching the gate capacitance of the power MOSFETs. Each time a MOSFET gate is switched from low to high to low again, a packet of charge, ΔQ, moves from DRV_{CC} to ground. The resulting $\Delta Q/\Delta t$ is a current out of DRV_{CC} that is typically much larger than the control circuit current. In continuous mode, $I_{GATECHG} = f(QT + QB)$, where QT and QB are the gate charges of the topside and bottom side MOSFETs.
3. DC I^2R losses. These arise from the resistances of the MOSFETs, sensing resistor, inductor and PC board traces and cause the efficiency to drop at high output currents.
4. Transition losses apply only to the bottom MOSFET(s), and become significant only when operating at low input voltages. Transition losses can be estimated from:

$$\text{Transition Loss} = (1.7)\frac{V_{OUT}^3}{V_{IN}} \bullet \frac{I_{OUT(MAX)}}{2} \bullet C_{RSS} \bullet f$$

5. Body diode conduction losses are more significant at higher switching frequency. During the dead time, the loss in the top MOSFETs is $I_{OUT} \bullet V_{DS}$, where V_{DS} is around 0.7V. At higher switching frequency, the dead time becomes a good percentage of switching cycle and causes the efficiency to drop.

Other hidden losses, such as copper trace and internal battery resistances, can account for an additional efficiency degradation in portable systems. It is very important to include these system-level losses during the design phase.

Overvoltage Fault

The LTC3897-2 limits the voltage at the IS^- pin during an overvoltage situation. An internal voltage amplifier regulates the SG pin voltage to maintain 1.235V at the SPFB pin (Figure 14). During this period of time, the N-channel MOSFET M_{SG} remains on and supplies current to the load. This allows uninterrupted operation during brief overvoltage transient events.

If the voltage regulation loop is engaged for longer than the timeout period, set by the timer capacitor, an overvoltage fault is detected. The SG pin is pulled down to the CS pin by a 130mA current, turning M_{SG} off. This prevents M_{SG} from being damaged during a long period of overvoltage, such as during load dump in automobiles. After the fault condition has disappeared and a cool down period has transpired, the SG pin starts to pull high again.

Overcurrent Fault

The LTC3897-2 features an adjustable current limit that protects against output short circuits and excessive load current. During an overcurrent event, the SG pin is regulated to limit the current sense voltage across the IS^+ and IS^- pins to 50mV when IS^- is above 2.5V. The current limit sense voltage is reduced to 27mV when IS^- is below 1.5V for additional protection during an output overcurrent event.

A current sense resistor is placed between IS^+ and IS^- and its value (R_{IS}) is determined by:

$$R_{IS} = \frac{\Delta V_{IS}}{I_{IS}}$$

where I_{IS} is the desired current limit.

APPLICATIONS INFORMATION

An overcurrent fault occurs when the current limit circuitry has been engaged for longer than the timeout delay set by the timer capacitor. The SG pin is then immediately pulled low by 130mA to the CS pin, turning off the MOSFET M_{SG}. After the fault condition has disappeared and a cool down period has transpired, the SG pin is allowed to pull back up and turn on the pass device.

During a fault event, after the MOSFET M_{SG} is turned off suddenly, the voltage on V_P node (see Figure 17) will discharge at a rate dependent on the amount of capacitance on V_P, the inductance value of the boost inductors L1 and L2, and the load current. A diode D_{IN} connected between ground and the V_P node is needed to provide a path for the inductor currents to continue to flow until they naturally discharge to zero. Since this diode only conducts large current transiently during a fault event and is normally reverse biased, it does not need to be rated for a large DC current. For most applications, a ~1A rated diode is sufficient.

Fault Timer

The LTC3897-2 includes an adjustable fault timer. Connecting a capacitor from the TMR pin to ground sets the delay period before the MOSFET M_{SG} is turned off during an overvoltage or overcurrent fault condition. The same capacitor also sets the cool down period before M_{SG} is allowed to turn back on after the fault condition has disappeared. Once a fault condition is detected, a current source charges up the TMR pin. The current level varies depending on the voltage drop across the V_{IN} pin and the IS^- pin, corresponding to the MOSFET V_{DS}. The on time is inversely proportional to the voltage drop across the MOSFET. This scheme therefore takes better advantage of the available safe operating area (SOA) of the MOSFET than would a fixed timer current.

The timer current starts at around 2.5µA with 0.5V or less of $V_{IN} – V_{IS^-}$, increasing linearly to 53µA with 70V of $V_{IN} – V_{IS^-}$ during an overvoltage fault:

$$I_{TMR(UP)OV} = 2.5\mu A + 0.73[\mu A/V] \bullet (V_{IN^-} V_{IS^-} – 0.5V)$$

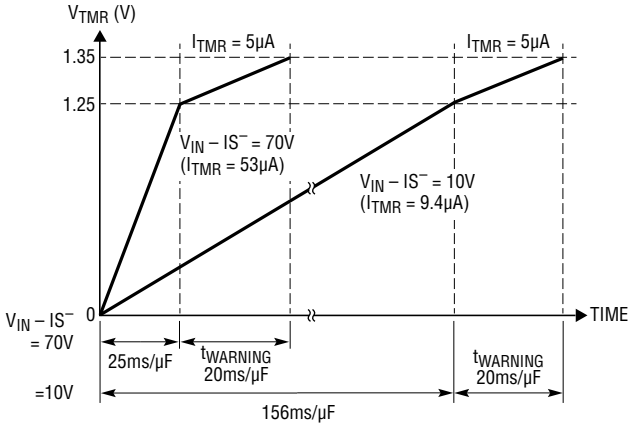
During an overcurrent fault, the timer current starts at 10µA with 0.5V or less of $V_{IN} – V_{IS^-}$ and increases to 250µA with 70V of $V_{IN} – V_{IS^-}$:

$$I_{TMR(UP)OC} = 10\mu A + 3.45[\mu A/V] \bullet (V_{IN} – V_{IS^-} – 0.5V)$$

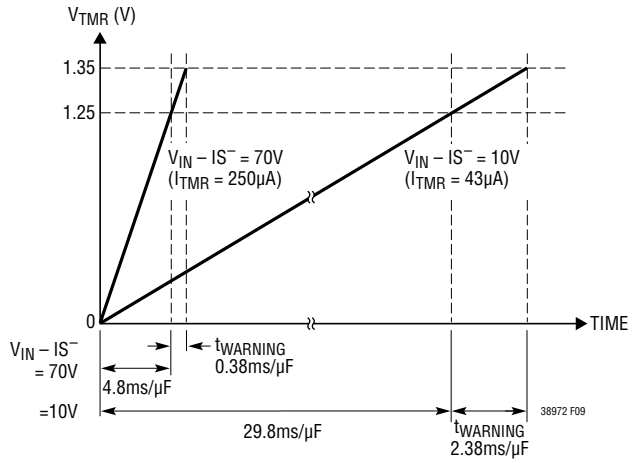
This arrangement allows the pass device to turn off faster during an overcurrent event, since more power is dissipated under this condition. Refer to the Typical Performance Characteristics section for the timer current at different $V_{IN} – IS^-$ in both overvoltage and overcurrent events.

When the voltage at the TMR pin, V_{TMR}, reaches 1.25V, and in the case of an overvoltage fault, the timer current switches to a fixed 5µA. The interval between V_{TMR} reaches 1.25V and the MOSFET M_{SG} turning off is given by

$$t_{WARNING} = \frac{C_{TMR} \bullet 100mV}{5\mu A}$$



(9a) Overvoltage Fault Timer Current



(9b) Overcurrent Fault Timer Current

Figure 9. Fault Timer Current of the LTC3897-2

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This constant early warning period allows the boost controller to perform housekeeping functions before the supply is cut off. After V_{TMR} crosses the 1.35V threshold, the pass device M_{SG} turns off immediately. Note that during an overcurrent event, the timer current is not reduced to 5µA after V_{TMR} has reached 1.25V threshold, since it would lengthen the overall fault timer period and cause more stress on the power transistor during an overcurrent event.

Assuming $V_{IN} – IS^–$ remains constant, the on-time of SG during an overvoltage fault is:

$$t_{OV} = \frac{C_{TMR} \bullet 1.25V}{I_{TMR(UP)OV}} + \frac{C_{TMR} \bullet 100mV}{5\mu A}$$

and that during an overcurrent fault is:

$$t_{OC} = \frac{C_{TMR} \bullet 1.35V}{I_{TMR(UP)OC}}$$

If the fault condition disappears after TMR reaches 1.25V but is lower than 1.35V, the TMR pin is discharged by 2µA. If the boost controller is enabled, the value of CTMR should be small, such as 1nF, to limit the large current during an output overcurrent event.

Cool Down Period and Restart

As soon as TMR reaches 1.35V and SG pulls low in a fault condition, the TMR pin starts discharging with a 2µA current. When the TMR pin voltage drops to 0.15V, TMR charges with 2.5µA. When TMR reaches 1.35V, it starts discharging again with 2µA. This pattern repeats 32 times to form a long cool down timer period before retry. At the end of the cool down period (when the TMR pin voltage drops to 0.15V the 32nd time), the LTC3897-2 retries, pulling the SG pin up and turning on the pass device M_{SG}. The total cool down timer period is given by:

$$t_{COOL} = \frac{32 \bullet C_{TMR} \bullet 1.2V}{2\mu A} + \frac{31 \bullet C_{TMR} \bullet 1.2V}{2.5\mu A}$$

Reverse Input Protection

The LTC3897-2 can withstand reverse voltage without damage. The V_{IN}, SGEN, SG, CS and DG pins can all withstand up to –40V with respect to GND.

The LTC3897-2 controls a second N-channel MOSFET (M_{DG}) as an ideal diode to replace an in-line blocking diode for reverse input protection with minimum voltage drop in normal operation. In the event of an input short or a power supply brownout, reverse current may temporarily flow through M_{DG}. The LTC3897-2 detects this reverse current and immediately pulls the DG pin to the CS pin, turning off M_{DG}. This minimizes discharge of the output reservoir capacitor and holds up the output voltage. In the case where the input supply drops below ground, the CS pin is pulled below ground through the body diode of M_{SG}. The LTC3897-2 responds to this condition by shorting the DG pin to the CS pin, keeping M_{DG} off.

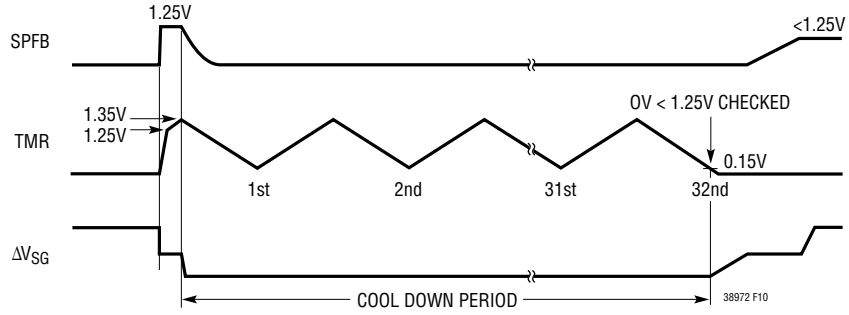


Figure 10. Auto-Retry Cool Down Timer Cycle Following Overvoltage Fault

APPLICATIONS INFORMATION

Limiting Inrush Current and SG Pin Compensation

The LTC3897-2 limits the inrush current to any load capacitance and through the inductor of the boost controller by controlling the SG pin voltage slew rate. An external capacitor, C_{SG}, can be connected from SG to ground to slow down the inrush current further at the expense of slower turn-off time. The gate capacitor is set at:

$$C_{SG} = \frac{I_{SG(UP)}}{I_{INRUSH}} C_L$$

where $I_{SG(UP)}$ is the SG pin pull-up current, I_{INRUSH} is the desired inrush current, C_L is total load capacitance at the output. In typical applications, a C_{SG} of 6.8nF is recommended for loop compensation during overvoltage and overcurrent events. With input voltage steps faster than 5V/µs, a larger gate capacitor helps prevent self enhancement of the N-channel MOSFET.

The added gate capacitor slows down the turn-off time during fault conditions and allows higher peak currents to build up during an output overcurrent event. If this is a concern, an extra resistor, R3, in series with C_{SG} can restore the turn-off time (Figure 14). A diode, D4, should be placed across R3 with the cathode connected to C_{SG}. In a fast transient input step, D4 provides a bypass path to C_{SG} for the benefit of holding SG low and preventing self enhancement.

Supply Transient Protection

The LTC3897-2 is tested to operate to 75V and guaranteed to be safe from damage between 76V and –40V. Voltage transients above 76V or below –40V may cause permanent damage. During an overcurrent condition, the large change in current flowing through power supply traces coupled with parasitic inductances from associated wiring can cause destructive voltage transients in both positive and negative directions at the V_{IN}, CS, and IS^- pins. To reduce the voltage transients, minimize the power trace parasitic inductance by using short, wide traces. A small RC filter at the V_{IN} pin filters high voltage spikes of short pulse width.

Another way to limit supply transients above 76V at the V_{IN} pin is to use a Zener diode and a resistor, D1 and R1, as shown in Figure 11. D1 clamps voltage spikes at the V_{IN} pin while R1 limits the current through D1 to a safe level during the surge. In the negative direction, D1 along with R1 clamps the V_{IN} pin near GND. The inclusion of R1 in series with the V_{IN} pin increases the minimum required supply voltage due to the extra voltage drop across the resistor, which is determined by the supply current of the LTC3897-2 and the leakage current of D1. 2.2k adds about 1V to the minimum operating voltage.

For sustained, elevated supply voltages, the power dissipation of R1 becomes unacceptable. This can be resolved by using an external NPN transistor (Q1 in Figure 11) as a buffer. To protect Q1 against supply reversal, block the collector of Q1 with a series diode or tie it to the cathode of D2 and D3 in Figure 14.

Transient suppressor D2 in Figure 14 clamps the input voltage to 200V for voltage transients higher than 200V, to prevent breakdown of M_{SG}. It also blocks forward conduction in D3. D3 limits the CS pin voltage to 24V below GND when the input goes negative. C_L helps absorb the inductive energy at the output upon a sudden input short, protecting the IS^+ and IS^- pins.

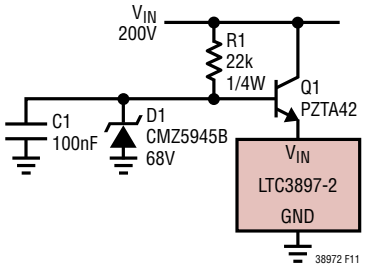


Figure 11. Buffering V_{IN} to Extend Input Supply Range

MOSFET Selection for the Surge Stopper and Ideal Diode

The LTC3897-2 drives two N-channel MOSFETs, M_{SG} and M_{DG}, as the pass devices to conduct the load current (Figure 14). The important features are on-resistance, $R_{DS(ON)}$, the maximum drain-source voltage, BV_{DSS}, the threshold voltage, and the safe operating area, SOA.

APPLICATIONS INFORMATION

The maximum drain-source voltage rating must be higher than the maximum input voltage. If the output is shorted to ground or in an overvoltage event, the full supply voltage will appear across M_{SG}. If the input is shorted to ground, M_{DG} will be stressed by the voltage held up at the output. The gate drive for both MOSFETs is guaranteed to be more than 10V and less than 16V for those applications with V_{IN} higher than 8V. This allows the use of standard threshold voltage N-channel MOSFETs. For systems with V_{IN} less than 8V, a logic-level MOSFET is required since the gate drive can be as low as 5V. For supplies of 24V or higher, a 15V Zener diode is recommended to be placed between gate and source of each MOSFET for extra protection.

Transient Stress in the MOSFET

The SOA of the MOSFET must encompass all fault conditions. In normal operation the pass devices are fully on, dissipating very little power. But during either overvoltage or overcurrent faults, the SG pin is controlled to regulate either the input voltage for the boost converter or the current through MOSFET M_{SG}. Large current and high voltage drop across M_{SG} can coexist in these cases. The SOA curves of the MOSFET must be considered carefully along with the selection of the fault timer capacitor.

During an overvoltage event, the LTC3897-2 drives the pass MOSFET M_{SG} to regulate the input voltage of the boost converter at an acceptable level. The load circuitry may continue operating throughout this interval, but only at the expense of dissipation in the MOSFET pass device. MOSFET dissipation or stress is a function of the input voltage waveform, regulation voltage and load current. The MOSFET must be sized to survive this stress.

Most transient event specifications use the model shown in Figure 12. The idealized waveform comprises a linear ramp of rise time t_r, reaching a peak voltage of V_{PK} and exponentially decaying back to V_{IN} with a time constant of τ. A typical automotive transient specification has constants of t_r = 10µs, V_{PK} = 80V and = 1ms. A surge condition known as “load dump” has constants of t_r = 5ms, V_{PK} = 60V and τ = 200ms.

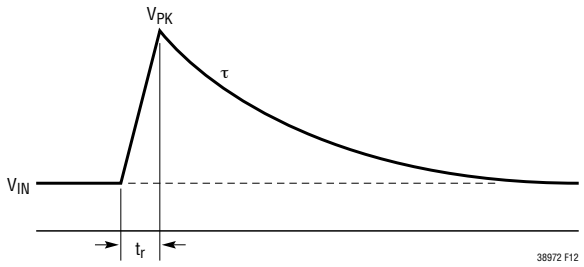


Figure 12. Prototypical Transient Waveform

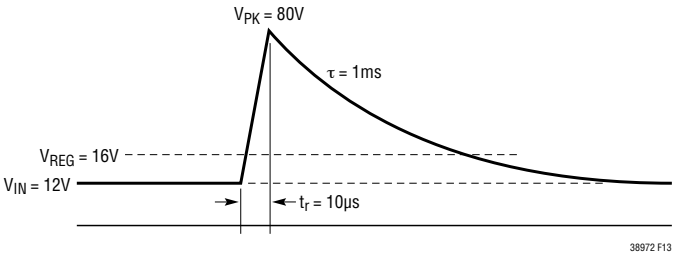


Figure 13. Safe Operating Area Required to Survive Prototypical Transient Waveform

MOSFET stress is the result of power dissipated within the device. For long duration surges of 100ms or more, stress is increasingly dominated by heat transfer; this is a matter of device packaging and mounting, and heat sink thermal mass. This is analyzed by simulation, using the MOSFET’s thermal model.

For short duration transients of less than 100ms, MOSFET survival is increasingly a matter of SOA, an intrinsic property of the MOSFET. SOA quantifies the time required at any given condition of V_{DS} and I_D to raise the junction temperature of the MOSFET to its rated maximum. MOSFET SOA is expressed in units of watt-squared-seconds (P^2t), which is an integral of $P(t)^2dt$ over the duration of the transient. This figure is essentially constant for intervals of less than 100ms for any given device type, and rises to infinity under DC operating conditions. Destruction mechanisms other than bulk die temperature distort the lines of an accurately drawn SOA graph so that P^2t is not the same for all combinations of I_D and V_{DS}. In particular P^2t tends to degrade as V_{DS} approaches the maximum rating, rendering some devices useless for absorbing energy above a certain voltage.

APPLICATIONS INFORMATION

Calculating Transient Stress for M_{SG}

To select a MOSFET suitable for any given application, the SOA stress of M_{SG} must be calculated for each input transient which shall not interrupt operation. It is then a simple matter to choose a device which has adequate SOA to survive the maximum calculated stress. P^2t for a prototypical transient waveform is calculated as follows (Figure 13).

Let:

$a = V_{REG} - V_{IN}$

$b = V_{PK} - V_{IN}$

where V_{IN} = Nominal Input Voltage.

Then:

$$P^2t = I_{LOAD}^2 \left[\frac{1}{3} t_r \frac{(b-a)^3}{b} + \frac{1}{2}\tau\left(2a^2 \ln\frac{b}{a} + 3a^2 + b^2 + 4ab\right)\right]$$

Typically $V_{REG} \approx V_{IN}$ and $\tau >> t_r$ simplifying the above to:

$$P^2t = \frac{1}{2} I_{LOAD}^2 \left(V_{PK} - V_{REG}\right)^2 \tau$$

For the transient conditions of V_{PK} = 80V, V_{IN} = 12V, V_{REG}= 16V, t_r = 10µs and τ = 1ms, and a load current of 3A, P^2t is 18.4W^2s—easily handled by a MOSFET in a D-pak package. The P^2t of other transient waveshapes is evaluated by integrating the square of MOSFET power versus time. LTspice® can be used to simulate timer behavior for more complex transients and cases where overvoltage and overcurrent faults coexist.

Overcurrent Stress for M_{SG}

SOA stress of M_{SG} must also be calculated for output overcurrent conditions. Short-circuit P^2t is given by:

$$P^2t = \left(V_{IN} \bullet \frac{\Delta V_{IS}}{R_{IS}}\right)^2 \bullet t_{OC}$$

where ΔV_{IS} is the overcurrent fault threshold and t_{OC} is the overcurrent timer interval.

For V_{IN} = 15V, IS^- = 0V, ΔV_{IS} = 25mV, R_{IS} = 12mΩ and C_{TMR} = 100nF, P^2t is 2.2W^2s—less than the transient SOA calculated in the previous example. Nevertheless, to account for circuit tolerances this figure should be doubled to 4.4W^2s.

Checking Transient Response (Boost Controller)

The regulator loop response can be checked by looking at the load current transient response. Switching regulators take several cycles to respond to a step in DC (resistive) load current. When a load step occurs, V_{OUT} shifts by an amount equal to $\Delta I_{LOAD(ESR)}$, where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT} generating the feedback error signal that forces the regulator to adapt to the current change and return V_{OUT} to its steady-state value. During this recovery time V_{OUT} can be monitored for excessive overshoot or ringing, which would indicate a stability problem. OPTI-LOOP® compensation allows the transient response to be optimized over a wide range of output capacitance and ESR values. The availability of the I_{TH} pin not only allows optimization of control loop behavior, but it also provides a DC coupled and AC filtered closed loop response test point. The DC step, rise time and settling at this test point truly reflects the closed loop response. Assuming a predominantly second order system, phase margin and/or damping factor can be estimated using the percentage of overshoot seen at this pin. The bandwidth can also be estimated by examining the rise time at the pin. The I_{TH} external components shown in the Figure 10 circuit will provide an adequate starting point for most applications.

The I_{TH} series $R_C - C_C$ filter sets the dominant pole-zero loop compensation. The values can be modified slightly to optimize transient response once the final PC layout is complete and the particular output capacitor type and value have been determined. The output capacitors must be selected because the various types and values determine the loop gain and phase. An output current pulse of 20% to 80% of full-load current having a rise time of 1µs to 10µs will produce output voltage and I_{TH} pin waveforms that will give a sense of the overall loop stability without breaking the feedback loop.

APPLICATIONS INFORMATION

Placing a power MOSFET and load resistor directly across the output capacitor and driving the gate with an appropriate signal generator is a practical way to produce a realistic load step condition. The initial output voltage step resulting from the step change in output current may not be within the bandwidth of the feedback loop, so this is why it is better to look at the I_{TH} pin signal which is in the feedback loop and is the filtered and compensated control loop response.

The gain of the loop will be increased by increasing R_C and the bandwidth of the loop will be increased by decreasing C_C. If R_C is increased by the same factor that C_C is decreased, the zero frequency will be kept the same, thereby keeping the phase shift the same in the most critical frequency range of the feedback loop. The output voltage settling behavior is related to the stability of the closed-loop system and will demonstrate the actual overall supply performance.

A second, more severe transient is caused by switching in loads with large (>1µF) supply bypass capacitors. The discharged bypass capacitors are effectively put in parallel with C_{OUT}, causing a rapid drop in V_{OUT}. No regulator can alter its delivery of current quickly enough to prevent this sudden step change in output voltage if the load switch resistance is low and it is driven quickly. If the ratio of C_{LOAD} to C_{OUT} is greater than 1:50, the switch rise time should be controlled so that the load rise time is limited to approximately 25 • C_{LOAD}. Thus, a 10µF capacitor would require a 250µs rise time, limiting the charging current to about 200mA.

Boost Converter Design Example

As a design example, assume V_{IN} = 12V (nominal), V_{IN} = 22V (max), V_{OUT} = 24V, $I_{OUT(MAX)}$ = 8A, $V_{SENSE(MAX)}$ = 95mV, and f = 350kHz.

The components are designed based on single channel operation. The inductance value is chosen first based on a 30% ripple current assumption. Tie the FREQ pin to GND, generating 350kHz operation. The minimum inductance for 30% ripple current is:

The largest ripple happens when V_{IN} = 1/2V_{OUT} = 12V, where the average maximum inductor current for each channel is:

$$I_{MAX} = \left(\frac{I_{OUT(MAX)}}{2}\right) \bullet \left(\frac{V_{OUT}}{V_{IN}}\right) = 8A$$

A 6.8µH inductor will produce a 31% ripple current. The peak inductor current will be the maximum DC value plus one half the ripple current, or 9.25A.

The R_{SENSE} resistor value can be calculated by using the maximum current sense voltage specification with some accommodation for tolerances:

$$R_{SENSE} \le \frac{75mV}{9.25A} = 0.008\Omega$$

Choosing 1% resistors: R_A = 24.9k and R_B = 475k yields an output voltage of 24.092V.

The power dissipation on the top side MOSFET in each channel can be easily estimated. Choosing a Vishay Si7848BDP MOSFET results in: $R_{DS(ON)}$ = 0.012Ω, C_{MILLER} = 150pF. At maximum input voltage with T (estimated) = 50°C:

$$P_{MAIN} = \frac{(24V - 12V)\,24V}{(12V)^2} \bullet (4A)^2 \bullet \left[1 + (0.005)(50°C - 25°C)\right] \bullet 0.008\Omega + (1.7)(24V)^3 \frac{4A}{12V}(150pF)(350kHz) = 0.7W$$

C_{OUT} is chosen to filter the square current in the output. The maximum output current peak is:

$$I_{OUT(PEAK)} = 8 \bullet \left(1 + \frac{31\%}{2}\right) = 9.3A$$

A low ESR (5mΩ) capacitor is suggested. This capacitor will limit output voltage ripple to 46.5mV (assuming ESR dominate ripple).

APPLICATIONS INFORMATION

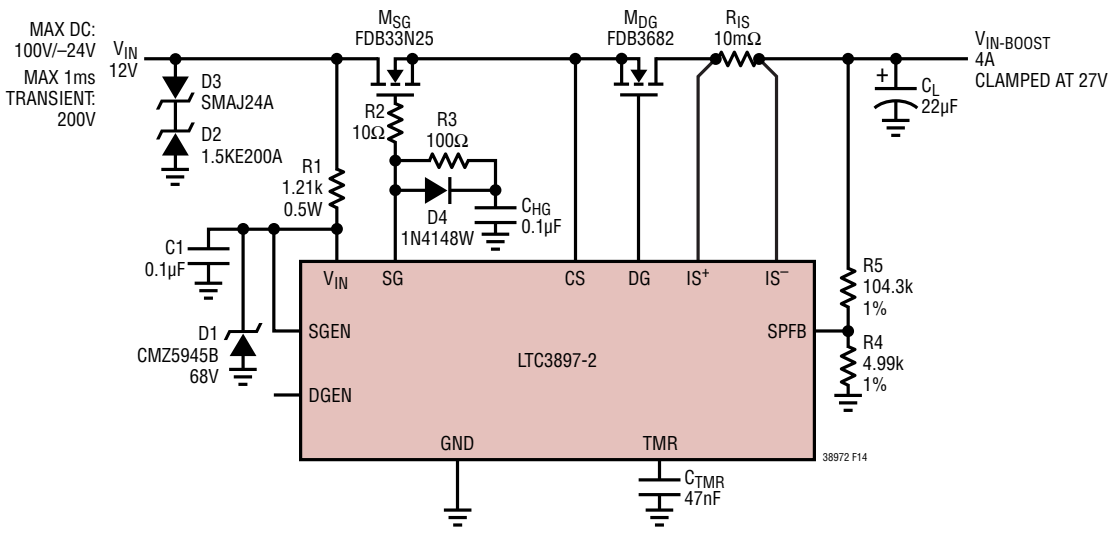


Figure 14. 4A, 12V Overvoltage and Reverse Current Protection

Surge Stopper and Ideal Diode Design Example

As a design example, consider an application with the following specifications: V_{IN} = 6V to 14V DC with a peak transient of 200V and decay time constant τ of 1ms, input to the boost controller $V_{IN-BOOST} \leq 27V$, minimum current limit $I_{LIM(MIN)}$ at 4A, and 1ms of overvoltage early warning (Figure 14).

Selection of CMZ5945B for D1 will limit the voltage at the V_{IN} pin to less than 71V during the 200V surge. The minimum required voltage at the V_{IN} pin is 4.2V when input supply is at 6V; the supply current for LTC3897-2 is 1.3mA. The maximum value for R1 to ensure proper operation is:

$$R1 = \frac{6V - 4.2V}{1.3mA} = 1.4k$$

Select 1.21k for R1 to accommodate all conditions. With the minimum Zener voltage at 64V, the peak current through R1 into D1 is then calculated as:

$$I_{D1(PK)} = \frac{200V - 64V}{1.1k} = 124mA$$

which can be handled by the CMZ5945B with a peak power rating of 200W at 10/1000µs.

With a bypass capacitance of 0.1µF (C1), along with R1 of 1.21k, high voltage transients up to 250V with a pulse width less than 10µs are filtered out at the V_{IN} pin.

Next, calculate the resistive divider value to limit $V_{IN-BOOST}$ to 27V during an overvoltage event:

$$V_{REG} = \frac{1.235V \bullet (R4 + R5)}{R4} = 27V$$

Choosing 250µA for the resistive divider:

$$R4 = \frac{1.235V}{250\mu A} = 5k$$

Select 4.99k for R4.

$$R5 = \frac{(27V - 1.235V) \bullet R4}{1.235V} = 104.3k$$

The closest standard value for R5 is 105k. Now, calculate the sense resistor, R_{IS}, value:

$$R_{IS} = \frac{\Delta V_{IS(MIN)}}{I_{LIM}} = \frac{45mV}{4A} = 11m\Omega$$

Choose 10mΩ for R_{IS}.

APPLICATIONS INFORMATION

C_{TMR} is then chosen for 1ms between when the TMR pin reaches 1.25V and M_{SG} turns off:

$$C_{TMR} = \frac{1ms \bullet 5\mu A}{100mV} = 50nF$$

The closest standard value for C_{TMR} is 47nF. Note that if the boost controller is enabled,the value of C_{TMR} should be small, such as 1nF, to limit the large current during an output overcurrent event.

The pass device, M_{SG}, should be chosen to withstand an output overcurrent condition with V_{IN} = 14V. In the case of a severe output overcurrent event where $V_{IN-BOOST}$ = 0V, $I_{TMR(UP)}$ = 57µA and the total overcurrent fault time is:

$$t_{OC} = \frac{C_{TMR} \bullet V_{TMR(G)}}{I_{TMR(UP)}} = \frac{47nF \bullet 1.35V}{57\mu A} = 1.11mst$$

The maximum power dissipation in M_{SG} is:

$$P = \frac{\Delta V_{DS(M1)} \bullet \Delta V_{IS(MAX)}}{R_{IS}} = \frac{14V \bullet 33mV}{10m\Omega} = 46.2W$$

The corresponding P^2t is $2.7W^2s$.

During an output overload or soft short, the voltage at the IS^- pin could stay at 2V or higher. The total overcurrent fault time when $V_{IN-BOOST}$ = 2V is:

$$t_{OC} = \frac{47nF \bullet 1.35V}{47\mu A} = 1.35ms$$

The maximum power dissipation in M_{SG} is:

$$P = \frac{(14V - 2V) \bullet 55mV}{10m\Omega} = 66W$$

The corresponding P^2t is $5.9W^2s$. Both of the above conditions are well within the safe operating area of FDB33N25.

To select the pass device, M_{DG}, first calculate $R_{DS(ON)}$ to achieve the desired forward drop V_{FW} at maximum load current (5.5A). If V_{FW} = 0.25V:

$$R_{DS(ON)} \leq \frac{V_{FW}}{I_{LOAD(MAX)}} = \frac{0.25V}{5.5A} = 45.5m\Omega$$

The FDB3682 offers a maximum $R_{DS(ON)}$ of 36mΩ at V_{GS} = 10V so is a good fit. Its minimum BV_{DSS} of 100V is also sufficient to handle $V_{IN-BOOST}$ transients up to 100V during an input short-circuit event.

PC Board Layout Checklist

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the IC. Figure 15 illustrates the current waveforms present in the various branches of the 2-phase synchronous regulators operating in the continuous mode. Check the following in your layout:

1. Put the bottom N-channel MOSFETs MBOT1 and MBOT2 and the top N-channel MOSFETs MTOP1 and MTOP2 in one compact area with C_{OUT}.
2. Are the signal and power grounds kept separate? The combined IC signal ground pin and the ground return of C_{IN} must return to the combined C_{OUT} (–) terminals. The path formed by the bottom N-channel MOSFET and the capacitor should have short leads and PC trace lengths. The output capacitor (–) terminals should be connected as close as possible to the source terminals of the bottom MOSFETs.
3. Does the LTC3897-2 V_{FB} pin's resistive divider connect to the (+) terminal of C_{OUT}? The resistive divider must be connected between the (+) terminal of C_{OUT} and signal ground and placed close to the V_{FB} pin. The feedback resistor connections should not be along the high current input feeds from the input capacitor(s).
4. Are the $SENSE^+$ and $SENSE^-$ leads routed together with minimum PC trace spacing? The filter capacitor between $SENSE^+$ and $SENSE^-$ should be as close as possible to the IC. Ensure accurate current sensing with Kelvin connections at the sense resistor.
5. Is the DRV_{CC} and decoupling capacitor connected close to the IC, between the DRV_{CC} and the ground pin? This capacitor carries the MOSFET drivers' current peaks.

APPLICATIONS INFORMATION

6. Keep the switching nodes (SW1, SW2), top gate (TG1, TG2) and boost nodes (BOOST1, BOOST2) away from sensitive small-signal nodes, especially from the opposites channel's voltage and current sensing feedback pins. All of these nodes have very large and fast moving signals and, therefore, should be kept on the output side of the LTC3897-2 and occupy a minimal PC trace area.

7. Use a modified "star ground" technique: a low impedance, large copper area central grounding point on the same side of the PC board as the input and output capacitors with tie-ins for the bottom of the DRV_{CC} decoupling capacitor, the bottom of the voltage feedback resistive divider and the GND pin of the IC.

8. To achieve accurate current sensing for the IS^+ and IS^- pins, use Kelvin connections to the current sense resistor. Limit the resistance from the CS pin to the sources of the MOSFETs to below 10Ω. The minimum trace width for 1oz copper foil is 0.02" per amp to ensure the trace stays at a reasonable temperature. Note that 1oz copper exhibits a sheet resistance of about 530μΩ/square. Small resistances can cause large errors in high current applications. Noise immunity will be improved significantly by locating resistive dividers close to the pins with short V_{IN} and GND traces.

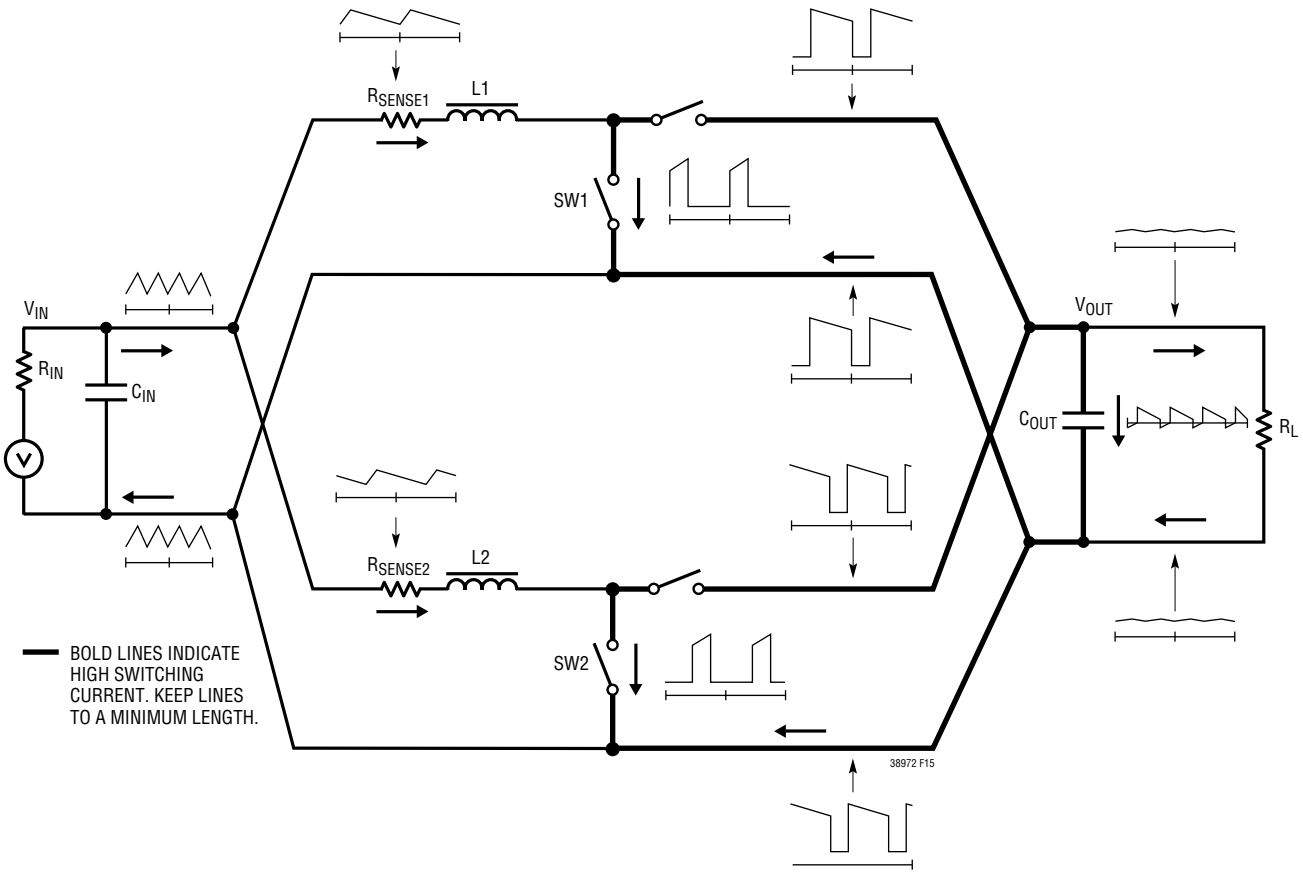


Figure 15. BOOST Converter Branch Current Waveforms

APPLICATIONS INFORMATION

PC Board Layout Debugging

Start with one controller on at a time. It is helpful to use a DC-50MHz current probe to monitor the current in the inductor while testing the circuit. Monitor the output switching node (SW pin) to synchronize the oscilloscope to the internal oscillator and probe the actual output voltage. Check for proper performance over the operating voltage and current range expected in the application. The frequency of operation should be maintained over the input voltage range down to dropout and until the output load drops below the low current operation threshold—typically 10% of the maximum designed current level in Burst Mode operation.

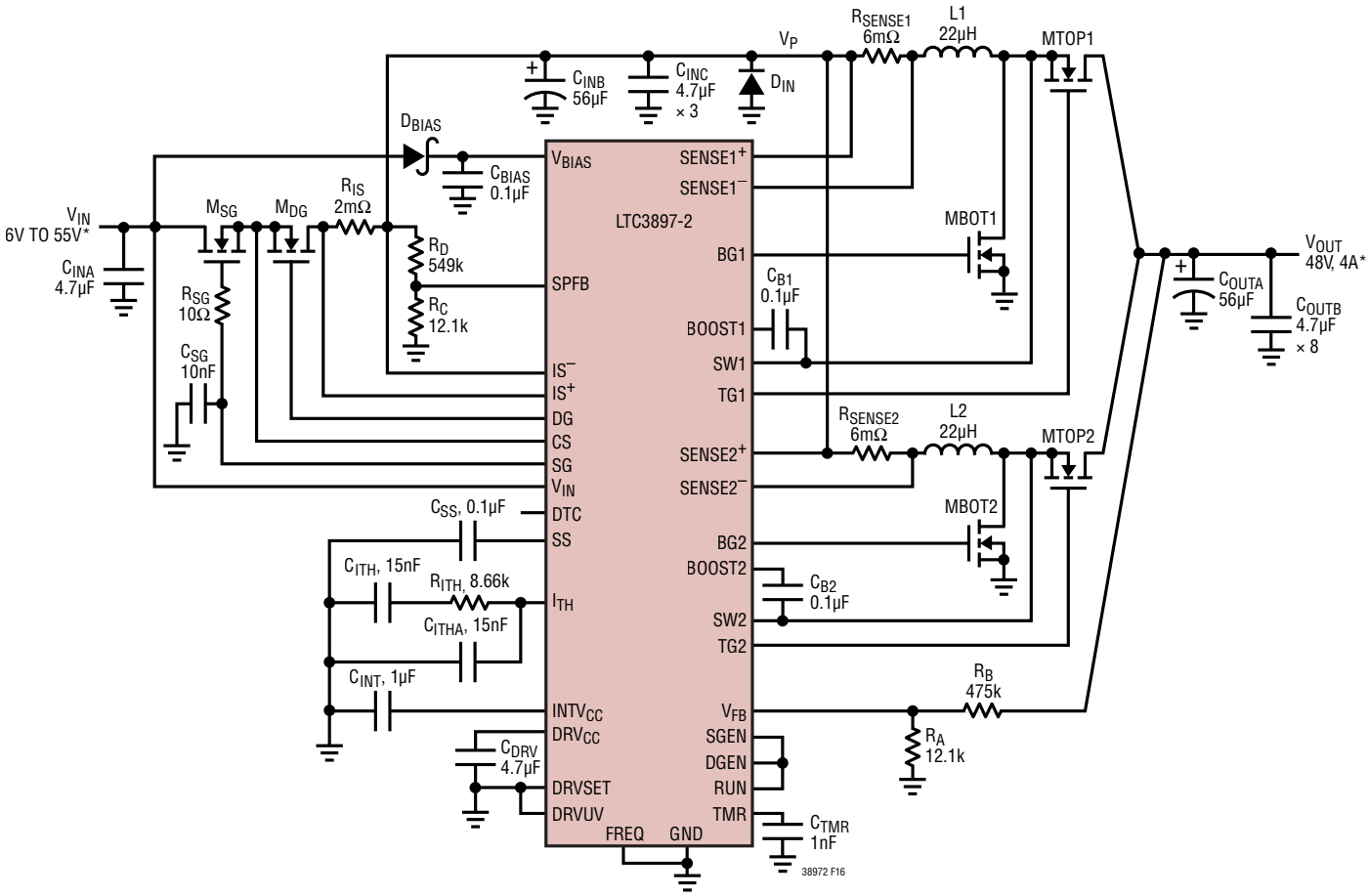
The duty cycle percentage should be maintained from cycle to cycle in a well designed, low noise PCB implementation. Variation in the duty cycle at a subharmonic rate can suggest noise pickup at the current or voltage sensing inputs or inadequate loop compensation. Overcompensation of the loop can be used to tame a poor PC layout if regulator bandwidth optimization is not required. Only after each controller is checked for its individual performance should both controllers be turned on at the same time. A particularly difficult region of operation is when one controller channel is nearing its current comparator trip point while the other channel is turning on its bottom MOSFET. This occurs around the 50% duty cycle on either channel due to the phasing of the internal clocks and may cause minor duty cycle jitter.

Reduce V_{IN} from its nominal level to verify operation with high duty cycle. Check the operation of the undervoltage lockout circuit by further lowering V_{IN} while monitoring the outputs to verify operation.

Investigate whether any problems exist only at higher output currents or only at higher input voltages. If problems coincide with high input voltages and low output currents, look for capacitive coupling between the BOOST, SW, TG, and possibly BG connections and the sensitive voltage and current pins. The capacitor placed across the current sensing pins needs to be placed immediately adjacent to the pins of the IC. This capacitor helps to minimize the effects of differential noise injection due to high frequency capacitive coupling.

An embarrassing problem which can be missed in an otherwise properly working switching regulator, results when the current sensing leads are hooked up backwards. The output voltage under this improper hook-up will still be maintained, but the advantages of current mode control will not be realized. Compensation of the voltage loop will be much more sensitive to component selection. This behavior can be investigated by temporarily shorting out the current sensing resistor—don't worry, the regulator will still maintain control of the output voltage.

APPLICATIONS INFORMATION



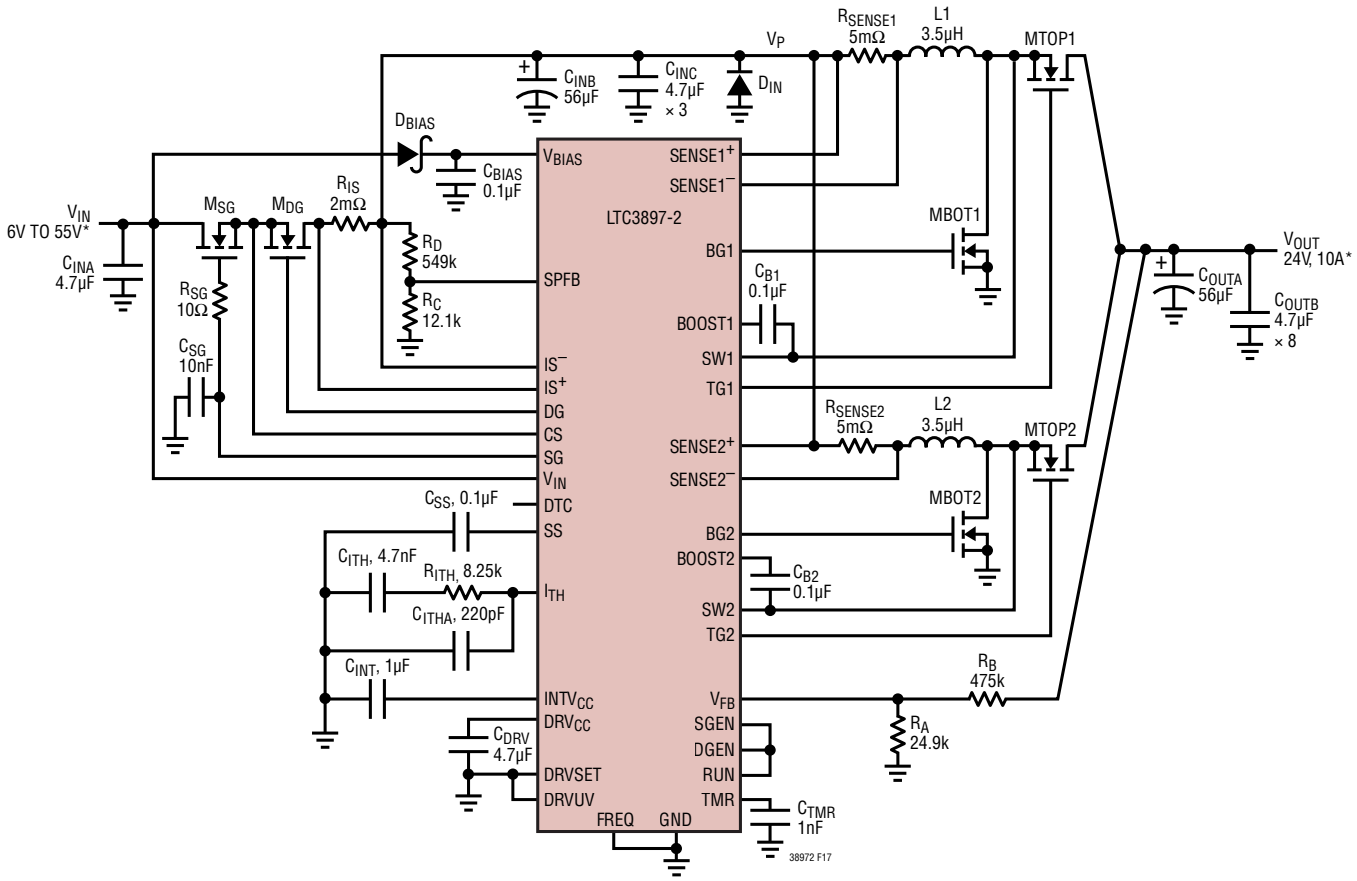
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MDG: INFINEON BSC035N10NS
MBOT1, MBOT2, MTOP1, MTOP2: INFINEON BSC028N06NS
L1, L2: WURTH 7443632200
DIN: VISHAY ES1B-E3
DBIAS: DIODES INC DFLS1150-7
COUTA, CINB: PANASONIC EEHZA1J560P
COUTB, CINA, CINC: TDK C3225X7S2A475M
CBIAS: AVX 06035C104KAT2A

PINS NOT SHOWN IN THIS CIRCUIT:
PLLIN/MODE, ILIM, PHASMD, CLKOUT, EXTVCC

*WHEN VIN < 8V, MAXIMUM LOAD CURRENT AVAILABLE IS REDUCED. VIN OPERATES THROUGH TRANSIENTS UP TO 75V. WHEN VIN > 48V, VOUT FOLLOWS VIN UP TO 57V.

Figure 16. High Efficiency 2-Phase 48V Boost Converter with In-Rush Current Control, Overcurrent Protection, Input Voltage Surge Protection and Reverse Input Protection

APPLICATIONS INFORMATION



MSG: INFINEON IPB020N10N5
MDG: INFINEON BSC035N10NS
MBOT1, MBOT2, MTOP1, MTOP2: INFINEON BSC028N06NS
L1, L2: WURTH 7443556350
DIN: VISHAY ES1B-E3
DBIAS: DIODES INC DFLS1150-7
COUTA, CINB: PANASONIC EEHZA1J560P
COUTB, CINA, CINC: TDK C3225X7S2A475M
CBIAS: AVX 06035C104KAT2A

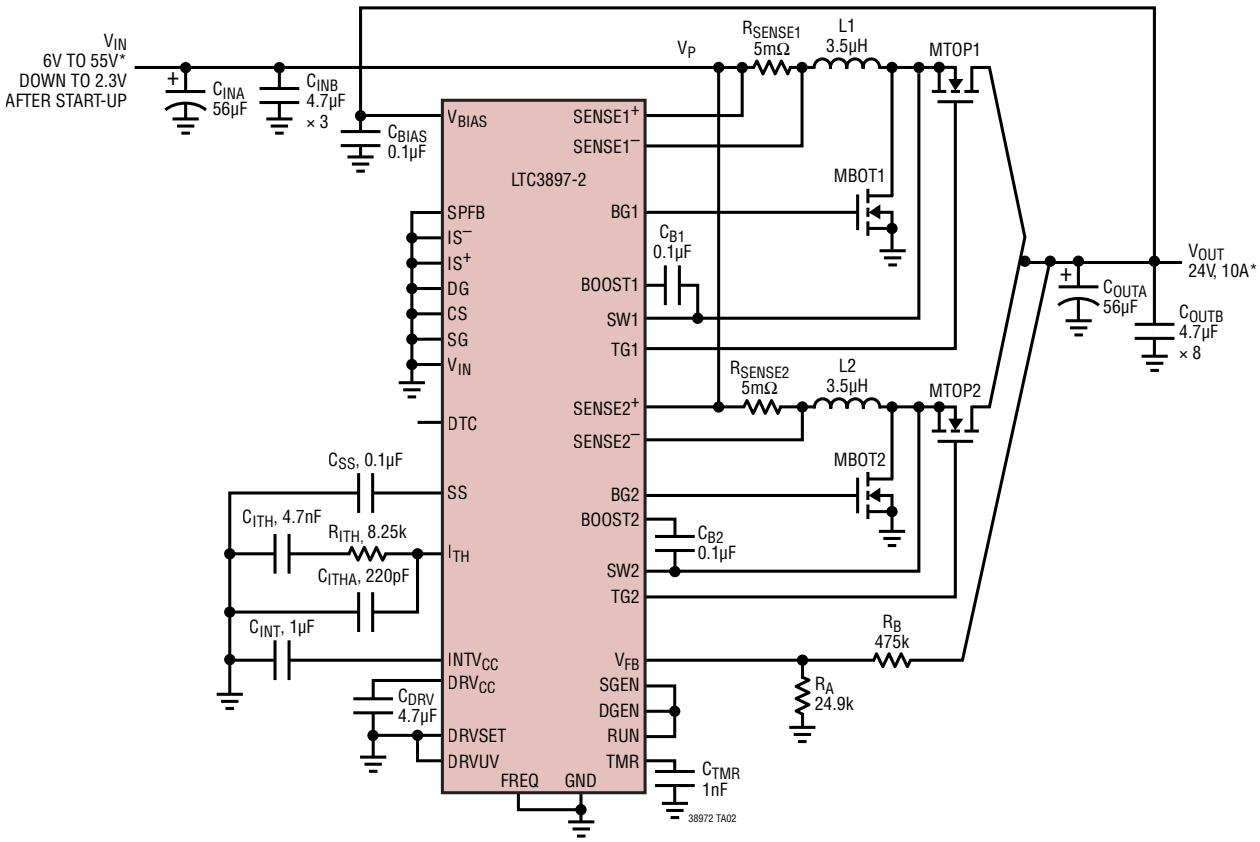
PINS NOT SHOWN IN THIS CIRCUIT:
PLLIN/MODE, I_{LIM}, PHASMD, CLKOUT, $EXTV_{CC}$

*WHEN V_{IN} < 8V, MAXIMUM LOAD CURRENT AVAILABLE IS REDUCED. V_{IN} OPERATES THROUGH TRANSIENTS UP TO 75V. WHEN V_{IN} > 24V, V_{OUT} FOLLOWS V_{IN} UP TO 57V.

Figure 17. High Efficiency 2-Phase 24V Boost Converter with In-Rush Current Control, Overcurrent Protection, Input Voltage Surge Protection and Reverse Input Protection

TYPICAL APPLICATIONS

High Efficiency 2-Phase 24V Boost Converter
(Input Supply Down to 2.3V After Start Up)



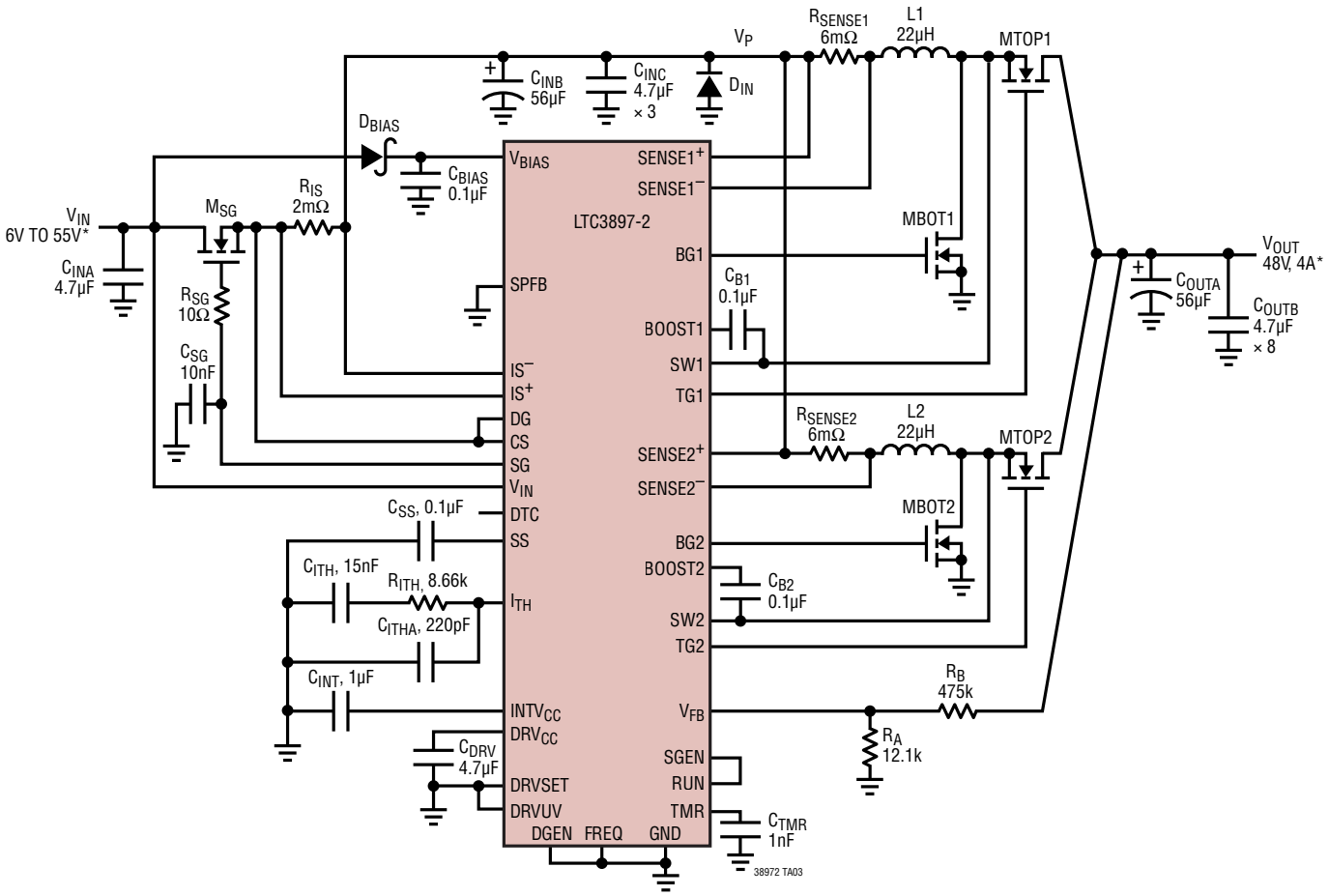
MBOT1, MBOT2, MTOP1, MTOP2: INFINEON BSC028N06NS
L1, L2: WURTH 7443556350
C_{OUTA}, C_{INA}: PANASONIC EEHZA1J560P
C_{OUTB}, C_{INB}: TDK C3225X7S2A475M
C_{BIAS}: AVX 06035C104KAT2A

PINS NOT SHOWN IN THIS CIRCUIT:
PLLIN/MODE, I_{LIM}, PHASMD, CLKOUT, $EXTV_{CC}$

*WHEN V_{IN} < 8V, MAXIMUM LOAD CURRENT AVAILABLE IS REDUCED.
WHEN V_{IN} > 24V, V_{OUT} FOLLOWS V_{IN} UP TO 55V.

TYPICAL APPLICATIONS

High Efficiency 2-Phase 48V Boost Converter with In-Rush Current Control, Input Voltage Surge Protection and Overcurrent Protection (Ideal Diode Controller Not Used)



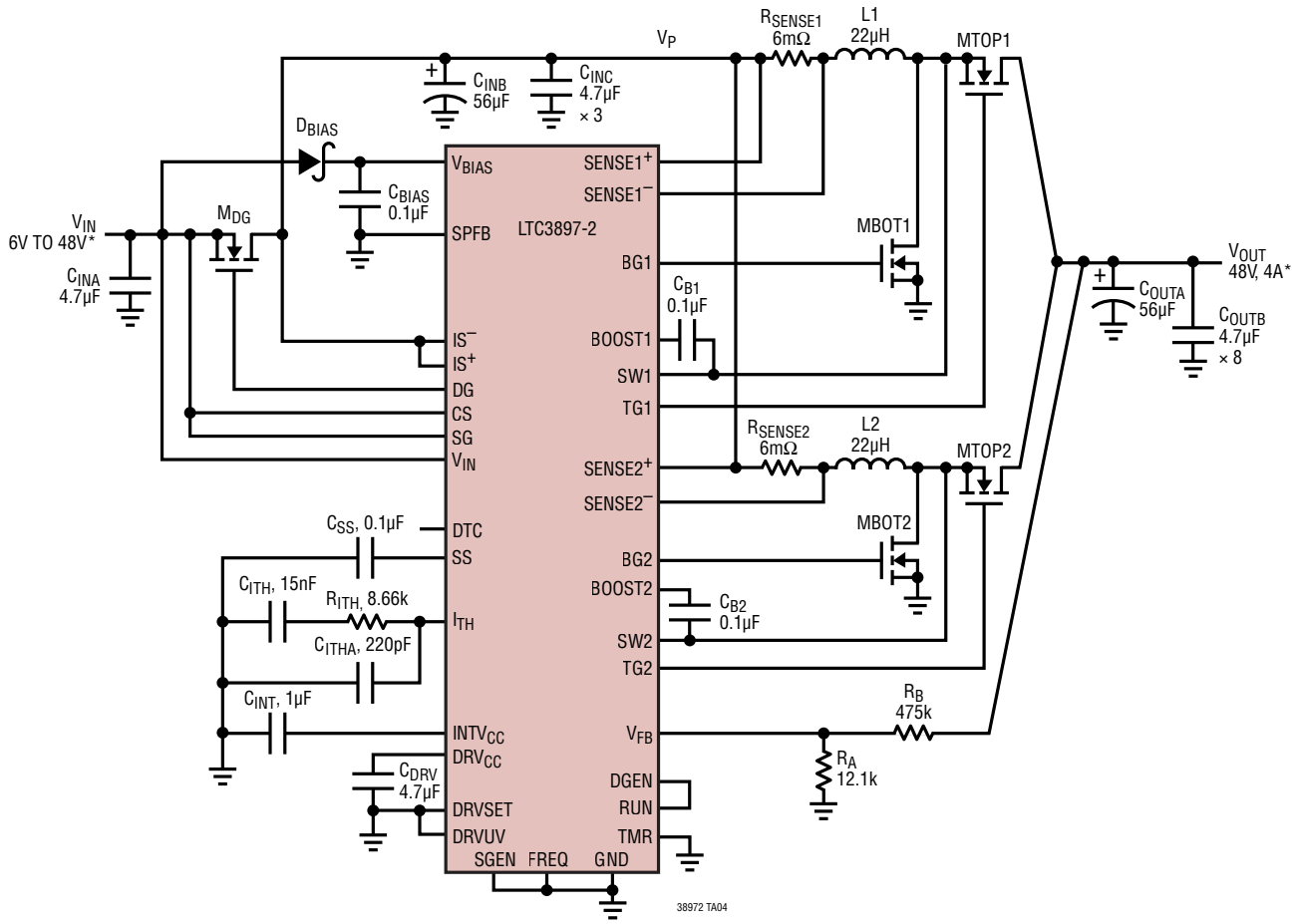
M_{SG}: INFINEON IPB020N10N5
MBOT1, MBOT2, MTOP1, MTOP2: INFINEON BSC028N06NS
L1, L2: WURTH 7443632200
D_{IN}: VISHAY ES1B-E3
D_{BIAS}: DIODES INC DFLS1150-7
C_{OUTA}, C_{INB}: PANASONIC EEHZA1J560P
C_{OUTB}, C_{INA}, C_{INC}: TDK C3225X7S2A475M
C_{BIAS}: AVX 06035C104KAT2A

PINS NOT SHOWN IN THIS CIRCUIT:
PLLIN/MODE, I_{LIM}, PHASMD, CLKOUT, $EXTV_{CC}$

*WHEN V_{IN} < 8V, MAXIMUM LOAD CURRENT AVAILABLE IS REDUCED. V_{IN} OPERATES THROUGH TRANSIENTS UP TO 75V. WHEN V_{IN} > 48V, V_{OUT} FOLLOWS V_{IN} UP TO 57V.

TYPICAL APPLICATIONS

High Efficiency 2-Phase 48V Boost Converter with Reverse Input Protection (Surge Stopper Controller Not Used)



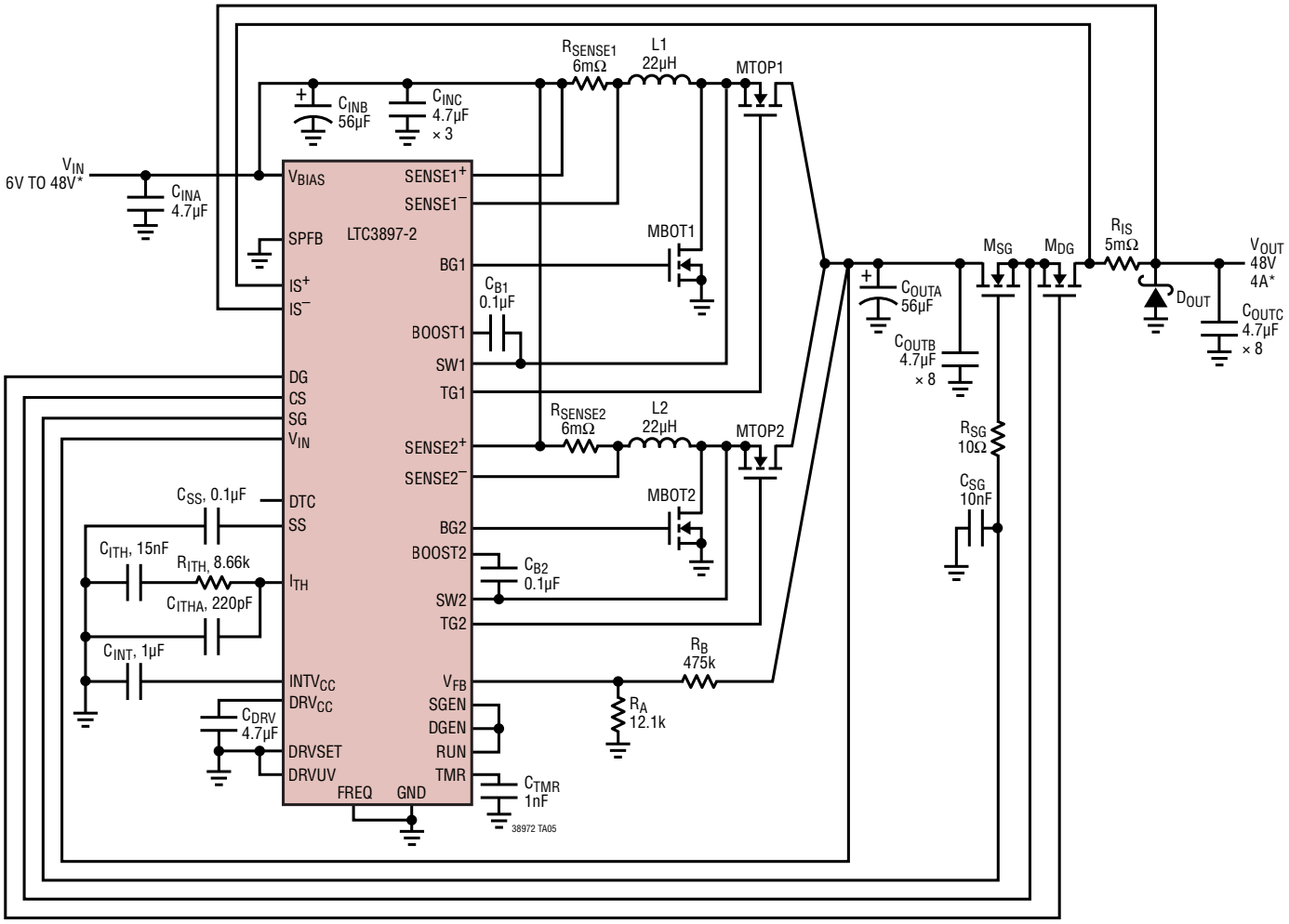
M_{DG}: INFINEON BSC035N10NS
MBOT1, MBOT2, MTOP1, MTOP2: INFINEON BSC028N06NS
L1, L2: WURTH 7443632200
D_{BIAS}: DIODES INC DFLS1150-7
C_{OUTA}, C_{INB}: PANASONIC EEHZA1J560P
C_{OUTB}, C_{INA}, C_{INC}: TDK C3225X7S2A475M
C_{BIAS}: AVX 06035C104KAT2A

PINS NOT SHOWN IN THIS CIRCUIT:
PLLIN/MODE, I_{LIM}, PHASMD, CLKOUT, $EXTV_{CC}$

*WHEN V_{IN} < 8V, MAXIMUM LOAD CURRENT AVAILABLE IS REDUCED.

TYPICAL APPLICATIONS

High Efficiency 2-Phase 48V Boost Converter with Overcurrent Protection (Ideal Diode and Surge Stopper Controllers at the Output)



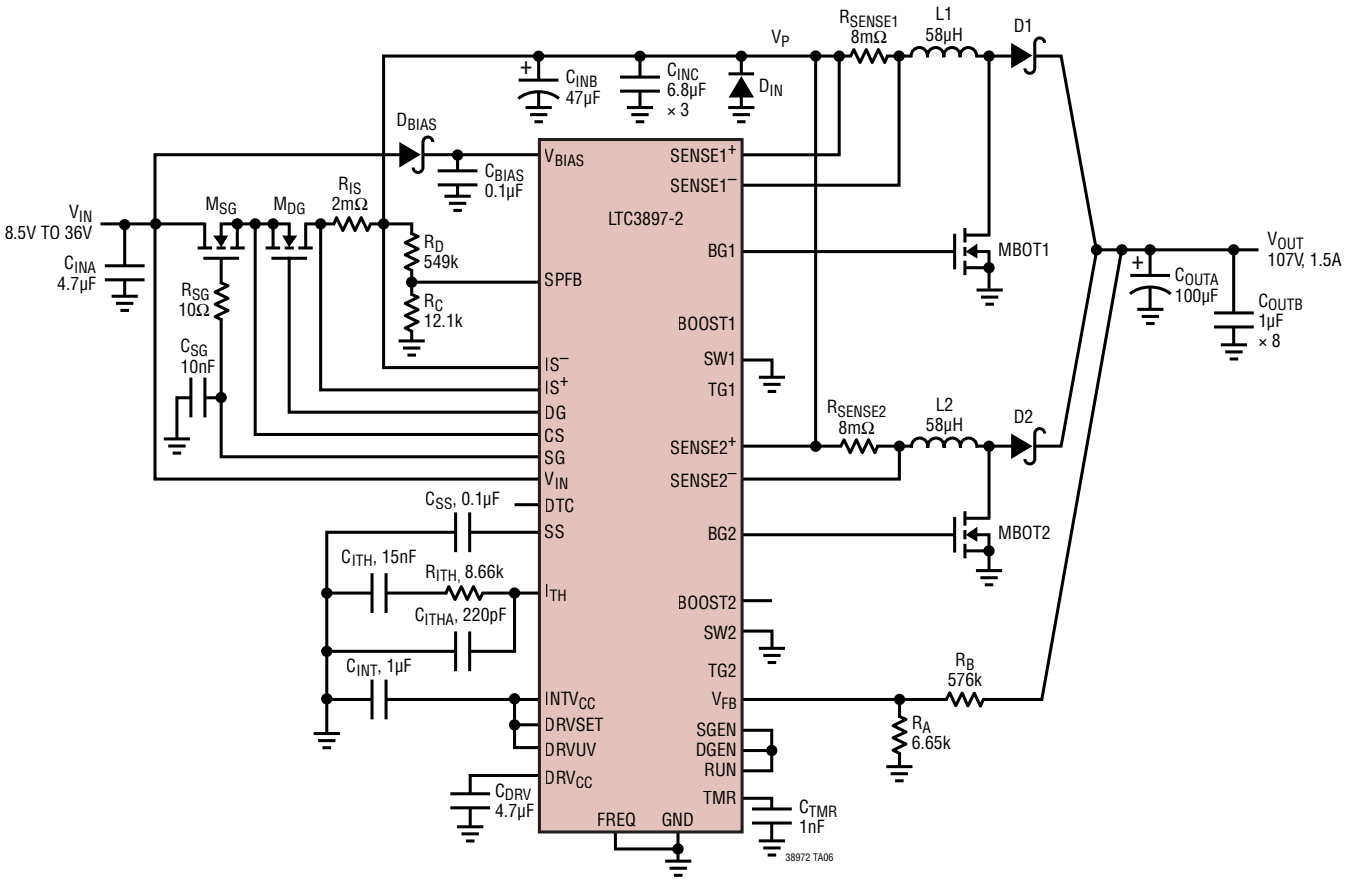
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MBOT1, MBOT2, MTOP1, MTOP2: INFINEON BSC028N06NS
L1, L2: WURTH 7443632200
DOUT: VISHAY ES1B-E3
DBIAS: DIODES INC DFLS1150-7
COUTA, CINB: PANASONIC EEHZA1J560P
COUTB, COUTC, CINA, CINC: TDK C3225X7S2A475M
CBIAS: AVX 06035C104KAT2A

PINS NOT SHOWN IN THIS CIRCUIT:
PLLIN/MODE, ILIM, PHASMD, CLKOUT, EXTVCC

*WHEN VIN < 8V, MAXIMUM LOAD CURRENT AVAILABLE IS REDUCED.

TYPICAL APPLICATIONS

Nonsynchronous 107V/1.5A 2-Phase Boost Converter with In-Rush Current Control, Overcurrent Protection, Input Voltage Surge Protection and Reverse Input Protection

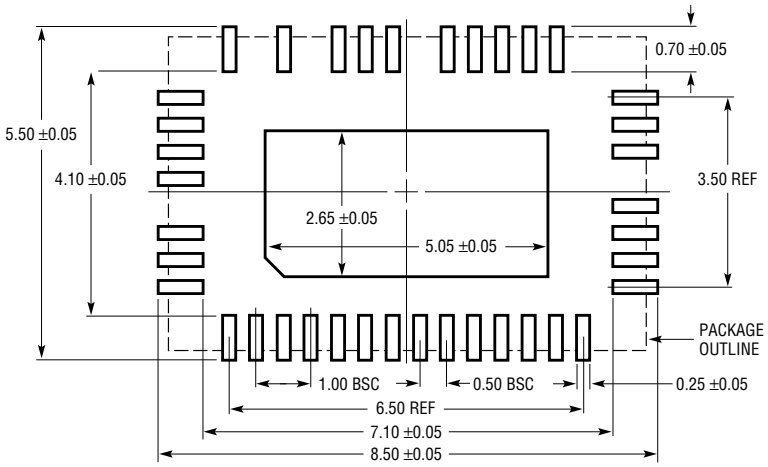


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MDG: INFINEON BSC035N10NS
MBOT1, MBOT2,: INFINEON BSC360N15NS
L1, L2: PULSE PA2050-583
D1, D2: DIODES INC PDS4150
DIN: VISHAY ES1B-E3
DBIAS: DIODES INC DFLS1150-7
COUTA: PANASONIC EEV-EB2D101M
COUTB: TDK C5750X7R2E105K230KM
CINB: SUNCON 63CE47LX
COUTB, CINA: TDK C3225X7S2A475M
CINC: TDK C4532X7R1H685K
CBIAS: AVX 06035C104KAT2A

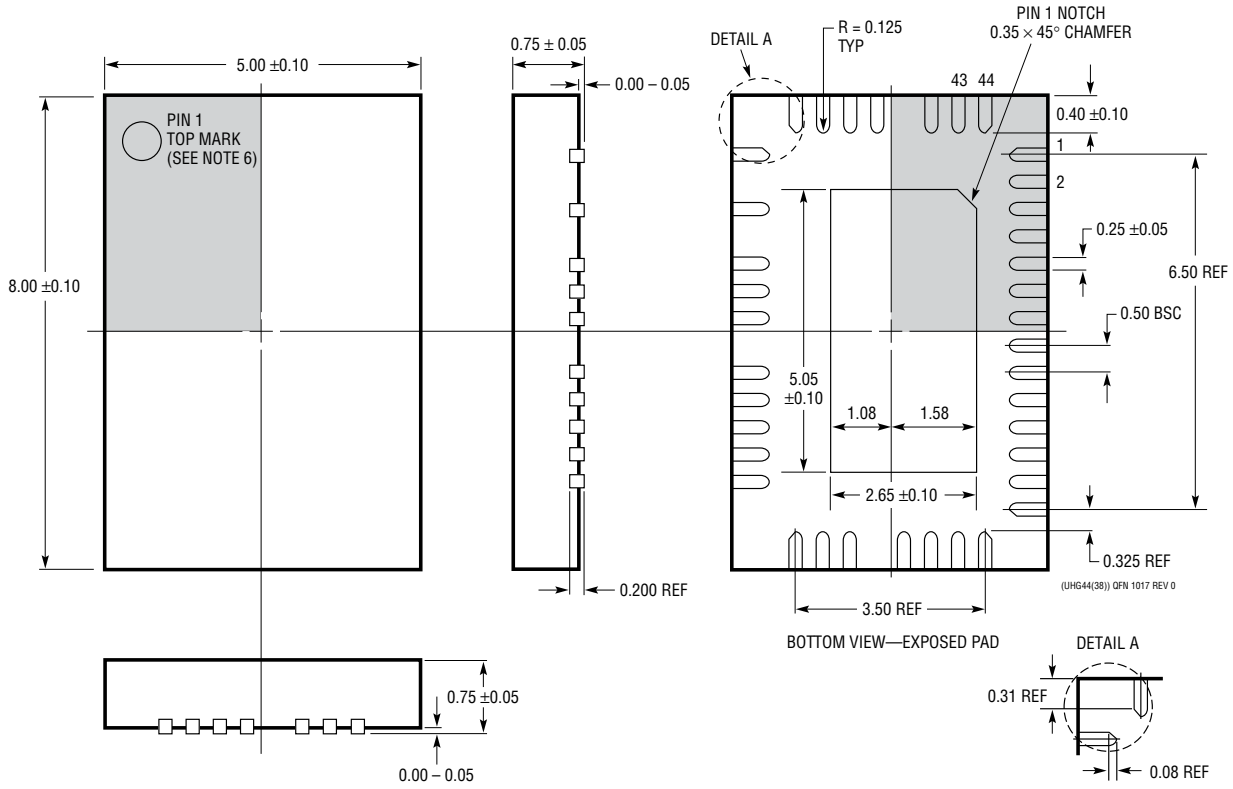
PINS NOT SHOWN IN THIS CIRCUIT:
PLLIN/MODE, ILIM, PHASMD, CLKOUT, EXTVCC

PACKAGE DESCRIPTION

UHG Package
44(38)-Lead Plastic QFN (5mm × 8mm)
(Reference LTC DWG # 05-08-1616 Rev Ø)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



NOTE:
1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

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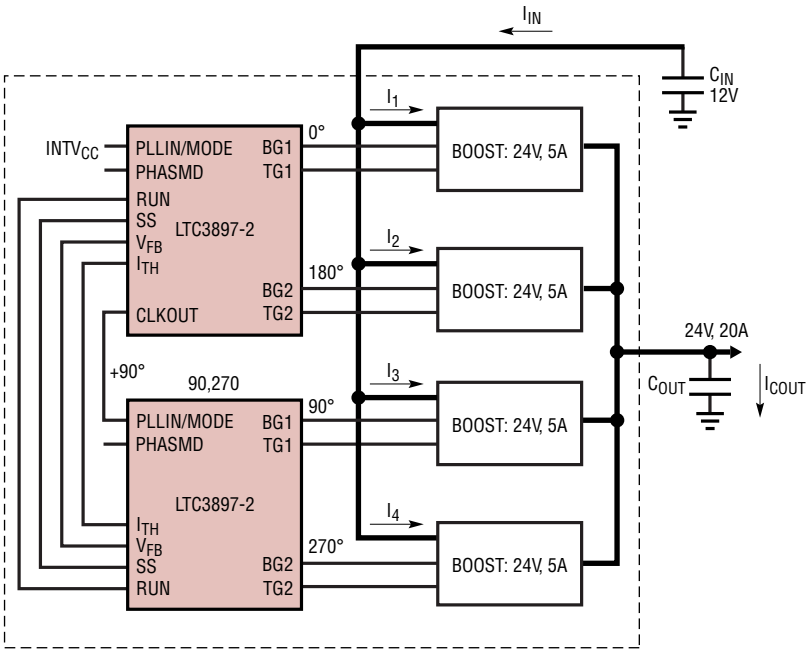
REVISION HISTORY

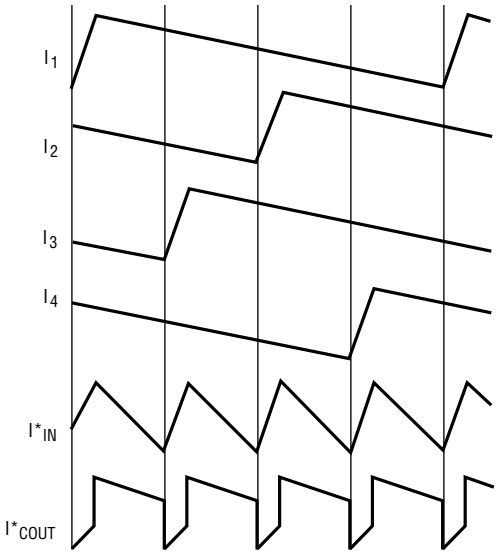
REV	DATE	DESCRIPTION	PAGE NUMBER
A	01/20	Minor typo corrections	13, 14, 18, 32, 37

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TYPICAL APPLICATION

4-Phase 480W Single Output Boost Regulator





* RIPPLE CURRENT CANCELLATION INCREASES THE RIPPLE FREQUENCY AND REDUCES THE RMS INPUT/OUTPUT RIPPLE CURRENT, THUS SAVING INPUT/OUTPUT CAPACITORS

38972 TA07

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC3897	PolyPhase Synchronous Boost Controller with Input/Output Protection in Smaller Packages	4.5V ≤ V_{IN} ≤ 65V, 75V Peak, V_{OUT} Up to 60V, PLL Fixed Frequency 75kHz to 550kHz, I_Q = 55µA, TSSOP-38, 5mm × 7mm QFN-38
LTC3784	Low I_Q, Multiphase, Dual Channel Single Output Synchronous Step-Up DC/DC Controller	4.5V (Down to 2.5V after Start-Up) ≤ V_{IN} ≤ 60V, V_{OUT} Up to 60V, PLL Fixed Frequency 50kHz to 900kHz, I_Q = 28µA
LTC3769	Low I_Q Synchronous Step-Up DC/DC Controller	4.5V (Down to 2.5V After Start-Up) ≤ V_{IN} ≤ 60V, V_{OUT} Up to 60V, I_Q = 28µA, PLL Fixed Frequency 50kHz to 900kHz, 4mm x 4mm QFN-24, TSSOP-20E
LTC3899	Low I_Q, Triple Output, Buck/Buck/Boost Synchronous Controller	4.5V (Down to 2.5V After Start-Up) ≤ V_{IN} ≤ 60V, Buck and Boost V_{OUT} Up to 60V, I_Q = 29µA, PLL Fixed Frequency 50kHz to 900kHz, 5mm x 7mm QFN-38, TSSOP-38E
LTC4364	Surge Stopper with Ideal Diode	4V to 80V Operation, –40V Reverse Input, –20V Reverse Output
LTC4359	Ideal Diode Controller with Reverse Input Protection	4V to 80V Operation, –40V Input Protection, 150µA I_Q
LTC4366	Floating Surge Stopper	9V to > 500V Operation, 8-Pin TSOT and 3mm × 2mm DFN Packages
LTC3862/ LTC3862-1/ LTC3862-2	Multiphase Current Mode Step-Up DC/DC Controller	2.5V ≤ V_{IN} ≤ 32V, 5V or 10V Gate Drive, 75kHz to 500kHz, TSSOP-24, SSOP-24, 5mm × 5mm QFN-24
LTC3788/ LTC3788-1	Multiphase Dual Output Synchronous Step-Up Controller	4.5V (Down to 2.5V After Start-Up) ≤ V_{IN} ≤ 38V, V_{OUT} Up to 60V, 50kHz to 900kHz Fixed Operating Frequency, 5mm × 5mm QFN-32, SSOP-28
LTC3787	Multiphase, Single Output Dual Channel Synchronous Step-Up Controller	4.5 (Down to 2.5V After Start-Up) ≤ V_{IN} ≤ 38V, V_{OUT} Up to 60V, 50kHz to 900kHz Fixed Operating Frequency, 4mm × 4mm QFN-28, SSOP-28

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