150V Low I_Q, Synchronous Inverting DC/DC Controller

FEATURES

- **Wide V_{IN} + $|V_{OUT}^-|$ Range: 4V to 140V (150V Abs Max)**
- **Wide Output Voltage Range: –60V to –0.8V**
- **Ground-Referenced Control / Interface Pins**
- **Adjustable Gate Drive Level 5V to 10V (OPTI-DRIVE)**
- **Integrated Bootstrap Diode**
- **Low Operating I_Q: 40µA (Shutdown = 10µA)**
- Selectable Gate Drive UVLO Thresholds
- Onboard LDO or External NMOS LDO for DRV_{CC}
- $EXTV_{CC}$ LDO Powers Drivers from Output
- Phase-Lockable Frequency (75kHz to 850kHz)
- Programmable Fixed Frequency (50kHz to 900kHz)
- Selectable Continuous, Pulse-Skipping or Low Ripple Burst Mode® Operation at Light Loads
- Adjustable Burst Clamp and Current Limit
- Power Good Output Voltage Monitor
- Programmable Input Overvoltage Lockout
- 38-Lead TSSOP High Voltage Package

APPLICATIONS

- Automotive and Industrial Power Systems
- Telecommunications Power Supplies
- Distributed Power Systems

DESCRIPTION

The LTC®3896 is a high performance inverting DC/DC switching regulator controller that drives an all N-channel synchronous power MOSFET stage. It converts a wide-ranging positive input voltage source to a regulated negative output that can be as much as 60V below ground. The input can operate from a voltage as low as 4V and as high as 140V – $|V_{OUT}^-|$.

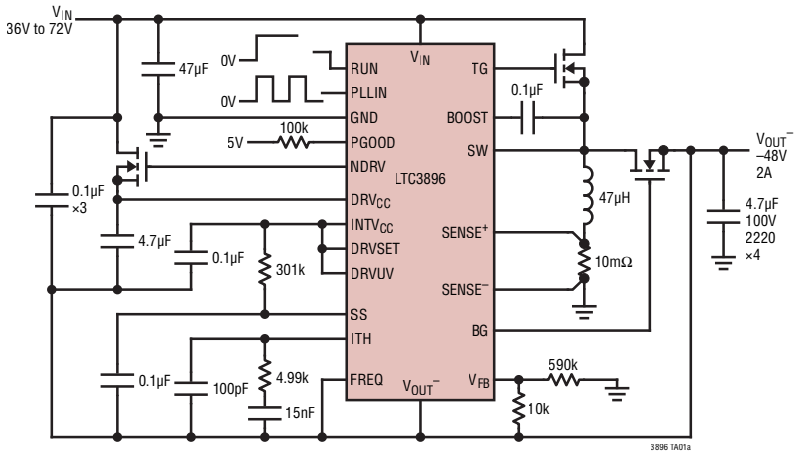
The LTC3896 contains true ground-referenced RUN, PLLIN and PGOOD pins, eliminating the need for external discrete level-shifting components to interface with the LTC3896.

A constant frequency current mode architecture allows a phase-lockable frequency of up to 850kHz. The low 40µA no-load quiescent current extends operating run time in battery-powered systems. OPTI-LOOP® compensation allows the transient response to be optimized over a wide range of output capacitance and ESR values. The LTC3896 features a precision 0.8V reference and power good output indicator. The soft-start (SS) pin ramps the output voltage during start-up.

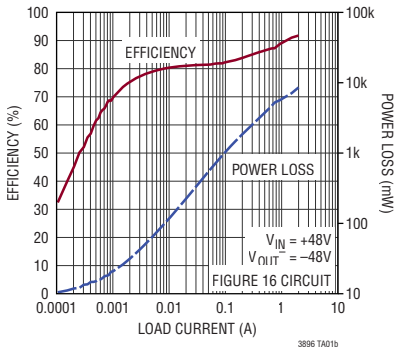
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TYPICAL APPLICATION

High Efficiency 36V–72V to –48V/2A Inverting Regulator



Efficiency and Power Loss vs Load Current

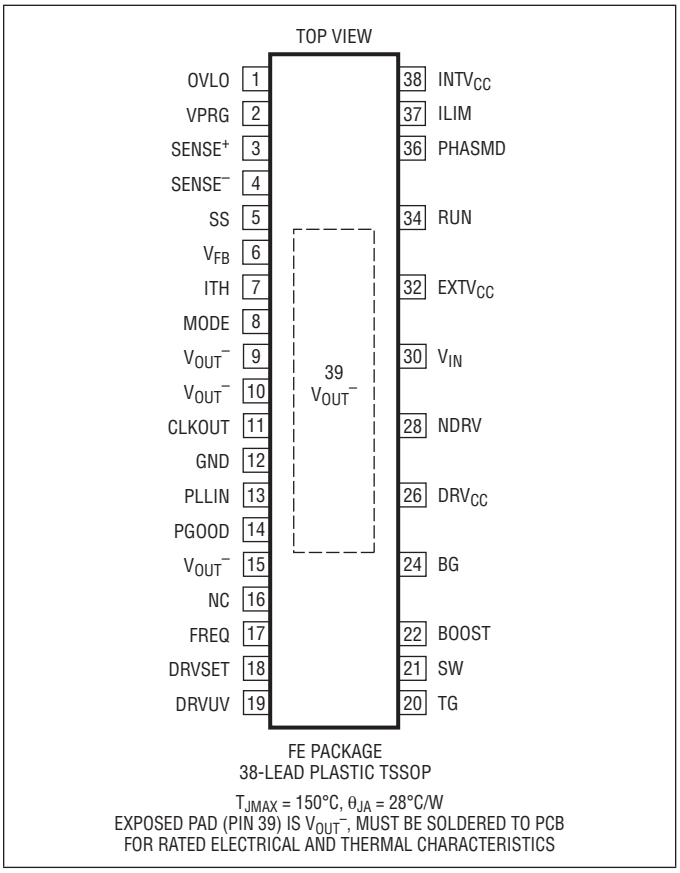


ABSOLUTE MAXIMUM RATINGS

All pins with respect to V_{OUT}^- unless otherwise noted (Note 1).

Input Supply Voltage (V_{IN}) ..... –0.3V to 150V
Top Side Driver Voltage BOOST ..... –0.3V to 150V
Switch Voltage (SW) ..... –5V to 150V
DRV_{CC}, (BOOST – SW) Voltages ..... –0.3V to 11V
BG, TG ..... (Note 8)
GND Voltage ..... –0.3V to 65V
RUN Voltage ..... (GND–0.3V) to 150V
(PLLIN – GND) Voltage ..... –0.3V to 6V
(PGOOD – GND) Voltage ..... –0.3V to 6V
$SENSE^+$, $SENSE^-$ Voltages ..... –0.3V to 65V
MODE, DRVUV Voltages ..... –0.3V to 6V
ILIM, VPRG, FREQ, PHASMD Voltages ..... –0.3V to 6V
DRVSET Voltage ..... –0.3V to 6V
NDRV ..... (Note 9)
$EXTV_{CC}$ Voltage ..... –0.3V to 14V
ITH, V_{FB} Voltages ..... –0.3V to 6V
SS, OVLO Voltages ..... –0.3V to 6V
Operating Junction Temperature Range (Notes 2, 3)
LTC3896E, LTC3896I ..... –40°C to 125°C
LTC3896H ..... –40°C to 150°C
Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



FE PACKAGE
38-LEAD PLASTIC TSSOP

T_{JMAX} = 150°C, θ_{JA} = 28°C/W
EXPOSED PAD (PIN 39) IS V_{OUT}^-, MUST BE SOLDERED TO PCB
FOR RATED ELECTRICAL AND THERMAL CHARACTERISTICS

ORDER INFORMATION

http://www.linear.com/product/LTC3896#orderinfo

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3896EFE#PBF	LTC3896EFE#TRPBF	LTC3896FE	38-Lead Plastic TSSOP	–40°C to 125°C
LTC3896IFE#PBF	LTC3896IFE#TRPBF	LTC3896FE	38-Lead Plastic TSSOP	–40°C to 125°C
LTC3896HFE#PBF	LTC3896HFE#TRPBF	LTC3896FE	38-Lead Plastic TSSOP	–40°C to 150°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Consult LTC Marketing for information on nonstandard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2), V_{IN} = 12V, V_{RUN} = 5V with respect to GND, $EXTV_{CC}$ = 0V, V_{DRVSET} = 0V, VPRG = FLOAT unless otherwise noted. All pin voltages with respect to V_{OUT}^-, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Input Supply Operating Voltage Range (V_{IN} + $\lvert V_{OUT}^- \rvert$)	(Note 10) DRVUV = V_{OUT}^-		4		140	V
V_{OUT}^-	Regulated Output Voltage Set Point	V_{IN} + $\lvert V_{OUT}^- \rvert \le 140V$		–60		–0.8	V
V_{FB}	Regulated Feedback Voltage	(Note 4); ITH Voltage = 1.2V					
		0°C to 85°C, VPRG = FLOAT		0.792	0.800	0.808	V
		VPRG = FLOAT	●	0.788	0.800	0.812	V
		VPRG = V_{OUT}^-	●	3.220	3.300	3.380	V
		VPRG = $INTV_{CC}$	●	4.875	5.000	5.125	V
I_{FB}	Feedback Current	(Note 4)					
		VPRG = FLOAT			–0.006	±0.050	µA
		VPRG = V_{OUT}^- or $INTV_{CC}$			4	6	µA
	Reference Voltage Line Regulation	(Note 4) V_{IN} = 4.5V to 150V			0.002	0.02	%/V
	Output Voltage Load Regulation	(Note 4) Measured in Servo Loop, ΔITH Voltage = 1.2V to 0.7V	●		0.01	0.1	%
		(Note 4) Measured in Servo Loop, ΔITH Voltage = 1.2V to 1.6V	●		–0.01	–0.1	%
g_m	Transconductance Amplifier g_m	(Note 4) ITH = 1.2V, Sink/Source 5µA			2.2		mmho
I_Q	Input DC Supply Current	(Note 5) V_{DRVSET} = V_{OUT}^-					
	Pulse-Skipping or Forced Continuous Mode	V_{FB} = 0.83V (No Load)			2.5		mA
	Sleep Mode	V_{FB} = 0.83V (No Load)			40	55	µA
	Shutdown	RUN = 0V with Respect to GND			10	20	µA
UVLO	Undervoltage Lockout	DRV_{CC} Ramping Up					
		DRVUV = V_{OUT}^-	●		4.0	4.2	V
		DRVUV = $INTV_{CC}$, DRVSET = $INTV_{CC}$	●		7.5	7.8	V
		DRV_{CC} Ramping Down					
		DRVUV = V_{OUT}^-	●	3.6	3.8	4.0	V
		DRVUV = $INTV_{CC}$, DRVSET = $INTV_{CC}$	●	6.4	6.7	7.0	V
V_{RUN} ON	RUN Pin ON Threshold	V_{RUN} Rising with Respect to GND	●	1.1	1.2	1.3	V
V_{RUN} Hyst	RUN Pin Hysteresis				80		mV
OVLO	Overvoltage Lockout Threshold	V_{OVLO} Rising with Respect to V_{OUT}^-	●	1.1	1.2	1.3	V
OVLO Hyst	OVLO Hysteresis				100		mV
	OVLO Delay				1		µs
	Feedback Overvoltage Protection	Measured at V_{FB}, Relative to Regulated V_{FB}		7	10	13	%
I_{SENSE}^+	$SENSE^+$ Pin Current					±1	µA
I_{SENSE}^-	$SENSE^-$ Pin Current	$SENSE^-$ < V_{INTVCC} – 0.5V				±1	µA
		$SENSE^-$ > V_{INTVCC} + 0.5V			850		µA
	Maximum Duty Factor	FREQ = V_{OUT}^-		98	99		%
I_{SS}	Soft-Start Charge Current	V_{SS} = 0V		8	10	12	µA
$V_{SENSE(MAX)}$	Maximum Current Sense Threshold	V_{FB} = 0.7V, V_{SENSE}^- = 3.3V					
		ILIM = FLOAT	●	66	75	84	mV
		ILIM = V_{OUT}^-	●	43	50	57	mV
		ILIM = $INTV_{CC}$	●	90	100	109	mV
Gate Driver							
	TG Pull-Up On-Resistance	V_{DRVSET} = $INTV_{CC}$			2.2		Ω
	TG Pull-Down On-Resistance				1.0		Ω

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2), V_{IN} = 12V, V_{RUN} = 5V with respect to GND, $EXTV_{CC}$ = 0V, V_{DRVSET} = 0V, VPRG = FLOAT unless otherwise noted. All pin voltages with respect to V_{OUT}^-, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	BG Pull-Up On-Resistance BG Pull-Down On-Resistance	V_{DRVSET} = $INTV_{CC}$			2.0 1.0		Ω Ω
	BOOST to DRV_{CC} Switch On-Resistance	V_{SW} = 0V, V_{DRVSET} = $INTV_{CC}$			11		Ω
	TG Transition Time: Rise Time Fall Time	(Note 6) V_{DRVSET} = $INTV_{CC}$ C_{LOAD} = 3300pF C_{LOAD} = 3300pF			 25 15		 ns ns
	BG Transition Time: Rise Time Fall Time	(Note 6) V_{DRVSET} = $INTV_{CC}$ C_{LOAD} = 3300pF C_{LOAD} = 3300pF			 25 15		 ns ns
	Top Gate Off to Bottom Gate On Delay Synchronous Switch-On Delay Time	C_{LOAD} = 3300pF each driver, V_{DRVSET} = $INTV_{CC}$			55		ns
	Bottom Gate Off to Top Gate On Delay Top Switch-On Delay Time	C_{LOAD} = 3300pF each driver, V_{DRVSET} = $INTV_{CC}$			50		ns
$t_{ON(MIN)}$	TG Minimum On-Time	(Note 7) V_{DRVSET} = $INTV_{CC}$			80		ns
DRV_{CC} LDO Regulator							
	DRV_{CC} Voltage from NDRV LDO Regulator	NDRV Driving External NFET, V_{EXTVCC} = 0V 7V < V_{IN} < 150V, DRVSET = V_{OUT}^- 11V < V_{IN} < 150V, DRVSET = INTVCC		 5.8 9.6	 6.0 10.0	 6.2 10.4	 V V
	DRV_{CC} Load Regulation from NDRV LDO Regulator	NDRV Driving External NFET I_{CC} = 0mA to 50mA, V_{EXTVCC} = 0V			 0	 1.0	 %
	DRV_{CC} Voltage from Internal V_{IN} LDO	NDRV = DRV_{CC} (NDRV LDO Off), V_{EXTVCC} = 0V 7V < V_{IN} < 150V, DRVSET = V_{OUT}^- 11V < V_{IN} < 150V, DRVSET = $INTV_{CC}$		 5.6 9.5	 5.85 9.85	 6.1 10.3	 V V
	DRV_{CC} Load Regulation from V_{IN} LDO	I_{CC} = 0mA to 50mA, V_{EXTVCC} = 0V DRVSET = V_{OUT} DRVSET = $INTV_{CC}$			 1.4 0.9	 2.5 2.0	 % %
	DRV_{CC} Voltage from Internal $EXTV_{CC}$ LDO	7V < V_{EXTVCC} < 13V, DRVSET = V_{OUT}^- 11V < V_{EXTVCC} < 13V, DRVSET = $INTV_{CC}$		5.8 9.6	6.0 10.0	6.2 10.4	V V
	DRV_{CC} Load Regulation from Internal $EXTV_{CC}$ LDO	I_{CC} = 0mA to 50mA DRVSET = V_{OUT}^-, V_{EXTVCC} = 8.5V DRVSET = $INTV_{CC}$, V_{EXTVCC} = 13V			 0.7 0.5	 2.0 2.0	 % %
	$EXTV_{CC}$ LDO Switchover Voltage	$EXTV_{CC}$ Ramping Positive DRVUV = V_{OUT}^- DRVUV = $INTV_{CC}$, DRVSET = $INTV_{CC}$		 4.5 7.4	 4.7 7.7	 4.9 8.0	 V V
	$EXTV_{CC}$ Hysteresis				250		mV
	Programmable DRVCC	R_{DRVSET} = 50kΩ, NDRV Driving External NFET, V_{EXTVCC} = 0V			5.0		V
	Programmable DRVCC	R_{DRVSET} = 70kΩ, NDRV Driving External NFET, V_{EXTVCC} = 0V		6.4	7.0	7.6	V
	Programmable DRVCC	R_{DRVSET} = 90kΩ, NDRV Driving External NFET, V_{EXTVCC} = 0V			9.0		V
$INTV_{CC}$ LDO Regulator							
V_{INTVCC}	$INTV_{CC}$ Voltage	I_{CC} = 0mA to 2mA		4.7	5.0	5.2	V
Oscillator and Phase-Locked Loop							
	Programmable Frequency	R_{FREQ} = 25kΩ, PLLIN = DC Voltage			105		kHz
	Programmable Frequency	R_{FREQ} = 65kΩ, PLLIN = DC Voltage		375	440	505	kHz
	Programmable Frequency	R_{FREQ} = 105kΩ, PLLIN = DC Voltage			835		kHz

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2), V_{IN} = 12V, V_{RUN} = 5V with respect to V_{OUT}^-, $EXTV_{CC}$ = 0V, V_{DRVSET} = 0V, VPRG = FLOAT unless otherwise noted. All pin voltages with respect to V_{OUT}^-, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	Low Fixed Frequency	V_{FREQ} = V_{OUT}^-, PLLIN = DC Voltage		320	350	380	kHz
	High Fixed Frequency	V_{FREQ} = $INTV_{CC}$, PLLIN = DC Voltage		485	535	585	kHz
f_{SYNC}	Synchronizable Frequency	PLLIN = External Clock	●	75		850	kHz
	PLLIN Input High Level PLLIN Input Low Level	PLLIN = External Clock with Respect to GND PLLIN = External Clock with Respect to GND	● ●	2.8		 0.5	V V
PGOOD Output							
V_{PGL}	PGOOD Voltage Low	I_{PGOOD} = 2mA, V_{PGL} with Respect to GND			0.02	0.04	V
I_{PGOOD}	PGOOD Leakage Current	V_{PGOOD} = 3.3V				10	µA
	PGOOD Trip Level	V_{FB} with Respect to Set Regulated Voltage V_{FB} Ramping Negative Hysteresis		 –13	 –10 2.5	 –7	 % %
		V_{FB} with Respect to Set Regulated Voltage V_{FB} Ramping Positive Hysteresis		7	10 2.5	13	% %
	Delay for Reporting a Fault				40		µs

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC3896 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC3896E is guaranteed to meet performance specifications from 0°C to 85°C. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3896I is guaranteed over the –40°C to 125°C operating junction temperature range and the LTC3896H is guaranteed over the –40°C to 150°C operating junction temperature range. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors. High temperatures degrade operating lifetimes; operating lifetime is derated for junction temperatures greater than 125°C. The junction temperature (T_J, in °C) is calculated from the ambient temperature (T_A, in °C) and power dissipation (P_D, in Watts) according to the formula:

$$T_J = T_A + (P_D \bullet \theta_{JA})$$

where θ_{JA} = 28°C/W for the TSSOP package.

Note 3: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. The maximum rated junction temperature will be exceeded when this protection is active. Continuous operation above the specified absolute maximum operating junction temperature may impair device reliability or permanently damage the device.

Note 4: The LTC3896 is tested in a feedback loop that servos V_{ITH} to a specified voltage and measures the resultant V_{FB}. The specification at 85°C is not tested in production and is assured by design, characterization and correlation to production testing at other temperatures (125°C for the LTC3896E and LTC3896I, 150°C for the LTC3896H). For the LTC3896I and LTC3896H, the specification at 0°C is note tested in production and is assured by design, characterization and correlation to production testing at –40°C.

Note 5: Dynamic supply current is higher due to the gate charge being delivered at the switching frequency. See the Applications Information section.

Note 6: Rise and fall times are measured using 10% and 90% levels. Delay times are measured using 50% levels.

Note 7: The minimum on-time condition is specified for an inductor peak-to-peak ripple current >40% of I_{MAX} (see Minimum On-Time Considerations in the Applications Information section).

Note 8: Do not apply a voltage or current source to these pins. They must be connected to capacitive loads only, otherwise permanent damage may occur.

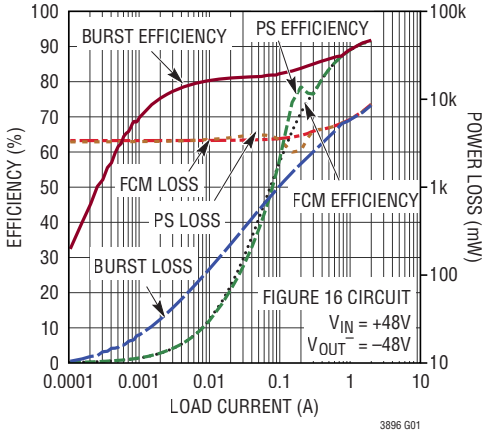
Note 9: Do not apply a voltage or current source to the NDRV pin, other than tying NDRV to DRV_{CC} when not used. If used it must be connected to capacitive loads only (see DRV_{CC} Regulators (OPTI-DRIVE) in the Applications Information section), otherwise permanent damage may occur.

Note 10: The minimum input supply (V_{IN} + $|V_{OUT}^-|$) operating range is dependent on the DRV_{CC} UVLO thresholds as determined by the DRVUV pin setting.

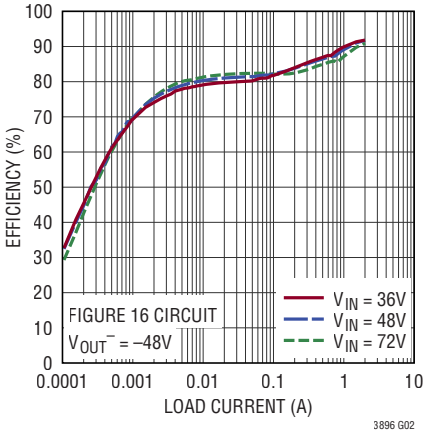
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} and V_{OUT}^- with respect to GND. All other voltages with respect to V_{OUT}^-, unless otherwise noted.

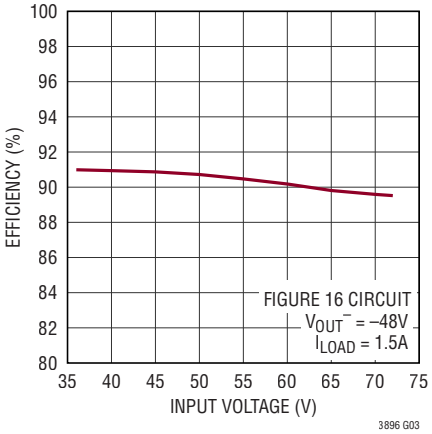
Efficiency and Power Loss vs Load Current



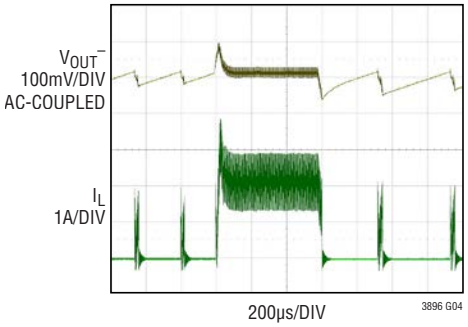
Efficiency vs Load Current



Efficiency vs Input Voltage

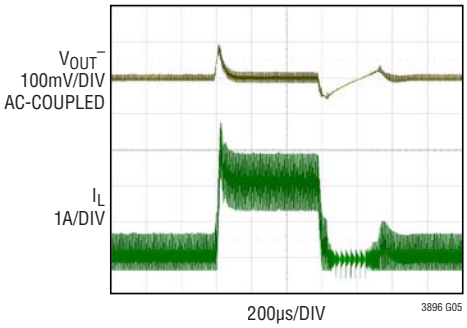


Load Step Burst Mode Operation



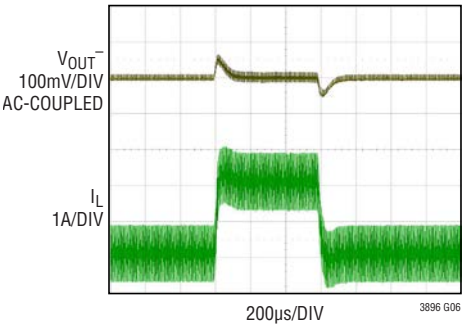
V_{OUT}^- = –48V
LOAD STEP = 0A to 1A
FIGURE 16 CIRCUIT

Load Step Pulse-Skipping Mode



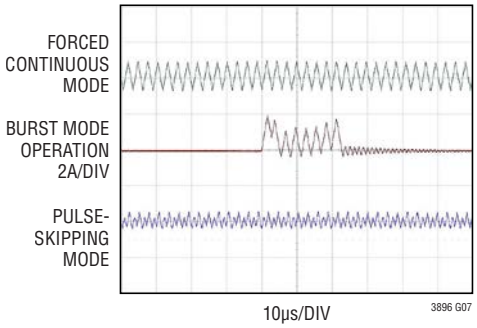
V_{OUT}^- = –48V
LOAD STEP = 0A to 1A
FIGURE 16 CIRCUIT

Load Step Forced Continuous Mode



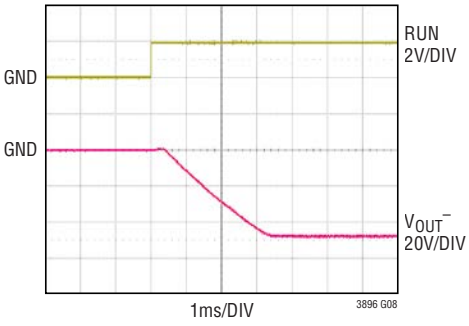
V_{OUT}^- = –48V
LOAD STEP = 0A to 1A
FIGURE 16 CIRCUIT

Inductor Current at Light Load



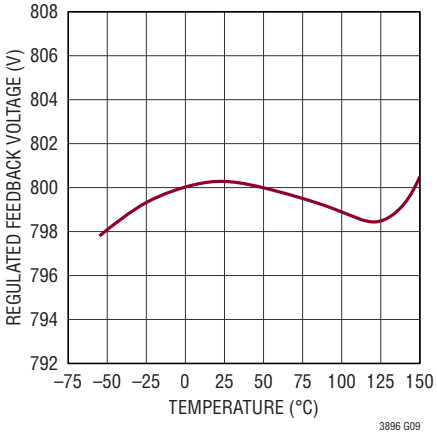
V_{OUT}^- = –48V
I_{LOAD} = 1mA
FIGURE 16 CIRCUIT

Soft Start-Up



V_{OUT}^- = –48V
FIGURE 16 CIRCUIT

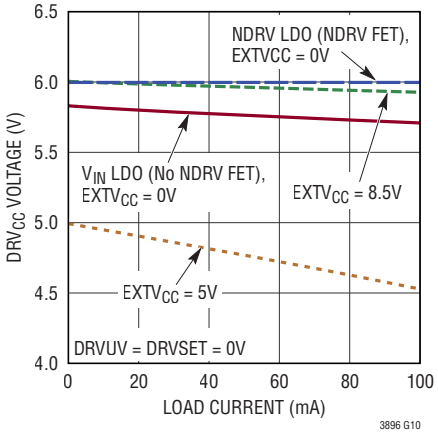
Regulated Feedback Voltage vs Temperature



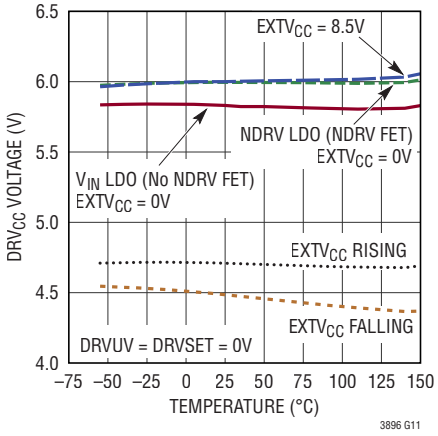
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} and V_{OUT}^- with respect to GND. All other voltages with respect to V_{OUT}^-, unless otherwise noted.

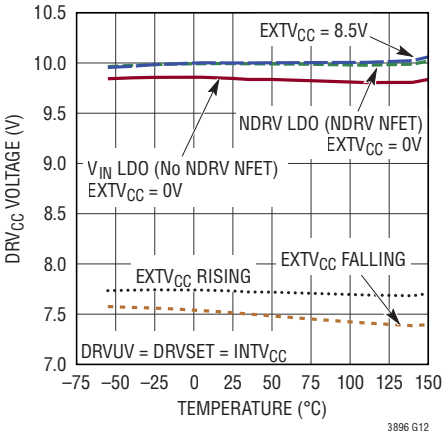
DRV_{CC} vs Load Current



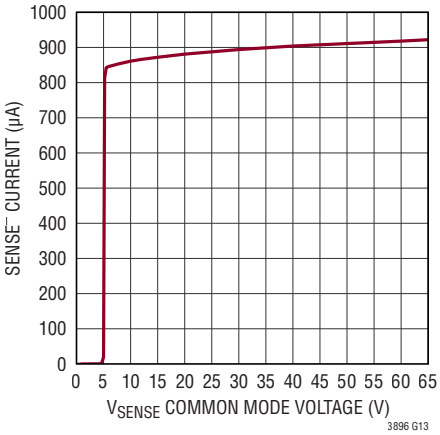
$EXTV_{CC}$ Switchover and DRV_{CC} Voltages vs Temperature



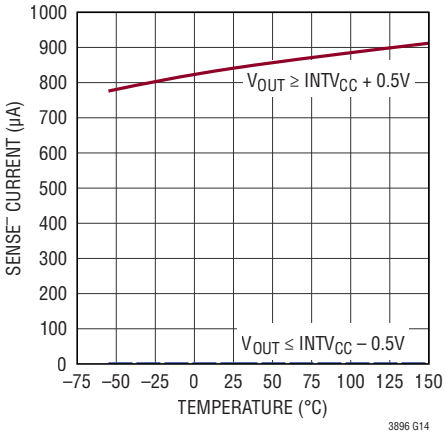
$EXTV_{CC}$ Switchover and DRV_{CC} Voltages vs Temperature



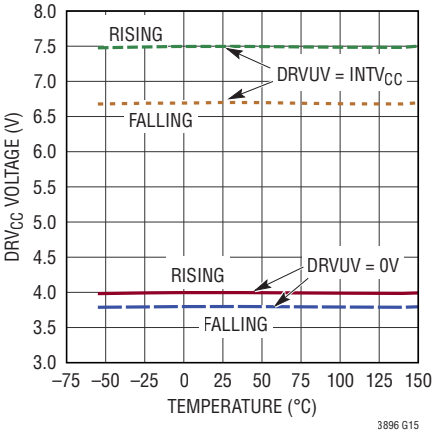
SENSE⁻ Pins Input Current vs V_{SENSE} Voltage



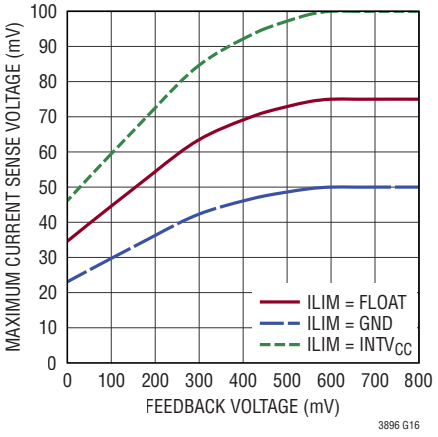
SENSE⁻ Pin Input Bias Current vs Temperature



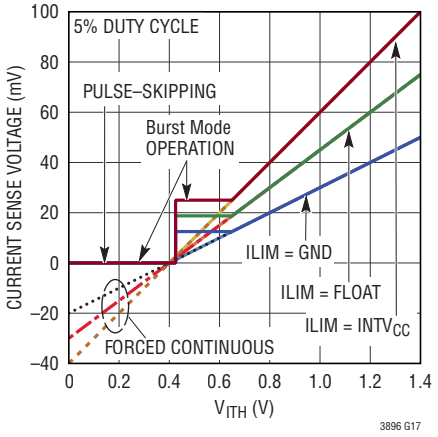
Undervoltage Lockout Threshold vs Temperature



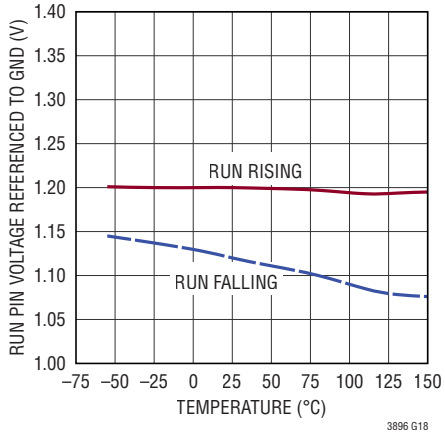
Foldback Current Limit



Maximum Current Sense Threshold vs ITH Voltage



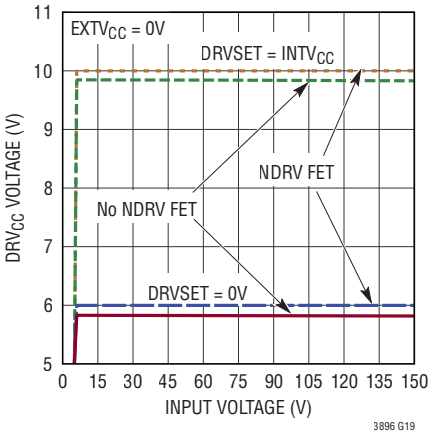
RUN Threshold vs Temperature



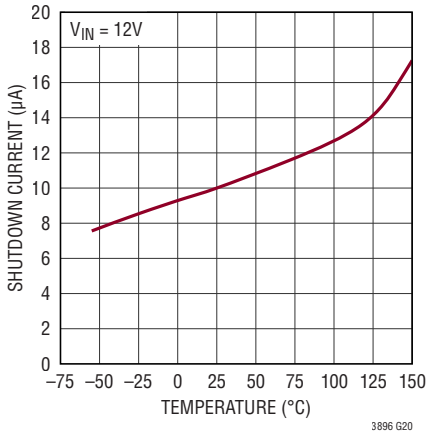
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} and V_{OUT}^- with respect to GND. All other voltages with respect to V_{OUT}^-, unless otherwise noted.

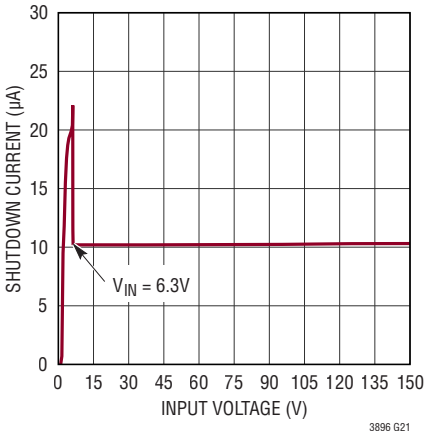
DRV_{CC} Line Regulation



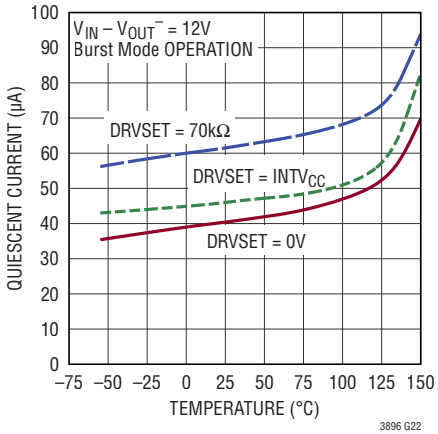
Shutdown Current vs Temperature



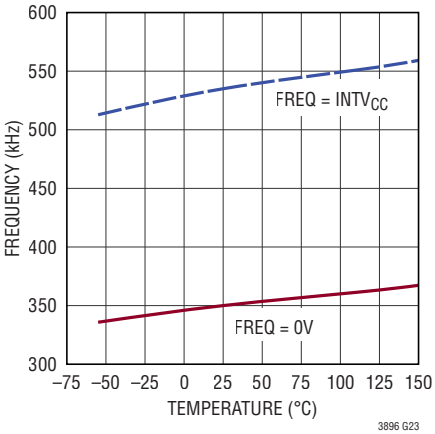
Shutdown Current vs Input Voltage



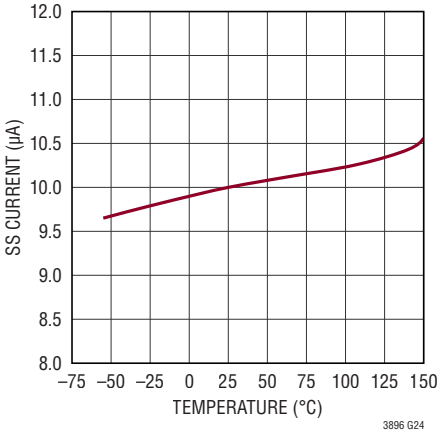
Quiescent Current vs Temperature



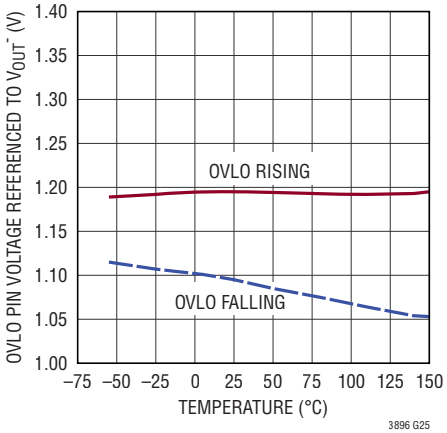
Oscillator Frequency vs Temperature



SS Pull-Up Current vs Temperature



OVLO Threshold vs Temperature



PIN FUNCTIONS

OVLO (Pin 1): Overvoltage Lockout Input. A voltage on this pin above 1.2V with respect to V_{OUT}^- disables switching of the controller. The DRV_{CC} and $INTV_{CC}$ supplies maintain regulation during an OVLO event. Exceeding the OVLO threshold triggers a soft-start reset. If the OVLO function is not used, connect this pin to V_{OUT}^-.

VPRG (Pin 2): Output Voltage Control Pin. This pin sets the regulator in adjustable output mode using external feedback resistors or fixed –5V/–3.3V output mode. Floating this pin allows the output to be programmed from –0.8V to –60V with an external resistor divider on the V_{FB} pin, regulating V_{FB} to 0.8V with respect to V_{OUT}^-. Tying this pin to $INTV_{CC}$ or V_{OUT}^- programs the output to –5V or –3.3V, respectively, through an internal resistor divider on V_{FB}. In fixed –5V/–3.3V output mode, V_{FB} should connect to GND, which is the positive terminal of the output.

$SENSE^+$ (Pin 3): The (+) Input to the Differential Current Comparator. The ITH pin voltage and controlled offsets between the $SENSE^-$ and $SENSE^+$ pins in conjunction with R_{SENSE} set the current trip threshold.

$SENSE^-$ (Pin 4): The (–) Input to the Differential Current Comparator. When $SENSE^-$ is greater than $INTV_{CC}$, the $SENSE^-$ pin supplies power to the current comparator.

SS (Pin 5): Soft-Start Input. The LTC3896 regulates the V_{FB} voltage with respect to V_{OUT}^- to the smaller of 0.8V or the voltage on the SS pin. An internal 10µA pull-up current source is connected to this pin. A capacitor to V_{OUT}^- at this pin sets the ramp time to final regulated output voltage. The SS pin is also used for the Regulator Shutdown (REGSD) feature. A 5µA/1µA pull-down current can be connected on SS depending on the state of the $EXTV_{CC}$ LDO and the voltage on SS. See Regulator Shutdown (REGSD) section in the Operation section for more information. To defeat the REGSD feature, place a 330kΩ or smaller resistor between $INTV_{CC}$ and SS. See Soft-Start Pin in the Applications Information section for more information on defeating REGSD.

V_{FB} (Pin 6): Feedback Input. If the VPRG pin is floating, the V_{FB} pin receives the remotely sensed feedback voltage from an external resistor divider across the output. If VPRG is tied to V_{OUT}^- or $INTV_{CC}$, the V_{FB} pin should connect to the GND pin.

ITH (Pin 7): Error Amplifier Output and Switching Regulator Compensation Point. The current comparator trip point increases with this control voltage.

MODE (Pin 8): Mode Select and Burst Clamp Adjust Input. This input determines how the LTC3896 operates at light loads. Pulling this pin to V_{OUT}^- selects Burst Mode operation with the burst clamp level defaulting to 25% of $V_{SENSE(MAX)}$. Tying this pin to a voltage between 0.5V and 1.0V with respect to V_{OUT}^- selects Burst Mode operation and adjusts the burst clamp between 10% and 60%. Tying this pin to $INTV_{CC}$ forces continuous inductor current operation. Tying this pin to a voltage greater than 1.4V and less than $INTV_{CC}$–1.3V (with respect to V_{OUT}^-) selects pulse-skipping operation.

V_{OUT}^- (Pins 9, 15, Exposed Pin 39): Negative Terminal of Output Voltage. This serves as a virtual ground return for most of the LTC3896's circuits. Most pins and components are referenced to V_{OUT}^-, which can operate at up to 60V (65V Abs Max) below the GND pin. The exposed pad must be soldered to the PCB for rated electrical and thermal performance.

V_{OUT}^- (Pin 10): This pin must be externally tied to the other V_{OUT}^- pins (Pin 9, e.g.) but is not internally electrically connected to them.

CLKOUT (Pin 11): Output Clock Signal. This signal is available to daisy-chain other controller ICs for additional MOSFET driver stages/phases. The output levels swing from $INTV_{CC}$ to V_{OUT}^-.

GND (Pin 12): Ground. This pin should be externally tied to the true ground (e.g., ground terminal of the positive input supply connected to V_{IN}). The RUN, PLLIN, and PGOOD pins are referenced to this GND pin.

PIN FUNCTIONS

PLLIN (Pin 13): External Synchronization Input to Phase Detector. When an external clock is applied to this pin, the phase-locked loop will force the rising TG signal to be synchronized with the rising edge of the external clock. If the MODE pin is set to Forced Continuous Mode or Burst Mode operation, then the regulator operates in Forced Continuous Mode when synchronized. If the MODE pin is set to pulse-skipping mode, then the regulator operates in pulse-skipping mode when synchronized. The PLLIN pin is referenced to the GND pin, allowing the LTC3896 to be used with a true ground-referenced external clock source with no level shifters needed.

PGOOD (Pin 14): Open-Drain Logic Output. PGOOD is pulled to GND when the voltage on the V_{FB} pin is not within ±10% of its set point. PGOOD is referenced to GND to allow it to interface with external true ground-referenced components with no level shifters needed.

NC (Pin 16): No connect. Float this pin or connect to GND or V_{OUT}^-.

FREQ (Pin 17): Frequency Control Pin for the Internal VCO. Connecting the pin to V_{OUT}^- forces the VCO to a fixed low frequency of 350kHz. Connecting the pin to $INTV_{CC}$ forces the VCO to a fixed high frequency of 535kHz. Other frequencies between 50kHz and 900kHz can be programmed by using a resistor between FREQ and V_{OUT}^-. An internal 20µA pull-up current develops the voltage to be used by the VCO to control the frequency.

DRVSET (Pin 18): DRV_{CC} Regulation Program Pin. This pin sets the regulated output voltage of the DRV_{CC} linear regulator. Tying this pin to V_{OUT}^- sets DRV_{CC} to 6.0V. Tying this pin to $INTV_{CC}$ sets DRV_{CC} to 10V. Other voltages between 5V and 10V can be programmed by placing a resistor (50k to 100k) between the DRVSET pin and V_{OUT}^-. An internal 20µA pull-up current develops the voltage to be used as the reference to the DRV_{CC} LDO.

DRVUV (Pin 19): DRV_{CC} UVLO Program Pin. This pin determines the higher or lower DRV_{CC} UVLO and $EXTV_{CC}$ switchover thresholds, as listed on the Electrical Characteristics table. Connecting DRVUV to V_{OUT}^- chooses the lower thresholds whereas tying DRVUV to $INTV_{CC}$ chooses the higher thresholds. Do not float this pin.

TG (Pin 20): High Current Gate Drives for Top N-Channel MOSFET. This is the output of floating high side driver with a voltage swing equal to DRV_{CC} superimposed on the switch node voltage SW.

SW (Pin 21): Switch Node Connection to Inductor.

BOOST (Pin 22): Bootstrapped Supply to the Topside Floating Driver. A capacitor is connected between the BOOST and SW pins. Voltage swing at the BOOST pin is from approximately DRV_{CC} to (V_{IN} + DRV_{CC}).

BG (Pin 24): High Current Gate Drive for Bottom (Synchronous) N-Channel MOSFET. Voltage swing at this pin is from V_{OUT}^- to DRV_{CC}.

DRV_{CC} (Pin 26): Output of the Internal or External Low Dropout Regulators. The gate drivers are powered from this voltage source. The DRV_{CC} voltage is set by the DRVSET pin. Must be decoupled to V_{OUT}^- with a minimum of 4.7µF ceramic or other low ESR capacitor, as close as possible to the IC. Do not use the DRV_{CC} pin for any other purpose.

NDRV (Pin 28): Drive Output for External Pass Device of the NDRV LDO Linear Regulator for DRV_{CC}. Connect this pin to the gate of an external NMOS pass device. To disable this external NDRV LDO, tie NDRV to DRV_{CC}.

V_{IN} (Pin 30): Main Supply Pin. A bypass capacitor should be tied between this pin and the GND pin. An additional bypass capacitor between the V_{IN} and V_{OUT}^- pins is recommended.

$EXTV_{CC}$ (Pin 32): External Power Input to an Internal LDO linear regulator Connected to DRV_{CC}. This LDO supplies DRV_{CC} power from $EXTV_{CC}$, bypassing the internal LDO powered from V_{IN} or the external NDRV LDO whenever $EXTV_{CC}$ is higher than its switchover threshold (4.7V or 7.7V referenced to V_{OUT}^- depending on the DRVUV pin). See the $EXTV_{CC}$ Connection section in the Applications Information section. Do not exceed 14V with respect to V_{OUT}^- on this pin. Do not connect $EXTV_{CC}$ to a voltage greater than V_{IN}. Connect to V_{OUT}^- if not used.

PIN FUNCTIONS

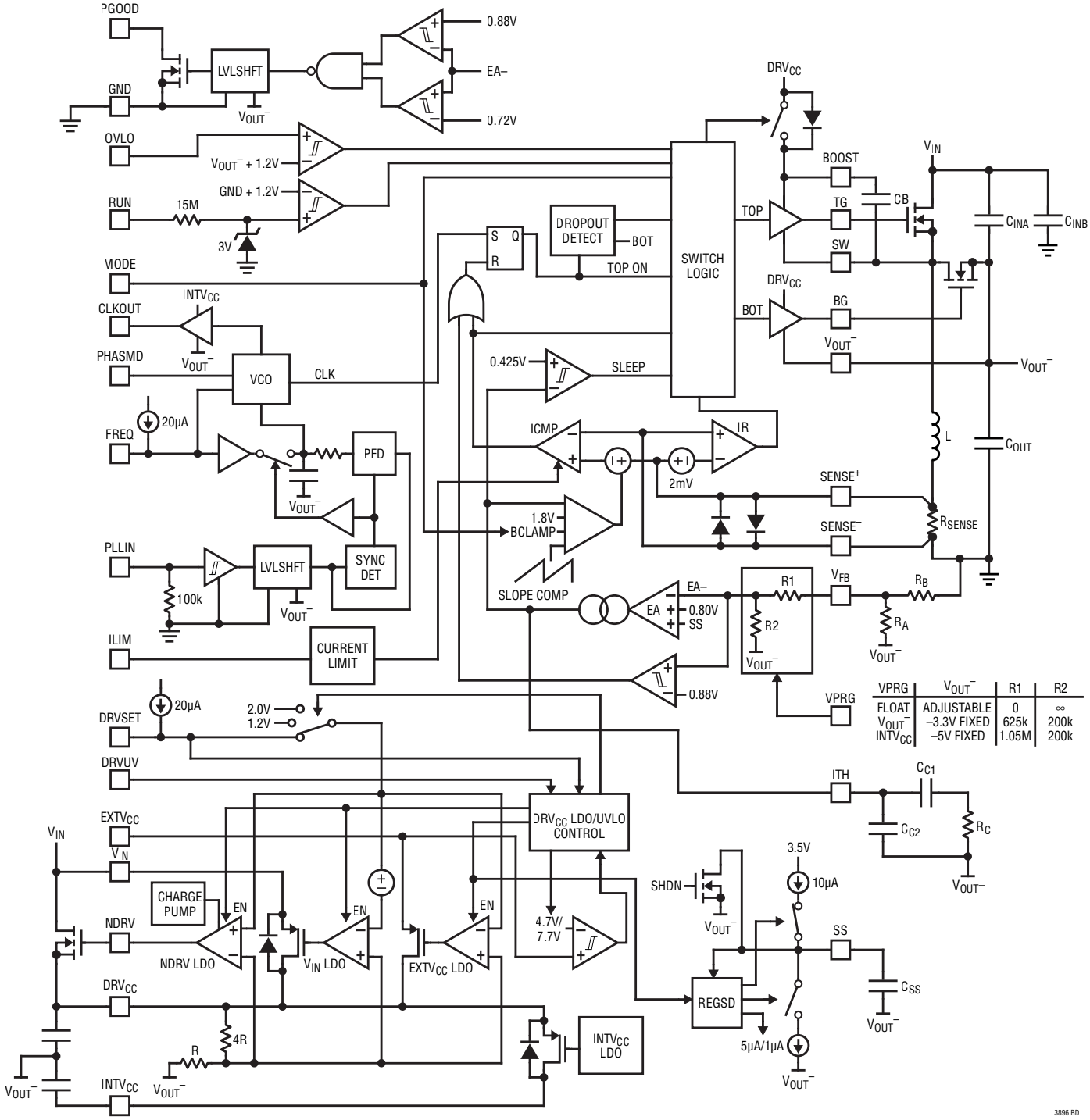
RUN (Pin 34): Run Control Input. Forcing this pin below 1.12V (with respect to GND) shuts down the controller. Forcing this pin below 0.7V shuts down the entire LTC3896, reducing quiescent current to approximately 10µA. The RUN pin is referenced to the GND pin, allowing the LTC3896 to be used with a true ground-referenced external signal or logic with no level shifters needed. This pin can be tied to V_{IN} for always-on operation. Do not float this pin.

PHASMD (Pin 36): Control Input to Phase Selector. This pin determines the CLKOUT phase relationships with respect to TG. Pulling this pin to V_{OUT}^- forces CLKOUT to be out of phase 90° with respect to TG. Connecting this pin to $INTV_{CC}$ forces CLKOUT to be out-of-phase 120° with respect to TG. Floating this pin forces CLKOUT to be out of phase 180° with respect to TG.

ILIM (Pin 37): Current Comparator Sense Voltage Range Input. Tying this pin to V_{OUT}^- or $INTV_{CC}$ or floating it sets the maximum current sense threshold to one of three different levels (50mV, 100mV, and 75mV, respectively).

$INTV_{CC}$ (Pin 38): Output of the Internal 5V (referenced to V_{OUT}^-) Low Dropout Regulator. CLKOUT and many of the low voltage analog and digital circuits are powered from this voltage source. A low ESR 0.1µF ceramic bypass capacitor should be connected between $INTV_{CC}$ and V_{OUT}^-, as close as possible to the IC.

BLOCK DIAGRAM



VPRG	V_{OUT^-}	R1	R2
FLOAT	ADJUSTABLE	0	∞
V_{OUT^-}	–3.3V FIXED	625k	200k
$INTV_{CC}$	–5V FIXED	1.05M	200k

* ALL VOLTAGES WITH RESPECT TO V_{OUT^-} UNLESS OTHERWISE NOTED.

OPERATION

Main Control Loop

The LTC3896 uses a constant frequency, current mode control architecture. During normal operation, the external top MOSFET is turned on when the clock sets the RS latch, and is turned off when the main current comparator, ICMP, resets the RS latch. The peak inductor current at which ICMP trips and resets the latch is controlled by the voltage on the ITH pin, which is the output of the error amplifier, EA. The error amplifier compares the output voltage feedback signal at the V_{FB} pin (which is generated with an external resistor divider connected across ground (GND) to the negative output voltage, V_{OUT}^-) to the internal 0.800V reference voltage (referenced to V_{OUT}^-). When the load current increases, it causes a slight decrease in V_{FB} relative to the reference, which causes the EA to increase the ITH voltage until the average inductor current matches the new load current.

After the top MOSFET is turned off each cycle, the bottom MOSFET is turned on until either the inductor current starts to reverse, as indicated by the current comparator IR, or the beginning of the next clock cycle.

$DRV_{CC}/EXTV_{CC}/INTV_{CC}$ Power

Power for the top and bottom MOSFET drivers is derived from the DRV_{CC} pin. The DRV_{CC} supply voltage can be programmed from 5V to 10V referenced to V_{OUT}^- by setting the DRVSET pin. Two separate LDOs (low dropout linear regulators) can provide power from V_{IN} to DRV_{CC}. The internal V_{IN} LDO uses an internal P-channel pass device between the V_{IN} and DRV_{CC} pins. To prevent high on-chip power dissipation in high input voltage applications, the LTC3896 also includes an NDRV LDO that utilizes the NDRV pin to supply power to DRV_{CC} by driving the gate of an external N-channel MOSFET acting as a linear regulator with its source connected to DRV_{CC} and drain connected to V_{IN}. The NDRV LDO includes an internal charge pump that allows NDRV to be driven above V_{IN} for low dropout performance.

When the $EXTV_{CC}$ pin is tied to a voltage below its switchover voltage (4.7V or 7.7V with respect to V_{OUT}^-, depending on the DRVUV pin), the V_{IN} and NDRV LDOs are enabled and one of them supplies power from V_{IN} to DRV_{CC}. The V_{IN} LDO has a slightly lower regulation point than the NDRV LDO. If the NDRV LDO is being used with an external N-channel MOSFET, the gate of the MOSFET tied to the NDRV pin is driven such that DRV_{CC} regulates above the V_{IN} LDO regulation point, causing all DRV_{CC} current to flow through the external N-channel MOSFET, bypassing the internal V_{IN} LDO pass device. If the NDRV LDO is not being used, all DRV_{CC} current flows through the internal P-channel pass device between the V_{IN} and DRV_{CC} pins.

If $EXTV_{CC}$ is taken above its switchover voltage, the V_{IN} and NDRV LDOs are turned off and an $EXTV_{CC}$ LDO is turned on. Once enabled, the $EXTV_{CC}$ LDO supplies power from $EXTV_{CC}$ to DRV_{CC}. Using the $EXTV_{CC}$ pin allows the DRV_{CC} power to be derived from a high efficiency external source such as the LTC3896 switching regulator output.

The top MOSFET driver is biased from the floating bootstrap capacitor, C_B, which normally recharges during each cycle through an internal switch whenever SW goes low.

The $INTV_{CC}$ supply powers most of the other internal circuits in the LTC3896. The $INTV_{CC}$ LDO regulates to a fixed value of 5V (with respect to V_{OUT}^-) and its power is derived from the DRV_{CC} supply.

Shutdown and Start-Up (RUN, SS Pins)

The LTC3896 can be shut down using the RUN pin. Connecting the RUN pin below 1.12V (with respect to GND) shuts down the main control loop. Connecting the RUN pin below 0.7V disables the controller and most internal circuits, including the DRV_{CC} and $INTV_{CC}$ LDOs. In this state, the LTC3896 draws only 10µA of quiescent current.

The RUN pin has no internal pull-up current, so the pin must be externally pulled up or driven directly by logic. The RUN pin can tolerate up to 150V (with respect to V_{OUT}^-), so it can be conveniently tied to V_{IN} in always-on applications where the controller is enabled continuously and never shut down.

The start-up of the controller's output voltage V_{OUT}^- is controlled by the voltage on the SS pin. When the voltage on the SS pin is less than the 0.8V internal reference (with respect to V_{OUT}^-), the LTC3896 regulates the V_{FB} voltage to the SS pin voltage instead of the 0.8V reference. This allows the SS pin to be used to program a soft-start by connecting an external capacitor from the SS pin to V_{OUT}^-.

OPERATION

An internal 10µA pull-up current charges this capacitor creating a voltage ramp on the SS pin. As the SS voltage rises linearly from V_{OUT}^- to 0.8V above V_{OUT}^- (and beyond), the output voltage V_{OUT}^- descends smoothly from zero to its final negative value.

Light Load Current Operation (Burst Mode Operation, Pulse-Skipping or Forced Continuous Mode) (MODE Pin)

The LTC3896 can be enabled to enter high efficiency Burst Mode operation, constant frequency pulse-skipping mode, or forced continuous conduction mode at light load currents. To select Burst Mode operation, tie the MODE pin to V_{OUT}^- or a voltage between 0.5V and 1.0V (with respect to V_{OUT}^-). To select forced continuous operation, tie the MODE pin to $INTV_{CC}$. To select pulse-skipping mode, tie the MODE pin to a DC voltage greater than 1.4V and less than $INTV_{CC}$ – 1.3V (with respect to V_{OUT}^-). This can be done with a simple resistor divider between $INTV_{CC}$ and V_{OUT}^-, with both resistors being 100kΩ.

When the controller is enabled for Burst Mode operation, the minimum peak current in the inductor (burst clamp) is adjustable and can be programmed by the voltage on the MODE pin. Tying the MODE pin to V_{OUT}^- sets the default burst clamp to approximately 25% of the maximum sense voltage even when the voltage on the ITH pin indicates a lower value. A voltage between 0.5V and 1.0V (with respect to V_{OUT}^-) on the MODE pin programs the burst clamp linearly between 10% and 60% of the maximum sense voltage.

In Burst Mode operation, if the average inductor current is higher than the load current, the error amplifier, EA, will decrease the voltage on the ITH pin. When the ITH voltage drops below 0.425V (with respect to V_{OUT}^-), the internal sleep signal goes high (enabling sleep mode) and both external MOSFETs are turned off. The ITH pin is then disconnected from the output of the EA and parked at 0.450V.

In sleep mode, much of the internal circuitry is turned off, reducing the quiescent current that the LTC3896 draws to only 40µA. In sleep mode, the load current is supplied by the output capacitor. As the output voltage decreases, the EA's output begins to rise. When the output voltage drops enough, the ITH pin is reconnected to the output of the EA, the sleep signal goes low, and the controller resumes normal operation by turning on the top external MOSFET on the next cycle of the internal oscillator.

When the controller is enabled for Burst Mode operation, the inductor current is not allowed to reverse. The reverse current comparator (IR) turns off the bottom external MOSFET just before the inductor current reaches zero, preventing it from reversing and going positive. Thus, the controller operates discontinuously.

In forced continuous operation, the inductor current is allowed to reverse at light loads or under large transient conditions. The peak inductor current is determined by the voltage on the ITH pin, just as in normal operation. In this mode, the efficiency at light loads is lower than in Burst Mode operation. However, continuous operation has the advantage of lower output voltage ripple and less interference to audio circuitry. In forced continuous mode, the output ripple is independent of load current.

When the MODE pin is connected for pulse-skipping mode, the LTC3896 operates in PWM pulse-skipping mode at light loads. In this mode, constant frequency operation is maintained down to approximately 1% of designed maximum output current. At very light loads, the current comparator, ICMP, may remain tripped for several cycles and force the external top MOSFET to stay off for the same number of cycles (i.e., skipping pulses). The inductor current is not allowed to reverse (discontinuous operation). This mode, like forced continuous operation, exhibits low output ripple as well as low audio noise and reduced RF interference as compared to Burst Mode operation. It provides higher low current efficiency than forced continuous mode, but not nearly as high as Burst Mode operation. At greater $|V_{OUT}^-|$ voltages, the efficiency in pulse-skipping mode is comparable to forced continuous mode.

If the PLLIN pin is clocked by an external clock source to use the phase-locked loop (see Frequency Selection and Phase-Locked Loop section), then the LTC3896 operates in forced continuous operation when the MODE pin is set to forced continuous or Burst Mode operation. The controller operates in pulse-skipping mode when clocked by an external clock source with the MODE pin set to pulse-skipping mode.

OPERATION

Frequency Selection and Phase-Locked Loop (FREQ and PLLIN Pins)

The selection of switching frequency is a trade-off between efficiency and component size. Low frequency operation increases efficiency by reducing MOSFET switching losses, but requires larger inductance and/or capacitance to maintain low output ripple voltage.

The switching frequency of the LTC3896 can be selected using the FREQ pin.

If the PLLIN pin is not being driven by an external clock source, the FREQ pin can be tied to V_{OUT}^-, tied to $INTV_{CC}$ or programmed through an external resistor to V_{OUT}^-. Tying FREQ to V_{OUT}^- selects 350kHz while tying FREQ to $INTV_{CC}$ selects 535kHz. Placing a resistor between FREQ and V_{OUT}^- allows the frequency to be programmed between 50kHz and 900kHz, as shown in Figure 15.

A phase-locked loop (PLL) is available on the LTC3896 to synchronize the internal oscillator to an external clock source that is connected to the PLLIN pin. The LTC3896's phase detector adjusts the voltage (through an internal lowpass filter) of the VCO input to align the turn-on of the external top MOSFET to the rising edge of the synchronizing signal.

The VCO input voltage is prebiased to the operating frequency set by the FREQ pin before the external clock is applied. If prebiased near the external clock frequency, the PLL loop only needs to make slight changes to the VCO input in order to synchronize the rising edge of the external clock's to the rising edge of TG. The ability to prebias the loop filter allows the PLL to lock-in rapidly without deviating far from the desired frequency.

The typical capture range of the LTC3896's phase-locked loop is from approximately 55kHz to 1MHz, with a guarantee to be between 75kHz and 850kHz. In other words, the LTC3896's PLL is guaranteed to lock to an external clock source whose frequency is between 75kHz and 850kHz. It is recommended that the external clock source swing from GND (0V) to at least 2.8V.

PolyPhase Applications (CLKOUT and PHASMD Pins)

The LTC3896 features two pins (CLKOUT and PHASMD) that allow other controller ICs to be daisy-chained with the LTC3896 in PolyPhase applications. The clock output signal on the CLKOUT pin, which swings from V_{OUT}^- to $INTV_{CC}$, can be used to synchronize additional power stages in a multiphase power supply solution feeding a single, high current output or multiple separate outputs. See the application circuit in Figure 17 for an example of how to configure two LTC3896 ICs to produce a two-phase inverting regulator. Pay particular attention to the RUN, PLLIN and GND connections on the slave LTC3896.

The PHASMD pin is used to adjust the phase of the CLKOUT signal. Pulling this pin to V_{OUT}^- forces CLKOUT to be out-of-phase 90° with respect to TG. Connecting this pin to $INTV_{CC}$ forces CLKOUT to be out of phase 120° with respect to TG. Floating this pin forces CLKOUT to be out-of-phase 180° with respect to TG.

V_{IN} + $|V_{OUT}^-|$ Overvoltage Lockout (OVLO Pin)

The LTC3896 implements a protection feature that inhibits switching when the total voltage between input and output (V_{IN} + $|V_{OUT}^-|$) rises above a programmable operating range. By using a resistor divider from the input supply to V_{OUT}^-, the OVLO pin serves as a precise voltage monitor. Switching is disabled when the OVLO pin rises above 1.2V with respect to V_{OUT}^-, which can be configured to limit switching to a specific range of total voltage applied to the external MOSFETs.

When switching is disabled, the LTC3896 can safely sustain V_{IN} + $|V_{OUT}^-|$ voltages up to the absolute maximum rating of 150V. Overvoltage events trigger a soft-start reset, which results in a graceful recovery from an input supply transient.

Negative Output Overvoltage Protection

An overvoltage comparator guards against transient overshoots as well as other more serious conditions that may overvoltage (in the negative direction) the output. When the V_{FB} pin rises by more than 10% above its regulation point of 0.800V with respect to V_{OUT}^-, the top MOSFET is turned off and the bottom MOSFET is turned on until the negative overvoltage condition is cleared.

OPERATION

Power Good Pin

The PGOOD pin is connected to an open drain of an internal N-channel MOSFET with its drain connected to GND. The MOSFET turns on and pulls the PGOOD pin low when the V_{FB} pin voltage is not within ±10% of the 0.8V reference voltage with respect to V_{OUT}^-. The PGOOD pin is also pulled low when the RUN pin is low (shut down). When the V_{FB} pin voltage is within the ±10% requirement, the MOSFET is turned off and the pin is allowed to be pulled up by an external resistor to a source no greater than 6V with respect to GND. PGOOD is referenced to GND to allow it to interface with other external true ground-referenced components with no level shifters needed.

Foldback Current

When the output voltage ($|V_{OUT}^-|$) falls to less than 70% of its nominal level, foldback current limiting is activated, progressively lowering the peak current limit in proportion to the severity of the overcurrent or short-circuit condition. Foldback current limiting is disabled during the soft-start interval (as long as the V_{FB} voltage is keeping up with the SS voltage). Foldback current limiting is intended to limit power dissipation during overcurrent and short-circuit fault conditions. Note that the LTC3896 continuously monitors the inductor current and prevents current runaway under all conditions.

Regulator Shutdown (REGSD)

High input voltage applications typically require using the $EXTV_{CC}$ LDO to keep power dissipation low. Fault conditions where the $EXTV_{CC}$ LDO becomes disabled ($EXTV_{CC}$ below the switchover threshold) for an extended period of time could result in overheating of the IC (or overheating the external N-channel MOSFET if the NDRV LDO is used). In the cases where $EXTV_{CC}$ is powered from the output, this event could happen during overload conditions such as a V_{OUT}^- short to ground. The LTC3896 includes a regulator shutdown (REGSD) feature that shuts down the regulator to substantially reduce power dissipation and the risk of overheating during such events.

The REGSD circuit monitors the $EXTV_{CC}$ LDO and the SS pin to determine when to shut down the regulator. Refer to the timing diagram in Figure 1. Whenever SS is above 2.2V with respect to V_{OUT}^- *and* the $EXTV_{CC}$ LDO is not switched over (the $EXTV_{CC}$ pin is below the switchover threshold), the internal 10µA pull-up current on SS turns off and a 5µA pull-down current turns on, discharging SS. Once SS discharges to 2.0V *and* the $EXTV_{CC}$ pin remains below the $EXTV_{CC}$ switchover threshold, the pull-down current reduces to 1µA and the regulator shuts down, eliminating all DRV_{CC} switching current. Switching stays off until the SS pin discharges to approximately 200mV, at which point the 10µA pull-up current turns back on and the regulator re-enables switching. If the short-circuit persists, the regulator cycles on and off at a low duty cycle interval of about 12%.

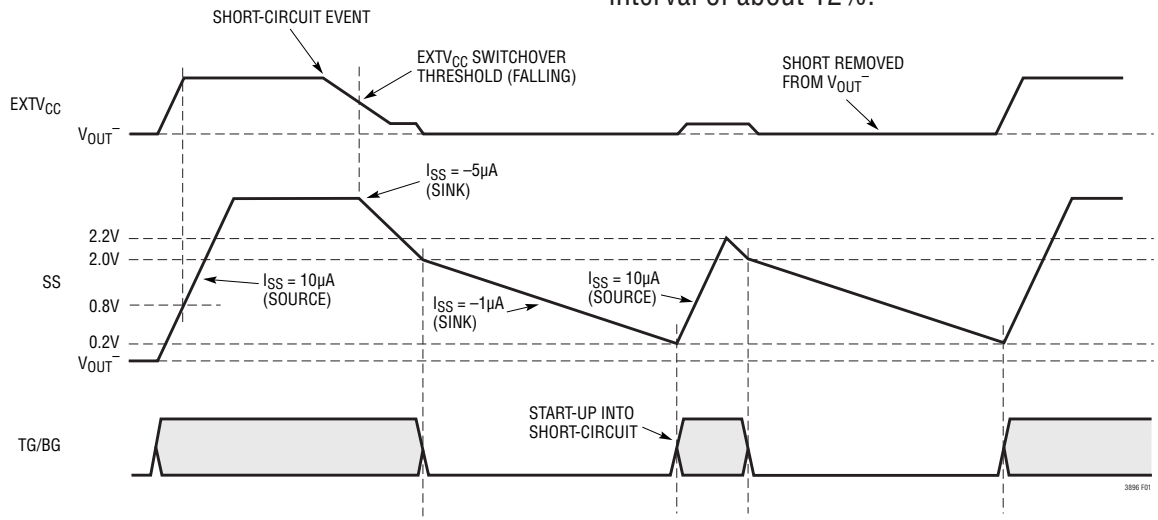


Figure 1. Regulator Shutdown Operation

APPLICATIONS INFORMATION

The Typical Application on the first page is a basic LTC3896 application circuit. LTC3896 can be configured to use either DCR (inductor resistance) sensing or low value resistor sensing. The choice between the two current sensing schemes is largely a design trade-off between cost, power consumption and accuracy. DCR sensing is becoming popular because it saves expensive current sensing resistors and is more power efficient, especially in high current applications. However, current sensing resistors provide the most accurate current limits for the controller. Other external component selection is driven by the load requirement, and begins with the selection of R_{SENSE} (if R_{SENSE} is used) and inductor value. Next, the power MOSFETs are selected. Finally, input and output capacitors are selected.

Current Limit Programming

The ILIM pin is a three-state logic input which sets the maximum current limit of the controller. When ILIM is tied to V_{OUT}^-, the maximum current limit threshold voltage of the current comparator is programmed to be 50mV. When ILIM is floated, the maximum current limit threshold is 75mV. When ILIM is tied to $INTV_{CC}$, the maximum current limit threshold is set to 100mV.

SENSE+ and SENSE– Pins

The $SENSE^+$ and $SENSE^-$ pins are the inputs to the current comparator. The common mode voltage range on these pins is 0V to 65V with respect to V_{OUT}^- (absolute maximum), enabling the LTC3896 to regulate output voltages down to a nominal set point of –60V with respect to GND (allowing margin for tolerances and transients). The $SENSE^+$ pin is high impedance over the full common mode range, drawing at most ±1µA. This high impedance allows the current comparators to be used with inductor DCR sensing. The impedance of the $SENSE^-$ pin changes depending on the common mode voltage. When $SENSE^-$ is less than $INTV_{CC}$ – 0.5V (with respect to V_{OUT}^-), a small current of less than 1µA flows out of the pin. When $SENSE^-$ is above $INTV_{CC}$ + 0.5V, a higher current (≈850µA) flows into the pin. Between $INTV_{CC}$ – 0.5V and $INTV_{CC}$ + 0.5V, the current transitions from the smaller current to the higher current.

Filter components mutual to the sense lines should be placed close to the LTC3896, and the sense lines should run close together to a Kelvin connection underneath the current sense element (shown in Figure 2). Sensing current elsewhere can effectively add parasitic inductance and capacitance to the current sense element, degrading the information at the sense terminals and making the programmed current limit unpredictable. If DCR sensing is used (Figure 4), resistor R1 should be placed close to the switching node, to prevent noise from coupling into sensitive small-signal nodes.

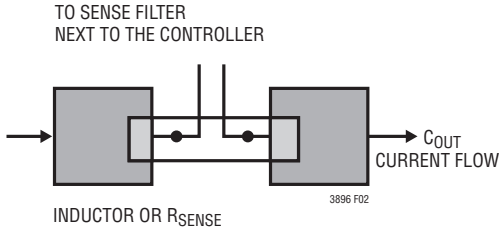


Figure 2. Sense Lines Placement with Inductor or Sense Resistor

Low Value Resistor Current Sensing

A typical sensing circuit using a discrete resistor is shown in Figure 3. R_{SENSE} is chosen based on the required output current.

The current comparator has a maximum threshold $V_{SENSE(MAX)}$ determined by the ILIM setting. The current comparator threshold voltage sets the peak of the inductor current, yielding a maximum average output current, I_{MAX}, equal to the peak value less half the peak-to-peak ripple current, ΔI_L. To calculate the sense resistor value, use the equation:

$$R_{SENSE} = \frac{V_{SENSE(MAX)}}{I_{MAX} + \frac{\Delta I_L}{2}}$$

Normally in high duty cycle conditions, the maximum output current level will be reduced due to the internal compensation required to meet stability criterion operating at greater than 50% duty factor. The LTC3896, however, uses a proprietary circuit to nullify the effect of slope compensation on the current limit performance.

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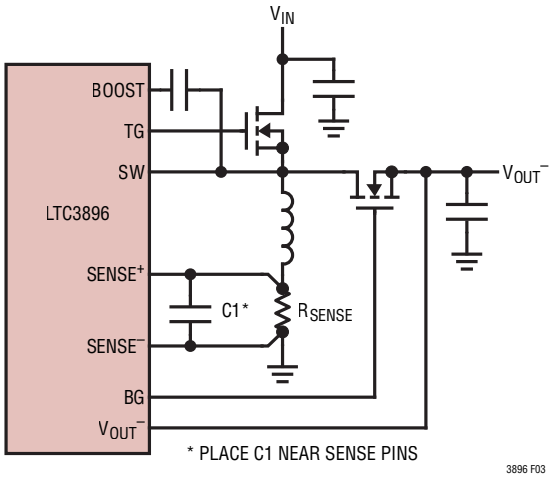


Figure 3. Using a Resistor to Sense Current

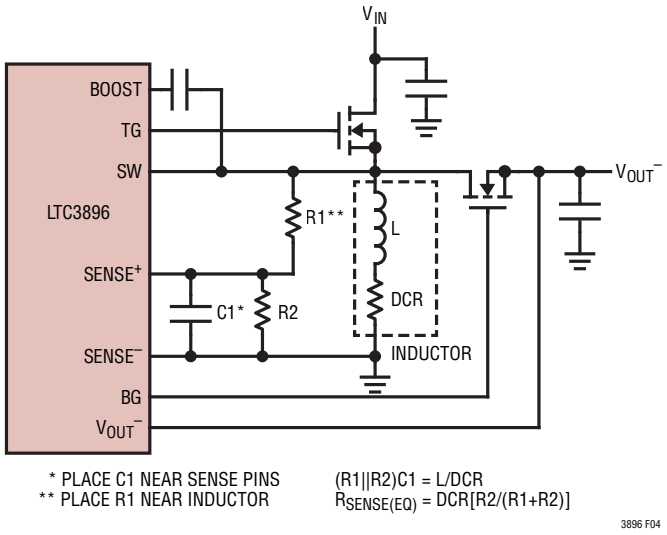


Figure 4. Using the Inductor DCR to Sense Current

Inductor DCR Sensing

For applications requiring the highest possible efficiency at high load currents, the LTC3896 is capable of sensing the voltage drop across the inductor DCR, as shown in Figure 4. The DCR of the inductor represents the small amount of DC winding resistance of the copper, which can be less than 1mΩ for today's low value, high current inductors. In a high current application requiring such an inductor, power loss through a sense resistor would cost several points of efficiency compared to inductor DCR sensing.

If the external (R1||R2) • C1 time constant is chosen to be exactly equal to the L/DCR time constant, the voltage drop across the external capacitor is equal to the drop across the inductor DCR multiplied by R2/(R1 + R2). R2 scales the voltage across the sense terminals for applications where the DCR is greater than the target sense resistor value. To properly dimension the external filter components, the DCR of the inductor must be known. It can be measured using a good RLC meter, but the DCR tolerance is not always the same and varies with temperature; consult the manufacturers' data sheets for detailed information.

Using the inductor ripple current value from the Inductor Value Calculation section, the target sense resistor value is:

$$R_{SENSE(EQUIV)} = \frac{V_{SENSE(MAX)}}{I_{MAX} + \frac{\Delta I_L}{2}}$$

To ensure that the application will deliver full load current over the full operating temperature range, choose the minimum value for $V_{SENSE(MAX)}$ in the Electrical Characteristics table.

Next, determine the DCR of the inductor. When provided, use the manufacturer's maximum value, usually given at 20°C. Increase this value to account for the temperature coefficient of copper resistance, which is approximately 0.4%/°C. A conservative value for $T_{L(MAX)}$ is 100°C.

To scale the maximum inductor DCR to the desired sense resistor value (R_D), use the divider ratio:

$$R_D = \frac{R_{SENSE(EQUIV)}}{DCR_{MAX} \text{ at } T_{L(MAX)}}$$

C1 is usually selected to be in the range of 0.1µF to 0.47µF. This forces R1|| R2 to around 2k, reducing error that might have been caused by the SENSE+ pin's ±1µA current.

The equivalent resistance R1|| R2 is scaled to the temperature inductance and maximum DCR:

$$R1||R2 = \frac{L}{(DCR \text{ at } 20°C) \bullet C1}$$

The values for R1 and R2 are:

$$R1 = \frac{R1||R2}{R_D};\ R2 = \frac{R1 \bullet R_D}{1 - R_D}$$

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The maximum power loss in R1 is related to duty cycle, and will occur in continuous mode at the maximum input voltage:

$$P_{LOSS}\ R1 = \frac{V_{IN(MAX)} \bullet |V_{OUT}^{-}|}{R1}$$

Ensure that R1 has a power rating higher than this value. If high efficiency is necessary at light loads, consider this power loss when deciding whether to use DCR sensing or sense resistors. Light load power loss can be modestly higher with a DCR network than with a sense resistor, due to the extra switching losses incurred through R1. However, DCR sensing eliminates a sense resistor, reduces conduction losses and provides higher efficiency at heavy loads. Peak efficiency is about the same with either method.

Inductor Value Calculation

The operating frequency and inductor selection are interrelated in that higher operating frequencies allow the use of smaller inductor and capacitor values. So why would anyone ever choose to operate at lower frequencies with larger components? The answer is efficiency. A higher frequency generally results in lower efficiency because of MOSFET switching and gate charge losses. In addition to this basic trade-off, the effect of inductor value on ripple current and low current operation must also be considered.

The inductor value has a direct effect on ripple current. The inductor ripple current, ΔI_L, decreases with higher inductance or higher frequency:

$$\Delta I_L = \frac{1}{(f)(L)} V_{IN} \left(\frac{|V_{OUT}^{-}|}{V_{IN} + |V_{OUT}^{-}|} \right)$$

Accepting larger values of ΔI_L allows the use of low inductances, but results in higher output voltage ripple and greater core losses. A reasonable starting point for setting ripple current is ΔI_L = 0.3(I_{MAX}). The maximum ΔI_L occurs at the maximum input voltage.

The inductor value also has secondary effects. The transition to Burst Mode operation begins when the average inductor current required results in a peak current below the burst clamp, which can be programmed between 10% and 60% of the current limit determined by R_{SENSE}. (For more information see the Burst Clamp Programming section.) Lower inductor values (higher ΔI_L) will cause this to occur at lower load currents, which can cause a dip in efficiency in the upper range of low current operation. In Burst Mode operation, lower inductance values will cause the burst frequency to decrease.

Inductor Core Selection

Once the value for L is known, the type of inductor must be selected. High efficiency converters generally cannot afford the core loss found in low cost powdered iron cores, forcing the use of more expensive ferrite or molypermalloy cores. Actual core loss is independent of core size for a fixed inductor value, but it is very dependent on inductance value selected. As inductance increases, core losses go down. Unfortunately, increased inductance requires more turns of wire and therefore copper losses will increase.

Ferrite designs have very low core loss and are preferred for high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates hard, which means that inductance collapses abruptly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current and consequent output voltage ripple. Do not allow the core to saturate!

Power MOSFET Selection

Two external power MOSFETs must be selected for the LTC3896 controller: one N-channel MOSFET for the top (main) switch, and one N-channel MOSFET for the bottom (synchronous) switch.

The peak-to-peak drive levels are set by the DRV_{CC} voltage. This voltage can range from 5V to 10V depending on configuration of the DRVSET pin. Therefore, both logic-level and standard-level threshold MOSFETs can be used in most applications depending on the programmed DRV_{CC} voltage. Pay close attention to the BV_{DSS} specification for the MOSFETs as well.

The LTC3896's ability to adjust the gate drive level between 5V to 10V (OPTI-DRIVE) allows an application circuit to be precisely optimized for efficiency. When adjusting the gate drive level, the final arbiter is the total input current for the regulator. If a change is made and the input

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current decreases, then the efficiency has improved. If there is no change in input current, then there is no change in efficiency.

Selection criteria for the power MOSFETs include the on-resistance $R_{DS(ON)}$, Miller capacitance C_{MILLER}, input voltage and maximum output current. Miller capacitance, C_{MILLER}, can be approximated from the gate charge curve usually provided on the MOSFET manufacturers' data sheet. C_{MILLER} is equal to the increase in gate charge along the horizontal axis while the curve is approximately flat divided by the specified change in V_{DS}. This result is then multiplied by the ratio of the application applied V_{DS} to the gate charge curve specified V_{DS}. When the IC is operating in continuous mode the duty cycles for the top and bottom MOSFETs are given by:

$$\text{Main Switch Duty Cycle} = \frac{|V_{OUT}^-|}{V_{IN}+|V_{OUT}^-|}$$

$$\text{Synchronous Switch Duty Cycle} = \frac{V_{IN}}{V_{IN}+|V_{OUT}^-|}$$

For a given V_{OUT}^-, the maximum duty cycle occurs at minimum V_{IN}.

The MOSFET power dissipations at maximum output current are given by:

$$P_{MAIN} = \frac{|V_{OUT}^-|\left(V_{IN}+|V_{OUT}^-|\right)}{V_{IN}^2}\left(I_{OUT(MAX)}\right)^2(1+\delta)$$

$$\bullet R_{DS(ON)} + \frac{\left(V_{IN}+|V_{OUT}^-|\right)^3}{V_{IN}}\left(\frac{I_{OUT(MAX)}}{2}\right)(R_{DR})(C_{MILLER})$$

$$\bullet\left[\frac{1}{V_{DRVCC}-V_{THMIN}}+\frac{1}{V_{THMIN}}\right](f)$$

$$P_{SYNC} = \frac{V_{IN}+|V_{OUT}^-|}{V_{IN}}\left(I_{OUT(MAX)}\right)^2(1+\delta)R_{DS(ON)}$$

where δ is the temperature dependency of $R_{DS(ON)}$ and R_{DR} (approximately 2Ω) is the effective driver resistance at the MOSFET's Miller threshold voltage. V_{THMIN} is the typical MOSFET minimum threshold voltage.

Both MOSFETs have I^2R losses while the main N-channel equations include an additional term for transition losses, which are highest at high input to output differential voltages. For $(V_{IN} + |V_{OUT}^-|) < 20V$ the high current efficiency generally improves with larger MOSFETs, while for $(V_{IN} + |V_{OUT}^-|) > 20V$ the transition losses rapidly increase to the point that the use of a higher $R_{DS(ON)}$ device with lower C_{MILLER} actually provides higher efficiency. The synchronous MOSFET losses are greatest at high input voltage when the top switch duty factor is low or during a short-circuit when the synchronous switch is on close to 100% of the period.

The term $(1+\delta)$ is generally given for a MOSFET in the form of a normalized $R_{DS(ON)}$ vs temperature curve, but $\delta = 0.005/°C$ can be used as an approximation for low voltage MOSFETs.

C_{IN} and C_{OUT} Selection

The input and output capacitance, C_{IN}/C_{OUT}, are required to filter the square wave current through the top and bottom MOSFETs respectively. Use a low ESR capacitor sized to handle the maximum RMS current.

$$I_{CIN(RMS)} = I_{COUT(RMS)} = I_{OUT} \bullet \sqrt{\frac{|V_{OUT}^-|}{V_{IN}}}$$

The formula shows that the RMS current is greater than the maximum I_{OUT} when $|V_{OUT}^-|$ is greater than V_{IN}. Choose capacitors with higher RMS rating with sufficient margin. Note that ripple current ratings from capacitor manufacturers are often based on only 2000 hours of life, which makes it advisable to derate the capacitor.

The selection of C_{OUT} is primarily determined by the ESR required to minimize voltage ripple and load step transients. The ΔV_{OUT} is approximately bounded by:

$$\Delta V_{OUT}^- \le I_{L(PEAK)} \bullet ESR + \frac{I_{OUT}}{f \bullet C_{OUT}}$$

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where $I_{L(PEAK)}$ is the peak inductor current and it's given as:

$$I_{L(PEAK)} = \frac{I_{OUT}(V_{IN}+|V_{OUT}^-|)}{V_{IN}} + \frac{V_{IN}\bullet|V_{OUT}^-|}{2\bullet L\bullet f\bullet(V_{IN}+|V_{OUT}^-|)}$$

Since $I_{L(PEAK)}$ reach its maximum values at minimum V_{IN}, the output voltage ripple is highest at minimum V_{IN} and maximum I_{OUT}. Typically, once the ESR requirement is satisfied, the capacitance is adequate for filtering and has the necessary RMS current rating.

Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirements. Dry tantalum, specialty polymer, aluminum electrolytic and ceramic capacitors are all available in surface mount packages. Specialty polymer capacitors offer very low ESR but have lower specific capacitance than other types. Tantalum capacitors have the highest specific capacitance, but it is important to only use types that have been surge tested for use in switching power supplies. Aluminum electrolytic capacitors have significantly higher ESR, but can be used in cost-sensitive applications provided that consideration is given to ripple current ratings and long-term reliability. Ceramic capacitors have excellent low ESR characteristics but can have a high voltage coefficient and audible piezoelectric effects.

The high Q of ceramic capacitors with trace inductance can also lead to significant ringing. When used as input capacitors, care must be taken to ensure that ringing from inrush currents and switching does not pose an overvoltage hazard to the power switch and controller. To dampen input voltage transients, add a small 5µF to 40µF aluminum electrolytic capacitor with an ESR in the range of 0.5Ω to 2Ω. High performance through-hole capacitors may also be used, but an additional ceramic capacitor in parallel is recommended to reduce the effect of lead inductance.

During shutdown and startup conditions, the output capacitor can experience a small reverse voltage (a positive voltage on V_{OUT}^- with respect to GND) as the result of IC quiescent current and/or capacitor charging current flowing into the V_{OUT}^- node while V_{OUT}^- is not being actively driven negative by the converter. This reverse voltage, which is typically clamped to a diode drop above ground by the reverse diode of the external bottom MOSFET, should be carefully considered when choosing the output capacitor. Certain polarized capacitors can be permanently damaged given enough reverse voltage. If considering a polarized capacitor at the output, always consult the manufacturer if there is any question regarding reverse voltage on the capacitor. Alternatively, an all ceramic capacitor solution at the output would make the reverse voltage a non-issue

Setting Output Voltage

The LTC3896 output voltage is set by an external feedback resistor divider carefully placed across the output, as shown in Figure 5. The regulated output voltage is determined by:

$$V_{OUT}^- = -0.8V\left(1+\frac{R_B}{R_A}\right)$$

To improve the frequency response, a feedforward capacitor, C_{FF}, may be used. Great care should be taken to route the V_{FB} line away from noise sources, such as the inductor or the SW line.

The LTC3896 also has the option to be programmed to a fixed –5V or –3.3V output through control of the VPRG pin. Figure 6 shows how the V_{FB} pin is used to sense ground in fixed output mode. Tying VPRG to $INTV_{CC}$ or V_{OUT}^- programs V_{OUT}^- to –5V or –3.3V, respectively. Floating VPRG sets V_{OUT}^- to adjustable output mode using external resistors.

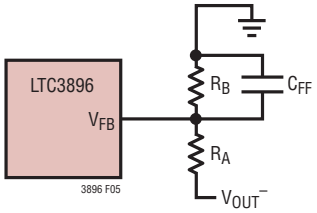


Figure 5. Setting Adjustable Output Voltage

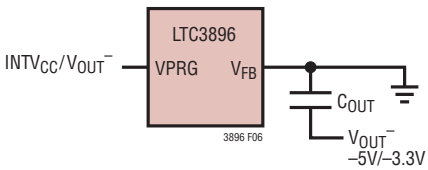


Figure 6. Setting Output to Fixed –5V/–3.3V Voltage

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RUN Pin

The LTC3896 is enabled using the RUN pin. It has a rising threshold of 1.2V with respect to GND with 80mV of hysteresis. The RUN pin is referenced to the GND pin, allowing the LTC3896 to be used with a true ground-referenced external signal or logic with no level shifters needed. Pulling the RUN pin below 1.12V shuts down the main control loop. Pulling it below 0.7V disables the controller and most internal circuits, including the DRV_{CC} and $INTV_{CC}$ LDOs. In this state the LTC3896 draws only 10µA of quiescent current.

The RUN pin is high impedance below 3V and must be externally pulled up/down or driven directly by logic. The RUN pin can tolerate up to 150V (absolute maximum), so it can be conveniently tied to V_{IN} in always-on applications where the controller is enabled continuously and never shut down. Above 3V, the RUN pin has approximately a 15MΩ impedance to an internal 3V clamp.

The RUN pin can be configured as an undervoltage (UVLO) lockout on the V_{IN} supply with a resistor divider from V_{IN} to GND, as shown in Figure 7.

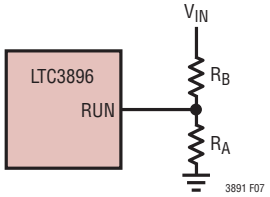


Figure 7. Using the RUN Pin as a UVLO

The rising and falling UVLO thresholds, referenced to ground, are calculated using the RUN pin thresholds:

$$V_{UVLO(RISING)} = 1.2V\left(1+\frac{R_B}{R_A}\right)$$

$$V_{UVLO(FALLING)} = 1.12V\left(1+\frac{R_B}{R_A}\right)$$

Overvoltage Lockout Pin (OVLO)

The LTC3896 implements a protection feature that inhibits switching when the total voltage between input and output (V_{IN} + $|V_{OUT^-}|$) rises above a programmable operating range. By using a resistor divider from the input supply to V_{OUT^-} (Figure 8), the OVLO pin serves as a precise voltage monitor. Switching is disabled when the OVLO pin rises above 1.2V with respect to V_{OUT^-}, which can be configured to limit switching to a specific range of total voltage applied to the external switching MOSFETs.

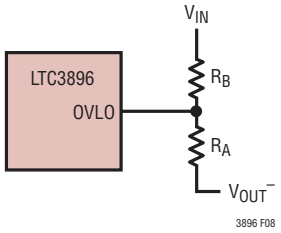


Figure 8. Programming the OVLO Pin

The rising and falling OVLO thresholds are calculated using the OVLO pin thresholds:

$$V_{OVLO(RISING)} = 1.2V\left(1+\frac{R_B}{R_A}\right)$$

$$V_{OVLO(FALLING)} = 1.1V\left(1+\frac{R_B}{R_A}\right)$$

where V_{OVLO} is the total voltage between V_{IN} and V_{OUT^-}.

Soft-Start (SS) Pin

The start-up of V_{OUT^-} is controlled by the voltage on the SS pin. When the voltage on the SS pin is less than the internal 0.8V reference (with respect to V_{OUT^-}), the LTC3896 regulates the V_{FB} pin voltage to the voltage on the SS pin instead of the internal reference. The SS pin can be used to program an external soft-start function.

Soft-start is enabled by simply connecting a capacitor from the SS pin to V_{OUT^-}, as shown in Figure 9. An internal 10µA current source charges the capacitor, providing a linear ramping voltage at the SS pin with respect to V_{OUT^-}. The LTC3896 will regulate its feedback voltage (and hence

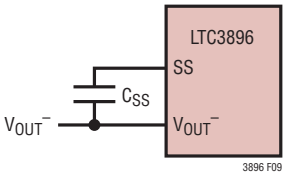


Figure 9. Using the SS Pin to Program Soft-Start

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V_{OUT}^-) according to the voltage on the SS pin, allowing V_{OUT}^- to fall smoothly from 0V to its final regulated value. The total soft-start time will be approximately:

$$t_{SS} = C_{SS} \bullet \frac{0.8V}{10\mu A}$$

The SS pin also controls the timing of the regulator shutdown (REGSD) feature (as discussed in Regulator Shutdown of the Operation section). If the application does not require the use of the $EXTV_{CC}$ LDO (the $EXTV_{CC}$ pin is tied to V_{OUT}^-), the REGSD feature must be defeated with a pull-up resistor between SS and $INTV_{CC}$, as shown in Figure 10. Any resistor 330kΩ or smaller between SS and $INTV_{CC}$ defeats the 5µA pull-down current on SS that turns on once SS reaches 2.2V with respect to V_{OUT}^- (with the $EXTV_{CC}$ LDO not enabled), preventing SS from discharging to 2.0V and shutting down the regulator. Note the current through this pull-up resistor adds to the internal 10µA SS pull-up current at start-up, causing the total soft-start time to be shorter than what it is calculated without the pull-up resistor. The total soft-start time with the pull-up resistor is approximately:

$$t_{SS} \approx C_{SS} \bullet \frac{0.8V}{\left(10\mu A + \frac{4.6V}{R_{SS}}\right)}$$

where R_{SS} is the value of the resistor between the SS and $INTV_{CC}$ pins.

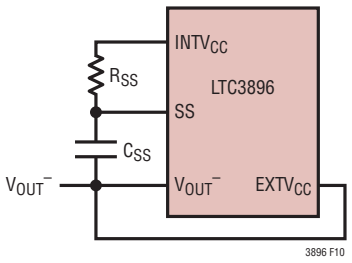


Figure 10. Using the SS Pin to Program Soft-Start with $EXTV_{CC}$ Unused/Tied to V_{OUT}^-

DRV_{CC} Regulators (OPTI-DRIVE)

The LTC3896 features three separate low dropout linear regulators (LDO) that can supply power at the DRV_{CC} pin. The internal V_{IN} LDO uses an internal P-channel pass device between the V_{IN} and DRV_{CC} pins. The internal $EXTV_{CC}$ LDO uses an internal P-channel pass device between the $EXTV_{CC}$ and DRV_{CC} pins. The NDRV LDO utilizes the NDRV pin to drive the gate of an external N-channel MOSFET acting as a linear regulator with its drain connected to V_{IN}. Note the return path for the DRV_{CC} regulators is the V_{OUT}^- pin.

The NDRV LDO provides an alternative method to supply power to DRV_{CC} from the input supply without dissipating the power inside the LTC3896 IC. It includes an internal charge pump that allows NDRV to be driven above the V_{IN} supply, allowing for low dropout performance. The V_{IN} LDO has a slightly lower regulation point than the NDRV LDO, such that all DRV_{CC} current flows through the external N-channel MOSFET (and not through the internal P-channel pass device) once DRV_{CC} reaches regulation.

When laying out the PC board, care should be taken to route NDRV away from any switching nodes, especially SW, TG, and BOOST. Coupling to the NDRV node could cause its voltage to collapse and the NDRV LDO to lose regulation. If this occurs, the internal V_{IN} LDO would take over and maintain DRV_{CC} voltage at a slightly lower regulation point. However, internal heating of the IC would become a concern.

High frequency noise on the drain of the external NFET could also couple into the NDRV node (through the gate-to-drain capacitance of the NDRV NFET) and adversely affect NDRV regulation. The following are methods that could mitigate this potential issue (refer to Figure 11a).

1. Add local decoupling capacitors to V_{OUT}^- right next to the drain of the external NDRV NFET in the PCB layout.
2. Insert a resistor (~100Ω) in series with the gate of the NDRV NFET.
3. Insert a small capacitor (~1nF) between the gate and source of the NDRV NFET.

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When testing the application circuit, be sure the NDRV voltage does not collapse over the entire input voltage and output current operating range of the buck regulator.

If the NDRV LDO is not being used, connect the NDRV pin to DRV_{CC} (Figure 11b).

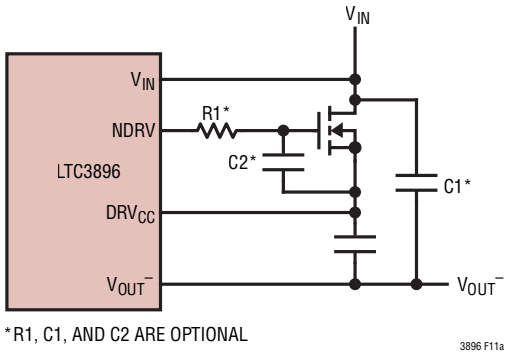


Figure 11a. Configuring the NDRV LDO

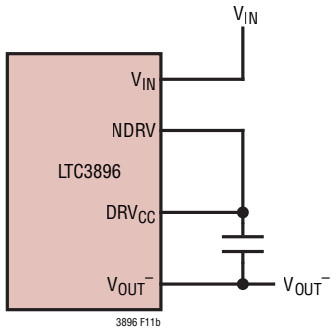


Figure 11b. Disabling the NDRV LDO

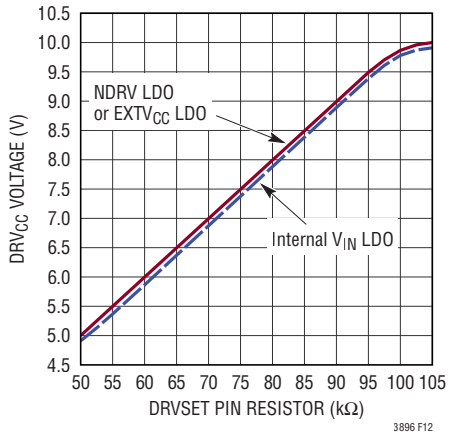


Figure 12. Relationship Between DRV_{CC} Voltage and Resistor Value at DRVSET Pin

The DRV_{CC} supply is regulated between 5V to 10V with respect to V_{OUT}^-, depending on how the DRVSET pin is set. The internal V_{IN} and $EXTV_{CC}$ LDOs can supply a peak current of at least 50mA. The DRV_{CC} pin must be bypassed to V_{OUT}^- with a minimum of 4.7µF ceramic capacitor. Good bypassing is needed to supply the high transient currents required by the MOSFET gate drivers.

The DRVSET pin programs the DRV_{CC} supply voltage and the DRVUV pin selects different DRV_{CC} UVLO and $EXTV_{CC}$ switchover threshold voltages. Table 1 summarizes the different DRVSET pin configurations along with the voltage settings that go with each configuration. Table 2 summarizes the different DRVUV pin settings. Tying the DRVSET pin to $INTV_{CC}$ programs DRV_{CC} to 10V. Tying the DRVSET pin to V_{OUT}^- programs DRV_{CC} to 6V. Placing a 50kΩ to 100kΩ resistor between DRVSET and V_{OUT}^- the programs DRV_{CC} between 5V to 10V, as shown in Figure 12.

Table 1

DRVSET PIN	DRV_{CC} VOLTAGE
V_{OUT}^-	6V
$INTV_{CC}$	10V
Resistor to V_{OUT}^- 50k to 100k	5V to 10V

Table 2

DRVUV PIN	DRVCC UVLO RISING/ FALLING THRESHOLDS	$EXTV_{CC}$ SWITCHOVER RISING/FALLING THRESHOLD
V_{OUT}^-	4.0V/3.8V	4.7V/4.45V
$INTV_{CC}$	7.5V/6.7V	7.7V/7.45V

All voltages with respect to V_{OUT}^-

Large $V_{IN} + |V_{OUT}^-|$ applications in which large MOSFETs are being driven at high frequencies may cause the maximum junction temperature rating for the LTC3896 to be exceeded. The DRV_{CC} current, which is dominated by the gate charge current, may be supplied by the V_{IN} LDO, NDRV LDO or the $EXTV_{CC}$ LDO. When the voltage on the $EXTV_{CC}$ pin is less than its switchover threshold (4.7V or 7.7V with respect to V_{OUT}^-, as determined by the DRVUV pin described above), the V_{IN} and NDRV LDOs are enabled. Power dissipation in this case is highest and is equal to $(V_{IN} + |V_{OUT}^-|) \bullet IDRV_{CC}$. If the NDRV LDO is not being used, this power is dissipated inside the IC. The gate charge current is dependent on operating frequency

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as discussed in the Efficiency Considerations section. The junction temperature can be estimated by using the equations given in Note 2 of the Electrical Characteristics. For example, if DRV_{CC} is set to 6V, the DRV_{CC} current is limited to less than 49mA if $V_{IN} + |V_{OUT^-}|$ is 40V when not using the $EXTV_{CC}$ or NDRV LDOs at a 70°C ambient temperature:

$$T_J = 70°C + (49mA)(40V)(28°C/W) = 125°C$$

To prevent the maximum junction temperature from being exceeded, the V_{IN} supply current must be checked while operating in forced continuous mode (MODE = $INTV_{CC}$) at maximum $V_{IN} + |V_{OUT^-}|$.

When the voltage applied to $EXTV_{CC}$ rises above its switchover threshold (with respect to V_{OUT^-}), the V_{IN} and NDRV LDOs are turned off and the $EXTV_{CC}$ LDO is enabled. The $EXTV_{CC}$ LDO remains on as long as the voltage applied to $EXTV_{CC}$ remains above the switchover threshold minus the comparator hysteresis. The $EXTV_{CC}$ LDO attempts to regulate the DRV_{CC} voltage to the voltage as programmed by the DRVSET pin, so while $EXTV_{CC}$ is less than this voltage, the LDO is in dropout and the DRV_{CC} voltage is approximately equal to $EXTV_{CC}$. When $EXTV_{CC}$ with respect to V_{OUT^-} is greater than the programmed DRV_{CC} voltage, up to an absolute maximum of 14V, DRV_{CC} is regulated to the programmed voltage.

Using the $EXTV_{CC}$ LDO allows the MOSFET driver and control power to be derived from the output (4.7V/7.7V ≤ $|V_{OUT^-}| \leq$ 14V) during normal operation and from the V_{IN} or NDRV LDO when the output is out of regulation (e.g., start-up, short-circuit). If more current is required through the $EXTV_{CC}$ LDO than is specified, an external Schottky diode can be added between the $EXTV_{CC}$ and DRV_{CC} pins. In this case, do not apply more than 10V between the $EXTV_{CC}$ and V_{OUT^-} pins and make sure that $EXTV_{CC} \leq V_{IN}$.

Significant efficiency and thermal gains can be realized by powering DRV_{CC} from the output using the $EXTV_{CC}$ LDO, since the V_{IN} current resulting from the driver and control currents will be scaled by a factor of (Duty Cycle)/(Switcher Efficiency).

For –5V to –14V regulator outputs, this means connecting the $EXTV_{CC}$ pin directly to ground. Tying the $EXTV_{CC}$ pin to ground with an –8.5V output supply reduces the junction temperature in the previous example from 125°C to:

$$T_J = 70°C + (49mA)(8.5V)(28°C/W) = 82°C$$

However, for –3.3V and other low voltage outputs, additional circuitry is required to derive DRV_{CC} power from the output.

The following list summarizes the four possible connections for $EXTV_{CC}$:

1. $EXTV_{CC}$ tied to V_{OUT^-}. This will cause DRV_{CC} to be powered from the internal V_{IN} or NDRV LDO resulting in an efficiency penalty of up to 10% at high input voltages. If $EXTV_{CC}$ is tied to V_{OUT^-}, the REGSD feature must be defeated with a pull-up resistor 330kΩ or smaller between SS and $INTV_{CC}$.
2. $EXTV_{CC}$ connected directly to ground. This is the normal connection for a –5V to –14V regulator and provides the highest efficiency.
3. $EXTV_{CC}$ connected to an external supply. If an external supply is available in the range 5V to 14V above V_{OUT^-}, it may be used to power $EXTV_{CC}$ providing it is compatible with the MOSFET gate drive requirements. Ensure that $EXTV_{CC} \leq V_{IN}$.
4. $EXTV_{CC}$ connected to ground through an external Zener diode. If the output voltage is more negative than –14V, a Zener diode can be used to drop the necessary voltage between ground and $EXTV_{CC}$ such that $EXTV_{CC}$ with respect to V_{OUT^-} remains below 14V (Figure 13). In this configuration, a bypass capacitor from $EXTV_{CC}$ to V_{OUT^-} of at least 0.1µF is recommended. An optional resistor between $EXTV_{CC}$ and V_{OUT^-} can be inserted to ensure adequate bias current through the Zener diode.

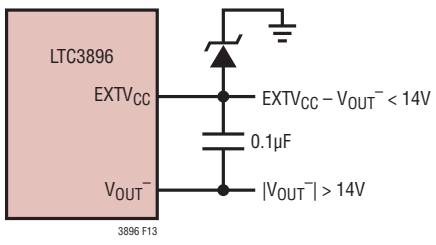


Figure 13. Using a Zener Diode Between $EXTV_{CC}$ and Ground

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$INTV_{CC}$ Regulator

An additional P-channel LDO supplies power at the $INTV_{CC}$ pin from the DRV_{CC} pin. Whereas DRV_{CC} powers the gate drivers, $INTV_{CC}$ powers much of the LTC3896's internal circuitry. The $INTV_{CC}$ supply must be bypassed with a 0.1µF ceramic capacitor to V_{OUT}^-. $INTV_{CC}$ is also used as a pull-up to bias other pins, such as MODE, ILIM, VPRG, etc.

Topside MOSFET Driver Supply (C_B)

An external bootstrap capacitor C_B connected to the BOOST pin supplies the gate drive voltage for the topside MOSFET. The LTC3896 features an internal 11Ω switch between DRV_{CC} and the BOOST pin. This internal switch eliminates the need for an external bootstrap diode between DRV_{CC} and BOOST. Capacitor C_B in the Functional Diagram is charged through this internal switch from DRV_{CC} when the SW pin is low. When the topside MOSFET is to be turned on, the driver places the C_B voltage across the gate-source of the MOSFET. This enhances the top MOSFET switch and turns it on. The switch node voltage, SW, rises to V_{IN} and the BOOST pin follows. With the topside MOSFET on, the BOOST voltage is above the input supply: $V_{BOOST} = V_{IN} + V_{DRVCC}$. The value of the boost capacitor, C_B, needs to be 100 times that of the total input capacitance of the topside MOSFET(s).

Burst Clamp Programming

Burst Mode operation is enabled if the voltage on the MODE pin is 0V (with respect to V_{OUT}^-) or in the range between 0.5V to 1V. The burst clamp, which sets the minimum peak inductor current, can be programmed by the MODE pin voltage. If the MODE pin is grounded, the burst clamp is set to 25% of the maximum sense voltage ($V_{SENSE(MAX)}$). A MODE pin voltage between 0.5V and 1V varies the burst clamp linearly between 10% and 60% of $V_{SENSE(MAX)}$ through the following equation:

$$\text{Burst Clamp} = \frac{V_{MODE} - 0.4V}{1V} \bullet 100$$

where V_{MODE} is the voltage on the MODE pin (with respect to V_{OUT}^-) and burst clamp is the percentage of $V_{SENSE(MAX)}$. The burst clamp level is determined by the desired amount of output voltage ripple at low output loads. As the burst clamp increases, the sleep time between pulses and the output voltage ripple increase.

The MODE pin is high impedance and V_{MODE} can be set by a resistor divider from the $INTV_{CC}$ pin to V_{OUT}^- (Figure 14a). Alternatively, the MODE pin can be tied directly to the V_{FB} pin to set the burst clamp to 40% (V_{MODE} = 0.8V), or through an additional divider resistor (R3). As shown in Figure 14b, this resistor can be placed below V_{FB} to program the burst clamp between 10% and 40% (V_{MODE}= 0.5V to 0.8V) or above V_{FB} to program the burst clamp between 40% and 60% (V_{MODE} = 0.8V to 1.0V).

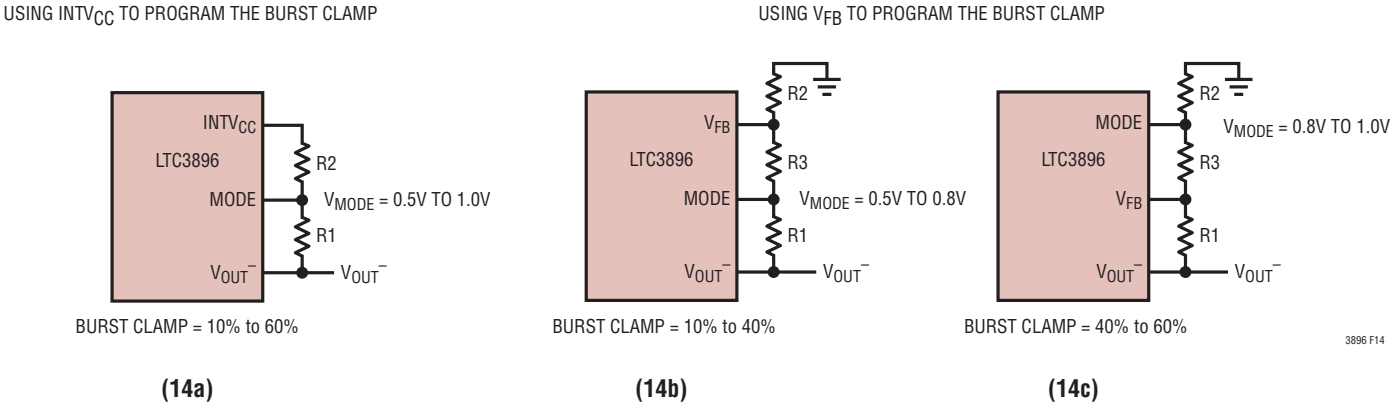


Figure 14. Programming the Burst Clamp

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Fault Conditions: Current Limit and Current Foldback

The LTC3896 includes current foldback to help limit load current when the output is overloaded or shorted to ground. If the output voltage ($|V_{OUT}^{-}|$) falls below 70% of its nominal level, then the maximum sense voltage is progressively lowered from 100% to 45% of its maximum selected value. Under short-circuit conditions with very low duty cycles, the LTC3896 will begin cycle skipping in order to limit the short-circuit current. In this situation the bottom MOSFET will be dissipating most of the power but less than in normal operation. The short-circuit ripple current is determined by the minimum on-time, $t_{ON(MIN)}$, of the LTC3896 (≈80ns), the input voltage and inductor value:

$$\Delta I_{L(SC)} = t_{ON(MIN)} \left(\frac{V_{IN}}{L} \right)$$

The resulting average short-circuit current is:

$$I_{SC} = 45\% \bullet I_{LIM(MAX)} - \frac{1}{2} \Delta I_{L(SC)}$$

Fault Conditions: Overtemperature Protection

At higher temperatures, or in cases where the internal power dissipation causes excessive self heating on chip, the overtemperature shutdown circuitry will shut down the LTC3896. When the junction temperature exceeds approximately 175°C, the overtemperature circuitry disables the DRV_{CC} LDO, causing the DRV_{CC} supply to collapse and effectively shutting down the entire LTC3896 chip. Once the junction temperature drops back to the approximately 155°C, the DRV_{CC} LDO turns back on. Long term overstress (T_J > 125°C) should be avoided as it can degrade the performance or shorten the life of the part.

Phase-Locked Loop and Frequency Synchronization

The LTC3896 has an internal phase-locked loop (PLL) comprised of a phase frequency detector, a lowpass filter, and a voltage-controlled oscillator (VCO). This allows the turn-on of the top MOSFET to be locked to the rising edge of an external clock signal applied to the PLLIN pin. The phase detector is an edge sensitive digital type that provides zero degrees phase shift between the external and internal oscillators. This type of phase detector does not exhibit false lock to harmonics of the external clock.

If the external clock frequency is greater than the internal oscillator's frequency, f_{OSC}, then current is sourced continuously from the phase detector output, pulling up the VCO input. When the external clock frequency is less than f_{OSC}, current is sunk continuously, pulling down the VCO input.

If the external and internal frequencies are the same but exhibit a phase difference, the current sources turn on for an amount of time corresponding to the phase difference. The voltage at the VCO input is adjusted until the phase and frequency of the internal and external oscillators are identical. At the stable operating point, the phase detector output is high impedance and the internal filter capacitor, CLP, holds the voltage at the VCO input.

Note that the LTC3896 can only be synchronized to an external clock whose frequency is within range of the LTC3896's internal VCO, which is nominally 55kHz to 1MHz. This is guaranteed to be between 75kHz and 850kHz. The LTC3896 is guaranteed to synchronize to an external clock that swings up to at least 2.8V and down to 0.5V or less with respect to GND.

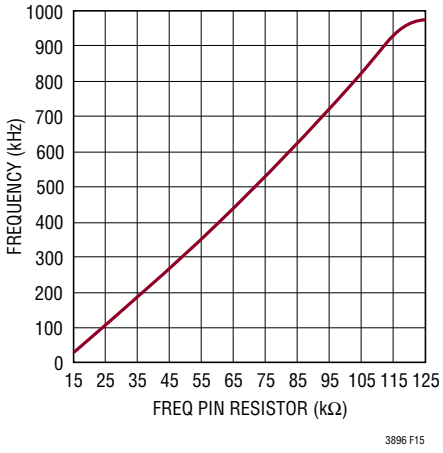


Figure 15. Relationship Between Oscillator Frequency and Resistor Value at the FREQ Pin

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Rapid phase-locking can be achieved by using the FREQ pin to set a free-running frequency near the desired synchronization frequency. The VCO's input voltage is prebiased at a frequency corresponding to the frequency set by the FREQ pin. Once prebiased, the PLL only needs to adjust the frequency slightly to achieve phase lock and synchronization. Although it is not required that the free-running frequency be near the external clock frequency, doing so will prevent the operating frequency from passing through a large range of frequencies as the PLL locks.

Table 3 summarizes the different states in which the FREQ pin can be used. When synchronized to an external clock, the LTC3896 operates in forced continuous mode at light loads if the MODE pin is set to Burst Mode operation or forced continuous operation. If the MODE pin is set to pulse-skipping operation, the LTC3896 maintains pulse-skipping operation when synchronized.

Table 3

FREQ PIN	PLLIN PIN	FREQUENCY
V_{OUT}^-	DC Voltage	350kHz
$INTV_{CC}$	DC Voltage	535kHz
Resistor to V_{OUT}^-	DC Voltage	50kHz to 900kHz
Any of the Above	External Clock 75kHz to 850kHz	Phase Locked to External Clock

Minimum On-Time Considerations

Minimum on-time $t_{ON(MIN)}$ is the smallest time duration that the LTC3896 is capable of turning on the top MOSFET. It is determined by internal timing delays and the gate charge required to turn on the top MOSFET. Low duty cycle applications may approach this minimum on-time limit and care should be taken to ensure that:

$$t_{ON(MIN)} < \frac{|V_{OUT}^-|}{V_{IN}+|V_{OUT}^-|} \bullet \frac{1}{f}$$

If the duty cycle falls below what can be accommodated by the minimum on-time, the controller will begin to skip cycles. The output voltage will continue to be regulated, but the ripple voltage and current will increase.

The minimum on-time for the LTC3896 is approximately 80ns. However, the peak sense voltage decreases the minimum on-time gradually increases up to about 130ns. This is of particular concern in forced continuous applications with low ripple current at light loads. If the duty cycle drops below the minimum on-time limit in this situation, a significant amount of cycle skipping can occur with correspondingly larger current and voltage ripple.

Efficiency Considerations

The percent efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Percent efficiency can be expressed as:

$$\%Efficiency = 100\% - (L1 + L2 + L3 + ...)$$

where L1, L2, etc. are the individual losses as a percentage of input power.

Although all dissipative elements in the circuit produce losses, four main sources usually account for most of the losses in LTC3896 circuits: 1) IC V_{IN} current, 2) DRV_{CC} regulator current, 3) I^2R losses, 4) Topside MOSFET transition losses.

1. The V_{IN} current is the DC supply current given in the Electrical Characteristics table, which excludes MOSFET driver and control currents. V_{IN} current typically results in a small (<0.1%) loss.
2. DRV_{CC} current is the sum of the MOSFET driver and control currents. The MOSFET driver current results from switching the gate capacitance of the power MOSFETs. Each time a MOSFET gate is switched from low to high to low again, a packet of charge, dQ, moves from DRV_{CC} to V_{OUT}^-. The resulting dQ/dt is a current out of DRV_{CC} that is typically much larger than the control circuit current. In continuous mode, $I_{GATECHG} = f(Q_T + Q_B)$, where Q_T and Q_B are the gate charges of the topside and bottom side MOSFETs.

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Supplying DRV_{CC} from the output through $EXTV_{CC}$ will scale the V_{IN} current required for the driver and control circuits by a factor of (Duty Cycle)/(Efficiency). For example, in a 15V to –5V application, 10mA of DRV_{CC} current results in approximately 2.5mA of V_{IN} current. This reduces the midcurrent loss from 10% or more (if the driver was powered directly from V_{IN}) to only a few percent.

3. I^2R losses are predicted from the DC resistances of the fuse (if used), MOSFET, inductor, current sense resistor and input and output capacitor ESR. In continuous mode the average output current flows through L and R_{SENSE}, but is chopped between the topside MOSFET and the synchronous MOSFET. If the two MOSFETs have approximately the same R_{DS}, then the resistance of one MOSFET can simply be summed with the resistances of L, R_{SENSE} and ESR to obtain I^2R losses. For example, if each $R_{DS(ON)} = 30m\Omega$, $R_L = 50m\Omega$, $R_{SENSE} = 10m\Omega$ and $R_{ESR} = 40m\Omega$ (sum of both input and output capacitance losses), then the total resistance is $130m\Omega$.

4. Transition losses apply only to the top MOSFET(s) and become significant only when operating at high V_{IN} + $|V_{OUT}^-|$ voltages (typically 20V or greater). Transition losses can be estimated from:

$$\text{Transition Loss} = (1.7) \bullet \frac{(V_{IN} + |V_{OUT}^-|)^3}{V_{IN}} \bullet I_{O(MAX)} \bullet C_{RSS} \bullet f$$

Other hidden losses such as copper trace and internal battery resistances can account for an additional 5% to 10% efficiency degradation in portable systems. It is very important to include these system level losses during the design phase. The internal battery and fuse resistance losses can be minimized by making sure that C_{IN} has adequate charge storage and very low ESR at the switching frequency. A 25W supply will typically require a minimum of 20µF to 40µF of capacitance having a maximum of $20m\Omega$ to $50m\Omega$ of ESR. Other losses including Schottky conduction losses during dead-time and inductor core losses generally account for less than 2% total additional loss.

Checking Transient Response

The regulator loop response can be checked by looking at the load current transient response. Switching regulators take several cycles to respond to a step in DC (resistive) load current. When a load step occurs, V_{OUT}^- shifts by an amount equal to ΔI_{LOAD} (ESR), where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT} generating the feedback error signal that forces the regulator to adapt to the current change and return V_{OUT}^- to its steady-state value. During this recovery time V_{OUT}^- can be monitored for excessive overshoot or ringing, which would indicate a stability problem. OPTI-LOOP compensation allows the transient response to be optimized over a wide range of output capacitance and ESR values. The availability of the ITH pin not only allows optimization of control loop behavior, but it also provides a DC coupled and AC filtered closed-loop response test point. The DC step, rise time and settling at this test point truly reflects the closed-loop response. Assuming a predominantly second order system, phase margin and/or damping factor can be estimated using the percentage of overshoot seen at this pin. The bandwidth can also be estimated by examining the rise time at the pin. The ITH external components shown in Figure 16 circuit will provide an adequate starting point for most applications.

The ITH series R_C-C_C filter sets the dominant pole-zero loop compensation. The values can be modified slightly to optimize transient response once the final PC layout is done and the particular output capacitor type and value have been determined. The output capacitors need to be selected because the various types and values determine the loop gain and phase. An output current pulse of 20% to 80% of full-load current having a rise time of 1µs to 10µs will produce output voltage and ITH pin waveforms that will give a sense of the overall loop stability without breaking the feedback loop.

Placing a power MOSFET directly across the output capacitor and driving the gate with an appropriate signal generator is a practical way to produce a realistic load step condition. The initial output voltage step resulting from the step change in output current may not be within the

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bandwidth of the feedback loop, so this signal cannot be used to determine phase margin. This is why it is better to look at the ITH pin signal which is in the feedback loop and is the filtered and compensated control loop response.

The gain of the loop will be increased by increasing R_C and the bandwidth of the loop will be increased by decreasing C_C. If R_C is increased by the same factor that C_C is decreased, the zero frequency will be kept the same, thereby keeping the phase shift the same in the most critical frequency range of the feedback loop. The output voltage settling behavior is related to the stability of the closed-loop system and will demonstrate the actual overall supply performance.

A second, more severe transient is caused by switching in loads with large (>1µF) supply bypass capacitors. The discharged bypass capacitors are effectively put in parallel with C_{OUT}, causing a rapid drop in V_{OUT}^-. No regulator can alter its delivery of current quickly enough to prevent this sudden step change in output voltage if the load switch resistance is low and it is driven quickly. If the ratio of C_{LOAD} to C_{OUT} is greater than 1:50, the switch rise time should be controlled so that the load rise time is limited to approximately 25 • C_{LOAD}. Thus a 10µF capacitor would require a 250µs rise time, limiting the charging current to about 200mA.

Design Example

As a design example, assume V_{IN} = 7V to 22V, V_{OUT}^- = –5V, $I_{OUT(MAX)}$ = 5A, $V_{SENSE(MAX)}$ = 75mV and f = 350kHz. Tie the FREQ pin to V_{OUT}^- to program 350kHz operation. Float the ILIM pin to program a maximum current sense threshold of 75mV.

For an inverting buck-boost converter in continuous conduction mode, the average inductor current and the inductor ripple current can be determined by the following equations:

$$I_{L(AVG)} = I_{OUT}\left(\frac{V_{IN}+|V_{OUT}^-|}{V_{IN}}\right)$$

$$\Delta I_L = \frac{1}{(f)(L)} V_{IN}\left(\frac{|V_{OUT}^-|}{V_{IN}+|V_{OUT}^-|}\right)$$

From these two equations and taking a starting point of 30% ripple current at maximum inductor ripple current (at maximum V_{IN}), the following equation can be used to calculate the inductor value:

$$L = \frac{1}{(f)(0.3)(I_{OUT(MAX)})} \bullet \frac{(V_{IN(MAX)})^2(|V_{OUT}^-|)}{(V_{IN(MAX)}+|V_{OUT}^-|)^2}$$

$$= \frac{1}{(350kHz)(0.3)(5A)} \bullet \frac{(22V)^2(5V)}{(22V+5V)^2}$$

$$\approx 6.32\mu H$$

Select a standard value of 6.2µH inductor.

The resulting ripple current at minimum V_{IN} is:

$$\Delta I_L = \frac{1}{(350kHz)(6.2\mu H)} \bullet \frac{(7V)(5V)}{(7V+5V)} \approx 1.34A$$

The peak inductor current will be the maximum average inductor current plus one half of the ripple current. This occurs at minimum V_{IN} and full load:

$$I_{L(PEAK_MAX)} = (5A)\frac{(7V+5V)}{7V} + \frac{1.34A}{2} \approx 9.24A$$

The minimum on-time occurs at maximum V_{IN}:

$$t_{ON(MIN)} = \frac{|V_{OUT}^-|}{V_{IN(MAX)}+|V_{OUT}^-|} \bullet \frac{1}{f} = 529ns$$

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The equivalent R_{SENSE} resistor value can be calculated by using the minimum value for the maximum current sense threshold (66mV):

$$R_{SENSE} \le \frac{66mV}{9.24A} \approx 0.007\Omega$$

Choosing 1% resistors with VPRG floating: R_A = 68.1kΩ and R_B = 357kΩ yields an output voltage of –4.99V. Alternatively, VPRG can be connected to $INTV_{CC}$ and V_{FB} tied to GND to program the –5V fixed output.

The power dissipation on the topside MOSFET can be easily estimated. Choosing a Fairchild FDS6982S dual MOSFET results in: $R_{DS(ON)}$ = 0.035Ω/0.022Ω, C_{MILLER} = 215pF. At maximum input voltage with T(estimated) = 50°C:

$$P_{MAIN} = \frac{(5V)(27V)}{(22V)^2}(5A)^2\left[1+(0.005)(50°C-25°C)\right]$$

$$(0.035\Omega)+\frac{(27V)^3}{22V}\frac{5A}{2}(2.5\Omega)(215pF)\bullet$$

$$\left[\frac{1}{6V-2.3V}+\frac{1}{2.3V}\right](350kHz) = 571mW$$

A short-circuit to ground will result in a folded back current of:

$$I_{SC} = \frac{34mV}{0.007\Omega} - \frac{1}{2}\left(\frac{80ns(22V)}{6.2\mu H}\right) = 4.72A$$

with a typical value of $R_{DS(ON)}$ and δ = (0.005/°C)(25°C) = 0.125. The resulting power dissipated in the bottom MOSFET is:

$$P_{SYNC} = (4.72A)^2\ (1.125)(0.022\Omega) = 551mW$$

which is less than under full-load conditions. C_{IN} is chosen for an RMS current rating of at least 4.3A at temperature. C_{OUT} is chosen based on the ESR that is required to satisfy the output voltage ripple requirement. The selected C_{OUT} must support the maximum RMS operating current of 4.3A at minimum V_{IN}.

PC Board Layout Checklist

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the IC.

1. Are the signal and power grounds kept separate? The combined IC signal ground pin and the ground return of C_{DRVCC} must return to the combined C_{OUT} (–) terminals. The path formed by the top N-channel MOSFET, bottom N-channel MOSFET and the C_{IN} and C_{OUT} capacitors should have short leads and PC trace lengths.
2. Does the LTC3896 V_{FB} pin's resistive divider connect to the (-) terminal of C_{OUT}? The resistive divider must be connected between the (–) terminal of C_{OUT} and signal ground. The feedback resistor connections should not be along the high current feeds from the input or output capacitors.
3. Are the $SENSE^-$ and $SENSE^+$ leads routed together with minimum PC trace spacing? The filter capacitor between $SENSE^+$ and $SENSE^-$ should be as close as possible to the IC. Ensure accurate current sensing with Kelvin connections at the SENSE resistor.
4. Is the DRV_{CC} and decoupling capacitor connected close to the IC, between the DRV_{CC} and the V_{OUT}^- pin? This capacitor carries the MOSFET drivers' current peaks.
5. Keep the SW, TG, and BOOST nodes away from sensitive small-signal nodes. All of these nodes have very large and fast moving signals and therefore should be kept on the output side of the LTC3896 and occupy minimum PC trace area.
6. Use a modified star virtual ground technique for V_{OUT}^-: a low impedance, large copper area central grounding point on the same side of the PC board as the input and output capacitors with tie-ins for the bottom of the DRV_{CC} decoupling capacitor, the bottom of the voltage feedback resistive divider and the V_{OUT}^- pin of the IC.

APPLICATIONS INFORMATION

PC Board Layout Debugging

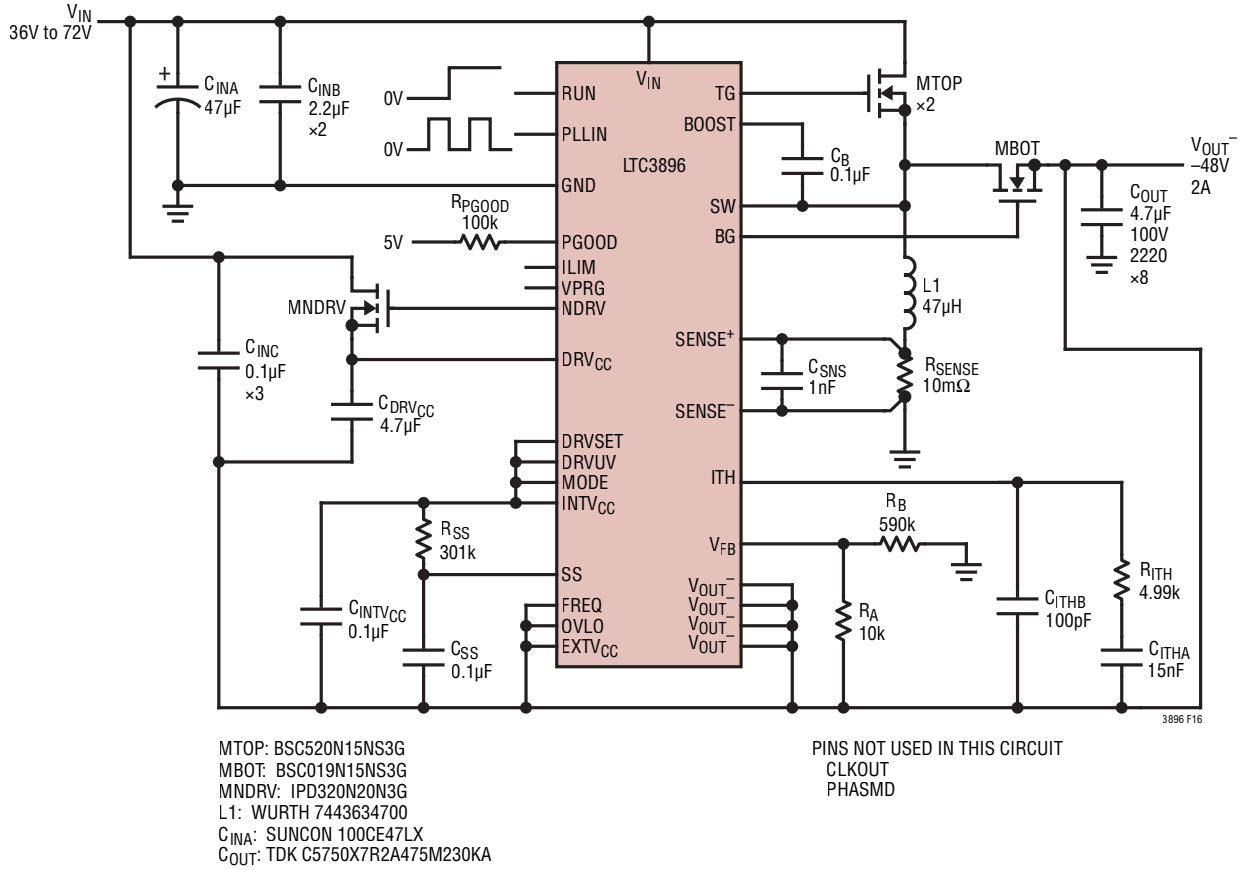
It is helpful to use a DC-50MHz current probe to monitor the current in the inductor while testing the circuit. Monitor the output switching node (SW pin) to synchronize the oscilloscope to the internal oscillator and probe the actual output voltage as well. Check for proper performance over the operating voltage and current range expected in the application. The frequency of operation should be maintained over the input voltage range down to dropout and until the output load drops below the low current operation threshold—typically 25% of the maximum designed current level in Burst Mode operation.

The duty cycle percentage should be maintained from cycle to cycle in a well-designed, low noise PCB implementation. Variation in the duty cycle at a subharmonic rate can suggest noise pickup at the current or voltage sensing inputs or inadequate loop compensation. Overcompensation of the loop can be used to tame a poor PC layout if regulator bandwidth optimization is not required.

Investigate whether any problems exist only at higher output currents or only at higher input voltages. If problems coincide with high input voltages and low output currents, look for capacitive coupling between the BOOST, SW, TG, and possibly BG connections and the sensitive voltage and current pins. The capacitor placed across the current sensing pins needs to be placed immediately adjacent to the pins of the IC. This capacitor helps to minimize the effects of differential noise injection due to high frequency capacitive coupling. If problems are encountered with high current output loading at lower input voltages, look for inductive coupling between C_{IN}, the top MOSFET and the bottom MOSFET to the sensitive current and voltage sensing traces. In addition, investigate common ground path voltage pickup between these components and the GND pin of the IC.

An embarrassing problem, which can be missed in an otherwise properly working switching regulator, results when the current sensing leads are hooked up backwards. The output voltage under this improper hookup will still be maintained but the advantages of current mode control will not be realized. Compensation of the voltage loop will be much more sensitive to component selection. This behavior can be investigated by temporarily shorting out the current sensing resistor—don't worry, the regulator will still maintain control of the output voltage.

TYPICAL APPLICATIONS



MTOP: BSC520N15NS3G
MBOT: BSC019N15NS3G
MNDRV: IPD320N20N3G
L1: WURTH 7443634700
C_{INA}: SUNCON 100CE47LX
C_{OUT}: TDK C5750X7R2A475M230KA

PINS NOT USED IN THIS CIRCUIT
CLKOUT
PHASMD

Figure 16. High Efficiency 35V – 72V to –48V/2A Inverting Regulator

TYPICAL APPLICATIONS

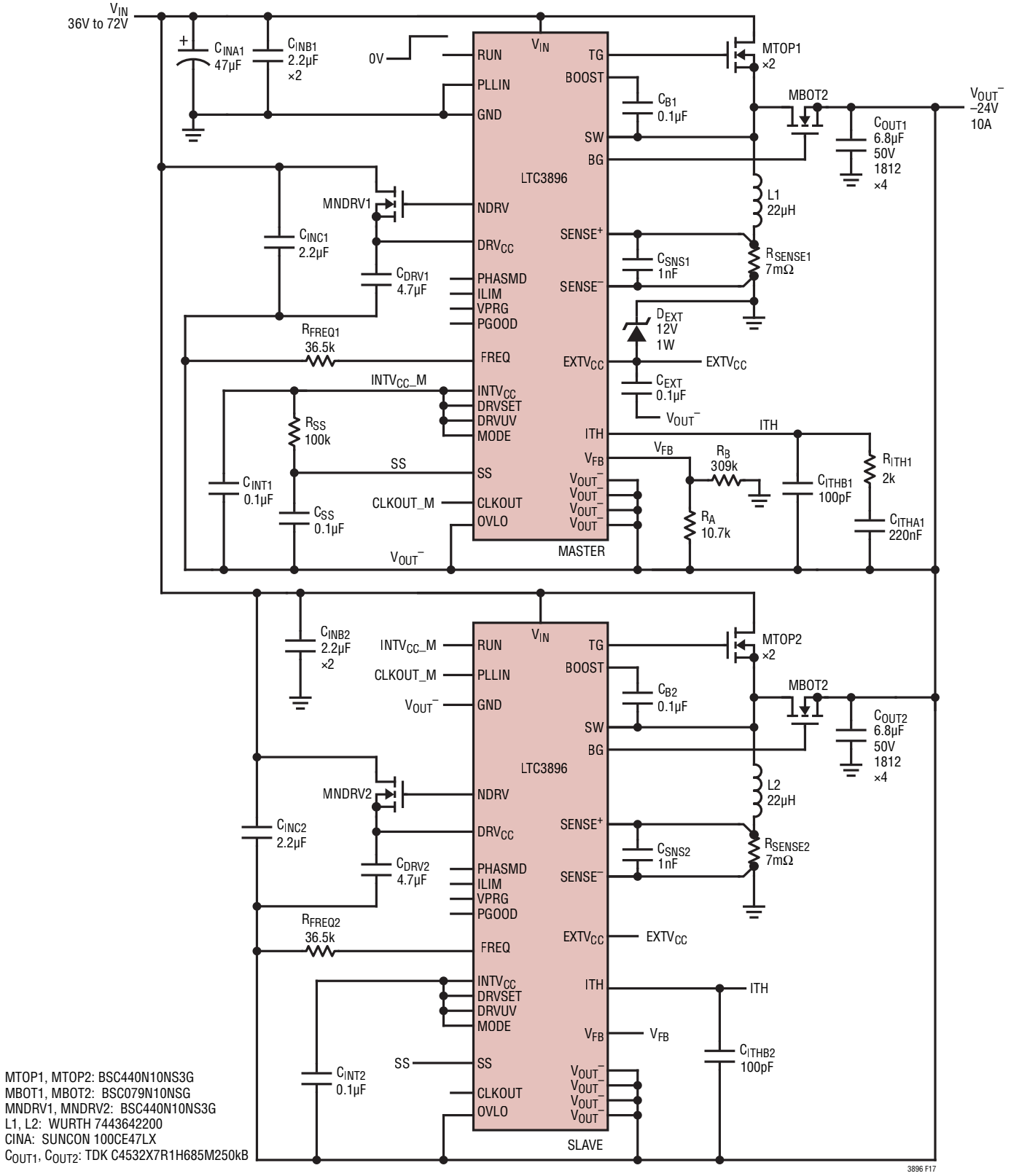
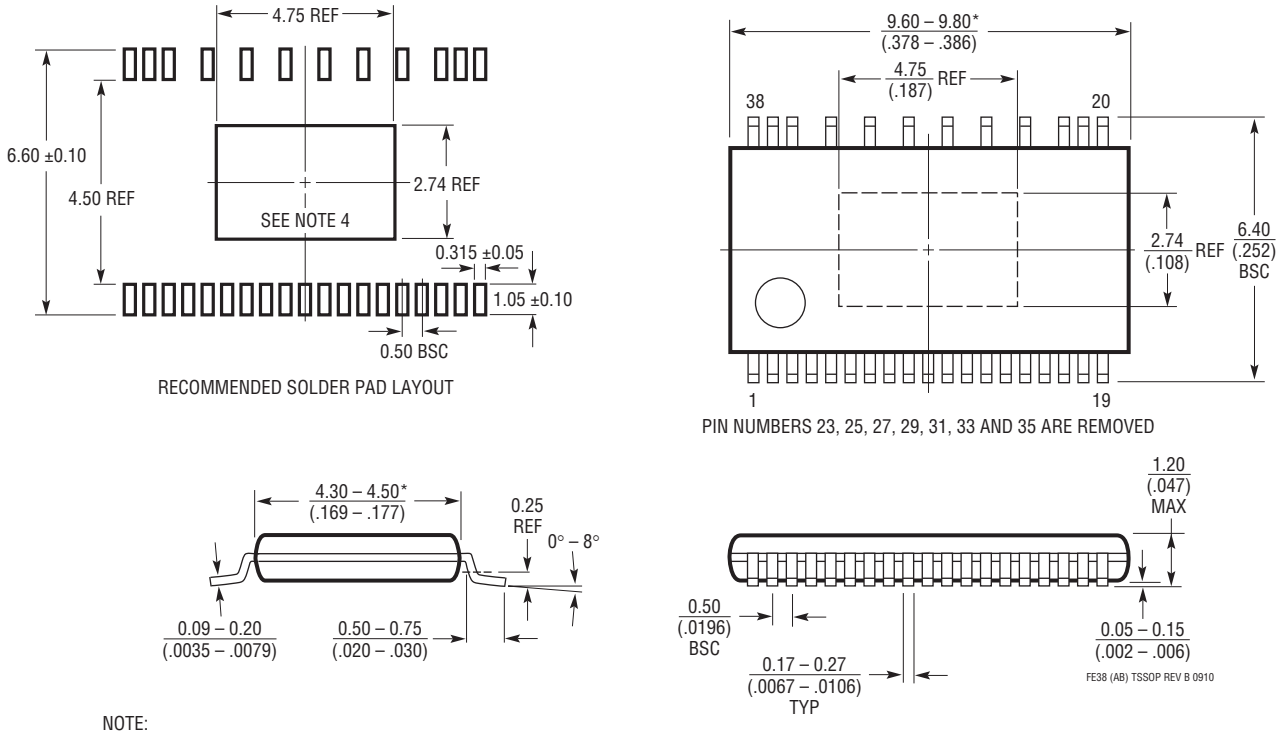


Figure 17. High Efficiency 2-Phase 36V–72V to –24V/10A Inverting Regulator

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LTC3896#packaging for the most recent package drawings.

FE Package
Package Variation: FE38 (31)
38-Lead Plastic TSSOP (4.4mm)
(Reference LTC DWG # 05-08-1865 Rev B)
Exposed Pad Variation AB

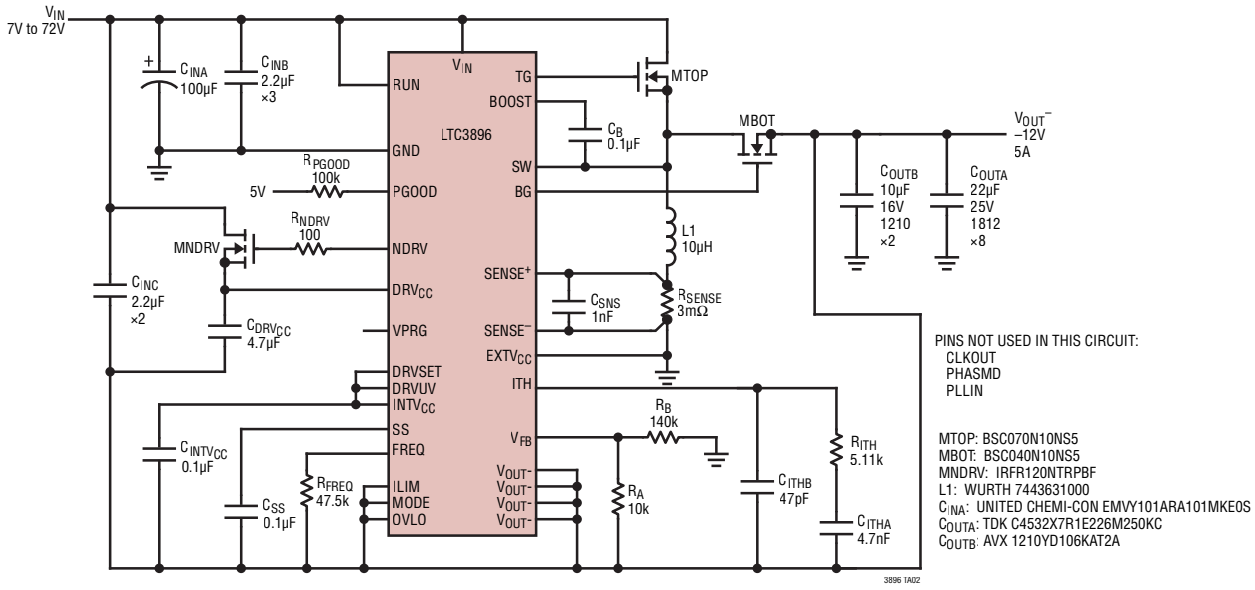


NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN MILLIMETERS (INCHES)
3. DRAWING NOT TO SCALE
4. RECOMMENDED MINIMUM PCB METAL SIZE FOR EXPOSED PAD ATTACHMENT
*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.150mm (.006") PER SIDE

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TYPICAL APPLICATION

High Efficiency 7V–72V to –12V/5A Inverting Regulator



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC3863	60V Low I_Q, Inverting DC/DC Controller	Fixed Frequency 50kHz to 850kHz, 3.5V ≤ V_{IN} ≤ 60V, Negative V_{OUT} from –0.4V to Beyond –150V , I_Q = 70µA, MSOP-12E, 3mm × 4mm DFN-12
LTC7149	60V, 4A Synchronous Step-Down Regulator	PLL Fixed Frequency 300kHz to 3MHz, 3.4V ≤ V_{IN} ≤ 60V, for Inverting Outputs 0V ≤ V_{OUT} ≤ –28V, 28-Lead (4mm × 5mm) QFN and TSSOP Packages
LT8710	80V Synchronous SEPIC/ Inverting/Boost Controller	Fixed Frequency Up to 750kHz, 4.5V ≤ V_{IN} ≤ 80V, with Output Current Control TSSOP-20 Package
LTC3704	Wide Input Range, No R_{SENSE} Positive-to-Negative DC/DC Controller	PLL Fixed Frequency 50kHz to 1MHz, 2.5V ≤ V_{IN} ≤ 36V, MSOP-10
LTC3895	150V Low I_Q, Synchronous Step-Down DC/DC Controller	PLL Fixed Frequency 50kHz to 900kHz, 4V ≤ V_{IN} ≤ 140V, 0.8V ≤ V_{OUT} ≤ 60V, I_Q = 40µA
LTC3892/ LTC3892-1	60V Low I_Q, Dual, 2-Phase Synchronous Step-Down DC/DC Controller with 99% Duty Cycle	PLL Fixed Frequency 50kHz to 900kHz, 4V ≤ V_{IN} ≤ 60V, 0.8V ≤ V_{OUT} ≤ 0.99V_{IN}, Adjustable 5V to 10V Gate Drive, I_Q = 29µA
LTC3639	High Efficiency, 150V 100mA Synchronous Step-Down Regulator	Integrated Power MOSFETs, 4V ≤ V_{IN} ≤ 150V, 0.8V ≤ V_{OUT} ≤ V_{IN}, I_Q = 12µA, MSOP-16(12)
LTC7138	High Efficiency, 140V 400mA Step-Down Regulator	Integrated Power MOSFETs, 4V ≤ V_{IN} ≤ 140V, 0.8V ≤ V_{OUT} ≤ V_{IN}, I_Q = 12µA, MSOP-16(12)
LTC3891	60V, Low I_Q, Synchronous Step-Down DC/DC Controller with 99% Duty Cycle	PLL Fixed Frequency 50kHz to 900kHz 4V ≤ V_{IN} ≤ 60V, 0.8V ≤ V_{OUT} ≤ 24V, I_Q = 50µA
LTC3810	100V Synchronous Step-Down DC/DC Controller	Constant On-time Valley Current Mode 4V ≤ V_{IN} ≤ 100V, 0.8V ≤ V_{OUT} ≤ 0.93V_{IN}, SSOP-28
LTC3638	High Efficiency, 140V 250mA Step-Down Regulator	Integrated Power MOSFETs, 4V ≤ V_{IN} ≤ 140V, 0.8V ≤ V_{OUT} ≤ V_{IN}, I_Q = 12µA, MSOP-16(12)
LTC7812	38V Synchronous Boost+Buck Controller Low EMI and Low Input/Output Ripple	4.5V (Down to 2.5V After Start-up) ≤ V_{IN} ≤ 38V, Boost V_{OUT} Up to 60V, 0.8V ≤ Buck V_{OUT} ≤ 24V, I_Q = 33µA, 5mm × 5mm QFN-32
LT8631	100V, 1A Synchronous Micropower Step-Down Regulator	PLL Fixed Frequency 100kHz to 1MHz, 3V ≤ V_{IN} ≤ 100V, 0.8V ≤ V_{OUT} ≤ 60V, TSSOP-20 Package with High Voltage Spacing

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