Low I_Q, 60V Synchronous Step-Down Controller

FEATURES

- **Wide V_{IN} Range: 4V to 60V (65V Abs Max)**
- **Low Operating I_Q: 50µA**
- **Wide Output Voltage Range: 0.8V ≤ V_{OUT} ≤ 24V**
- **R_{SENSE} or DCR Current Sensing**
- Phase-Lockable Frequency (75kHz to 750kHz)
- Programmable Fixed Frequency (50kHz to 900kHz)
- Selectable Continuous, Pulse-Skipping or Low Ripple Burst Mode® Operation at Light Load
- Selectable Current Limit
- Very Low Dropout Operation: 99% Duty Cycle
- Adjustable Output Voltage Soft-Start or Tracking
- Power Good Output Voltage Monitor
- Output Overvoltage Protection
- Low Shutdown I_Q: < 14µA
- Internal LDO Powers Gate Drive from V_{IN} or $EXTV_{CC}$
- No Current Foldback During Start-Up
- Small 20-Pin 3mm × 4mm QFN and TSSOP Packages

APPLICATIONS

- Automotive Always-On Systems
- Battery Powered Digital Devices
- Distributed DC Power Systems

DESCRIPTION

The LTC®3891 is a high performance step-down switching regulator DC/DC controller that drives an all N-channel synchronous power MOSFET stage. A constant frequency current mode architecture allows a phase-lockable frequency of up to 750kHz.

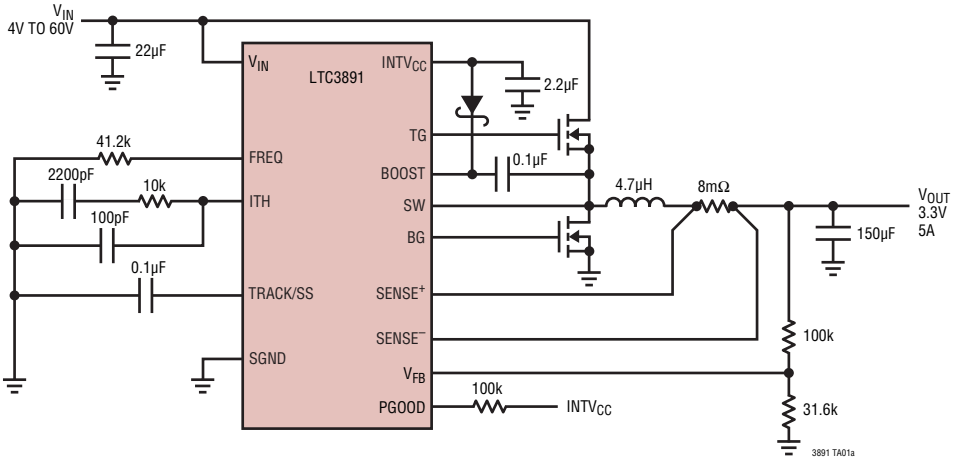
The 50µA no-load quiescent current extends operating run time in battery-powered systems. OPTI-LOOP® compensation allows the transient response to be optimized over a wide range of output capacitance and ESR values. The LTC3891 features a precision 0.8V reference and power good output indicator. A wide 4V to 60V input supply range encompasses a wide range of intermediate bus voltages and battery chemistries. The output voltage of the LTC3891 can be programmed between 0.8V to 24V.

The TRACK/SS pin ramps the output voltages during start-up. Current foldback limits MOSFET heat dissipation during short-circuit conditions. The PLLIN/MODE pin selects among Burst Mode operation, pulse-skipping mode, or continuous conduction mode at light loads.

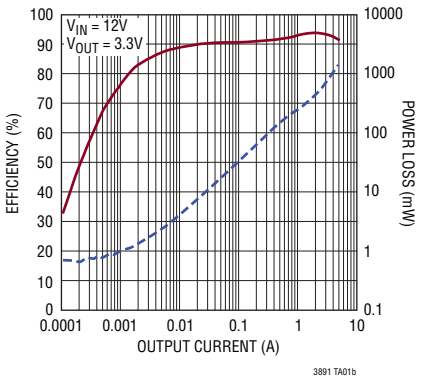
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TYPICAL APPLICATION

High Efficiency 3.3V Step-Down Converter



Efficiency and Power Loss vs Output Current

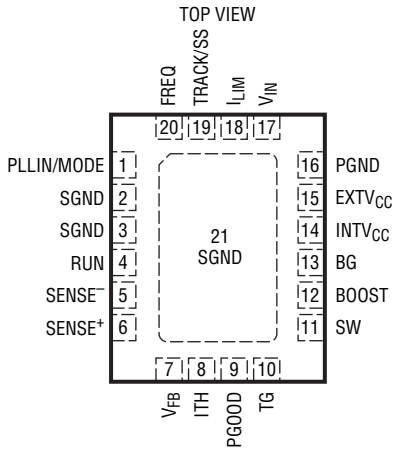


ABSOLUTE MAXIMUM RATINGS

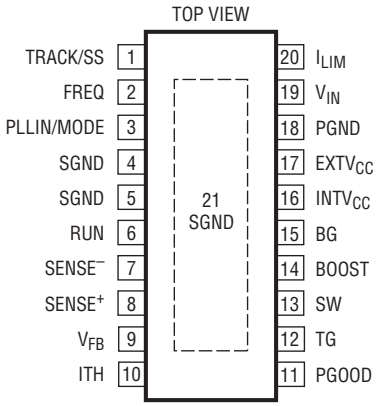
(Note 1)

Input Supply Voltage (V_{IN}) ..... –0.3V to 65V
Topside Driver Voltage (BOOST) ..... –0.3V to 71V
Switch Voltage (SW) ..... –5V to 65V
(BOOST-SW) ..... –0.3V to 6V
RUN ..... –0.3V to 8V
Maximum Current Sourced into Pin from Source > 8V 100µA
SENSE+, SENSE– Voltages ..... –0.3V to 28V
PLLIN/MODE, $INTV_{CC}$ Voltages ..... –0.3V to 6V
I_{LIM}, FREQ Voltages ..... –0.3V to $INTV_{CC}$
$EXTV_{CC}$ ..... –0.3V to 14V
ITH, V_{FB} Voltages ..... –0.3V to 6V
PGOOD Voltage ..... –0.3V to 6V
TRACK/SS Voltage ..... –0.3V to 6V
Operating Junction Temperature Range (Notes 2, 3)
LTC3891E, LTC3891I ..... –40°C to 125°C
LTC3891H ..... –40°C to 150°C
LTC3891MP ..... –55°C to 150°C
Maximum Junction Temperature (Notes 2, 3)
LTC3891E, LTC3891I ..... 125°C
LTC3891H, LTC3891MP ..... 150°C
Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



UDC PACKAGE
20-LEAD (3mm × 4mm) PLASTIC QFN
T_{JMAX} = 150°C, θ_{JA} = 43°C/W
EXPOSED PAD (PIN 21) IS SGND, MUST BE SOLDERED TO PCB



FE PACKAGE
20-LEAD PLASTIC TSSOP
T_{JMAX} = 150°C, θ_{JA} = 38°C/W
EXPOSED PAD (PIN 21) IS SGND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3891EUDC#PBF	LTC3891EUDC#TRPBF	LFXV	20-Lead (3mm × 4mm) Plastic QFN	–40°C to 125°C
LTC3891IUDC#PBF	LTC3891IUDC#TRPBF	LFXV	20-Lead (3mm × 4mm) Plastic QFN	–40°C to 125°C
LTC3891HUDC#PBF	LTC3891HUDC#TRPBF	LFXV	20-Lead (3mm × 4mm) Plastic QFN	–40°C to 150°C
LTC3891MPUDC#PBF	LTC3891MPUDC#TRPBF	LFXV	20-Lead (3mm × 4mm) Plastic QFN	–55°C to 150°C

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3891EFE#PBF	LTC3891EFE#TRPBF	LTC3891FE	20-Lead Plastic TSSOP	–40°C to 125°C
LTC3891IFE#PBF	LTC3891IFE#TRPBF	LTC3891FE	20-Lead Plastic TSSOP	–40°C to 125°C
LTC3891HFE#PBF	LTC3891HFE#TRPBF	LTC3891FE	20-Lead Plastic TSSOP	–40°C to 150°C
LTC3891MPFE#PBF	LTC3891MPFE#TRPBF	LTC3891FE	20-Lead Plastic TSSOP	–55°C to 150°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2), V_{IN} = 12V, V_{RUN} = 5V, $EXTV_{CC}$ = 0V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Input Supply Operating Voltage Range			4		60	V
V_{FB}	Regulated Feedback Voltage	(Note 4); I_{TH} Voltage = 1.2V					
		–40°C to 85°C		0.792	0.800	0.808	V
		LTC3891E, LTC3891I	●	0.788	0.800	0.812	V
		LTC3891H, LTC3891MP	●	0.786	0.800	0.812	V
I_{FB}	Feedback Current	(Note 4)			±5	±50	nA
$V_{REFLNREG}$	Reference Voltage Line Regulation	(Note 4); V_{IN} = 4.5V to 60V			0.002	0.02	%/V
$V_{LOADREG}$	Output Voltage Load Regulation	(Note 4) Measured in Servo Loop; ΔI_{TH} Voltage = 1.2V to 0.7V	●		0.01	0.1	%
		(Note 4) Measured in Servo Loop; ΔI_{TH} Voltage = 1.2V to 2V	●		–0.01	–0.1	%
g_m	Transconductance Amplifier g_m	(Note 4); I_{TH} = 1.2V; Sink/Source 5µA			2		mmho
I_Q	Input DC Supply Current	(Note 5)					
	Pulse Skip or Forced Continuous Mode	V_{FB} = 0.83V (No Load)			2		mA
	Sleep Mode	V_{FB} = 0.83V (No Load)			50	75	µA
	Shutdown	RUN = 0V			14	25	µA
UVLO	Undervoltage Lockout	$INTV_{CC}$ Ramping Up	●		3.92	4.2	V
		$INTV_{CC}$ Ramping Down	●	3.6	3.80	4.0	V
V_{OVL}	Feedback Overvoltage Protection	Measured at V_{FB} Relative to Regulated V_{FB}		7	10	13	%
I_{SENSE}^+	$SENSE^+$ Pin Current					±1	µA
I_{SENSE}^-	$SENSE^-$ Pins Current	V_{SENSE}^- < $INTV_{CC}$ – 0.5V				±2	µA
		V_{SENSE}^- > $INTV_{CC}$ + 0.5V			700		µA
DF_{MAX}	Maximum Duty Factor	In Dropout		98	99		%
$I_{TRACK/SS}$	Soft-Start Charge Current	V_{TRACK} = 0V		7	10	14	µA
V_{RUN} On	RUN Pin On Threshold	V_{RUN} Rising	●	1.15	1.21	1.27	V
V_{RUN} Hyst	RUN Pin Hysteresis				50		mV
$V_{SENSE(MAX)}$	Maximum Current Sense Threshold	V_{FB} = 0.7V, V_{SENSE}^- = 3.3V, I_{LIM} = 0	●	22	30	36	mV
		V_{FB} = 0.7V, V_{SENSE}^- = 3.3V, I_{LIM} = $INTV_{CC}$	●	43	50	57	mV
		V_{FB} = 0.7V, V_{SENSE}^- = 3.3V, I_{LIM} = FLOAT	●	64	75	85	mV

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2), V_{IN} = 12V, V_{RUN} = 5V, $EXTV_{CC}$ = 0V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Gate Driver							
TG	Pull-Up On-Resistance Pull-Down On-Resistance				2.5 1.5		Ω Ω
BG	Pull-Up On-Resistance Pull-Down On-Resistance				2.4 1.1		Ω Ω
TG t_r TG t_f	TG Transition Time: Rise Time Fall Time	(Note 6) C_{LOAD} = 3300pF C_{LOAD} = 3300pF			 25 16		 ns ns
BG t_r BG t_f	BG Transition Time: Rise Time Fall Time	(Note 6) C_{LOAD} = 3300pF C_{LOAD} = 3300pF			 25 13		 ns ns
TG/BG t_{1D}	Top Gate Off to Bottom Gate On Delay Synchronous Switch-On Delay Time	C_{LOAD} = 3300pF			30		ns
BG/TG t_{1D}	Bottom Gate Off to Top Gate On Delay Top Switch-On Delay Time	C_{LOAD} = 3300pF			30		ns
$t_{ON(MIN)}$	Minimum On-Time	(Note 7)			95		ns
$INTV_{CC}$ Linear Regulator							
$V_{INTVCCVIN}$	Internal V_{CC} Voltage	6V < V_{IN} < 60V, V_{EXTVCC} = 0V		4.85	5.1	5.35	V
V_{LDOVIN}	$INTV_{CC}$ Load Regulation	I_{CC} = 0mA to 50mA, V_{EXTVCC} = 0V			0.7	1.1	%
$V_{INTVCCEXT}$	Internal V_{CC} Voltage	6V < V_{EXTVCC} < 13V		4.85	5.1	5.35	V
V_{LDOEXT}	$INTV_{CC}$ Load Regulation	I_{CC} = 0mA to 50mA, V_{EXTVCC} = 8.5V			0.6	1.1	%
V_{EXTVCC}	$EXTV_{CC}$ Switchover Voltage	I_{CC} = 0mA to 50mA, $EXTV_{CC}$ Ramping Positive		4.5	4.7	4.9	V
V_{LDOHYS}	$EXTV_{CC}$ Hysteresis				250		mV
Oscillator and Phase-Locked Loop							
$f_{25k\Omega}$	Programmable Frequency	R_{FREQ} = 25k; PLLIN/MODE = DC Voltage			105		kHz
$f_{65k\Omega}$	Programmable Frequency	R_{FREQ} = 65k; PLLIN/MODE = DC Voltage		375	440	505	kHz
$f_{105k\Omega}$	Programmable Frequency	R_{FREQ} =105k; PLLIN/MODE = DC Voltage			835		kHz
f_{LOW}	Low Fixed Frequency	V_{FREQ} = 0V; PLLIN/MODE = DC Voltage		320	350	380	kHz
f_{HIGH}	High Fixed Frequency	V_{FREQ} = $INTV_{CC}$; PLLIN/MODE = DC Voltage		485	535	585	kHz
f_{SYNC}	Synchronizable Frequency	PLLIN/MODE = External Clock	●	75		750	kHz
PGOOD1 Output							
V_{PGL}	PGOOD Voltage Low	I_{PGOOD} = 2mA			0.2	0.4	V
I_{PGOOD}	PGOOD Leakage Current	V_{PGOOD} = 5V				±1	µA
V_{PG}	PGOOD Trip Level	V_{FB} with Respect to Set Regulated Voltage					
		V_{FB} Ramping Negative		–13	–10	–7	%
		Hysteresis			2.5		%
		V_{FB} Ramping Positive		7	10	13	%
		Hysteresis			2.5		%
t_{PG}	Delay for Reporting a Fault				25		µs

ELECTRICAL CHARACTERISTICS

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC3891 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC3891E is guaranteed to meet performance specifications from 0°C to 85°C. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3891I is guaranteed over the –40°C to 125°C operating junction temperature range, the LTC3891H is guaranteed over the –40°C to 150°C operating junction temperature range and the LTC3891MP is tested and guaranteed over the –55°C to 150°C operating junction temperature range. High junction temperatures degrade operating lifetimes; operating lifetime is derated for junction temperatures greater than 125°C. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors.

Note 3: The junction temperature (T_J, in °C) is calculated from the ambient temperature (T_A, in °C) and power dissipation (P_D, in Watts) according to the formula:

$T_J = T_A + (P_D \bullet \theta_{JA})$, where θ_{JA} is 43°C/W for the QFN or 38°C/W for the TSSOP.

Note 4: The LTC3891 is tested in a feedback loop that servos V_{ITH} to a specified voltage and measures the resultant V_{FB}. The specification at 85°C is not tested in production and is assured by design, characterization and correlation to production testing at other temperatures (125°C for the LTC3891E/LTC3891I, 150°C for the LTC3891H/LTC3891MP). For the LTC3891MP, the specification at –40°C is not tested in production and is assured by design, characterization and correlation to production testing at –55°C.

Note 5: Dynamic supply current is higher due to the gate charge being delivered at the switching frequency. See Applications Information.

Note 6: Rise and fall times are measured using 10% and 90% levels. Delay times are measured using 50% levels

Note 7: The minimum on-time condition is specified for an inductor peak-to-peak ripple current ≥ 40% of I_{MAX} (See Minimum On-Time Considerations in the Applications Information section).

TYPICAL PERFORMANCE CHARACTERISTICS

Efficiency and Power Loss vs Output Current

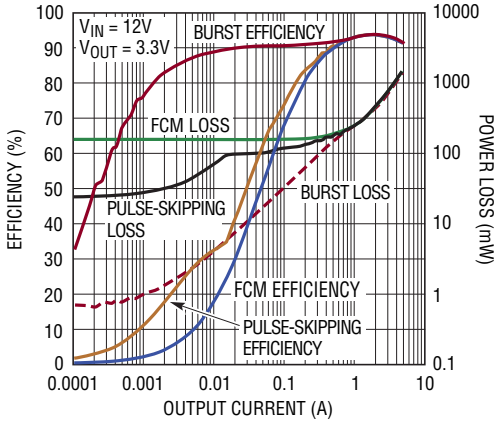
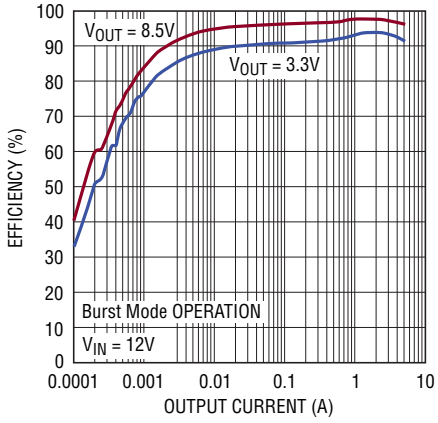


FIGURE 12 CIRCUIT

3891 G01

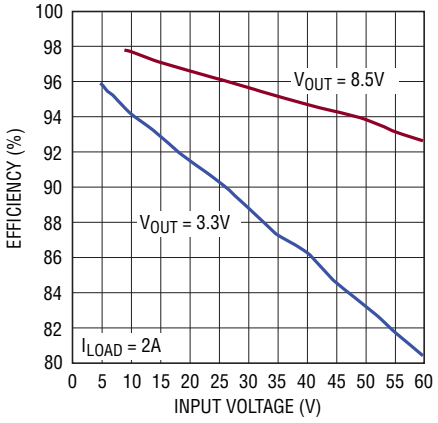
Efficiency vs Output Current



FIGURES 12, 14 CIRCUITS

3891 G02

Efficiency vs Input Voltage

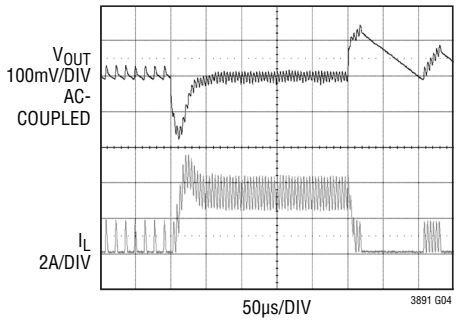


FIGURES 12, 14 CIRCUITS

3891 G03

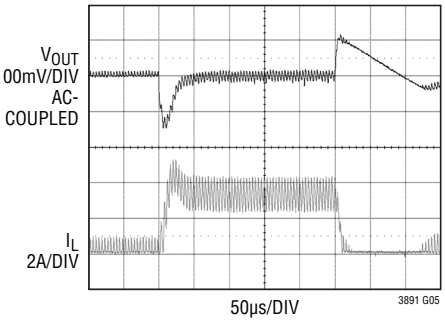
TYPICAL PERFORMANCE CHARACTERISTICS

Load Step
Burst Mode Operation



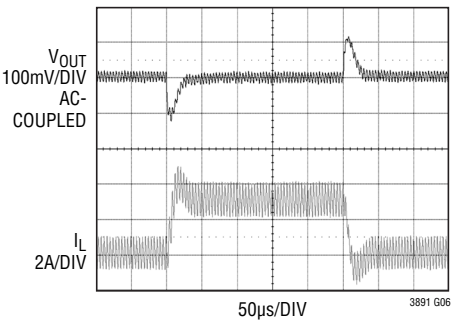
LOAD STEP = 100mA TO 3A
V_{IN} = 12V
V_{OUT} = 3.3V
FIGURE 12 CIRCUIT

Load Step
Pulse-Skipping Mode



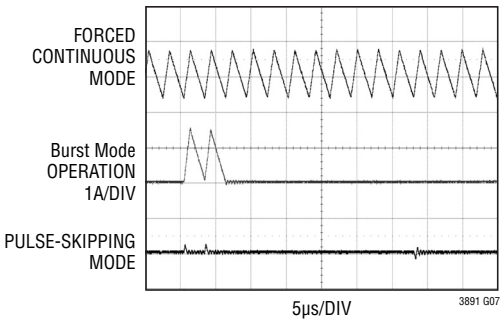
LOAD STEP = 100mA TO 3A
V_{IN} = 12V
V_{OUT} = 3.3V
FIGURE 12 CIRCUIT

Load Step
Forced Continuous Mode



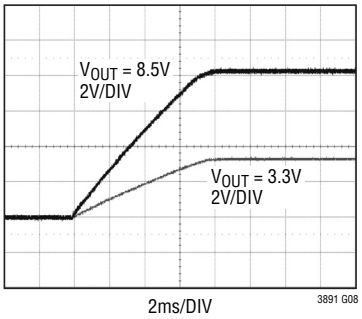
LOAD STEP = 100mA TO 3A
V_{IN} = 12V
V_{OUT} = 3.3V
FIGURE 12 CIRCUIT

Inductor Current at Light Load



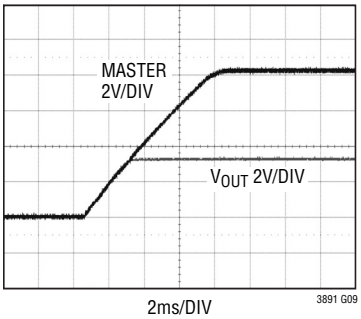
V_{IN} = 12V
V_{OUT} = 3.3V
I_{LOAD} = 200µA

Soft Start-Up

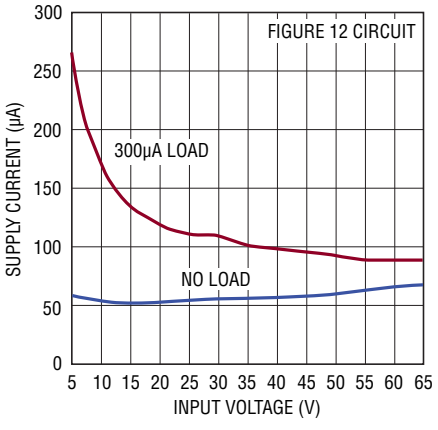


FIGURES 12, 14 CIRCUITS

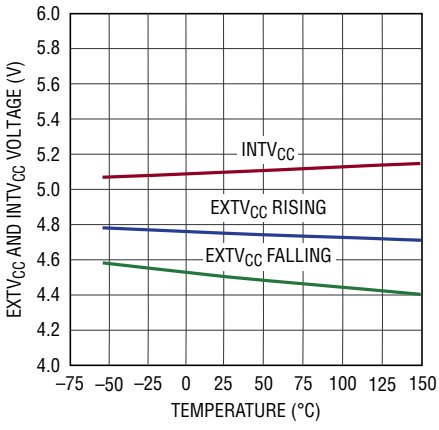
Tracking Start-Up



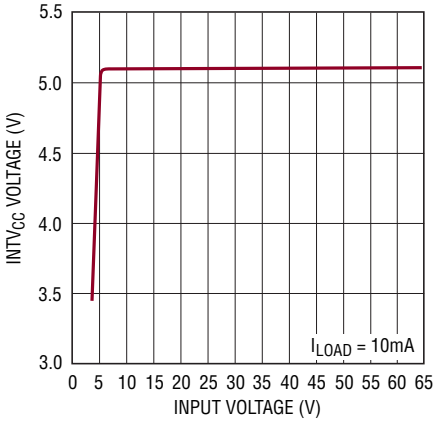
Total Input Supply Current vs Input Voltage



$EXTV_{CC}$ Switchover and $INTV_{CC}$ Voltages vs Temperature

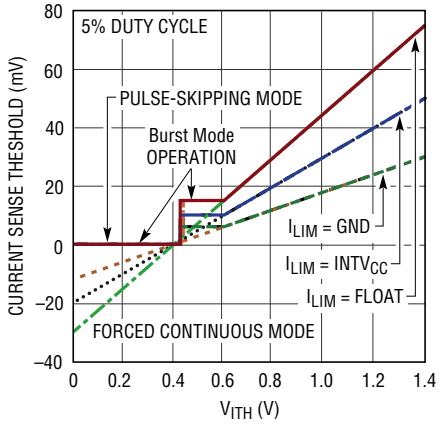


$INTV_{CC}$ Line Regulation



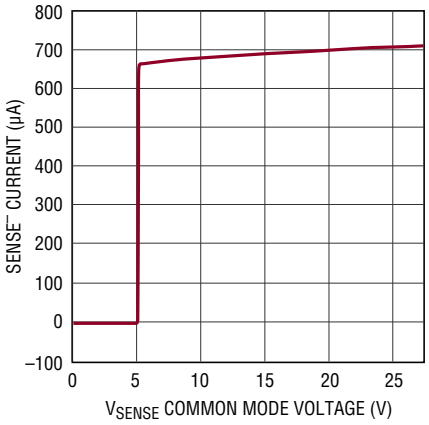
TYPICAL PERFORMANCE CHARACTERISTICS

Maximum Current Sense Voltage vs I_{TH} Voltage



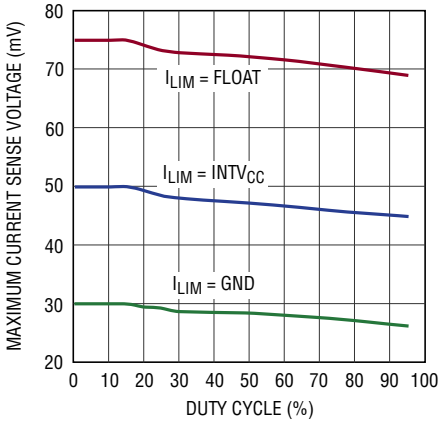
3891 G13

SENSE⁻ Pin Input Bias Current



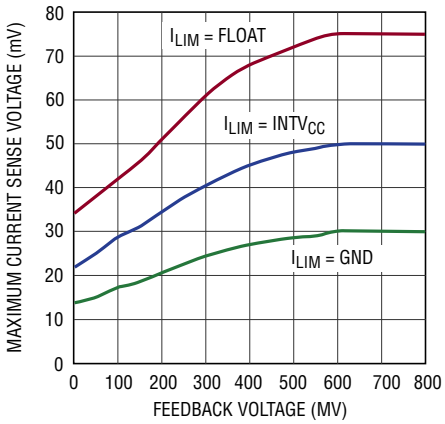
3891 G14

Maximum Current Sense Threshold vs Duty Cycle



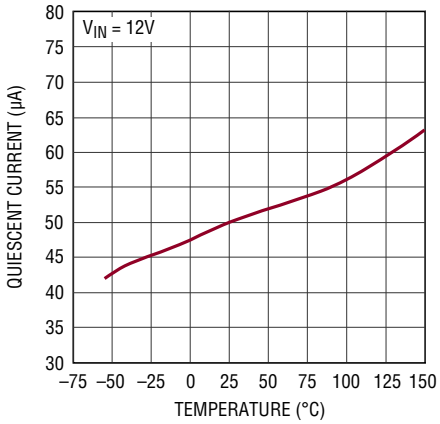
3891 G15

Foldback Current Limit



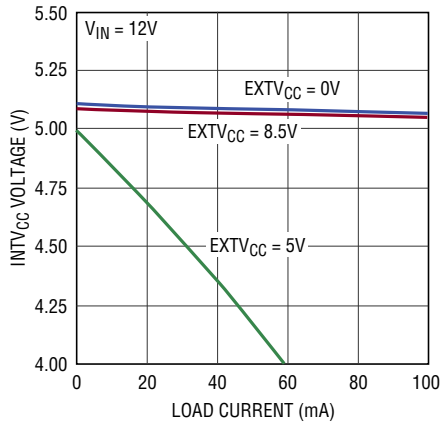
3891 G16

Quiescent Current vs Temperature



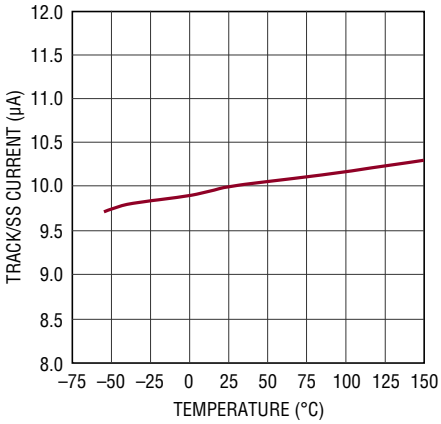
3891 G17

$INTV_{CC}$ vs Load Current



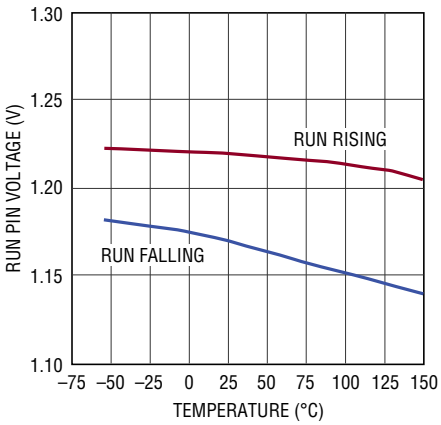
3891 G18

TRACK/SS Pull-Up Current vs Temperature



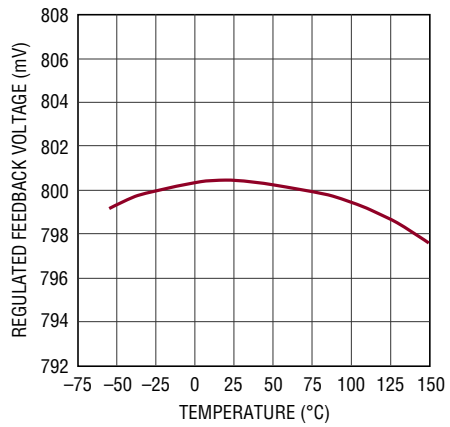
3891 G19

Shutdown (RUN) Threshold vs Temperature



3891 G20

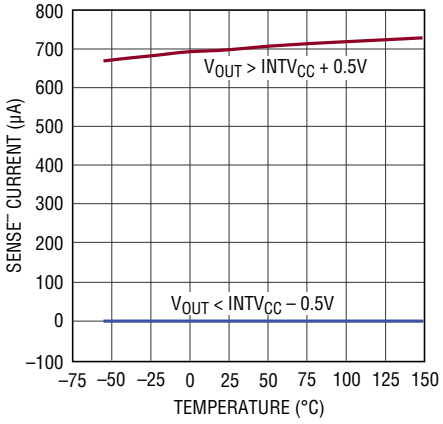
Regulated Feedback Voltage vs Temperature



3891 G21

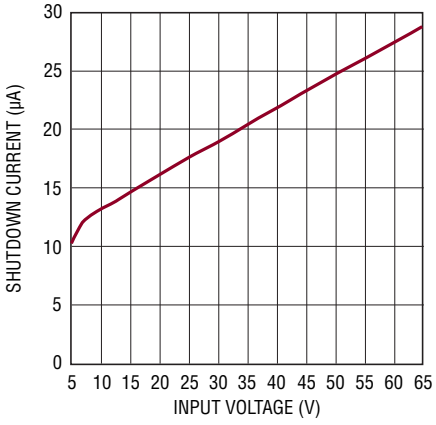
TYPICAL PERFORMANCE CHARACTERISTICS

SENSE⁻ Pin Input Bias Current vs Temperature



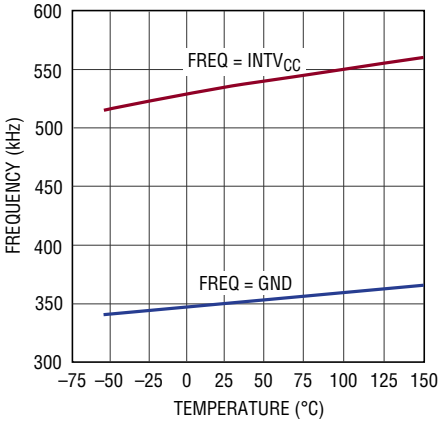
3891 G22

Shutdown Current vs Input Voltage



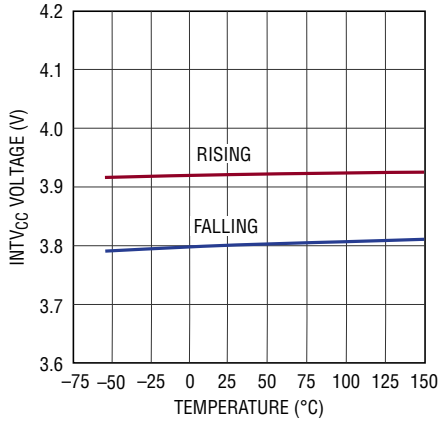
3891 G23

Oscillator Frequency vs Temperature



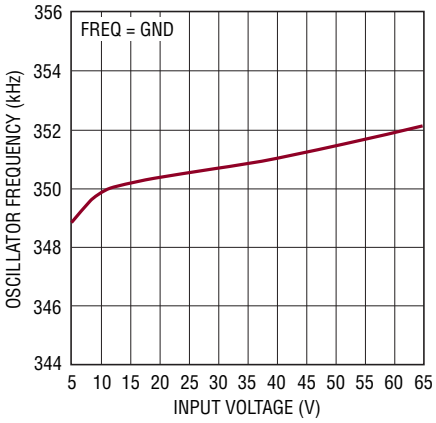
3891 G24

Undervoltage Lockout Threshold vs Temperature



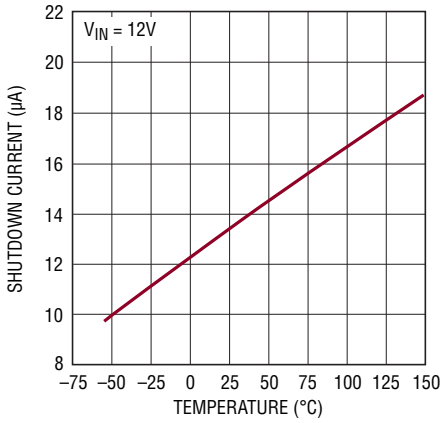
3891 G25

Oscillator Frequency vs Input Voltage



3891 G26

Shutdown Current vs Temperature



3891 G27

PIN FUNCTIONS (QFN/eTSSOP)

PLLIN/MODE (Pin 1/Pin 3): External Synchronization Input to Phase Detector and Forced Continuous Mode Input. When an external clock is applied to this pin, the phase-locked loop will force the rising TG signal to be synchronized with the rising edge of the external clock, and the regulator operates in forced continuous mode. When not synchronizing to an external clock, this input determines how the LTC3891 operates at light loads. Pulling this pin to ground selects Burst Mode operation. An internal 100k resistor to ground also invokes Burst Mode operation when the pin is floated. Tying this pin to $INTV_{CC}$ forces continuous inductor current operation. Tying this pin to a voltage greater than 1.2V and less than $INTV_{CC}$ –1.3V selects pulse-skipping operation.

SGND (Pins 2, 3, Exposed Pad Pin 21/Pins 4, 5, Exposed Pad Pin 21): Small-signal ground, must be routed separately from high current grounds to the common (–) terminals of the C_{IN} capacitor. Pins 2, 3/4, 5, must both be electrically connected to small signal ground for proper operation.The exposed pad must be soldered to PCB ground for rated thermal performance.

RUN (Pin 4/Pin 6): Digital Run Control Input. Forcing this pin below 1.16V shuts down the controller. Forcing this pin below 0.7V shuts down the entire LTC3891, reducing quiescent current to approximately 14µA.

$SENSE^-$ (Pin 5/Pin 7): The (–) Input to the Differential Current Comparator. When greater than $INTV_{CC}$ – 0.5V, the $SENSE^-$ pin supplies power to the current comparator.

$SENSE^+$ (Pin 6/Pin 8): The (+) input to the differential current comparator is normally connected to DCR sensing network or current sensing resistor. The ITH pin voltage and controlled offsets between the $SENSE^-$ and $SENSE^+$ pins in conjunction with R_{SENSE} set the current trip threshold.

V_{FB} (Pin 7/Pin 9): Receives the remotely sensed feedback voltage from an external resistive divider across the output.

ITH (Pin 8/Pin 10): Error Amplifier Outputs and Switching Regulator Compensation Point. The current comparator trip point increases with this control voltage.

PGOOD (Pin 9/Pin 11): Open-Drain Logic Output. PGOOD is pulled to ground when the voltage on the V_{FB} pin is not within 10% of its set point.

TG (Pin 10/Pin 12): High Current Gate Drives for Top N-channel MOSFET. This is the output of floating driver with a voltage swing equal to $INTV_{CC}$ superimposed on the switch node voltage SW.

SW (Pin 11/ Pin 13): Switch Node Connection to Inductor.

BOOST (Pin 12/Pin 14): Bootstrapped Supply to the Topside Floating Driver. A capacitor is connected between the BOOST and SW pin and a Schottky diode is tied between the BOOST and $INTV_{CC}$ pins. Voltage swing at the BOOST pin is from $INTV_{CC}$ to (V_{IN} + $INTV_{CC}$).

BG (Pin 13/Pin 15): High Current Gate Drive for Bottom (Synchronous) N-channel MOSFET. Voltage swing at this pin is from ground to $INTV_{CC}$.

$INTV_{CC}$ (Pin 14/Pin 16): Output of the Internal Linear Low Dropout Regulator. The driver and control circuits are powered from this voltage source. Must be decoupled to PGND with a minimum of 2.2µF ceramic or other low ESR capacitor. Do not use the $INTV_{CC}$ pin for any other purpose.

$EXTV_{CC}$ (Pin 15/Pin 17): External Power Input to an Internal LDO Connected to $INTV_{CC}$. This LDO supplies $INTV_{CC}$ power, bypassing the internal LDO powered from V_{IN} whenever $EXTV_{CC}$ is higher than 4.7V. See $EXTV_{CC}$ Connection in the Applications Information section. Do not float or exceed 14V on this pin.

PGND (Pin 16/Pin 18): Driver Power Ground. Connects to the source of bottom (synchronous) N-channel MOSFET and the (–) terminal of C_{IN}.

V_{IN} (Pin 17/Pin 19): Main Supply Pin. A bypass capacitor should be tied between this pin and the SGND pins.

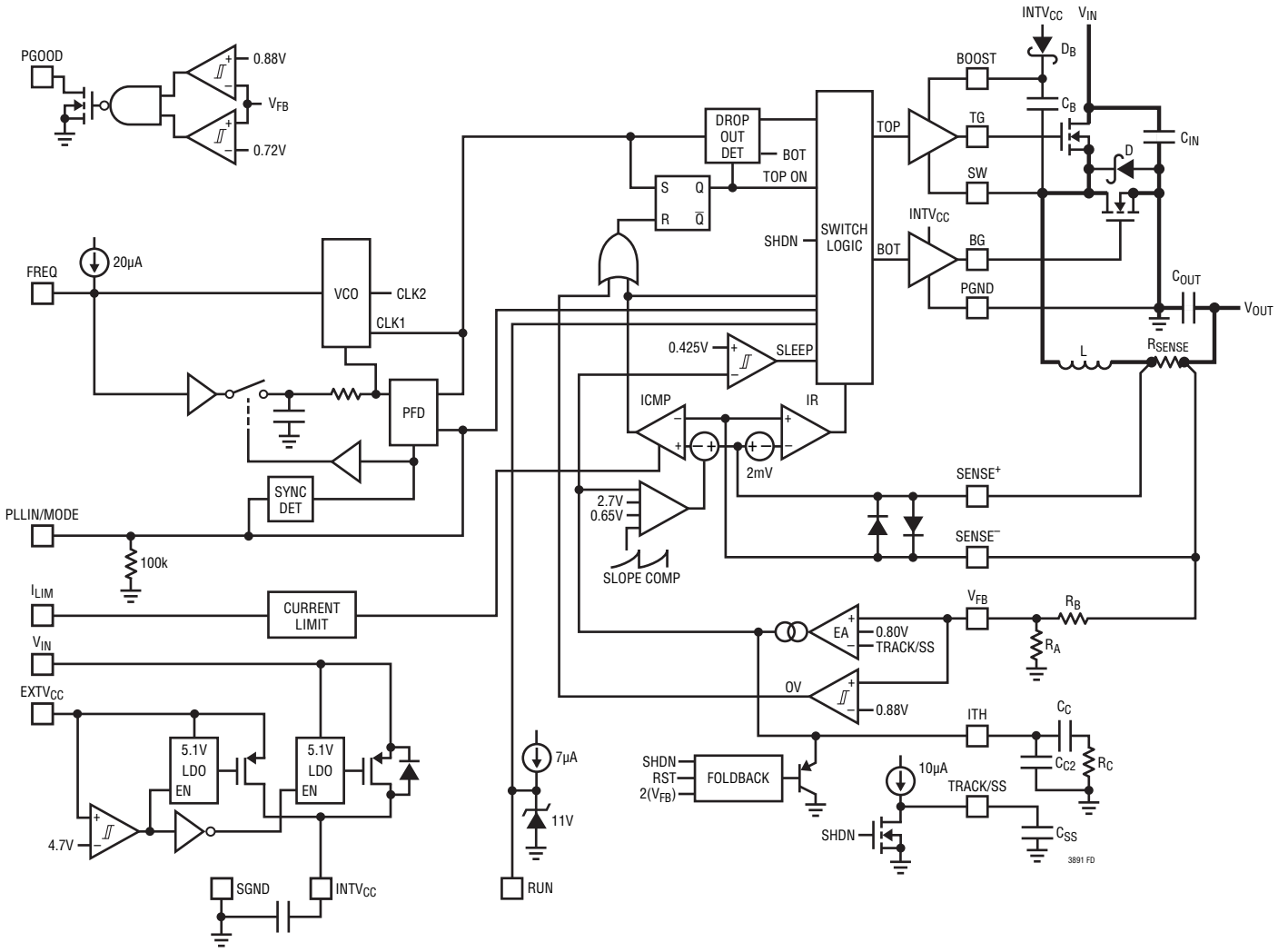
I_{LIM} (Pin 18/Pin 20): Current Comparator Sense Voltage Range Inputs. Tying this pin to SGND, FLOAT or $INTV_{CC}$ sets the maximum current sense threshold to one of three different levels for the comparator.

PIN FUNCTIONS

TRACK/SS (Pin 19/Pin 1): External Tracking and Soft-Start Input. The LTC3891 regulates the V_{FB} voltage to the smaller of 0.8V or the voltage on the TRACK/SS pin. An internal 10µA pull-up current source is connected to this pin. A capacitor to ground at this pin sets the ramp time to final regulated output voltage. Alternatively, a resistor divider on another voltage supply connected to this pin allows the LTC3891 output to track another supply during start-up.

FREQ (Pin 20/Pin 2): The frequency control pin for the internal VCO. Connecting the pin to GND forces the VCO to a fixed low frequency of 350kHz. Connecting the pin to $INTV_{CC}$ forces the VCO to a fixed high frequency of 535kHz. Other frequencies between 50kHz and 900kHz can be programmed by using a resistor between FREQ and GND. An internal 20µA pull-up current develops the voltage to be used by the VCO to control the frequency.

FUNCTIONAL DIAGRAM



OPERATION

Main Control Loop

The LTC3891 uses a constant frequency, current mode step-down architecture. During normal operation, the external top MOSFET is turned on when the clock for that channel sets the RS latch, and is turned off when the main current comparator, ICMP, resets the RS latch. The peak inductor current at which ICMP trips and resets the latch is controlled by the voltage on the ITH pin, which is the output of the error amplifier, EA. The error amplifier compares the output voltage feedback signal at the V_{FB} pin (which is generated with an external resistor divider connected across the output voltage, V_{OUT}, to ground) to the internal 0.800V reference voltage. When the load current increases, it causes a slight decrease in V_{FB} relative to the reference, which causes the EA to increase the ITH voltage until the average inductor current matches the new load current.

After the top MOSFET is turned off each cycle, the bottom MOSFET is turned on until either the inductor current starts to reverse, as indicated by the current comparator IR, or the beginning of the next clock cycle.

$INTV_{CC}/EXTV_{CC}$ Power

Power for the top and bottom MOSFET drivers and most other internal circuitry is derived from the $INTV_{CC}$ pin. When the $EXTV_{CC}$ pin is tied to a voltage less than 4.7V, the V_{IN} LDO (low dropout linear regulator) supplies 5.1V from V_{IN} to $INTV_{CC}$. If $EXTV_{CC}$ is taken above 4.7V, the V_{IN} LDO is turned off and an $EXTV_{CC}$ LDO is turned on. Once enabled, the $EXTV_{CC}$ LDO supplies 5.1V from $EXTV_{CC}$ to $INTV_{CC}$. Using the $EXTV_{CC}$ pin allows the $INTV_{CC}$ power to be derived from a high efficiency external source such as one of the LTC3891 switching regulator outputs.

The top MOSFET driver is biased from the floating bootstrap capacitor, C_B, which normally recharges during each cycle through an external diode when the top MOSFET turns off. If the input voltage, V_{IN}, decreases to a voltage close to V_{OUT}, the loop may enter dropout and attempt to turn on the top MOSFET continuously. The dropout detector detects this and forces the top MOSFET off for about one twelfth of the clock period every tenth cycle to allow C_B to recharge.

Shutdown and Start-Up (RUN, TRACK/SS Pins)

The LTC3891 can be shut down using the RUN pin. Pulling this pin below 1.16V shuts down the main control loop. Pulling the RUN pin below 0.7V disables the controller and most internal circuits, including the $INTV_{CC}$ LDOs. In this state, the LTC3891 draws only 14µA of quiescent current.

Releasing the RUN pin allows a small internal current to pull up the pin to enable the controller. The RUN pin has a 7µA pull-up which is designed to be large enough so that the RUN pin can be safely floated (to always enable the controller) without worry of condensation or other small board leakage pulling the pin down. This is ideal for always-on applications where the controller is enabled continuously and never shut down.

The RUN pin may be externally pulled up or driven directly by logic. When driving the RUN pin with a low impedance source, do not exceed the absolute maximum rating of 8V. The RUN pin has an internal 11V voltage clamp that allows the RUN pin to be connected through a resistor to a higher voltage (for example, V_{IN}), so long as the maximum current into the RUN pin does not exceed 100µA.

The RUN pin can also be implemented as a UVLO by connecting it to the output of an external resistor divider network off V_{IN} (see Applications Information section).

The start-up of the controller's output voltage V_{OUT} is controlled by the voltage on the TRACK/SS pin. When the voltage on the TRACK/SS pin is less than the 0.8V internal reference, the LTC3891 regulates the V_{FB} voltage to the TRACK/SS pin voltage instead of the 0.8V reference. This allows the TRACK/SS pin to be used to program a soft-start by connecting an external capacitor from the TRACK/SS pin to SGND. An internal 10µA pull-up current charges this capacitor creating a voltage ramp on the TRACK/SS pin. As the TRACK/SS voltage rises linearly from 0V to 0.8V (and beyond up to 5V), the output voltage V_{OUT} rises smoothly from zero to its final value. Alternatively the TRACK/SS pin can be used to cause the start-up of V_{OUT} to track that of another supply. Typically, this requires connecting to the TRACK/SS pin an external resistor divider from the other supply to ground (see Applications Information section).

OPERATION

Light Load Current Operation (Burst Mode Operation, Pulse-Skipping or Forced Continuous Mode) (PLLIN/MODE Pin)

The LTC3891 can be enabled to enter high efficiency Burst Mode operation, constant frequency pulse-skipping mode, or forced continuous conduction mode at low load currents. To select Burst Mode operation, tie the PLLIN/MODE pin to SGND. To select forced continuous operation, tie the PLLIN/MODE pin to $INTV_{CC}$. To select pulse-skipping mode, tie the PLLIN/MODE pin to a DC voltage greater than 1.2V and less than $INTV_{CC}$ – 1.3V.

When the controller is enabled for Burst Mode operation, the minimum peak current in the inductor is set to approximately 25% of the maximum sense voltage even though the voltage on the ITH pin indicates a lower value. If the average inductor current is higher than the load current, the error amplifier, EA, will decrease the voltage on the ITH pin. When the ITH voltage drops below 0.425V, the internal sleep signal goes high (enabling sleep mode) and both external MOSFETs are turned off. The ITH pin is then disconnected from the output of the EA and parked at 0.450V.

In sleep mode, much of the internal circuitry is turned off, reducing the quiescent current that the LTC3891 draws to only 50µA. In sleep mode, the load current is supplied by the output capacitor. As the output voltage decreases, the EA's output begins to rise. When the output voltage drops enough, the ITH pin is reconnected to the output of the EA, the sleep signal goes low, and the controller resumes normal operation by turning on the top external MOSFET on the next cycle of the internal oscillator.

When the controller is enabled for Burst Mode operation, the inductor current is not allowed to reverse. The reverse current comparator, IR, turns off the bottom external MOSFET just before the inductor current reaches zero, preventing it from reversing and going negative. Thus, the controller operates in discontinuous operation.

In forced continuous operation or clocked by an external clock source to use the phase-locked loop (see Frequency Selection and Phase-Locked Loop section), the inductor current is allowed to reverse at light loads or under large transient conditions. The peak inductor current is determined by the voltage on the ITH pin, just as in normal operation. In this mode, the efficiency at light loads is lower than in Burst Mode operation. However, continuous operation has the advantage of lower output voltage ripple and less interference to audio circuitry. In forced continuous mode, the output ripple is independent of load current.

When the PLLIN/MODE pin is connected for pulse-skipping mode, the LTC3891 operates in PWM pulse-skipping mode at light loads. In this mode, constant frequency operation is maintained down to approximately 1% of designed maximum output current. At very light loads, the current comparator, ICMP, may remain tripped for several cycles and force the external top MOSFET to stay off for the same number of cycles (i.e., skipping pulses). The inductor current is not allowed to reverse (discontinuous operation). This mode, like forced continuous operation, exhibits low output ripple as well as low audio noise and reduced RF interference as compared to Burst Mode operation. It provides higher low current efficiency than forced continuous mode, but not nearly as high as Burst Mode operation.

Frequency Selection and Phase-Locked Loop (FREQ and PLLIN/MODE Pins)

The selection of switching frequency is a trade-off between efficiency and component size. Low frequency operation increases efficiency by reducing MOSFET switching losses, but requires larger inductance and/or capacitance to maintain low output ripple voltage.

The switching frequency of the LTC3891 can be selected using the FREQ pin.

If the PLLIN/MODE pin is not being driven by an external clock source, the FREQ pin can be tied to SGND, tied to $INTV_{CC}$ or programmed through an external resistor. Tying FREQ to SGND selects 350kHz while tying FREQ to $INTV_{CC}$ selects 535kHz. Placing a resistor between FREQ and SGND allows the frequency to be programmed between 50kHz and 900kHz, as shown in Figure 9.

A phase-locked loop (PLL) is available on the LTC3891 to synchronize the internal oscillator to an external clock source that is connected to the PLLIN/MODE pin. The

OPERATION

LTC3891's phase detector adjusts the voltage (through an internal lowpass filter) of the VCO input to align the turn-on of the controller's external top MOSFET to the rising edge of the synchronizing signal.

The VCO input voltage is prebiased to the operating frequency set by the FREQ pin before the external clock is applied. If prebiased near the external clock frequency, the PLL loop only needs to make slight changes to the VCO input in order to synchronize the rising edge of the external clock's to the rising edge of TG. The ability to prebias the loop filter allows the PLL to lock-in rapidly without deviating far from the desired frequency.

The typical capture range of the phase-locked loop is from approximately 55kHz to 900kHz, with a guarantee to be between 75kHz and 750kHz. In other words, the LTC3891's PLL is guaranteed to lock to an external clock source whose frequency is between 75kHz and 750kHz.

The typical input clock thresholds on the PLLIN/MODE pin are 1.6V (rising) and 1.2V (falling).

Output Overvoltage Protection

An overvoltage comparator guards against transient overshoots as well as other more serious conditions that may overvoltage the output. When the V_{FB} pin rises by more than 10% above its regulation point of 0.800V, the top MOSFET is turned off and the bottom MOSFET is turned on until the overvoltage condition is cleared.

Power Good Pin

The PGOOD pin is connected to an open drain of an internal N-channel MOSFET. The MOSFET turns on and pulls the PGOOD pin low when the V_{FB} pin voltage is not within ±10% of the 0.8V reference voltage. The PGOOD pin is also pulled low when the RUN pin is low (shut down). When the V_{FB} pin voltage is within the ±10% requirement, the MOSFET is turned off and the pin is allowed to be pulled up by an external resistor to a source no greater than 6V.

Foldback Current

When the output voltage falls to less than 70% of its nominal level, foldback current limiting is activated, progressively lowering the peak current limit in proportion to the severity of the overcurrent or short-circuit condition. Foldback current limiting is disabled during the soft-start interval (as long as the V_{FB} voltage is keeping up with the TRACK/SS voltage).

APPLICATIONS INFORMATION

The Typical Application on the first page is a basic LTC3891 application circuit. LTC3891 can be configured to use either DCR (inductor resistance) sensing or low value resistor sensing. The choice between the two current sensing schemes is largely a design trade-off between cost, power consumption and accuracy. DCR sensing is becoming popular because it saves expensive current sensing resistors and is more power efficient, especially in high current applications. However, current sensing resistors provide the most accurate current limits for the controller. Other external component selection is driven by the load requirement, and begins with the selection of R_{SENSE} (if R_{SENSE} is used) and inductor value. Next, the power MOSFETs and Schottky diodes are selected. Finally, input and output capacitors are selected.

Current Limit Programming

The I_{LIM} pin is a tri-level logic input which sets the maximum current limit of the controller. When I_{LIM} is grounded, the maximum current limit threshold voltage of the current comparator is programmed to be 30mV. When I_{LIM} is floated, the maximum current limit threshold is 75mV. When I_{LIM} is tied to $INTV_{CC}$, the maximum current limit threshold is set to 50mV.

SENSE+ and SENSE– Pins

The SENSE+ and SENSE– pins are the inputs to the current comparators. The common mode voltage range on these pins is 0V to 28V (abs max), enabling the LTC3891 to regulate output voltages up to a nominal 24V (allowing margin for tolerances and transients).

The SENSE+ pin is high impedance over the full common mode range, drawing at most ±1µA. This high impedance allows the current comparators to be used in inductor DCR sensing.

The impedance of the SENSE– pin changes depending on the common mode voltage. When SENSE– is less than $INTV_{CC}$ – 0.5V, a small current of less than 1µA flows out of the pin. When SENSE– is above $INTV_{CC}$ + 0.5V, a higher current (~700µA) flows into the pin. Between $INTV_{CC}$ – 0.5V and $INTV_{CC}$ + 0.5V, the current transitions from the smaller current to the higher current.

Filter components mutual to the sense lines should be placed close to the LTC3891, and the sense lines should run close together to a Kelvin connection underneath the current sense element (shown in Figure 1). Sensing current elsewhere can effectively add parasitic inductance and capacitance to the current sense element, degrading the information at the sense terminals and making the programmed current limit unpredictable. If inductor DCR sensing is used (Figure 2b), sense resistor R1 should be placed close to the switching node, to prevent noise from coupling into sensitive small-signal nodes.

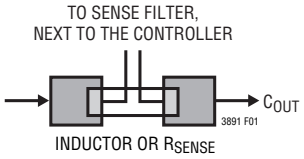
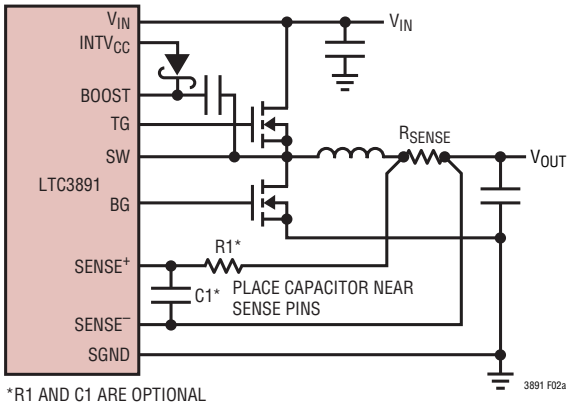
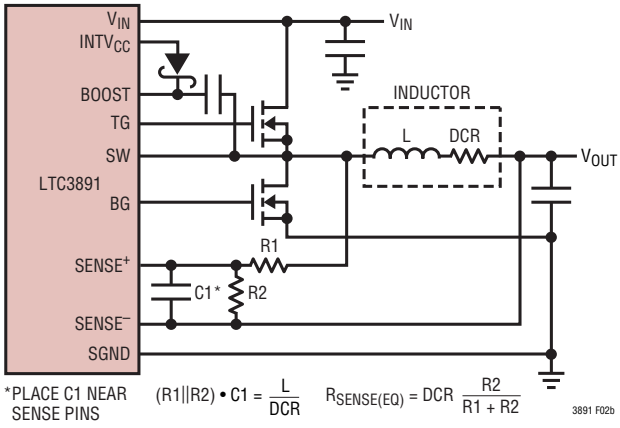


Figure 1. Sense Lines Placement with Inductor or Sense Resistor



(2a) Using a Resistor to Sense Current



(2b) Using the Inductor DCR to Sense Current

Figure 2. Current Sensing Methods

APPLICATIONS INFORMATION

Low Value Resistor Current Sensing

A typical sensing circuit using a discrete resistor is shown in Figure 2a. R_{SENSE} is chosen based on the required output current.

The current comparator has a maximum threshold $V_{SENSE(MAX)}$ determined by the I_{LIM} setting. The current comparator threshold voltage sets the peak of the inductor current, yielding a maximum average output current, I_{MAX}, equal to the peak value less half the peak-to-peak ripple current, ΔI_L. To calculate the sense resistor value, use the equation:

$$R_{SENSE} = \frac{V_{SENSE(MAX)}}{I_{MAX} + \frac{\Delta I_L}{2}}$$

To ensure that the application will deliver full load current over the full operating temperature range, choose the minimum value for the Maximum Current Sense Threshold ($V_{SENSE(MAX)}$) in the Electrical Characteristics table (30mV, 50mV or 75mV, depending on the state of the I_{LIM} pin).

When using the controller in very low dropout conditions, the maximum output current level will be reduced due to the internal compensation required to meet stability criterion for buck regulators operating at greater than 50% duty factor. A curve is provided in the Typical Performance Characteristics section to estimate this reduction in peak inductor current depending upon the operating duty factor.

Inductor DCR Sensing

For applications requiring the highest possible efficiency at high load currents, the LTC3891 is capable of sensing the voltage drop across the inductor DCR, as shown in Figure 2b. The DCR of the inductor represents the small amount of DC resistance of the copper wire, which can be less than 1mΩ for today's low value, high current inductors. In a high current application requiring such an inductor, power loss through a sense resistor would cost several points of efficiency compared to inductor DCR sensing.

If the external (R1||R2) • C1 time constant is chosen to be exactly equal to the L/DCR time constant, the voltage drop across the external capacitor is equal to the drop across the inductor DCR multiplied by R2/(R1 + R2). R2 scales the voltage across the sense terminals for applications where the DCR is greater than the target sense resistor value. To properly dimension the external filter components, the DCR of the inductor must be known. It can be measured using a good RLC meter, but the DCR tolerance is not always the same and varies with temperature; consult the manufacturers' data sheets for detailed information.

Using the inductor ripple current value from the Inductor Value Calculation section, the target sense resistor value is:

$$R_{SENSE(EQUIV)} = \frac{V_{SENSE(MAX)}}{I_{MAX} + \frac{\Delta I_L}{2}}$$

To ensure that the application will deliver full load current over the full operating temperature range, choose the minimum value for the Maximum Current Sense Threshold ($V_{SENSE(MAX)}$) in the Electrical Characteristics table (30mV, 50mV or 75mV, depending on the state of the I_{LIM} pin).

Next, determine the DCR of the inductor. When provided, use the manufacturer's maximum value, usually given at 20°C. Increase this value to account for the temperature coefficient of copper resistance, which is approximately 0.4%/°C. A conservative value for $T_{L(MAX)}$ is 100°C.

To scale the maximum inductor DCR to the desired sense resistor value (R_D), use the divider ratio:

$$R_D = \frac{R_{SENSE(EQUIV)}}{DCR_{MAX}\ at\ T_{L(MAX)}}$$

C1 is usually selected to be in the range of 0.1µF to 0.47µF. This forces R1 || R2 to around 2k, reducing error that might have been caused by the SENSE+ pin's ±1µA current.

APPLICATIONS INFORMATION

The equivalent resistance R1 || R2 is scaled to the temperature inductance and maximum DCR:

$$R1||R2 = \frac{L}{(DCR\ at\ 20°C)\bullet C1}$$

The sense resistor values are:

$$R1 = \frac{R1||R2}{R_D};\ R2 = \frac{R1\bullet R_D}{1-R_D}$$

The maximum power loss in R1 is related to duty cycle, and will occur in continuous mode at the maximum input voltage:

$$P_{LOSS}\ R1 = \frac{(V_{IN(MAX)} - V_{OUT})\bullet V_{OUT}}{R1}$$

Ensure that R1 has a power rating higher than this value. If high efficiency is necessary at light loads, consider this power loss when deciding whether to use DCR sensing or sense resistors. Light load power loss can be modestly higher with a DCR network than with a sense resistor, due to the extra switching losses incurred through R1. However, DCR sensing eliminates a sense resistor, reduces conduction losses and provides higher efficiency at heavy loads. Peak efficiency is about the same with either method.

Inductor Value Calculation

The operating frequency and inductor selection are interrelated n that higher operating frequencies allow the use of smaller inductor and capacitor values. So why would anyone ever choose to operate at lower frequencies with larger components? The answer is efficiency. A higher frequency generally results in lower efficiency because of MOSFET switching and gate charge losses. In addition to this basic trade-off, the effect of inductor value on ripple current and low current operation must also be considered.

The inductor value has a direct effect on ripple current. The inductor ripple current, ΔI_L, decreases with higher inductance or higher frequency and increases with higher V_{IN}:

$$\Delta I_L = \frac{1}{(f)(L)} V_{OUT}\left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Accepting larger values of ΔI_L allows the use of low inductances, but results in higher output voltage ripple and greater core losses. A reasonable starting point for setting ripple current is $\Delta I_L = 0.3(I_{MAX})$. The maximum ΔI_L occurs at the maximum input voltage.

The inductor value also has secondary effects. The transition to Burst Mode operation begins when the average inductor current required results in a peak current below 25% of the current limit determined by R_{SENSE}. Lower inductor values (higher ΔI_L) will cause this to occur at lower load currents, which can cause a dip in efficiency in the upper range of low current operation. In Burst Mode operation, lower inductance values will cause the burst frequency to decrease.

Inductor Core Selection

Once the value for L is known, the type of inductor must be selected. High efficiency converters generally cannot afford the core loss found in low cost powdered iron cores, forcing the use of more expensive ferrite or molypermalloy cores. Actual core loss is independent of core size for a fixed inductor value, but it is very dependent on inductance value selected. As inductance increases, core losses go down. Unfortunately, increased inductance requires more turns of wire and therefore copper losses will increase.

Ferrite designs have very low core loss and are preferred for high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates hard, which means that inductance collapses abruptly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current and consequent output voltage ripple. Do not allow the core to saturate!

APPLICATIONS INFORMATION

Power MOSFET and Schottky Diode (Optional) Selection

Two external power MOSFETs must be selected for the LTC3891 controller: one N-channel MOSFET for the top (main) switch, and one N-channel MOSFET for the bottom (synchronous) switch.

The peak-to-peak drive levels are set by the $INTV_{CC}$ voltage. This voltage is typically 5.1V during start-up (see $EXTV_{CC}$ Pin Connection). Consequently, logic-level threshold MOSFETs must be used in most applications. Pay close attention to the BV_{DSS} specification for the MOSFETs as well.

Selection criteria for the power MOSFETs include the on-resistance, $R_{DS(ON)}$, Miller capacitance, C_{MILLER}, input voltage and maximum output current. Miller capacitance, C_{MILLER}, can be approximated from the gate charge curve usually provided on the MOSFET manufacturers' datasheet. C_{MILLER} is equal to the increase in gate charge along the horizontal axis while the curve is approximately flat divided by the specified change in V_{DS}. This result is then multiplied by the ratio of the application applied V_{DS} to the gate charge curve specified V_{DS}. When the IC is operating in continuous mode the duty cycles for the top and bottom MOSFETs are given by:

$$\text{Main Switch Duty Cycle} = \frac{V_{OUT}}{V_{IN}}$$

$$\text{Synchronous Switch Duty Cycle} = \frac{V_{IN} - V_{OUT}}{V_{IN}}$$

The MOSFET power dissipations at maximum output current are given by:

$$P_{MAIN} = \frac{V_{OUT}}{V_{IN}}\left(I_{MAX}\right)^2\left(1+\delta\right)R_{DS(ON)} + \left(V_{IN}\right)^2\left(\frac{I_{MAX}}{2}\right)\left(R_{DR}\right)\left(C_{MILLER}\right)\bullet\left[\frac{1}{V_{INTVCC} - V_{THMIN}} + \frac{1}{V_{THMIN}}\right]\left(f\right)$$

$$P_{SYNC} = \frac{V_{IN} - V_{OUT}}{V_{IN}}\left(I_{MAX}\right)^2\left(1+\delta\right)R_{DS(ON)}$$

where δ is the temperature dependency of $R_{DS(ON)}$ and R_{DR} (approximately 2Ω) is the effective driver resistance at the MOSFET's Miller threshold voltage. V_{THMIN} is the typical MOSFET minimum threshold voltage.

Both MOSFETs have I^2R losses while the topside N-channel equation includes an additional term for transition losses, which are highest at high input voltages. For $V_{IN} < 20V$ the high current efficiency generally improves with larger MOSFETs, while for $V_{IN} > 20V$ the transition losses rapidly increase to the point that the use of a higher $R_{DS(ON)}$ device with lower C_{MILLER} actually provides higher efficiency. The synchronous MOSFET losses are greatest at high input voltage when the top switch duty factor is low or during a short-circuit when the synchronous switch is on close to 100% of the period.

The term $(1+\delta)$ is generally given for a MOSFET in the form of a normalized $R_{DS(ON)}$ vs Temperature curve, but $\delta = 0.005/°C$ can be used as an approximation for low voltage MOSFETs.

A Schottky diode can be inserted in parallel with the bottom MOSFET to conduct during the dead-time between the conduction of the two power MOSFETs. This prevents the body diode of the bottom MOSFET from turning on, storing charge during the dead-time and requiring a reverse recovery period that could cost as much as 3% in efficiency at high V_{IN}. A 1A to 3A Schottky is generally a good compromise for both regions of operation due to the relatively small average current. Larger diodes result in additional transition losses due to their larger junction capacitance.

C_{IN} and C_{OUT} Selection

The selection of C_{IN} is usually based off the worst-case RMS input current. The highest $(V_{OUT})(I_{OUT})$ product needs to be used in the formula shown in Equation 1 to determine the maximum RMS capacitor current requirement.

In continuous mode, the source current of the top MOSFET is a square wave of duty cycle $(V_{OUT})/(V_{IN})$. To prevent large voltage transients, a low ESR capacitor sized for the

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maximum RMS current of one channel must be used. The maximum RMS capacitor current is given by:

$$C_{IN}\ \text{Required}\ I_{RMS} \approx \frac{I_{MAX}}{V_{IN}}\left[\left(V_{OUT}\right)\left(V_{IN}-V_{OUT}\right)\right]^{1/2} \quad (1)$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that capacitor manufacturers' ripple current ratings are often based on only 2000 hours of life. This makes it advisable to further derate the capacitor, or to choose a capacitor rated at a higher temperature than required. Several capacitors may be paralleled to meet size or height requirements in the design. Due to the high operating frequency of the LTC3891, ceramic capacitors can also be used for C_{IN}. Always consult the manufacturer if there is any question.

A small (0.1µF to 1µF) bypass capacitor between the chip V_{IN} pin and ground, placed close to the LTC3891, is also suggested. A small (≤10Ω) resistor placed between C_{IN} (C1) and the V_{IN} pin provides further isolation.

The selection of C_{OUT} is driven by the effective series resistance (ESR). Typically, once the ESR requirement is satisfied, the capacitance is adequate for filtering. The output ripple (ΔV_{OUT}) is approximated by:

$$\Delta V_{OUT} \approx \Delta I_L\left(ESR + \frac{1}{8 \bullet f \bullet C_{OUT}}\right)$$

where f is the operating frequency, C_{OUT} is the output capacitance and ΔI_L is the ripple current in the inductor. The output ripple is highest at maximum input voltage since ΔI_L increases with input voltage.

Setting Output Voltage

The LTC3891 output voltage is set by an external feedback resistor divider carefully placed across the output, as shown in Figure 3. The regulated output voltage is determined by:

$$V_{OUT} = 0.8V\left(1+\frac{R_B}{R_A}\right)$$

To improve the frequency response, a feedforward capacitor, C_{FF}, may be used. Great care should be taken to route the V_{FB} line away from noise sources, such as the inductor or the SW line.

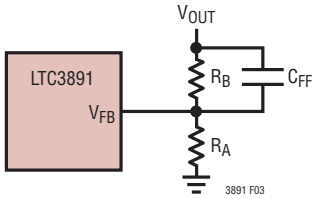


Figure 3. Setting Output Voltage

RUN Pin

The LTC3891 is enabled using the RUN pin. It has a rising threshold of 1.21V with 50mV of hysteresis. Pulling the RUN pin below 1.16V shuts down the main control loop. Pulling it below 0.7V disables the controller and most internal circuits, including the $INTV_{CC}$ LDOs. In this state, the LTC3891 draws only 14µA of quiescent current.

Releasing the RUN pin allows a small 7µA internal current to pull up the pin to enable the controller. The RUN pin may be externally pulled up or driven directly by logic. When driving the RUN pin with a low impedance source, do not exceed the absolute maximum rating of 8V. The RUN pin has an internal 11V voltage clamp that allows the RUN pin to be connected through a resistor to a higher voltage (for example, V_{IN}), so long as the maximum current into the RUN pin does not exceed 100µA.

The RUN pin can be implemented as a UVLO by connecting it to the output of an external resistor divider network off V_{IN}, as shown in Figure 4.

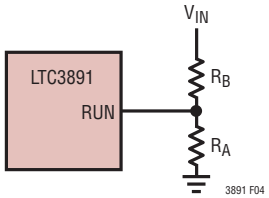


Figure 4. Using the RUN Pin as a UVLO

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The rising and falling UVLO thresholds are calculated using the RUN pin thresholds:

$$V_{UVLO(RISING)} = 1.21V\left(1+\frac{R_B}{R_A}\right)$$

$$V_{UVLO(FALLING)} = 1.16V\left(1+\frac{R_B}{R_A}\right)$$

The resistor values should be carefully chosen such that the absolute maximum ratings of the RUN pin do not get violated over the entire V_{IN} voltage range.

Tracking and Soft-Start (TRACK/SS Pin)

The start-up of V_{OUT} is controlled by the voltage on the TRACK/SS pin. When the voltage on the TRACK/SS pin is less than the internal 0.8V reference, the LTC3891 regulates the V_{FB} pin voltage to the voltage on the TRACK/SS pin instead of 0.8V. The TRACK/SS pin can be used to program an external soft-start function or to allow V_{OUT} to track another supply during start-up.

Soft-start is enabled by simply connecting a capacitor from the TRACK/SS pin to ground, as shown in Figure 5. An internal 10µA current source charges the capacitor, providing a linear ramping voltage at the TRACK/SS pin. The LTC3891 will regulate the V_{FB} pin (and hence V_{OUT}) according to the voltage on the TRACK/SS pin, allowing V_{OUT} to rise smoothly from 0V to its final regulated value. The total soft-start time will be approximately:

$$t_{SS} = C_{SS} \bullet \frac{0.8V}{10\mu A}$$

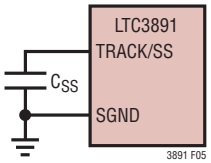


Figure 5. Using the TRACK/SS Pin to Program Soft-Start

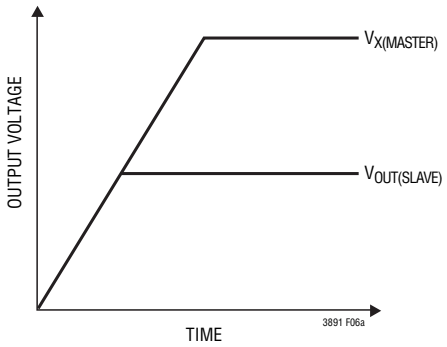
Alternatively, the TRACK/SS pin can be used to track another supply during start-up, as shown qualitatively in Figures 6a and 6b. To do this, a resistor divider should be connected from the master supply (V_X) to the TRACK/SS pin of the slave supply (V_{OUT}), as shown in Figure 7. During start-up V_{OUT} will track V_X according to the ratio set by the resistor divider:

$$\frac{V_X}{V_{OUT}} = \frac{R_A}{R_{TRACKA}} \bullet \frac{R_{TRACKA} + R_{TRACKB}}{R_A + R_B}$$

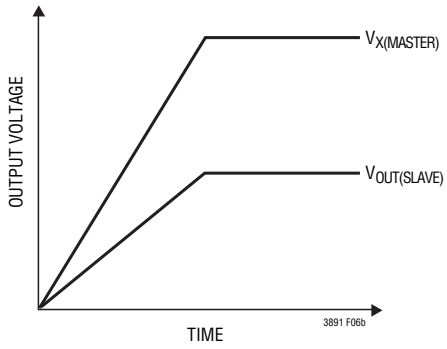
For coincident tracking ($V_{OUT} = V_X$ during start-up):

$R_A = R_{TRACKA}$

$R_B = R_{TRACKB}$



(6a) Coincident Tracking



(6b) Ratiometric Tracking

Figure 6. Two Different Modes of Output Voltage Tracking

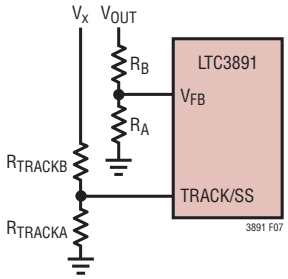


Figure 7. Using the TRACK/SS Pin for Tracking

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$INTV_{CC}$ Regulators

The LTC3891 features two separate internal P-channel low dropout linear regulators (LDO) that supply power at the $INTV_{CC}$ pin from either the V_{IN} supply pin or the $EXTV_{CC}$ pin depending on the connection of the $EXTV_{CC}$ pin. $INTV_{CC}$ powers the gate drivers and much of the LTC3891's internal circuitry. The V_{IN} LDO and the $EXTV_{CC}$ LDO regulate $INTV_{CC}$ to 5.1V. Each of these can supply a peak current of at least 50mA and must be bypassed to ground with a minimum of 2.2µF ceramic capacitor. No matter what type of bulk capacitor is used, an additional 1µF ceramic capacitor placed directly adjacent to the $INTV_{CC}$ and PGND pins is highly recommended. Good bypassing is needed to supply the high transient currents required by the MOSFET gate drivers and to prevent interaction between the channels.

High input voltage applications in which large MOSFETs are being driven at high frequencies may cause the maximum junction temperature rating for the LTC3891 to be exceeded. The $INTV_{CC}$ current, which is dominated by the gate charge current, may be supplied by either the V_{IN} LDO or the $EXTV_{CC}$ LDO. When the voltage on the $EXTV_{CC}$ pin is less than 4.7V, the V_{IN} LDO is enabled. Power dissipation for the IC in this case is highest and is equal to $V_{IN} \bullet I_{INTVCC}$. The gate charge current is dependent on operating frequency as discussed in the Efficiency Considerations section. The junction temperature can be estimated by using the equations given in Note 3 of the Electrical Characteristics. For example, the LTC3891 $INTV_{CC}$ current is limited to less than 32mA from a 40V supply when not using the $EXTV_{CC}$ supply at a 70°C ambient temperature:

$$T_J = 70°C + (32mA)(40V)(43°C/W \text{ for QFN}) = 125°C$$

To prevent the maximum junction temperature from being exceeded, the input supply current must be checked while operating in forced continuous mode (PLLIN/MODE = $INTV_{CC}$) at maximum V_{IN}.

When the voltage applied to $EXTV_{CC}$ rises above 4.7V, the V_{IN} LDO is turned off and the $EXTV_{CC}$ LDO is enabled. The $EXTV_{CC}$ LDO remains on as long as the voltage applied to $EXTV_{CC}$ remains above 4.5V. The $EXTV_{CC}$ LDO attempts to regulate the $INTV_{CC}$ voltage to 5.1V, so while $EXTV_{CC}$ is less than 5.1V, the LDO is in dropout and the $INTV_{CC}$ voltage is approximately equal to $EXTV_{CC}$. When $EXTV_{CC}$ is greater than 5.1V, up to an absolute maximum of 14V, $INTV_{CC}$ is regulated to 5.1V.

Using the $EXTV_{CC}$ LDO allows the MOSFET driver and control power to be derived from one of the LTC3891's switching regulator outputs ($4.7V \le V_{OUT} \le 14V$) during normal operation and from the V_{IN} LDO when the output is out of regulation (e.g., start-up, short-circuit). If more current is required through the $EXTV_{CC}$ LDO than is specified, an external Schottky diode can be added between the $EXTV_{CC}$ and $INTV_{CC}$ pins. In this case, do not apply more than 6V to the $EXTV_{CC}$ pin and make sure that $EXTV_{CC} \le V_{IN}$.

Significant efficiency and thermal gains can be realized by powering $INTV_{CC}$ from the output, since the V_{IN} current resulting from the driver and control currents will be scaled by a factor of (Duty Cycle)/(Switcher Efficiency).

For 5V to 14V regulator outputs, this means connecting the $EXTV_{CC}$ pin directly to V_{OUT}. Tying the $EXTV_{CC}$ pin to an 8.5V supply reduces the junction temperature in the previous example from 125°C to:

$$T_J = 70°C + (32mA)(8.5V)(43°C/W) = 82°C$$

However, for 3.3V and other low voltage outputs, additional circuitry is required to derive $INTV_{CC}$ power from the output.

The following list summarizes the four possible connections for $EXTV_{CC}$:

1. $EXTV_{CC}$ Grounded. This will cause $INTV_{CC}$ to be powered from the internal 5.1V regulator resulting in an efficiency penalty of up to 10% at high input voltages.
2. $EXTV_{CC}$ Connected Directly to V_{OUT}. This is the normal connection for a 5V to 14V regulator and provides the highest efficiency.
3. $EXTV_{CC}$ Connected to an External Supply. If an external supply is available in the 5V to 14V range, it may be used to power $EXTV_{CC}$ providing it is compatible with the MOSFET gate drive requirements. Ensure that $EXTV_{CC} < V_{IN}$.

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4. $EXTV_{CC}$ Connected to an Output-Derived Boost Network. For 3.3V and other low voltage regulators, efficiency gains can still be realized by connecting $EXTV_{CC}$ to an output-derived voltage that has been boosted to greater than 4.7V. This can be done with the capacitive charge pump shown in Figure 8. Ensure that $EXTV_{CC} < V_{IN}$.

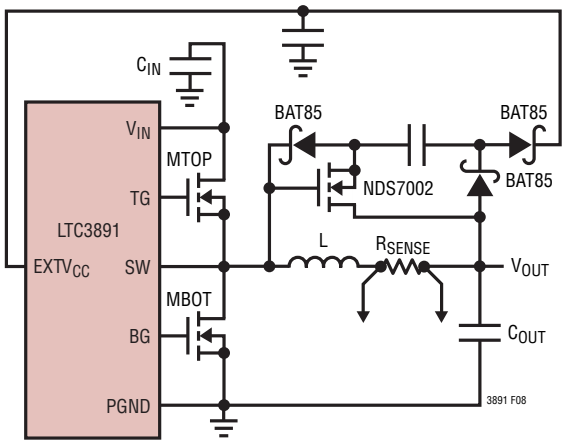


Figure 8. Capacitive Charge Pump for $EXTV_{CC}$

Topside MOSFET Driver Supply (C_B, D_B)

An external bootstrap capacitor, C_B, connected to the BOOST pin supplies the gate drive voltage for the topside MOSFET. Capacitor C_B in the Functional Diagram is charged though external diode D_B from $INTV_{CC}$ when the SW pin is low. When the topside MOSFET is to be turned on, the driver places the C_B voltage across the gate-source of the MOSFET. This enhances the top MOSFET switch and turns it on. The switch node voltage, SW, rises to V_{IN} and the BOOST pin follows. With the topside MOSFET on, the boost voltage is above the input supply: $V_{BOOST} = V_{IN} + V_{INTVCC}$. The value of the boost capacitor, C_B, needs to be 100 times that of the total input capacitance of the topside MOSFET(s). The reverse breakdown of the external Schottky diode must be greater than $V_{IN(MAX)}$.

When adjusting the gate drive level, the final arbiter is the total input current for the regulator. If a change is made and the input current decreases, then the efficiency has improved. If there is no change in input current, then there is no change in efficiency.

Fault Conditions: Current Limit and Current Foldback

The LTC3891 includes current foldback to help limit load current when the output is shorted to ground. If the output voltage falls below 70% of its nominal output level, then the maximum sense voltage is progressively lowered from 100% to 45% of its maximum selected value. Under short-circuit conditions with very low duty cycles, the LTC3891 will begin cycle skipping in order to limit the short-circuit current. In this situation the bottom MOSFET will be dissipating most of the power but less than in normal operation. The short-circuit ripple current is determined by the minimum on-time, $t_{ON(MIN)}$, of the LTC3891 (≈95ns), the input voltage and inductor value:

$$\Delta I_{L(SC)} = t_{ON(MIN)} \left(\frac{V_{IN}}{L} \right)$$

The resulting average short-circuit current is:

$$I_{SC} = 45\% \bullet I_{LIM(MAX)} - \frac{1}{2} \Delta I_{L(SC)}$$

Fault Conditions: Overvoltage Protection (Crowbar)

The overvoltage crowbar is designed to blow a system input fuse when the output voltage of the regulator rises much higher than nominal levels. The crowbar causes huge currents to flow, that blow the fuse to protect against a shorted top MOSFET if the short occurs while the controller is operating.

A comparator monitors the output for overvoltage conditions. The comparator detects faults greater than 10% above the nominal output voltage. When this condition is sensed, the top MOSFET is turned off and the bottom MOSFET is turned on until the overvoltage condition is cleared. The bottom MOSFET remains on continuously for as long as the overvoltage condition persists; if V_{OUT} returns to a safe level, normal operation automatically resumes.

A shorted top MOSFET will result in a high current condition which will open the system fuse. The switching regulator will regulate properly with a leaky top MOSFET by altering the duty cycle to accommodate the leakage.

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Phase-Locked Loop and Frequency Synchronization

The LTC3891 has an internal phase-locked loop (PLL) comprised of a phase frequency detector, a lowpass filter, and a voltage-controlled oscillator (VCO). This allows the turn-on of the top MOSFET to be locked to the rising edge of an external clock signal applied to the PLLIN/MODE pin. The phase detector is an edge sensitive digital type that provides zero degrees phase shift between the external and internal oscillators. This type of phase detector does not exhibit false lock to harmonics of the external clock.

If the external clock frequency is greater than the internal oscillator's frequency, f_{OSC}, then current is sourced continuously from the phase detector output, pulling up the VCO input. When the external clock frequency is less than f_{OSC}, current is sunk continuously, pulling down the VCO input.

If the external and internal frequencies are the same but exhibit a phase difference, the current sources turn on for an amount of time corresponding to the phase difference. The voltage at the VCO input is adjusted until the phase and frequency of the internal and external oscillators are identical. At the stable operating point, the phase detector output is high impedance and the internal filter capacitor, CLP, holds the voltage at the VCO input.

Note that the LTC3891 can only be synchronized to an external clock whose frequency is within range of the LTC3891's internal VCO, which is nominally 55kHz to 900kHz.

This is guaranteed to be between 75kHz and 750kHz. Typically, the external clock (on the PLLIN/MODE pin) input high threshold is 1.6V, while the input low threshold is 1.1V.

Rapid phase locking can be achieved by using the FREQ pin to set a free-running frequency near the desired synchronization frequency. The VCO's input voltage is prebiased at a frequency corresponding to the frequency set by the FREQ pin. Once prebiased, the PLL only needs to adjust the frequency slightly to achieve phase lock and synchronization. Although it is not required that the free-running frequency be near external clock frequency, doing so will prevent the operating frequency from passing through a large range of frequencies as the PLL locks.

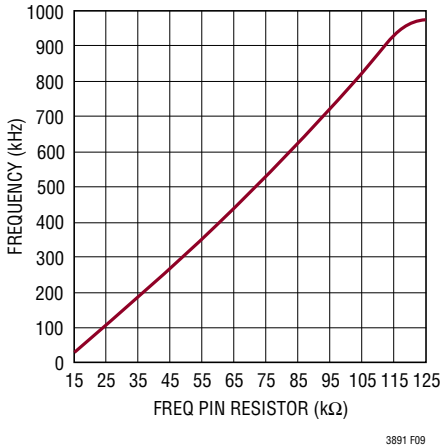


Figure 9. Relationship Between Oscillator Frequency and Resistor Value at the FREQ Pin

Table 2 summarizes the different states in which the FREQ pin can be used.

Table 2

FREQ PIN	PLLIN/MODE PIN	FREQUENCY
0V	DC Voltage	350kHz
$INTV_{CC}$	DC Voltage	535kHz
Resistor	DC Voltage	50kHz to 900kHz
Any of the Above	External Clock	Phase Locked to External Clock

Minimum On-Time Considerations

Minimum on-time, $t_{ON(MIN)}$, is the smallest time duration that the LTC3891 is capable of turning on the top MOSFET. It is determined by internal timing delays and the gate

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charge required to turn on the top MOSFET. Low duty cycle applications may approach this minimum on-time limit and care should be taken to ensure that:

$$t_{ON(MIN)} < \frac{V_{OUT}}{V_{IN}(f)}$$

If the duty cycle falls below what can be accommodated by the minimum on-time, the controller will begin to skip cycles. The output voltage will continue to be regulated, but the ripple voltage and current will increase.

The minimum on-time for the LTC3891 is approximately 95ns. However, as the peak sense voltage decreases the minimum on-time gradually increases up to about 130ns. This is of particular concern in forced continuous applications with low ripple current at light loads. If the duty cycle drops below the minimum on-time limit in this situation, a significant amount of cycle skipping can occur with correspondingly larger current and voltage ripple.

Efficiency Considerations

The percent efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Percent efficiency can be expressed as:

%Efficiency = 100% – (L1 + L2 + L3 + ...)

where L1, L2, etc. are the individual losses as a percentage of input power.

Although all dissipative elements in the circuit produce losses, four main sources usually account for most of the losses in LTC3891 circuits: 1) IC V_{IN} current, 2) $INTV_{CC}$ regulator current, 3) I^2R losses, 4) topside MOSFET transition losses.

1. The V_{IN} current is the DC supply current given in the Electrical Characteristics table, which excludes MOSFET driver and control currents. V_{IN} current typically results in a small (<0.1%) loss.

2. $INTV_{CC}$ current is the sum of the MOSFET driver and control currents. The MOSFET driver current results from switching the gate capacitance of the power MOSFETs. Each time a MOSFET gate is switched from low to high to low again, a packet of charge, dQ, moves from $INTV_{CC}$ to ground. The resulting dQ/dt is a current out of $INTV_{CC}$ that is typically much larger than the control circuit current. In continuous mode, $I_{GATECHG} = f(Q_T + Q_B)$, where Q_T and Q_B are the gate charges of the topside and bottom side MOSFETs.

   Supplying $INTV_{CC}$ from an output-derived source power through $EXTV_{CC}$ will scale the V_{IN} current required for the driver and control circuits by a factor of (Duty Cycle)/(Efficiency). For example, in a 20V to 5V application, 10mA of $INTV_{CC}$ current results in approximately 2.5mA of V_{IN} current. This reduces the midcurrent loss from 10% or more (if the driver was powered directly from V_{IN}) to only a few percent.

3. I^2R losses are predicted from the DC resistances of the fuse (if used), MOSFET, inductor, current sense resistor and input and output capacitor ESR. In continuous mode the average output current flows through L and R_{SENSE}, but is chopped between the topside MOSFET and the synchronous MOSFET. If the two MOSFETs have approximately the same $R_{DS(ON)}$, then the resistance of one MOSFET can simply be summed with the resistances of L, R_{SENSE} and ESR to obtain I^2R losses. For example, if each $R_{DS(ON)} = 30m\Omega$, $R_L = 50m\Omega$, $R_{SENSE} = 10m\Omega$ and $R_{ESR} = 40m\Omega$ (sum of both input and output capacitance losses), then the total resistance is $130m\Omega$. This results in losses ranging from 3% to 13% as the output current increases from 1A to 5A for a 5V output, or a 4% to 20% loss for a 3.3V output. Efficiency varies as the inverse square of V_{OUT} for the same external components and output power level. The combined effects of increasingly lower output voltages and higher currents required by high performance digital systems is not doubling but quadrupling the importance of loss terms in the switching regulator system!

4. Transition losses apply only to the topside MOSFET(s), and become significant only when operating at high input voltages (typically 15V or greater). Transition losses can be estimated from:

   $$\text{Transition Loss} = (1.7) \bullet V_{IN} \bullet 2 \bullet I_{O(MAX)} \bullet C_{RSS} \bullet f$$

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Other hidden losses such as copper trace and internal battery resistances can account for an additional 5% to 10% efficiency degradation in portable systems. It is very important to include these system level losses during the design phase. The internal battery and fuse resistance losses can be minimized by making sure that C_{IN} has adequate charge storage and very low ESR at the switching frequency. A 25W supply will typically require a minimum of 20µF to 40µF of capacitance having a maximum of 20mΩ to 50mΩ of ESR. Other losses including body diode conduction losses during dead-time and inductor core losses generally account for less than 2% total additional loss.

Checking Transient Response

The regulator loop response can be checked by looking at the load current transient response. Switching regulators take several cycles to respond to a step in DC (resistive) load current. When a load step occurs, V_{OUT} shifts by an amount equal to ΔI_{LOAD} (ESR), where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT} generating the feedback error signal that forces the regulator to adapt to the current change and return V_{OUT} to its steady-state value. During this recovery time V_{OUT} can be monitored for excessive overshoot or ringing, which would indicate a stability problem. OPTI-LOOP compensation allows the transient response to be optimized over a wide range of output capacitance and ESR values. The availability of the ITH pin not only allows optimization of control loop behavior, but it also provides a DC coupled and AC filtered closed-loop response test point. The DC step, rise time and settling at this test point truly reflects the closed-loop response. Assuming a predominantly second order system, phase margin and/or damping factor can be estimated using the percentage of overshoot seen at this pin. The bandwidth can also be estimated by examining the rise time at the pin. The ITH external components shown in Figure 10 circuit will provide an adequate starting point for most applications.

The ITH series RC-CC filter sets the dominant pole-zero loop compensation. The values can be modified slightly to optimize transient response once the final PC layout is done and the particular output capacitor type and value have been determined. The output capacitors need to be selected because the various types and values determine the loop gain and phase. An output current pulse of 20% to 80% of full-load current having a rise time of 1µs to 10µs will produce output voltage and ITH pin waveforms that will give a sense of the overall loop stability without breaking the feedback loop.

Placing a power MOSFET directly across the output capacitor and driving the gate with an appropriate signal generator is a practical way to produce a realistic load step condition. The initial output voltage step resulting from the step change in output current may not be within the bandwidth of the feedback loop, so this signal cannot be used to determine phase margin. This is why it is better to look at the ITH pin signal which is in the feedback loop and is the filtered and compensated control loop response.

The gain of the loop will be increased by increasing RC and the bandwidth of the loop will be increased by decreasing CC. If RC is increased by the same factor that CC is decreased, the zero frequency will be kept the same, thereby keeping the phase shift the same in the most critical frequency range of the feedback loop. The output voltage settling behavior is related to the stability of the closed-loop system and will demonstrate the actual overall supply performance.

A second, more severe transient is caused by switching in loads with large (>1µF) supply bypass capacitors. The discharged bypass capacitors are effectively put in parallel with C_{OUT}, causing a rapid drop in V_{OUT}. No regulator can alter its delivery of current quickly enough to prevent this sudden step change in output voltage if the load switch resistance is low and it is driven quickly. If the ratio of C_{LOAD} to C_{OUT} is greater than 1:50, the switch rise time should be controlled so that the load rise time is limited to approximately $25 \bullet C_{LOAD}$. Thus a 10µF capacitor would require a 250µs rise time, limiting the charging current to about 200mA.

Design Example

As a design example, assume V_{IN} = 12V (nominal), V_{IN} = 22V (max), V_{OUT} = 3.3V, I_{MAX} = 5A, $V_{SENSE(MAX)}$ = 75mV and f = 350kHz. The inductance value is chosen first based on a 30% ripple current

APPLICATIONS INFORMATION

assumption. The highest value of ripple current occurs at the maximum input voltage. Tie the FREQ pin to GND, generating 350kHz operation. The minimum inductance for 30% ripple current is:

$$\Delta I_L = \frac{V_{OUT}}{(f)(L)}\left(1-\frac{V_{OUT}}{V_{IN(NOM)}}\right)$$

A 4.7µH inductor will produce 29% ripple current. The peak inductor current will be the maximum DC value plus one half the ripple current, or 5.73A. Increasing the ripple current will also help ensure that the minimum on-time of 95ns is not violated. The minimum on-time occurs at maximum V_{IN}:

$$t_{ON(MIN)} = \frac{V_{OUT}}{V_{IN(MAX)}(f)} = \frac{3.3V}{22V(350kHz)} = 429ns$$

The equivalent R_{SENSE} resistor value can be calculated by using the minimum value for the maximum current sense threshold (64mV):

$$R_{SENSE} \le \frac{64mV}{5.73A} \approx 0.01\Omega$$

Choosing 1% resistors: R_A = 25k and R_B = 78.7k yields an output voltage of 3.32V.

The power dissipation on the topside MOSFET can be easily estimated. Choosing a Fairchild FDS6982S dual MOSFET results in: $R_{DS(ON)}$ = 0.035Ω/0.022Ω, C_{MILLER} = 215pF. At maximum input voltage with T(estimated) = 50°C:

$$P_{MAIN} = \frac{3.3V}{22V}(5A)^2\left[1+(0.005)(50°C-25°C)\right](0.035\Omega)+(22V)^2\frac{5A}{2}(2.5\Omega)(215pF)\bullet\left[\frac{1}{5V-2.3V}+\frac{1}{2.3V}\right](350kHz) = 331mW$$

A short-circuit to ground will result in a folded back current of:

$$I_{SC} = \frac{34mV}{0.01\Omega} - \frac{1}{2}\left(\frac{95ns(22V)}{4.7\mu H}\right) = 3.18A$$

with a typical value of $R_{DS(ON)}$ and δ = (0.005/°C)(25°C) = 0.125. The resulting power dissipated in the bottom MOSFET is:

$$P_{SYNC} = (3.28A)^2(1.125)(0.022\Omega) = 250mW$$

which is less than under full-load conditions. C_{IN} is chosen for an RMS current rating of at least 3A at temperature assuming only this channel is on. C_{OUT} is chosen with an ESR of 0.02Ω for low output ripple. The output ripple in continuous mode will be highest at the maximum input voltage. The output voltage ripple due to ESR is approximately:

$V_{ORIPPLE} = R_{ESR}(\Delta I_L) = 0.02\Omega(1.45A) = 29mV_{P-P}$

PC Board Layout Checklist

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the IC.

Check the following in your layout:

1. Are the signal and power grounds kept separate? The combined IC signal ground pin and the ground return of C_{INTVCC} must return to the combined C_{OUT} (–) terminals. The path formed by the top N-channel MOSFET, Schottky diode and the C_{IN} capacitor should have short leads and PC trace lengths. The output capacitor (–) terminals should be connected as close as possible to the (–) terminals of the input capacitor by placing the capacitors next to each other and away from the Schottky loop described above.
2. Does the LTC3891 V_{FB} pin's resistive divider connect to the (+) terminal of C_{OUT}? The resistive divider must be connected between the (+) terminal of C_{OUT} and signal ground. The feedback resistor connections should not be along the high current input feeds from the input capacitor(s).

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3. Are the SENSE$^-$ and SENSE$^+$ leads routed together with minimum PC trace spacing? The filter capacitor between SENSE$^+$ and SENSE$^-$ should be as close as possible to the IC. Ensure accurate current sensing with Kelvin connections at the SENSE resistor.
4. Is the $INTV_{CC}$ decoupling capacitor connected close to the IC, between the $INTV_{CC}$ and the power ground pins? This capacitor carries the MOSFET drivers' current peaks. An additional 1µF ceramic capacitor placed immediately next to the $INTV_{CC}$ and PGND pins can help improve noise performance substantially.
5. Keep the SW, TG, and BOOST nodes away from sensitive small-signal nodes. All of these nodes have very large and fast moving signals and therefore should be kept on the output side of the LTC3891 and occupy minimum PC trace area.
6. Use a modified star ground technique: a low impedance, large copper area central grounding point on the same side of the PC board as the input and output capacitors with tie-ins for the bottom of the $INTV_{CC}$ decoupling capacitor, the bottom of the voltage feedback resistive divider and the SGND pin of the IC.

PC Board Layout Debugging

It is helpful to use a DC-50MHz current probe to monitor the current in the inductor while testing the circuit. Monitor the output switching node (SW pin) to synchronize the oscilloscope to the internal oscillator and probe the actual output voltage as well. Check for proper performance over the operating voltage and current range expected in the application. The frequency of operation should be maintained over the input voltage range down to dropout and until the output load drops below the low current operation threshold—typically 25% of the maximum designed current level in Burst Mode operation.

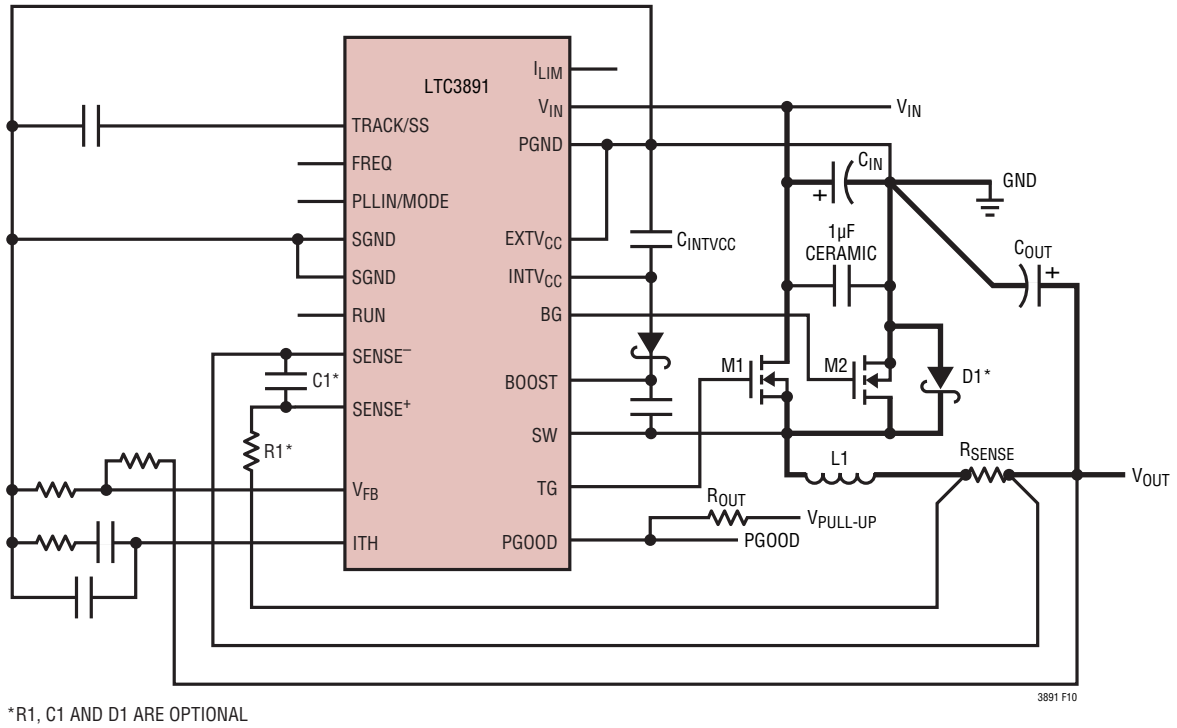
The duty cycle percentage should be maintained from cycle to cycle in a well-designed, low noise PCB implementation. Variation in the duty cycle at a subharmonic rate can suggest noise pickup at the current or voltage sensing inputs or inadequate loop compensation. Overcompensation of the loop can be used to tame a poor PC layout if regulator bandwidth optimization is not required.

Reduce V_{IN} from its nominal level to verify operation of the regulator in dropout. Check the operation of the undervoltage lockout circuit by further lowering V_{IN} while monitoring the outputs to verify operation.

Investigate whether any problems exist only at higher output currents or only at higher input voltages. If problems coincide with high input voltages and low output currents, look for capacitive coupling between the BOOST, SW, TG, and possibly BG connections and the sensitive voltage and current pins. The capacitor placed across the current sensing pins needs to be placed immediately adjacent to the pins of the IC. This capacitor helps to minimize the effects of differential noise injection due to high frequency capacitive coupling. If problems are encountered with high current output loading at lower input voltages, look for inductive coupling between C_{IN}, Schottky and the top MOSFET components to the sensitive current and voltage sensing traces. In addition, investigate common ground path voltage pickup between these components and the SGND pin of the IC.

An embarrassing problem, which can be missed in an otherwise properly working switching regulator, results when the current sensing leads are hooked up backwards. The output voltage under this improper hookup will still be maintained but the advantages of current mode control will not be realized. Compensation of the voltage loop will be much more sensitive to component selection. This behavior can be investigated by temporarily shorting out the current sensing resistor—don't worry, the regulator will still maintain control of the output voltage.

APPLICATIONS INFORMATION



*R1, C1 AND D1 ARE OPTIONAL

Figure 10. Recommended Printed Circuit Layout Diagram

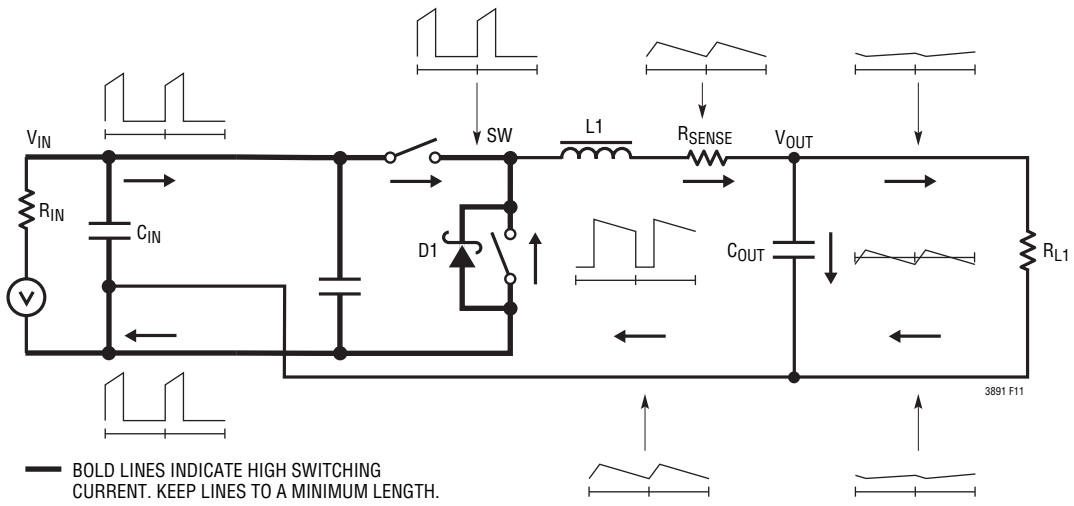
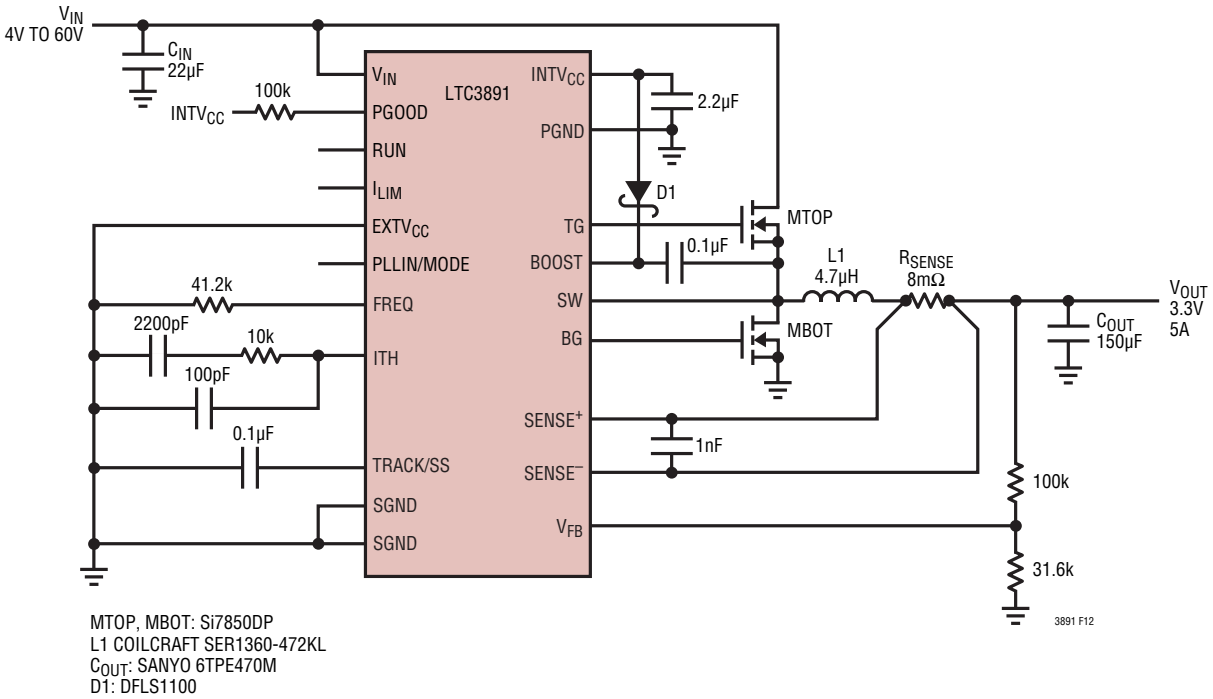


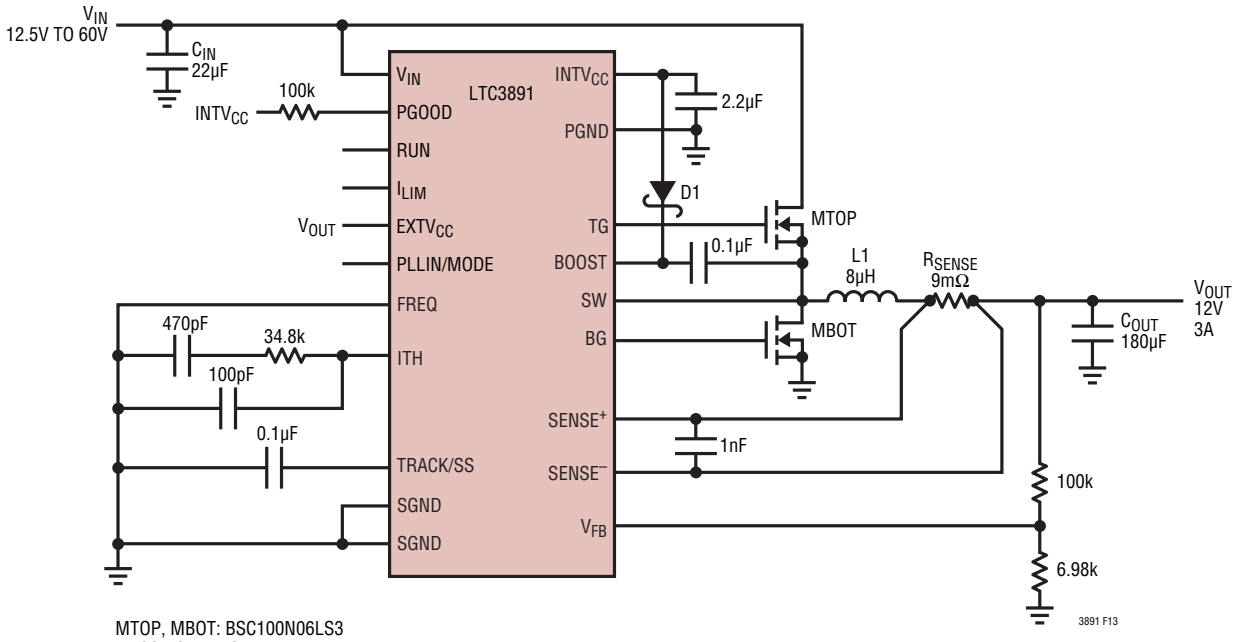
Figure 11. Branch Current Waveforms

APPLICATIONS INFORMATION



MTOP, MBOT: Si7850DP
L1 COILCRAFT SER1360-472KL
C_{OUT}: SANYO 6TPE470M
D1: DFLS1100

Figure 12. High Efficiency 3.3V Step-Down Converter



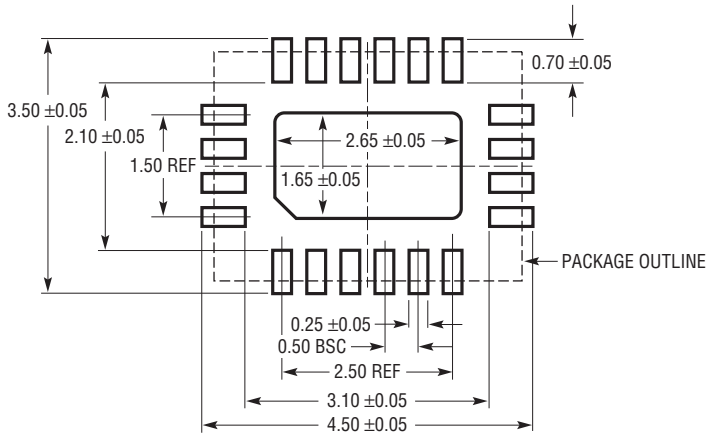
MTOP, MBOT: BSC100N06LS3
L1 COILCRAFT SER1360-802KL
C_{OUT}: SANYO 16SVP180MX
D1: DFLS1100

Figure 13. High Efficiency 12V Step-Down Converter

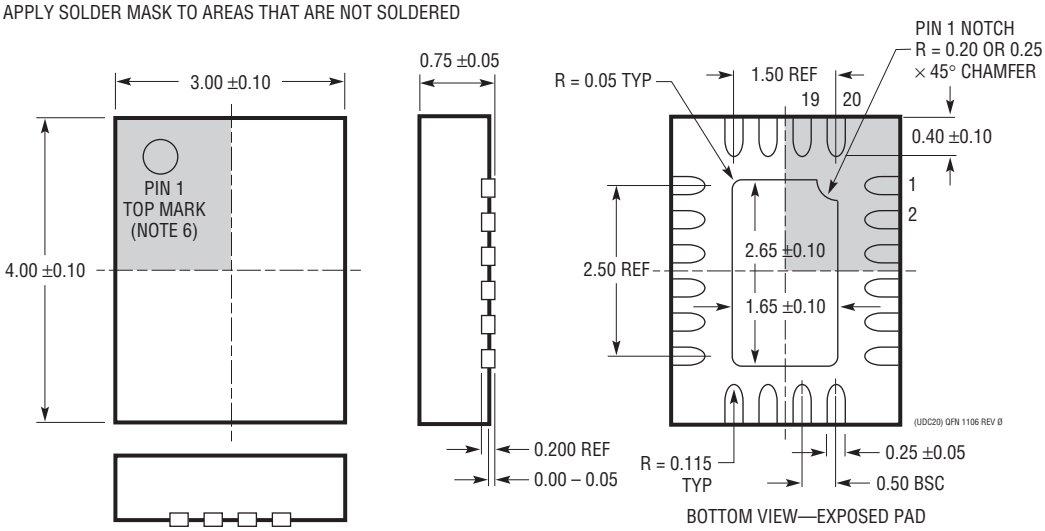
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

UDC Package
20-Lead Plastic QFN (3mm × 4mm)
(Reference LTC DWG # 05-08-1742 Rev Ø)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



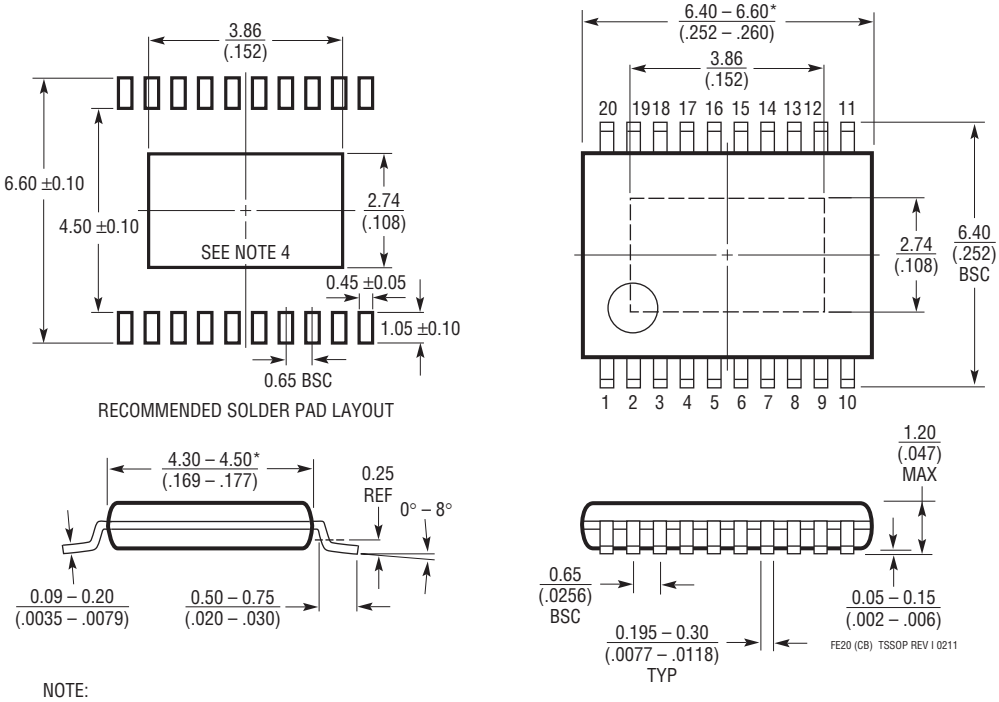
BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

FE Package
20-Lead Plastic TSSOP (4.4mm)
(Reference LTC DWG # 05-08-1663 Rev I)
Exposed Pad Variation CB



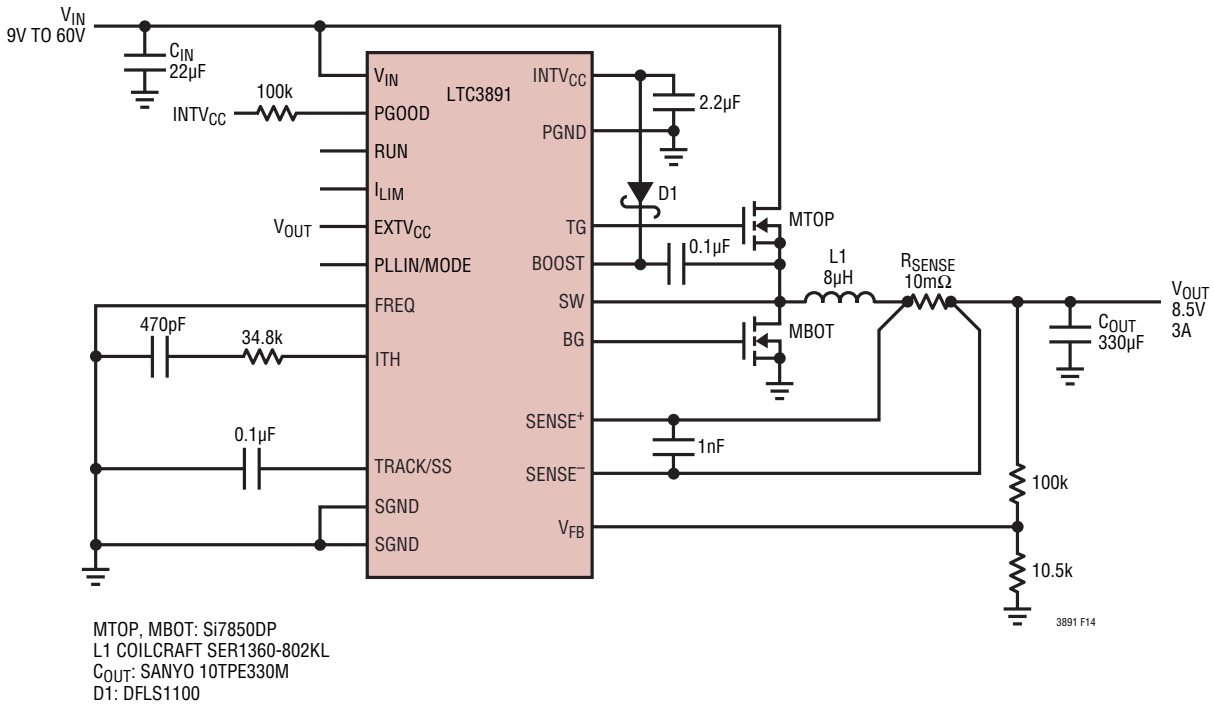
NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN $\frac{\text{MILLIMETERS}}{(\text{INCHES})}$
3. DRAWING NOT TO SCALE
4. RECOMMENDED MINIMUM PCB METAL SIZE FOR EXPOSED PAD ATTACHMENT
*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.150mm (.006") PER SIDE

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	10/12	Added $INTV_{CC}$ to Absolute Maximum Ratings	2
		Updated FE package	30

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

TYPICAL APPLICATION



MTOP, MBOT: Si7850DP
L1 COILCRAFT SER1360-802KL
C_{OUT}: SANYO 10TPE330M
D1: DFLS1100

Figure 14. High Efficiency 8.5V Step-Down Converter

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC3890/LTC3890-1	60V, Low I_Q, Dual Output 2-Phase Synchronous Step-Down DC/DC Controller	Phase-Lockable Fixed Frequency 50kHz to 900kHz, 4V ≤ V_{IN} ≤ 60V, 0.8V ≤ V_{OUT} ≤ 24V, I_Q = 50µA
LTC3857/LTC3857-1	Low I_Q, Dual Output 2-Phase Synchronous Step-Down DC/DC Controllers with 99% Duty Cycle	Phase-Lockable Fixed Frequency 50kHz to 900kHz, 4V ≤ V_{IN} ≤ 38V, 0.8V ≤ V_{OUT} ≤ 24V, I_Q = 50µA
LTC3858/LTC3858-1	Low I_Q, Dual Output 2-Phase Synchronous Step-Down DC/DC Controllers with 99% Duty Cycle	Phase-Lockable Fixed Frequency 50kHz to 900kHz, 4V ≤ V_{IN} ≤ 38V, 0.8V ≤ V_{OUT} ≤ 24V, I_Q = 170µA
LTC3868/LTC3868-1	Low I_Q, Dual Output 2-Phase Synchronous Step-Down DC/DC Controller with 99% Duty Cycle	Phase-Lockable Fixed Frequency 50kHz to 900kHz, 4V ≤ V_{IN} ≤ 24V, 0.8V ≤ V_{OUT} ≤ 14V, I_Q = 170µA
LTC3834/LTC3834-1	Low I_Q, Single Output Synchronous Step-Down DC/DC Controller with 99% Duty Cycle	Phase-Lockable Fixed Frequency 140kHz to 650kHz, 4V ≤ V_{IN} ≤ 36V, 0.8V ≤ V_{OUT} ≤ 10V, I_Q = 30µA
LTC3835/LTC3835-1	Low I_Q, Single Output Synchronous Step-Down DC/DC Controller with 99% Duty Cycle	Phase-Lockable Fixed Frequency 140kHz to 650kHz, 4V ≤ V_{IN} ≤ 36V, 0.8V ≤ V_{OUT} ≤ 10V, I_Q = 80µA
LT3845A	60V, Low I_Q, Single Output Synchronous Step-Down DC/DC Controller	Adjustable Fixed Frequency 100kHz to 500kHz, 4V ≤ V_{IN} ≤ 60V, 1.23V ≤ V_{OUT} ≤ 36V, I_Q = 120µA
LTC3859	Low I_Q, Triple Output Buck/Buck/Boost Synchronous DC/DC Controller	Outputs ≥ 4V Remain in Regulation Through Cold Crank, 2.5V ≤ V_{IN} ≤ 38V, $V_{OUT(BUCKS)}$ Up to 24V, $V_{OUT(BOOST)}$ Up to 60V, I_Q = 55µA
LTC3824	Low I_Q, Single Output Step-Down Controller, 100% Duty Cycle	Fixed 200kHz to 600kHz, 4V ≤ V_{IN} ≤ 60V, 0.8V ≤ V_{OUT} ≤ V_{IN}, I_Q = 40µA, MSOP-10E

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