Low I_Q, Dual 2-Phase Synchronous Step-Down Controller

FEATURES

- **Low Operating I_Q: 170µA (One Channel On)**
- **Wide Output Voltage Range: 0.8V ≤ V_{OUT} ≤ 24V**
- **Wide V_{IN} Range: 4V to 38V**
- **R_{SENSE} or DCR Current Sensing**
- Out-of-Phase Controllers Reduce Required Input Capacitance and Power Supply Induced Noise
- OPTI-LOOP® Compensation Minimizes C_{OUT}
- Phase-Lockable Frequency (75kHz-850kHz)
- Programmable Fixed Frequency (50kHz-900kHz)
- Selectable Continuous, Pulse-Skipping or Burst Mode® Operation at Light Loads
- Very Low Dropout Operation: 99% Duty Cycle
- Adjustable Output Voltage Soft-Start or Tracking
- Power Good Output Voltage Monitor
- Low Shutdown I_Q: 8µA
- Internal LDO Powers Gate Drive from V_{IN} or $EXTV_{CC}$
- No Current Foldback During Start-Up
- 5mm × 5mm QFN Package

APPLICATIONS

- Automotive Systems
- Battery Operated Digital Devices
- Distributed DC Power Systems

DESCRIPTION

The LTC®3858-2 is a high performance dual step-down switching regulator controller that drives all N-channel synchronous power MOSFET stages. A constant frequency current mode architecture allows a phase-lockable frequency of up to 850kHz. Power loss and noise due to the input capacitor ESR are minimized by operating the two controller outputs out of phase.

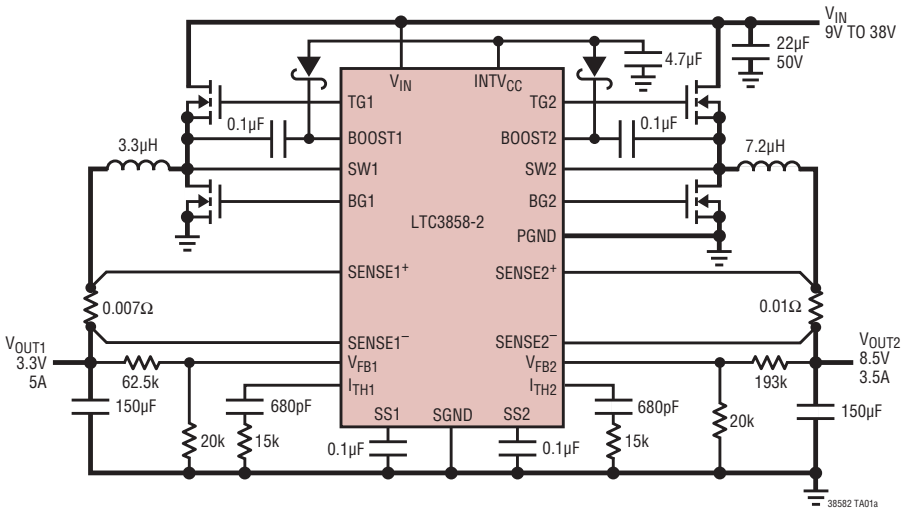
The 170µA no-load quiescent current extends operating life in battery-powered systems. OPTI-LOOP compensation allows the transient response to be optimized over a wide range of output capacitance and ESR values. The LTC3858-2 differs from the LTC3858 by having the overvoltage protection crowbar and short-circuit latchoff disabled. A wide 4V to 38V input supply range encompasses a wide range of intermediate bus voltages and battery chemistries.

Independent soft-start pins for each controller ramp the output voltages during start-up. Current foldback limits MOSFET heat dissipation during short-circuit conditions.

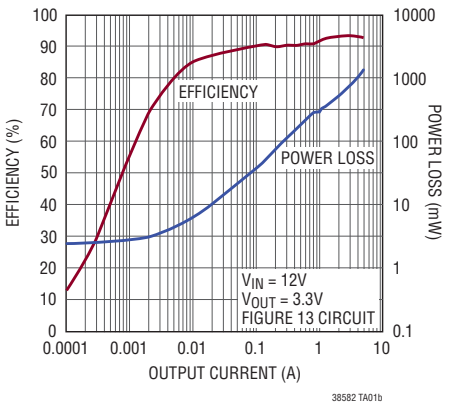
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TYPICAL APPLICATION

High Efficiency Dual 8.5V/3.3V Step-Down Converter



Efficiency and Power Loss vs Load Current

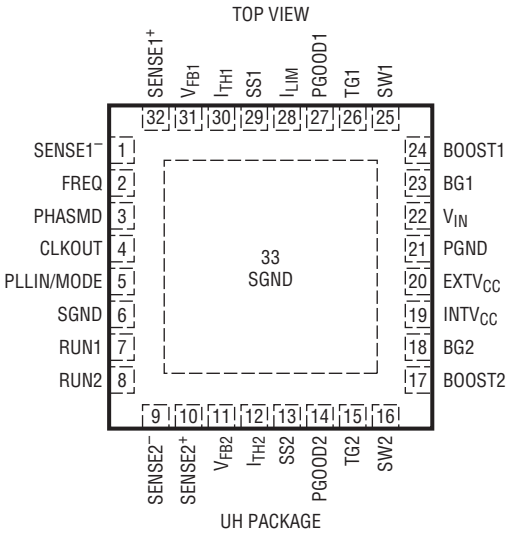


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Input Supply Voltage (V_{IN}) ..... –0.3V to 40V
Topside Driver Voltages
BOOST1, BOOST2 ..... –0.3V to 46V
Switch Voltage (SW1, SW2) ..... –5V to 40V
(BOOST1-SW1), (BOOST2-SW2) ..... –0.3V to 6V
RUN1, RUN2 ..... –0.3V to 8V
Maximum Current Sourced into Pin
from Source >8V 100µA
$SENSE1^+$, $SENSE2^+$, $SENSE1^-$
$SENSE2^-$ Voltages ..... –0.3V to 28V
PLLIN/MODE Voltage ..... –0.3V to 6V
I_{LIM}, PHASMD, FREQ Voltages ..... –0.3V to $INTV_{CC}$
$EXTV_{CC}$ ..... –0.3V to 14V
I_{TH1}, I_{TH2}, V_{FB1}, V_{FB2} Voltages ..... –0.3V to 6V
PGOOD1, PGOOD2 Voltages ..... –0.3V to 6V
SS1, SS2, $INTV_{CC}$ Voltages ..... –0.3V to 6V
Operating Junction Temperature Range
(Note 2) ..... –40°C to 125°C
Maximum Junction Temperature (Note 3) ..... 125°C
Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



UH PACKAGE
32-LEAD (5mm × 5mm) PLASTIC QFN
T_{JMAX} = 125°C, θ_{JA} = 34°C/W
EXPOSED PAD (PIN 33) IS SGND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3858EUH-2#PBF	LTC3858EUH-2#TRPBF	38582	32-Lead (5mm × 5mm) Plastic QFN	–40°C to 125°C
LTC3858IUH-2#PBF	LTC3858IUH-2#TRPBF	38582	32-Lead (5mm × 5mm) Plastic QFN	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{IN} = 12V, $V_{RUN1,2}$ = 5V, $EXTV_{CC}$ = 0V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Input Supply Operating Voltage Range			4		38	V
$V_{FB1,2}$	Regulated Feedback Voltage	(Note 4) $I_{TH1,2}$ = 1.2V –40°C to 125°C –40°C to 85°C	 ● ●	 0.788 0.792	 0.800 0.800	 0.812 0.808	 V V
$I_{FB1,2}$	Feedback Current	(Note 4)			±5	±50	nA
$V_{REFLNREG}$	Reference Voltage Line Regulation	(Note 4) V_{IN} = 4.5V to 38V			0.002	0.02	%/V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{IN} = 12V, $V_{RUN1,2}$ = 5V, $EXTV_{CC}$ = 0V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$V_{LOADREG}$	Output Voltage Load Regulation	(Note 4) Measured in Servo Loop, ΔI_{TH} Voltage = 1.2V to 0.7V	●		0.01	0.1	%
		(Note 4) Measured in Servo Loop, ΔI_{TH} Voltage = 1.2V to 2V	●		–0.01	–0.1	%
$g_{m1,2}$	Transconductance Amplifier g_m	(Note 4) $I_{TH1,2}$ = 1.2V, Sink/Source = 5µA			2		mmho
I_Q	Input DC Supply Current	(Note 5)					
	Pulse-Skipping or Forced Continuous Mode (One Channel On)	RUN1 = 5V and RUN2 = 0V, V_{FB1} = 0.83V (No Load) or RUN1 = 0V and RUN2 = 5V, V_{FB2} = 0.83V (No Load)			1.3		mA
	Pulse-Skipping or Forced Continuous Mode (Both Channels On)	RUN1,2 = 5V, $V_{FB1,2}$ = 0.83V (No Load)			2		mA
	Sleep Mode (One Channel On)	RUN1 = 5V and RUN2 = 0V, V_{FB1} = 0.83V (No Load) or RUN1 = 0V and RUN2 = 5V, V_{FB2} = 0.83V (No Load)			170	250	µA
	Sleep Mode (Both Channels On)	RUN1,2 = 5V, $V_{FB1,2}$ = 0.83V (No Load)			300	450	µA
	Shutdown	RUN1,2 = 0V			8	20	µA
UVLO	Undervoltage Lockout	$INTV_{CC}$ Ramping Up $INTV_{CC}$ Ramping Down	● ●	 3.6	4.0 3.8	4.2 4	V V
V_{OVL}	Feedback Overvoltage Protection	Measured at $V_{FB1,2}$, Relative to Regulated $V_{FB1,2}$		7	10	13	%
I_{SENSE}^+	SENSE+ Pins Current	Each Channel				±1	µA
I_{SENSE}^-	SENSE– Pins Current	Each Channel $V_{OUT1,2} < INTV_{CC} – 0.5V$ $V_{OUT1,2} > INTV_{CC} + 0.5V$			 550	±1	 µA µA
DF_{MAX}	Maximum Duty Factor	In Dropout, FREQ = 0V		98	99		%
$I_{SS1,2}$	Soft-Start Charge Current	$V_{SS1,2}$ = 0V		0.7	1.0	1.4	µA
$V_{RUN1,2}$ On	RUN Pin On Threshold Voltage	V_{RUN1}, V_{RUN2} Rising	●	1.21	1.26	1.31	V
$V_{RUN1,2}$ Hyst	RUN Pin Hysteresis Voltage				50		mV
$V_{SENSE(MAX)}$	Maximum Current Sense Threshold Voltage	$V_{FB1,2}$ = 0.7V, $V_{SENSE1^-,2^-}$ = 3.3V, I_{LIM} = 0 $V_{FB1,2}$ = 0.7V, $V_{SENSE1^-,2^-}$ = 3.3V, I_{LIM} = FLOAT $V_{FB1,2}$ = 0.7V, $V_{SENSE1^-,2^-}$ = 3.3V, I_{LIM} = $INTV_{CC}$	● ● ●	22 43 64	30 50 75	36 57 86	mV mV mV
Gate Driver							
TG1,2	Pull-Up On-Resistance Pull-Down On-Resistance				2.5 1.5		Ω Ω
BG1,2	Pull-Up On-Resistance Pull-Down On-Resistance				2.4 1.1		Ω Ω
 TG1,2 t_r TG1,2 t_f	TG Transition Time: Rise Time Fall Time	(Note 6) C_{LOAD} = 3300pF C_{LOAD} = 3300pF			 25 16		 ns ns
 BG1,2 t_r BG1,2 t_f	BG Transition Time: Rise Time Fall Time	(Note 6) C_{LOAD} = 3300pF C_{LOAD} = 3300pF			 28 13		 ns ns
TG/BG t_{1D}	Top Gate Off to Bottom Gate On Delay Synchronous Switch-On Delay Time	C_{LOAD} = 3300pF Each Driver			30		ns
BG/TG t_{1D}	Bottom Gate Off to Top Gate On Delay Top Switch-On Delay Time	C_{LOAD} = 3300pF Each Driver			30		ns
$t_{ON(MIN)}$	Minimum On-Time	(Note 7)			95		ns

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{IN} = 12V, $V_{RUN1,2}$ = 5V, $EXTV_{CC}$ = 0V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$INTV_{CC}$ Linear Regulator							
$V_{INTVCCVIN}$	Internal V_{CC} Voltage	6V < V_{IN} < 38V, V_{EXTVCC} = 0V		4.85	5.1	5.35	V
V_{LDOVIN}	$INTV_{CC}$ Load Regulation	I_{CC} = 0mA to 50mA, V_{EXTVCC} = 0V			0.7	1.1	%
$V_{INTVCCEXT}$	Internal V_{CC} Voltage	6V < V_{EXTVCC} < 13V		4.85	5.1	5.35	V
V_{LDOEXT}	$INTV_{CC}$ Load Regulation	I_{CC} = 0mA to 50mA, V_{EXTVCC} = 8.5V			0.6	1.1	%
V_{EXTVCC}	$EXTV_{CC}$ Switchover Voltage	$EXTV_{CC}$ Ramping Positive		4.5	4.7	4.9	V
V_{LDOHYS}	$EXTV_{CC}$ Hysteresis Voltage				250		mV
Oscillator and Phase-Locked Loop							
$f_{25k\Omega}$	Programmable Frequency	R_{FREQ} = 25k, PLLIN/MODE = DC Voltage			105		kHz
$f_{65k\Omega}$	Programmable Frequency	R_{FREQ} = 65k, PLLIN/MODE = DC Voltage		375	440	505	kHz
$f_{105k\Omega}$	Programmable Frequency	R_{FREQ} = 105k, PLLIN/MODE = DC Voltage			835		kHz
f_{LOW}	Low Fixed Frequency	V_{FREQ} = 0V, PLLIN/MODE = DC Voltage		320	350	380	kHz
f_{HIGH}	High Fixed Frequency	V_{FREQ} = $INTV_{CC}$, PLLIN/MODE = DC Voltage		485	535	585	kHz
f_{SYNC}	Synchronizable Frequency	PLLIN/MODE = External Clock	●	75		850	kHz
PGOOD1 and PGOOD2 Outputs							
V_{PGL}	PGOOD Voltage Low	I_{PGOOD} = 2mA			0.2	0.4	V
I_{PGOOD}	PGOOD Leakage Current	V_{PGOOD} = 5V				±1	µA
V_{PG}	PGOOD Trip Level	V_{FB} with Respect to Set Regulated Voltage V_{FB} Ramping Negative Hysteresis		–13	–10 2.5	–7	% %
		V_{FB} with Respect to Set Regulated Voltage V_{FB} Ramping Positive Hysteresis		7	10 2.5	13	% %
t_{PG}	Delay for Reporting a Fault (PGOOD Low)				25		µs

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Ratings for extended periods may affect device reliability and lifetime.

Note 2: The LTC3858-2 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC3858E-2 is guaranteed to meet performance specifications from 0°C to 85°C. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3858I-2 is guaranteed over the full –40°C to 125°C operating junction temperature range. Note that the maximum ambient temperature is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance and other environmental factors.

Note 3: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formula:

$$T_J = T_A + (P_D \bullet 34°C/W)$$

Note 4: The LTC3858-2 is tested in a feedback loop that servos $V_{ITH1,2}$ to a specified voltage and measures the resultant $V_{FB1,2}$. The specification at 85°C is not tested in production. This specification is assured by design, characterization and correlation to production testing at 125°C.

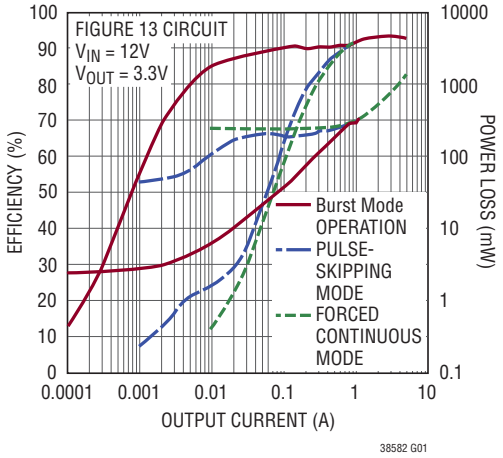
Note 5: Dynamic supply current is higher due to the gate charge being delivered at the switching frequency. See the Applications information section.

Note 6: Rise and fall times are measured using 10% and 90% levels. Delay times are measured using 50% levels

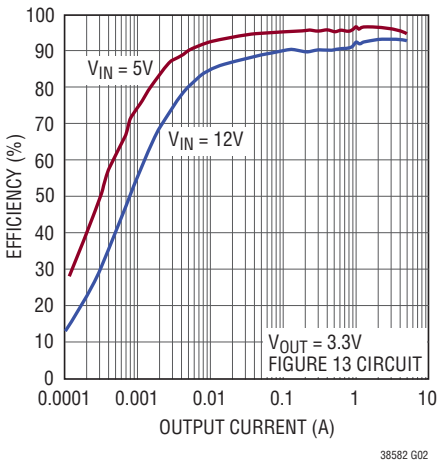
Note 7: The minimum on-time condition is specified for an inductor peak-to-peak ripple current ≥ of 40% I_{MAX} (See Minimum On-Time Considerations in the Applications Information section).

TYPICAL PERFORMANCE CHARACTERISTICS

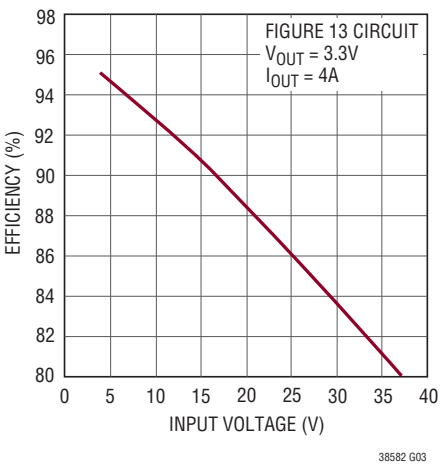
Efficiency and Power Loss vs Output Current



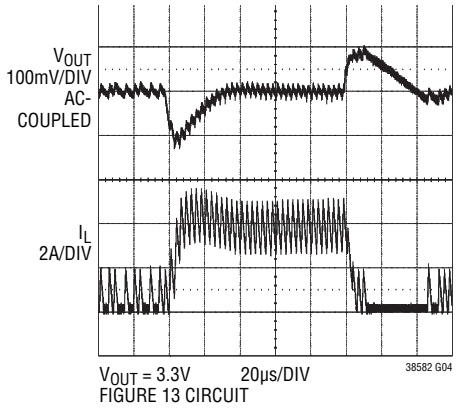
Efficiency vs Output Current



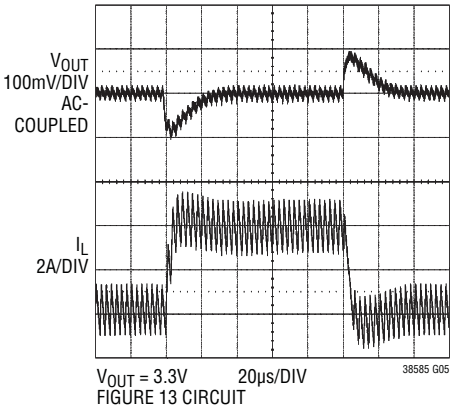
Efficiency vs Input Voltage



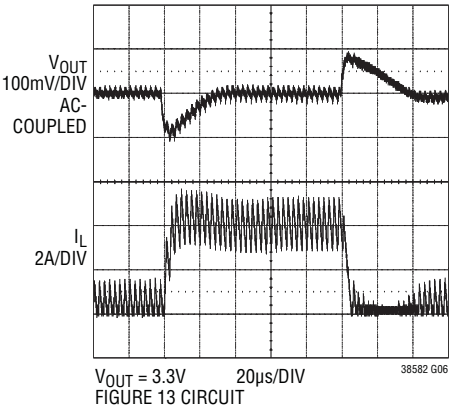
Load Step (Burst Mode Operation)



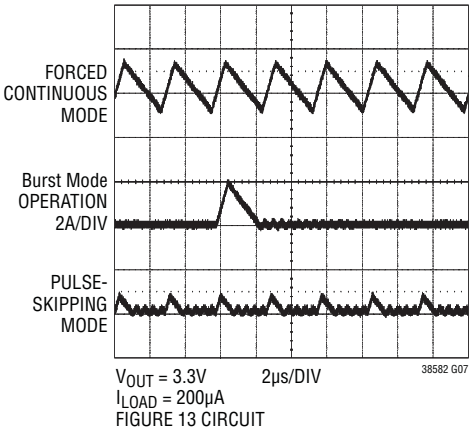
Load Step (Forced Continuous Mode)



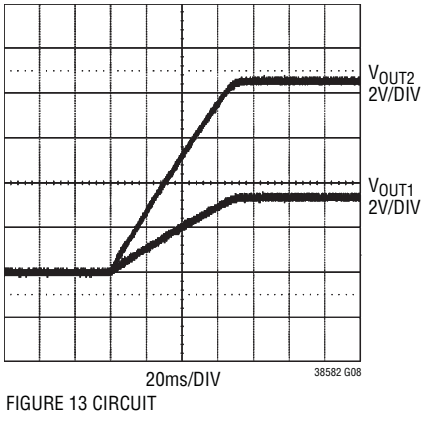
Load Step (Pulse-Skipping Mode)



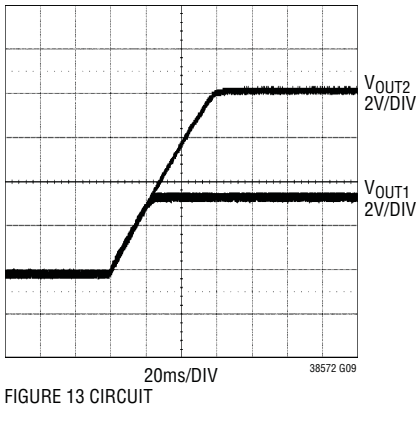
Inductor Current at Light Load



Soft-Start

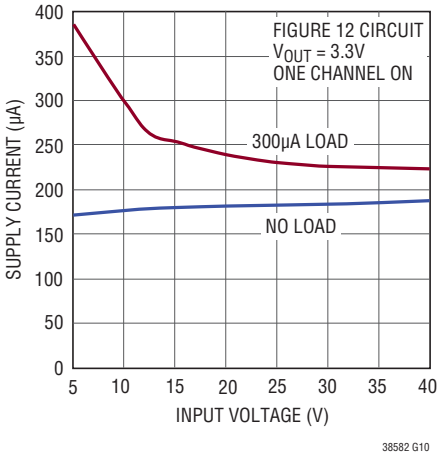


Tracking Start-Up



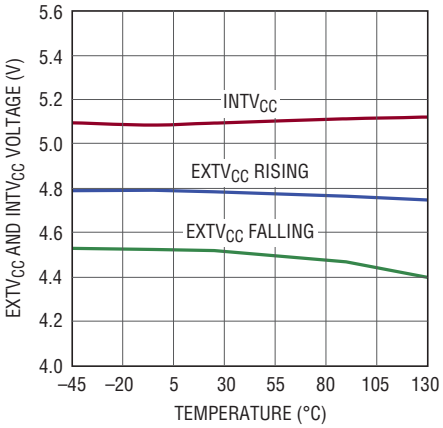
TYPICAL PERFORMANCE CHARACTERISTICS

Total Input Supply Current vs Input Voltage



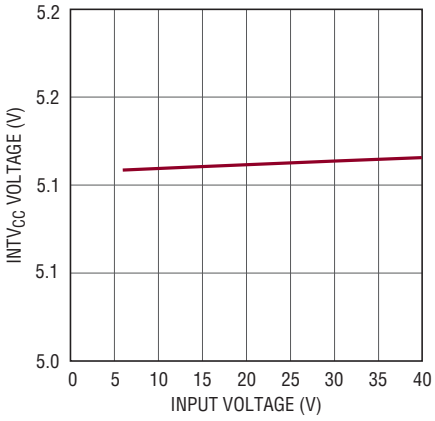
38582 G10

EXTVCC Switchover and INTVCC Voltages vs Temperature



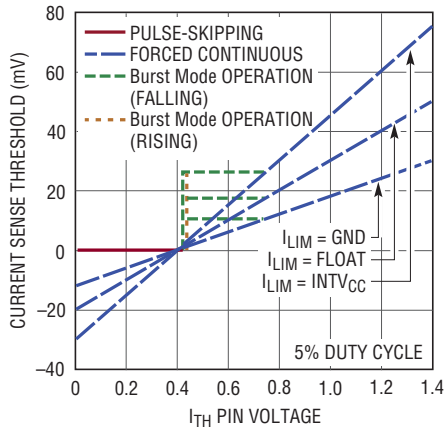
38582 G11

INTVCC Line Regulation



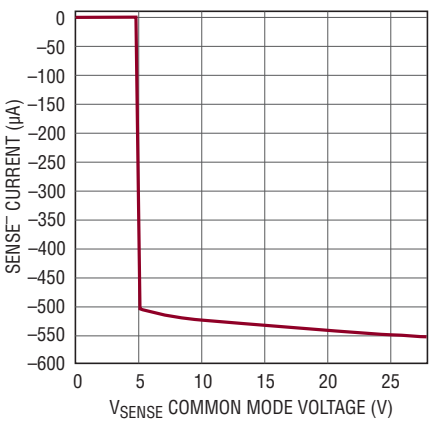
38582 G12

Maximum Current Sense Voltage vs ITH Voltage



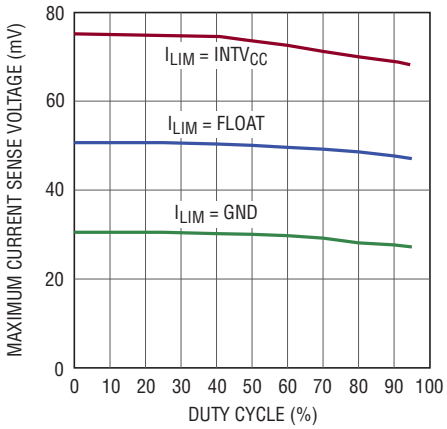
38582 G13

SENSE– Pin Input Bias Current



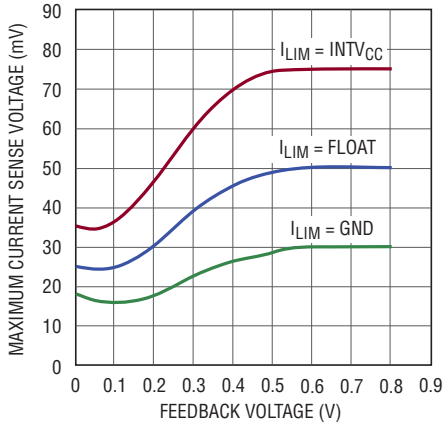
38582 G14

Maximum Current Sense Threshold vs Duty Cycle



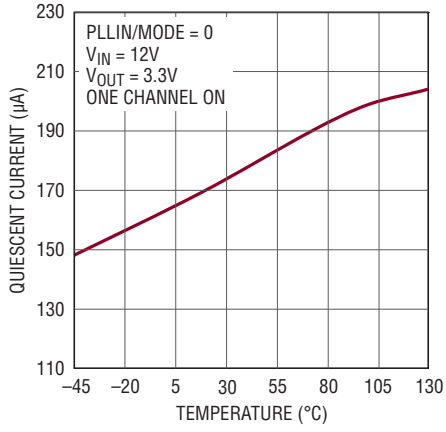
38582 G15

Foldback Current Limit



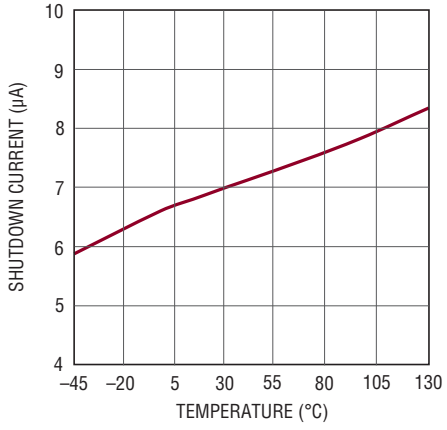
38582 G16

Quiescent Current vs Temperature



38582 G17

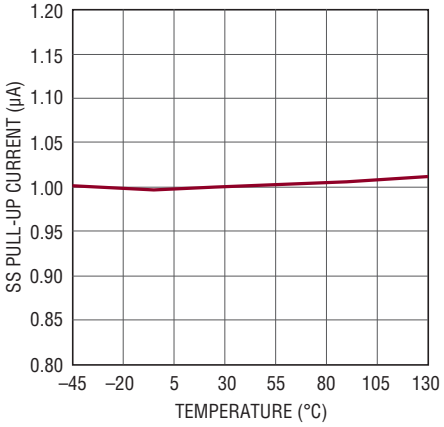
Shutdown Current vs Temperature



38582 G18

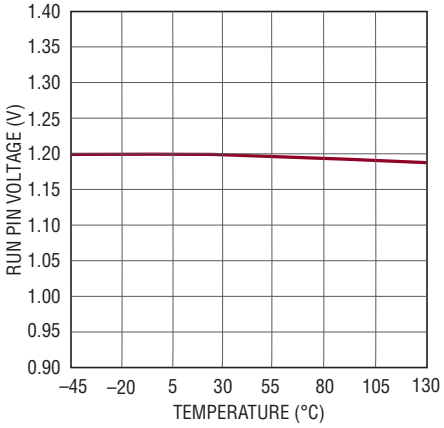
TYPICAL PERFORMANCE CHARACTERISTICS

Soft-Start Pull-Up Current vs Temperature



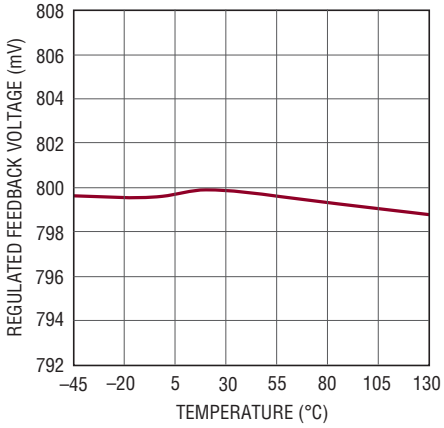
38582 G19

Shutdown (RUN) Threshold vs Temperature



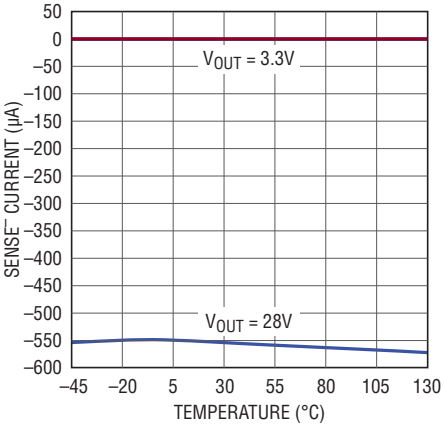
38582 G20

Regulated Feedback Voltage vs Temperature



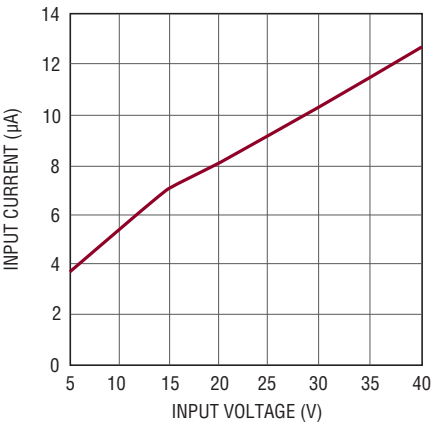
38582 G21

SENSE– Pin Input Current vs Temperature



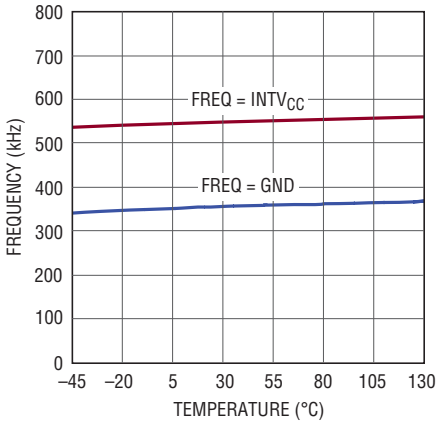
38582 G22

Shutdown Input Current vs Input Voltage



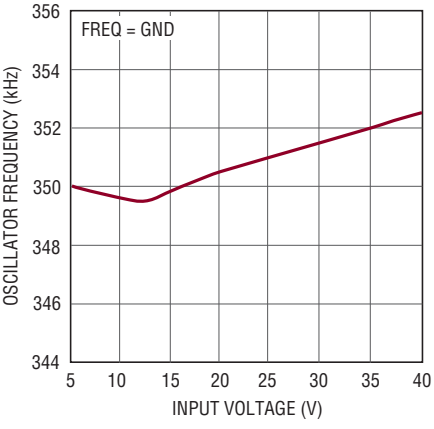
38582 G23

Oscillator Frequency vs Temperature



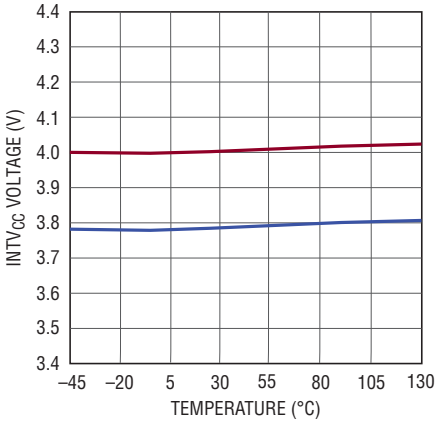
38582 G24

Oscillator Frequency vs Input Voltage



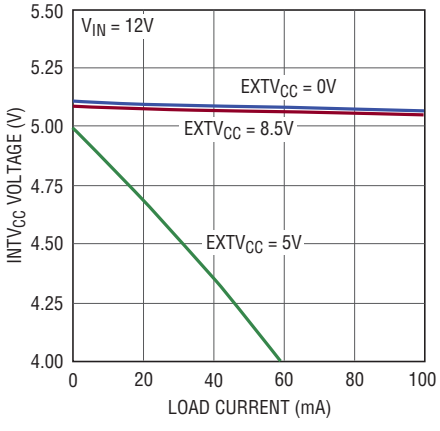
38582 G25

Undervoltage Lockout Threshold vs Temperature



38582 G26

INTVCC vs Load Current



38582 G27

PIN FUNCTIONS

SENSE1$^-$, SENSE2$^-$ (Pin 1, Pin 9): The (–) Input to the Differential Current Comparators. When greater than $INTV_{CC}$ – 0.5V, the SENSE$^-$ pin supplies current to the current comparator.

FREQ (Pin 2): The Frequency Control Pin for the Internal Voltage-Controlled Oscillator (VCO). Connecting this pin to GND forces the VCO to a fixed low frequency of 350kHz. Connecting this pin to $INTV_{CC}$ forces the VCO to a fixed high frequency of 535kHz. Other frequencies between 50kHz and 900kHz can be programmed using a resistor between FREQ and GND. An internal 20µA pull-up current develops the voltage to be used by the VCO to control the frequency

PHASMD (Pin 3): Control input to phase selector which determines the phase relationships between controller 1, controller 2 and the CLKOUT signal. Pulling this pin to ground forces TG2 and CLKOUT to be out of phase 180° and 60° with respect to TG1. Connecting this pin to $INTV_{CC}$ forces TG2 and CLKOUT to be out of phase 240° and 120° with respect to TG1. Floating this pin forces TG2 and CLKOUT to be out of phase 180° and 90° with respect to TG1. Refer to the Table 1.

CLKOUT (Pin 4): Output clock signal available to daisy-chain other controller ICs for additional MOSFET driver stages/phases. The output levels swing from $INTV_{CC}$ to ground.

PLLIN/MODE (Pin 5): External Synchronization Input to Phase Detector and Forced Continuous Mode Input. When an external clock is applied to this pin, the phase-locked loop will force the rising TG1 signal to be synchronized with the rising edge of the external clock. When not synchronizing to an external clock, this input, which acts on both controllers, determines how the LTC3858-2 operates at light loads. Pulling this pin to ground selects Burst Mode operation. An internal 100k resistor to ground also invokes Burst Mode operation when the pin is floated. Tying this pin to $INTV_{CC}$ forces continuous inductor current operation. Tying this pin to a voltage greater than 1.2V and less than $INTV_{CC}$ – 1.3V selects pulse-skipping operation.

SGND (Pin 6, Exposed Pad Pin 33): Small-signal ground common to both controllers, must be routed separately from high current grounds to the common (–) terminals of the C_{IN} capacitors. The exposed pad must be soldered to the PCB for rated thermal performance.

RUN1, RUN2 (Pin 7, Pin 8): Digital Run Control Inputs for Each Controller. Forcing either of these pins below 1.2V shuts down that controller. Forcing both of these pins below 0.7V shuts down the entire LTC3858-2, reducing quiescent current to approximately 8µA.

I_{LIM} (Pin 28): Current Comparator Sense Voltage Range Inputs. Tying this pin to SGND, FLOAT or $INTV_{CC}$ sets the maximum current sense threshold to one of three different levels for both comparators.

PIN FUNCTIONS

$INTV_{CC}$ (Pin 19): Output of the Internal Linear Low Dropout Regulator. The driver and control circuits are powered from this voltage source. Must be decoupled to power ground with a minimum of 4.7µF ceramic or other low ESR capacitor. Do not use the $INTV_{CC}$ pin for any other purpose.

$EXTV_{CC}$ (Pin 20): External Power Input to an Internal LDO Connected to $INTV_{CC}$. This LDO supplies $INTV_{CC}$ power, bypassing the internal LDO powered from V_{IN} whenever $EXTV_{CC}$ is higher than 4.7V. See $EXTV_{CC}$ Connection in the Applications Information section. Do not exceed 14V on this pin.

PGND (Pin 21): Driver Power Ground. Connects to the sources of bottom (synchronous) N-channel MOSFETs and the (–) terminal(s) of C_{IN}.

V_{IN} (Pin 22): Main Input Supply Pin. A bypass capacitor should be tied between this pin and the signal ground pin.

BG1, BG2 (Pin 23, Pin 18): High Current Gate Drives for Bottom (Synchronous) N-Channel MOSFETs. Voltage swing at these pins is from ground to $INTV_{CC}$.

BOOST1, BOOST2 (Pin 24, Pin 17): Bootstrapped Supplies to the Topside Floating Drivers. Capacitors are connected between the BOOST and SW pins and Schottky diodes are tied between the BOOST and $INTV_{CC}$ pins. Voltage swing at the BOOST pins is from $INTV_{CC}$ to (V_{IN} + $INTV_{CC}$).

SW1, SW2 (Pin 25, Pin 16): Switch Node Connections to Inductors.

TG1, TG2 (Pin 26, Pin 15): High Current Gate Drives for Top N-Channel MOSFETs. These are the outputs of floating drivers with a voltage swing equal to $INTV_{CC}$ – 0.5V superimposed on the switch node voltage SW.

PGOOD1, PGOOD2 (Pin 27, Pin 14): Open-Drain Logic Output. PGOOD1,2 is pulled to ground when the voltage on the $V_{FB1,2}$ pin is not within ±10% of its set point.

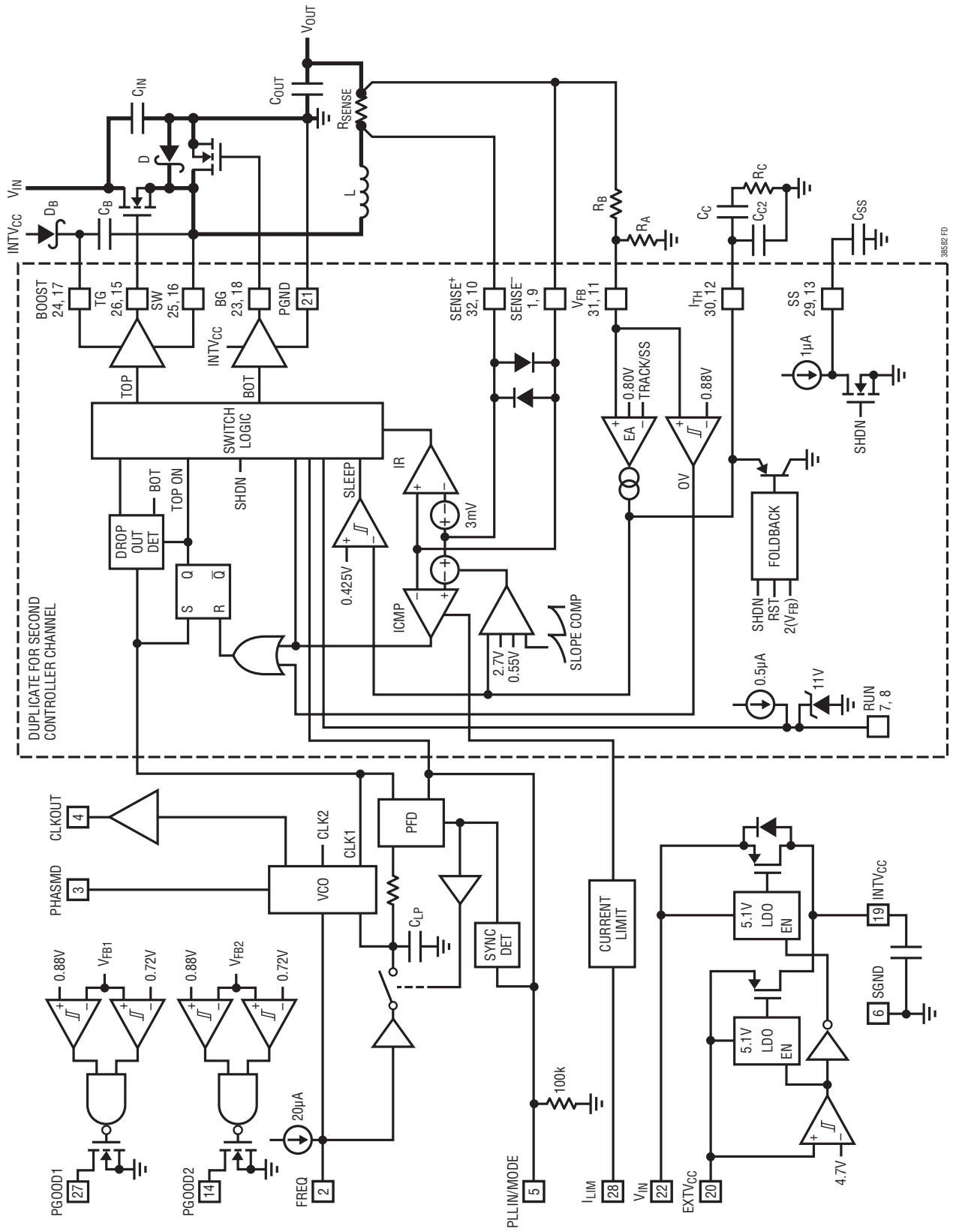
SS1, SS2 (Pin 29, Pin 13): External Soft-Start Input. The LTC3858-2 regulates the $V_{FB1,2}$ voltage to the smaller of 0.8V or the voltage on the SS1,2 pin. An internal 1µA pull-up current source is connected to this pin. A capacitor to ground at this pin sets the ramp time to final regulated output voltage. Alternatively, a resistor divider on another voltage supply connected to this pin allows the LTC3858-2 output to track the other supply during start-up.

I_{TH1}, I_{TH2} (Pin 30, Pin 12): Error Amplifier Outputs and Switching Regulator Compensation Points. Each associated channel's current comparator trip point increases with this control voltage.

V_{FB1}, V_{FB2} (Pin 31, Pin 11): Receives the remotely sensed feedback voltage for each controller from an external resistive divider across the output.

$SENSE1^+$, $SENSE2^+$ (Pin 32, Pin 10): The (+) Input to the differential current comparators that are normally connected to inductor DCR sensing networks or current sensing resistors. The I_{TH} pin voltage and controlled offsets between the $SENSE^-$ and $SENSE^+$ pins in conjunction with R_{SENSE} set the current trip threshold.

FUNCTIONAL DIAGRAM



OPERATION (Refer to the Functional Diagram)

Table 1 summarizes the differences between the LTC3858-2 and its sister parts, the LTC3858 and LTC3858-1. The LTC3858-2 uses a constant frequency, current mode step-down architecture with the two controller channels operating 180 degrees out of phase. During normal operation, each external top MOSFET is turned on when the clock for that channel sets the RS latch, and is turned off when the main current comparator, ICMP, resets the RS latch. The peak inductor current at which ICMP trips and resets the latch is controlled by the voltage on the I_{TH} pin, which is the output of the error amplifier, EA. The error amplifier compares the output voltage feedback signal at the V_{FB} pin (which is generated with an external resistor divider connected across the output voltage, V_{OUT}, to ground) to the internal 0.800V reference voltage. When the load current increases, it causes a slight decrease in V_{FB} relative to the reference, which causes the EA to increase the I_{TH} voltage until the average inductor current matches the new load current.

After the top MOSFET is turned off each cycle, the bottom MOSFET is turned on until either the inductor current starts to reverse, as indicated by the current comparator IR, or the beginning of the next clock cycle.

$INTV_{CC}/EXTV_{CC}$ Power

Power for the top and bottom MOSFET drivers and most other internal circuitry is derived from the $INTV_{CC}$ pin. When the $EXTV_{CC}$ pin is left open or tied to a voltage less than 4.7V, the V_{IN} LDO (low dropout linear regulator) supplies 5.1V from V_{IN} to $INTV_{CC}$. If $EXTV_{CC}$ is taken above 4.7V, the V_{IN} LDO is turned off and the $EXTV_{CC}$ LDO is turned on. Once enabled, the $EXTV_{CC}$ LDO supplies 5.1V from $EXTV_{CC}$ to $INTV_{CC}$. Using the $EXTV_{CC}$ pin allows the $INTV_{CC}$ power to be derived from a high efficiency external source such as one of the LTC3858-2 switching regulator outputs.

Each top MOSFET driver is biased from the floating bootstrap capacitor, C_B, which normally recharges during each switching cycle through an external diode when the top MOSFET turns off. If the input voltage, V_{IN}, decreases to a voltage close to V_{OUT}, the loop may enter dropout and attempt to turn on the top MOSFET continuously. The dropout detector detects this and forces the top MOSFET off for about one-twelfth of the clock period every tenth cycle to allow C_B to recharge.

Table 1. Summary of the Differences Between LTC3858, LTC3858-1 and LTC3858-2

	LTC3858	LTC3858-1	LTC3858-2
Short-Circuit Latchoff Feature?	Yes, But Can Be Defeated	Yes, But Can Be Defeated	Not Present
Overvoltage Protection	BG Forced On (Bottom MOSFET "Crowbar")	BG Forced On (Bottom MOSFET "Crowbar")	BG Not Forced On (Behavior Depends on Light Load Mode)
Optional Tracking Start-Up?	No	No	Yes
Independent PGOOD1 and PGOOD2 Pins?	Yes	No, PGOOD1 Only	Yes
CLKOUT/PHASMD Pins for PolyPhase	Yes	No	Yes
Adjustable Current Limit (I_{LIM} Pin)	Yes	No	Yes
Package	5mm × 5mm QFN	4mm × 5mm QFN and Narrow SSOP	5mm × 5mm QFN

OPERATION (Refer to the Functional Diagram)

Shutdown and Start-Up (RUN1, RUN2 and SS1, SS2 Pins)

The two channels of the LTC3858-2 can be independently shut down using the RUN1 and RUN2 pins. Pulling either of these pins below 1.26V shuts down the main control loop for that controller. Pulling both pins below 0.7V disables both controllers and most internal circuits, including the $INTV_{CC}$ LDOs. In this state, the LTC3858-2 draws only 8µA of quiescent current.

The RUN pin may be externally pulled up or driven directly by logic. When driving the RUN pin with a low impedance source, do not exceed the absolute maximum rating of 8V. The RUN pin has an internal 11V voltage clamp that allows the RUN pin to be connected through a resistor to a higher voltage (for example, V_{IN}), so long as the maximum current into the RUN pin does not exceed 100µA.

The start-up of each controller's output voltage, V_{OUT}, is controlled by the voltage on the SS pin for that channel. When the voltage on the SS pin is less than the 0.8V internal reference, the LTC3858-2 regulates the V_{FB} voltage to the SS pin voltage instead of the 0.8V reference. This allows the SS pin to be used to program a soft-start by connecting an external capacitor from the SS pin to SGND. An internal 1µA pull-up current charges this capacitor creating a voltage ramp on the SS pin. As the SS voltage rises linearly from 0V to 0.8V (and beyond up to the absolute maximum rating of 6V), the output voltage V_{OUT} rises smoothly from zero to its final value.

Alternatively, the SS pin can be used to cause the start-up of V_{OUT} to track that of another supply. Typically, this requires connecting to the SS pin an external resistor divider from the other supply to ground (see the Applications Information section).

Light Load Current Operation (Burst Mode Operation, Pulse-Skipping or Forced Continuous) (PLLIN/MODE Pin)

The LTC3858-2 can be enabled to enter high efficiency Burst Mode operation, constant frequency pulse-skipping mode, or forced continuous conduction mode at low load currents. To select Burst Mode operation, tie the PLLIN/ MODE pin to ground. To select forced continuous operation, tie the PLLIN/MODE pin to $INTV_{CC}$. To select pulse-skipping mode, tie the PLLIN/MODE pin to a DC voltage greater than 1.2V and less than $INTV_{CC}$ – 1.3V.

When a controller is enabled for Burst Mode operation, the minimum peak current in the inductor is set to approximately 30% of the maximum sense voltage even though the voltage on the I_{TH} pin indicates a lower value. If the average inductor current is higher than the load current, the error amplifier EA will decrease the voltage on the I_{TH} pin. When the I_{TH} voltage drops below 0.425V, the internal sleep signal goes high (enabling "sleep" mode) and both external MOSFETs are turned off.

In sleep mode, much of the internal circuitry is turned off, reducing the quiescent current. If one channel is shut down and the other channel is in sleep mode, the LTC3858-2 draws only 170µA of quiescent current. If both channels are in sleep mode, the LTC3858-2 draws only 300µA of quiescent current. In sleep mode, the load current is supplied by the output capacitor. As the output voltage decreases, the EA's output begins to rise. When the output voltage drops enough, the I_{TH} pin is reconnected to the output of the EA, the sleep signal goes low, and the controller resumes normal operation by turning on the top external MOSFET on the next cycle of the internal oscillator.

When a controller is enabled for Burst Mode operation, the inductor current is not allowed to reverse. The reverse current comparator, IR, turns off the bottom external MOSFET just before the inductor current reaches zero, preventing it from reversing and going negative. Thus, the controller is in discontinuous operation.

OPERATION (Refer to the Functional Diagram)

In forced continuous operation or when clocked by an external clock source to use the phase-locked loop (see the Frequency Selection and Phase-Locked Loop section), the inductor current is allowed to reverse at light loads or under large transient conditions. The peak inductor current is determined by the voltage on the I_{TH} pin, just as in normal operation. In this mode, the efficiency at light loads is lower than in Burst Mode operation. However, continuous operation has the advantages of lower output voltage ripple and less interference to audio circuitry. In forced continuous mode, the output ripple is independent of load current.

When the PLLIN/MODE pin is connected for pulse-skipping mode, the LTC3858-2 operates in PWM pulse-skipping mode at light loads. In this mode, constant frequency operation is maintained down to approximately 1% of designed maximum output current. At very light loads, the current comparator, ICMP, may remain tripped for several cycles and force the external top MOSFET to stay off for the same number of cycles (i.e., skipping pulses). The inductor current is not allowed to reverse (discontinuous operation). This mode, like forced continuous operation, exhibits low output ripple as well as low audio noise and reduced RF interference when compared to Burst Mode operation. It provides higher light load efficiency than forced continuous mode, but not nearly as high as Burst Mode operation.

Frequency Selection and Phase-Locked Loop (FREQ and PLLIN/MODE Pins)

The selection of switching frequency is a trade-off between efficiency and component size. Low frequency operation increases efficiency by reducing MOSFET switching losses, but requires larger inductance and/or capacitance to maintain low output ripple voltage.

The switching frequency of the LTC3858-2's controllers can be selected using the FREQ pin.

If the PLLIN/MODE pin is not being driven by an external clock source, the FREQ pin can be tied to SGND, tied to $INTV_{CC}$ or programmed through an external resistor. Tying FREQ to SGND selects 350kHz while tying FREQ to $INTV_{CC}$ selects 535kHz. Placing a resistor between FREQ and SGND allows the frequency to be programmed between 50kHz and 900kHz, as shown in Figure 10.

A phase-locked loop (PLL) is available on the LTC3858-2 to synchronize the internal oscillator to an external clock source that is connected to the PLLIN/MODE pin. The phase detector adjusts the voltage (through an internal lowpass filter) of the VCO input to align the turn-on of controller 1's external top MOSFET to the rising edge of the synchronizing signal. Thus, the turn-on of controller 2's external top MOSFET is 180 degrees out of phase to the rising edge of the external clock source.

The VCO input voltage is pre-biased to the operating frequency set by the FREQ pin before the external clock is applied. If prebiased near the external clock frequency, the PLL loop only needs to make slight changes to the VCO input in order to synchronize the rising edge of the external clock's to the rising edge of TG1. The ability to pre-bias the loop filter allows the PLL to lock-in rapidly without deviating far from the desired frequency.

The typical capture range of the phase-locked loop is from approximately 55kHz to 1MHz, with a guarantee over all manufacturing variations to be between 75kHz and 850kHz. In other words, the LTC3858-2's PLL is guaranteed to lock to an external clock source whose frequency is between 75kHz and 850kHz.

The typical input clock thresholds on the PLLIN/MODE pin are 1.6V (rising) and 1.1V (falling).

OPERATION (Refer to the Functional Diagram)

PolyPhase® Applications (CLKOUT and PHASMD Pins)

The LTC3858-2 features two pins (CLKOUT and PHASMD) that allow other controller ICs to be daisy-chained with the LTC3858-2 in PolyPhase applications. The clock output signal on the CLKOUT pin can be used to synchronize additional power stages in a multiphase power supply solution feeding a single, high current output or multiple separate outputs. The PHASMD pin is used to adjust the phase of the CLKOUT signal as well as the relative phases between the two internal controllers, as summarized in Table 2. The phases are calculated relative to the zero degrees phase being defined as the rising edge of the top gate driver output of controller 1 (TG1). The CLKOUT pin swings from ground to $INTV_{CC}$ with a pull-down impedance of 120Ω and a pull-up impedance of 150Ω.

Table 2

V_{PHASMD}	CONTROLLER 2-PHASE	CLKOUT PHASE
GND	180°	60°
Floating	180°	90°
$INTV_{CC}$	240°	120°

Output Overvoltage Protection

An overvoltage (OV) comparator guards against transient overshoots as well as other more serious conditions that may overvoltage the output. When the V_{FB} pin rises by more than 10% above its regulation point of 0.800V, the top MOSFET is turned off until the overvoltage condition is cleared.

The state of the bottom MOSFET during the overvoltage condition depends on the light load mode of operation, as selected by the PLLIN/MODE pin. In forced continuous mode, the bottom gate driver BG naturally turns on whenever the top gate driver TG is off, resulting in negative inductor current which discharges the output to (try to) bring it back into regulation. In pulse-skipping mode, BG is held off most of the time but is turned on for a brief pulse every ten clock cycles (for an effective BG-on duty cycle of ~1%) to refresh the BOOST-SW capacitor. This causes a slightly negative average inductor current which, in addition to whatever load current is present, may slowly discharge the output. In Burst Mode operation, BG is held off continuously, leaving only the load current to discharge the output to bring it back into regulation.

Power Good (PGOOD1 and PGOOD2) Pins

Each PGOOD pin is connected to an open drain of an internal N-channel MOSFET. The MOSFET turns on and pulls the PGOOD pin low when the corresponding V_{FB} pin voltage is not within ±10% of the 0.8V reference voltage. The PGOOD pin is also pulled low when the corresponding RUN pin is low (shut down). When the V_{FB} pin voltage is within the ±10% requirement, the MOSFET is turned off and the pin is allowed to be pulled up by an external resistor to a source no greater than 6V.

Foldback Current

When the output voltage falls to less than 70% of its nominal level, foldback current limiting is activated, progressively lowering the peak current limit in proportion to the severity of the overcurrent or short-circuit condition. Foldback current limiting is disabled during the soft-start interval (as long as the V_{FB} voltage is keeping up with the TRACK/SS voltage).

Theory and Benefits of 2-Phase Operation

Why the need for 2-phase operation? Up until the 2-phase family, constant frequency dual switching regulators operated both channels in phase (i.e., single phase operation). This means that both switches turned on at the same time, causing current pulses of up to twice the amplitude of those for one regulator to be drawn from the input capacitor and battery. These large amplitude current pulses increased the total RMS current flowing from the input capacitor, requiring the use of more expensive input capacitors and increasing both EMI and losses in the input capacitor and battery.

With 2-phase operation, the two channels of the dual switching regulator are operated 180 degrees out of phase. This effectively interleaves the current pulses drawn by the switches, greatly reducing the overlap time where they add together. The result is a significant reduction in total RMS input current, which in turn allows less expensive input capacitors to be used, reduces shielding requirements for EMI and improves real world operating efficiency.

OPERATION (Refer to the Functional Diagram)

Figure 1 compares the input waveforms for a representative single-phase dual switching regulator to the LTC3858-2 2-phase dual switching regulator. An actual measurement of the RMS input current under these conditions shows that 2-phase operation dropped the input current from $2.53A_{RMS}$ to $1.55A_{RMS}$. While this is an impressive reduction in itself, remember that the power losses are proportional to I_{RMS}^2, meaning that the actual power wasted is reduced by a factor of 2.66. The reduced input ripple voltage also means less power is lost in the input power path, which could include batteries, switches, trace/connector resistances and protection circuitry. Improvements in both conducted and radiated EMI also directly accrue as a result of the reduced RMS input current and voltage.

Of course, the improvement afforded by 2-phase operation is a function of the dual switching regulator's relative duty cycles which, in turn, are dependent upon the input voltage V_{IN} (Duty Cycle = V_{OUT}/V_{IN}). Figure 2 shows how the RMS input current varies for single phase and 2-phase operation for 3.3V and 5V regulators over a wide input voltage range.

It can readily be seen that the advantages of 2-phase operation are not just limited to a narrow operating range, for most applications is that 2-phase operation will reduce the input capacitor requirement to that for just one channel operating at maximum current and 50% duty cycle.

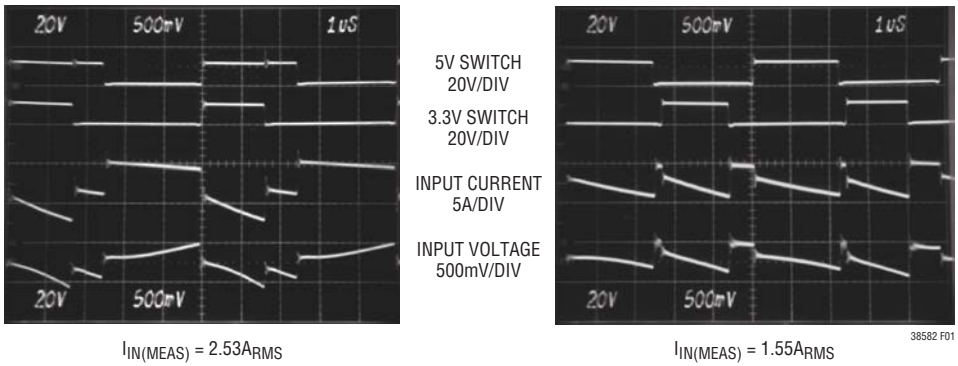


Figure 1. Input Waveforms Comparing Single-Phase (a) and 2-Phase (b) Operation for Dual Switching Regulators Converting 12V to 5V and 3.3V at 3A Each. The Reduced Input Ripple with the 2-Phase Regulator Allows Less Expensive Input Capacitors, Reduces Shielding Requirements for EMI and Improves Efficiency

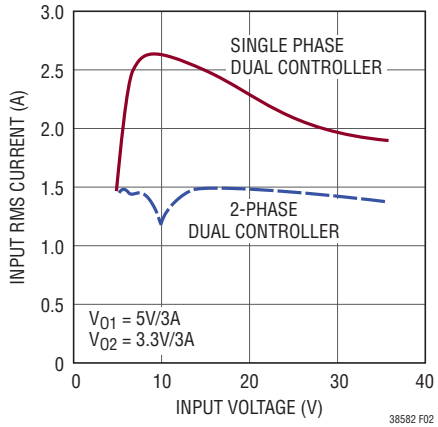


Figure 2. RMS Input Current Comparison

APPLICATIONS INFORMATION

The Typical Application on the first page is a basic LTC3858-2 application circuit. LTC3858-2 can be configured to use either DCR (inductor resistance) sensing or low value resistor sensing. The choice between the two current sensing schemes is largely a design trade-off between cost, power consumption and accuracy. DCR sensing is becoming popular because it saves expensive current sensing resistors and is more power efficient, especially in high current applications. However, current sensing resistors provide the most accurate current limits for the controller. Other external component selection is driven by the load requirement, and begins with the selection of R_{SENSE} (if R_{SENSE} is used) and inductor value. Next, the power MOSFETs and Schottky diodes are selected. Finally, input and output capacitors are selected.

Current Limit Programming

The I_{LIM} pin is a tri-level logic input which sets the maximum current limit of the converter. When I_{LIM} is grounded, the maximum current limit threshold voltage of the current comparator is programmed to be 30mV. When I_{LIM} is floated, the maximum current limit threshold is 50mV. When I_{LIM} is tied to $INTV_{CC}$, the maximum current limit threshold is set to 75mV.

SENSE+ and SENSE– Pins

The $SENSE^+$ and $SENSE^–$ pins are the inputs to the current comparators. The common mode voltage range on these pins is 0V to 28V (Abs Max), enabling the LTC3858-2 to regulate output voltages up to a nominal 24V (allowing plenty of margin for tolerances and transients).

The $SENSE^+$ pin is high impedance over the full common mode range, drawing at most ±1µA. This high impedance allows the current comparators to be used in inductor DCR sensing.

The impedance of the $SENSE^–$ pin changes depending on the common mode voltage. When $SENSE^–$ is less than $INTV_{CC}$ – 0.5V, a small current of less than 1µA flows out of the pin. When $SENSE^–$ is above $INTV_{CC}$ + 0.5V, a higher current (~550µA) flows into the pin. Between $INTV_{CC}$ – 0.5V and $INTV_{CC}$ + 0.5V, the current transitions from the smaller current to the higher current.

Filter components mutual to the sense lines should be placed close to the LTC3858-2, and the sense lines should run close together to a Kelvin connection underneath the current sense element (shown in Figure 3). Sensing current elsewhere can effectively add parasitic inductance and capacitance to the current sense element, degrading the information at the sense terminals and making the programmed current limit unpredictable. If inductor DCR sensing is used (Figure 4b), resistor R1 should be placed close to the switching node, to prevent noise from coupling into sensitive small-signal nodes.

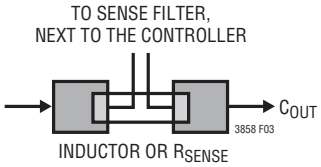


Figure 3. Sense Lines Placement with Inductor or Sense Resistor

Low Value Resistor Current Sensing

A typical sensing circuit using a discrete resistor is shown in Figure 4a. R_{SENSE} is chosen based on the required output current.

The current comparator has a maximum threshold $V_{SENSE(MAX)}$ determined by the I_{LIM} setting. The current comparator threshold voltage sets the peak of the inductor current, yielding a maximum average output current, I_{MAX}, equal to the peak value less half the peak-to-peak ripple current, ΔI_L. To calculate the sense resistor value, use the equation:

$$R_{SENSE} = \frac{V_{SENSE(MAX)}}{I_{MAX} + \frac{\Delta I_L}{2}}$$

When using the controller in very low dropout conditions, the maximum output current level will be reduced due to the internal compensation required to meet stability criterion for buck regulators operating at greater than 50% duty factor. A curve is provided in the Typical Performance Characteristics section to estimate this reduction in peak output current depending upon the operating duty factor.

APPLICATIONS INFORMATION

Inductor DCR Sensing

For applications requiring the highest possible efficiency at high load currents, the LTC3850 is capable of sensing the voltage drop across the inductor DCR, as shown in Figure 4b. The DCR of the inductor represents the small amount of DC resistance of the copper wire, which can be less than 1mΩ for today's low value, high current inductors. In a high current application requiring such an inductor, power loss through a sense resistor would cost several points of efficiency compared to inductor DCR sensing.

If the external R1||R2 • C1 time constant is chosen to be exactly equal to the L/DCR time constant, the voltage drop across the external capacitor is equal to the drop across the inductor DCR multiplied by R2/(R1 + R2). R2 scales the voltage across the sense terminals for applications where the DCR is greater than the target sense resistor value. To properly dimension the external filter components, the DCR of the inductor must be known. It can be measured using a good RLC meter, but the DCR tolerance is not always the same and varies with temperature; consult the manufacturers' data sheets for detailed information.

Using the inductor ripple current value from the Inductor Value Calculation section, the target sense resistor value is:

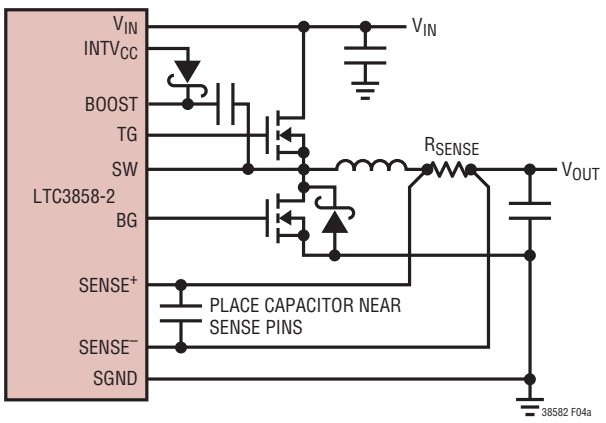
$$R_{SENSE(EQUIV)} = \frac{V_{SENSE(MAX)}}{I_{MAX} + \frac{\Delta I_L}{2}}$$

To ensure that the application will deliver full load current over the full operating temperature range, choose the minimum value for the Maximum Current Sense Threshold Voltage ($V_{SENSE(MAX)}$) in the Electrical Characteristics table (30mV, 50mV or 75mV depending on the state of the I_{LIM} pin).

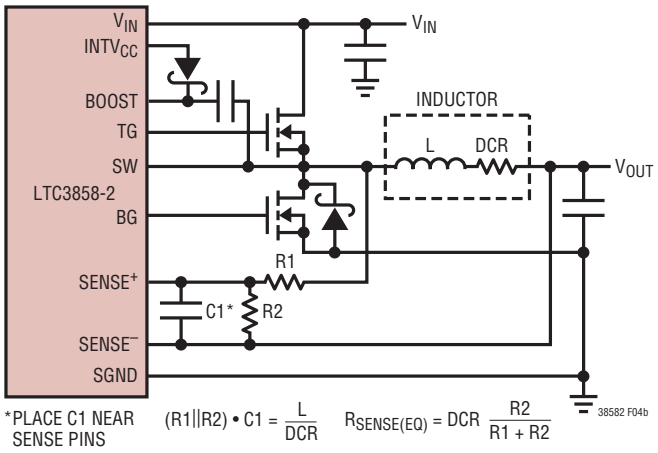
Next, determine the DCR of the inductor. When provided, use the manufacturer's maximum value, usually given at 20°C. Increase this value to account for the temperature coefficient of copper, which is approximately 0.4%/°C. A conservative value for $T_{L(MAX)}$ is 100°C.

To scale the maximum inductor DCR to the desired sense resistor (R_D) value, use the divider ratio:

$$R_D = \frac{R_{SENSE(EQUIV)}}{DCR_{MAX\ at\ T_{L(MAX)}}}$$



(4a) Using a Resistor to Sense Current



(4b) Using the Inductor DCR to Sense Current

Figure 4. Current Sensing Methods

APPLICATIONS INFORMATION

C1 is usually selected to be in the range of 0.1µF to 0.47µF. This forces R1||R2 to around 2k, reducing error that might have been caused by the SENSE+ pin's ±1µA current.

The equivalent resistance R1||R2 is scaled to the room temperature inductance and maximum DCR:

$$R1||R2 = \frac{L}{(DCR\ at\ 20°C) \bullet C1}$$

The sense resistor values are:

$$R1 = \frac{R1||R2}{R_D};\ R2 = \frac{R1 \bullet R_D}{1 - R_D}$$

The maximum power loss in R1 is related to duty cycle, and will occur in continuous mode at the maximum input voltage:

$$P_{LOSS}\ R1 = \frac{(V_{IN(MAX)} - V_{OUT}) \bullet V_{OUT}}{R1}$$

Ensure that R1 has a power rating higher than this value. If high efficiency is necessary at light loads, consider this power loss when deciding whether to use inductor DCR sensing or sense resistors. Light load power loss can be modestly higher with a DCR network than with a sense resistor, due to the extra switching losses incurred through R1. However, DCR sensing eliminates a sense resistor, reduces conduction losses and provides higher efficiency at heavy loads. Peak efficiency is about the same with either method.

Inductor Value Calculation

The operating frequency and inductor selection are interrelated in that higher operating frequencies allow the use of smaller inductor and capacitor values. So why would anyone ever choose to operate at lower frequencies with larger components? The answer is efficiency. A higher frequency generally results in lower efficiency because of MOSFET gate charge losses. In addition to this basic trade-off, the effect of inductor value on ripple current and low current operation must also be considered.

The inductor value has a direct effect on ripple current. The inductor ripple current ΔI_L decreases with higher inductance or higher frequency and increases with higher V_{IN}:

$$\Delta I_L = \frac{1}{(f)(L)} V_{OUT} \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Accepting larger values of ΔI_L allows the use of low inductances, but results in higher output voltage ripple and greater core losses. A reasonable starting point for setting ripple current is $\Delta I_L = 0.3(I_{MAX})$. The maximum ΔI_L occurs at the maximum input voltage.

The inductor value also has secondary effects. The transition to Burst Mode operation begins when the average inductor current required results in a peak current below 30% of the current limit determined by R_{SENSE}. Lower inductor values (higher ΔI_L) will cause this to occur at lower load currents, which can cause a dip in efficiency in the upper range of low current operation. In Burst Mode operation, lower inductance values will cause the burst frequency to decrease.

Inductor Core Selection

Once the value for L is known, the type of inductor must be selected. High efficiency converters generally cannot afford the core loss found in low cost powdered iron cores, forcing the use of more expensive ferrite or molypermalloy cores. Actual core loss is independent of core size for a fixed inductor value, but it is very dependent on inductance value selected. As inductance increases, core losses go down. Unfortunately, increased inductance requires more turns of wire and therefore copper losses will increase.

Ferrite designs have very low core loss and are preferred for high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates "hard," which means that inductance collapses abruptly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current and consequent output voltage ripple. Do not allow the core to saturate!

APPLICATIONS INFORMATION

Power MOSFET and Schottky Diode (Optional) Selection

Two external power MOSFETs must be selected for each controller in the LTC3858-2: one N-channel MOSFET for the top (main) switch, and one N-channel MOSFET for the bottom (synchronous) switch.

The peak-to-peak drive levels are set by the $INTV_{CC}$ voltage. This voltage is typically 5.2V during start-up (see $EXTV_{CC}$ Pin Connection). Consequently, logic-level threshold MOSFETs must be used in most applications. The only exception is if low input voltage is expected (V_{IN} < 4V); then, sub-logic level threshold MOSFETs ($V_{GS(TH)}$ < 3V) should be used. Pay close attention to the BV_{DSS} specification for the MOSFETs as well; many of the logic-level MOSFETs are limited to 30V or less.

Selection criteria for the power MOSFETs include the on-resistance, $R_{DS(ON)}$, Miller capacitance, C_{MILLER}, input voltage and maximum output current. Miller capacitance, C_{MILLER}, can be approximated from the gate charge curve usually provided on the MOSFET manufacturers' data sheet. C_{MILLER} is equal to the increase in gate charge along the horizontal axis while the curve is approximately flat divided by the specified change in V_{DS}. This result is then multiplied by the ratio of the application applied V_{DS} to the gate charge curve specified V_{DS}. When the IC is operating in continuous mode the duty cycles for the top and bottom MOSFETs are given by:

$$\text{Main Switch Duty Cycle} = \frac{V_{OUT}}{V_{IN}}$$

$$\text{Synchronous Switch Duty Cycle} = \frac{V_{IN} - V_{OUT}}{V_{IN}}$$

The MOSFET power dissipations at maximum output current are given by:

$$P_{MAIN} = \frac{V_{OUT}}{V_{IN}}(I_{MAX})^2(1+\delta)R_{DS(ON)} + (V_{IN})^2\left(\frac{I_{MAX}}{2}\right)(R_{DR})(C_{MILLER})\bullet\left[\frac{1}{V_{INTVCC} - V_{THMIN}} + \frac{1}{V_{THMIN}}\right](f)$$

$$P_{SYNC} = \frac{V_{IN} - V_{OUT}}{V_{IN}}(I_{MAX})^2(1+\delta)R_{DS(ON)}$$

where δ is the temperature dependency of $R_{DS(ON)}$ and R_{DR} (approximately 2Ω) is the effective driver resistance at the MOSFET's Miller threshold voltage. V_{THMIN} is the typical MOSFET minimum threshold voltage.

Both MOSFETs have I^2R losses while the topside N-channel equation includes an additional term for transition losses, which are highest at high input voltages. For V_{IN} < 20V the high current efficiency generally improves with larger MOSFETs, while for V_{IN} > 20V the transition losses rapidly increase to the point that the use of a higher $R_{DS(ON)}$ device with lower C_{MILLER} actually provides higher efficiency. The synchronous MOSFET losses are greatest at high input voltage when the top switch duty factor is low or during a short-circuit when the synchronous switch is on close to 100% of the period.

The term (1+ δ) is generally given for a MOSFET in the form of a normalized $R_{DS(ON)}$ vs Temperature curve, but δ = 0.005/°C can be used as an approximation for low voltage MOSFETs.

The optional Schottky diodes D3 and D4 shown in Figure 13 conduct during the dead-time between the conduction of the two power MOSFETs. This prevents the body diode of the bottom MOSFET from turning on, storing charge during the dead-time and requiring a reverse recovery period that could cost as much as 3% in efficiency at high V_{IN}. A 1A to 3A Schottky is generally a good compromise for both regions of operation due to the relatively small average current. Larger diodes result in additional transition losses due to their larger junction capacitance.

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C_{IN} and C_{OUT} Selection

The selection of C_{IN} is simplified by the 2-phase architecture and its impact on the worst-case RMS current drawn through the input network (battery/fuse/capacitor). It can be shown that the worst-case capacitor RMS current occurs when only one controller is operating. The controller with the highest $(V_{OUT})(I_{OUT})$ product needs to be used in the formula shown in Equation 1 to determine the maximum RMS capacitor current requirement. Increasing the output current drawn from the other controller will actually decrease the input RMS ripple current from its maximum value. The out-of-phase technique typically reduces the input capacitor's RMS ripple current by a factor of 30% to 70% when compared to a single phase power supply solution.

In continuous mode, the source current of the top MOSFET is a square wave of duty cycle $(V_{OUT})/(V_{IN})$. To prevent large voltage transients, a low ESR capacitor sized for the maximum RMS current of one channel must be used. The maximum RMS capacitor current is given by:

$$C_{IN}\ \text{Required}\ I_{RMS} \approx \frac{I_{MAX}}{V_{IN}}\left[(V_{OUT})(V_{IN} - V_{OUT})\right]^{1/2} \quad (1)$$

Equation 1 has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that capacitor manufacturers' ripple current ratings are often based on only 2000 hours of life. This makes it advisable to further derate the capacitor, or to choose a capacitor rated at a higher temperature than required. Several capacitors may be paralleled to meet size or height requirements in the design. Due to the high operating frequency of the LTC3858-2, ceramic capacitors can also be used for C_{IN}. Always consult the manufacturer if there is any question.

The benefit of 2-phase operation can be calculated by using Equation 1 for the higher power controller and then calculating the loss that would have resulted if both controller channels switched on at the same time. The total RMS power lost is lower when both controllers are operating due to the reduced overlap of current pulses required through the input capacitor's ESR. This is why the input capacitor's requirement calculated above for the worst-case controller is adequate for the dual controller design. Also, the input protection fuse resistance, battery resistance, and PC board trace resistance losses are also reduced due to the reduced peak currents in a 2-phase system. The overall benefit of a multiphase design will only be fully realized when the source impedance of the power supply/battery is included in the efficiency testing. The drains of the top MOSFETs should be placed within 1cm of each other and share a common C_{IN} (s). Separating the sources and C_{IN} may produce undesirable voltage and current resonances at V_{IN}.

A small (0.1µF to 1µF) bypass capacitor between the chip V_{IN} pin and ground, placed close to the LTC3858-2, is also suggested. A small (1Ω to 10Ω) resistor placed between C_{IN} (C1) and the V_{IN} pin provides further isolation between the two channels.

The selection of C_{OUT} is driven by the effective series resistance (ESR). Typically, once the ESR requirement is satisfied, the capacitance is adequate for filtering. The output ripple (ΔV_{OUT}) is approximated by:

$$\Delta V_{OUT} \approx \Delta I_L \left(ESR + \frac{1}{8 \bullet f \bullet C_{OUT}}\right)$$

where f_O is the operating frequency, C_{OUT} is the output capacitance and ΔI_L is the ripple current in the inductor. The output ripple is highest at maximum input voltage since ΔI_L increases with input voltage.

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Setting Output Voltage

The LTC3858-2 output voltages are each set by an external feedback resistor divider carefully placed across the output, as shown in Figure 5. The regulated output voltage is determined by:

$$V_{OUT} = 0.8V\left(1+\frac{R_B}{R_A}\right)$$

To improve the frequency response, a feedforward capacitor, C_{FF}, may be used. Great care should be taken to route the V_{FB} line away from noise sources, such as the inductor or the SW line.

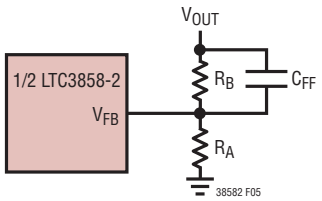


Figure 5. Setting Output Voltage

Soft-Start (SS Pins)

The start-up of each V_{OUT} is controlled by the voltage on the respective SS pin. When the voltage on the SS pin is less than the internal 0.8V reference, the LTC3858-2 regulates the V_{FB} pin voltage to the voltage on the SS pin instead of 0.8V. The SS pin can be used to program an external soft-start function or to allow V_{OUT} to track another supply during start-up.

Soft-start is enabled by simply connecting a capacitor from the SS pin to ground, as shown in Figure 6. An internal 1µA current source charges the capacitor, providing a linear ramping voltage at the SS pin. The LTC3858-2 will regulate the V_{FB} pin (and hence V_{OUT}) according to the voltage on the SS pin, allowing V_{OUT} to rise smoothly from 0V to its final regulated value. The total soft-start time will be approximately:

$$t_{SS} = C_{SS} \bullet \frac{0.8V}{1\mu A}$$

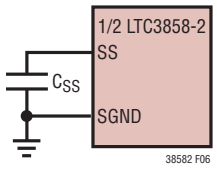


Figure 6. Using the SS Pin to Program Soft-Start

APPLICATIONS INFORMATION

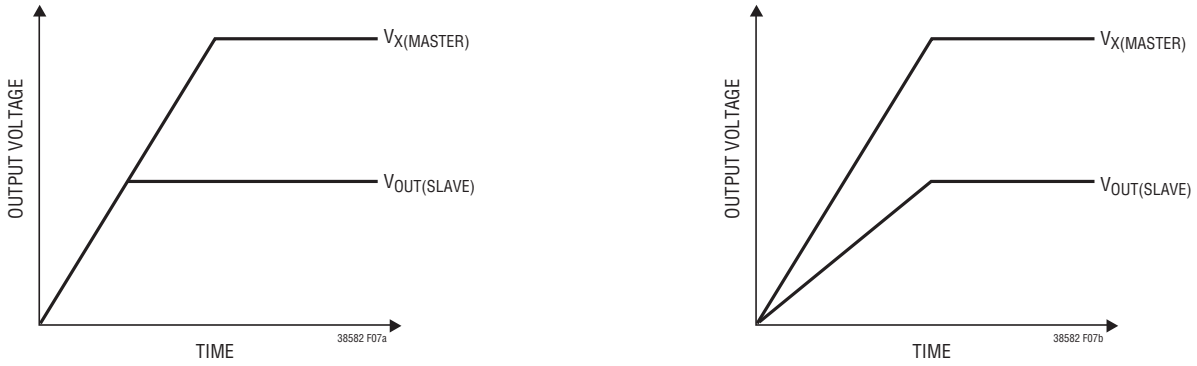
Alternatively, the SS pin can be used to track two (or more) supplies during start-up, as shown qualitatively in Figures 7a and 7b. To do this, a resistor divider should be connected from the master supply (V_X) to the SS pin of the slave supply (V_{OUT}), as shown in Figure 8. During start-up, V_{OUT} will track V_X according to the ratio set by the resistor divider:

$$\frac{V_X}{V_{OUT}} = \frac{R_A}{R_{TRACKA}} \bullet \frac{R_{TRACKA} + R_{TRACKB}}{R_A + R_B}$$

For coincident tracking ($V_{OUT} = V_X$ during start-up):

$R_A = R_{TRACKA}$

$R_B = R_{TRACKB}$



(7a) Coincident Tracking

(7b) Ratiometric Tracking

Figure 7. Two Different Modes of Output Voltage Tracking

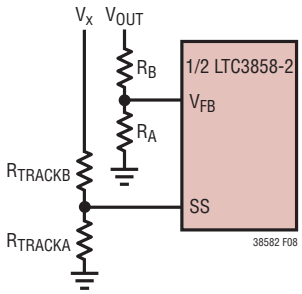


Figure 8. Using the SS Pin for Tracking

APPLICATIONS INFORMATION

$INTV_{CC}$ Regulators

The LTC3858-2 features two separate internal P-channel low dropout linear regulators (LDO) that supply power at the $INTV_{CC}$ pin from either the V_{IN} supply pin or the $EXTV_{CC}$ pin depending on the connection of the $EXTV_{CC}$ pin. $INTV_{CC}$ powers the gate drivers and much of the internal circuitry. The V_{IN} LDO and the $EXTV_{CC}$ LDO regulate $INTV_{CC}$ to 5.1V. Each of these can supply a peak current of 50mA and must be bypassed to ground with a minimum of 4.7µF low ESR capacitor. Regardless of what type of bulk capacitor is used, an additional 1µF ceramic capacitor placed directly adjacent to the $INTV_{CC}$ and PGND pins is highly recommended. Good bypassing is needed to supply the high transient currents required by the MOSFET gate drivers and to prevent interaction between the channels.

High input voltage applications in which large MOSFETs are being driven at high frequencies may cause the maximum junction temperature rating for the LTC3858-2 to be exceeded. The $INTV_{CC}$ current, which is dominated by the gate charge current, may be supplied by either the V_{IN} LDO or the $EXTV_{CC}$ LDO. When the voltage on the $EXTV_{CC}$ pin is less than 4.7V, the V_{IN} LDO is enabled. Power dissipation for the IC in this case is highest and is equal to $V_{IN} \bullet I_{INTVCC}$. The gate charge current is dependent on operating frequency as discussed in the Efficiency Considerations section. The junction temperature can be estimated by using the equations given in Note 3 of the Electrical Characteristics. For example, the LTC3858-2 $INTV_{CC}$ current is limited to less than 32mA from a 40V supply when not using the $EXTV_{CC}$ supply at 70°C ambient temperature:

$$T_J = 70°C + (32mA)(40V)(43°C/W) = 125°C$$

To prevent the maximum junction temperature from being exceeded, the input supply current must be checked while operating in forced continuous mode (PLLIN/MODE = $INTV_{CC}$) at maximum V_{IN}.

When the voltage applied to $EXTV_{CC}$ rises above 4.7V, the V_{IN} LDO is turned off and the $EXTV_{CC}$ LDO is enabled. The $EXTV_{CC}$ LDO remains on as long as the voltage applied to $EXTV_{CC}$ remains above 4.5V. The $EXTV_{CC}$ LDO attempts to regulate the $INTV_{CC}$ voltage to 5.1V, so while $EXTV_{CC}$ is less than 5.1V, the LDO is in dropout and the $INTV_{CC}$ voltage is approximately equal to $EXTV_{CC}$. When $EXTV_{CC}$ is greater than 5.1V, up to an absolute maximum of 14V, $INTV_{CC}$ is regulated to 5.1V.

Using the $EXTV_{CC}$ LDO allows the MOSFET driver and control power to be derived from one of the switching regulator outputs ($4.7V \le V_{OUT} \le 14V$) during normal operation and from the V_{IN} LDO when the output is out of regulation (e.g., start-up, short-circuit). If more current is required through the $EXTV_{CC}$ LDO than is specified, an external Schottky diode can be added between the $EXTV_{CC}$ and $INTV_{CC}$ pins. In this case, do not apply more than 6V to the $EXTV_{CC}$ pin and make sure that $EXTV_{CC} \le V_{IN}$.

Significant efficiency and thermal gains can be realized by powering $INTV_{CC}$ from the output, since the V_{IN} current resulting from the driver and control currents will be scaled by a factor of (Duty Cycle)/(Switcher Efficiency). For 5V to 14V regulator outputs, this means connecting the $EXTV_{CC}$ pin directly to V_{OUT}. Tying the $EXTV_{CC}$ pin to an 8.5V supply reduces the junction temperature in the previous example from 125°C to:

$$T_J = 70°C + (32mA)(8.5V)(43°C/W) = 82°C$$

However, for 3.3V and other low voltage outputs, additional circuitry is required to derive $INTV_{CC}$ power from the output.

The following list summarizes the four possible connections for $EXTV_{CC}$:

1. $EXTV_{CC}$ Grounded. This will cause $INTV_{CC}$ to be powered from the internal 5.1V regulator resulting in an efficiency penalty of up to 10% at high input voltages.
2. $EXTV_{CC}$ Connected Directly to V_{OUT}. This is the normal connection for a 5V to 14V regulator and provides the highest efficiency.
3. $EXTV_{CC}$ Connected to an External Supply. If an external supply is available in the 5V to 14V range, it may be used to power $EXTV_{CC}$. Ensure that $EXTV_{CC} < V_{IN}$.
4. $EXTV_{CC}$ Connected to an Output-Derived Boost Network. For 3.3V and other low voltage regulators, efficiency gains can still be realized by connecting $EXTV_{CC}$ to an output-derived voltage that has been boosted to greater than 4.7V. This can be done with the capacitive charge pump shown in Figure 9. Ensure that $EXTV_{CC} < V_{IN}$.

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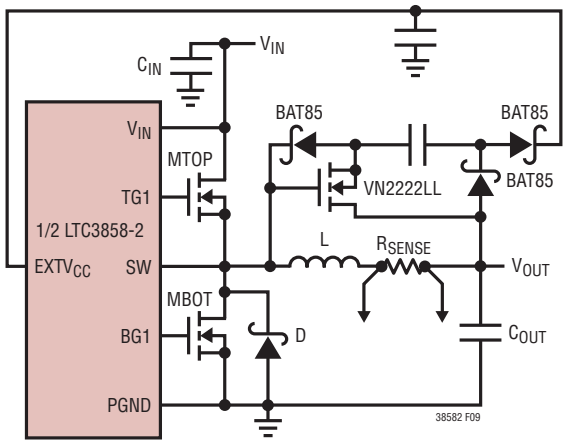


Figure 9. Capacitive Charge Pump for $EXTV_{CC}$

Topside MOSFET Driver Supply (C_B, D_B)

External bootstrap capacitors, C_B, connected to the BOOST pins supply the gate drive voltages for the topside MOSFETs. Capacitor C_B in the Functional Diagram is charged though external diode D_B from $INTV_{CC}$ when the SW pin is low. When one of the topside MOSFETs is turned on, the driver places the C_B voltage across the gate-source of the desired MOSFET. This enhances the top MOSFET switch and turns it on. The switch node voltage, SW, rises to V_{IN} and the BOOST pin follows. With the topside MOSFET on, the boost voltage is above the input supply: $V_{BOOST} = V_{IN} + V_{INTVCC}$. The value of the boost capacitor, C_B, needs to be 100 times that of the total input capacitance of the topside MOSFET(s). The reverse breakdown of the external Schottky diode must be greater than $V_{IN(MAX)}$.

When adjusting the gate drive level, the final arbiter is the total input current for the regulator. If a change is made and the input current decreases, then the efficiency has improved. If there is no change in input current, then there is no change in efficiency.

Fault Conditions: Current Limit and Current Foldback

When the output current hits the current limit, the output voltage begins to drop. If the output voltage falls below 70% of its nominal output level, then the maximum sense voltage is progressively lowered to about half of its maximum selected value. Under short-circuit conditions with very low duty cycles, the LTC3858-2 will begin cycle skipping in order to limit the short-circuit current. In this situation the bottom MOSFET will be dissipating most of the power but less than in normal operation. The short-circuit ripple current is determined by the minimum on-time, $t_{ON(MIN)}$, of the LTC3858-2 (≈95ns), the input voltage and inductor value:

$$\Delta I_{L(SC)} = t_{ON(MIN)} \left(\frac{V_{IN}}{L} \right)$$

The resulting average short-circuit current is:

$$I_{SC} = \frac{50\% \bullet I_{LIM(MAX)}}{R_{SENSE}} - \frac{1}{2} \Delta I_{L(SC)}$$

Phase-Locked Loop and Frequency Synchronization

The LTC3858-2 has an internal phase-locked loop (PLL) comprised of a phase frequency detector, a lowpass filter, and a voltage-controlled oscillator (VCO). This allows the turn-on of the top MOSFET of controller 1 to be locked to the rising edge of an external clock signal applied to the PLLIN/MODE pin. The turn-on of controller 2's top MOSFET is thus 180 degrees out of phase with the external clock. The phase detector is an edge sensitive digital type that provides zero degrees phase shift between the external and internal oscillators. This type of phase detector does not exhibit false lock to harmonics of the external clock.

When not prebiased, applying an external clock will invoke traditional PLL operation. If the external clock frequency is greater than the internal oscillator's frequency, f_{OSC}, then current is sourced continuously from the phase detector output, pulling up the VCO input. When the external clock frequency is less than f_{OSC}, current is sunk continuously, pulling down the VCO input. If the external and internal frequencies are the same but exhibit a phase difference, the current sources turn on for an amount of time corresponding to the phase difference. The voltage at the VCO input is adjusted until the phase and frequency of the internal and external oscillators are identical. At the stable operating point, the phase detector output is high impedance and the internal filter capacitor, C_{LP}, holds the voltage at the VCO input.

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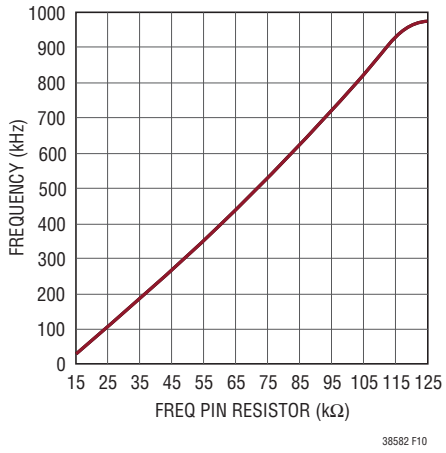


Figure 10. Relationship Between Oscillator Frequency and Resistor Value at the FREQ Pin

Note that the LTC3858-2 can only be synchronized to an external clock whose frequency is within range of the LTC3858-2's internal VCO, which is nominally 55kHz to 1MHz. This is guaranteed to be between 75kHz and 850kHz.

Typically, the external clock (on the PLLIN/MODE pin) input high threshold is 1.6V, while the input low threshold is 1.1V.

Rapid phase-locking can be achieved by using the FREQ pin to set a free-running frequency near the desired synchronization frequency. The VCO's input voltage is prebiased at a frequency corresponding to the frequency set by the FREQ pin. Once prebiased, the PLL only needs to adjust the frequency slightly to achieve phase-locking and synchronization. Although it is not required that the free-running frequency be near external clock frequency, doing so will prevent the operating frequency from passing through a large range of frequencies as the PLL locks.

Table 3 summarizes the different states in which the FREQ pin can be used.

Table 3

FREQ PIN	PLLIN/MODE PIN	FREQUENCY
0V	DC Voltage	350kHz
$INTV_{CC}$	DC Voltage	535kHz
Resistor	DC Voltage	50kHz to 900kHz
Any of the Above	External Clock	Phase-Locked to External Clock

Minimum On-Time Considerations

Minimum on-time, $t_{ON(MIN)}$, is the smallest time duration that the LTC3858-2 is capable of turning on the top MOSFET. It is determined by internal timing delays and the gate charge required to turn on the top MOSFET. Low duty cycle applications may approach this minimum on-time limit and care should be taken to ensure that:

$$t_{ON(MIN)} < \frac{V_{OUT}}{V_{IN}(f)}$$

If the duty cycle falls below what can be accommodated by the minimum on-time, the controller will begin to skip cycles. The output voltage will continue to be regulated, but the ripple voltage and current will increase.

The minimum on-time for the LTC3858-2 is approximately 95ns. However, as the peak sense voltage decreases the minimum on-time gradually increases up to about 130ns. This is of particular concern in forced continuous applications with low ripple current at light loads. If the duty cycle drops below the minimum on-time limit in this situation, a significant amount of cycle skipping can occur with correspondingly larger current and voltage ripple.

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Efficiency Considerations

The percent efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Percent efficiency can be expressed as:

%Efficiency = 100% – (L1 + L2 + L3 + ...)

where L1, L2, etc. are the individual losses as a percentage of input power.

Although all dissipative elements in the circuit produce losses, four main sources usually account for most of the losses in LTC3858-2 circuits: 1) IC V_{IN} current, 2) INTV$_{CC}$ regulator current, 3) I^2R losses, 4) topside MOSFET transition losses.

1. The V_{IN} current is the DC input supply current given in the Electrical Characteristics table, which excludes MOSFET driver and control currents. V_{IN} current typically results in a small (<0.1%) loss.

2. INTV$_{CC}$ current is the sum of the MOSFET driver and control currents. The MOSFET driver current results from switching the gate capacitance of the power MOSFETs. Each time a MOSFET gate is switched from low to high to low again, a packet of charge, dQ, moves from INTV$_{CC}$ to ground. The resulting dQ/dt is a current out of INTV$_{CC}$ that is typically much larger than the control circuit current. In continuous mode, $I_{GATECHG} = f(Q_T + Q_B)$, where Q_T and Q_B are the gate charges of the topside and bottom side MOSFETs.

   Supplying INTV$_{CC}$ from an output-derived power source through EXTV$_{CC}$ will scale the V_{IN} current required for the driver and control circuits by a factor of (Duty Cycle)/(Efficiency). For example, in a 20V to 5V application, 10mA of INTV$_{CC}$ current results in approximately 2.5mA of V_{IN} current. This reduces the midcurrent loss from 10% or more (if the driver was powered directly from V_{IN}) to only a few percent.

3. I^2R losses are predicted from the DC resistances of the fuse (if used), MOSFET, inductor, current sense resistor, and input and output capacitor ESR. In continuous mode the average output current flows through L and R_{SENSE}, but is "chopped" between the topside MOSFET and the synchronous MOSFET. If the two MOSFETs have approximately the same $R_{DS(ON)}$, then the resistance of one MOSFET can simply be summed with the resistances of L, R_{SENSE} and ESR to obtain I^2R losses. For example, if each $R_{DS(ON)} = 30m\Omega$, $R_L = 50m\Omega$, $R_{SENSE} = 10m\Omega$ and $R_{ESR} = 40m\Omega$ (sum of both input and output capacitance losses), then the total resistance is $130m\Omega$. This results in losses ranging from 3% to 13% as the output current increases from 1A to 5A for a 5V output, or a 4% to 20% loss for a 3.3V output. Efficiency varies as the inverse square of V_{OUT} for the same external components and output power level. The combined effects of increasingly lower output voltages and higher currents required by high performance digital systems is not doubling but quadrupling the importance of loss terms in the switching regulator system!

4. Transition losses apply only to the topside MOSFET(s), and become significant only when operating at high input voltages (typically 15V or greater). Transition losses can be estimated from:

   $$\text{Transition Loss} = (1.7) \bullet V_{IN} \bullet 2 \bullet I_{O(MAX)} \bullet C_{RSS} \bullet f$$

   Other "hidden" losses such as copper trace and internal battery resistances can account for an additional 5% to 10% efficiency degradation in portable systems. It is very important to include these "system" level losses during the design phase. The internal battery and fuse resistance losses can be minimized by making sure that C_{IN} has adequate charge storage and very low ESR at the switching frequency. A 25W supply will typically require a minimum of 20µF to 40µF of capacitance having a maximum of $20m\Omega$ to $50m\Omega$ of ESR. The LTC3858-2 2-phase architecture typically halves this input capacitance requirement over competing solutions. Other losses including Schottky conduction losses during dead-time and inductor core losses generally account for less than 2% total additional loss.

APPLICATIONS INFORMATION

Checking Transient Response

The regulator loop response can be checked by looking at the load current transient response. Switching regulators take several cycles to respond to a step in DC (resistive) load current. When a load step occurs, V_{OUT} shifts by an amount equal to ΔI_{LOAD} (ESR), where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT} generating the feedback error signal that forces the regulator to adapt to the current change and return V_{OUT} to its steady-state value. During this recovery time V_{OUT} can be monitored for excessive overshoot or ringing, which would indicate a stability problem. OPTI-LOOP compensation allows the transient response to be optimized over a wide range of output capacitance and ESR values. *The availability of the I_{TH} pin not only allows optimization of control loop behavior, but it also provides a DC coupled and AC filtered closed-loop response test point. The DC step, rise time and settling at this test point truly reflects the closed-loop response.* Assuming a predominantly second order system, phase margin and/or damping factor can be estimated using the percentage of overshoot seen at this pin. The bandwidth can also be estimated by examining the rise time at the pin. The I_{TH} external components shown in Figure 13 circuit will provide an adequate starting point for most applications.

The I_{TH} series R_C-C_C filter sets the dominant pole-zero loop compensation. The values can be modified slightly (from 0.5 to 2 times their suggested values) to optimize transient response once the final PC layout is done and the particular output capacitor type and value have been determined. The output capacitors need to be selected because the various types and values determine the loop gain and phase. An output current pulse of 20% to 80% of full-load current having a rise time of 1µs to 10µs will produce output voltage and I_{TH} pin waveforms that will give a sense of the overall loop stability without breaking the feedback loop.

Placing a resistive load and a power MOSFET directly across the output capacitor and driving the gate with an appropriate signal generator is a practical way to produce a realistic load step condition. The initial output voltage step resulting from the step change in output current may not be within the bandwidth of the feedback loop, so this signal cannot be used to determine phase margin. This is why it is better to look at the I_{TH} pin signal which is in the feedback loop and is the filtered and compensated control loop response.

The gain of the loop will be increased by increasing R_C and the bandwidth of the loop will be increased by decreasing C_C. If R_C is increased by the same factor that C_C is decreased, the zero frequency will be kept the same, thereby keeping the phase shift the same in the most critical frequency range of the feedback loop. The output voltage settling behavior is related to the stability of the closed-loop system and will demonstrate the actual overall supply performance.

A second, more severe transient is caused by switching in loads with large (>1µF) supply bypass capacitors. The discharged bypass capacitors are effectively put in parallel with C_{OUT}, causing a rapid drop in V_{OUT}. No regulator can alter its delivery of current quickly enough to prevent this sudden step change in output voltage if the load switch resistance is low and it is driven quickly. If the ratio of C_{LOAD} to C_{OUT} is greater than 1:50, the switch rise time should be controlled so that the load rise time is limited to approximately $25 \bullet C_{LOAD}$. Thus a 10µF capacitor would require a 250µs rise time, limiting the charging current to about 200mA.

APPLICATIONS INFORMATION

Design Example

As a design example for one channel, assume V_{IN} = 12V(nominal), V_{IN} = 22V (max), V_{OUT} = 3.3V, I_{MAX} = 5A, $V_{SENSE(MAX)}$ = 75mV and f = 350kHz.

The inductance value is chosen first based on a 30% ripple current assumption. The highest value of ripple current occurs at the maximum input voltage. Tie the FREQ pin to GND, generating 350kHz operation. The minimum inductance for 30% ripple current is:

$$\Delta I_L = \frac{V_{OUT}}{(f)(L)}\left(1-\frac{V_{OUT}}{V_{IN}}\right)$$

A 4.7µH inductor will produce 29% ripple current. The peak inductor current will be the maximum DC value plus one half the ripple current, or 5.73A. Increasing the ripple current will also help ensure that the minimum on-time of 95ns is not violated. The minimum on-time occurs at maximum V_{IN}:

$$t_{ON(MIN)} = \frac{V_{OUT}}{V_{IN}(f)} = \frac{3.3V}{22V(350kHz)} = 429ns$$

The equivalent R_{SENSE} resistor value can be calculated by using the minimum value for the maximum current sense threshold (64mV):

$$R_{SENSE} \le \frac{64mV}{5.73A} = 0.011\Omega$$

Choosing 0.5% resistors: R_A = 24.9k and R_B = 77.7k yields an output voltage of 3.296V.

The power dissipation on the topside MOSFET can be easily estimated. Choosing a Fairchild FDS6982S dual MOSFET results in: $R_{DS(ON)}$ = 0.035Ω/0.022Ω, C_{MILLER} = 215pF. At maximum input voltage with T(estimated) = 50°C:

$$P_{MAIN} = \frac{3.3V}{22V}(5A)^2\left[1+(0.005)(50°C-25°C)\right](0.035\Omega)+(22V)^2\frac{5A}{2}(2.5\Omega)(215pF)\bullet\left[\frac{1}{5V-2.3V}+\frac{1}{2.3V}\right](350kHz) = 331mW$$

A short-circuit to ground will result in a folded back current of:

$$I_{SC} = \frac{32mV}{0.015\Omega}-\frac{1}{2}\left(\frac{95ns(22V)}{4.7\mu H}\right) = 2.98A$$

with a typical value of $R_{DS(ON)}$ and δ = (0.005/°C)(25°C) = 0.125. The resulting power dissipated in the bottom MOSFET is:

$$P_{SYNC} = (2.98A)^2(1.125)(0.022\Omega) = 220mW$$

which is less than full-load conditions.

C_{IN} is chosen for an RMS current rating of at least 3A at temperature assuming only this channel is on. C_{OUT} is chosen with an ESR of 0.02Ω for low output ripple voltage. The output ripple in continuous mode will be highest at the maximum input voltage. The output voltage ripple due to ESR is approximately:

$$V_{ORIPPLE} = R_{ESR}(\Delta I_L) = 0.02\Omega(1.45A) = 29mV_{P-P}$$

APPLICATIONS INFORMATION

PC Board Layout Checklist

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the IC. These items are also illustrated graphically in the layout diagram of Figure 11. Figure 12 illustrates the current waveforms present in the various branches of the 2-phase synchronous regulators operating in the continuous mode. Check the following in your layout:

1. Are the top N-channel MOSFETs MTOP1 and MTOP2 located within 1cm of each other with a common drain connection at C_{IN}? Do not attempt to split the input decoupling for the two channels as it can cause a large resonant loop.
2. Are the signal and power grounds kept separate? The combined IC signal ground pin and the ground return of C_{INTVCC} must return to the combined C_{OUT} (–) terminals. The path formed by the top N-channel MOSFET, Schottky diode and the C_{IN} capacitor should have short leads and PC trace lengths. The output capacitor (–) terminals should be connected as close as possible to the (–) terminals of the input capacitor by placing the capacitors next to each other and away from the Schottky loop described above.
3. Do the LTC3858-2 V_{FB} pins' resistive dividers connect to the (+) terminals of C_{OUT}? The resistive divider must be connected between the (+) terminal of C_{OUT} and signal ground. The feedback resistor connections should not be along the high current input feeds from the input capacitor(s).
4. Are the $SENSE^-$ and $SENSE^+$ leads routed together with minimum PC trace spacing? The filter capacitor between $SENSE^+$ and $SENSE^-$ should be as close as possible to the IC. Ensure accurate current sensing with Kelvin connections at the SENSE resistor.
5. Is the $INTV_{CC}$ decoupling capacitor connected close to the IC, between the $INTV_{CC}$ and the power ground pins? This capacitor carries the MOSFET drivers' current peaks. An additional 1µF ceramic capacitor placed immediately next to the $INTV_{CC}$ and PGND pins can help improve noise performance substantially.
6. Keep the switching nodes (SW1, SW2), top gate nodes (TG1, TG2), and boost nodes (BOOST1, BOOST2) away from sensitive small-signal nodes, especially from the opposites channel's voltage and current sensing feedback pins. All of these nodes have very large and fast moving signals and therefore should be kept on the "output side" of the LTC3858-2 and occupy minimum PC trace area.
7. Use a modified "star ground" technique: a low impedance, large copper area central grounding point on the same side of the PC board as the input and output capacitors with tie-ins for the bottom of the $INTV_{CC}$ decoupling capacitor, the bottom of the voltage feedback resistive divider and the SGND pin of the IC.

APPLICATIONS INFORMATION

PC Board Layout Debugging

Start with one controller on at a time. It is helpful to use a DC-50MHz current probe to monitor the current in the inductor while testing the circuit. Monitor the output switching node (SW pin) to synchronize the oscilloscope to the internal oscillator and probe the actual output voltage as well. Check for proper performance over the operating voltage and current range expected in the application. The frequency of operation should be maintained over the input voltage range down to dropout and until the output load drops below the low current operation threshold—typically 10% of the maximum designed current level in Burst Mode operation.

The duty cycle percentage should be maintained from cycle to cycle in a well-designed, low noise PCB implementation. Variation in the duty cycle at a subharmonic rate can suggest noise pickup at the current or voltage sensing inputs or inadequate loop compensation. Overcompensation of the loop can be used to tame a poor PC layout if regulator bandwidth optimization is not required. Only after each controller is checked for its individual performance should both controllers be turned on at the same time. A particularly difficult region of operation is when one controller channel is nearing its current comparator trip point when the other channel is turning on its top MOSFET. This occurs around 50% duty cycle on either channel due to the phasing of the internal clocks and may cause minor duty cycle jitter.

Reduce V_{IN} from its nominal level to verify operation of the regulator in dropout. Check the operation of the undervoltage lockout circuit by further lowering V_{IN} while monitoring the outputs to verify operation.

Investigate whether any problems exist only at higher output currents or only at higher input voltages. If problems coincide with high input voltages and low output currents, look for capacitive coupling between the BOOST, SW, TG, and possibly BG connections and the sensitive voltage and current pins. The capacitor placed across the current sensing pins needs to be placed immediately adjacent to the pins of the IC. This capacitor helps to minimize the effects of differential noise injection due to high frequency capacitive coupling. If problems are encountered with high current output loading at lower input voltages, look for inductive coupling between C_{IN}, Schottky and the top MOSFET components to the sensitive current and voltage sensing traces. In addition, investigate common ground path voltage pickup between these components and the SGND pin of the IC.

An embarrassing problem, which can be missed in an otherwise properly working switching regulator, results when the current sensing leads are hooked up backwards. The output voltage under this improper hookup will still be maintained but the advantages of current mode control will not be realized. Compensation of the voltage loop will be much more sensitive to component selection. This behavior can be investigated by temporarily shorting out the current sensing resistor—don't worry, the regulator will still maintain control of the output voltage.

APPLICATIONS INFORMATION

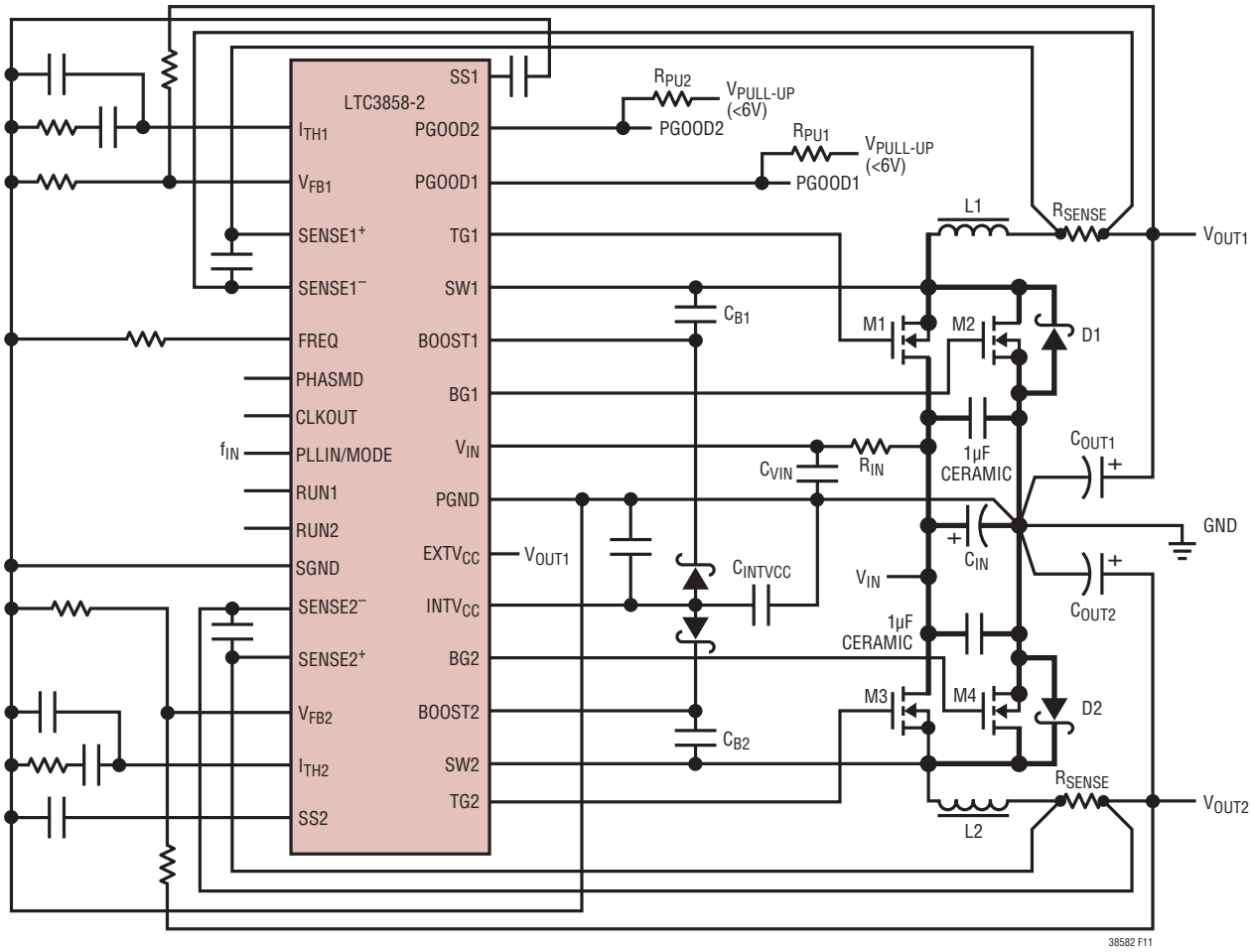


Figure 11. Recommended Printed Circuit Layout Diagram

APPLICATIONS INFORMATION

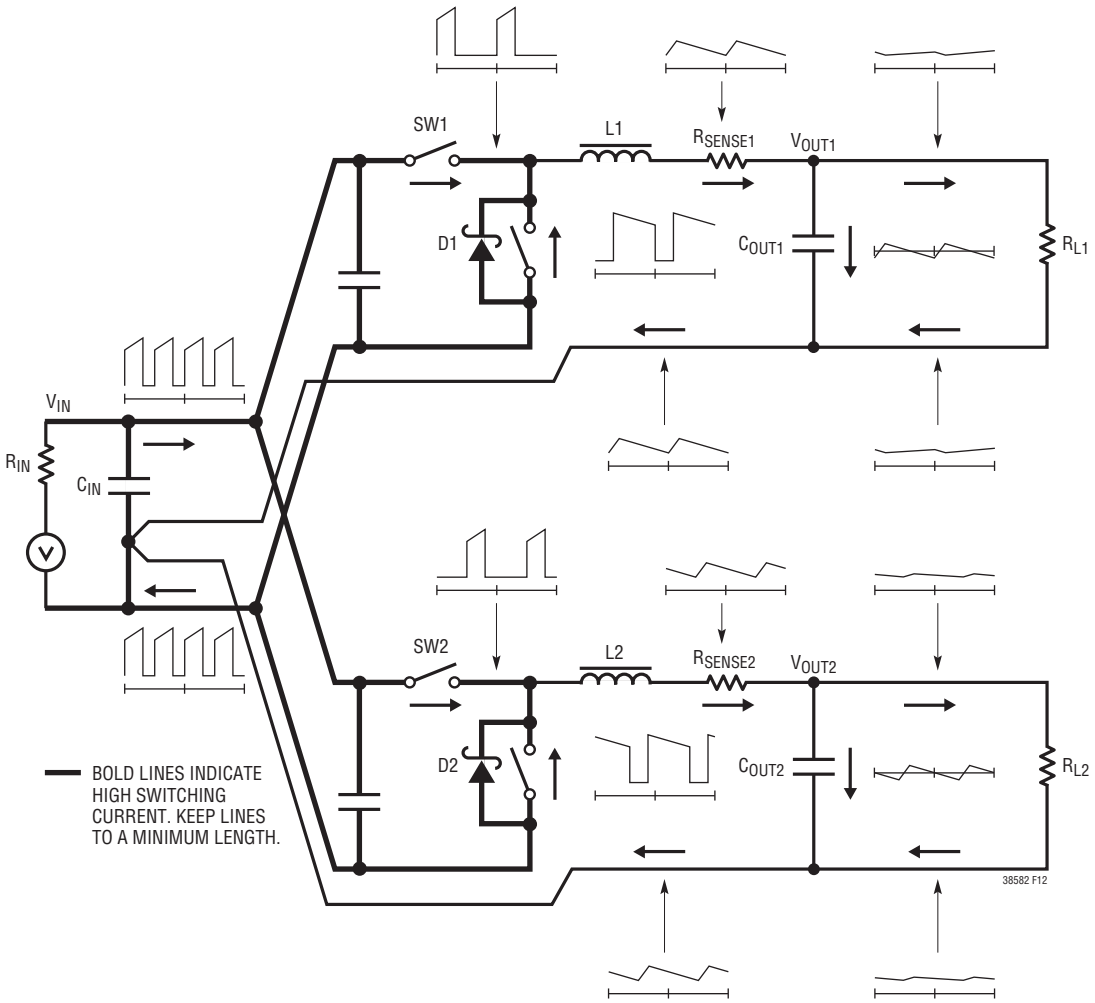
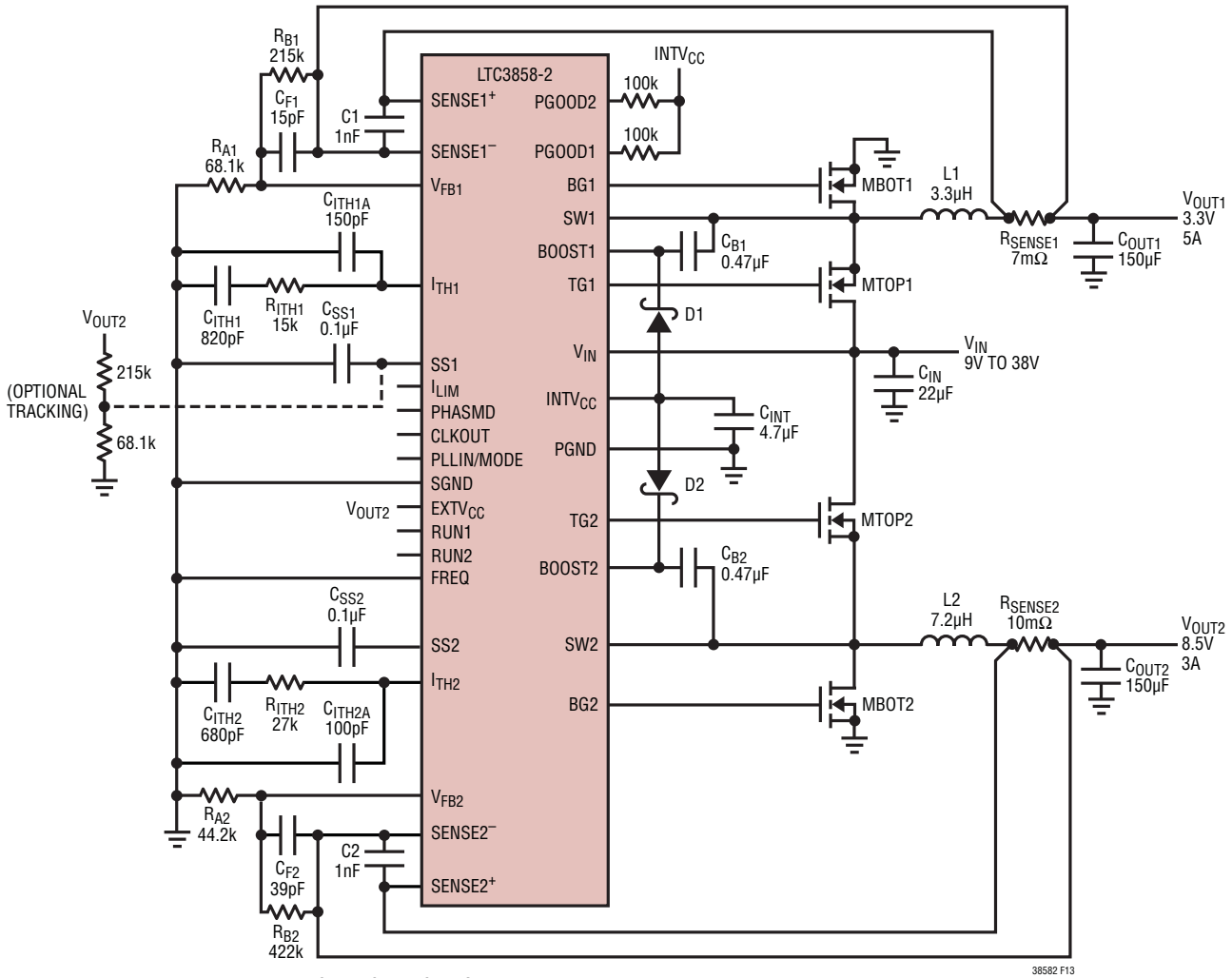


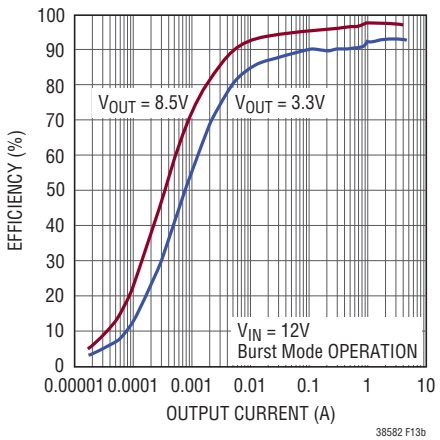
Figure 12. Branch Current Waveforms

TYPICAL APPLICATIONS

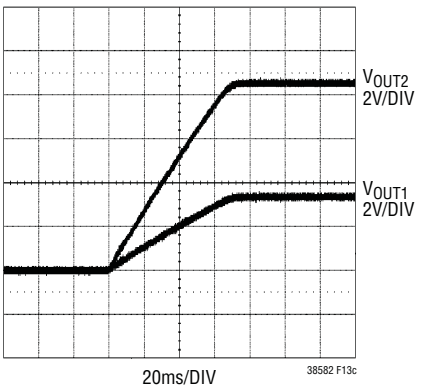


C_{OUT1}, C_{OUT2}: SANYO 10TPD150M
L1: SUMIDA CDEP105-3R2M
L2: SUMIDA CDEP105-7R2M
MTOP1, MTOP2, MBOT1, MBOT2: VISHAY Si7848DP

Efficiency vs Output Current



Start-Up



SW Node Waveforms

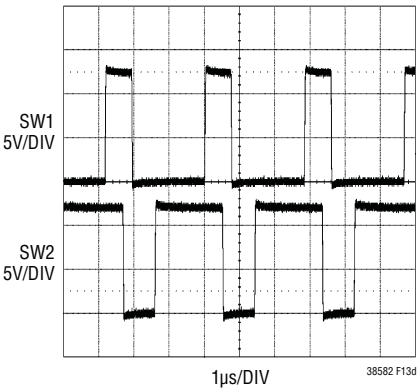
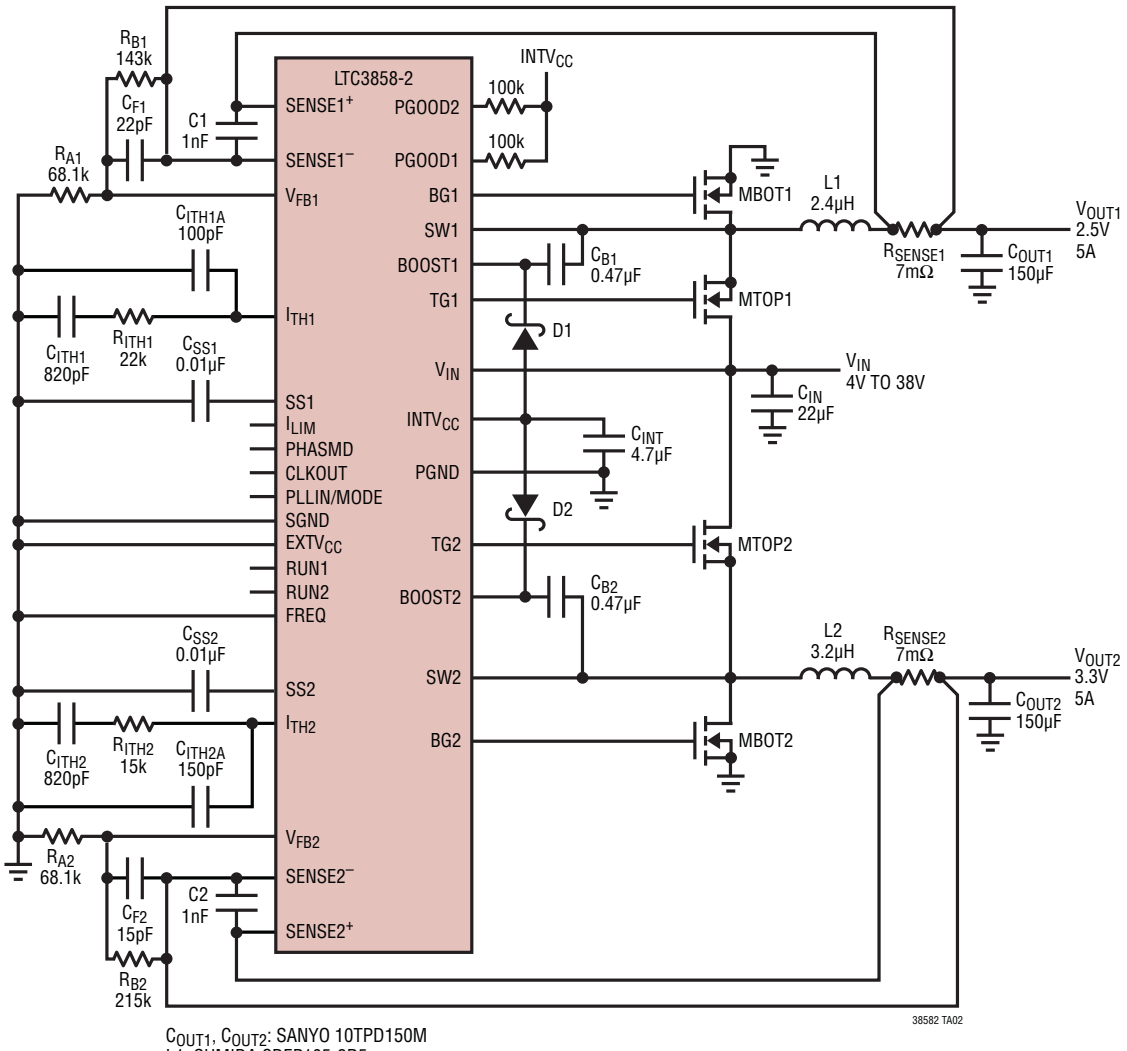


Figure 13. High Efficiency Dual 8.5V/3.3V Step-Down Converter

TYPICAL APPLICATIONS

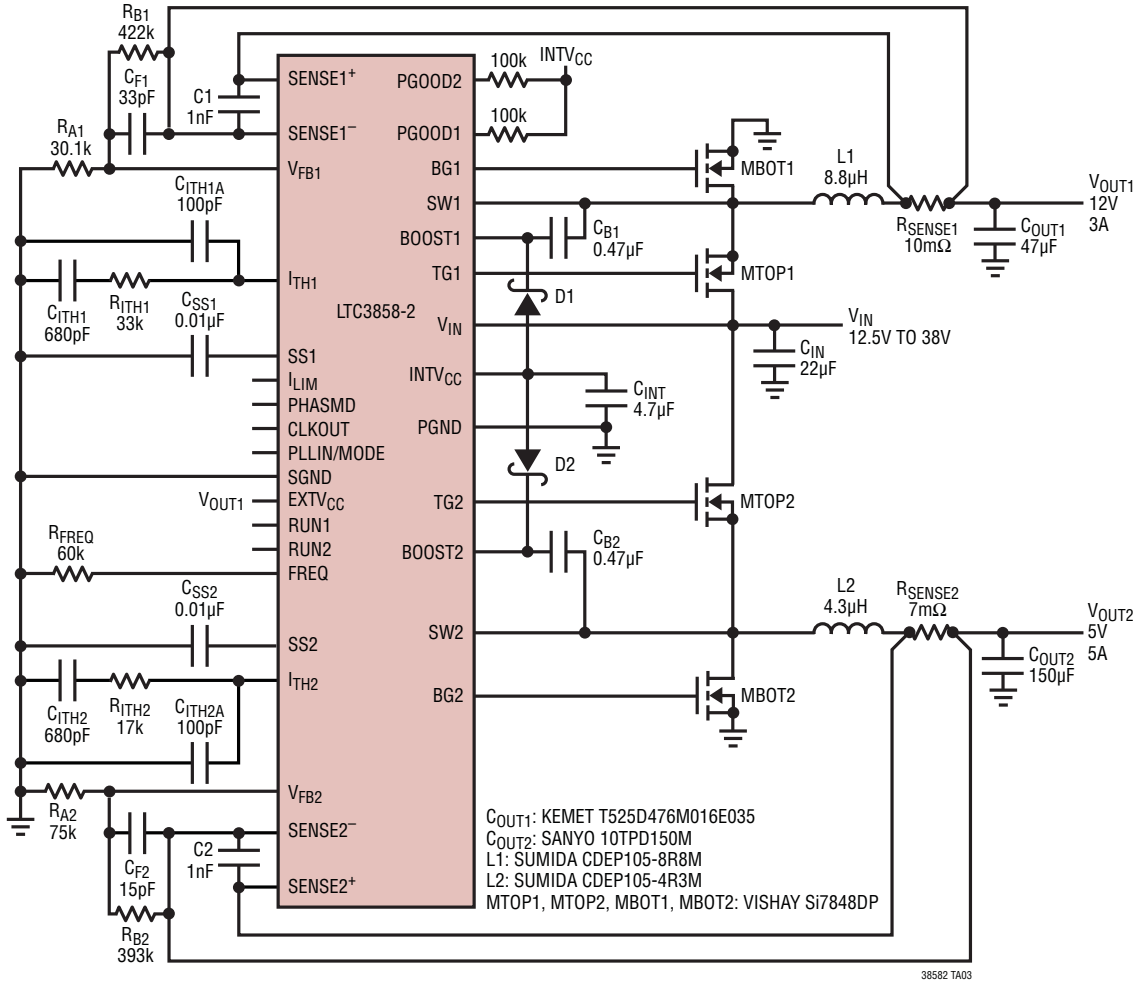
High Efficiency Dual 2.5V/3.3V Step-Down Converter



C_{OUT1}, C_{OUT2}: SANYO 10TPD150M
L1: SUMIDA CDEP105-2R5
L2: SUMIDA CDEP105-3R2M
MTOP1, MTOP2, MBOT1, MBOT2: VISHAY Si7848DP

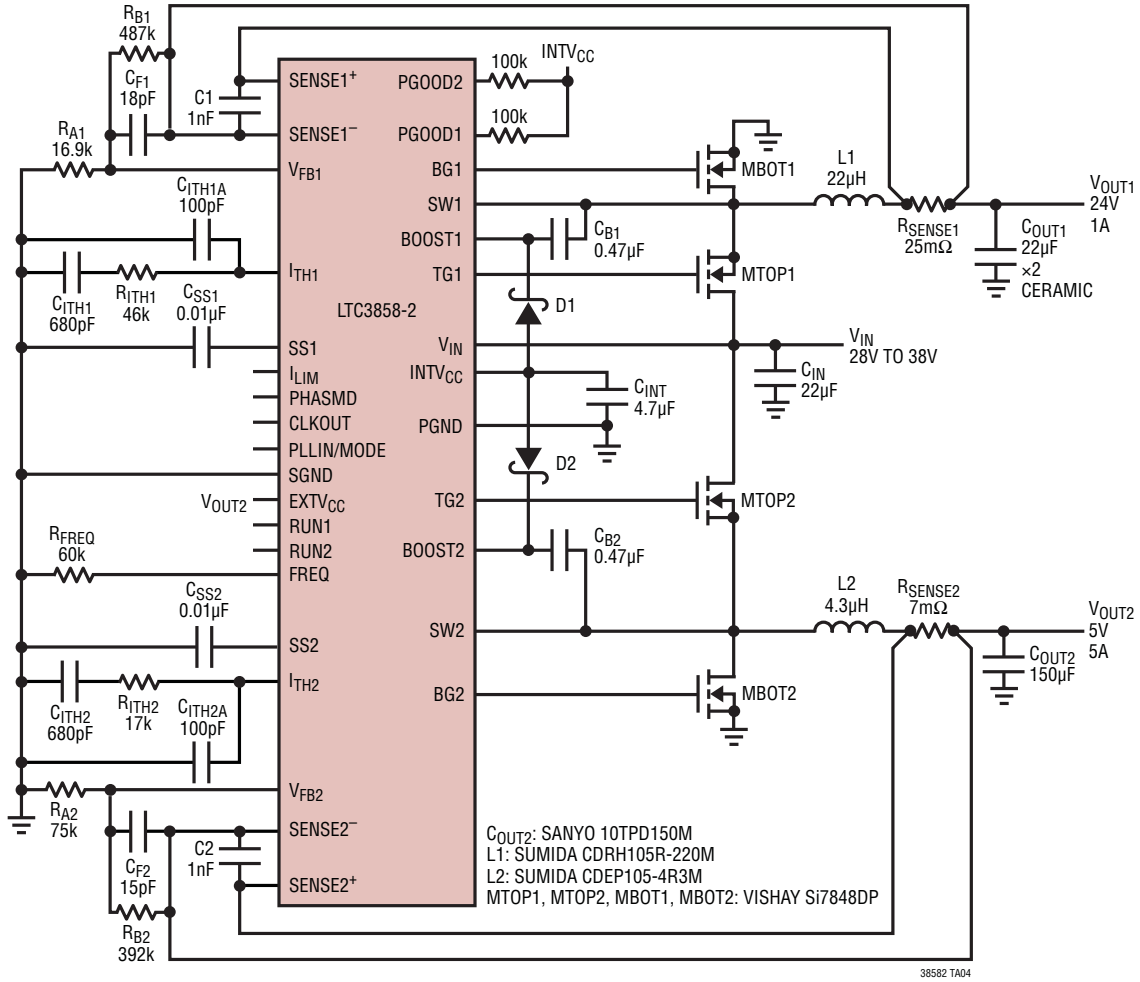
TYPICAL APPLICATIONS

High Efficiency Dual 12V/5V Step-Down Converter



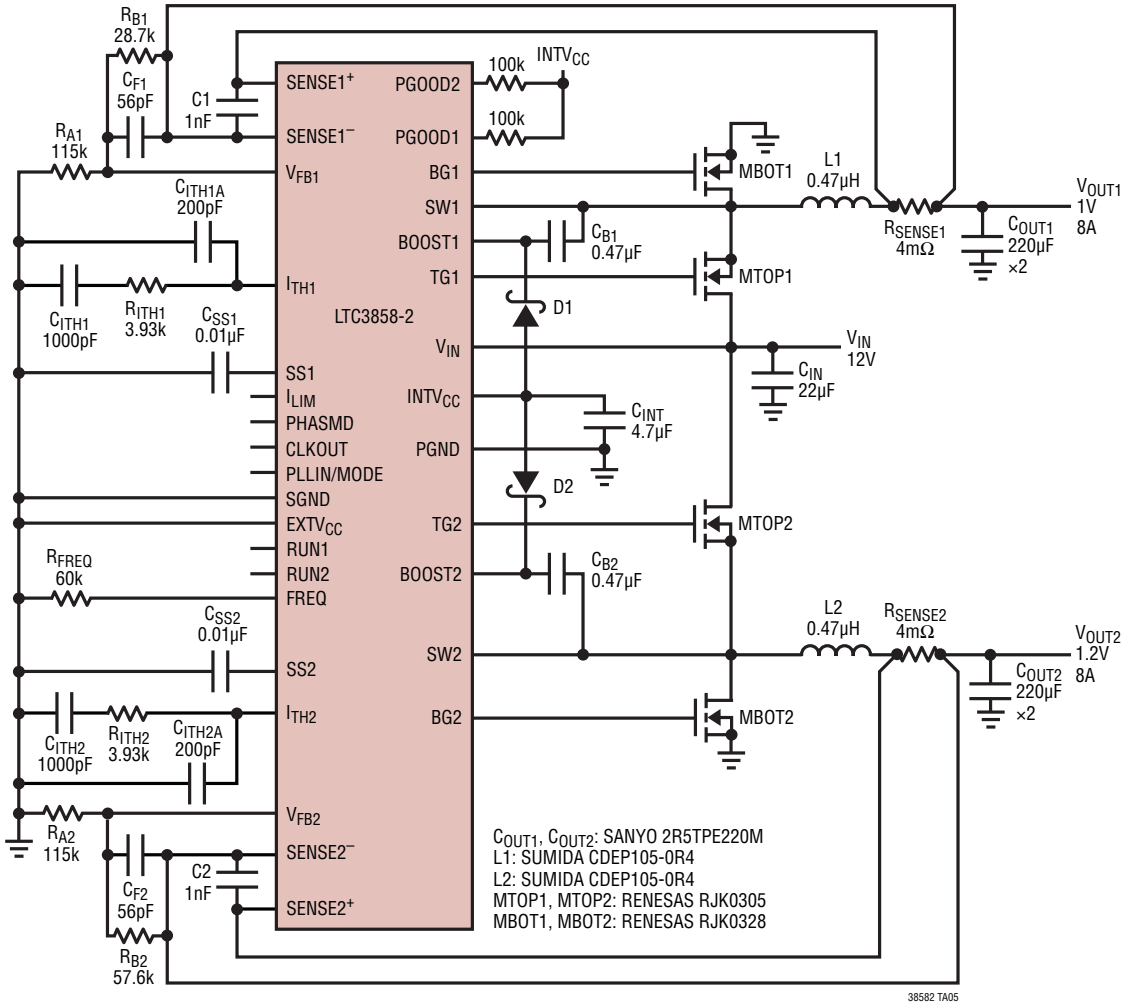
TYPICAL APPLICATIONS

High Efficiency Dual 24V/5V Step-Down Converter



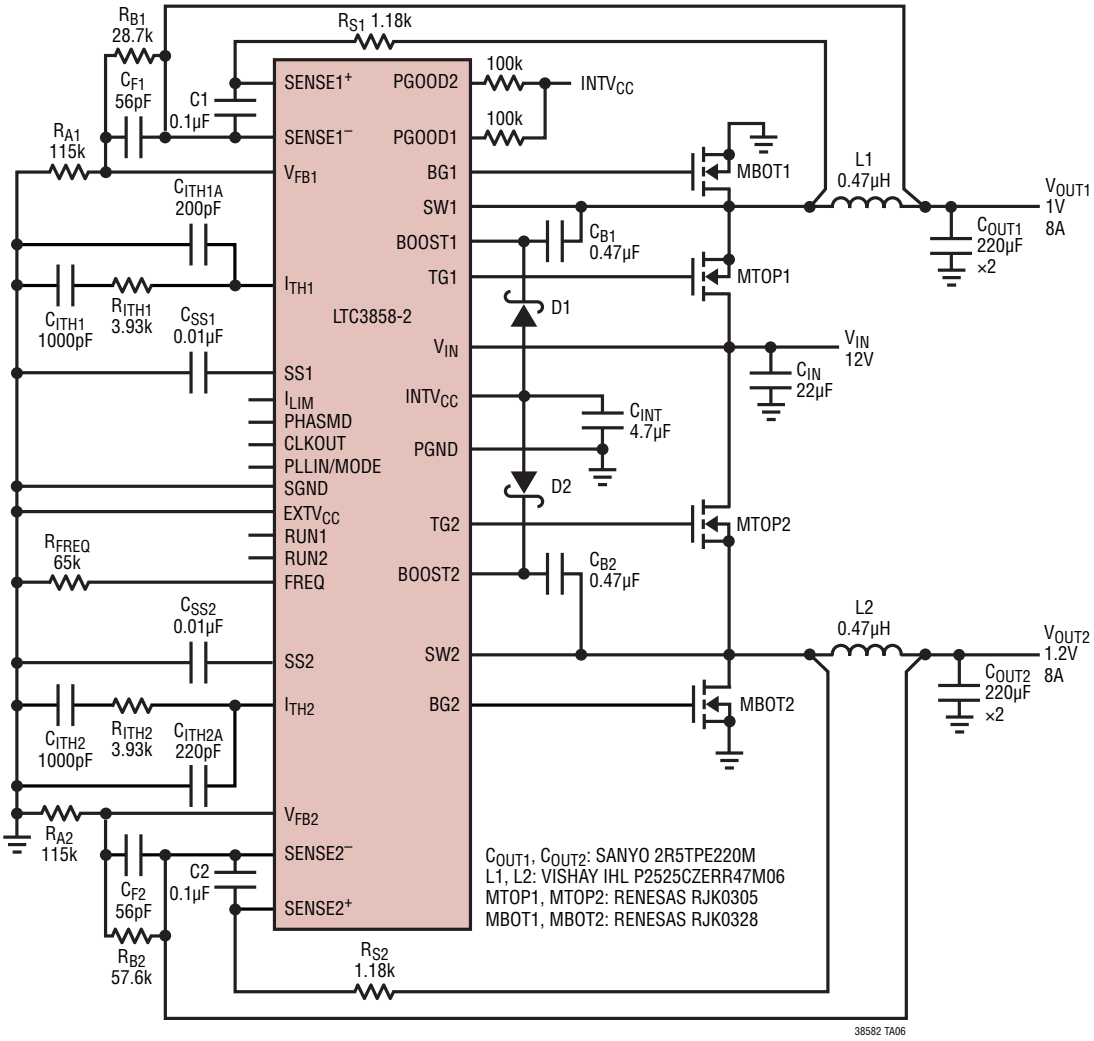
TYPICAL APPLICATIONS

High Efficiency Dual 1V/1.2V Step-Down Converter



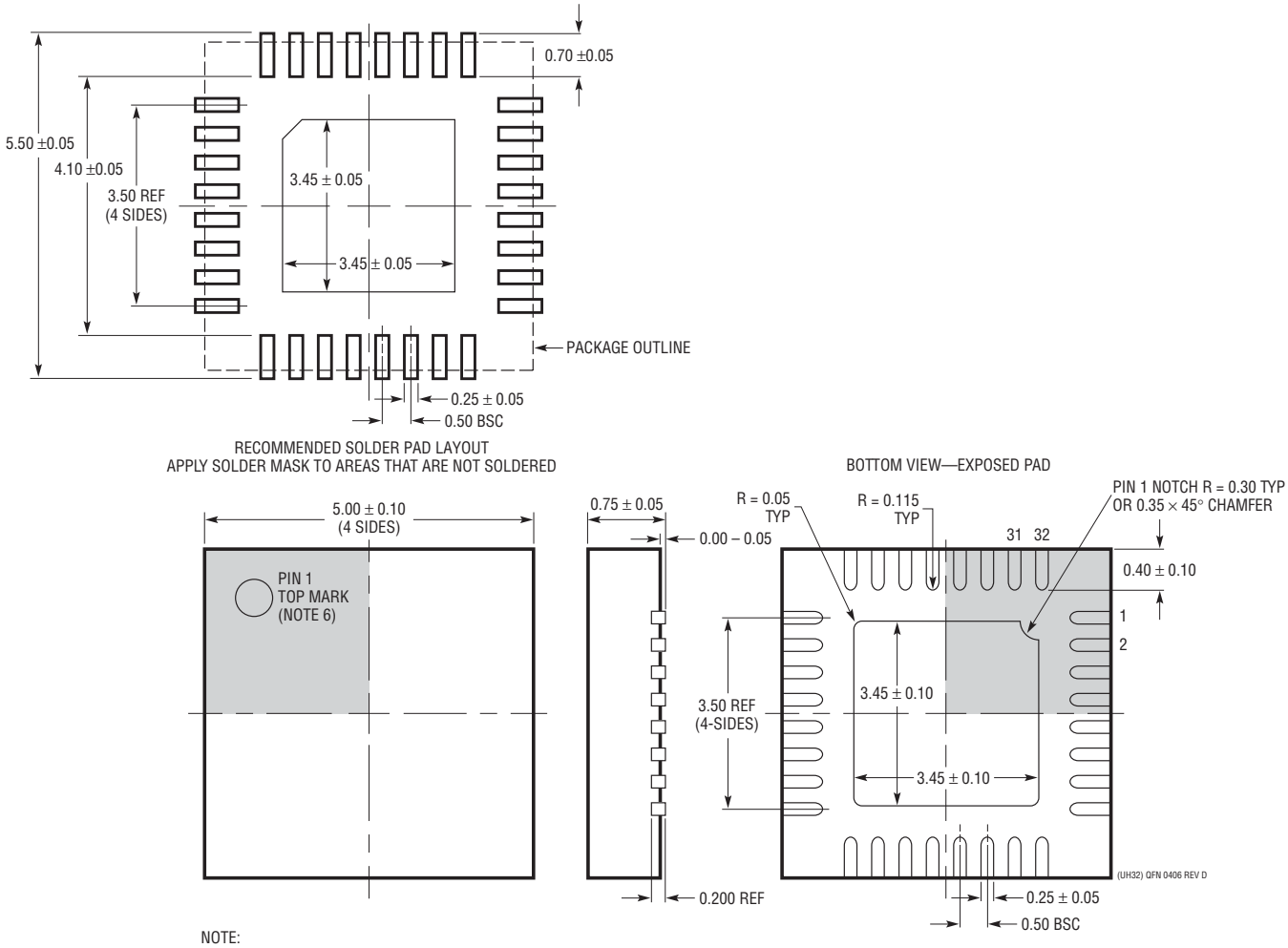
TYPICAL APPLICATIONS

High Efficiency Dual 1V/1.2V Step-Down Converter with Inductor DCR Current Sensing



PACKAGE DESCRIPTION

UH Package
32-Lead Plastic QFN (5mm × 5mm)
(Reference LTC DWG # 05-08-1693 Rev D)

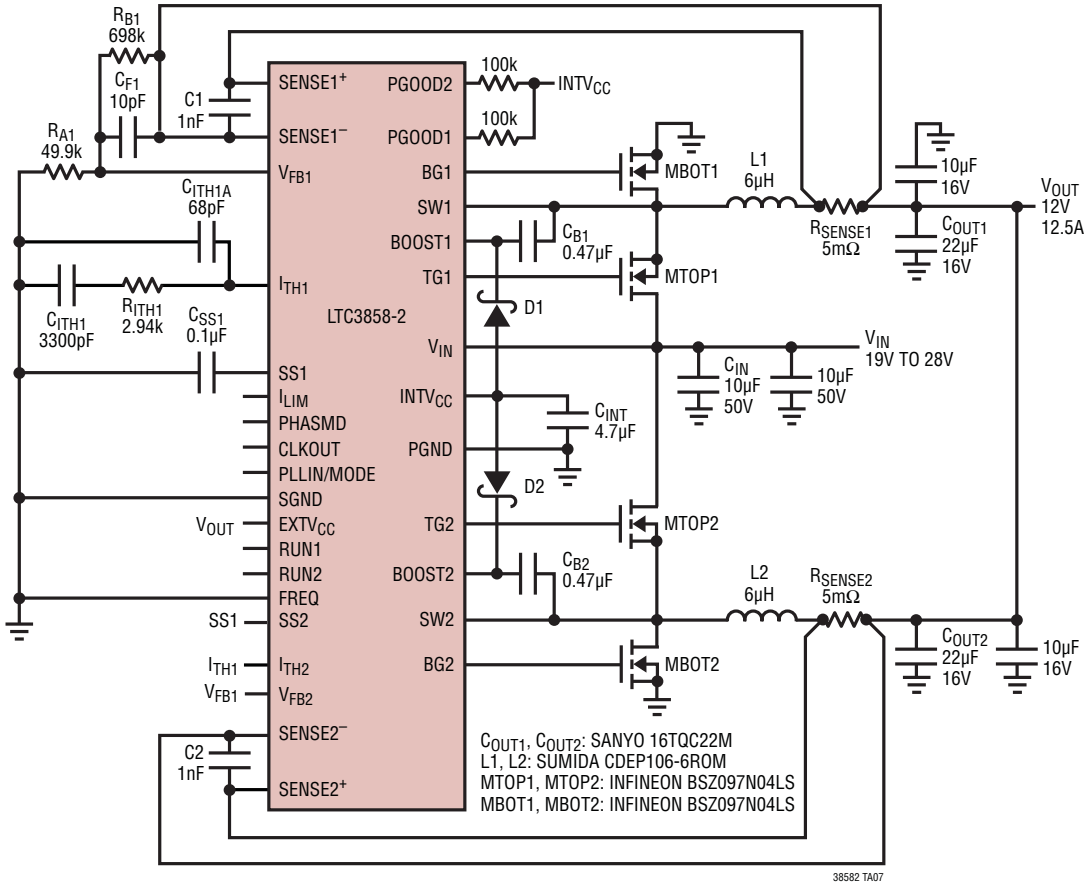


NOTE:
1. DRAWING PROPOSED TO BE A JEDEC PACKAGE OUTLINE
   M0-220 VARIATION WHHD-(X) (TO BE APPROVED)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE
   MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION
   ON THE TOP AND BOTTOM OF PACKAGE

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

TYPICAL APPLICATION

High Efficiency 2-Phase 12V/150W Step-Down Converter



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC3859	Low I_Q, Triple Output Buck/Buck/Boost Synchronous DC/DC Controller	Outputs (≥5V) Remain in Regulation Through Cold Crank 2.5V ≤ V_{IN} ≤ 38V, $V_{OUT(BUCKS)}$ Up to 24V, $V_{OUT(BOOST)}$ Up to 60V, I_Q = 55µA,
LTC3868/LTC3868-1	Low I_Q, Dual Output 2-Phase Synchronous Step-Down DC/DC Controllers with 99% Duty Cycle	Phase-Lockable Fixed Operating Frequency 50kHz to 900kHz, 4V ≤ V_{IN} ≤ 24V, 0.8V ≤ V_{OUT} ≤ 14V, I_Q = 170µA
LTC3857/LTC3857-1	Low I_Q, Dual Output 2-Phase Synchronous Step-Down DC/DC Controllers with 99% Duty Cycle	Phase-Lockable Fixed Operating Frequency 50kHz to 900kHz, 4V≤ V_{IN} ≤ 38V, 0.8V ≤ V_{OUT} ≤ 24V, I_Q = 50µA,
LTC3890/LTC3890-1	60V, Low I_Q, Dual 2-Phase Synchronous Step-Down DC/DC Controller with 99% Duty Cycle	Phase-Lockable Fixed Operating Frequency 50kHz to 900kHz, 4V ≤ V_{IN} ≤ 60V, 0.8V ≤ V_{OUT} ≤ 24V, I_Q = 50µA,
LTC3834/LTC3834-1	Low I_Q, Synchronous Step-Down DC/DC Controllers	Phase-Lockable Fixed Operating Frequency 140kHz to 650kHz, 4V ≤ V_{IN} ≤ 36V, 0.8V ≤ V_{OUT} ≤ 10V, I_Q = 30µA,
LTC3835/LTC3835-1	Low I_Q, Synchronous Step-Down DC/DC Controllers	Phase-Lockable Fixed Operating Frequency 140kHz to 650kHz, 4V ≤ V_{IN} ≤ 36V, 0.8V ≤ V_{OUT} ≤ 10V, I_Q = 80µA,
LTC3891	60V, Low I_Q, Synchronous Step-Down DC/DC Controller with 99% Duty Cycle	Phase-Lockable Fixed Operating Frequency 50kHz to 900kHz, 4V ≤ V_{IN} ≤ 60V, 0.8V ≤ V_{OUT} ≤ 24V, I_Q = 50µA,
LTC3824	Low I_Q, High Voltage DC/DC Controller, 100% Duty Cycle	Selectable Fixed 200kHz to 600kHz Operating Frequency 4V ≤ V_{IN} ≤ 60V, 0.8V ≤ V_{OUT} ≤ V_{IN}, I_Q = 40µA, MSOP-10E

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LT 1110 • PRINTED IN USA
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