Synchronous Step-Down Switching Regulator Controller

FEATURES

- **Wide V_{IN} Range: 4V to 38V Operation**
- **R_{SENSE} or DCR Current Sensing**
- **±1% Output Voltage Accuracy**
- **Phase-Lockable Fixed Frequency: 250kHz to 750kHz**
- Dual N-Channel MOSFET Synchronous Drive
- Very Low Dropout Operation: 99% Duty Cycle
- Adjustable Output Voltage Soft-Start or Tracking
- Output Current Foldback Limiting
- Output Overvoltage Protection
- 5V Internal Regulator
- OPTI-LOOP® Compensation Minimizes C_{OUT}
- Selectable Continuous, Pulse-Skipping or Burst Mode® Operation at Light Loads
- Low Shutdown I_Q: 20µA
- V_{OUT} Range: 0.8V to 5.5V
- Thermally Enhanced 16-Lead MSOP, 16-Lead Narrow SSOP or 3mm × 3mm QFN Package

APPLICATIONS

- Automotive Systems
- Telecom Systems
- Industrial Equipment
- Distributed DC Power Systems

DESCRIPTION

The LTC®3851A is a high performance synchronous step-down switching regulator controller that drives an all N-channel synchronous power MOSFET stage. A constant frequency current mode architecture allows a phase-lockable frequency of up to 750kHz.

OPTI-LOOP compensation allows the transient response to be optimized over a wide range of output capacitance and ESR values. The LTC3851A features a precision 0.8V reference that is compatible with a wide 4V to 38V input supply range.

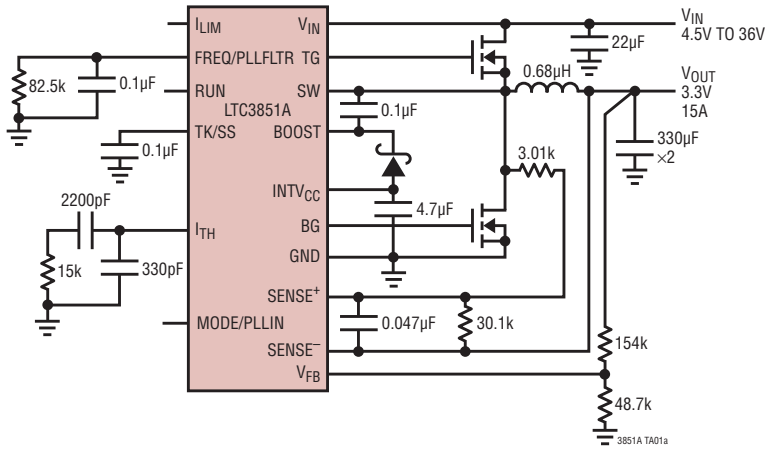
The TK/SS pin ramps the output voltage during start-up. Current foldback limits MOSFET heat dissipation during short-circuit conditions. The MODE/PLLIN pin selects among Burst Mode operation, pulse-skipping mode or continuous inductor current mode at light loads and allows the IC to be synchronized to an external clock. The LTC3851A contains an improved PLL compared to the LTC3851.

The LTC3851A-1 is a version with a power good output signal instead of adjustable current limit.

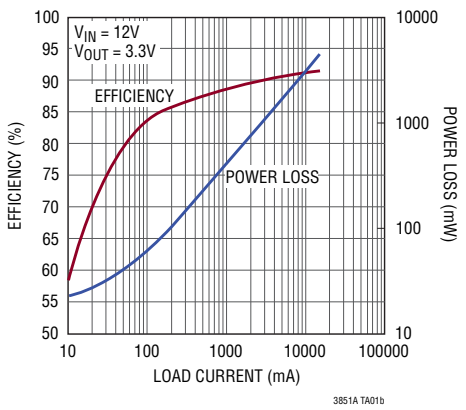
LT, LTC, LTM, Burst Mode, OPTI-LOOP, Linear Technology and the Linear logo are registered trademarks and No R_{SENSE}, UltraFast are trademarks of Linear Technology Corporation. All other trademarks are the property of their respective owners. Protected by U.S. Patents including 5408150, 5481178, 5705919, 5929620, 6304066, 6498466, 6580258, 6611131.

TYPICAL APPLICATION

High Efficiency Synchronous Step-Down Converter



Efficiency and Power Loss vs Load Current

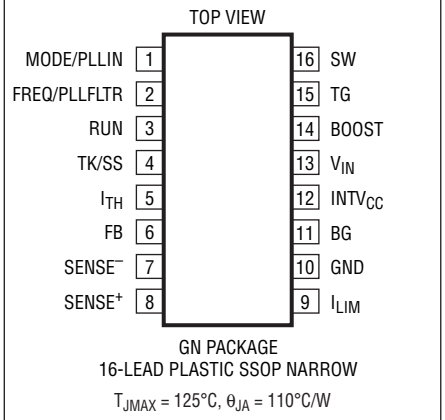


ABSOLUTE MAXIMUM RATINGS (Note 1)

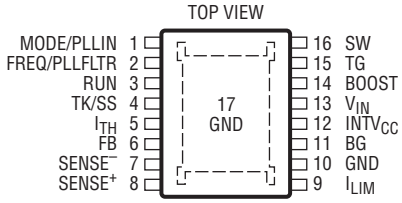
Input Supply Voltage (V_{IN}) ..... 40V to –0.3V
Topside Driver Voltage (BOOST) ..... 46V to –0.3V
Switch Voltage (SW) ..... 40V to –5V
$INTV_{CC}$, (BOOST – SW), RUN ..... 6V to –0.3V
TK/SS, I_{LIM} ..... $INTV_{CC}$ to –0.3V
$SENSE^+$, $SENSE^-$ ..... 6V to –0.3V
MODE/PLLIN, FREQ/PLLFLTR ..... $INTV_{CC}$ to –0.3V
I_{TH}, V_{FB} Voltages ..... 3V to –0.3V

$INTV_{CC}$ Peak Output Current 50mA
Operating Junction Temperature Range (Notes 2, 3)
E-Grade, I-Grade ..... –40°C to 125°C
H-Grade ..... –40°C to 150°C
MP-Grade ..... –55°C to 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)
GN/MSE ..... 300°C

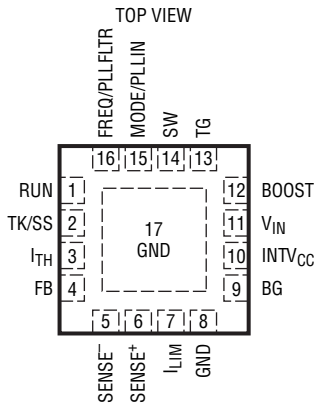
PIN CONFIGURATION



GN PACKAGE
16-LEAD PLASTIC SSOP NARROW
T_{JMAX} = 125°C, θ_{JA} = 110°C/W



MSE PACKAGE
16-LEAD PLASTIC MSOP
T_{JMAX} = 125°C, θ_{JA} = 35°C/W TO 40°C/W
EXPOSED PAD (PIN 17) IS GND,
MUST BE SOLDERED TO PCB



UD PACKAGE
16-LEAD (3mm × 3mm) PLASTIC QFN
T_{JMAX} = 125°C, θ_{JA} = 68°C/W, θ_{JC} = 4.2°C/W
EXPOSED PAD (PIN 17) IS GND,
MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3851AEGN#PBF	LTC3851AEGN#TRPBF	3851A	16-Lead Plastic SSOP	–40°C to 125°C
LTC3851AIGN#PBF	LTC3851AIGN#TRPBF	3851A	16-Lead Plastic SSOP	–40°C to 125°C
LTC3851AEMSE#PBF	LTC3851AEMSE#TRPBF	3851A	16-Lead Plastic MSOP	–40°C to 125°C
LTC3851AIMSE#PBF	LTC3851AIMSE#TRPBF	3851A	16-Lead Plastic MSOP	–40°C to 125°C
LTC3851AHMSE#PBF	LTC3851AHMSE#TRPBF	3851A	16-Lead Plastic MSOP	–40°C to 150°C
LTC3851AMPMSE#PBF	LTC3851AMPMSE#TRPBF	3851A	16-Lead Plastic MSOP	–55°C to 150°C
LTC3851AEUD#PBF	LTC3851AEUD#TRPBF	LFPZ	16-Lead (3mm × 3mm) Plastic QFN	–40°C to 125°C
LTC3851AIUD#PBF	LTC3851AIUD#TRPBF	LFPZ	16-Lead (3mm × 3mm) Plastic QFN	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{IN} = 15V, V_{RUN} = 5V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Main Control Loops							
V_{IN}	Operating Input Voltage Range		●	4		38	V
V_{FB}	Regulated Feedback Voltage	I_{TH} = 1.2V (Note 4) 0°C to 85°C	●	0.792	0.800	0.808	V
		I_{TH} = 1.2V (Note 4) –40°C to 125°C	●	0.788		0.812	V
		I_{TH} = 1.2V (Note 4) –40°C to 150°C	●	0.788		0.812	V
		I_{TH} = 1.2V (Note 4) –55°C to 150°C	●	0.788		0.812	V
I_{FB}	Feedback Current	(Note 4)			–10	–50	nA
$V_{REFLNREG}$	Reference Voltage Line Regulation	V_{IN} = 6V to 38V (Note 4)			0.002	0.02	%/V
$V_{LOADREG}$	Output Voltage Load Regulation	(Note 4) Measured in Servo Loop, ΔI_{TH} = 1.2V to 0.7V	●		0.01	0.1	%
		(Note 4) Measured in Servo Loop, ΔI_{TH} = 1.2V to 0.7V (H-Grade, MP-Grade)	●			0.2	%
		(Note 4) Measured in Servo Loop, ΔI_{TH} = 1.2V to 1.6V	●		–0.01	–0.1	%
		(Note 4) Measured in Servo Loop, ΔI_{TH} = 1.2V to 1.6V (H-Grade, MP-Grade)	●			–0.2	%
g_m	Transconductance Amplifier g_m	I_{TH} = 1.2V, Sink/Source = 5µA (Note 4)			2		mmho
g_m GBW	Transconductance Amp Gain Bandwidth	I_{TH} = 1.2V (Note 8)			3		MHz
I_Q	Input DC Supply Current	(Note 5)					
	Normal Mode	V_{RUN} = 5V			1.2		mA
	Shutdown	V_{RUN} = 0V			25	50	µA
UVLO	Undervoltage Lockout on $INTV_{CC}$	V_{INTVCC} Ramping Down			3.25		V
UVLO Hys	UVLO Hysteresis				0.4		V
V_{OVL}	Feedback Overvoltage Lockout	V_{FB} with Respect to Set Regulated Voltage V_{FB} Ramping Positive (OV)		7.5	10	12.5	%
I_{SENSE}	SENSE Pins Current				±1	±2	µA
$I_{TK/SS}$	Soft-Start Charge Current	$V_{TK/SS}$ = 0V		0.6	1	2	µA
V_{RUN}	RUN Pin On—Threshold	V_{RUN} Rising	●	1.10	1.22	1.35	V
V_{RUNHYS}	RUN Pin On—Hysteresis				120		mV
$V_{SENSE(MAX)}$	Maximum Current Sense Threshold	V_{FB} = 0.7V, V_{SENSE} = 3.3V, I_{LIM} = 0V	●	20	30	40	mV
		V_{FB} = 0.7V, V_{SENSE} = 3.3V, I_{LIM} = 0V (H-/MP-Grade)	●	15		45	mV
		V_{FB} = 0.7V, V_{SENSE} = 3.3V, I_{LIM} = Float	●	40	53	65	mV
		V_{FB} = 0.7V, V_{SENSE} = 3.3V, I_{LIM} = Float (H-/MP-Grade)	●	35		70	mV
		V_{FB} = 0.7V, V_{SENSE} = 3.3V, I_{LIM} = $INTV_{CC}$	●	65	80	95	mV
		V_{FB} = 0.7V, V_{SENSE} = 3.3V, I_{LIM} = $INTV_{CC}$ (H-/MP-Grade)	●	60		100	mV
TG R_{UP}	TG Driver Pull-Up On-Resistance	TG High			2.2		Ω
TG R_{DOWN}	TG Driver Pull-Down On-Resistance	TG Low			1.2		Ω
BG R_{UP}	BG Driver Pull-Up On-Resistance	BG High			2.1		Ω
BG R_{DOWN}	BG Driver Pull-Down On-Resistance	BG Low			1.1		Ω
	TG Transition Time	(Note 6)					
TG t_r	Rise Time	C_{LOAD} = 3300pF			25		ns
TG t_f	Fall Time	C_{LOAD} = 3300pF			25		ns
	BG Transition Time	(Note 6)					
BG tr	Rise Time	C_{LOAD} = 3300pF			25		ns
BG tf	Fall Time	C_{LOAD} = 3300pF			25		ns
TG/BG t_{1D}	Top Gate Off to Bottom Gate On Delay Bottom Switch-On Delay Time	C_{LOAD} = 3300pF Each Driver (Note 6)			30		ns
BG/TG t_{2D}	Bottom Gate Off to Top Gate On Delay Top Switch-On Delay Time	C_{LOAD} = 3300pF Each Driver (Note 6)			30		ns
$t_{ON(MIN)}$	Minimum On-Time	(Note 7)			90		ns

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{IN} = 15V, V_{RUN} = 5V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$INTV_{CC}$ Linear Regulator							
V_{INTVCC}	Internal V_{CC} Voltage	6V < V_{IN} < 38V		4.8	5	5.2	V
V_{LDO} INT	$INTV_{CC}$ Load Regulation	I_{CC} = 0mA to 50mA			0.5	2	%
Oscillator and Phase-Locked Loop							
f_{NOM}	Nominal Frequency	R_{FREQ} = 60k		460	500	540	kHz
f_{LOW}	Lowest Frequency	R_{FREQ} = 160k		205	235	265	kHz
f_{HIGH}	Highest Frequency	R_{FREQ} = 36k		690	750	810	kHz
$R_{MODE/PLLIN}$	MODE/PLLIN Input Resistance				100		kΩ
f_{MODE}	MODE/PLLIN Minimum Input Frequency MODE/PLLIN Maximum Input Frequency	V_{MODE} = External Clock V_{MODE} = External Clock			250 750		kHz kHz
I_{FREQ}	Phase Detector Output Current Sinking Capability Sourcing Capability	 $f_{MODE} > f_{OSC}$ $f_{MODE} < f_{OSC}$			 –90 75		 µA µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC3851A is tested under pulsed load conditions such that $T_A \approx T_J$. The LTC3851AE is guaranteed to meet performance specifications from 0°C to 85°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3851AI is guaranteed to meet specifications over the –40°C to 125°C operating junction temperature range, the LTC3851AH is guaranteed over the –40°C to 150°C operating junction temperature range and the LTC3851AMP is tested and guaranteed over the –55°C to 150°C operating junction temperature range. High junction temperatures degrade operating lifetimes; operating lifetime is derated for junction temperatures greater than 125°C. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors.

Note 3: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formulas:

LTC3851AGN: $T_J = T_A + (P_D \bullet 110°C/W)$

LTC3851AUD: $T_J = T_A + (P_D \bullet 68°C/W)$

LTC3851AMSE: $T_J = T_A + (P_D \bullet 40°C/W)$

Note 4: The LTC3851A is tested in a feedback loop that servos V_{ITH} to a specified voltage and measures the resultant V_{FB}.

Note 5: Dynamic supply current is higher due to the gate charge being delivered at the switching frequency. See Applications Information.

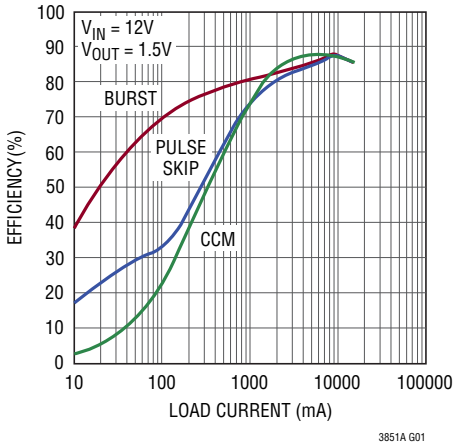
Note 6: Rise and fall times are measured using 10% and 90% levels. Delay times are measured using 50% levels. Rise and fall times are assured by design, characterization and correlation with statistical process controls.

Note 7: The minimum on-time condition is specified for an inductor peak-to-peak ripple current ~40% of I_{MAX} (see Minimum On-Time Considerations in the Applications Information section).

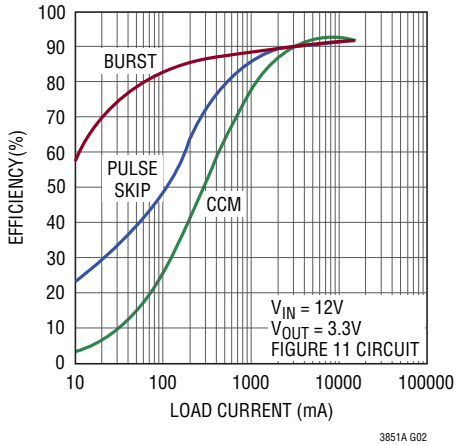
Note 8: Guaranteed by design; not tested in production.

TYPICAL PERFORMANCE CHARACTERISTICS

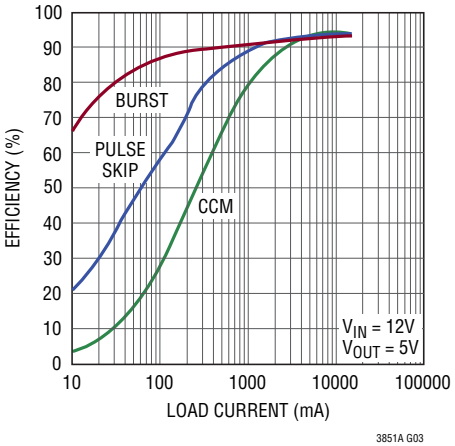
Efficiency vs Output Current and Mode



Efficiency vs Output Current and Mode

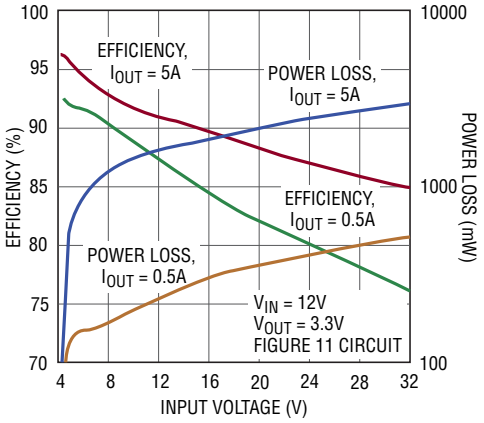


Efficiency vs Output Current and Mode

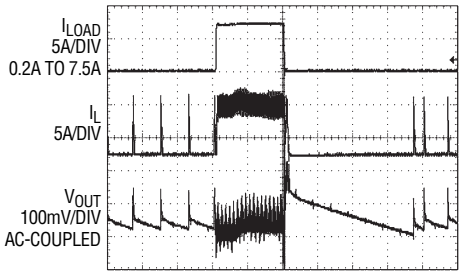


TYPICAL PERFORMANCE CHARACTERISTICS

Efficiency and Power Loss vs Input Voltage

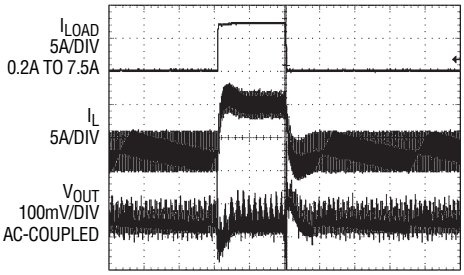


Load Step (Burst Mode Operation)



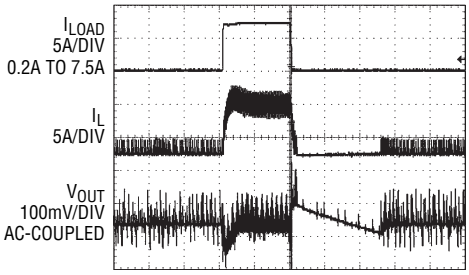
V_{OUT} = 1.5V 100µs/DIV
V_{IN} = 12V
FIGURE 11 CIRCUIT

Load Step (Forced Continuous Mode)



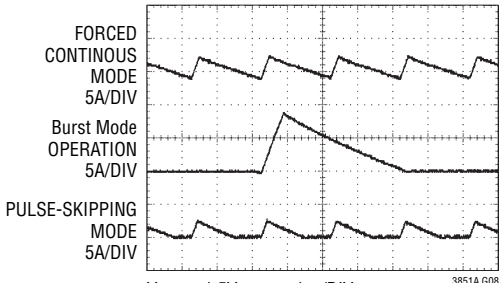
V_{OUT} = 1.5V 100µs/DIV
V_{IN} = 12V
FIGURE 11 CIRCUIT

Load Step (Pulse-Skipping Mode)



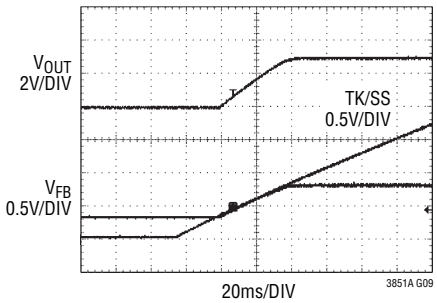
V_{OUT} = 1.5V 100µs/DIV
V_{IN} = 12V
FIGURE 11 CIRCUIT

Inductor Current at Light Load



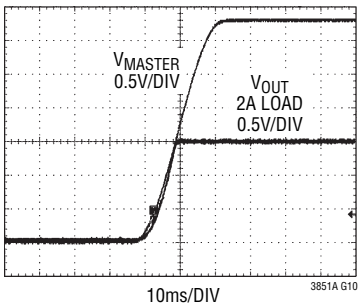
V_{OUT} = 1.5V 1µs/DIV
V_{IN} = 12V
I_{LOAD} = 1mA
FIGURE 11 CIRCUIT

Start-Up with Prebiased Output at 2V



20ms/DIV

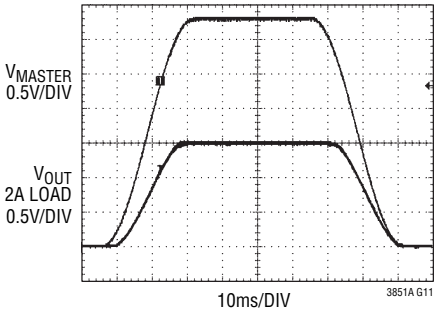
Coincident Tracking with Master Supply



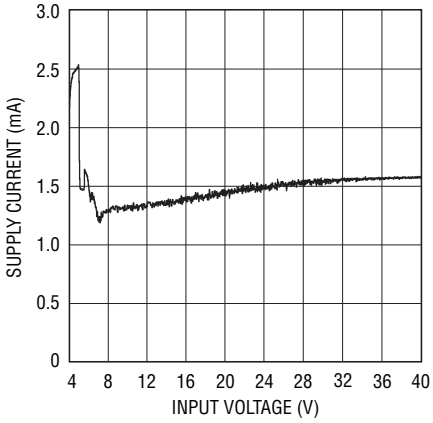
10ms/DIV

TYPICAL PERFORMANCE CHARACTERISTICS

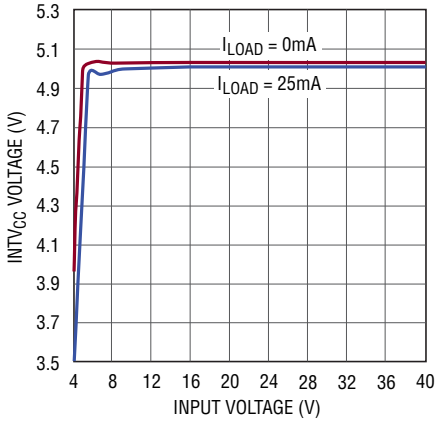
Ratiometric Tracking with Master Supply



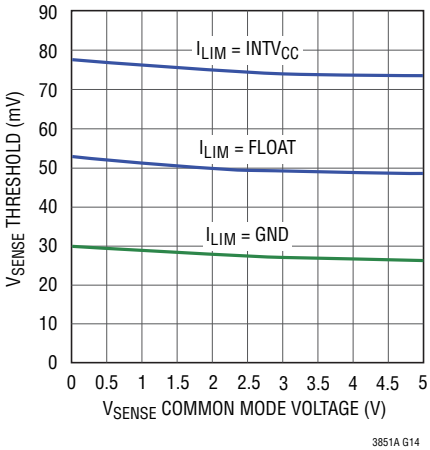
Input DC Supply Current vs Input Voltage



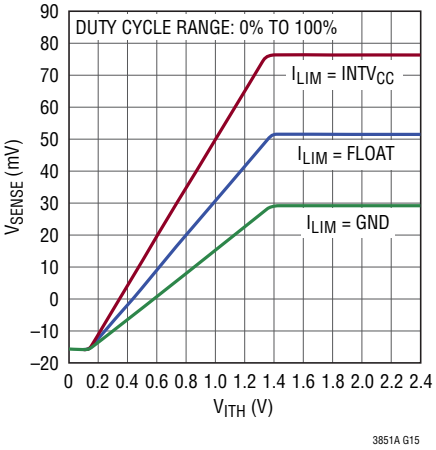
$INTV_{CC}$ Line Regulation



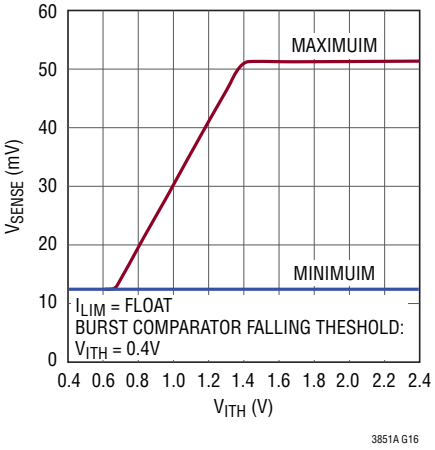
Maximum Current Sense Threshold vs Common Mode Voltage



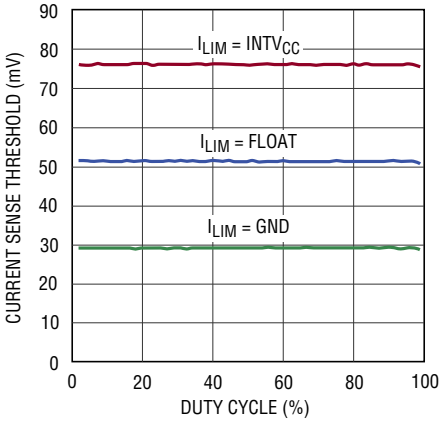
Maximum Peak Current Sense Threshold vs I_{TH} Voltage



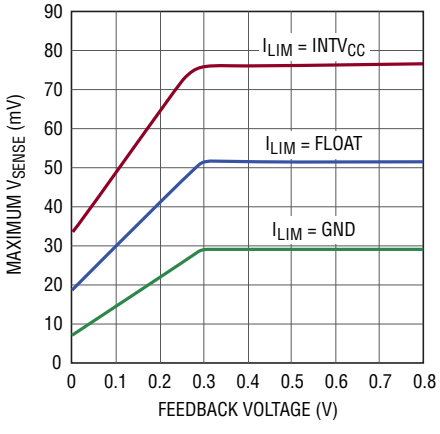
Burst Mode Peak Current Sense Threshold vs I_{TH} Voltage



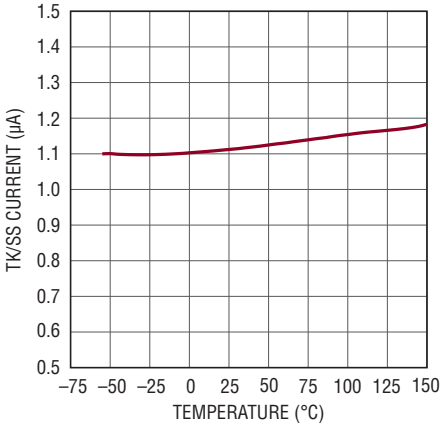
Maximum Current Sense Threshold vs Duty Cycle



Maximum Current Sense Threshold vs Feedback Voltage (Current Foldback)

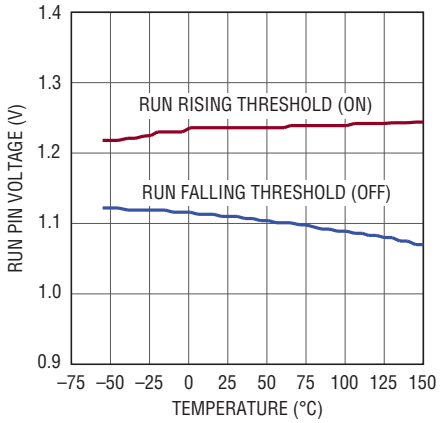


TK/SS Pull-Up Current vs Temperature



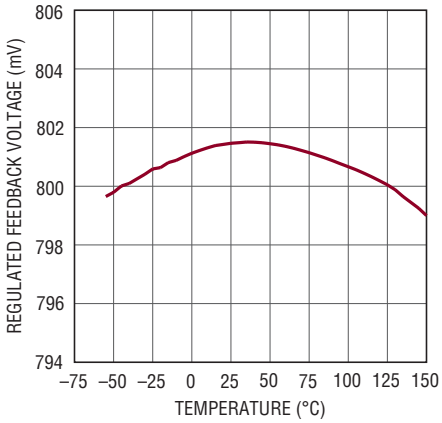
TYPICAL PERFORMANCE CHARACTERISTICS

Shutdown (RUN) Threshold vs Temperature



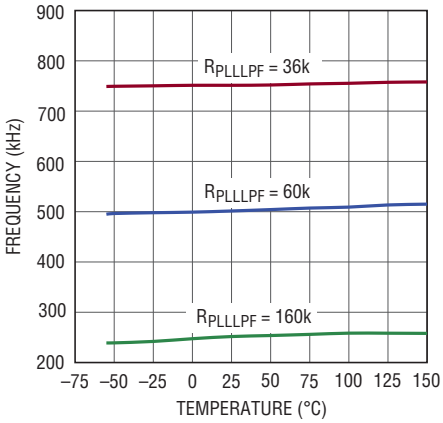
3851A G20

Regulated Feedback Voltage vs Temperature



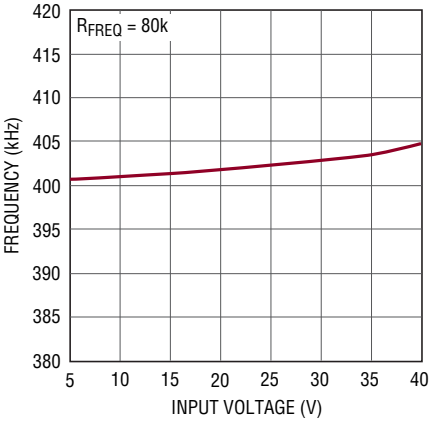
3851A G21

Oscillator Frequency vs Temperature



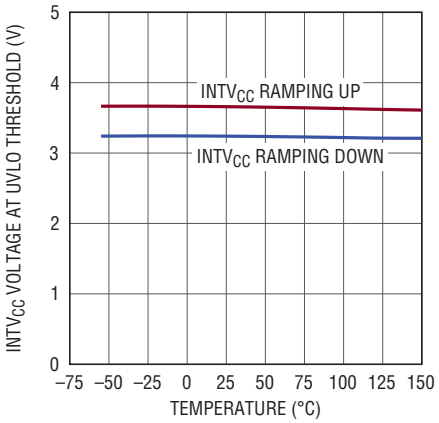
3851A G22

Oscillator Frequency vs Input Voltage



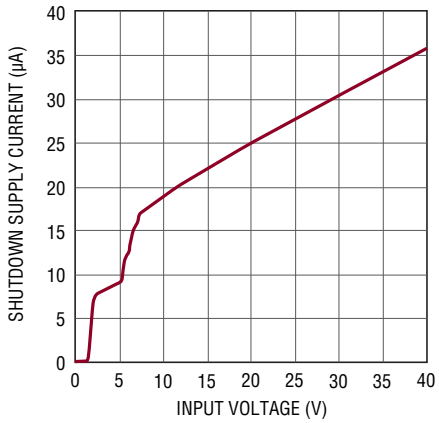
3851A G23

Undervoltage Lockout Threshold ($INTV_{CC}$) vs Temperature



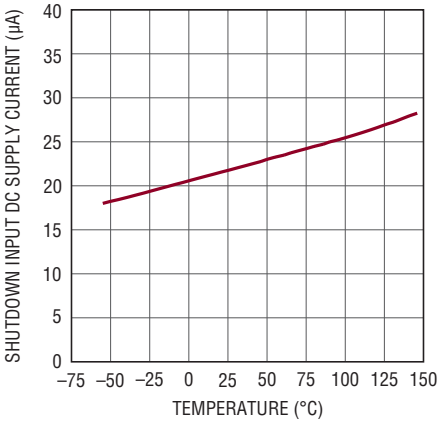
3851A G24

Shutdown Input DC Supply Current vs Input Voltage



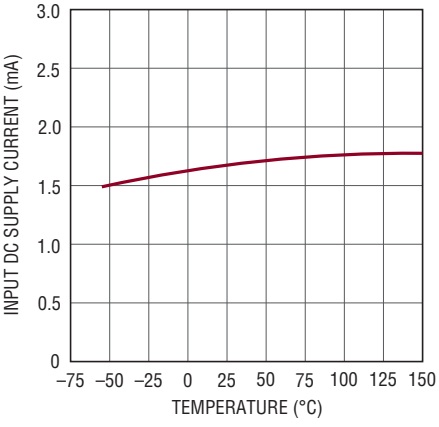
3851A G25

Shutdown Input DC Supply Current vs Temperature



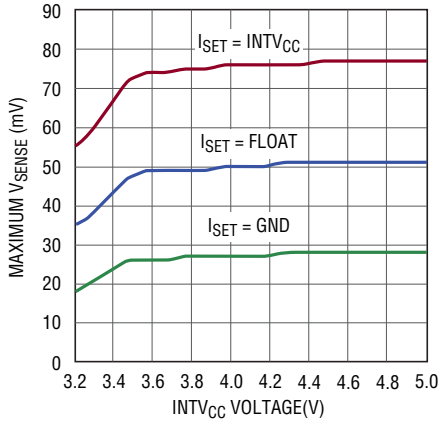
3851A G26

Input DC Supply Current vs Temperature



3851A G27

Maximum Current Sense Threshold vs $INTV_{CC}$ Voltage



3851A G28

PIN FUNCTIONS (GN and MSE/UD)

MODE/PLLIN (Pin 1/Pin 15): Forced Continuous Mode, Burst Mode or Pulse-Skipping Mode Selection Pin and External Synchronization Input to Phase Detector Pin. Connect this pin to $INTV_{CC}$ to force continuous conduction mode of operation. Connect to GND to enable pulse-skipping mode of operation. To select Burst Mode operation, tie this pin to $INTV_{CC}$ through a resistor no less than 50k, but no greater than 250k. A clock on the pin will cause the controller to operate in forced continuous mode of operation and synchronize the internal oscillator.

FREQ/PLLFLTR (Pin 2/Pin 16): The phase-locked loop's lowpass filter is tied to this pin. Alternatively, a resistor can be connected between this pin and GND to vary the frequency of the internal oscillator.

RUN (Pin 3/Pin 1): Run Control Input. A voltage above 1.22V on this pin turns on the IC. However, forcing this pin below 1.1V causes the IC to shut down the IC. There is a 2µA pull-up current on this pin.

TK/SS (Pin 4/Pin 2): Output Voltage Tracking and Soft-Start Input. A capacitor to ground at this pin sets the ramp rate for the output voltage. An internal soft-start current of of 1µA charges this capacitor.

I_{TH} (Pin 5/Pin 3): Current Control Threshold and Error Amplifier Compensation Point. The current comparator tripping threshold increases with its I_{TH} control voltage.

FB (Pin 6/Pin 4): Error Amplifier Feedback Input. This pin receives the remotely sensed feedback voltage from an external resistive divider across the output.

$SENSE^-$ (Pin 7/Pin 5): Current Sense Comparator Inverting Input. The (–) input to the current comparator is connected to the output.

$SENSE^+$ (Pin 8/Pin 6): Current Sense Comparator Noninverting Input. The (+) input to the current comparator is normally connected to the DCR sensing network or current sensing resistor.

I_{LIM} (Pin 9/Pin 7): Current Comparator Sense Voltage Range Input. Tying this pin to GND, FLOAT or $INTV_{CC}$ selects the maximum current sense threshold from three different levels.

GND (Pin 10/Pin 8, Exposed Pad Pin 17): Ground. All small-signal components and compensation components should be Kelvin connected to this ground. The (–) terminal of CV_{CC} and the (–) terminal of C_{IN} should be closely connected to this pin. The exposed pad should be soldered to ground for good thermal conductivity.

BG (Pin 11/Pin 9): Bottom Gate Driver Output. This pin drives the gate of the bottom N-channel MOSFET between GND and $INTV_{CC}$.

$INTV_{CC}$ (Pin 12/Pin 10): Internal 5V Regulator Output. The control circuit is powered from this voltage. Decouple this pin to GND with a minimum 2.2µF low ESR tantalum or ceramic capacitor.

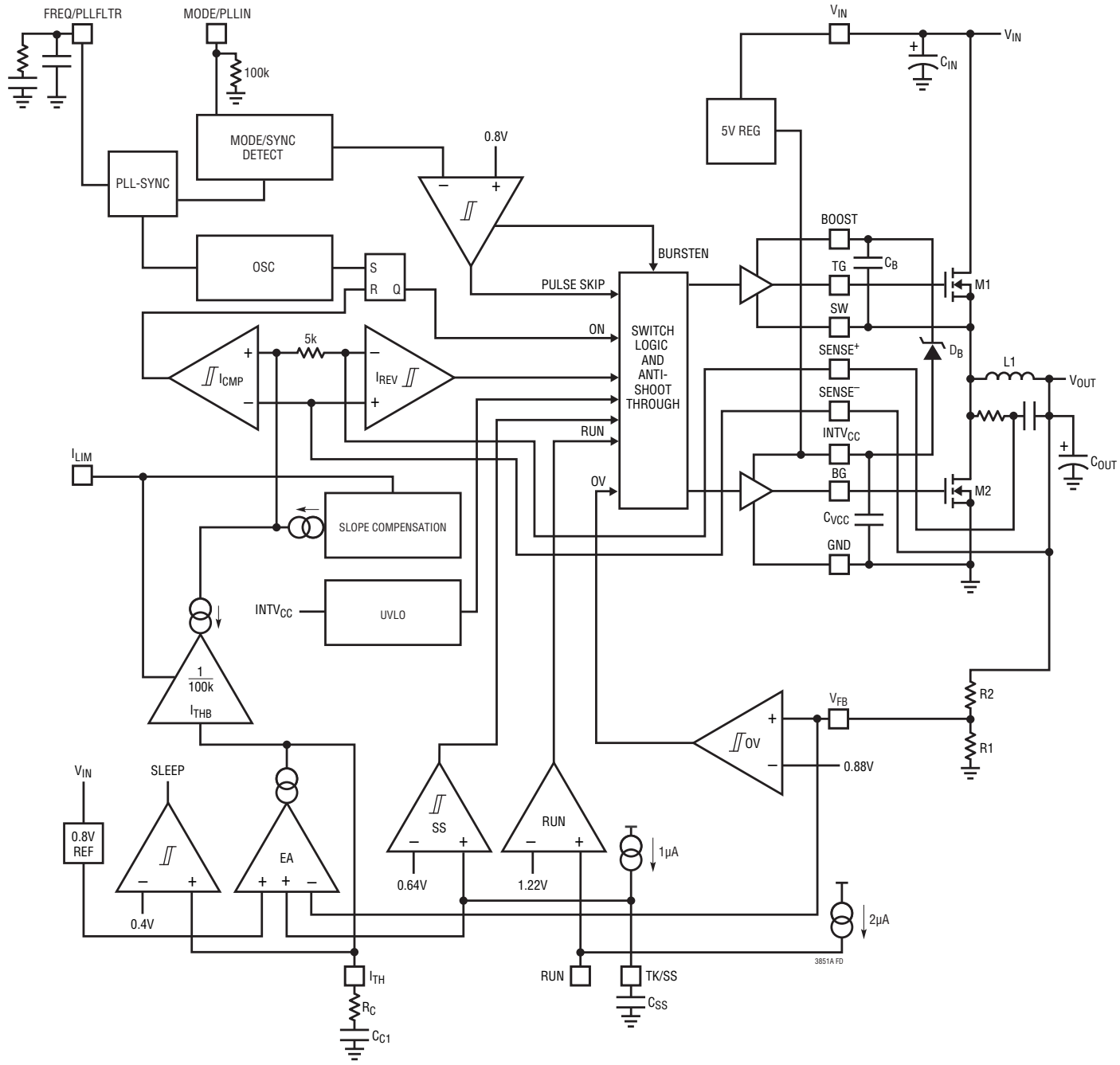
V_{IN} (Pin 13/Pin 11): Main Input Supply. Decouple this pin to GND with a capacitor.

BOOST (Pin 14/Pin 12): Boosted Floating Driver Supply. The (+) terminal of the boost-strap capacitor is connected to this pin. This pin swings from a diode voltage drop below $INTV_{CC}$ up to V_{IN} + $INTV_{CC}$.

TG (Pin 15/Pin 13): Top Gate Driver Output. This is the output of a floating driver with a voltage swing equal to $INTV_{CC}$ superimposed on the switch node voltage.

SW (Pin 16/Pin 14): Switch Node Connection to the Inductor. Voltage swing at this pin is from a Schottky diode (external) voltage drop below ground to V_{IN}.

FUNCTIONAL DIAGRAM



OPERATION

Main Control Loop

The LTC3851A is a constant frequency, current mode step-down controller. During normal operation, the top MOSFET is turned on when the clock sets the RS latch, and is turned off when the main current comparator, I_{CMP}, resets the RS latch. The peak inductor current at which I_{CMP} resets the RS latch is controlled by the voltage on the I_{TH} pin, which is the output of the error amplifier, EA. The V_{FB} pin receives the voltage feedback signal, which is compared to the internal reference voltage by the EA. When the load current increases, it causes a slight decrease in V_{FB} relative to the 0.8V reference, which in turn causes the I_{TH} voltage to increase until the average inductor current matches the new load current. After the top MOSFET has turned off, the bottom MOSFET is turned on until either the inductor current starts to reverse, as indicated by the reverse current comparator, I_{REV}, or the beginning of the next cycle.

$INTV_{CC}$ Power

Power for the top and bottom MOSFET drivers and most other internal circuitry is derived from the $INTV_{CC}$ pin. An internal 5V low dropout linear regulator supplies $INTV_{CC}$ power from V_{IN}.

The top MOSFET driver is biased from the floating bootstrap capacitor, C_B, which normally recharges during each off cycle through an external diode when the top MOSFET turns off. If the input voltage, V_{IN}, decreases to a voltage close to V_{OUT}, the loop may enter dropout and attempt to turn on the top MOSFET continuously. The dropout detector detects this and forces the top MOSFET off for about 1/10 of the clock period every tenth cycle to allow C_B to recharge. However, it is recommended that there is always a load present during the drop-out transition to ensure C_B is recharged.

Shutdown and Start-Up (RUN and TK/SS)

The LTC3851A can be shut down using the RUN pin. Pulling this pin below 1.1V disables the controller and most of the internal circuitry, including the $INTV_{CC}$ regulator. Releasing the RUN pin allows an internal 2µA current to pull up the pin and enable that controller. Alternatively, the RUN pin may be externally pulled up or driven directly by logic. Be careful not to exceed the absolute maximum rating of 6V on this pin.

The start-up of the controller's output voltage, V_{OUT}, is controlled by the voltage on the TK/SS pin. When the voltage on the TK/SS pin is less than the 0.8V internal reference, the LTC3851A regulates the V_{FB} voltage to the TK/SS pin voltage instead of the 0.8V reference. This allows the TK/SS pin to be used to program a soft-start by connecting an external capacitor from the TK/SS pin to GND. An internal 1µA pull-up current charges this capacitor creating a voltage ramp on the TK/SS pin. As the TK/SS voltage rises linearly from 0V to 0.8V (and beyond), the output voltage V_{OUT} rises smoothly from zero to its final value. Alternatively, the TK/SS pin can be used to cause the start-up of V_{OUT} to *track* another supply. Typically, this requires connecting to the TK/SS pin an external resistor divider from the other supply to ground (see the Applications Information section). When the RUN pin is pulled low to disable the controller, or when $INTV_{CC}$ drops below its undervoltage lockout threshold of 3.2V, the TK/SS pin is pulled low by an internal MOSFET. When in undervoltage lockout, the controller is disabled and the external MOSFETs are held off.

Light Load Current Operation (Burst Mode Operation, Pulse-Skipping or Continuous Conduction)

The LTC3851A can be enabled to enter high efficiency Burst Mode operation, constant frequency pulse-skipping mode or forced continuous conduction mode. To select forced continuous operation, tie the MODE/PLLIN pin to $INTV_{CC}$. To select pulse-skipping mode of operation, float the MODE/PLLIN pin or tie it to GND. To select Burst Mode operation, tie MODE/PLLIN to $INTV_{CC}$ through a resistor no less than 50k, but no greater than 250k.

When the controller is enabled for Burst Mode operation, the peak current in the inductor is set to approximately one-forth of the maximum sense voltage even though the voltage on the I_{TH} pin indicates a lower value. If the average inductor current is higher than the load current,

OPERATION

the error amplifier, EA, will decrease the voltage on the I_{TH} pin. When the I_{TH} voltage drops below 0.4V, the internal sleep signal goes high (enabling *sleep* mode) and both external MOSFETs are turned off.

In sleep mode, the load current is supplied by the output capacitor. As the output voltage decreases, the EA's output begins to rise. When the output voltage drops enough, the sleep signal goes low, and the controller resumes normal operation by turning on the top external MOSFET on the next cycle of the internal oscillator. When a controller is enabled for Burst Mode operation, the inductor current is not allowed to reverse. The reverse current comparator, I_{REV}, turns off the bottom external MOSFET just before the inductor current reaches zero, preventing it from reversing and going negative. Thus, the controller operates in discontinuous operation. In forced continuous operation, the inductor current is allowed to reverse at light loads or under large transient conditions. The peak inductor current is determined by the voltage on the I_{TH} pin, just as in normal operation. In this mode the efficiency at light loads is lower than in Burst Mode operation. However, continuous mode has the advantages of lower output ripple and less interference to audio circuitry.

When the MODE/PLLIN pin is connected to GND, the LTC3851A operates in PWM pulse-skipping mode at light loads. At very light loads the current comparator, I_{CMP}, may remain tripped for several cycles and force the external top MOSFET to stay off for the same number of cycles (i.e., skipping pulses). The inductor current is not allowed to reverse (discontinuous operation). This mode, like forced continuous operation, exhibits low output ripple as well as low audio noise and reduced RF interference as compared to Burst Mode operation. It provides higher low current efficiency than forced continuous mode, but not nearly as high as Burst Mode operation.

Frequency Selection and Phase-Locked Loop (FREQ/PLLFLTR and MODE/PLLIN Pins)

The selection of switching frequency is a trade-off between efficiency and component size. Low frequency operation increases efficiency by reducing MOSFET switching losses, but requires larger inductance and/or capacitance to maintain low output ripple voltage. The switching frequency of the LTC3851A can be selected using the FREQ/PLLFLTR pin. If the MODE/PLLIN pin is not being driven by an external clock source, the FREQ/PLLFLTR pin can be used to program the controller's operating frequency from 250kHz to 750kHz.

A phase-locked loop (PLL) is available on the LTC3851A to synchronize the internal oscillator to an external clock source that is connected to the MODE/PLLIN pin. The controller operates in forced continuous mode of operation when it is synchronized. A series RC should be connected between the FREQ/PLLFLTR pin and GND to serve as the PLL's loop filter. It is suggested that the external clock be applied before enabling the controller unless a second resistor is connected in parallel with the series RC network. The second resistor prevents very low switching frequency operation if the controller is enabled before the clock.

Output Overvoltage Protection

An overvoltage comparator, OV, guards against transient overshoots (>10%) as well as other more serious conditions that may overvoltage the output. In such cases, the top MOSFET is turned off and the bottom MOSFET is turned on until the overvoltage condition is cleared.

APPLICATIONS INFORMATION

The Typical Application on the first page of this data sheet is a basic LTC3851A application circuit. The LTC3851A can be configured to use either DCR (inductor resistance) sensing or low value resistor sensing. The choice of the two current sensing schemes is largely a design trade-off between cost, power consumption and accuracy. DCR sensing is becoming popular because it saves expensive current sensing resistors and is more power efficient, especially in high current applications. However, current sensing resistors provide the most accurate current limits for the controller. Other external component selection is driven by the load requirement, and begins with the selection of R_{SENSE} (if R_{SENSE} is used) and the inductor value. Next, the power MOSFETs and Schottky diodes are selected. Finally, input and output capacitors are selected. The circuit shown on the first page can be configured for operation up to 38V at V_{IN}.

Current Limit Programming

The I_{LIM} pin is a tri-level logic input to set the maximum current limit of the controller. When I_{LIM} is grounded, the maximum current limit threshold of the current comparator is programmed to be 30mV. When I_{LIM} is floated, the maximum current limit threshold is 50mV. When I_{LIM} is tied to $INTV_{CC}$, the maximum current limit threshold is set to 75mV.

SENSE+ and SENSE– Pins

The SENSE+ and SENSE– pins are the inputs to the current comparators. The common mode input voltage range of the current comparators is 0V to 5.5V. Both SENSE pins are high impedance inputs with small base currents of less than 1µA. When the SENSE pins ramp up from 0V to 1.4V, the small base currents flow out of the SENSE pins. When the SENSE pins ramp down from 5V to 1.1V, the small base currents flow into the SENSE pins. The high impedance inputs to the current comparators allow accurate DCR sensing. However, care must be taken not to float these pins during normal operation.

Low Value Resistors Current Sensing

A typical sensing circuit using a discrete resistor is shown in Figure 1. R_{SENSE} is chosen based on the required output current.

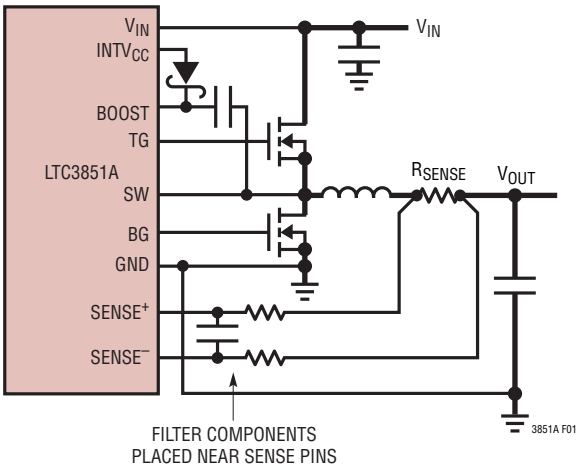


Figure 1. Using a Resistor to Sense Current with the LTC3851A

The current comparator has a maximum threshold, V_{MAX}, determined by the I_{LIM} setting. The current comparator threshold sets the maximum peak of the inductor current, yielding a maximum average output current, I_{MAX}, equal to the maximum peak value less half the peak-to-peak ripple current, ΔI_L. Allowing a margin of 20% for variations in the IC and external component values yields:

$$R_{SENSE} = 0.8 \bullet \frac{V_{MAX}}{I_{MAX} + \Delta I_L/2}$$

Inductor DCR Sensing

For applications requiring the highest possible efficiency, the LTC3851A is capable of sensing the voltage drop across the inductor DCR, as shown in Figure 2. The DCR of the inductor represents the small amount of DC winding resistance of the copper, which can be less than 1mΩ for today's low value, high current inductors. If the external R1||R2 • C1 time constant is chosen to be exactly equal to the L/DCR time constant, the voltage drop across the external capacitor is equal to the voltage drop across the inductor DCR multiplied by R2/(R1 + R2). Therefore, R2 may be used to scale the voltage across the sense terminals when the DCR is greater than the target sense resistance. Check the manufacturer's data sheet for specifications regarding the inductor DCR, in order to properly dimension the external filter components. The DCR of the inductor can also be measured using a good RLC meter.

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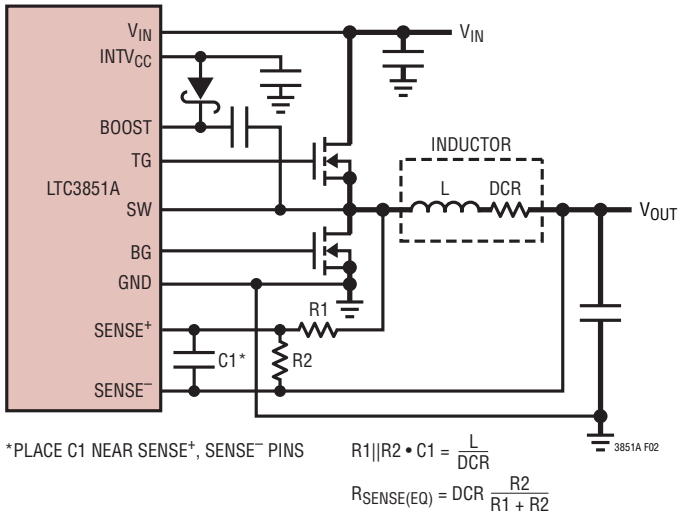


Figure 2. Current Mode Control Using the Inductor DCR

Slope Compensation and Inductor Peak Current

Slope compensation provides stability in constant frequency architectures by preventing sub-harmonic oscillations at high duty cycles. It is accomplished internally by adding a compensating ramp to the inductor current signal. Normally, this results in a reduction of maximum inductor peak current for duty cycles > 40%. However, the LTC3851A uses a novel scheme that allows the maximum inductor peak current to remain unaffected throughout all duty cycles.

Inductor Value Calculation

The operating frequency and inductor selection are interrelated in that higher operating frequencies allow the use of smaller inductor and capacitor values. A higher frequency generally results in lower efficiency because of MOSFET gate charge losses. In addition to this basic trade-off, the effect of inductor value on ripple current and low current operation must also be considered.

The inductor value has a direct effect on ripple current. The inductor ripple current ΔI_L decreases with higher inductance or frequency and increases with higher V_{IN}:

$$\Delta I_L = \frac{1}{f \bullet L} V_{OUT}\left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Accepting larger values of ΔI_L allows the use of low inductances, but results in higher output voltage ripple and greater core losses. A reasonable starting point for setting ripple current is $\Delta I_L = 0.3(I_{MAX})$. The maximum ΔI_L occurs at the maximum input voltage.

The inductor value also has secondary effects. The transition to Burst Mode operation begins when the average inductor current required results in a peak current below ≈10% of the current limit determined by R_{SENSE}. Lower inductor values (higher ΔI_L) will cause this to occur at lower load currents, which can cause a dip in efficiency in the upper range of low current operation. In Burst Mode operation, lower inductance values will cause the burst frequency to increase.

Inductor Core Selection

Once the value for L is known, the type of inductor must be selected. High efficiency converters generally cannot afford the core loss found in low cost powdered iron cores, forcing the use of more expensive ferrite or molypermalloy cores. Actual core loss is independent of core size for a fixed inductor value, but it is very dependent on inductance selected. As inductance increases, core losses go down. Unfortunately, increased inductance requires more turns of wire and therefore copper losses will increase.

Ferrite designs have very low core loss and are preferred at high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates *hard*, which means that inductance collapses abruptly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current and consequent output voltage ripple. Do not allow the core to saturate!

Power MOSFET and Schottky Diode (Optional) Selection

Two external power MOSFETs must be selected for the LTC3851A controller: one N-channel MOSFET for the top (main) switch, and one N-channel MOSFET for the bottom (synchronous) switch.

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The peak-to-peak drive levels are set by the $INTV_{CC}$ voltage. This voltage is typically 5V during start-up. Consequently, logic-level threshold MOSFETs must be used in most applications. The only exception is if low input voltage is expected (V_{IN} < 5V); then, sub-logic level threshold MOSFETs ($V_{GS(TH)}$ < 3V) should be used. Pay close attention to the BV_{DSS} specification for the MOSFETs as well; most of the logic-level MOSFETs are limited to 30V or less.

Selection criteria for the power MOSFETs include the on-resistance, $R_{DS(ON)}$, Miller capacitance, C_{MILLER}, input voltage and maximum output current. Miller capacitance, C_{MILLER}, can be approximated from the gate charge curve usually provided on the MOSFET manufacturers' data sheet. C_{MILLER} is equal to the increase in gate charge along the horizontal axis while the curve is approximately flat divided by the specified change in V_{DS}. This result is then multiplied by the ratio of the application applied V_{DS} to the gate charge curve specified V_{DS}. When the IC is operating in continuous mode, the duty cycles for the top and bottom MOSFETs are given by:

$$\text{Main Switch Duty Cycle} = \frac{V_{OUT}}{V_{IN}}$$

$$\text{Synchronous Switch Duty Cycle} = \frac{V_{IN} - V_{OUT}}{V_{IN}}$$

The MOSFET power dissipations at maximum output current are given by:

$$P_{MAIN} = \frac{V_{OUT}}{V_{IN}}(I_{MAX})^2(1+\delta)R_{DS(ON)} + (V_{IN})^2\left(\frac{I_{MAX}}{2}\right)(R_{DR})(C_{MILLER})\bullet\left[\frac{1}{V_{INTVCC} - V_{TH(MIN)}} + \frac{1}{V_{TH(MIN)}}\right](f)$$

$$P_{SYNC} = \frac{V_{IN} - V_{OUT}}{V_{IN}}(I_{MAX})^2(1+\delta)R_{DS(ON)}$$

where δ is the temperature dependency of $R_{DS(ON)}$ and R_{DR} (approximately 2Ω) is the effective driver resistance at the MOSFET's Miller threshold voltage. $V_{TH(MIN)}$ is the typical MOSFET minimum threshold voltage.

Both MOSFETs have I^2R losses while the topside N-channel equation includes an additional term for transition losses, which are highest at high input voltages. For V_{IN} < 20V, the high current efficiency generally improves with larger MOSFETs, while for V_{IN} > 20V, the transition losses rapidly increase to the point that the use of a higher $R_{DS(ON)}$ device with lower C_{MILLER} actually provides higher efficiency. The synchronous MOSFET losses are greatest at high input voltage when the top switch duty factor is low or during short-circuit when the synchronous switch is on close to 100% of the period.

The term (1 + δ) is generally given for a MOSFET in the form of a normalized $R_{DS(ON)}$ vs Temperature curve, but δ = 0.005/°C can be used as an approximation for low voltage MOSFETs.

The optional Schottky diode conducts during the dead time between the conduction of the two power MOSFETs. This prevents the body diode of the bottom MOSFET from turning on, storing charge during the dead time and requiring a reverse recovery period that could cost as much as 3% in efficiency at high V_{IN}. A 1A to 3A Schottky is generally a good size due to the relatively small average current. Larger diodes result in additional transition losses due to their larger junction capacitance.

Soft-Start and Tracking

The LTC3851A has the ability to either soft-start by itself with a capacitor or track the output of another channel or external supply. When the LTC3851A is configured to soft-start by itself, a capacitor should be connected to the TK/SS pin. The LTC3851A is in the shutdown state if the RUN pin voltage is below 1.10V. TK/SS pin is actively pulled to ground in this shutdown state.

Once the RUN pin voltage is above 1.22V, the LTC3851A powers up. A soft-start current of 1µA then starts to charge its soft-start capacitor. Note that soft-start or tracking is achieved not by limiting the maximum output current of the controller but by controlling the output ramp voltage according to the ramp rate on the TK/SS pin. Current foldback is disabled during this phase to ensure smooth soft-start or tracking. The soft-start or tracking range is

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0V to 0.8V on the TK/SS pin. The total soft-start time can be calculated as:

$$t_{SOFT\text{-}START} = 0.8 \bullet \frac{C_{SS}}{1.0\mu A}$$

Regardless of the mode selected by the MODE/PLLIN pin, the regulator will always start in pulse-skipping mode up to TK/SS = 0.64V. Between TK/SS = 0.64V and 0.72V, it will operate in forced continuous mode and revert to the selected mode once TK/SS > 0.72V. The output ripple is minimized during the 80mV forced continuous mode window.

When the regulator is configured to track another supply, the feedback voltage of the other supply is duplicated by a resistor divider and applied to the TK/SS pin. Therefore, the voltage ramp rate on this pin is determined by the ramp rate of the other supply's voltage. Note that the small soft-start capacitor charging current is always flowing, producing a small offset error. To minimize this error, one can select the tracking resistive divider value to be small enough to make this error negligible.

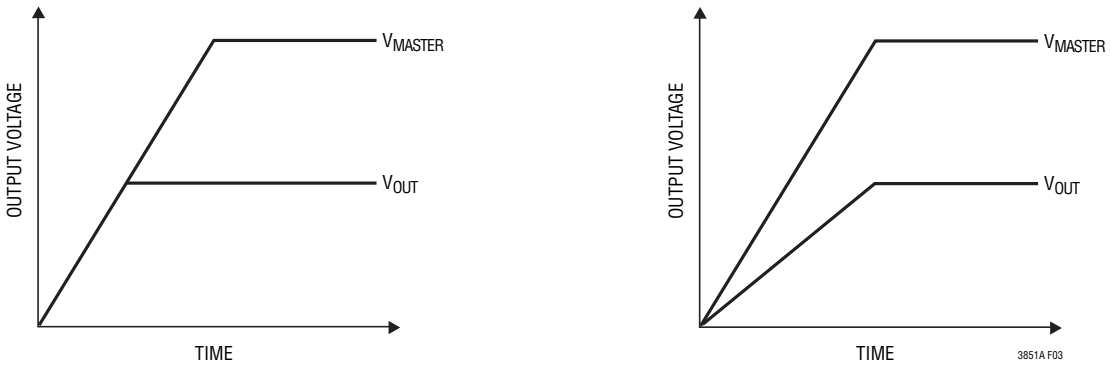
In order to track down another supply after the soft-start phase expires, the LTC3851A must be configured for forced continuous operation by connecting MODE/PLLIN to $INTV_{CC}$.

Output Voltage Tracking

The LTC3851A allows the user to program how its output ramps up and down by means of the TK/SS pins. Through this pin, the output can be set up to either coincidentally or ratiometrically track with another supply's output, as shown in Figure 3. In the following discussions, V_{MASTER} refers to a master supply and V_{OUT} refers to the LTC3851A's output as a slave supply. To implement the coincident tracking in Figure 3a, connect a resistor divider to V_{MASTER} and connect its midpoint to the TK/SS pin of the LTC3851A. The ratio of this divider should be selected the same as that of the LTC3851A's feedback divider as shown in Figure 4a. In this tracking mode, V_{MASTER} must be higher than V_{OUT}. To implement ratiometric tracking, the ratio of the resistor divider connected to V_{MASTER} is determined by:

$$\frac{V_{OUT}}{V_{MASTER}} = \frac{R2}{R4}\left(\frac{R3+R4}{R1+R2}\right)$$

So which mode should be programmed? While either mode in Figure 4 satisfies most practical applications, the coincident mode offers better output regulation. This concept can be better understood with the help of Figure 5. At the input stage of the error amplifier, two common anode diodes are used to clamp the equivalent reference voltage and an additional diode is used to match the shifted common mode voltage. The top two current sources are of the same amplitude. In the coincident

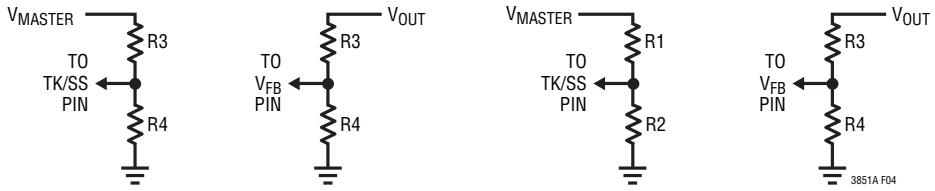


(3a) Coincident Tracking

(3b) Ratiometric Tracking

Figure 3. Two Different Modes of Output Voltage Tracking

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(4a) Coincident Tracking Setup **(4b) Ratiometric Tracking Setup**

Figure 4. Setup for Coincident and Ratiometric Tracking

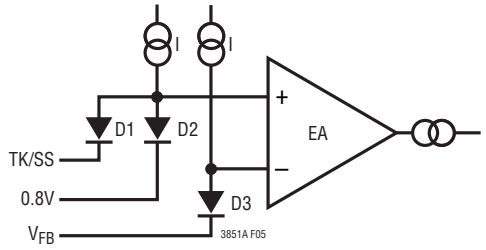


Figure 5. Equivalent Input Circuit of Error Amplifier

mode, the TK/SS voltage is substantially higher than 0.8V at steady state and effectively turns off D1. D2 and D3 will therefore conduct the same current and offer tight matching between V_{FB} and the internal precision 0.8V reference. In the ratiometric mode, however, TK/SS equals 0.8V at steady state. D1 will divert part of the bias current to make V_{FB} slightly lower than 0.8V.

Although this error is minimized by the exponential I-V characteristic of the diode, it does impose a finite amount of output voltage deviation. Furthermore, when the master supply's output experiences dynamic excursion (under load transient, for example), the slave channel output will be affected as well. For better output regulation, use the coincident tracking mode instead of ratiometric.

$INTV_{CC}$ Regulator

The LTC3851A features a PMOS low dropout linear regulator (LDO) that supplies power to $INTV_{CC}$ from the V_{IN} supply. $INTV_{CC}$ powers the gate drivers and much of the LTC3851A's internal circuitry. The LDO regulates the voltage at the $INTV_{CC}$ pin to 5V.

The LDO can supply a peak current of 50mA and must be bypassed to ground with a minimum of 2.2µF ceramic capacitor or low ESR electrolytic capacitor. No matter what type of bulk capacitor is used, an additional 0.1µF ceramic capacitor placed directly adjacent to the $INTV_{CC}$ and GND pins is highly recommended. Good bypassing is needed to supply the high transient currents required by the MOSFET gate drivers.

High input voltage applications in which large MOSFETs are being driven at high frequencies may cause the maximum junction temperature rating for the LTC3851A to be exceeded. The $INTV_{CC}$ current, which is dominated by the gate charge current, is supplied by the 5V LDO.

Power dissipation for the IC in this case is highest and is approximately equal to $V_{IN} \bullet I_{INTVCC}$. The gate charge current is dependent on operating frequency as discussed in the Efficiency Considerations section. The junction temperature can be estimated by using the equations given in Note 3 of the Electrical Characteristics. For example, the LTC3851A $INTV_{CC}$ current is limited to less than 14mA from a 36V supply in the GN package:

$$T_J = 70°C + (14mA)(36V)(110°C/W) = 125°C$$

To prevent the maximum junction temperature from being exceeded, the input supply current must be checked while operating in continuous conduction mode (MODE/PLLIN = $INTV_{CC}$) at maximum V_{IN}.

Topside MOSFET Driver Supply (C_B, D_B)

An external bootstrap capacitor, C_B, connected to the BOOST pin supplies the gate drive voltage for the topside MOSFET. Capacitor C_B in the Functional Diagram is charged though external diode D_B from $INTV_{CC}$ when the SW pin is low. When the topside MOSFET is to be turned on, the driver places the C_B voltage across the gate source of the MOSFET. This enhances the MOSFET and turns on the topside switch. The switch node voltage, SW, rises to V_{IN}

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and the BOOST pin follows. With the topside MOSFET on, the boost voltage is above the input supply:

$$V_{BOOST} = V_{IN} + V_{INTVCC}$$

The value of the boost capacitor C_B needs to be 100 times that of the total input capacitance of the topside MOSFET. The reverse breakdown of the external Schottky diode must be greater than $V_{IN(MAX)}$.

Undervoltage Lockout

The LTC3851A has two functions that help protect the controller in case of undervoltage conditions. A precision UVLO comparator constantly monitors the $INTV_{CC}$ voltage to ensure that an adequate gate-drive voltage is present. It locks out the switching action when $INTV_{CC}$ is below 3.2V. To prevent oscillation when there is a disturbance on the $INTV_{CC}$, the UVLO comparator has 400mV of precision hysteresis.

Another way to detect an undervoltage condition is to monitor the V_{IN} supply. Because the RUN pin has a precision turn-on reference of 1.22V, one can use a resistor divider to V_{IN} to turn on the IC when V_{IN} is high enough.

C_{IN} Selection

In continuous mode, the source current of the top N-channel MOSFET is a square wave of duty cycle V_{OUT}/V_{IN}. To prevent large voltage transients, a low ESR input capacitor sized for the maximum RMS current must be used. The maximum RMS capacitor current is given by:

$$I_{RMS} \cong I_{O(MAX)} \frac{V_{OUT}}{V_{IN}} \left(\frac{V_{IN}}{V_{OUT}} - 1 \right)^{1/2}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{O(MAX)}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that capacitor manufacturers' ripple current ratings are often based on only 2000 hours of life. This makes it advisable to further derate the capacitor or to choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design. Always consult the manufacturer if there is any question.

C_{OUT} Selection

The selection of C_{OUT} is primarily determined by the effective series resistance, ESR, to minimize voltage ripple. The output ripple, ΔV_{OUT}, in continuous mode is determined by:

$$\Delta V_{OUT} \approx \Delta I_L \left(ESR + \frac{1}{8fC_{OUT}} \right)$$

where f = operating frequency, C_{OUT} = output capacitance and ΔI_L = ripple current in the inductor. The output ripple is highest at maximum input voltage since ΔI_L increases with input voltage. Typically, once the ESR requirement for C_{OUT} has been met, the RMS current rating generally far exceeds the $I_{RIPPLE(P-P)}$ requirement. With $\Delta I_L = 0.3 I_{OUT(MAX)}$ and allowing 2/3 of the ripple to be due to ESR, the output ripple will be less than 50mV at maximum V_{IN} if the I_{LIM} pin is configured to float and:

$$C_{OUT} \text{ Required ESR} < 2.2R_{SENSE}$$

$$C_{OUT} > \frac{1}{8fR_{SENSE}}$$

The first condition relates to the ripple current into the ESR of the output capacitance while the second term guarantees that the output capacitance does not significantly discharge during the operating frequency period due to ripple current. The choice of using smaller output capacitance increases the ripple voltage due to the discharging term but can be compensated for by using capacitors of very low ESR to maintain the ripple voltage at or below 50mV. The I_{TH} pin OPTI-LOOP compensation components can be optimized to provide stable, high performance transient response regardless of the output capacitors selected.

The selection of output capacitors for applications with large load current transients is primarily determined by the voltage tolerance specifications of the load. The resistive component of the capacitor, ESR, multiplied by the load current change, plus any output voltage ripple must be within the voltage tolerance of the load.

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The required ESR due to a load current step is:

$$R_{ESR} \leq \frac{\Delta V}{\Delta I}$$

where ΔI is the change in current from full load to zero load (or minimum load) and ΔV is the allowed voltage deviation (not including any droop due to finite capacitance).

The amount of capacitance needed is determined by the maximum energy stored in the inductor. The capacitance must be sufficient to absorb the change in inductor current when a high current to low current transition occurs. The opposite load current transition is generally determined by the control loop OPTI-LOOP components, so make sure not to over compensate and slow down the response. The minimum capacitance to assure the inductors' energy is adequately absorbed is:

$$C_{OUT} > \frac{L(\Delta I)^2}{2(\Delta V)V_{OUT}}$$

where ΔI is the change in load current.

Manufacturers such as Nichicon, United Chemi-Con and Sanyo can be considered for high performance through-hole capacitors. The OS-CON semiconductor electrolyte capacitor available from Sanyo has the lowest (ESR) (size) product of any aluminum electrolytic at a somewhat higher price. An additional ceramic capacitor in parallel with OS-CON capacitors is recommended to reduce the inductance effects.

In surface mount applications, ESR, RMS current handling and load step specifications may require multiple capacitors in parallel. Aluminum electrolytic, dry tantalum and special polymer capacitors are available in surface mount packages. Special polymer surface mount capacitors offer very low ESR but have much lower capacitive density per unit volume than other capacitor types. These capacitors offer a very cost-effective output capacitor solution and are an ideal choice when combined with a controller having high loop bandwidth. Tantalum capacitors offer the highest capacitance density and are often used as output capacitors for switching regulators having controlled soft-start. Several excellent surge-tested choices are the AVX TPS, AVX TPSV or the KEMET T510 series of surface mount tantalums, available in case heights ranging from 1.5mm to 4.1mm. Aluminum electrolytic capacitors can be used in cost-driven applications, provided that consideration is given to ripple current ratings, temperature and long-term reliability. A typical application will require several to many aluminum electrolytic capacitors in parallel. A combination of the above mentioned capacitors will often result in maximizing performance and minimizing overall cost. Other capacitor types include Nichicon PL series, NEC Neocap, Panasonic SP and Sprague 595D series. Consult manufacturers for other specific recommendations.

Like all components, capacitors are not ideal. Each capacitor has its own benefits and limitations. Combinations of different capacitor types have proven to be a very cost effective solution. Remember also to include high frequency decoupling capacitors. They should be placed as close as possible to the power pins of the load. Any inductance present in the circuit board traces negates their usefulness.

Setting Output Voltage

The LTC3851A output voltage is set by an external feedback resistive divider carefully placed across the output, as shown in Figure 6. The regulated output voltage is determined by:

$$\Delta I_{L(SC)} = t_{ON(MIN)} \bullet \frac{V_{IN}}{L}$$

To improve the transient response, a feed-forward capacitor, C_{FF}, may be used. Great care should be taken to route the V_{FB} line away from noise sources, such as the inductor or the SW line.

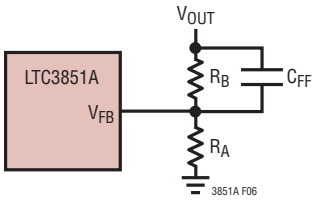


Figure 6. Settling Output Voltage

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Fault Conditions: Current Limit and Current Foldback

The LTC3851A includes current foldback to help limit load current when the output is shorted to ground. If the output falls below 40% of its nominal output level, the maximum sense voltage is progressively lowered from its maximum programmed value to about 25% of the that value. Foldback current limiting is disabled during soft-start or tracking. Under short-circuit conditions with very low duty cycles, the LTC3851A will begin cycle skipping in order to limit the short-circuit current. In this situation the bottom MOSFET will be dissipating most of the power but less than in normal operation. The short-circuit ripple current is determined by the minimum on-time $t_{ON(MIN)}$ of the LTC3851A (≈90ns), the input voltage and inductor value:

$$V_{OUT} = 0.8V\left(1+\frac{R_B}{R_A}\right)$$

The resulting short-circuit current is:

$$I_{SC} = \frac{1/4 Max V_{SENSE}}{R_{SENSE}} - \frac{1}{2}\Delta I_{L(SC)}$$

Programming Switching Frequency

To set the switching frequency of the LTC3851A, connect a resistor, R_{FREQ}, between FREQ/PLLFLTR and GND. The relationship between the oscillator frequency and R_{FREQ} is shown in Figure 7. A 0.1µF bypass capacitor should be connected in parallel with R_{FREQ}.

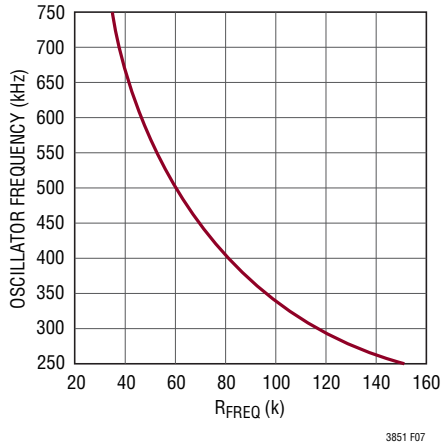


Figure 7. Relationship Between Oscillator Frequency and Resistor Connected Between FREQ/PLLFLTR and GND

Phase-Locked Loop and Frequency Synchronization

The LTC3851A has a phase-locked loop (PLL) comprised of an internal voltage-controlled oscillator (V_{CO}) and a phase detector. This allows the turn-on of the top MOSFET to be locked to the rising edge of an external clock signal applied to the MODE/PLLIN pin. This phase detector is an edge sensitive digital type that provides zero degrees phase shift between the external and internal oscillators. This type of phase detector does not exhibit false lock to harmonics of the external clock.

The output of the phase detector is a pair of complementary current sources that charge or discharge the external filter network connected to the FREQ/PLLFLTR pin. Note that the LTC3851A can only be synchronized to an external clock whose frequency is within range of the LTC3851A's internal V_{CO}. This is guaranteed to be between 250kHz and 750kHz. A simplified block diagram is shown in Figure 8.

If the external clock frequency is greater than the internal oscillator's frequency, f_{OSC}, then current is sunk continuously from the phase detector output, pulling down the FREQ/PLLFLTR pin. When the external clock frequency is less than f_{OSC}, current is sourced continuously, pulling up the FREQ/PLLFLTR pin. If the external and internal frequencies are the same but exhibit a phase difference, the current sources turn on for an amount of time corresponding to the phase difference. The voltage on the FREQ/PLLFLTR pin is adjusted until the phase and frequency of the internal and external oscillators are identical. At the stable operating point, the phase detector output is high impedance and the filter capacitor C_{LP} holds the voltage.

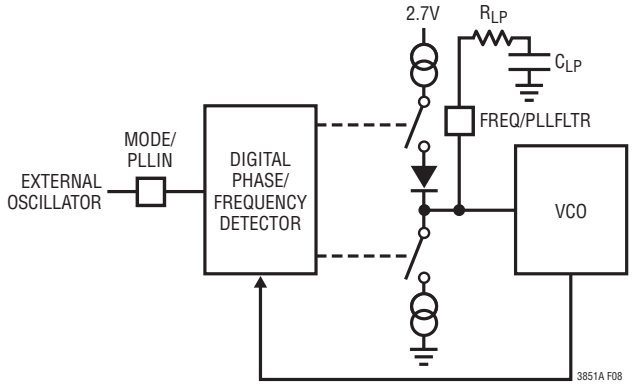


Figure 8. Phase-Locked Loop Block Diagram

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The loop filter components, C_{LP} and R_{LP}, smooth out the current pulses from the phase detector and provide a stable input to the voltage-controlled oscillator. The filter components C_{LP} and R_{LP} determine how fast the loop acquires lock. Typically R_{LP} is 1k to 10k and C_{LP} is 2200pF to 0.01µF.

When the external oscillator is active before the LTC3851A is enabled, the internal oscillator frequency will track the external oscillator frequency as described in the preceding paragraphs. In situations where the LTC3851A is enabled before the external oscillator is active, a low free-running oscillator frequency of approximately 50kHz will result. It is possible to increase the free-running, pre-synchronization frequency by adding a second resistor, R_{FREQ}, in parallel with R_{LP} and C_{LP}. R_{FREQ} will also cause a phase difference between the internal and external oscillator signals. The magnitude of the phase difference is inversely proportional to the value of R_{FREQ}. The free-running frequency may be programmed by using Figure 7 to determine the appropriate value of R_{FREQ}. In order to maintain adequate phase margin for the PLL, the typical value for C_{LP} is 0.01µF and for R_{LP} is 1k.

The external clock (on MODE/PLLIN pin) input high threshold is nominally 1.6V, while the input low threshold is nominally 1.2V.

Minimum On-Time Considerations

Minimum on-time, $t_{ON(MIN)}$, is the smallest time duration that the LTC3851A is capable of turning on the top MOSFET. It is determined by internal timing delays and the gate charge required to turn on the top MOSFET. Low duty cycle applications may approach this minimum on-time limit and care should be taken to ensure that:

$$t_{ON(MIN)} < \frac{V_{OUT}}{V_{IN}(f)}$$

If the duty cycle falls below what can be accommodated by the minimum on-time, the controller will begin to skip cycles. The output voltage will continue to be regulated, but the ripple voltage and current will increase.

The minimum on-time for the LTC3851A is approximately 90ns. However, as the peak sense voltage decreases the minimum on-time gradually increases. This is of particular concern in forced continuous applications with low ripple current at light loads. If the duty cycle drops below the minimum on-time limit in this situation, a significant amount of cycle skipping can occur with correspondingly larger current and voltage ripple.

Efficiency Considerations

The percent efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Percent efficiency can be expressed as:

$$\%Efficiency = 100\% - (L1 + L2 + L3 + ...)$$

where L1, L2, etc. are the individual losses as a percentage of input power.

Although all dissipative elements in the circuit produce losses, four main sources usually account for most of the losses in LTC3851A circuits: 1) IC V_{IN} current, 2) $INTV_{CC}$ regulator current, 3) I^2R losses, 4) topside MOSFET transition losses.

1. The V_{IN} current is the DC supply current given in the Electrical Characteristics table, which excludes MOSFET driver current. V_{IN} current typically results in a small (<0.1%) loss.
2. $INTV_{CC}$ current is the sum of the MOSFET driver and control currents. The MOSFET driver current results from switching the gate capacitance of the power MOSFETs. Each time a MOSFET gate is switched from low to high to low again, a packet of charge dQ moves from $INTV_{CC}$ to ground. The resulting dQ/dt is a current out of $INTV_{CC}$ that is typically much larger than the control circuit current. In continuous mode, $I_{GATECHG} = f(Q_T + Q_B)$, where Q_T and Q_B are the gate charges of the topside and bottom side MOSFETs.

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3. I^2R losses are predicted from the DC resistances of the fuse (if used), MOSFET, inductor and current sense resistor. In continuous mode, the average output current flows through L and R_{SENSE}, but is *chopped* between the topside MOSFET and the synchronous MOSFET. If the two MOSFETs have approximately the same $R_{DS(ON)}$, then the resistance of one MOSFET can simply be summed with the resistances of L and R_{SENSE} to obtain I^2R losses. For example, if each $R_{DS(ON)}$ = 10mΩ, DCR = 10mΩ and R_{SENSE} = 5mΩ, then the total resistance is 25mΩ. This results in losses ranging from 2% to 8% as the output current increases from 3A to 15A for a 5V output, or a 3% to 12% loss for a 3.3V output. Efficiency varies as the inverse square of V_{OUT} for the same external components and output power level. The combined effects of increasingly lower output voltages and higher currents required by high performance digital systems is not doubling but quadrupling the importance of loss terms in the switching regulator system!

4. Transition losses apply only to the topside MOSFET(s), and become significant only when operating at high input voltages (typically 15V or greater). Transition losses can be estimated from:

$$\text{Transition Loss} = (1.7)V_{IN}^2 \bullet I_{O(MAX)} \bullet C_{RSS} \bullet f$$

Other *hidden* losses such as copper trace and the battery internal resistance can account for an additional 5% to 10% efficiency degradation in portable systems. It is very important to include these *system* level losses during the design phase. The internal battery and fuse resistance losses can be minimized by making sure that C_{IN} has adequate charge storage and very low ESR at the switching frequency. A 25W supply will typically require a minimum of 20µF to 40µF of capacitance having a maximum of 20mΩ to 50mΩ of ESR. Other losses including Schottky conduction losses during dead time and inductor core losses generally account for less than 2% total additional loss.

Checking Transient Response

The regulator loop response can be checked by looking at the load current transient response. Switching regulators take several cycles to respond to a step in DC (resistive) load current. When a load step occurs, V_{OUT} shifts by an amount equal to ΔI_{LOAD} (ESR), where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT} generating the feedback error signal that forces the regulator to adapt to the current change and return V_{OUT} to its steady-state value. During this recovery time V_{OUT} can be monitored for excessive overshoot or ringing, which would indicate a stability problem. The availability of the I_{TH} pin not only allows optimization of control loop behavior but also provides a DC coupled and AC filtered closed-loop response test point. The DC step, rise time and settling at this test point truly reflects the closed-loop response. Assuming a predominantly second order system, phase margin and/or damping factor can be estimated using the percentage of overshoot seen at this pin. The bandwidth can also be estimated by examining the rise time at the pin. The I_{TH} external components shown in the Typical Application circuit will provide an adequate starting point for most applications.

The I_{TH} series R_C-C_C filter sets the dominant pole-zero loop compensation. The values can be modified slightly (from 0.5 to 2 times their suggested values) to optimize transient response once the final PC layout is done and the particular output capacitor type and value have been determined. The output capacitors need to be selected because the various types and values determine the loop gain and phase. An output current pulse of 20% to 80% of full-load current having a rise time of 1µs to 10µs will produce output voltage and I_{TH} pin waveforms that will give a sense of the overall loop stability without breaking the feedback loop. Placing a power MOSFET directly across the output capacitor and driving the gate with an appropriate signal generator is a practical way to produce a realistic load step condition. The initial output voltage step resulting from the step change in output current may not be within the bandwidth of the feedback loop, so this signal cannot be used to determine phase margin. This is why it is better to look at the I_{TH} pin signal which is in the feedback loop and is the filtered and compensated control loop response. The midband gain of the loop will be increased by increasing R_C and the bandwidth of the loop will be increased by decreasing C_C. If R_C is increased by the same factor that C_C is decreased, the zero frequency will be kept the same, thereby keeping the phase shift the same in the most critical frequency range of the feedback loop. The output voltage settling behavior is related to the

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stability of the closed-loop system and will demonstrate the actual overall supply performance.

A second, more severe transient is caused by switching in loads with large (>1µF) supply bypass capacitors. The discharged bypass capacitors are effectively put in parallel with C_{OUT}, causing a rapid drop in V_{OUT}. No regulator can alter its delivery of current quickly enough to prevent this sudden step change in output voltage if the load switch resistance is low and it is driven quickly. If the ratio of C_{LOAD} to C_{OUT} is greater than 1:50, the switch rise time should be controlled so that the load rise time is limited to approximately 25 • C_{LOAD}. Thus a 10µF capacitor would require a 250µs rise time, limiting the charging current to about 200mA.

PC Board Layout Checklist

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the LTC3851A. These items are also illustrated graphically in the layout diagram of Figure 9. Check the following in your layout:

1. Are the board signal and power grounds segregated? The LTC3851A GND pin should tie to the ground plane close to the input capacitor(s). The low current or signal ground lines should make a single point tie directly to the GND pin. The synchronous MOSFET source pins should connect to the input capacitor(s) ground.

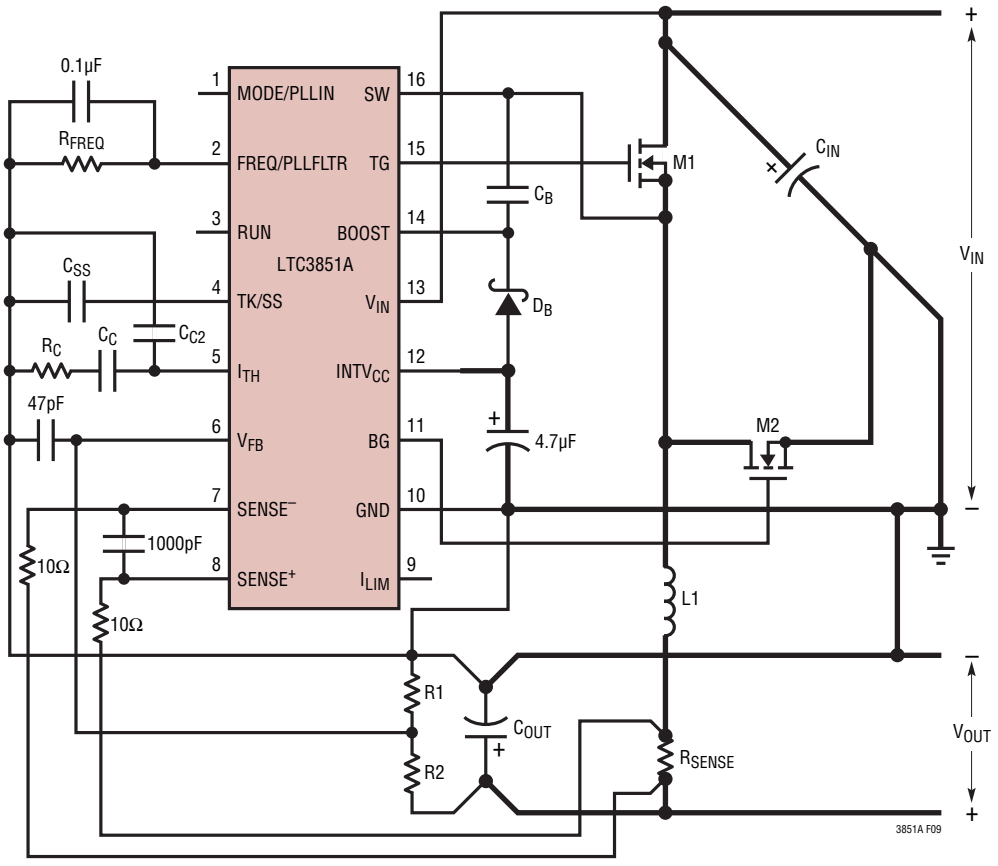


Figure 9. LTC3851A Layout Diagram

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2. Does the V_{FB} pin connect directly to the feedback resistors? The resistive divider R1, R2 must be connected between the (+) plate of C_{OUT} and signal ground. The 47pF to 100pF capacitor should be as close as possible to the LTC3851A. Be careful locating the feedback resistors too far away from the LTC3851A. The V_{FB} line should not be routed close to any other nodes with high slew rates.

3. Are the $SENSE^-$ and $SENSE^+$ leads routed together with minimum PC trace spacing? The filter capacitor between $SENSE^+$ and $SENSE^-$ should be as close as possible to the LTC3851A. Ensure accurate current sensing with Kelvin connections as shown in Figure 10. Series resistance can be added to the SENSE lines to increase noise rejection and to compensate for the ESL of R_{SENSE}.

4. Does the (+) terminal of C_{IN} connect to the drain of the topside MOSFET(s) as closely as possible? This capacitor provides the AC current to the MOSFET(s).

5. Is the $INTV_{CC}$ decoupling capacitor connected closely between $INTV_{CC}$ and GND? This capacitor carries the MOSFET driver peak currents. An additional 1µF ceramic capacitor placed immediately next to the $INTV_{CC}$ and GND pins can help improve noise performance.

6. Keep the switching node (SW), top gate node (TG) and boost node (BOOST) away from sensitive small-signal nodes, especially from the voltage and current sensing feedback pins. All of these nodes have very large and fast moving signals and therefore should be kept on the *output side* (Pin 9 to Pin 16) of the LTC3851AEGN and occupy minimum PC trace area.

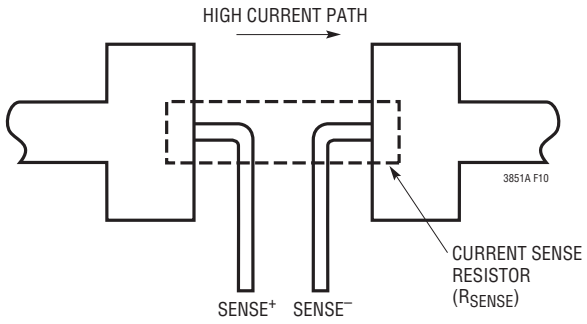


Figure 10. Kelvin Sensing R_{SENSE}

PC Board Layout Debugging

It is helpful to use a DC-50MHz current probe to monitor the current in the inductor while testing the circuit. Monitor the output switching node (SW pin) to synchronize the oscilloscope to the internal oscillator and probe the actual output voltage as well. Check for proper performance over the operating voltage and current range expected in the application. The frequency of operation should be maintained over the input voltage range down to dropout and until the output load drops below the low current operation threshold—typically 10% of the maximum designed current level in Burst Mode operation.

The duty cycle percentage should be maintained from cycle to cycle in a well designed, low noise PCB implementation. Variation in the duty cycle at a subharmonic rate can suggest noise pick-up at the current or voltage sensing inputs or inadequate loop compensation. Overcompensation of the loop can be used to tame a poor PC layout if regulator bandwidth optimization is not required.

Reduce V_{IN} from its nominal level to verify operation of the regulator in dropout. Check the operation of the undervoltage lockout circuit by further lowering V_{IN} while monitoring the outputs to verify operation.

Investigate whether any problems exist only at higher output currents or only at higher input voltages. If problems coincide with high input voltages and low output currents, look for capacitive coupling between the BOOST, SW, TG and possibly BG connections and the sensitive voltage and current pins. The capacitor placed across the current sensing pins needs to be placed immediately adjacent to the pins of the IC. This capacitor helps to minimize the effects of differential noise injection due to high frequency capacitive coupling. If problems are encountered with high current output loading at lower input voltages, look for inductive coupling between C_{IN}, the Schottky and the top MOSFET to the sensitive current and voltage sensing traces. In addition, investigate common ground path voltage pickup between these components and the GND pin of the IC.

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Design Example

As a design example, assume V_{IN} = 12V (nominal), V_{IN} = 22V (maximum), V_{OUT} = 1.8V, I_{MAX} = 5A, and f = 250kHz. Refer to Figure 13.

The inductance value is chosen first based on a 30% ripple current assumption. The highest value of ripple current occurs at the maximum input voltage. Connect a 160k resistor between the FREQ/PLLFLTR and GND pins, generating 250kHz operation. The minimum inductance for 30% ripple current is:

$$\Delta I_L = \frac{1}{(f)(L)} V_{OUT}\left(1-\frac{V_{OUT}}{V_{IN}}\right)$$

A 4.7µH inductor will produce 28% ripple current and a 3.3µH will result in 40%. The peak inductor current will be the maximum DC value plus one-half the ripple current, or 6A, for the 3.3µH value. Increasing the ripple current will also help ensure that the minimum on-time of 90ns is not violated. The minimum on-time occurs at maximum V_{IN}:

$$t_{ON(MIN)} = \frac{V_{OUT}}{V_{IN(MAX)}(f)} = \frac{1.8V}{22V(250kHz)} = 327ns$$

The R_{SENSE} resistor value can be calculated by connecting I_{LIM} to $INTV_{CC}$ and using the maximum current sense voltage specification with some accommodation for tolerances. Tie I_{LIM} to $INTV_{CC}$.

$$R_{SENSE} \le \frac{75mV}{6A} = 0.0125\Omega, \text{ so } 0.01\Omega \text{ is selected}$$

Choosing 1% resistors: R1 = 25.5k and R2 = 32.4k yields an output voltage of 1.816V.

The power dissipation on the topside MOSFET can be easily estimated. Choosing a Fairchild FDS6982S dual MOSFET results in: $R_{DS(ON)}$ = 0.035Ω/0.022Ω, C_{MILLER} = 215pF. At maximum input voltage with T (estimated) = 50°C:

$$P_{MAIN} = \frac{1.8V}{22V}(5)^2\left[1+(0.005)(50°C-25°C)\right]\bullet$$
$$(0.035\Omega)+(22V)^2\left(\frac{5A}{2}\right)(2\Omega)(215pF)\bullet$$
$$\left[\frac{1}{5-2.3}+\frac{1}{2.3}\right](250kHz) = 185mW$$

A short circuit to ground will result in a folded back current of:

$$I_{SC} = \frac{29mV}{0.0125\Omega} - \frac{1}{2}\left(\frac{90ns(22V)}{3.3\mu H}\right) = 2.02A$$

with a typical value of $R_{DS(ON)}$ and δ = (0.005/°C)(25°C) = 0.125. The resulting power dissipated in the bottom MOSFET is:

$$P_{SYNC} = \frac{22V}{22V}(2.02A)^2(1.125)(0.022\Omega)$$
$$= 101.0mW$$

which is less than under full-load conditions.

C_{IN} is chosen for an RMS current rating of at least 3A at temperature. C_{OUT} is chosen with an ESR of 0.02Ω for low output ripple. The output ripple in continuous mode will be highest at the maximum input voltage. The output voltage ripple due to ESR is approximately:

$V_{ORIPPLE} = R_{ESR}(\Delta I_L) = 0.02\Omega\ (2A) = 40mV_{P-P}$

TYPICAL APPLICATIONS

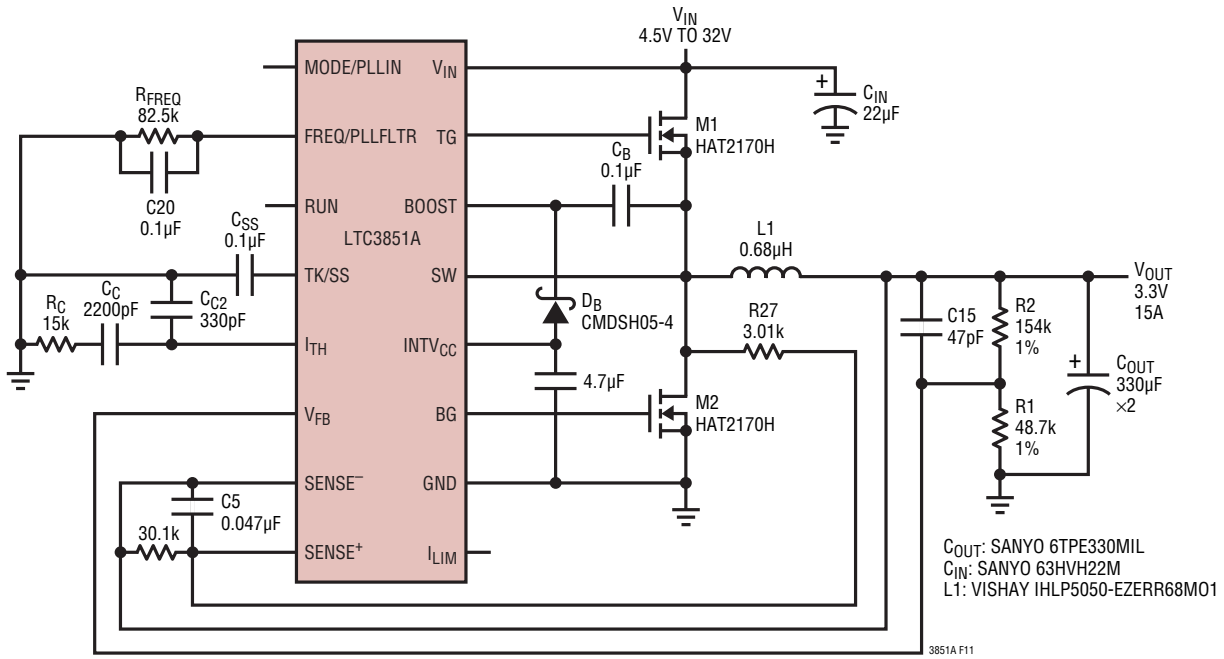


Figure 11. High Efficiency 3.3V/15A Step-Down Converter

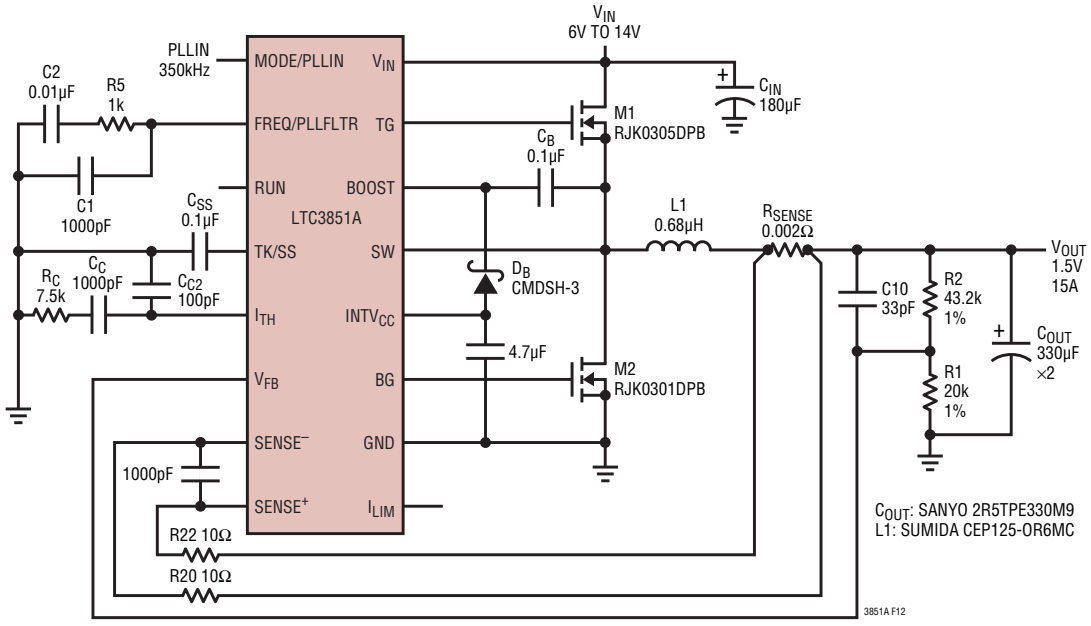
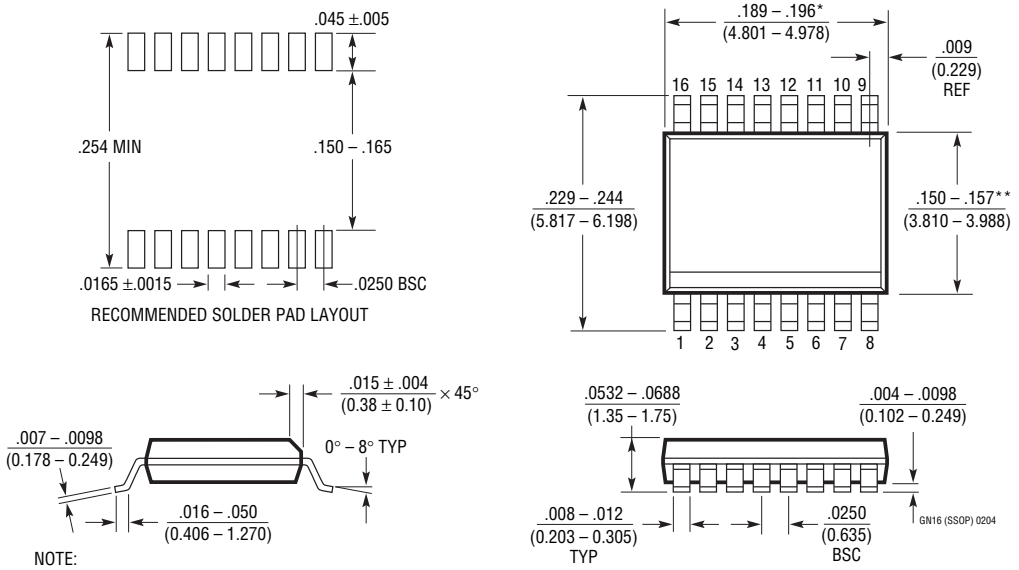


Figure 12. 1.5V/15A Synchronized at 350kHz

PACKAGE DESCRIPTION

GN Package
16-Lead Plastic SSOP (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1641)



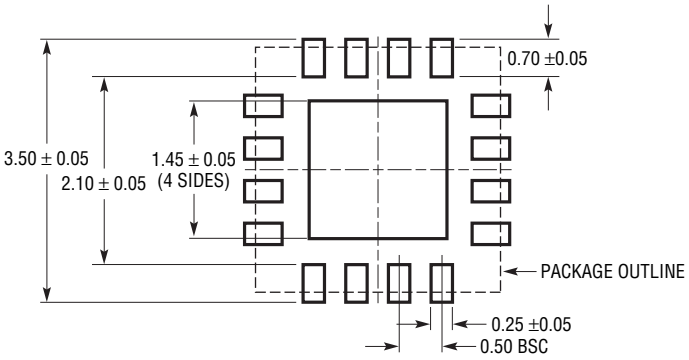
NOTE:
1. CONTROLLING DIMENSION: INCHES
2. DIMENSIONS ARE IN $\frac{\text{INCHES}}{(\text{MILLIMETERS})}$
3. DRAWING NOT TO SCALE

*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

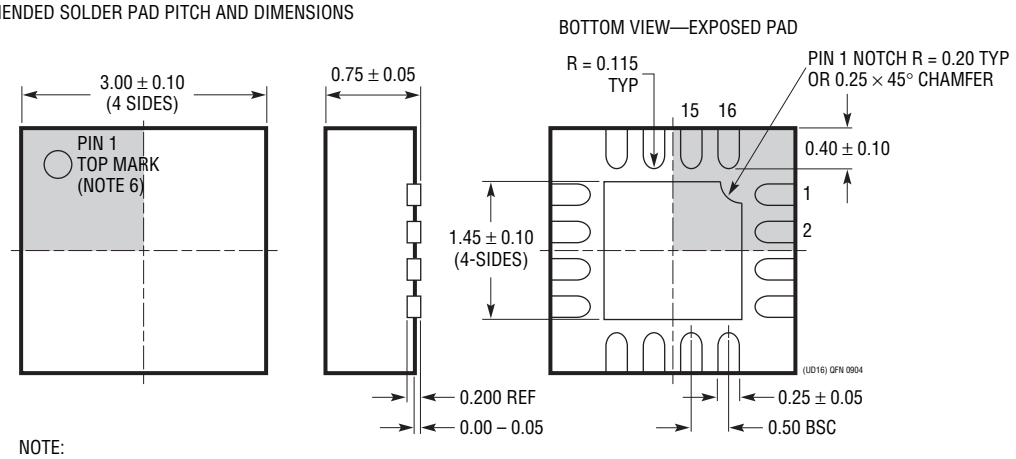
**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

PACKAGE DESCRIPTION

UD Package
16-Lead Plastic QFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1691)



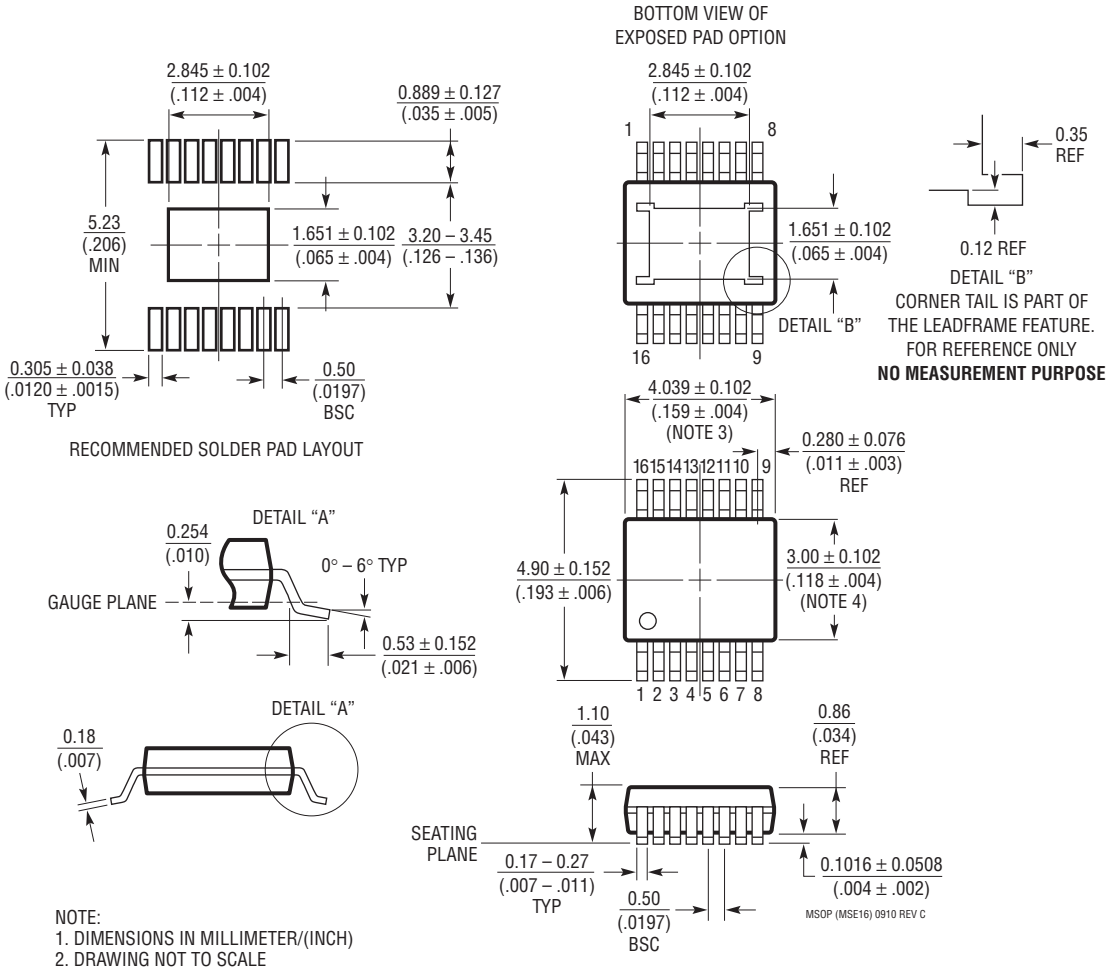
RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



NOTE:
1. DRAWING CONFORMS TO JEDEC PACKAGE OUTLINE MO-220 VARIATION (WEED-2)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

MSE Package
16-Lead Plastic MSOP, Exposed Die Pad
(Reference LTC DWG # 05-08-1667 Rev C)



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	6/11	Added H-Grade and MP-Grade parts. Reflected throughout the data sheet.	1-30

LINEAR TECHNOLOGY

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

TYPICAL APPLICATION

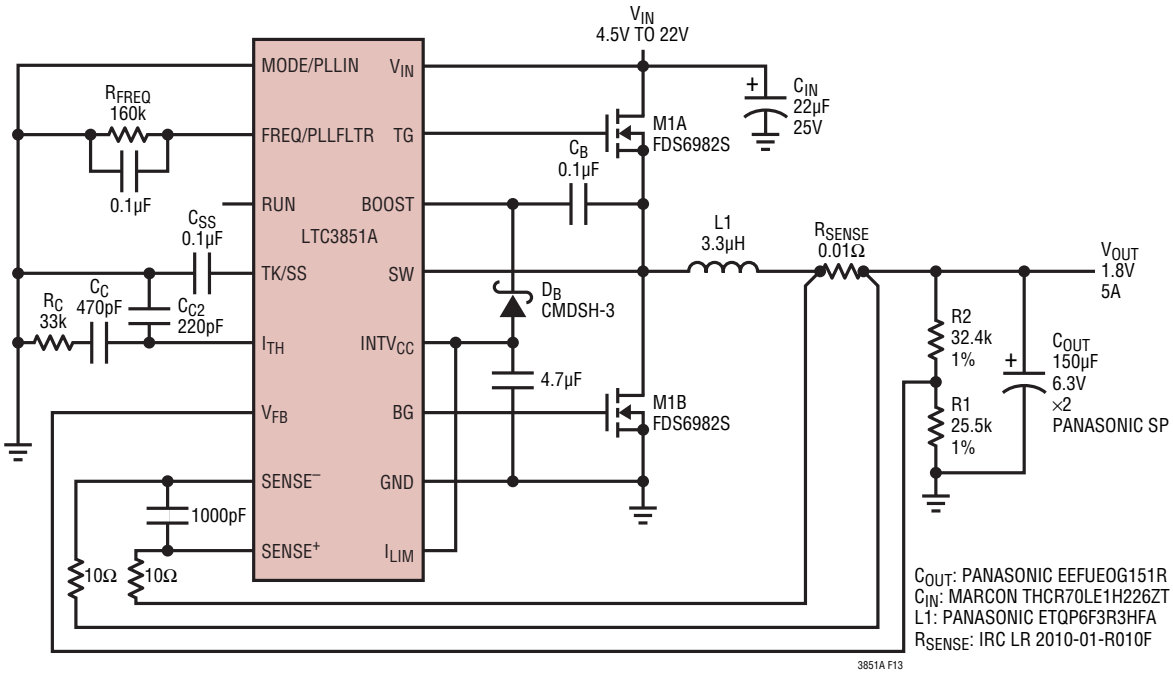


Figure 13. 1.8V/5A Converter from Design Example with Pulse-Skipping Operation

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC3854	Small Footprint Wide V_{IN} Range Synchronous Step-Down DC/DC Controller	Fixed 400kHz Operating Frequency, 4.5V≤ V_{IN} ≤ 38V, 0.8V ≤ V_{OUT} ≤ 5.25V, 2mm × 3mm QFN-12
LTC3878	No R_{SENSE}™ Constant On-Time Synchronous Step-Down DC/DC Controller	Very Fast Transient Response, $t_{ON(MIN)}$ = 43ns, 4V≤ V_{IN} ≤ 38V, 0.8V ≤ V_{OUT} ≤ 0.9V_{IN}, SSOP-16
LTC3879	No R_{SENSE} Constant On-Time Synchronous Step-Down DC/DC Controller	Very Fast Transient Response, $t_{ON(MIN)}$ = 43ns, 4V≤ V_{IN} ≤ 38V, 0.6V ≤ V_{OUT} ≤ 0.9V_{IN}, MSOP-16E, 3mm × 3mm QFN-16
LTC3850/LTC3850-1 LTC3850-2	Dual 2-Phase, High Efficiency Synchronous Step-Down DC/DC Controllers, R_{SENSE} or DCR Current Sensing and Tracking	Phase-Lockable Fixed Operating Frequency 250kHz to 780kHz, 4V≤ V_{IN} ≤ 30V, 0.8V ≤ V_{OUT} ≤ 5.25V
LTC3853	Triple Output, Multiphase Synchronous Step-Down DC/DC Controller, R_{SENSE} or DCR Current Sensing and Tracking	Phase-Lockable Fixed Operating Frequency 250kHz to 750kHz, 4V≤ V_{IN} ≤ 24V, V_{OUT} Up to 13.5V
LTC3610	12A, 1MHz, Monolithic Synchronous Step-Down DC/DC Converter	High Efficiency, Adjustable Constant On-Time, 4V≤ V_{IN} ≤ 24V, $V_{OUT(MIN)}$ = 0.6V, 9mm × 9mm QFN-64
LTC3611	10A, 1MHz, Monolithic Synchronous Step-Down DC/DC Converter	High Efficiency, Adjustable Constant On-Time, 4V≤ V_{IN} ≤ 32V, $V_{OUT(MIN)}$ = 0.6V, 9mm × 9mm QFN-64
LTC3775	High Frequency Synchronous Voltage Mode Step-Down DC/DC Controller	Synchronizable Fixed Frequency 250kHz to 1MHz, $t_{ON(MIN)}$ = 30ns, 4V ≤ V_{IN} ≤ 38V, 0.6V ≤ V_{OUT} ≤ 0.8V_{IN}, MSOP-16E, 3mm × 3mm QFN-16

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