Dual 2-Phase, No R_{SENSE}™ Low V_{IN} Synchronous Controller

FEATURES

- **No Current Sense Resistors Required**
- **Out-of-Phase Controllers Reduce Required Input Capacitance**
- **All N-Channel Synchronous Drive**
- V_{IN} Range: 2.75V to 4.5V
- Constant-Frequency Current Mode Operation
- 0.6V ±1.5% Voltage Reference
- Low Dropout Operation: 97% Duty Cycle
- True PLL for Frequency Locking or Adjustment
- Selectable Pulse-Skipping/Continuous Operation
- Tracking Function
- Internal Soft-Start Circuitry
- Power Good Output Voltage Monitor
- Output Overvoltage Protection
- Micropower Shutdown: I_Q = 6.5µA
- Tiny Low Profile (4mm × 5mm) QFN and Narrow SSOP Packages

APPLICATIONS

- General Purpose 3.3V to 1.X Supplies
- Single Lithium-Ion Powered Devices
- Distributed DC Power Systems

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DESCRIPTION

The LTC®3836 is a 2-phase dual output synchronous step-down switching regulator controller with tracking that drives external N-channel power MOSFETs using few external components. The constant-frequency current mode architecture with MOSFET V_{DS} sensing eliminates the need for sense resistors and improves efficiency. The power loss and noise due to the ESR of the input capacitance are minimized by operating the two controllers out-of-phase. Pulse-skipping operation provides high efficiency at light loads. The 97% duty cycle capability provides low dropout operation, extending operating time in battery-powered systems.

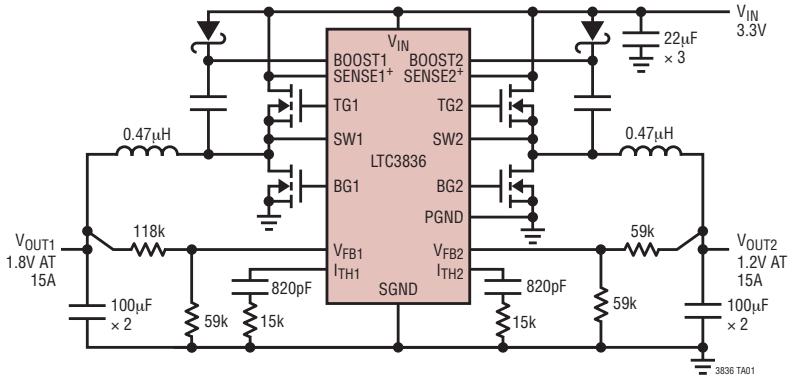
The operating frequency is selectable from 300kHz to 750kHz, allowing the use of small surface mount inductors and capacitors. For noise sensitive applications, the LTC3836 operating frequency can be externally synchronized from 250kHz to 850kHz.

The LTC3836 features an internal 1ms soft-start that can be extended with an external capacitor. A tracking input allows the second output to track the first during start-up.

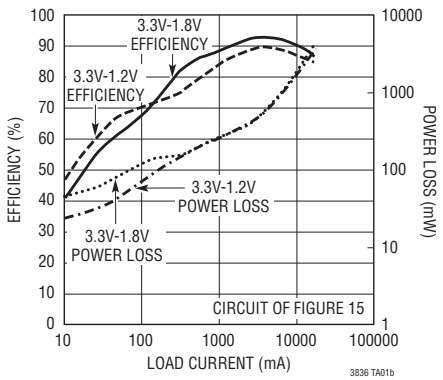
The LTC3836 is available in the tiny thermally enhanced (4mm × 5mm) QFN and 28-lead narrow SSOP packages.

TYPICAL APPLICATION

High Efficiency, 2-Phase, Dual Synchronous DC/DC Step-Down Converter



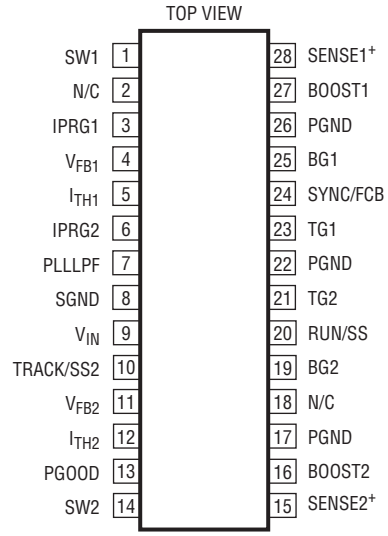
Efficiency/Power Loss vs Load Current



ABSOLUTE MAXIMUM RATINGS (Note 1)

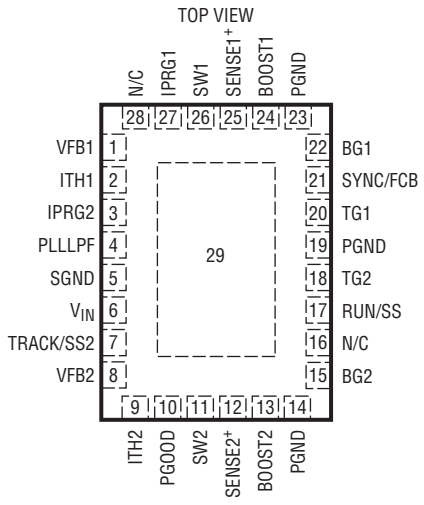
BOOST1, BOOST2 Voltages ..... –0.3V to 10V
Input Supply Voltage (V_{IN}) ..... –0.3V to 4.5V
PLLLPF, RUN/SS, SYNC/FCB,
SENSE1+, SENSE2+,
IPRG1, IPRG2 Voltages.....–0.3V to (V_{IN} + 0.3V)
V_{FB1}, V_{FB2}, I_{TH1}, I_{TH2},
TRACK/SS2 Voltages ..... –0.3V to 2.4V
SW1, SW2 Voltages..... –2V to V_{IN} + 1V
PGOOD..... –0.3V to 10V
Operating Temperature Range (Note 2).... –40°C to 85°C
Storage Temperature Range..... –65°C to 125°C
Junction Temperature (Note 3) ..... 125°C

PIN CONFIGURATION



GN PACKAGE
28-LEAD PLASTIC SSOP

T_{JMAX} = 125°C, θ_{JA} = 90°C/W



UFD PACKAGE
28-LEAD (4mm × 5mm) PLASTIC QFN

T_{JMAX} = 125°C, θ_{JA} = 43°C/W
EXPOSED PAD (PIN 29) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3836EGN#PBF	LTC3836EGN#TRPBF	LTC3836EGN	28-Lead Plastic SSOP	–40°C to 85°C
LTC3836EUFD#PBF	LTC3836EUFD#TRPBF	3836	28-Lead (4mm × 5mm) Plastic QFN	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 3.3V unless otherwise specified.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Main Control Loops						
Input DC Supply Current Normal Mode Shutdown UVLO	(Note 4) RUN/SS = V_{IN} RUN/SS = 0V V_{IN} = UVLO Threshold –200mV			 450 6.5 4	 700 15 10	 µA µA µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 3.3V unless otherwise specified.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Undervoltage Lockout Threshold	V_{IN} Falling V_{IN} Rising	● ●	1.95 2.15	2.25 2.45	2.55 2.75	V V
Shutdown Threshold at RUN/SS			0.45	0.65	0.85	V
Start-Up Current Source	RUN/SS = 0V		0.4	0.65	1	µA
Regulated Feedback Voltage	–40°C to 85°C (Note 5)	●	0.591	0.6	0.609	V
Output Voltage Line Regulation	2.75V < V_{IN} < 4.5V (Note 5)			0.05	0.2	mV/V
Output Voltage Load Regulation	I_{TH} = 0.9V (Note 5) I_{TH} = 1.7V			0.12 –0.12	0.5 –0.5	% %
$V_{FB1,2}$ Input Current	(Note 5)			10	50	nA
TRACK/SS2 Input Current	TRACK/SS2 = 0V		1	1.5	2.2	µA
Overvoltage Protect Threshold	Measured at V_{FB}		0.66	0.68	0.7	V
Overvoltage Protect Hysteresis				20		mV
Auxiliary Feedback Threshold	SYNC/FCB Ramping Positive		0.525	0.6	0.675	V
Top Gate (TG) Drive 1, 2 Rise Time	C_L = 3000pF			40		ns
Top Gate (TG) Drive 1, 2 Fall Time	C_L = 3000pF			40		ns
Bottom Gate (BG) Drive 1, 2 Rise Time	C_L = 3000pF			50		ns
Bottom Gate (BG) Drive 1, 2 Fall Time	C_L = 3000pF			40		ns
Maximum Current Sense Voltage ($\Delta V_{SENSE(MAX)}$) ($SENSE^+$ – SW)	IPRG = Floating IPRG = 0V IPRG = V_{IN}	● ● ●	110 70 185	122 82 202	135 95 220	mV mV mV
Maximum Duty Cycle	In Dropout			97		%
Soft-Start Time	Time for V_{FB1} to Ramp from 0.05V to 0.55V		0.6	0.8	1	ms
Oscillator and Phase-Locked Loop						
Oscillator Frequency	Unsynchronized (SYNC/FCB Not Clocked) PLLLPF = Floating PLLLPF = 0V PLLLPF = V_{IN}		 480 260 650	 550 300 750	 600 340 825	 kHz kHz kHz
Phase-Locked Loop Lock Range	SYNC/FCB Clocked Minimum Synchronizable Frequency Maximum Synchronizable Frequency	 ● ●	 850	 200 1150	 250 	 kHz kHz
Phase Detector Output Current Sinking Sourcing	 $f_{OSC} > f_{SYNC/FCB}$ $f_{OSC} > f_{SYNC/FCB}$			 –4 4		 µA µA
PGOOD Output						
PGOOD Voltage Low	I_{PGOOD} Sinking 1mA			140		mV
PGOOD Trip Level	V_{FB} with Respect to Set Output Voltage V_{FB} < 0.6V, Ramping Positive V_{FB} < 0.6V, Ramping Negative V_{FB} > 0.6V, Ramping Negative V_{FB} > 0.6V, Ramping Positive		 –13 –16 7 10	 –10.0 –13.3 10.0 13.3	 –7 –10 13 16	 % % % %

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC3836 is guaranteed to meet specified performance from 0°C to 85°C. Specifications over the –40°C to 85°C operating range are assured by design, characterization and correlation with statistical process controls.

Note 3: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formula: $T_J = T_A + (P_D \bullet \theta_{JA}°C/W)$

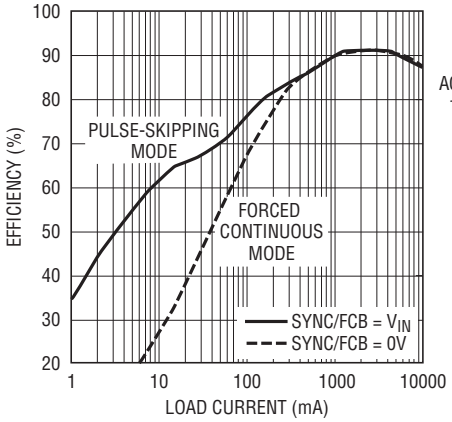
Note 4: Dynamic supply current is higher due to gate charge being delivered at the switching frequency.

Note 5: The LTC3836 is tested in a feedback loop that servos I_{TH} to a specified voltage and measures the resultant V_{FB} voltage.

Note 6: Peak current sense voltage is reduced dependent on duty cycle to a percentage of value as shown in Figure 1.

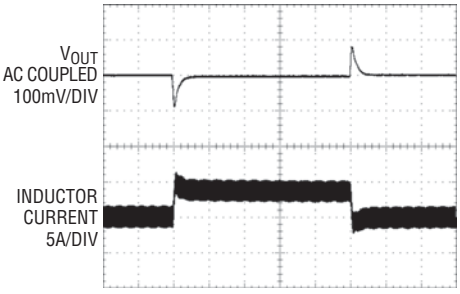
TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C unless otherwise noted.

Efficiency vs Load Current



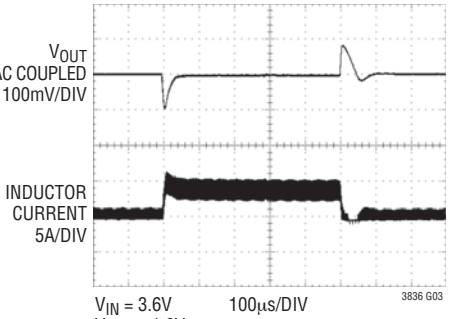
V_{IN} = 3.3V
V_{OUT} = 1.5V
CIRCUIT OF FIGURE 15

Load Step (Forced Continuous Mode)



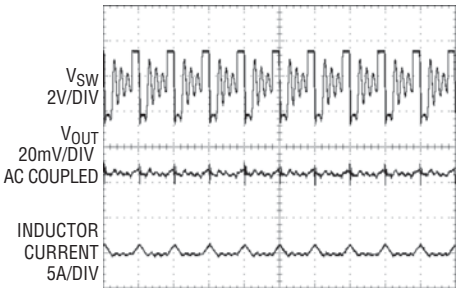
V_{IN} = 3.6V 100µs/DIV
V_{OUT} = 1.8V
CONTINUOUS MODE: 400mA TO 4A
CIRCUIT OF FIGURE 15

Load Step (Pulse-Skipping Mode)



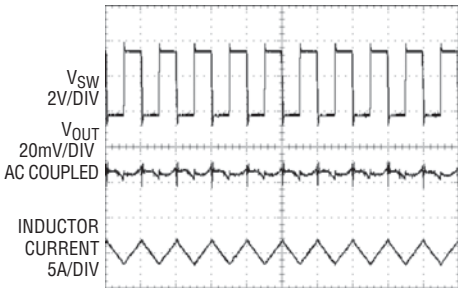
V_{IN} = 3.6V 100µs/DIV
V_{OUT} = 1.8V
PULSE-SKIPPING MODE: 400MA TO 4A
CIRCUIT OF FIGURE 15

Light Load (Pulse-Skipping Mode)



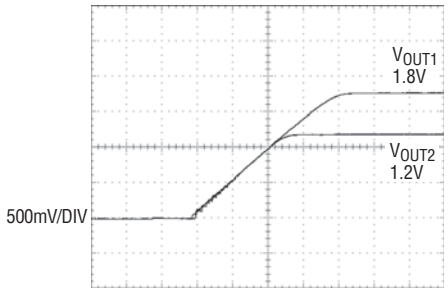
V_{IN} = 3.6V 2µs/DIV
V_{OUT} = 1.8V
I_{LOAD} = 300mA
CIRCUIT OF FIGURE 15

Light Load (Forced Continuous Mode)



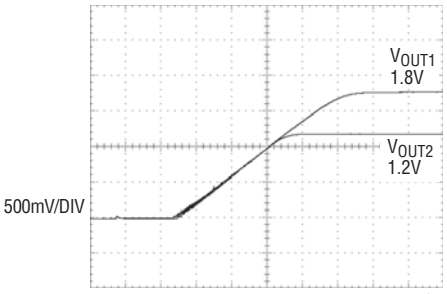
V_{IN} = 3.6V 2µs/DIV
V_{OUT} = 1.8V
I_{LOAD} = 300mA
CIRCUIT OF FIGURE 15

Tracking Start-Up with Internal Soft-Start ($C_{RUN/SS}$ = 0µF)



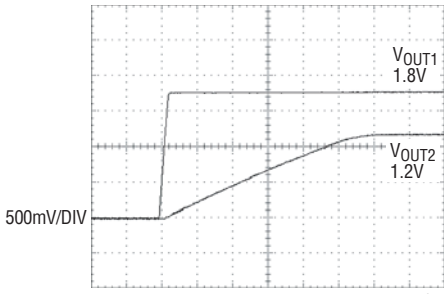
V_{IN} = 3.6V 250µs/DIV
R_{LOAD1} = R_{LOAD2} = 1Ω
CIRCUIT OF FIGURE 15

Tracking Start-Up with External Soft-Start ($C_{RUN/SS}$ = 0.01µF)



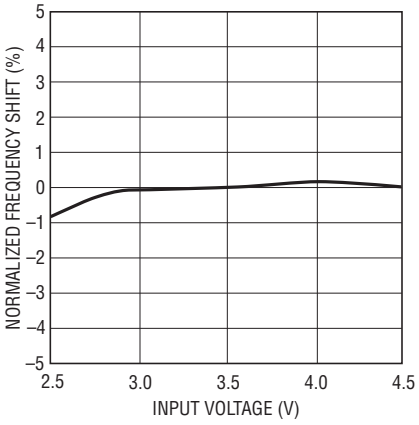
V_{IN} = 3.6V 2.50ms/DIV
R_{LOAD1} = R_{LOAD2} = 1Ω
CIRCUIT OF FIGURE 15

Sequential Start-Up



V_{IN} = 3.3V 4ms/DIV
R_{LOAD1} = R_{LOAD2} = 1Ω
V_{OUT1}: INTERNAL SOFT-START
V_{OUT2}: $C_{TRACK/SS}$ = 0.047µF
CIRCUIT OF FIGURE 15

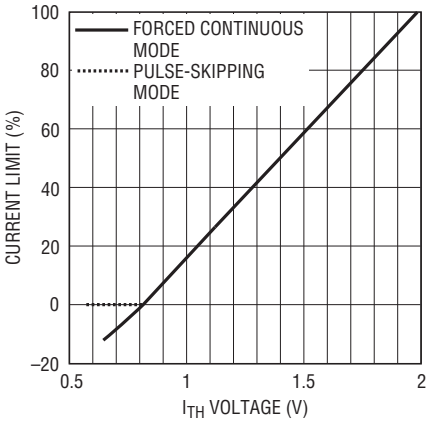
Oscillator Frequency vs Input Voltage



TYPICAL PERFORMANCE CHARACTERISTICS

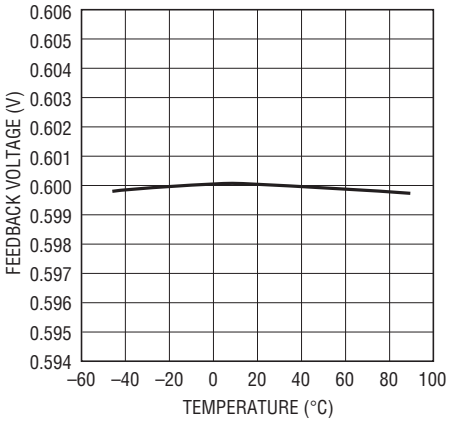
T_A = 25°C unless otherwise noted.

Maximum Current Sense Voltage vs I_{TH} Pin Voltage



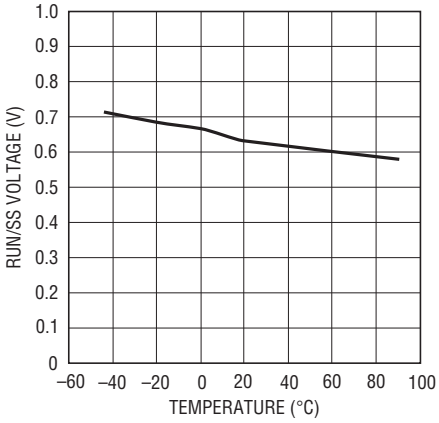
3836 G09

Regulated Feedback Voltage vs Temperature



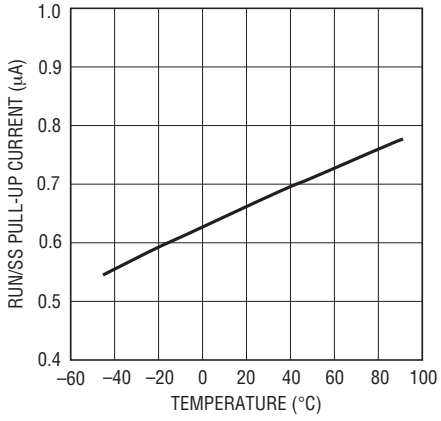
3836 G11

Shutdown (RUN/SS) Threshold vs Temperature



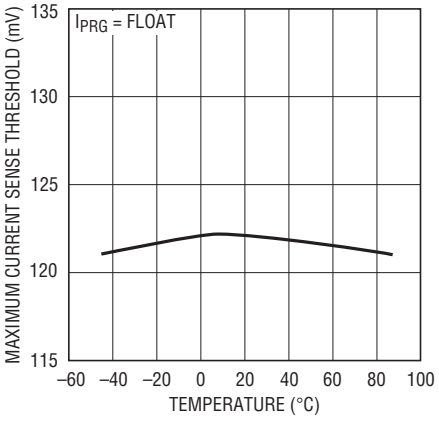
3836 G12

RUN/SS Pull-Up Current vs Temperature



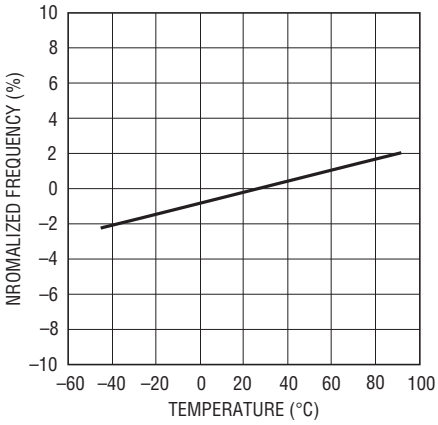
3836 G13

Maximum Current Sense Threshold vs Temperature



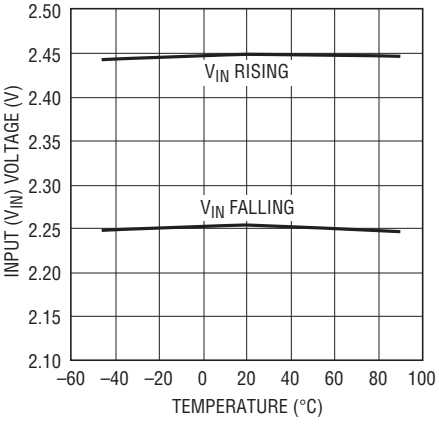
3836 G14

Oscillator Frequency vs Temperature



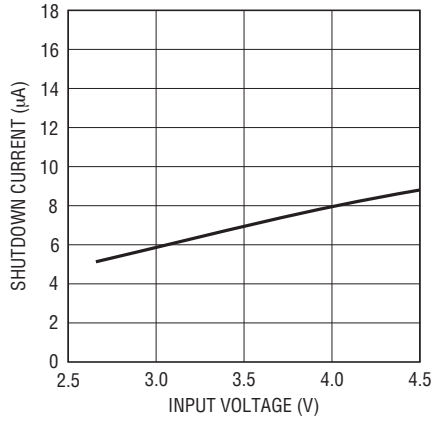
3836 G15

Undervoltage Lockout Threshold vs Temperature



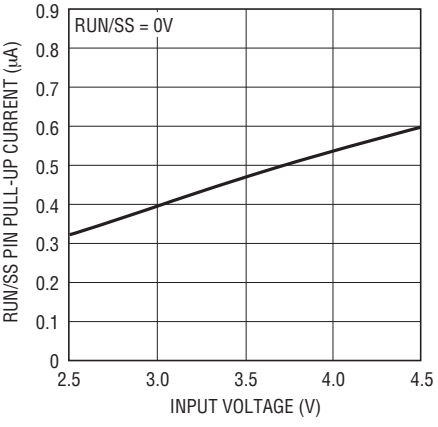
3836 G16

Shutdown Quiescent Current vs Input Voltage



3836 G17

RUN/SS Start-Up Current vs Input Voltage



3836 G18

PIN FUNCTIONS (GN Package)/(UFD Package)

SW1/SW2 (Pins 1, 14)/(Pins 26, 11): Switch Node Connection to Inductor and External MOSFETs. Also the negative input to differential peak current comparator and an input to the reverse current comparator. Normally connected to the source of the main MOSFET, the drain of the synchronous MOSFET, and the inductor.

NC (Pins 2, 18)/(Pins 16, 28): No Connection.

IPRG1/IPRG2 (Pins 3, 6)/(Pins 27, 3): Three-State Pins to Select Maximum Peak Sense Voltage Threshold. These pins select the maximum allowed voltage drop between the SENSE+ and SW pins (i.e., the maximum allowed drop across the external main MOSFET) for each channel. Tie to V_{IN}, GND or float to select 202mV, 82mV, or 122mV respectively.

V_{FB1}/V_{FB2} (Pins 4, 11)/(Pins 1, 8): Feedback Pins. Receives the remotely sensed feedback voltage for its controller from an external resistor divider across the output.

I_{TH1}/I_{TH2} (Pins 5, 12)/(Pins 2, 9): Current Threshold and Error Amplifier Compensation Point. Nominal operating range on these pins is from 0.7V to 2V. The voltage on these pins determines the threshold of the main current comparator.

PLLLPF (Pin 7)/(Pin 4): Frequency Set/PLL Lowpass Filter. When synchronizing to an external clock, this pin serves as the lowpass filter point for the phase-locked loop. Normally a series RC is connected between this pin and ground.

When not synchronizing to an external clock, this pin serves as the frequency select input. Tying this pin to GND selects 300kHz operation; tying this pin to V_{IN} selects 750kHz operation. Floating this pin selects 550kHz operation.

SGND (Pin 8)/(Pin 5): Small-Signal Ground. This pin serves as the ground connection for most internal circuits.

V_{IN} (Pin 9)/(Pin 6): Small-Signal Power Supply. This pin powers the entire chip except for the gate drivers. Externally filtering this pin with a lowpass RC network (e.g., R = 10Ω, C = 1µF) is suggested to minimize noise pickup, especially in high load current applications.

TRACK/SS2 (Pin 10)/(Pin 7): Channel 2 Tracking and Soft-Start Input. The LTC3836 regulates the V_{FB2} voltage to the smaller of 0.6V or the voltage on the TRACK/SS2 pin. An internal 1.5µA pull-up current source is connected to this pin. A capacitor to ground at this pin sets the ramp time to final regulated output voltage. Alternatively, a resistor divider on another voltage supply connected to this pin allows the LTC3836 output to track the other supply during start-up.

PGOOD (Pin 13)/(Pin 10): Power-Good Output Voltage Monitor Open-Drain Logic Output. This pin is pulled to ground when the voltage on either feedback pin (V_{FB1}, V_{FB2}) is not within ±13.3% of its nominal set point.

PGND (Pins 17, 22, 26)/(Pins 14, 19, 23): Power Ground. These pins serve as the ground connection for the gate drivers and the negative input to the reverse current comparators. The Exposed Pad must be soldered to PCB ground.

RUN/SS (Pin 20)/(Pin 17): Run Control Input and Optional External Soft-Start Input. Forcing this pin below 0.65V shuts down the chip (both channels). Driving this pin to V_{IN} or releasing this pin enables the chip, using the chip's internal soft-start. An external soft-start can be programmed by connecting a capacitor between this pin and ground.

TG1/TG2 (Pins 23, 21)/(Pins 20, 18): Top Gate Drive Output. These pins drive the gates of the external topside MOSFETs. These pins have an output swing from PGND to BOOST.

SYNC/FCB (Pin 24)/(Pin 21): This pin performs two functions: 1) external clock synchronization input for phase-locked loop, and 2) pulse-skipping operation or forced continuous mode select. To synchronize with an external clock using the PLL, apply a CMOS compatible clock with a frequency between 250kHz and 850kHz. To select pulse-skipping operation at light loads, tie this pin to V_{IN}. Grounding this pin selects forced continuous operation, which allows the inductor current to reverse. When synchronized to an external clock, pulse-skipping operation is enabled at light loads.

BG1/BG2 (Pins 25, 19)/(Pins 22, 15): Bottom Gate Drive Output. These pins drive the gates of the external synchronous MOSFETs. These pins have an output swing from PGND to BOOST.

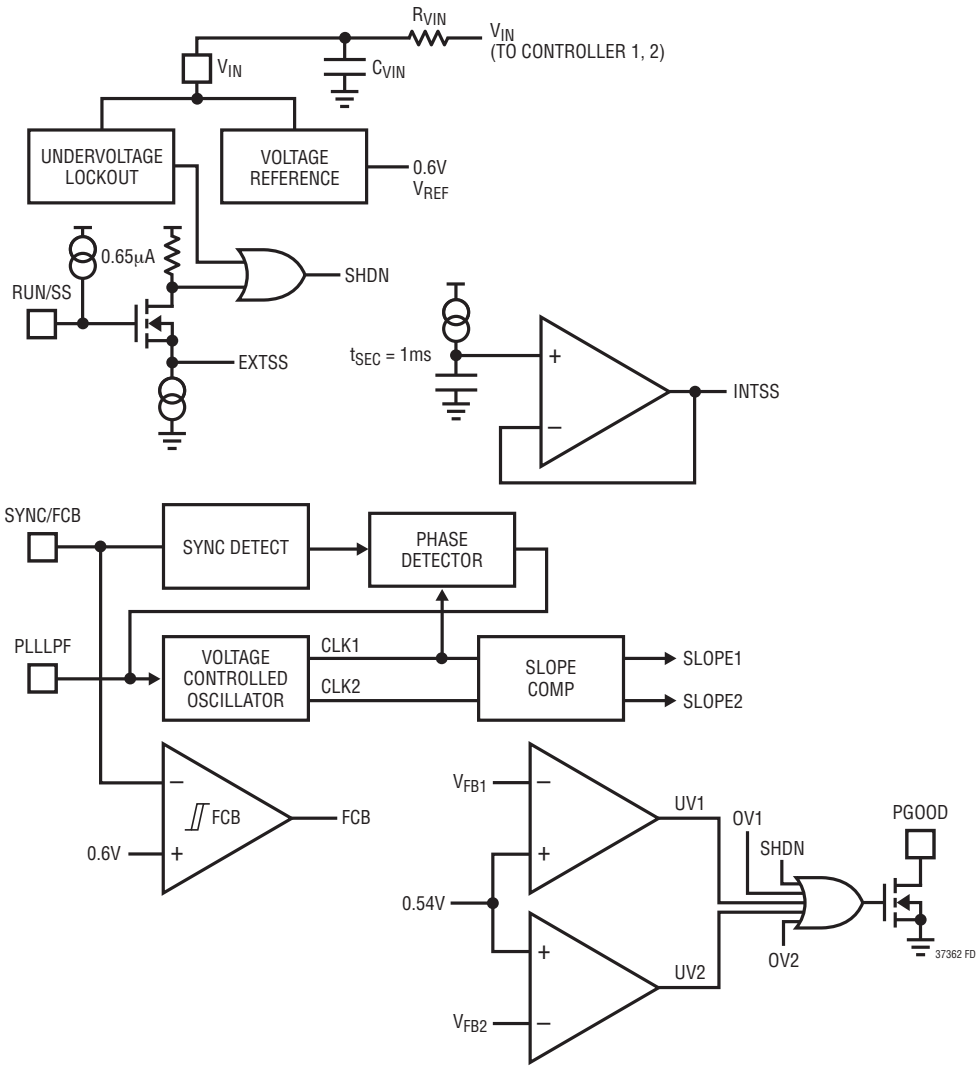
PIN FUNCTIONS (GN/UFD Package)

BOOST1/BOOST2 (Pins 27, 16)/(Pins 24, 13): Positive Supply Pin for the Gate Driver Circuitry. A bootstrapped capacitor, charged with an external Schottky diode and a boost voltage source, is connected between the BOOST and SW pins. Voltage swing at the BOOST pins is from boost source voltage (typically V_{IN}) to this boost source voltage + V_{IN}.

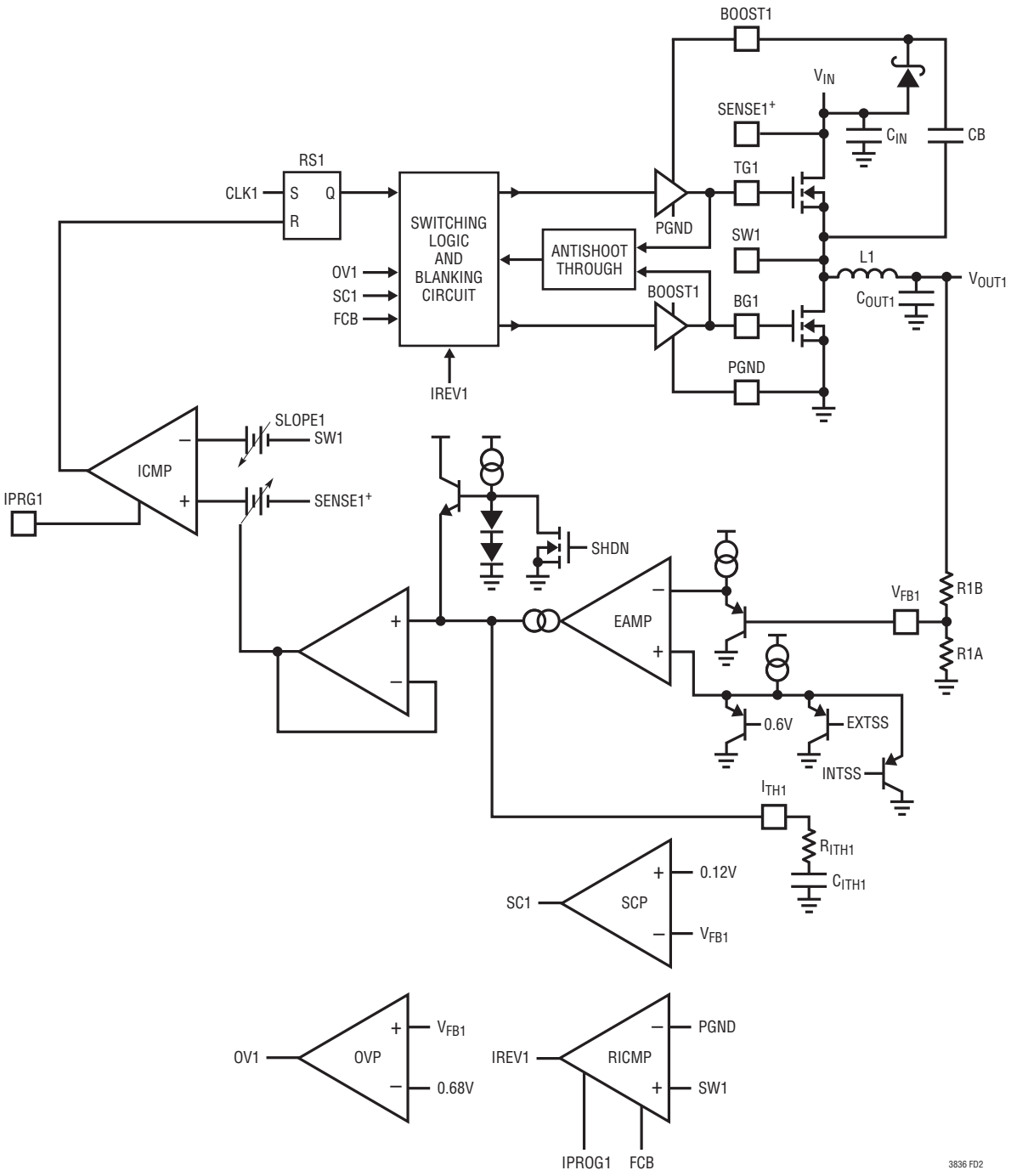
SENSE1+/SENSE2+ (Pins 28, 5)/(Pins 25, 12): Positive Input to Differential Current Comparator. Also powers the gate drivers. Normally connected to the drain of the main external MOSFET.

Exposed Pad (Pin 29) UFD Package Only: Must be soldered to PCB ground.

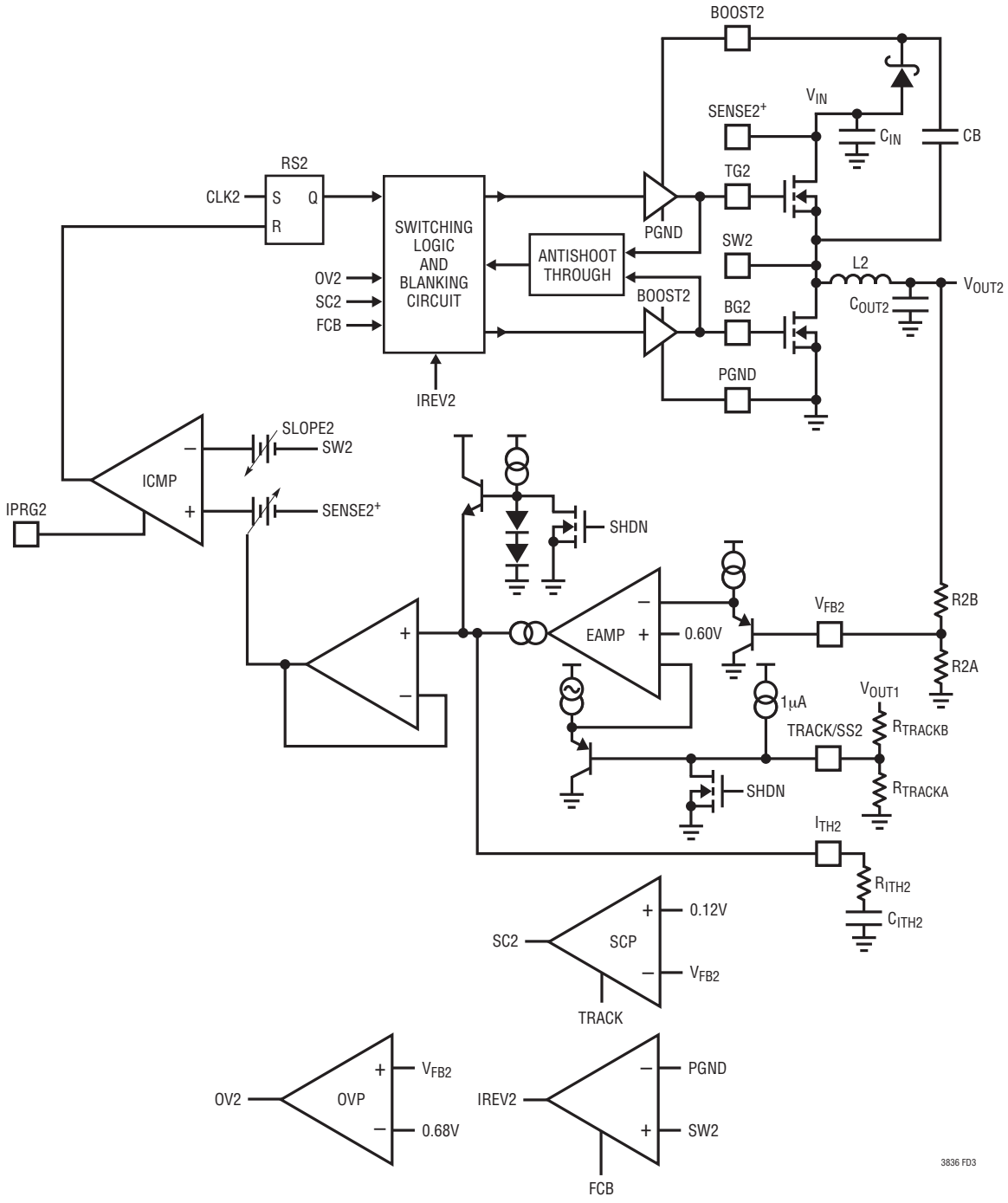
FUNCTIONAL DIAGRAM (Common Circuitry)



FUNCTIONAL DIAGRAM (Controller 1)



FUNCTIONAL DIAGRAM (Controller 2)



OPERATION (Refer to Functional Diagram)

Main Control Loop

The LTC3836 uses a constant-frequency, current mode architecture with the two controllers operating 180 degrees out-of-phase. During normal operation, the top external power MOSFET is turned on when the clock for its channel sets the RS latch, and turned off when the current comparator (I_{CMP}) resets the latch. The peak inductor current at which I_{CMP} resets the RS latch is determined by the voltage on the I_{TH} pin, which is driven by the output of the error amplifier (EAMP). The V_{FB} pin receives the output voltage feedback signal from an external resistor divider. This feedback signal is compared to the internal 0.6V reference voltage by the EAMP. When the load current increases, it causes a slight decrease in V_{FB} relative to the 0.6V reference, which in turn causes the I_{TH} voltage to increase until the average inductor current matches the new load current. While the top N-channel MOSFET is off, the bottom N-channel MOSFET is turned on until either the inductor current starts to reverse, as indicated by the current reversal comparator, I_{RCMP}, or the beginning of the next cycle.

Shutdown, Soft-Start and Tracking Start-Up (RUN/SS and TRACK/SS2 Pins)

The LTC3836 is shut down by pulling the RUN/SS pin low. In shutdown, all controller functions are disabled and the chip draws only 6.5µA. The TG and BG outputs are held low (off) in shutdown. Releasing RUN/SS allows an internal 0.65µA current source to charge up the RUN/SS pin. When the RUN/SS pin reaches 0.65V, the LTC3836's two controllers are enabled.

The start-up of V_{OUT1} is controlled by the LTC3836's internal soft-start. During soft-start, the error amplifier EAMP compares the feedback signal V_{FB1} to the internal soft-start ramp (instead of the 0.6V reference), which rises linearly from 0V to 0.6V in about 1ms. This allows the output voltage to rise smoothly from 0V to its final value, while maintaining control of the inductor current.

The 1ms soft-start time can be increased by connecting the optional external soft-start capacitor C_{SS} between the RUN/SS and SGND pins. As the RUN/SS pin continues to rise linearly from approximately 0.65V to 1.3V (being charged by the internal 0.65µA current source), the EAMP regulates the V_{FB1} proportionally from 0V to 0.6V.

The start-up of V_{OUT2} is controlled by the voltage on the TRACK/SS2 pin. When the voltage on the TRACK/SS2 pin is less than the 0.6V internal reference, the LTC3836 regulates the V_{FB2} voltage to the TRACK/SS2 pin voltage instead of the 0.6V reference. This allows the TRACK/SS2 pin to be used to program a soft-start by connecting an external capacitor from the TRACK/SS2 pin to SGND. An internal 1µA pull-up current charges this capacitor, creating a voltage ramp on the TRACK/SS2 pin. As the TRACK/SS2 voltage rises linearly from 0V to 0.6V (and beyond), the output voltage V_{OUT2} rises smoothly from zero to its final value.

Alternatively, the TRACK/SS2 pin can be used to cause the start-up of V_{OUT2} to "track" that of another supply. Typically, this requires connecting to the TRACK/SS2 pin an external resistor divider from the other supply to ground (see Applications Information section).

When the RUN/SS pin is pulled low to disable the LTC3836, or when V_{IN} drops below its undervoltage lockout threshold, the TRACK/SS2 pin is pulled low by an internal MOSFET. When in undervoltage lockout, both controllers are disabled and the external MOSFETs are held off.

Light Load Operation (Pulse-Skipping or Continuous Conduction) (SYNC/FCB Pin)

The LTC3836 can be enabled to enter high efficiency pulse-skipping operation or forced continuous conduction mode at low load currents. To select pulse-skipping operation, tie the SYNC/FCB pin to a DC voltage above 0.6V (e.g., V_{IN}). To select forced continuous operation, tie the SYNC/FCB to a DC voltage below 0.6V (e.g., SGND).

In forced continuous operation, the inductor current is allowed to reverse at light loads or under large transient conditions. The peak inductor current is determined by the voltage on the I_{TH} pin. The main N-channel MOSFET is turned on every cycle (constant-frequency) regardless of the I_{TH} pin voltage. In this mode, the efficiency at light loads is lower than in pulse-skipping operation. However, continuous mode has the advantages of lower output ripple and less interference with audio circuitry.

OPERATION (Refer to Functional Diagram)

When the SYNC/FCB pin is tied to a DC voltage above 0.6V or when it is clocked by an external clock source to use the phase-locked loop (see Frequency Selection and Phase-Locked Loop), the LTC3836 operates in PWM pulse-skipping mode at light loads. In this mode, the current comparator I_{CMP} may remain tripped for several cycles and force the main N-channel MOSFET to stay off for the same number of cycles. The inductor current is not allowed to reverse, though (discontinuous operation). This mode, like forced continuous operation, exhibits low output ripple as well as low audio noise and reduced RF interference. However, it provides low current efficiency higher than forced continuous mode. During start-up or a short-circuit condition (V_{FB1} or $V_{FB2} \leq 0.54V$), the LTC3836 operates in pulse-skipping mode (no current reversal allowed), regardless of the state of the SYNC/FCB pin.

Short-Circuit Protection

When an output is shorted to ground ($V_{FB} < 0.12V$), the switching frequency of that controller is reduced to one-fifth of the normal operating frequency. The other controller maintains regulation in pulse-skipping mode.

The short-circuit threshold on V_{FB2} is based on the smaller of 0.12V and a fraction of the voltage on the TRACK/SS2 pin. This also allows V_{OUT2} to start up and track V_{OUT1} more easily. Note that if V_{OUT1} is truly short-circuited ($V_{OUT1} = V_{FB1} = 0V$), then the LTC3836 will try to regulate V_{OUT2} to 0V if a resistor divider on V_{OUT1} is connected to the TRACK/SS pin.

Output Overvoltage Protection

As a further protection, the overvoltage comparator (OV) guards against transient overshoots, as well as other more serious conditions that may overvoltage the output. When the feedback voltage on the V_{FB} pin has risen 13.33% above the reference voltage of 0.6V, the main N-channel MOSFET is turned off and the synchronous N-channel MOSFET is turned on until the overvoltage is cleared.

Frequency Selection and Phase-Locked Loop (PLLLPF and SYNC/FCB Pins)

The selection of switching frequency is a tradeoff between efficiency and component size. Low frequency operation increases efficiency by reducing MOSFET switching losses, but requires larger inductance and/or capacitance to maintain low output ripple voltage.

The switching frequency of the LTC3836's controllers can be selected using the PLLLPF pin.

If the SYNC/FCB is not being driven by an external clock source, the PLLLPF can be floated, tied to V_{IN} or tied to SGND to select 550kHz, 750kHz or 300kHz respectively.

A phase-locked loop (PLL) is available on the LTC3836 to synchronize the internal oscillator to an external clock source that is connected to the SYNC/FCB pin. In this case, a series RC should be connected between the PLLLPF pin and SGND to serve as the PLL's loop filter. The LTC3836 phase detector adjusts the voltage on the PLLLPF pin to align the turn-on of controller 1's top MOSFET to the rising edge of the synchronizing signal. Thus, the turn-on of controller 2's top MOSFET is 180 degrees out-of-phase with the rising edge of the external clock source.

The typical capture range of the LTC3836's phase-locked loop is from approximately 200kHz to 1MHz, and is guaranteed over temperature between 250kHz and 850kHz. In other words, the LTC3836's PLL is guaranteed to lock to an external clock source whose frequency is between 250kHz and 850kHz.

Dropout Operation

Each top MOSFET driver is biased from the floating bootstrap capacitor C_B, which normally recharges during each off cycle through an external diode when the top MOSFET turns off. If the input voltage V_{IN} decreases to a voltage close to V_{OUT}, the loop may enter dropout and attempt to turn on the top MOSFET continuously. The dropout detector detects this and forces the top MOSFET off for about 200ns every fourth cycle to allow C_B to recharge.

OPERATION (Refer to Functional Diagram)

Undervoltage Lockout

To prevent operation of the external MOSFETs below safe input voltage levels, an undervoltage lockout is incorporated in the LTC3836. When the input supply voltage (V_{IN}) drops below 2.25V, the external MOSFETs and all internal circuitry are turned off except for the undervoltage block, which draws only a few microamperes.

Peak Current Sense Voltage Selection and Slope Compensation (IPRG1 and IPRG2 Pins)

When a controller is operating below 20% duty cycle, the peak current sense voltage (between the SENSE+ and SW pins) allowed across the main N-channel MOSFET is determined by:

$$\Delta V_{SENSE(MAX)} = \frac{A\left(V_{ITH} - 0.7V\right)}{10}$$

where A is a constant determined by the state of the IPRG pins. Floating the IPRG pin selects A = 1; tying IPRG to V_{IN} selects A = 5/3; tying IPRG to SGND selects A = 2/3. The maximum value of V_{ITH} is typically about 1.98V, so the maximum sense voltage allowed across the main N-channel MOSFET is 122mV, 202mV, or 82mV for the three respective states of the IPRG pin. The peak sense voltages for the two controllers can be independently selected by the IPRG1 and IPRG2 pins.

However, once the controller's duty cycle exceeds 20%, slope compensation begins and effectively reduces the peak sense voltage by a scale factor given by the curve in Figure 1.

The peak inductor current is determined by the peak sense voltage and the on-resistance of the main N-channel MOSFET:

$$I_{PK} = \frac{\Delta V_{SENSE(MAX)}}{R_{DS(ON)}}$$

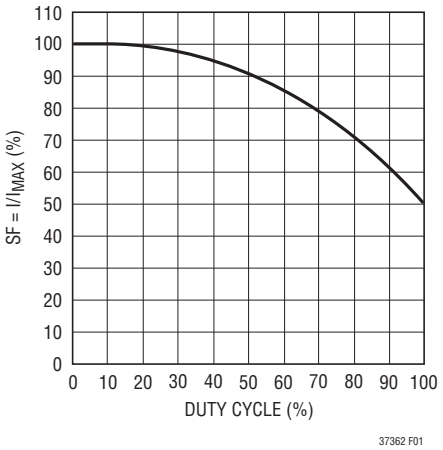


Figure 1. Maximum Peak Current vs Duty Cycle

Power-Good (PGOOD) Pin

A window comparator monitors both feedback voltages and the open-drain PGOOD output pin is pulled low when either or both feedback voltages are not within ±10% of the 0.6V reference voltage. PGOOD is low when the LTC3836 is shut down or in undervoltage lockout.

2-Phase Operation

Why the need for 2-phase operation? Many constant-frequency dual switching regulators operate both controllers in phase (i.e., single phase operation). This means that both topside MOSFETs are turned on at the same time, causing current pulses of up to twice the amplitude of those from a single regulator to be drawn from the input capacitor. These large amplitude pulses increase the total RMS current flowing in the input capacitor, requiring the use of larger and more expensive input capacitors, and increase both EMI and power losses in the input capacitor and input power supply.

With 2-phase operation, the two controllers of the LTC3836 are operated 180 degrees out-of-phase. This effectively interleaves the current pulses coming from the topside MOSFET switches, greatly reducing the time where they overlap and add together. The result is a significant reduction in the total RMS current, which in turn allows the use of smaller, less expensive input capacitors, reduces shielding requirements for EMI and improves real world operating efficiency.

OPERATION (Refer to Functional Diagram)

Figure 2 shows example waveforms for a single phase dual controller versus a 2-phase LTC3836 system. In this case, two outputs of different voltage, each drawing the same load current are derived from a single input supply. In this example, 2-phase operation could halve the RMS input capacitor current. While this is an impressive reduction by itself, remember that power losses are proportional to I_{RMS}^2, meaning that just one-fourth the actual power is wasted.

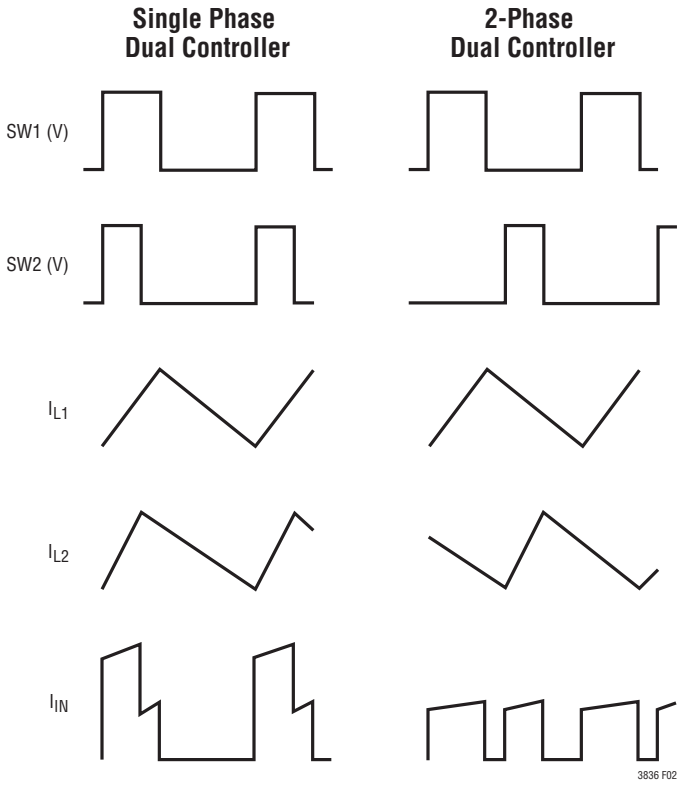


Figure 2. Example Waveforms for a Single Phase Dual Controller vs the 2-Phase LTC3836

The reduced input ripple current also means that less power is lost in the input power path, which could include batteries, switches, trace/connector resistances, and protection circuitry. Improvements in both conducted and radiated EMI also directly accrue as a result of the reduced RMS input current and voltage. Significant cost and board footprint savings are also realized by being able to use smaller, less expensive, lower RMS current-rated input capacitors.

Of course, the improvement afforded by 2-phase operation is a function of the relative duty cycles of the two controllers, which in turn are dependent upon the input supply voltage. Figure 3 depicts how the RMS input current varies for single phase and 2-phase dual controllers with 2.5V and 1.8V outputs. A good rule of thumb for most applications is that 2-phase operation will reduce the input capacitor requirement to that for just one channel operating at maximum current and 50% duty cycle.

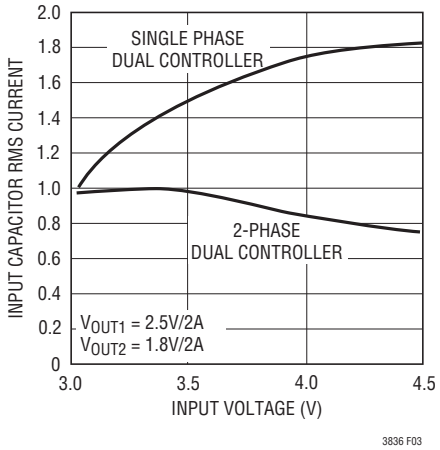


Figure 3. RMS Input Current Comparison

APPLICATIONS INFORMATION

The typical LTC3836 application circuit is shown in Figure 13. External component selection for each of the LTC3836's controllers is driven by the load requirement and begins with the selection of the inductor (L) and the power MOSFETs (M1 to M4).

Power MOSFET Selection

Each of the LTC3836's two controllers requires two external N-channel power MOSFETs for the topside (main) switch and the bottom (synchronous) switch. Important parameters for the power MOSFETs are the breakdown voltage $V_{BR(DSS)}$, threshold voltage $V_{GS(TH)}$, on-resistance $R_{DS(ON)}$, reverse transfer capacitance C_{RSS}, turn-off delay $t_{D(OFF)}$ and the total gate charge Q_G.

The gate drive voltage is the input supply voltage. Since the LTC3836 is designed for operation down to low input voltages, a sublogic level MOSFET ($R_{DS(ON)}$ guaranteed at V_{GS} = 2.5V) is required for applications that work close to this voltage.

The main MOSFET's on-resistance is chosen based on the required load current. The maximum average output load current $I_{OUT(MAX)}$ is equal to the peak inductor current minus half the peak-to-peak ripple current I_{RIPPLE}. The LTC3836's current comparator monitors the drain-to-source voltage V_{DS} of the main MOSFET, which is sensed between the SENSE+ and SW pins. The peak inductor current is limited by the current threshold, set by the voltage on the I_{TH} pin of the current comparator. The voltage on the I_{TH} pin is internally clamped, which limits the maximum current sense threshold $\Delta V_{SENSE(MAX)}$ to approximately 122mV when IPRG is floating (82mV when IPRG is tied low; 202mV when IPRG is tied high).

The output current that the LTC3836 can provide is given by:

$$I_{OUT(MAX)} = \frac{\Delta V_{SENSE(MAX)}}{R_{DS(ON)}} - \frac{I_{RIPPLE}}{2}$$

A reasonable starting point is setting ripple current I_{RIPPLE} to be 40% of $I_{OUT(MAX)}$. Rearranging the above equation yields:

$$R_{DS(ON)(MAX)} = \frac{5}{6} \bullet \frac{\Delta V_{SENSE(MAX)}}{I_{OUT(MAX)}}$$

for Duty Cycle < 20%.

However, for operation above 20% duty cycle, slope compensation has to be taken into consideration to select the appropriate value of $R_{DS(ON)}$ to provide the required amount of load current:

$$R_{DS(ON)(MAX)} = \frac{5}{6} \bullet SF \bullet \frac{\Delta V_{SENSE(MAX)}}{I_{OUT(MAX)}}$$

where SF is a scale factor whose value is obtained from the curve in Figure 1.

These must be further derated to take into account the significant variation in on-resistance with temperature. The following equation is a good guide for determining the required $R_{DS(ON)MAX}$ at 25°C (manufacturer's specification), allowing some margin for variations in the LTC3836 and external component values:

$$R_{DS(ON)(MAX)} = \frac{5}{6} \bullet 0.9 \bullet SF \bullet \frac{\Delta V_{SENSE(MAX)}}{I_{OUT(MAX)} \bullet \rho_T}$$

The ρ_T is a normalizing term accounting for the temperature variation in on-resistance, which is typically about 0.4%/°C, as shown in Figure 4. Junction to case temperature T_{JC} is about 10°C in most applications. For a maximum ambient temperature of 70°C, using $\rho_{80°C} \approx 1.3$ in the above equation is a reasonable choice.

The power dissipated in the top and bottom MOSFETs strongly depends on their respective duty cycles and load current. When the LTC3836 is operating in continuous mode, the duty cycles for the MOSFETs are:

$$\text{Top MOSFET Duty Cycle} = \frac{V_{OUT}}{V_{IN}}$$

$$\text{Bottom MOSFET Duty Cycle} = \frac{V_{IN} - V_{OUT}}{V_{IN}}$$

APPLICATIONS INFORMATION

The MOSFET power dissipations at maximum output current are:

$$P_{TOP} = \frac{V_{OUT}}{V_{IN}} \bullet I_{OUT(MAX)}{}^2 \bullet \rho_T \bullet R_{DS(ON)} + 2 \bullet V_{IN}{}^2 \bullet I_{OUT(MAX)} \bullet C_{RSS} \bullet f_{OSC}$$

$$P_{BOT} = \frac{V_{IN} - V_{OUT}}{V_{IN}} \bullet I_{OUT(MAX)}{}^2 \bullet \rho_T \bullet R_{DS(ON)}$$

Both MOSFETs have I^2R losses and the P_{TOP} equation includes an additional term for transition losses, which are largest at high input voltages. The bottom MOSFET losses are greatest at high input voltage or during a short-circuit when the bottom duty cycle is nearly 100%.

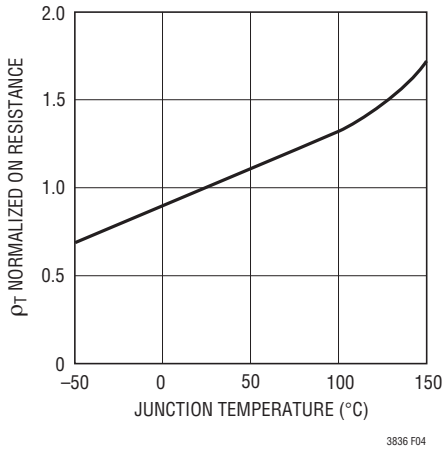


Figure 4. $R_{DS(ON)}$ vs Temperature

The LTC3836 utilizes a nonoverlapping, antishoot-through gate drive control scheme to ensure that the MOSFETs are not turned on at the same time. To function properly, the control scheme requires that the MOSFETs used are intended for DC/DC switching applications. Many power MOSFETs are intended to be used as static switches and therefore are slow to turn on or off.

Operating Frequency and Synchronization

The choice of operating frequency, f_{OSC}, is a trade-off between efficiency and component size. Low frequency operation improves efficiency by reducing MOSFET switching losses, both gate charge loss and transition loss. However, lower frequency operation requires more inductance for a given amount of ripple current.

The internal oscillator for each of the LTC3836's controllers runs at a nominal 550kHz frequency when the PLLLPF pin is left floating and the SYNC/FCB pin is a DC low or high. Pulling the PLLLPF to V_{IN} selects 750kHz operation; pulling the PLLLPF to GND selects 300kHz operation.

Alternatively, the LTC3836 will phase-lock to a clock signal applied to the SYNC/FCB pin with a frequency between 250kHz and 850kHz (see Phase-Locked Loop and Frequency Synchronization).

Inductor Value Calculation

Given the desired input and output voltages, the inductor value and operating frequency f_{OSC} directly determine the inductor's peak-to-peak ripple current:

$$I_{RIPPLE} = \frac{V_{OUT}}{V_{IN}} \left(\frac{V_{IN} - V_{OUT}}{f_{OSC} \bullet L} \right)$$

Lower ripple current reduces core losses in the inductor, ESR losses in the output capacitors, and output voltage ripple. Thus, highest efficiency operation is obtained at low frequency with a small ripple current. Achieving this, however, requires a large inductor.

A reasonable starting point is to choose a ripple current that is about 40% of $I_{OUT(MAX)}$. Note that the largest ripple current occurs at the highest input voltage. To guarantee that ripple current does not exceed a specified maximum, the inductor should be chosen according to:

$$L \geq \frac{V_{IN} - V_{OUT}}{f_{OSC} \bullet I_{RIPPLE}} \bullet \frac{V_{OUT}}{V_{IN}}$$

APPLICATIONS INFORMATION

Inductor Core Selection

Once the inductance value is determined, the type of inductor must be selected. Core loss is independent of core size for a fixed inductor value, but it is very dependent on inductance selected. As inductance increases, core losses go down. Unfortunately, increased inductance requires more turns of wire and therefore copper losses will increase.

Ferrite designs have very low core loss and are preferred at high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates "hard," which means that inductance collapses abruptly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current and consequent output voltage ripple. Do not allow the core to saturate!

Schottky Diode Selection (Optional)

The Schottky diodes D1 and D2 in Figure 16 conduct current during the dead time between the conduction of the power MOSFETs . This prevents the body diode of the bottom MOSFET from turning on and storing charge during the dead time, which could cost as much as 1% in efficiency. A 1A Schottky diode is generally a good size for most LTC3836 applications, since it conducts a relatively small average current. Larger diodes result in additional transition losses due to their larger junction capacitance. This diode may be omitted if the efficiency loss can be tolerated.

C_{IN} and C_{OUT} Selection

The selection of C_{IN} is simplified by the 2-phase architecture and its impact on the worst-case RMS current drawn through the input network (battery/fuse/capacitor). It can be shown that the worst-case capacitor RMS current occurs when only one controller is operating. The controller with the highest $(V_{OUT})(I_{OUT})$ product needs to be used in the formula below to determine the maximum RMS capacitor current requirement. Increasing the output current drawn from the other controller will actually decrease the input RMS ripple current from its maximum value. The out-of-phase technique typically reduces the input capacitor's RMS ripple current by a factor of 30% to 70% when compared to a single phase power supply solution.

In continuous mode, the source current of the main N-channel MOSFET is a square wave of duty cycle $(V_{OUT})/(V_{IN})$. To prevent large voltage transients, a low ESR capacitor sized for the maximum RMS current of one channel must be used. The maximum RMS capacitor current is given by:

$$C_{IN}\ \text{Required}\ I_{RMS} \approx \frac{I_{MAX}}{V_{IN}}\left[(V_{OUT})(V_{IN}-V_{OUT})\right]^{1/2}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that capacitor manufacturers' ripple current ratings are often based on only 2000 hours of life. This makes it advisable to further derate the capacitor, or to choose a capacitor rated at a higher temperature than required. Several capacitors may be paralleled to meet size or height requirements in the design. Due to the high operating frequency of the LTC3836, ceramic capacitors can also be used for C_{IN}. Always consult the manufacturer if there is any question.

The benefit of the LTC3836 2-phase operation can be calculated by using the equation above for the higher power controller and then calculating the loss that would have resulted if both controller channels switched on at the same time. The total RMS power lost is lower when both controllers are operating due to the reduced overlap of current pulses required through the input capacitor's ESR. This is why the input capacitor's requirement calculated above for the worst-case controller is adequate for the dual controller design. Also, the input protection fuse resistance, battery resistance, and PC board trace resistance losses are also reduced due to the reduced peak currents in a 2-phase system. The overall benefit of a multiphase design will only be fully realized when the source impedance of the power supply/battery is included in the efficiency testing. The drains of the main MOSFETs should be placed within 1cm of each other and share a common C_{IN}(s). Separating the drains and C_{IN} may produce undesirable voltage and current resonances at V_{IN}.

APPLICATIONS INFORMATION

A small (0.1µF to 1µF) bypass capacitor between the chip V_{IN} pin and ground, placed close to the LTC3836, is also suggested. A 10Ω resistor placed between C_{IN} (C1) and the V_{IN} pin provides further isolation between the two channels.

The selection of C_{OUT} is driven by the effective series resistance (ESR). Typically, once the ESR requirement is satisfied, the capacitance is adequate for filtering. The output ripple (ΔV_{OUT}) is approximated by:

$$\Delta V_{OUT} \approx I_{RIPPLE}\left(ESR + \frac{1}{8fC_{OUT}}\right)$$

where f is the operating frequency, C_{OUT} is the output capacitance and I_{RIPPLE} is the ripple current in the inductor. The output ripple is highest at maximum input voltage since I_{RIPPLE} increases with input voltage.

Setting Output Voltage

The LTC3836 output voltages are each set by an external feedback resistor divider carefully placed across the output, as shown in Figure 5. The regulated output voltage is determined by:

$$V_{OUT} = 0.6V \bullet \left(1 + \frac{R_B}{R_A}\right)$$

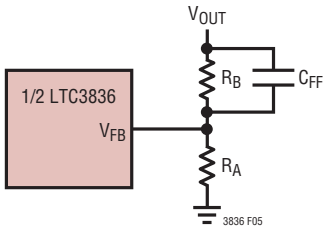


Figure 5. Setting Output Voltage

To improve the frequency response, a feedforward capacitor, C_{FF}, may be used. Great care should be taken to route the V_{FB} line away from noise sources, such as the inductor or the SW line.

Run/Soft-Start Function

The RUN/SS pin is a dual purpose pin that provides the optional external soft-start function and a means to shut down the LTC3836.

Pulling the RUN/SS pin below 0.65V puts the LTC3836 into a low quiescent current shutdown mode (I_Q = 6.5µA). If RUN/SS has been pulled all the way to ground, there will be a delay before the LTC3836 comes out of shutdown and is given by:

$$t_{DELAY} = 0.65V \bullet \frac{C_{SS}}{0.65\mu A} = 1s/\mu F \bullet C_{SS}$$

This pin can be driven directly from logic as shown in Figure 6. Diode D_{SS} in Figure 6 reduces the start delay but allows C_{SS} to ramp up slowly providing the soft-start function. This diode (and capacitor) can be deleted if the external soft-start is not needed.

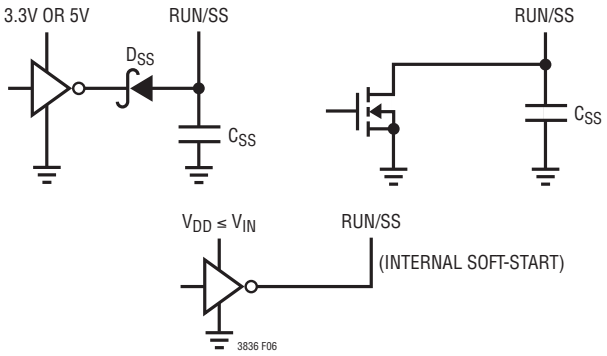


Figure 6. RUN/SS Pin Interfacing

APPLICATIONS INFORMATION

During soft-start, the start-up of V_{OUT1} is controlled by slowly ramping the positive reference to the error amplifier from 0V to 0.6V, allowing V_{OUT1} to rise smoothly from 0V to its final value. The default internal soft-start time is 1ms. This can be increased by placing a capacitor between the RUN/SS pin and SGND. In this case, the soft-start time will be approximately:

$$t_{SS1} = C_{SS} \bullet \frac{600mV}{0.65\mu A}$$

Tracking

The start-up of V_{OUT2} is controlled by the voltage on the TRACK/SS2 pin. Normally this pin is used to allow the start-up of V_{OUT2} to track that of V_{OUT1} as shown qualitatively in Figures 7a and 7b. When the voltage on the TRACK/SS2 pin is less than the internal 0.6V reference, the LTC3836 regulates the V_{FB2} voltage to the TRACK/SS2 pin voltage instead of 0.6V. The start-up of V_{OUT2} may ratiometrically track that of V_{OUT1}, according to a ratio set by a resistor divider (Figure 7c):

$$\frac{V_{OUT1}}{V_{OUT2}} = \frac{R2A}{R_{TRACKA}} \bullet \frac{R_{TRACKA} + R_{TRACKB}}{R2B + R2A}$$

For coincident tracking (V_{OUT1} = V_{OUT2} during start-up),

$R2A = R_{TRACKA}$

$R2B = R_{TRACKB}$

The ramp time for V_{OUT2} to rise from 0V to its final value is:

$$t_{SS2} = t_{SS1} \bullet \frac{0.6}{V_{OUT1F}} \bullet \frac{R_{TRACKA} + R_{TRACKB}}{R_{TRACKA}}$$

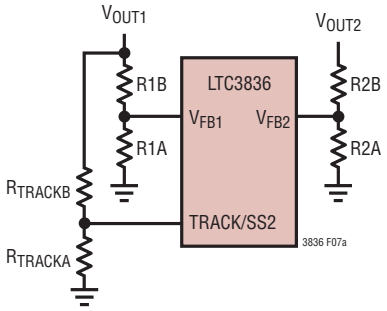
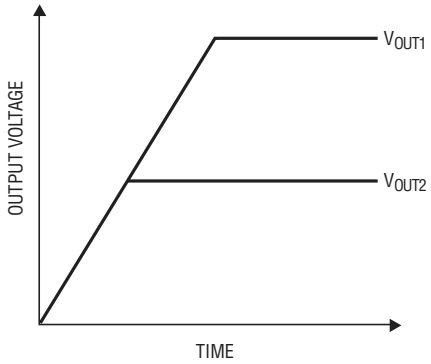
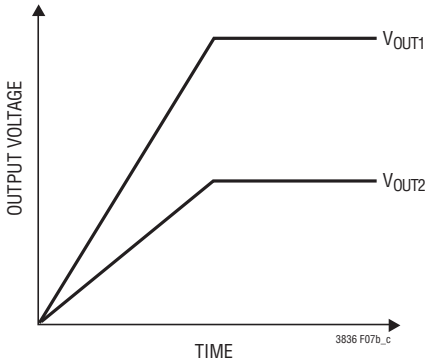


Figure 7a. Using the TRACK/SS Pin



(7b) Coincident Tracking



(7c) Ratiometric Tracking

Figures 7b and 7c. Two Different Modes of Output Voltage Tracking

APPLICATIONS INFORMATION

For coincident tracking,

$$t_{SS2} = t_{SS1} \bullet \frac{V_{OUT2F}}{V_{OUT1F}}$$

where V_{OUT1F} and V_{OUT2F} are the final, regulated values of V_{OUT1} and V_{OUT2}. V_{OUT1} should always be greater than V_{OUT2} when using the TRACK/SS2 pin for tracking. If no tracking function is desired, then the TRACK/SS2 pin may be tied to a capacitor to ground, which sets the ramp time to final regulated output voltage.

Phase-Locked Loop and Frequency Synchronization

The LTC3836 has a phase-locked loop (PLL) comprised of an internal voltage-controlled oscillator (VCO) and a phase detector. This allows the turn-on of the main N-channel MOSFET of controller 1 to be locked to the rising edge of an external clock signal applied to the SYNC/FCB pin. The turn-on of controller 2's main N-channel MOSFET is thus 180 degrees out-of-phase with the external clock. The phase detector is an edge sensitive digital type that provides zero degrees phase shift between the external and internal oscillators. This type of phase detector does not exhibit false lock to harmonics of the external clock.

The output of the phase detector is a pair of complementary current sources that charge or discharge the external filter network connected to the PLLLPF pin. The relationship between the voltage on the PLLLPF pin and operating frequency, when there is a clock signal applied to SYNC/FCB, is shown in Figure 8 and specified in the Electrical Characteristics table. Note that the LTC3836 can only be synchronized to an external clock whose frequency is within range of the LTC3836's internal VCO, which is nominally 200kHz to 1MHz. This is guaranteed, over temperature and variations, to be between 300kHz and 750kHz. A simplified block diagram is shown in Figure 9.

If the external clock frequency is greater than the internal oscillator's frequency, f_{OSC}, then current is sourced continuously from the phase detector output, pulling up the PLLLPF pin. When the external clock frequency is less than f_{OSC}, current is sunk continuously, pulling down the PLLLPF pin. If the external and internal frequencies

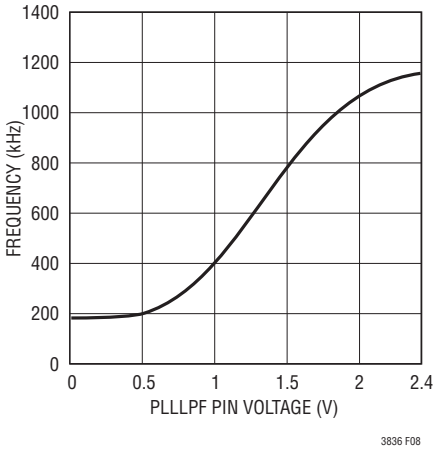


Figure 8. Relationship Between Oscillator Frequency and Voltage at the PLLLPF Pin When Synchronizing to an External Clock

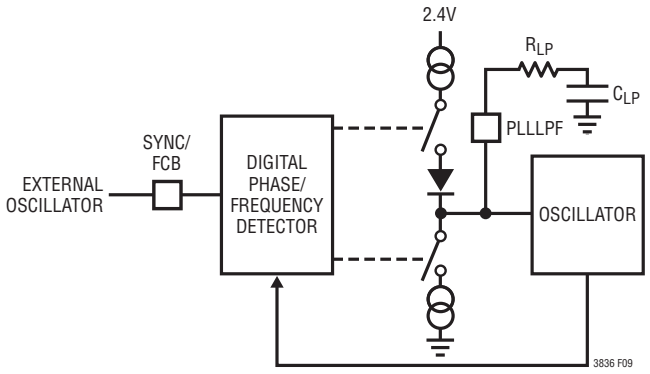


Figure 9. Phase-Locked Loop Block Diagram

APPLICATIONS INFORMATION

are the same but exhibit a phase difference, the current sources turn on for an amount of time corresponding to the phase difference. The voltage on the PLLLPF pin is adjusted until the phase and frequency of the internal and external oscillators are identical. At the stable operating point, the phase detector output is high impedance and the filter capacitor C_{LP} holds the voltage.

The loop filter components, C_{LP} and R_{LP}, smooth out the current pulses from the phase detector and provide a stable input to the voltage-controlled oscillator. The filter components C_{LP} and R_{LP} determine how fast the loop acquires lock. Typically R_{LP} = 10k and C_{LP} is 2200pF to 0.01µF.

Typically, the external clock (on SYNC/FCB pin) input high level is 1.6V, while the input low level is 1.2V.

Table 1 summarizes the different states in which the PLLLPF pin can be used.

Table 1.

PLLLPF PIN	SYNC/FCB PIN	FREQUENCY
0V	DC Voltage	300kHz
Floating	DC Voltage	550kHz
V_{IN}	DC Voltage	750kHz
RC Loop Filter	Clock Signal	Phase-Locked to External Clock

Topside MOSFET Drive Supply (C_B, D_B)

In the Functional Diagram, external bootstrap capacitor C_B is charged from a boost power source (usually V_{IN}) through diode D_B when the SW node is low. When a MOSFET is to be turned on, the C_B voltage is applied across the gate-source of the desired device. When the topside MOSFET is on, the BOOST pin voltage is above the input supply. $V_{BOOST} = 2V_{IN}$. C_B must be 100 times the total input capacitance of the topside MOSFET. The reverse breakdown of D_B must be greater than $V_{IN(MAX)}$. Figure 6 shows how a 5V gate drive can be achieved if a secondary 5V supply is available. Note that in applications where the supply voltage to C_B exceeds V_{IN}, the BOOST pin will draw approximately 500µA in shutdown mode.

Table 2 summarizes the different states in which the SYNC/FCB pin can be used

Table 2.

SYNC/FCB PIN	CONDITION
0V to 0.5V	Forced Continuous Mode Current Reversal Allowed
0.7V to V_{IN}	Pulse-Skipping Operation Enabled No Current Reversal Allowed
External Clock Signal	Enable Phase-Locked Loop (Synchronize to External CLK) Pulse-Skipping at Light Loads No Current Reversal Allowed

Fault Condition: Short-Circuit and Current Limit

To prevent excessive heating of the bottom MOSFET, foldback current limiting can be added to reduce the current in proportion to the severity of the fault.

Foldback current limiting is implemented by adding diodes D_{FB1} and D_{FB2} between the output and the I_{TH} pin as shown in Figure 11. In a hard short (V_{OUT} = 0V), the current will be reduced to approximately 50% of the maximum output current.

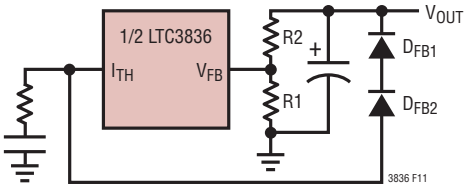


Figure 11. Foldback Current Limiting

APPLICATIONS INFORMATION

Using a Sense Resistor

A sense resistor R_{SENSE} can be connected between V_{IN} and SW to sense the output load current. In this case, the drain of the topside N-channel MOSFET is connected to $SENSE^-$ pin and the source is connected to the SW pin of the LTC3836. Therefore, the current comparator monitors the voltage developed across R_{SENSE}, not the V_{DS} of the top MOSFET. The output current that the LTC3836 can provide in this case is given by:

$$I_{OUT(MAX)} = \frac{\Delta V_{SENSE(MAX)}}{R_{DS(ON)}} - \frac{I_{RIPPLE}}{2}$$

Setting ripple current as 40% of $I_{OUT(MAX)}$ and using Figure 1 to choose SF, the value of R_{SENSE} is:

$$R_{SENSE} = \frac{5}{6} \bullet SF \bullet \frac{\Delta V_{SENSE(MAX)}}{I_{OUT(MAX)}}$$

Variation in the resistance of a sense resistor is much smaller than the variation in on-resistance of an external MOSFET. Therefore the load current is well controlled with a sense resistor. However the sense resistor causes extra I^2R losses in addition to those of the MOSFET. Therefore, using a sense resistor lowers the efficiency of LTC3836, especially at high load currents.

Low Supply Operation

Although the LTC3836 can function down to below 2.4V, the maximum allowable output current is reduced as V_{IN} decreases below 3V. Figure 12 shows the amount of change as the supply is reduced down to 2.4V. Also shown is the effect on V_{REF}.

Minimum On-Time Considerations

Minimum on-time, $t_{ON(MIN)}$, is the smallest amount of time that the LTC3836 is capable of turning the main N-channel MOSFET on and then off. It is determined by internal timing delays and the gate charge required to turn on the top MOSFET. Low duty cycle and high frequency applications may approach the minimum on-time limit and care should be taken to ensure that:

$$t_{ON(MIN)} < \frac{V_{OUT}}{f_{OSC} \bullet V_{IN}}$$

If the duty cycle falls below what can be accommodated by the minimum on-time, the LTC3836 will begin to skip cycles (unless forced continuous mode is selected). The output voltage will continue to be regulated, but the ripple current and ripple voltage will increase. The minimum on-time for the LTC3836 is typically about 200ns. However, as the peak sense voltage ($I_{L(PEAK)} \bullet R_{DS(ON)}$) decreases, the minimum on-time gradually increases up to about 250ns. This is of particular concern in forced continuous applications with low ripple current at light loads. If forced continuous mode is selected and the duty cycle falls below the minimum on-time requirement, the output will be regulated by overvoltage protection.

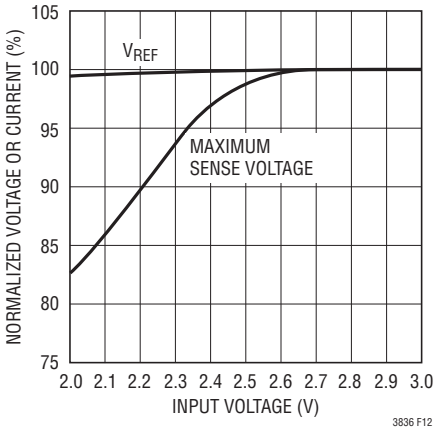


Figure 12. Line Regulation of V_{REF} and Maximum Sense Voltage for Low Input Supply

APPLICATIONS INFORMATION

Efficiency Considerations

The efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting efficiency and which change would produce the most improvement. Efficiency can be expressed as:

Efficiency = 100% – (L1 + L2 + L3 + …)

where L1, L2, etc. are the individual losses as a percentage of input power.

Although all dissipative elements in the circuit produce losses, five main sources usually account for most of the losses in LTC3836 circuits: 1) LTC3836 DC bias current, 2) MOSFET gate charge current, 3) I^2R losses, and 4) transition losses.

1) The V_{IN} (pin) current is the DC supply current, given in the electrical characteristics, excluding MOSFET driver currents. V_{IN} current results in a small loss that increases with V_{IN}.
2) MOSFET gate charge current results from switching the gate capacitance of the power MOSFETs. Each time a MOSFET gate is switched from low to high to low again, a packet of charge dQ moves from $SENSE^+$ to ground. The resulting dQ/dt is a current out of $SENSE^+$, which is typically much larger than the DC supply current. In continuous mode, $I_{GATECHG} = f \bullet Q_P$.
3) I^2R losses are calculated from the DC resistances of the MOSFETs and inductor. In continuous mode, the average output current flows through L but is "chopped" between the top MOSFET and the bottom MOSFET. The MOSFET $R_{DS(ON)}$s multiplied by duty cycle can be summed with the resistance of L to obtain I^2R losses.
4) Transition losses apply to the top MOSFET and increase with higher operating frequencies and input voltages. Transition losses can be estimated from:

Transition Loss = $2 (V_{IN})^2 I_{O(MAX)} C_{RSS} (f)$

Other losses, including C_{IN} and C_{OUT} ESR dissipative losses and inductor core losses, generally account for less than 2% total additional loss.

Checking Transient Response

The regulator loop response can be checked by looking at the load transient response. Switching regulators take several cycles to respond to a step in load current. When a load step occurs, V_{OUT} immediately shifts by an amount equal to $(\Delta I_{LOAD})(ESR)$, where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT}, which generates a feedback error signal. The regulator loop then returns V_{OUT} to its steady-state value. During this recovery time, V_{OUT} can be monitored for overshoot or ringing. OPTI-LOOP® compensation allows the transient response to be optimized over a wide range of output capacitance and ESR values.

The I_{TH} series R_C-C_C filter (see Functional Diagram) sets the dominant pole-zero loop compensation. The I_{TH} external components shown in the Typical Application on the front page of this data sheet will provide an adequate starting point for most applications. The values can be modified slightly (from 0.2 to 5 times their suggested values) to optimize transient response once the final PC layout is done and the particular output capacitor type and value have been determined. The output capacitors need to be decided upon because the various types and values determine the loop feedback factor gain and phase. An output current pulse of 20% to 100% of full load current having a rise time of 1µs to 10µs will produce output voltage and I_{TH} pin waveforms that will give a sense of the overall loop stability. The gain of the loop will be increased by increasing R_C, and the bandwidth of the loop will be increased by decreasing C_C. The output voltage settling behavior is related to the stability of the closed-loop system and will demonstrate the actual overall supply performance. For a detailed explanation of optimizing the compensation components, including a review of control loop theory, refer to Application Note 76.

A second, more severe transient is caused by switching in loads with large (>1µF) supply bypass capacitors. The discharged bypass capacitors are effectively put in parallel with C_{OUT}, causing a rapid drop in V_{OUT}. No regulator can deliver enough current to prevent this problem if the load switch resistance is low and it is driven quickly. The only solution is to limit the rise time of the switch drive so that the load rise time is limited to approximately $(25)(C_{LOAD})$. Thus a 10µF capacitor would require a 250µs rise time, limiting the charging current to about 200mA.

APPLICATIONS INFORMATION

PC Board Layout Checklist

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the LTC3836. These items are illustrated in the layout diagram of Figure 13. Figure 14 depicts the current waveforms present in the various branches of the 2-phase dual regulator.

1) The power loop (input capacitor, MOSFETs, inductor, output capacitor) of each channel should be as small as possible and isolated as much as possible from the power loop of the other channel. Ideally, the main and synchronous FETs should be connected close to one another with an input capacitor placed right at the FETs. It is better to have two separate, smaller valued input capacitors (e.g., two 10µF — one for each channel) than it is to have a single larger valued capacitor (e.g., 22µF) that the channels share with a common connection.

2) The signal and power grounds should be kept separate. The signal ground consists of the feedback resistor dividers, I_{TH} compensation networks and the SGND pin.

   The power grounds consist of the (–) terminal of the input and output capacitors and the source of the synchronous N-channel MOSFET. Each channel should have its own power ground for its power loop (as described above in item 1). The power grounds for the two channels should connect together at a common point. It is most important to keep the ground paths with high switching currents away from each other.

   The PGND pins on the LTC3836 should be shorted together and connected to the common power ground connection (away from the switching currents).

3) Put the feedback resistors close to the V_{FB} pins. The trace connecting the top feedback resistor (R_B) to the output capacitor should be a Kelvin trace. The I_{TH} compensation components should also be very close to the LTC3836.

4) The current sense traces (SENSE+ and SW) should be Kelvin connections right at the main N-channel MOSFET drains and sources.

5) Keep the switch nodes (SW1, SW2) and the gate driver nodes (TG1, TG2, BG1, BG2) away from the small-signal components, especially the opposite channel's feedback resistors, I_{TH} compensation components, and the current sense pins (SENSE+ and SW).

6) Connect the boost capacitors to the switch nodes, not to the small signal nodes SWn. Connect the boost diodes to the positive terminal of the input capacitor.

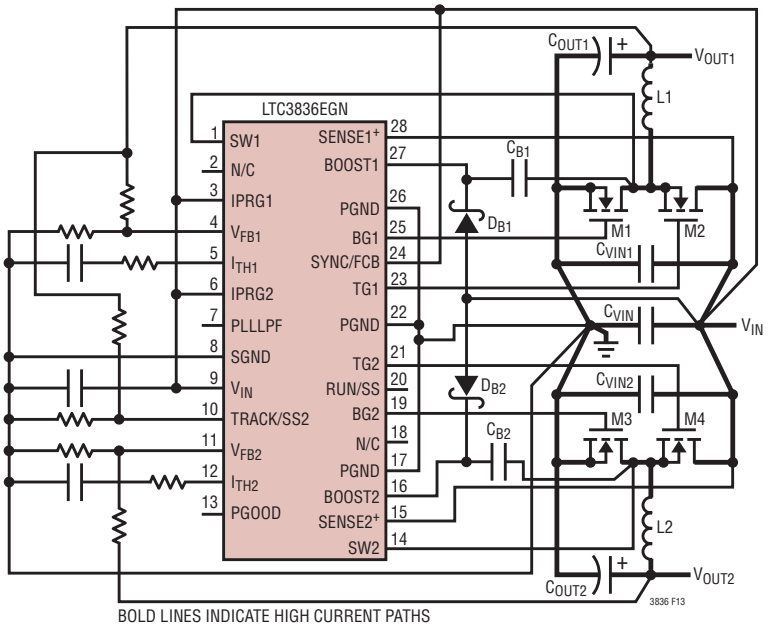


Figure 13. LTC3836 Layout Diagram

APPLICATIONS INFORMATION

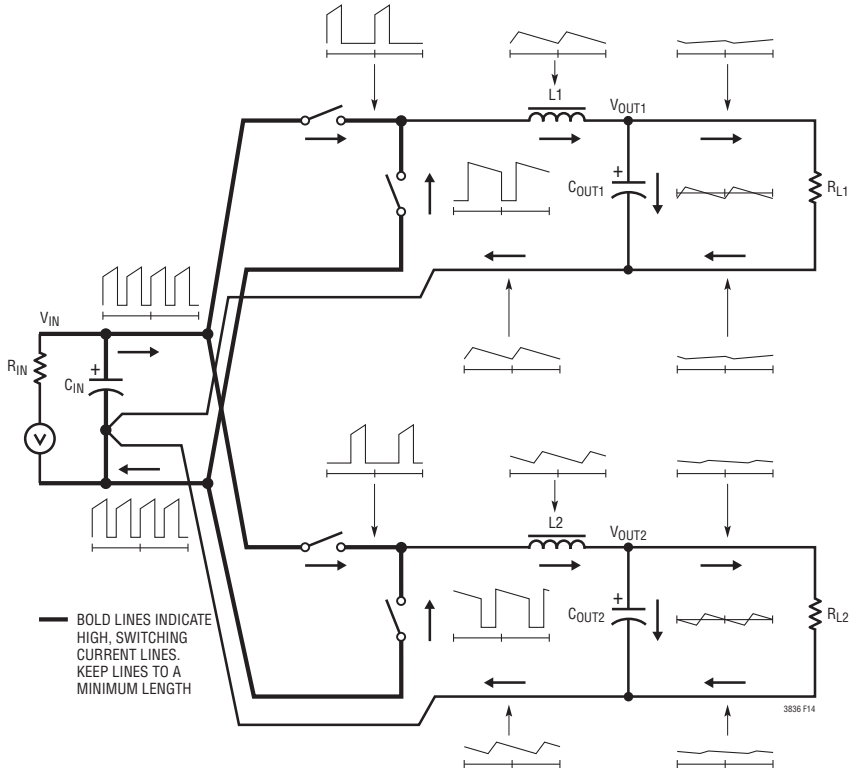
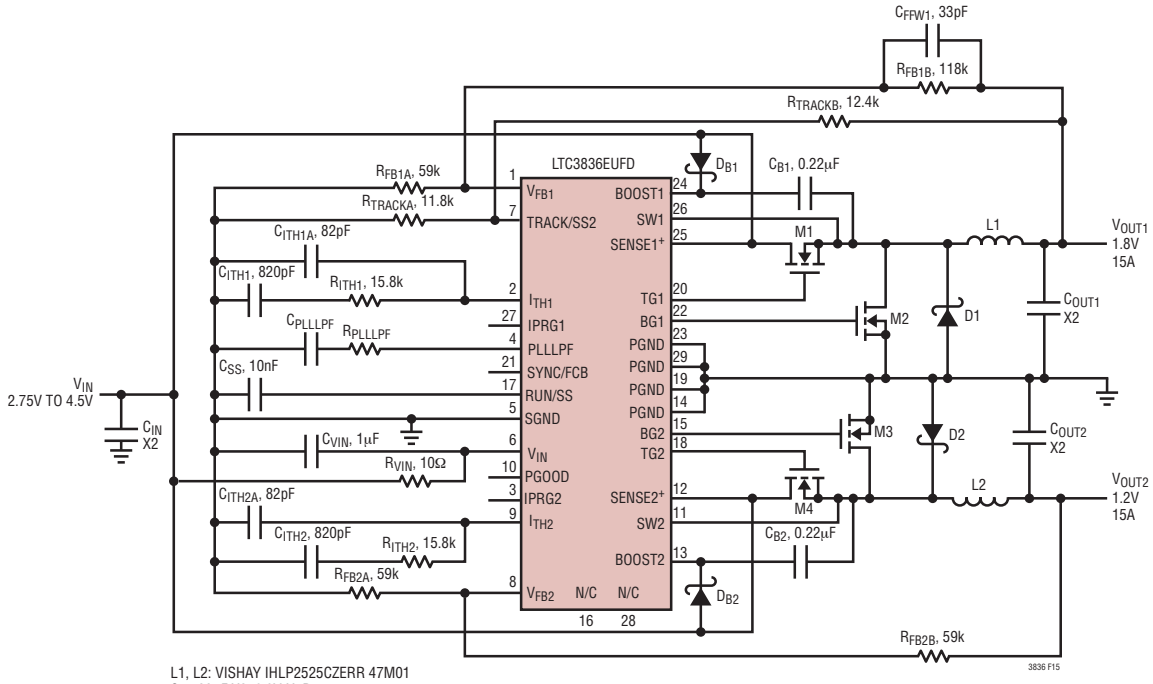


Figure 14. Branch Current Waveforms



L1, L2: VISHAY IHLP2525CZERR 47M01
C_{IN}: 22µF X2, 6.3V, X5R
C_{OUT1}, C_{OUT2}: TAIYO YUDEN JMK235BJ107MM X2
M1-M4: VISHAY Si7882DP

Figure 15. 2-Phase, 550kHz, Dual Output Synchronous DC/DC Converter with Ceramic Output Capacitors

APPLICATIONS INFORMATION

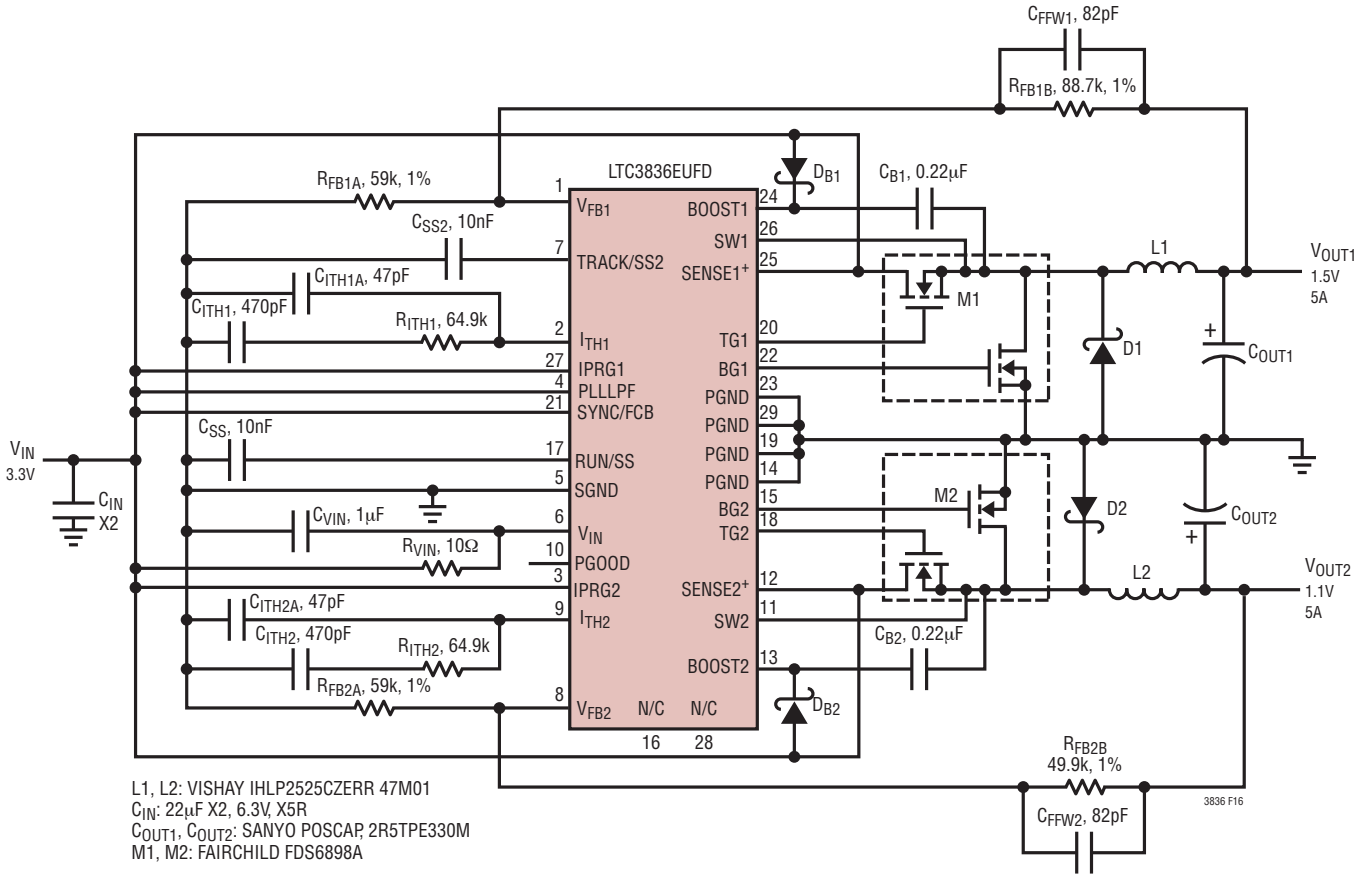


Figure 16a. 2-Phase, 750kHz, Dual Output Synchronous DC/DC Converter

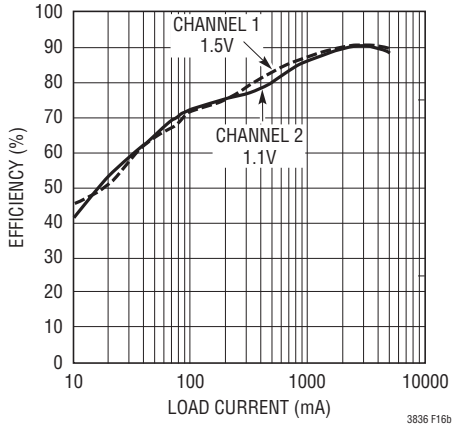


Figure 16b. Efficiency vs Load Current

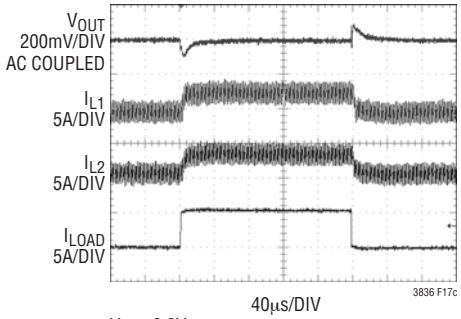


Figure 16c. Load Step

TYPICAL APPLICATIONS

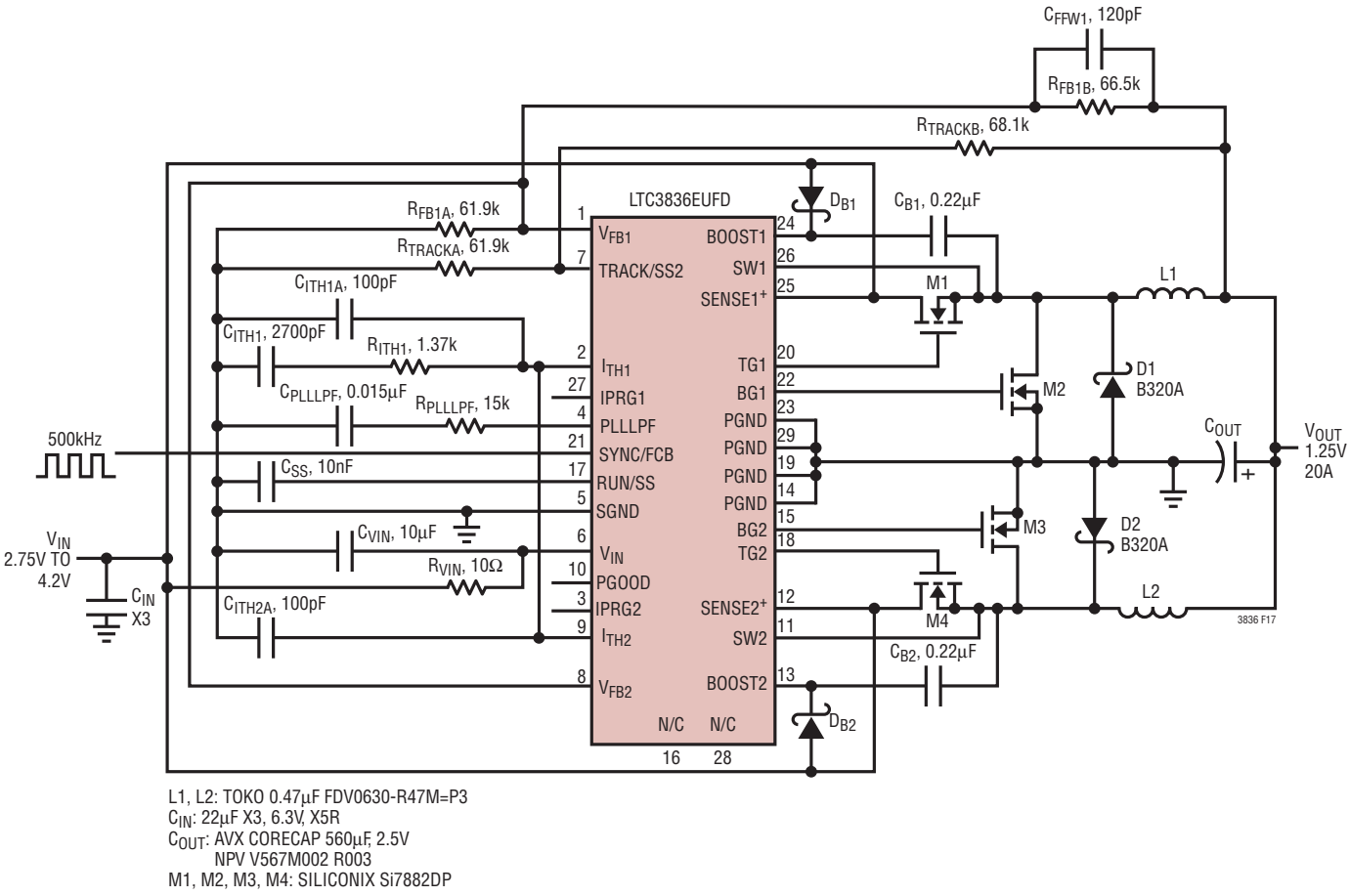


Figure 17a. Single Output, High Current Application with External Frequency Synchronization

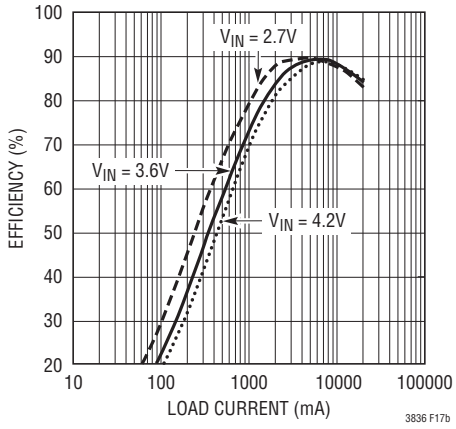


Figure 17b. Efficiency vs Load Current

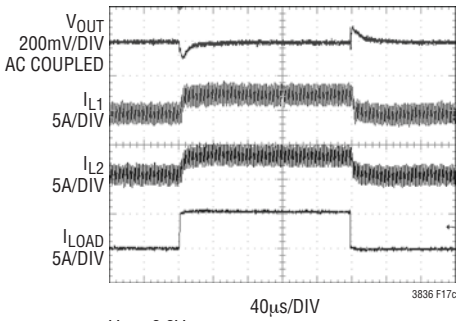
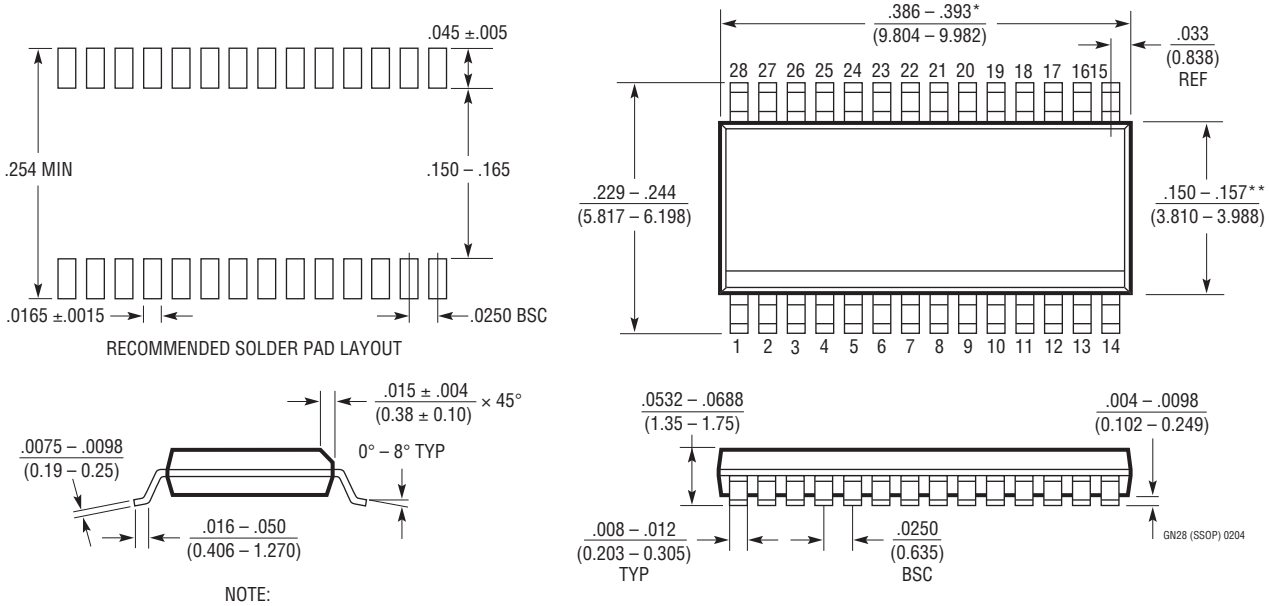


Figure 17c. Load Step

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

GN Package
28-Lead Plastic SSOP (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1641)



NOTE:
1. CONTROLLING DIMENSION: INCHES
2. DIMENSIONS ARE IN $\frac{\text{INCHES}}{(\text{MILLIMETERS})}$
3. DRAWING NOT TO SCALE

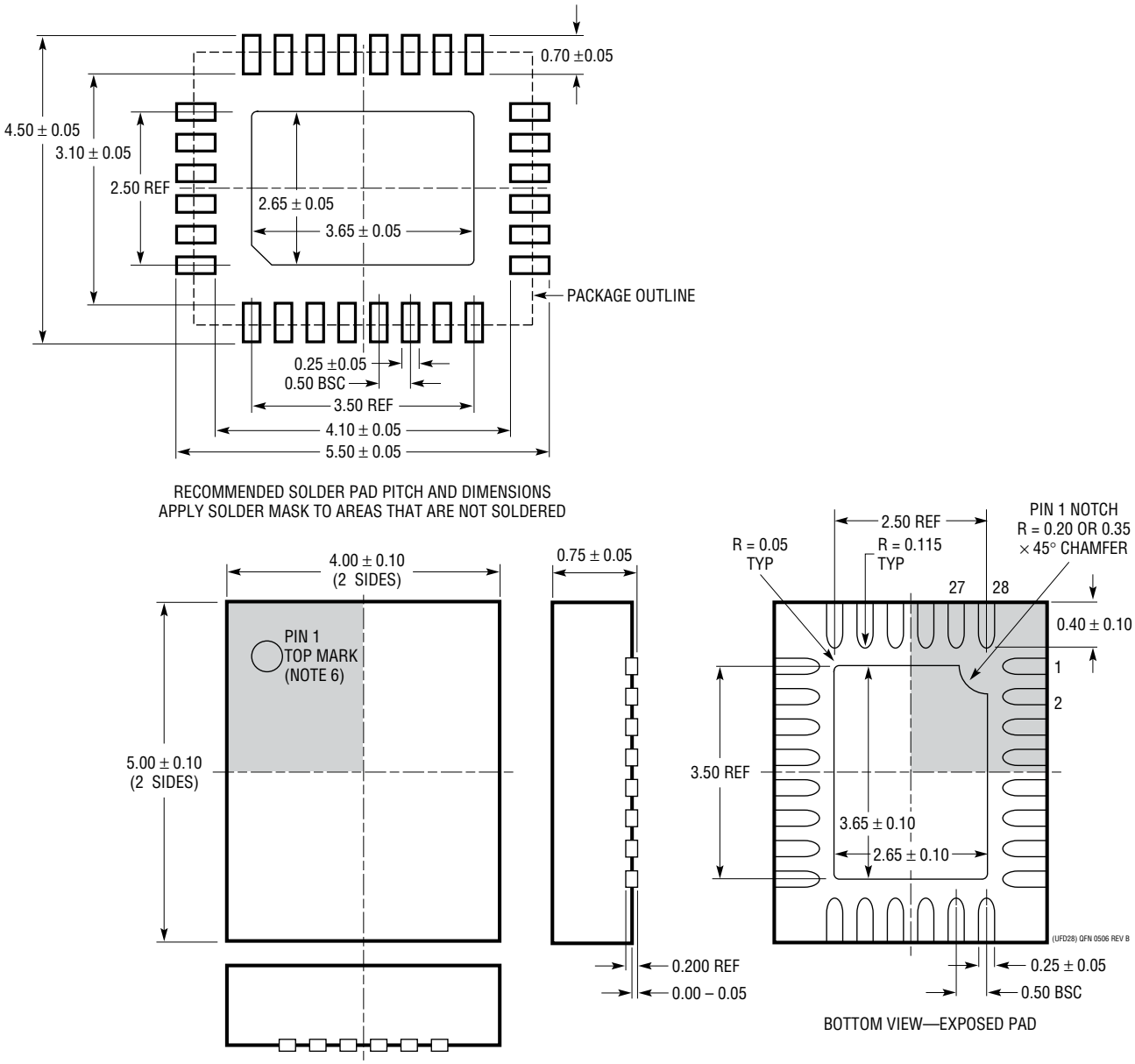
*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

UFD Package
28-Lead Plastic QFN (4mm × 5mm)
(Reference LTC DWG # 05-08-1712 Rev B)



NOTE:
1. DRAWING PROPOSED TO BE MADE A JEDEC PACKAGE OUTLINE MO-220 VARIATION (WXXX-X).
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED

REVISION HISTORY (Revision history begins at Rev B)

REV	DATE	DESCRIPTION	PAGE NUMBER
B	11/11	Updated Figure 17a	26

LINEAR TECHNOLOGY

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1735	High Efficiency Synchronous Step-Down Controller	Burst Mode® Operation, 16-Pin Narrow SSOP, 3.5V ≤ V_{IN} ≤ 36V
LTC1778	No R_{SENSE} Synchronous Step-Down Controller	Current Mode Operation Without Sense Resistor, Fast Transient Response, 4V ≤ V_{IN} ≤ 36V
LTC2923	Power Supply Tracking Controller	Controls Up to Three Supplies, 10-Lead MSOP
LTC3411	1.25A (I_{OUT}), 4MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 2.5V to 5.5V, I_Q = 60µA, I_{SD} = <1µA, MS Package
LTC3412A	3A (I_{OUT}), 4MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 2.25V to 5.5V, V_{OUT} = 0.8V, I_Q = 60mA, I_{SD} = <1mA, TSSOP-16E and 4mm × 4mm QFN Packages
LTC3415	7A, PolyPhase Synchronous Step-Down Regulator with Output Tracking and Margining	V_{IN}: 2.5V to 5.5V, Spread Spectrum Operation, 5mm × 7mm QFN Package
LTC3416	4A (I_{OUT}), 4MHz, Synchronous Step-Down DC/DC Converter with Output Tracking	95% Efficiency, V_{IN}: 2.25V to 5.5V, I_{SD} = <1µA, TSSOP-20E Package
LTC3418	8A, 4MHz Synchronous Step-Down Regulator	V_{IN}: 2.25V to 5.5V, 5mm × 7mm QFN Package
LTC3701	2-Phase, Low Input Voltage Dual Step-Down DC/DC Controller	2.5V ≤ V_{IN} ≤ 9.8V, 550kHz, PGOOD, PLL, 16-Lead SSOP
LTC3708	Fast 2-Phase, No R_{SENSE} Buck Controller with Output Tracking	Constant On-Time Dual Controller, V_{IN} Up to 36V, Very Low Duty Cycle Operation, 5mm × 5mm QFN Package
LTC3728/LTC3728L	Dual, 550kHz, 2-Phase Synchronous Step-Down Switching Regulator	Constant-Frequency, V_{IN} to 36V, 5V and 3.3V LDOs, 5mm × 5mm QFN or 28-Lead SSOP
LTC3736	Dual, 2-Phase, No R_{SENSE} Synchronous Controller	2.75V ≤ V_{IN} ≤ 9.8V, Output Tracking, Burst Mode Operation
LTC3736-1	Dual, 2-Phase, No R_{SENSE} Synchronous Controller with Spread Spectrum	V_{IN}: 2.75V to 9.8V, 4mm × 4mm QFN Package Spread Spectrum Operation; Output Tracking
LTC3736-2	2-Phase, No R_{SENSE}, Dual Synchronous Controller with Output Tracking	2.75V ≤ V_{IN} ≤ 9.8V, 0.6V ≤ V_{OUT} ≤ V_{IN}, 0.6V ±1% Reference, High Current Limit, 4mm × 4mm QFN Package
LTC3737	Dual, 2-Phase, No R_{SENSE} Controller with Output Tracking	Non-Synchronous Constant-Frequency with PLL, 4mm × 4mm QFN and 24-Lead SSOP Packages
LTC3772	No R_{SENSE} Step-Down DC/DC Controller	2.75V ≤ V_{IN} ≤ 9.8V, SOT-23 or 3mm × 2mm DFN Packages
LTC3776	Dual, 2-Phase, No R_{SENSE} Synchronous Controller for DDR/QDR Memory Termination	Provides V_{DDQ} and V_{TT} with One IC, 2.75V ≤ V_{IN} ≤ 9.8V, 4mm × 4mm QFN and 24-Lead SSOP Packages
LTC3808	No R_{SENSE}, Low EMI, Synchronous Step-Down Controller with Output Tracking	2.75V ≤ V_{IN} ≤ 9.8V; Spread Spectrum Operation; 3mm × 4mm DFN and 16-Lead SSOP Packages
LTC3809/LTC3809-1	No R_{SENSE} Synchronous Step-Down Controllers	2.75V to 9.8V, 3mm × 3mm DFN and 10-Lead MSOPE Packages
LTC3822	No R_{SENSE}, Low V_{IN}, All N-Channel MOSFET, Synchronous Step-Down DC/DC Controller	2.75V ≤ V_{IN} ≤ 4.5V; 0.6V ≤ V_{OUT} ≤ V_{IN}, 10-Lead MS and 3mm x 3mm DFN Packages
LTC3822-1	No R_{SENSE}, Low V_{IN}, All N-Channel MOSFET, Synchronous Step-Down DC/DC Controller with External Soft-Start	2.75V ≤ V_{IN} ≤ 4.5V; 0.6V ≤ V_{OUT} ≤ V_{IN}, 16-Lead SSOP and 3mm x 3mm DFN Packages

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