High Power Step-Down Synchronous DC/DC Controllers for Low Voltage Operation

FEATURES

- **V_{OUT} as Low as 0.6V**
- **High Power Switching Regulator Controller for 3.3V-5V to 0.6V-3.xV Step-Down Applications**
- **No Current Sense Resistor Required**
- **Low Input Supply Voltage Range: 3V to 8V**
- **Maximum Duty Cycle >91% Over Temperature**
- All N-Channel External MOSFETs
- Excellent Output Regulation: ±1% Over Line, Load and Temperature Variations
- High Efficiency: Over 95% Possible
- Adjustable or Fixed 2.5V Output (LTC3832)
- Programmable Fixed Frequency Operation: 100kHz to 500kHz
- External Clock Synchronization
- Soft-Start
- Low Shutdown Current: <10µA
- Overtemperature Protection
- Available in SO-8 and SSOP-16 Packages

APPLICATIONS

- CPU Power Supplies
- Multiple Logic Supply Generator
- Distributed Power Applications
- High Efficiency Power Conversion

DESCRIPTION

The LTC®3832/LTC3832-1 are high power, high efficiency switching regulator controllers optimized for 3.3V-5V to 0.6V-3.xV step-down applications. A precision internal reference and feedback system provide ±1% output regulation over temperature, load current and line voltage variations. The LTC3832/LTC3832-1 use a synchronous switching architecture with N-channel MOSFETs. Additionally, the chip senses output current through the drain-source resistance of the upper N-channel MOSFET, providing an adjustable current limit without a current sense resistor.

The LTC3832/LTC3832-1 operate with an input supply voltage as low as 3V and with a maximum duty cycle of >91% over temperature. They include a fixed frequency PWM oscillator for low output ripple operation. The 300kHz free-running clock frequency can be externally adjusted or synchronized with an external signal from 100kHz to 500kHz. In shutdown mode, the LTC3832 supply current drops to <10µA. The LTC3832-1 is the SO-8 version without current limit, frequency adjustment and shutdown functions.

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TYPICAL APPLICATION

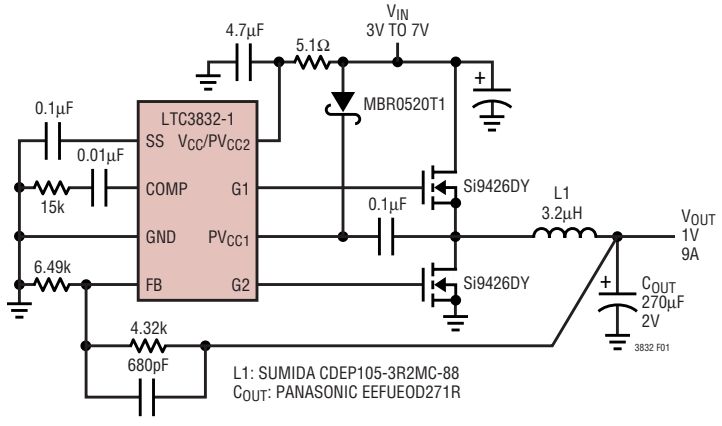
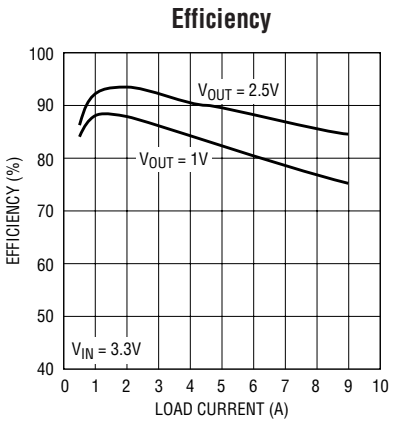


Figure 1. High Efficiency 3.3V to 1V Power Converter



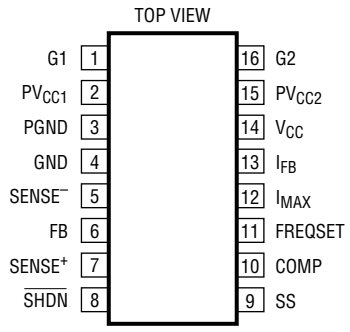
ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage
- V_{CC} 9V
- $PV_{CC1,2}$ 14V

Input Voltage
- I_{FB}, I_{MAX} ..... –0.3V to 14V
- $\overline{SENSE}^+$, $SENSE^-$, FB, $\overline{SHDN}$, FREQSET ..... –0.3V to V_{CC} + 0.3V

Junction Temperature ..... 125°C
Operating Temperature Range (Note 9) .. –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

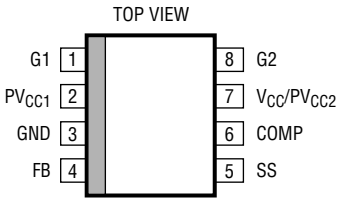
PACKAGE/ORDER INFORMATION



GN PACKAGE
16-LEAD PLASTIC SSOP

T_{JMAX} = 125°C, θ_{JA} = 130°C/W

ORDER PART NUMBER
LTC3832EGN
GN PART MARKING
3832



S8 PACKAGE
8-LEAD PLASTIC SO

T_{JMAX} = 125°C, θ_{JA} = 130°C/W

ORDER PART NUMBER
LTC3832-1ES8
S8 PART MARKING
38321

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes specifications that apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC}, PV_{CC1}, PV_{CC2} = 5V, unless otherwise noted. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CC}	Supply Voltage		●	3	5	8	V
PV_{CC}	PV_{CC1}, PV_{CC2} Voltage	(Note 7)	●	3		13.2	V
V_{UVLO}	Undervoltage Lockout Voltage				2.4	2.9	V
V_{FB}	Feedback Voltage	V_{COMP} = 1.25V	 ●	0.595 0.593	0.6 0.6	0.605 0.607	V V
V_{OUT}	Output Voltage	V_{COMP} = 1.25V	 ●	2.462 2.450	2.5 2.5	2.538 2.550	V V
ΔV_{OUT}	Output Load Regulation Output Line Regulation	I_{OUT} = 0A to 10A (Note 6) V_{CC} = 4.75V to 5.25V			2 0.1		mV mV

ELECTRICAL CHARACTERISTICS

The ● denotes specifications that apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC}, PV_{CC1}, PV_{CC2} = 5V, unless otherwise noted. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_{VCC}	Supply Current	Figure 2, $V_{\overline{SHDN}} = V_{CC}$ $V_{\overline{SHDN}} = 0V$	● ●		0.7 1	1.6 10	mA µA
I_{PVCC}	PV_{CC} Supply Current	Figure 2, $V_{\overline{SHDN}} = V_{CC}$ (Note 3) $V_{\overline{SHDN}} = 0V$	● ●		20 0.1	30 10	mA µA
f_{OSC}	Internal Oscillator Frequency	FREQSET Floating	●	230	300	360	kHz
V_{SAWL}	V_{COMP} at Minimum Duty Cycle				1.2		V
V_{SAWH}	V_{COMP} at Maximum Duty Cycle				2.2		V
$V_{COMPMAX}$	Maximum V_{COMP}	V_{FB} = 0V, PV_{CC1} = 8V			2.85		V
$\Delta f_{OSC}/\Delta I_{FREQSET}$	Frequency Adjustment				10		kHz/µA
A_V	Error Amplifier Open-Loop DC Gain	Measured from FB to COMP, $SENSE^+$ and $SENSE^-$ Floating, (Note 4)	●	50	65		dB
g_m	Error Amplifier Transconductance	Measured from FB to COMP, $SENSE^+$ and $SENSE^-$ Floating, (Note 4)	●	1600	2000	2400	µmho
I_{COMP}	Error Amplifier Output Sink/Source Current				100		µA
I_{MAX}	I_{MAX} Sink Current	$V_{IMAX} = V_{CC}$ (Note 10)	 ●	8 4	12 12	16 20	µA µA
	I_{MAX} Sink Current Tempco	$V_{IMAX} = V_{CC}$ (Note 6)			3300		ppm/°C
V_{IH}	$\overline{SHDN}$ Input High Voltage		●	2.4			V
V_{IL}	$\overline{SHDN}$ Input Low Voltage		●			0.8	V
I_{IN}	$\overline{SHDN}$ Input Current	$V_{\overline{SHDN}} = V_{CC}$	●		0.1	1	µA
I_{SS}	Soft-Start Source Current	V_{SS} = 0V, V_{IMAX} = 0V, $V_{IFB} = V_{CC}$	●	–8	–12	–18	µA
I_{SSIL}	Maximum Soft-Start Sink Current In Current Limit	$V_{IMAX} = V_{CC}$, V_{IFB} = 0V, $V_{SS} = V_{CC}$ (Note 8), PV_{CC1} = 8V			1.6		mA
R_{SENSE}	SENSE Input Resistance				23.7		kΩ
$R_{SENSEFB}$	SENSE to FB Resistance				18		kΩ
t_r, t_f	Driver Rise/Fall Time	Figure 2, $PV_{CC1} = PV_{CC2}$ = 5V (Note 5)	●		80	250	ns
t_{NOV}	Driver Nonoverlap Time	Figure 2, $PV_{CC1} = PV_{CC2}$ = 5V (Note 5)	●	25	120	250	ns
DC_{MAX}	Maximum G1 Duty Cycle	Figure 2, V_{FB} = 0V (Note 5), PV_{CC1} = 8V	●	91	95		%

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.

Note 3: Supply current in normal operation is dominated by the current needed to charge and discharge the external FET gates. This will vary with the LTC3832 operating frequency, operating voltage and the external FETs used.

Note 4: The open-loop DC gain and transconductance from the $SENSE^+$ and $SENSE^-$ pins to COMP pin will be $(A_V)(0.6/2.5)$ and $(g_m)(0.6/2.5)$ respectively.

Note 5: Rise and fall times are measured using 10% and 90% levels. Duty cycle and nonoverlap times are measured using 50% levels.

Note 6: Guaranteed by design, not subject to test.

Note 7: PV_{CC1} must be higher than V_{CC} by at least 2.5V for G1 to operate at 95% maximum duty cycle and for the current limit protection circuit to be active.

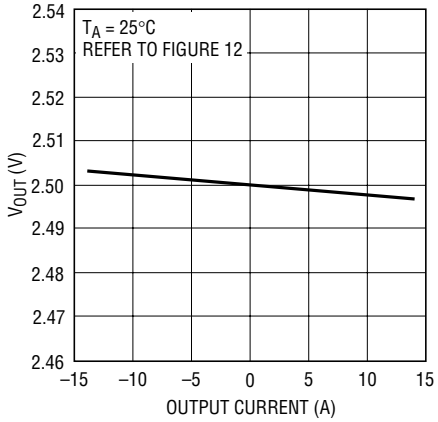
Note 8: The current limiting amplifier can sink but cannot source current. Under normal (not current limited) operation, the output current will be zero.

Note 9: The LTC3832E/LTC3832-1E are guaranteed to meet performance specifications from 0°C to 70°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls.

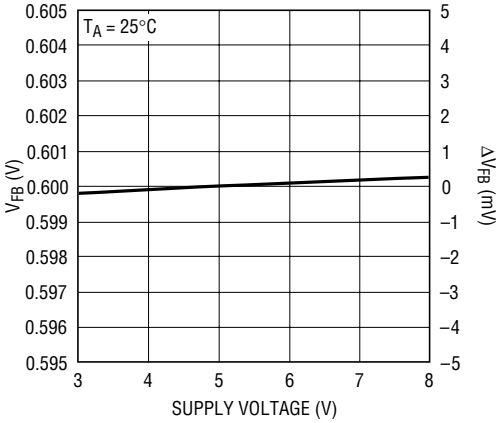
Note 10: The minimum and maximum limits for I_{MAX} over temperature includes the intentional temperature coefficient of 3300ppm/°C. This induced temperature coefficient counteracts the typical temperature coefficient of the external power MOSFET on-resistance. This results in a relatively flat current limit over temperature for the application.

TYPICAL PERFORMANCE CHARACTERISTICS

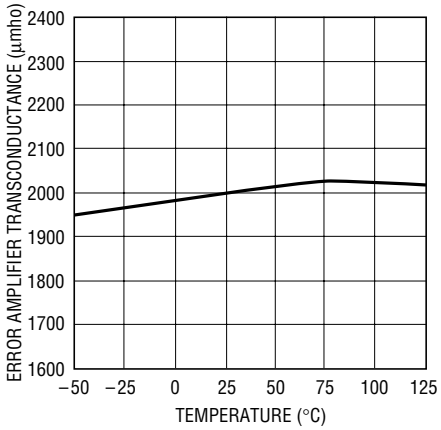
Load Regulation



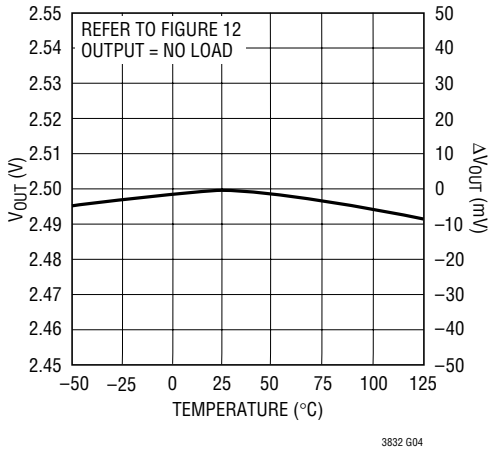
Line Regulation



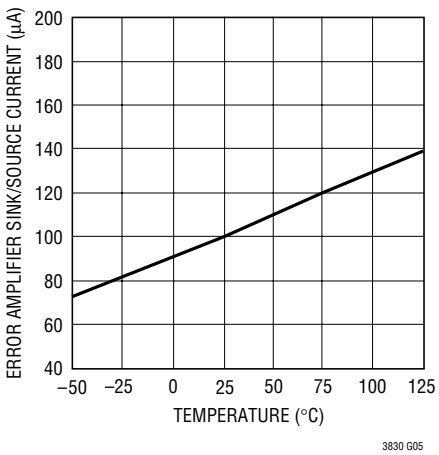
Error Amplifier Transconductance vs Temperature



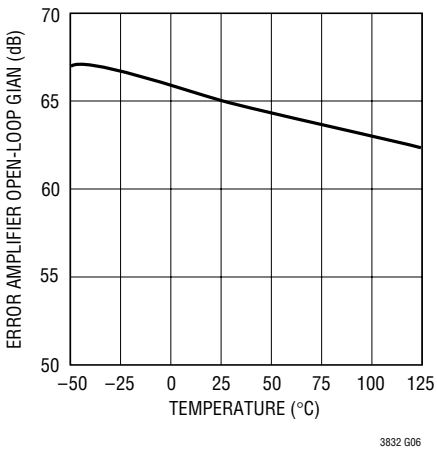
Output Voltage Temperature Drift



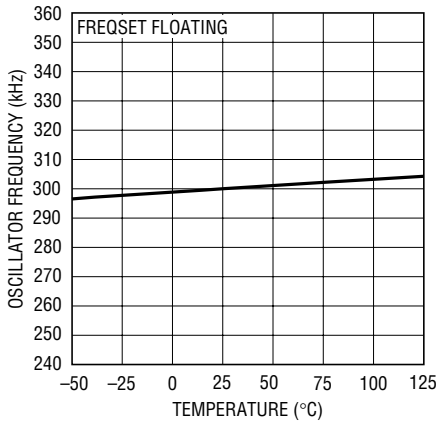
Error Amplifier Sink/Source Current vs Temperature



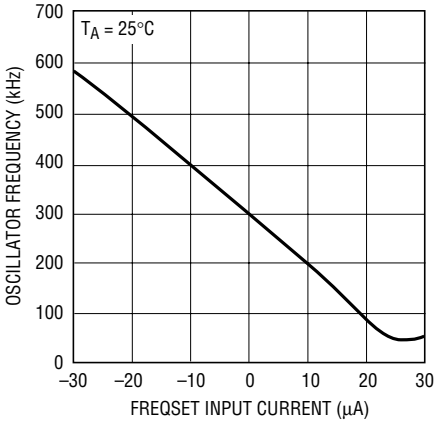
Error Amplifier Open-Loop Gain vs Temperature



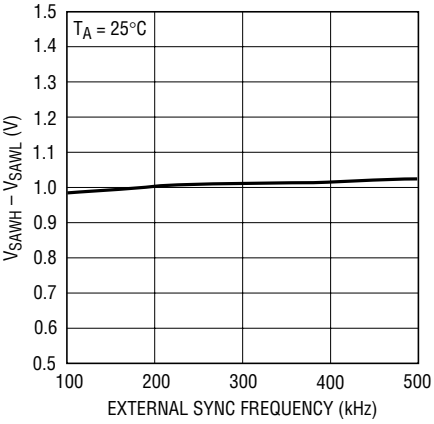
Oscillator Frequency vs Temperature



Oscillator Frequency vs FREQSET Input Current

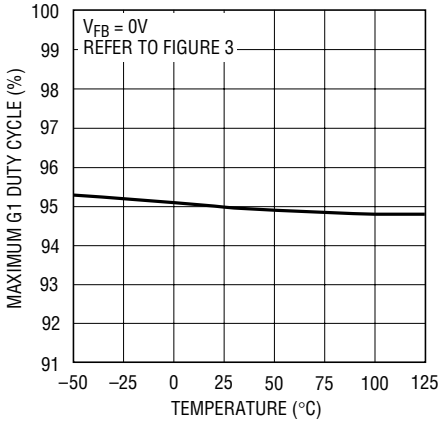


Oscillator (V_{SAWH} – V_{SAWL}) vs External Sync Frequency

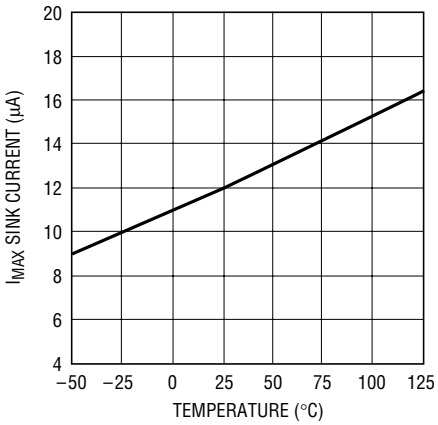


TYPICAL PERFORMANCE CHARACTERISTICS

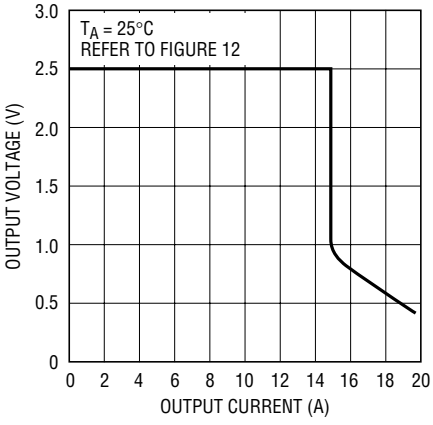
Maximum G1 Duty Cycle vs Temperature



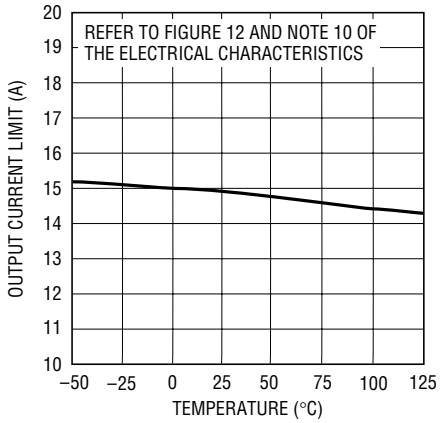
I_{MAX} Sink Current vs Temperature



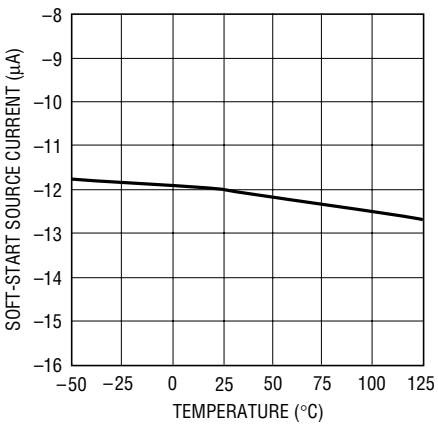
Output Overcurrent Protection



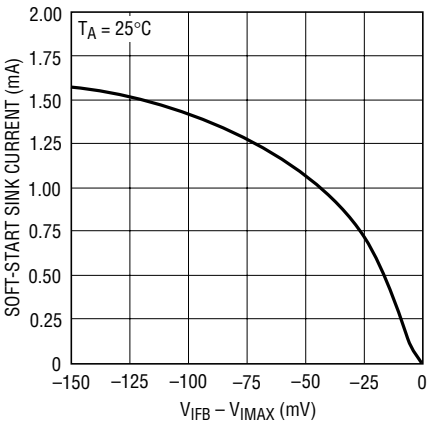
Output Current Limit Threshold vs Temperature



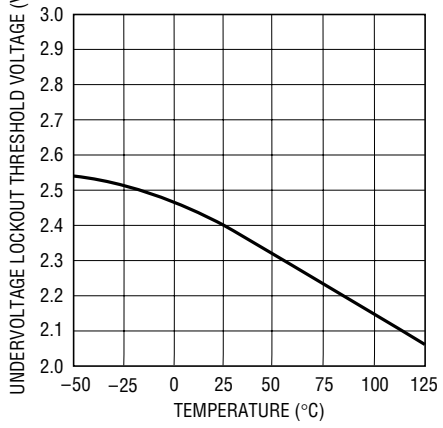
Soft-Start Source Current vs Temperature



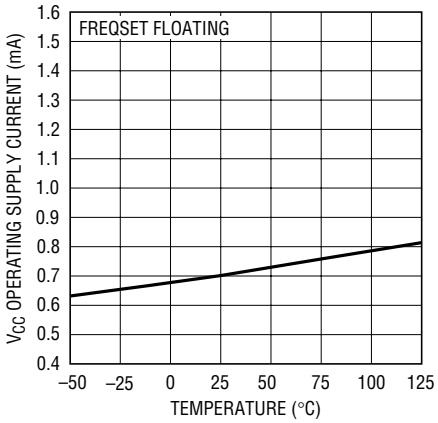
Soft-Start Sink Current vs ($V_{IFB} – V_{IMAX}$)



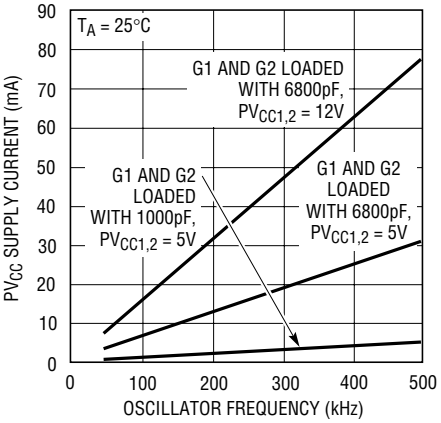
Undervoltage Lockout Threshold Voltage vs Temperature



V_{CC} Operating Supply Current vs Temperature

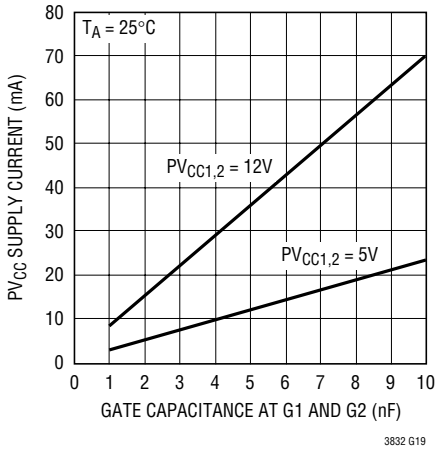


PV_{CC} Supply Current vs Oscillator Frequency

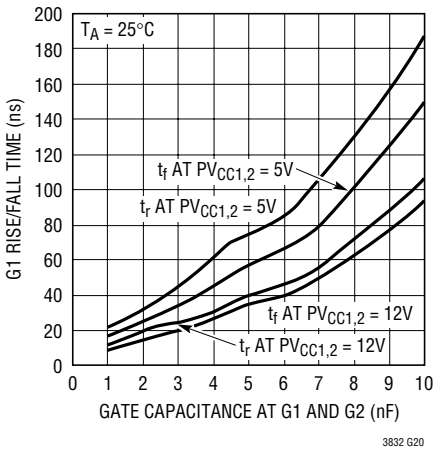


TYPICAL PERFORMANCE CHARACTERISTICS

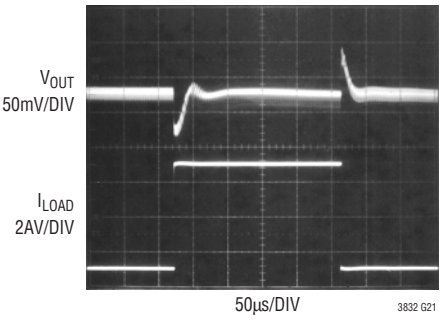
PV_{CC} Supply Current vs Gate Capacitance



G1 Rise/Fall Time vs Gate Capacitance



Transient Response



PIN FUNCTIONS (LTC3832/LTC3832-1)

G1 (Pin 1/Pin 1): Top Gate Driver Output. Connect this pin to the gate of the upper N-channel MOSFET, Q1. This output swings from PGND to PV_{CC1}. It remains low if G2 is high or during shutdown mode.

PV_{CC1} (Pin 2/Pin 2): Power Supply Input for G1. Connect this pin to a potential of at least $V_{IN} + V_{GS(ON)(Q1)}$. This potential can be generated using an external supply or charge pump.

PGND (Pin 3/Pin 3): Power Ground. Both drivers return to this pin. Connect this pin to a low impedance ground in close proximity to the source of Q2. Refer to the Layout Consideration section for more details on PCB layout techniques. The LTC3832-1 has PGND and GND tied together internally at Pin 3.

GND (Pin 4/Pin 3): Signal Ground. All low power internal circuitry returns to this pin. To minimize regulation errors due to ground currents, connect GND to PGND right at the LTC3832.

$SENSE^-$, FB, $SENSE^+$ (Pins 5, 6, 7/Pin 4): These three pins connect to the internal resistor divider and input of the error amplifier. To use the internal divider to set the output voltage to 2.5V, connect $SENSE^+$ to the positive terminal of the output capacitor and $SENSE^-$ to the negative terminal. FB should be left floating. To use an external resistor divider to set the output voltage, float $SENSE^+$ and $SENSE^-$ and connect the external resistor divider to FB. The internal resistor divider is not included in the LTC3832-1.

$\overline{SHDN}$ (Pin 8/NA): Shutdown. A TTL compatible low level at $\overline{SHDN}$ for longer than 100µs puts the LTC3832 into shutdown mode. In shutdown, G1 and G2 go low, all internal circuits are disabled and the quiescent current drops to 10µA max. A TTL compatible high level at $\overline{SHDN}$ allows the part to operate normally. This pin also doubles as an external clock input to synchronize the internal oscillator with an external clock. The shutdown function is disabled in the LTC3832-1.

SS (Pin 9/Pin 5): Soft-Start. Connect this pin to an external capacitor, C_{SS}, to implement a soft-start function. If the LTC3832 goes into current limit, C_{SS} is discharged to reduce the duty cycle. C_{SS} must be selected such that during power-up, the current through Q1 will not exceed the current limit level.

COMP (Pin 10/Pin 6): External Compensation. This pin internally connects to the output of the error amplifier and input of the PWM comparator. Use a RC + C network at this pin to compensate the feedback loop to provide optimum transient response.

PIN FUNCTIONS

FREQSET (Pin 11/NA): Frequency Set. Use this pin to adjust the free-running frequency of the internal oscillator. With the pin floating, the oscillator runs at about 300kHz. A resistor from FREQSET to ground speeds up the oscillator; a resistor to V_{CC} slows it down.

I_{MAX} (Pin 12/NA): Current Limit Threshold Set. I_{MAX} sets the threshold for the internal current limit comparator. If I_{FB} drops below I_{MAX} with G1 on, the LTC3832 goes into current limit. I_{MAX} has an internal 12µA pull-down to GND. Connect this pin to the main V_{IN} supply at the drain of Q1, through an external resistor to set the current limit threshold. Connect a 0.1µF decoupling capacitor across this resistor to filter switching noise.

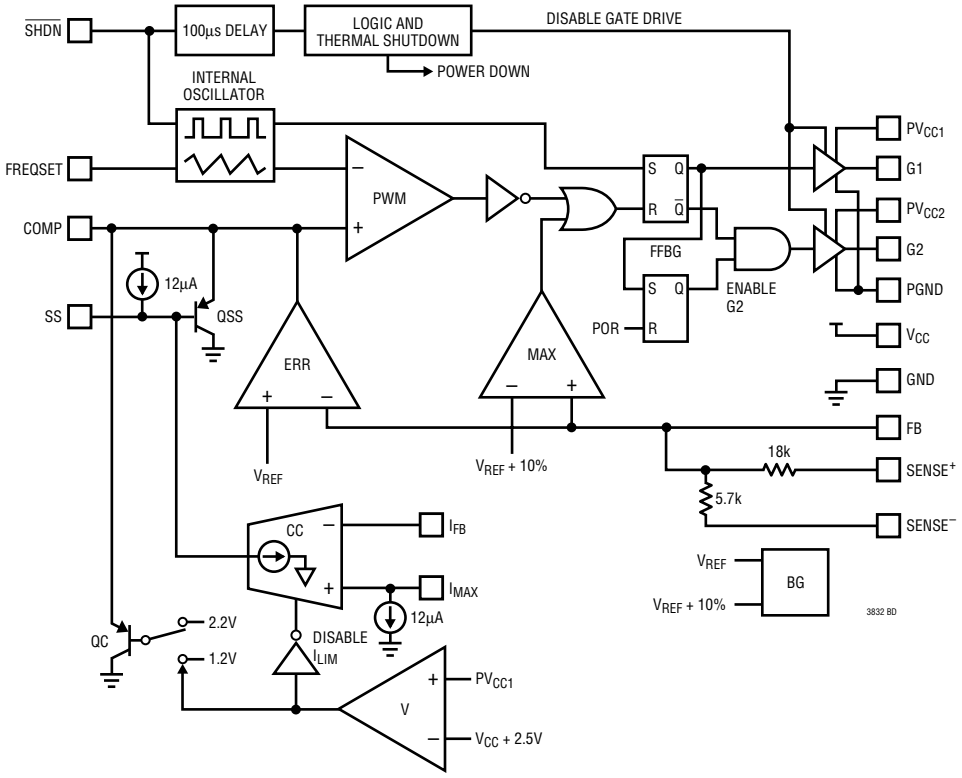
I_{FB} (Pin 13/NA): Current Limit Sense. Connect this pin to the switching node at the source of Q1 and the drain of Q2 through a 1k resistor. The 1k resistor is required to prevent voltage transients from damaging I_{FB}.This pin is used for sensing the voltage drop across the upper N-channel MOSFET, Q1.

V_{CC} (Pin 14/Pin 7): Power Supply Input. All low power internal circuits draw their supply from this pin. Connect this pin to a clean power supply, separate from the main V_{IN} supply at the drain of Q1. This pin requires a 4.7µF bypass capacitor. The LTC3832-1has V_{CC} and PV_{CC2} tied together at Pin 7 and requires a 10µF bypass capacitor to GND.

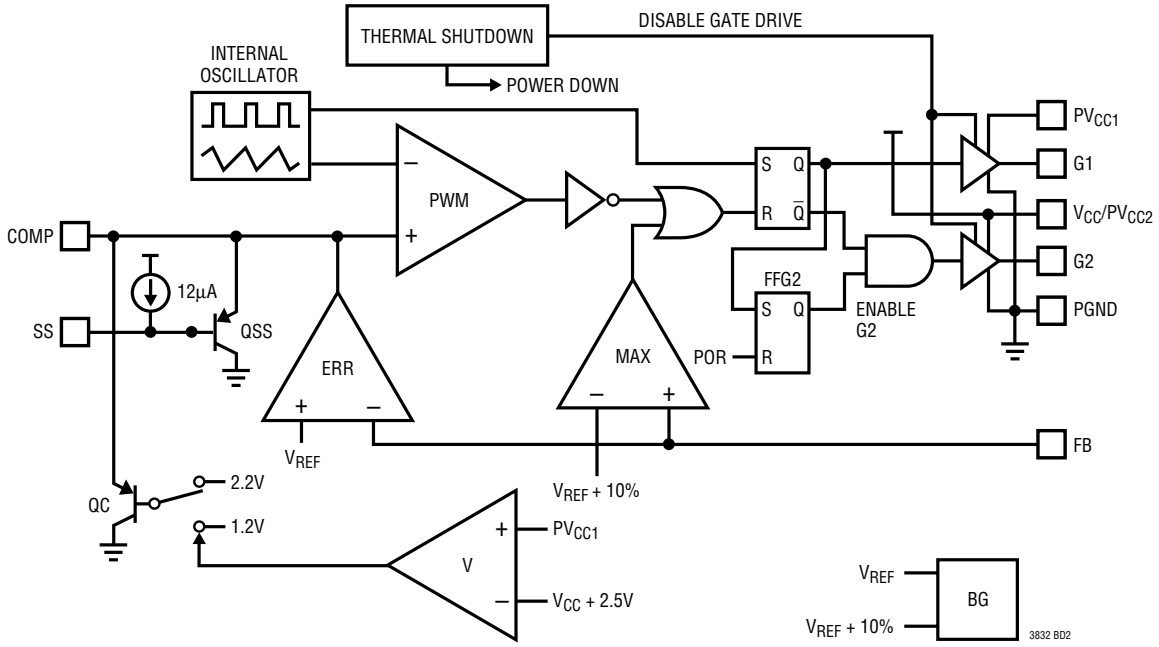
PV_{CC2} (Pin 15/Pin 7): Power Supply Input for G2. Connect this pin to the main high power supply.

G2 (Pin 16/Pin 8): Bottom Gate Driver Output. Connect this pin to the gate of the lower N-channel MOSFET, Q2. This output swings from PGND to PV_{CC2}. It remains low when G1 is high or during shutdown mode. To prevent output undershoot during a soft-start cycle, G2 is held low until G1 first goes high (FFBG in the Block Diagram).

BLOCK DIAGRAM (LTC3832)



BLOCK DIAGRAM (LTC3832-1)



TEST CIRCUITS

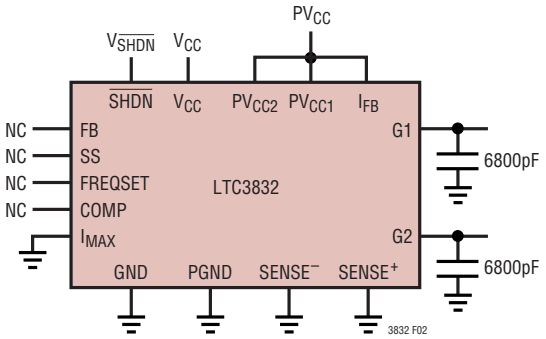


Figure 2

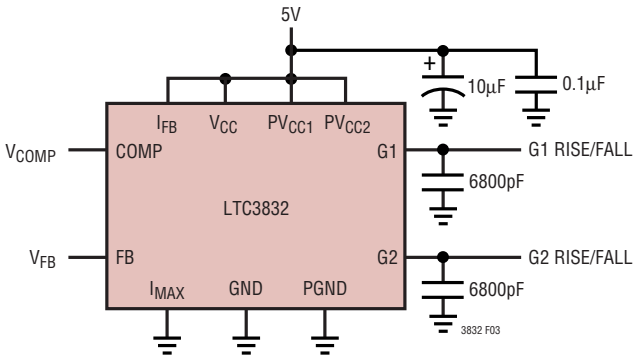


Figure 3

APPLICATIONS INFORMATION

OVERVIEW

The LTC3832/LTC3832-1 are voltage mode feedback, synchronous switching regulator controllers (see Block Diagram) designed for use in high power, low voltage step-down (buck) converters. They include an onboard PWM generator, a precision reference trimmed to ±0.8%, two high power MOSFET gate drivers and all necessary feedback and control circuitry to form a complete switching regulator circuit. The PWM loop nominally runs at 300kHz.

The LTC3832 includes a current limit sensing circuit that uses the topside external N-channel power MOSFET as a current sensing element, eliminating the need for an external sense resistor.

APPLICATIONS INFORMATION

Also included in the LTC3832 is an internal soft-start feature that requires only a single external capacitor to operate. In addition, the LTC3832 features an adjustable oscillator that can free run or synchronize to external signal with frequencies from 100kHz to 500kHz, allowing added flexibility in external component selection. The LTC3832-1 does not include current limit, frequency adjustability, external synchronization and the shutdown function.

THEORY OF OPERATION

Primary Feedback Loop

The LTC3832/LTC3832-1 sense the output voltage of the circuit at the output capacitor and feeds this voltage back to the internal transconductance error amplifier, ERR, through a resistor divider network. The error amplifier compares the resistor-divided output voltage to the internal 0.6V reference and outputs an error signal to the PWM comparator. This error signal is compared with a fixed frequency ramp waveform, from the internal oscillator, to generate a pulse width modulated signal. This PWM signal drives the external MOSFETs through the G1 and G2 pins. The resulting chopped waveform is filtered by L_O and C_{OUT} which closes the loop. Loop compensation is achieved with an external compensation network at the COMP pin, the output node of the error amplifier.

MAX Feedback Loop

An additional comparator in the feedback loop provides high speed output voltage correction in situations where the error amplifier may not respond quickly enough. MAX compares the feedback signal to a voltage 60mV above the internal reference. If the signal is above the comparator threshold, the MAX comparator overrides the error amplifier and forces the loop to minimum duty cycle, 0%. To prevent this comparator from triggering due to noise, the MAX comparator's response time is deliberately delayed by two to three microseconds. This comparator helps prevent extreme output perturbations with fast output load current transients, while allowing the main feedback loop to be optimally compensated for stability.

Thermal Shutdown

The LTC3832/LTC3832-1 have a thermal protection circuit that disables both gate drivers if activated. If the chip junction temperature reaches 150°C, both G1 and G2 are pulled low. G1 and G2 remain low until the junction temperature drops below 125°C, after which, the chip resumes normal operation.

Soft-Start and Current Limit

The LTC3832 includes a soft-start circuit that is used for start-up and current limit operation. The LTC3832-1 only has the soft-start function; the current limit function is disabled. The SS pin requires an external capacitor, C_{SS}, to GND with the value determined by the required soft-start time. An internal 12μA current source is included to charge C_{SS}. During power-up, the COMP pin is clamped to a diode drop (B-E junction of QSS in the Block Diagram) above the voltage at the SS pin. This prevents the error amplifier from forcing the loop to maximum duty cycle. The LTC3832/LTC3832-1 operate at low duty cycle as the SS pin rises above 0.6V ($V_{COMP} \approx 1.2V$). As SS continues to rise, QSS turns off and the error amplifier takes over to regulate the output.

The LTC3832 includes yet another feedback loop to control operation in current limit. Just before every falling edge of G1, the current comparator, CC, samples and holds the voltage drop measured across the external upper MOSFET, Q1, at the I_{FB} pin. CC compares the voltage at I_{FB} to the voltage at the I_{MAX} pin. As the peak current rises, the measured voltage across Q1 increases due to the drop across the $R_{DS(ON)}$ of Q1. When the voltage at I_{FB} drops below I_{MAX}, indicating that Q1's drain current has exceeded the maximum level, CC starts to pull current out of C_{SS}, cutting the duty cycle and controlling the output current level. The CC comparator pulls current out of the SS pin in proportion to the voltage difference between I_{FB} and I_{MAX}. Under minor overload conditions, the SS pin falls gradually, creating a time delay before current limit takes effect. Very short, mild overloads may not affect the output voltage at all. More significant overload conditions allow the SS pin to reach a steady state, and the output

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remains at a reduced voltage until the overload is removed. Serious overloads generate a large overdrive at CC, allowing it to pull SS down quickly and preventing damage to the output components. By using the $R_{DS(ON)}$ of Q1 to measure the output current, the current limiting circuit eliminates an expensive discrete sense resistor that would otherwise be required. This helps minimize the number of components in the high current path.

The current limit threshold can be set by connecting an external resistor R_{IMAX} from the I_{MAX} pin to the main V_{IN} supply at the drain of Q1. The value of R_{IMAX} is determined by:

$$R_{IMAX} = (I_{LMAX})(R_{DS(ON)Q1})/I_{IMAX}$$

where:

$I_{LMAX} = I_{LOAD} + (I_{RIPPLE}/2)$

I_{LOAD} = Maximum load current

I_{RIPPLE} = Inductor ripple current

$$= \frac{(V_{IN} - V_{OUT})(V_{OUT})}{(f_{OSC})(L_O)(V_{IN})}$$

f_{OSC} = LTC3832 oscillator frequency = 300kHz

L_O = Inductor value

$R_{DS(ON)Q1}$ = On-resistance of Q1 at I_{LMAX}

I_{IMAX} = Internal 12µA sink current at I_{MAX}

The $R_{DS(ON)}$ of Q1 usually increases with temperature. To keep the current limit threshold constant, the internal 12µA sink current at I_{MAX} is designed with a positive temperature coefficient to provide first order correction for the temperature coefficient of $R_{DS(ON)Q1}$.

In order for the current limit circuit to operate properly and to obtain a reasonably accurate current limit threshold, the I_{IMAX} and I_{FB} pins must be Kelvin sensed at Q1's drain and source pins. In addition, connect a 0.1µF decoupling capacitor across R_{IMAX} to filter switching noise. Otherwise, noise spikes or ringing at Q1's source can cause the actual maximum current to be greater than the desired current limit set point. Due to switching noise and variation of $R_{DS(ON)}$, the actual current limit trip point is not highly accurate. The current limiting circuitry is primarily meant to prevent damage to the power supply circuitry during fault conditions. The exact current level where the limiting circuit begins to take effect will vary from unit to unit as the $R_{DS(ON)}$ of Q1 varies. Typically, $R_{DS(ON)}$ varies as much as ±40%, and with ±33% variation on the LTC3832's I_{MAX} current, this can give a ±73% variation on the current limit threshold.

The $R_{DS(ON)}$ is high if the V_{GS} applied to the MOSFET is low. This occurs during power up when PV_{CC1} is ramping up. To prevent the high $R_{DS(ON)}$ from activating the current limit, the LTC3832 will disable the current limit circuit if PV_{CC1} is less than 2.5V above V_{CC}. To ensure proper operation of the current limit circuit, PV_{CC1} must be at least 2.5V above V_{CC} when G1 is high. PV_{CC1} can go low when G1 is low, allowing the use of the external charge pump to power PV_{CC1}.

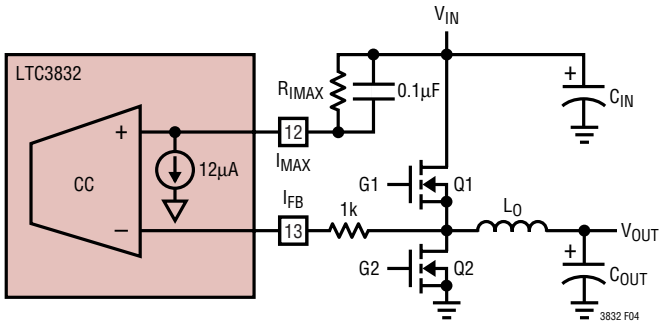

Figure 4. Current Limit Setting

Oscillator Frequency

The LTC3832 includes an onboard current controlled oscillator that typically free-runs at 300kHz. The oscillator frequency can be adjusted by forcing current into or out of the FREQSET pin. With the pin floating, the oscillator runs at about 300kHz. Every additional 1µA of current into/out of the FREQSET pin decreases/increases the frequency by 10kHz. The pin is internally servoed to 1.265V. The frequency can be estimated as:

$$f = 300kHz + \frac{1.265V - V_{EXT}}{R_{FSET}} \bullet \frac{10kHz}{1\mu A}$$

where R_{FSET} is a frequency programming resistor connected between FREQSET and the external voltage source V_{EXT}.

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Connecting a 82k resistor from FREQSET to ground forces 15μA out of the pin, causing the internal oscillator to run at approximately 450kHz. Forcing an external 20μA current into FREQSET cuts the internal frequency to 100kHz. An internal clamp prevents the oscillator from running slower than about 50kHz. Tying FREQSET to V_{CC} forces the chip to run at this minimum speed. The LTC3832-1 does not have this frequency adjustment function.

Shutdown

The LTC3832 includes a low power shutdown mode, controlled by the logic at the $\overline{SHDN}$ pin. A high at $\overline{SHDN}$ allows the part to operate normally. A low level at $\overline{SHDN}$ for more than 100μs forces the LTC3832 into shutdown mode. In this mode, all internal switching stops, the COMP and SS pins pull to ground and Q1 and Q2 turn off. The LTC3832 supply current drops to <10μA, although off-state leakage in the external MOSFETs may cause the total V_{IN} current to be some what higher, especially at elevated temperatures. If $\overline{SHDN}$ returns high, the LTC3832 reruns a soft-start cycle and resumes normal operation. The LTC3832-1 does not have this shutdown function.

External Clock Synchronization

The LTC3832 $\overline{SHDN}$ pin doubles as an external clock input for applications that require a synchronized clock. An internal circuit forces the LTC3832 into external synchronization mode if a negative transition at the $\overline{SHDN}$ pin is detected. In this mode, every negative transition on the $\overline{SHDN}$ pin resets the internal oscillator and pulls the ramp signal low, this forces the LTC3832 internal oscillator to lock to the external clock frequency. The LTC3832-1 does not have this external synchronization function.

The LTC3832 internal oscillator can be externally synchronized from 100kHz to 500kHz. Frequencies above 300kHz can cause a decrease in the maximum obtainable duty cycle as rise/fall time and propagation delay take up a larger percentage of the switch cycle. Circuits using these frequencies should be checked carefully in applications where operation near dropout is important—like 3.3V to 2.5V converters. The low period of this clock signal must not be >100μs, or else the LTC3832 enters shutdown mode.

Figure 5 describes the operation of the conventional synchronization function. A negative transition at the $\overline{SHDN}$ pin forces the internal ramp signal low to restart a new PWM cycle. Notice that the ramp amplitude is lowered as the external clock frequency goes higher. The effect of this decrease in ramp amplitude increases the open-loop gain of the controller feedback loop. As a result, the loop crossover frequency increases and it may cause the feedback loop to be unstable if the phase margin is insufficient.

To overcome this problem, the LTC3832 monitors the peak voltage of the ramp signal and adjusts the oscillator charging current to maintain a constant ramp peak.

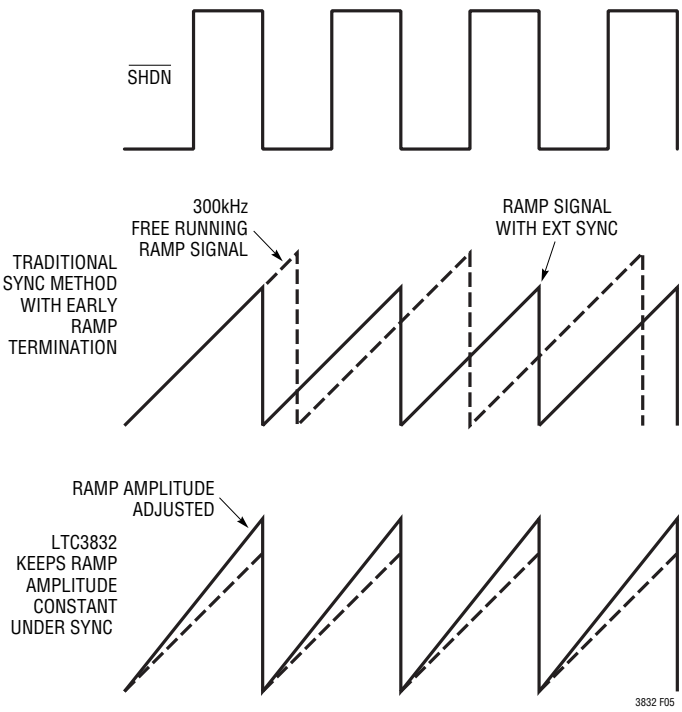

Figure 5. External Synchronization Operation

Input Supply Considerations/Charge Pump

The LTC3832 requires four supply voltages to operate: V_{IN} for the main power input, PV_{CC1} and PV_{CC2} for MOSFET gate drive and a clean, low ripple V_{CC} for the LTC3832 internal circuitry (Figure 6). The LTC3832-1 has the PV_{CC2} and V_{CC} pins tied together inside the package (Figure 7). This pin, brought out as V_{CC}/PV_{CC2}, has the same low ripple requirements as the LTC3832, but must also be able to supply the gate drive current to Q2.

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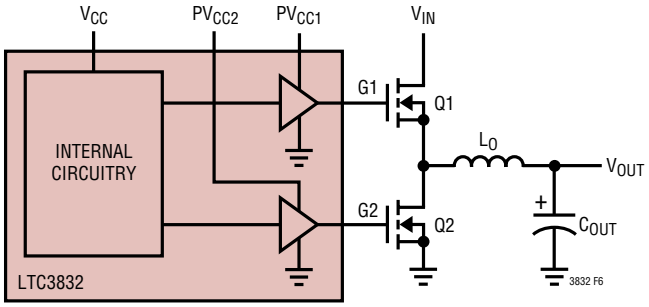

Figure 6. LTC3832 Power Supplies

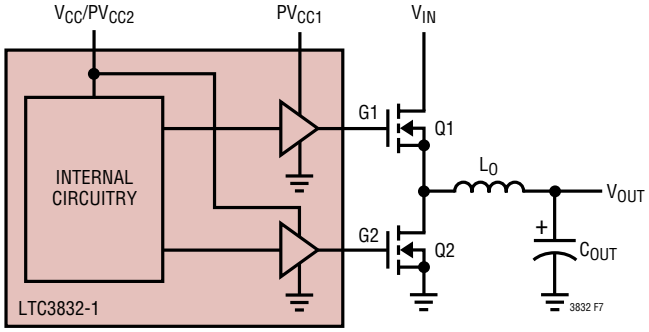

Figure 7. LTC3832-1 Power Supplies

In many applications, V_{CC} can be powered from V_{IN} through an RC filter. This supply can be as low as 3V. The low quiescent current (typically 800µA) allows the use of relatively large filter resistors and correspondingly small filter capacitors. 100Ω and 4.7µF usually provide adequate filtering for V_{CC}. For best performance, connect the 4.7µF bypass capacitor as close to the LTC3832 V_{CC} pin as possible.

Gate drive for the top N-channel MOSFET Q1 is supplied from PV_{CC1}. This supply must be above V_{IN} (the main power supply input) by at least one power MOSFET $V_{GS(ON)}$ for efficient operation. An internal level shifter allows PV_{CC1} to operate at voltages above V_{CC} and V_{IN}, up to 14V maximum. This higher voltage can be supplied with a separate supply, or it can be generated using a charge pump.

Gate drive for the bottom MOSFET Q2 is provided through PV_{CC2} for the LTC3832 or V_{CC}/PV_{CC2} for the LTC3832-1. This supply only needs to be above the power MOSFET $V_{GS(ON)}$ for efficient operation. PV_{CC2} can also be driven from the same supply/charge pump for the PV_{CC1}, or it can be connected to a lower supply to improve efficiency.

Figure 8 shows a tripling charge pump circuit that can be used to provide $2V_{IN}$ and $3V_{IN}$ gate drive for the external top and bottom MOSFETs respectively. These should fully enhance MOSFETs with 5V logic level thresholds. This circuit provides $3V_{IN} – 3V_F$ to PV_{CC1} while Q1 is ON and $2V_{IN} – 2V_F$ to PV_{CC2} where V_F is the forward voltage of the Schottky diodes. The circuit requires the use of Schottky diodes to minimize forward drop across the diodes at start-up. The tripling charge pump circuit can rectify any ringing at the drain of Q2 and provide more than $3V_{IN}$ at PV_{CC1}; a 12V zener diode should be included from PV_{CC1} to PGND to prevent transients from damaging the circuitry at PV_{CC1} or the gate of Q1.

The charge pump capacitors for PV_{CC1} refresh when the G2 pin goes high and the switch node is pulled low by Q2. The G2 on-time becomes narrow when LTC3832/LTC3832-1 operates at a maximum duty cycle (95% typical), which can occur if the input supply rises more slowly than the soft-start capacitor or if the input voltage droops during load transients. If the G2 on-time gets so narrow that the switch node fails to pull completely to ground, the charge pump voltage may collapse or fail to start, causing excessive dissipation in external MOSFET, Q1. This condition is most likely with low V_{CC} voltages and high switching frequencies, coupled with large external MOSFETs which slow the G2 and switch node slew rates.

The LTC3832/LTC3832-1 overcome this problem by sensing the PV_{CC1} voltage when G1 is high. If PV_{CC1} is less than 2.5V above V_{CC}, the maximum G1 duty cycle is reduced to 70% by clamping the COMP pin at 1.8V (QC in the Block

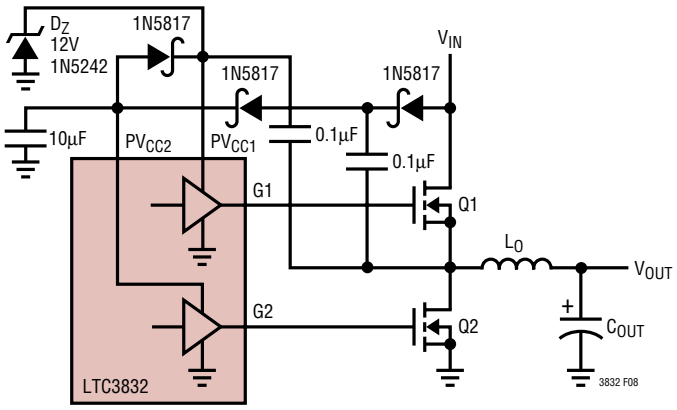

Figure 8. Tripling Charge Pump

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Diagram). This increases the G2 on-time and allows the charge pump capacitors to be refreshed.

For applications using an external supply to PV_{CC1}, this supply must also be higher than V_{CC} by at least 2.5V to ensure normal operation.

For applications with a 5V or higher V_{IN} supply, PV_{CC2} can be tied to V_{IN} if a logic level MOSFET is used. PV_{CC1} can be supplied using a doubling charge pump as shown in Figure 9. This circuit provides $2V_{IN} – V_F$ to PV_{CC1} while Q1 is ON.

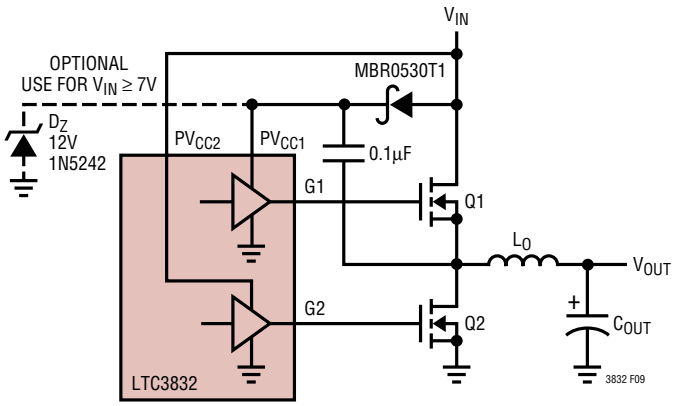

Figure 9. Doubling Charge Pump

Power MOSFETs

Two N-channel power MOSFETs are required for most LTC3832 circuits. These should be selected based primarily on threshold voltage and on-resistance considerations. Thermal dissipation is often a secondary concern in high efficiency designs. The required MOSFET threshold should be determined based on the available power supply voltages and/or the complexity of the gate drive charge pump scheme. In 3.3V input designs where an auxiliary 12V supply is available to power PV_{CC1} and PV_{CC2}, standard MOSFETs with $R_{DS(ON)}$ specified at V_{GS} = 5V or 6V can be used with good results. The current drawn from this supply varies with the MOSFETs used and the LTC3832's operating frequency, but is generally less than 50mA.

LTC3832 applications that use 5V or lower V_{IN} voltage and a doubling/tripling charge pump to generate PV_{CC1} and PV_{CC2}, do not provide enough gate drive voltage to fully enhance standard power MOSFETs. Under this condition, the effective MOSFET $R_{DS(ON)}$ may be quite high, raising the dissipation in the FETs and reducing efficiency. Logic level FETs are the recommended choice for 5V or lower voltage systems. Logic level FETs can be fully enhanced with a doubler/tripling charge pump and will operate at maximum efficiency.

After the MOSFET threshold voltage is selected, choose the $R_{DS(ON)}$ based on the input voltage, the output voltage, allowable power dissipation and maximum output current. In a typical LTC3832 circuit, operating in continuous mode, the average inductor current is equal to the output load current. This current flows through either Q1 or Q2 with the power dissipation split up according to the duty cycle:

$$DC(Q1) = \frac{V_{OUT}}{V_{IN}}$$

$$DC(Q2) = 1 - \frac{V_{OUT}}{V_{IN}} = \frac{V_{IN} - V_{OUT}}{V_{IN}}$$

The $R_{DS(ON)}$ required for a given conduction loss can now be calculated by rearranging the relation $P = I^2R$.

$$R_{DS(ON)Q1} = \frac{P_{MAX(Q1)}}{DC(Q1) \bullet (I_{LOAD})^2} = \frac{V_{IN} \bullet P_{MAX(Q1)}}{V_{OUT} \bullet (I_{LOAD})^2}$$

$$R_{DS(ON)Q2} = \frac{P_{MAX(Q2)}}{DC(Q2) \bullet (I_{LOAD})^2} = \frac{V_{IN} \bullet P_{MAX(Q2)}}{(V_{IN} - V_{OUT}) \bullet (I_{LOAD})^2}$$

P_{MAX} should be calculated based primarily on required efficiency or allowable thermal dissipation. A typical high efficiency circuit designed for 3.3V input and 2.5V at 10A output might allow no more than 3% efficiency loss at full load for each MOSFET. Assuming roughly 90% efficiency at this current level, this gives a P_{MAX} value of:

(2.5V)(10A/0.9)(0.03) = 0.83W per FET

and a required $R_{DS(ON)}$ of:

$$R_{DS(ON)Q1} = \frac{(3.3V) \bullet (0.83W)}{(2.5V)(10A)^2} = 0.011\Omega$$

$$R_{DS(ON)Q2} = \frac{(3.3V) \bullet (0.83W)}{(3.3V - 2.5V)(10A)^2} = 0.034\Omega$$

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Note that the required $R_{DS(ON)}$ for Q2 is roughly three times that of Q1 in this example. Note also that while the required $R_{DS(ON)}$ values suggest large MOSFETs, the power dissipation numbers are only 0.83W per device or less; large TO-220 packages and heat sinks are not necessarily required in high efficiency applications. Siliconix Si4410DY or International Rectifier IRF7413 (both in SO-8) or Siliconix SUD50N03-10 (TO-252) or ON Semiconductor MTD20N03HDL (DPAK) are small footprint surface mount devices with $R_{DS(ON)}$ values below 0.03Ω at 5V of V_{GS} that work well in LTC3832 circuits. Using a higher P_{MAX} value in the $R_{DS(ON)}$ calculations generally decreases the MOSFET cost and the circuit efficiency and increases the MOSFET heat sink requirements.

Table 1 highlights a variety of power MOSFETs for use in LTC3832 applications.

Inductor Selection

The inductor is often the largest component in an LTC3832 design and must be chosen carefully. Choose the inductor value and type based on output slew rate requirements. The maximum rate of rise of inductor current is set by the inductor's value, the input-to-output voltage differential and the LTC3832's maximum duty cycle. In a typical 3.3V input, 2.5V output application, the maximum rise time will be:

$$\frac{DC_{MAX} \bullet (V_{IN} - V_{OUT})}{L_O} = \frac{0.76}{L_O} \frac{A}{\mu s}$$

where L_O is the inductor value in µH. With proper frequency compensation, the combination of the inductor and output capacitor values determine the transient recovery time. In general, a smaller value inductor improves transient response at the expense of ripple and inductor core saturation rating. A 1µH inductor has a 0.76A/µs rise time in this application, resulting in a 6.6µs delay in responding to a 5A load current step. During this 6.6µs, the difference between the inductor current and the output current is made up by the output capacitor. This action causes a temporary voltage droop at the output. To minimize this effect, the inductor value should usually be in the 1µH to 5µH range for most 3.3V input LTC3832 circuits. To optimize performance, different combinations of input and output voltages and expected loads may require different inductor values.

Once the required value is known, the inductor core type can be chosen based on peak current and efficiency

Table 1. Recommended MOSFETs for LTC3832 Applications

PARTS	$R_{DS(ON)}$ AT 25°C (mΩ)	RATED CURRENT (A)	TYPICAL INPUT CAPACITANCE C_{ISS} (pF)	θ_{JC} (°C/W)	T_{JMAX} (°C)
Siliconix SUD50N03-10 TO-252	19	15 at 25°C 10 at 100°C	3200	1.8	175
Siliconix Si4410DY SO-8	20	10 at 25°C 8 at 70°C	2700		150
ON Semiconductor MTD20N03HDL DPAK	35	20 at 25°C 16 at 100°C	880	1.67	150
Fairchild FDS6670A SO-8	8	13 at 25°C	3200	25	150
Fairchild FDS6680 SO-8	10	11.5 at 25°C	2070	25	150
ON Semiconductor MTB75N03HDL DD PAK	9	75 at 25°C 59 at 100°C	4025	1	150
IR IRL3103S DD PAK	19	64 at 25°C 45 at 100°C	1600	1.4	175
IR IRLZ44 TO-220	28	50 at 25°C 36 at 100°C	3300	1	175
Fuji 2SK1388 TO-220	37	35 at 25°C	1750	2.08	150

Note: Please refer to the manufacturer's data sheet for testing conditions and detailed information.

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requirements. Peak current in the inductor will be equal to the maximum output load current plus half of the peak-to-peak inductor ripple current. Ripple current is set by the inductor value, the input and output voltage and the operating frequency. The ripple current is approximately equal to:

$$I_{RIPPLE} = \frac{(V_{IN} - V_{OUT}) \bullet (V_{OUT})}{f_{OSC} \bullet L_O \bullet V_{IN}}$$

f_{OSC} = LTC3832 oscillator frequency = 300kHz

L_O = Inductor value

Solving this equation with our typical 3.3V to 2.5V application with a 1µH inductor, we get:

$$\frac{(3.3V - 2.5V) \bullet 2.5V}{300kHz \bullet 1\mu H \bullet 3.3V} = 2A_{P-P}$$

Peak inductor current at 10A load:

10A + (2A/2) = 11A

The ripple current should generally be between 10% and 40% of the output current. The inductor must be able to withstand this peak current without saturating, and the copper resistance in the winding should be kept as low as possible to minimize resistive power loss. Note that in circuits not employing the current limit function, the current in the inductor may rise above this maximum under short-circuit or fault conditions; the inductor should be sized accordingly to withstand this additional current. Inductors with gradual saturation characteristics are often the best choice.

Input and Output Capacitors

A typical LTC3832 design places significant demands on both the input and the output capacitors. During normal steady load operation, a buck converter like the LTC3832 draws square waves of current from the input supply at the switching frequency. The peak current value is equal to the output load current plus 1/2 the peak-to-peak ripple current. Most of this current is supplied by the input bypass capacitor. The resulting RMS current flow in the input capacitor heats it and causes premature capacitor failure in extreme cases. Maximum RMS current occurs with 50% PWM duty cycle, giving an RMS current value equal to $I_{OUT}/2$. A low ESR input capacitor with an adequate ripple current rating must be used to ensure reliable operation. Note that capacitor manufacturers' ripple current ratings are often based on only 2000 hours (3 months) lifetime at rated temperature. Further derating of the input capacitor ripple current beyond the manufacturer's specification is recommended to extend the useful life of the circuit. Lower operating temperature has the largest effect on capacitor longevity.

The output capacitor in a buck converter under steady-state conditions sees much less ripple current than the input capacitor. Peak-to-peak current is equal to inductor ripple current, usually 10% to 40% of the total load current. Output capacitor duty places a premium not on power dissipation but on ESR. During an output load transient, the output capacitor must supply all of the additional load current demanded by the load until the LTC3832 adjusts the inductor current to the new value. ESR in the output capacitor results in a step in the output voltage equal to the ESR value multiplied by the change in load current. An 5A load step with a 0.05Ω ESR output capacitor results in a 250mV output voltage shift; this is 10% of the output voltage for a 2.5V supply! Because of the strong relationship between output capacitor ESR and output load transient response, choose the output capacitor for ESR, not for capacitance value. A capacitor with suitable ESR will usually have a larger capacitance value than is needed to control steady-state output ripple.

Electrolytic capacitors rated for use in switching power supplies with specified ripple current ratings and ESR can be used effectively in LTC3832 applications. OS-CON electrolytic capacitors from Sanyo and other manufacturers give excellent performance and have a very high performance/size ratio for electrolytic capacitors. Surface mount applications can use either electrolytic or dry tantalum capacitors. Tantalum capacitors must be surge tested and specified for use in switching power supplies. Low cost, generic tantalums are known to have very short lives followed by explosive deaths in switching power supply applications. Other capacitors that can be used include the Sanyo POSCAP and MV-WX series.

A common way to lower ESR and raise ripple current capability is to parallel several capacitors. A typical

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LTC3832 application might exhibit 5A input ripple current. Sanyo OS-CON capacitors, part number 10SA220M (220µF/10V), feature 2.3A allowable ripple current at 85°C; three in parallel at the input (to withstand the input ripple current) meet the above requirements. Similarly, Sanyo POSCAP 4TPB470M (470µF/4V) capacitors have a maximum rated ESR of 0.04Ω; three in parallel lower the net output capacitor ESR to 0.013Ω.

Feedback Loop Compensation

The LTC3832 voltage feedback loop is compensated at the COMP pin, which is the output node of the error amplifier. The feedback loop is generally compensated with an RC + C network from COMP to GND as shown in Figure 10a.

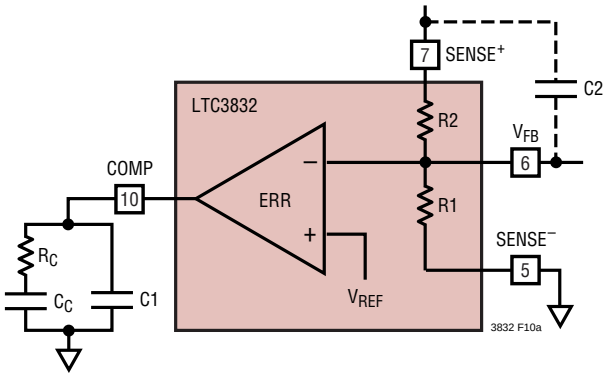

Figure 10a. Compensation Pin Hook-Up

Loop stability is affected by the values of the inductor, the output capacitor, the output capacitor ESR, the error amplifier transconductance and the error amplifier compensation network. The inductor and the output capacitor create a double pole at the frequency:

$$f_{LC} = 1/\left[2\pi\sqrt{(L_O)(C_{OUT})}\right]$$

The ESR of the output capacitor and the output capacitor value form a zero at the frequency:

$$f_{ESR} = 1/\left[2\pi(ESR)(C_{OUT})\right]$$

The compensation network used with the error amplifier must provide enough phase margin at the 0dB crossover frequency for the overall open-loop transfer function. The zero and pole from the compensation network are:

$f_Z = 1/[2\pi(R_C)(C_C)]$ and

$f_P = 1/[2\pi(R_C)(C1)]$ respectively

Figure 10b shows the Bode plot of the overall transfer function.

When low ESR output capacitors (Sanyo OS-CON) are used, the ESR zero can be high enough in frequency that it provides little phase boost at the loop crossover frequency. As a result, the phase margin becomes inadequate and the load transient is not optimized. To resolve this problem, a small capacitor can be connected

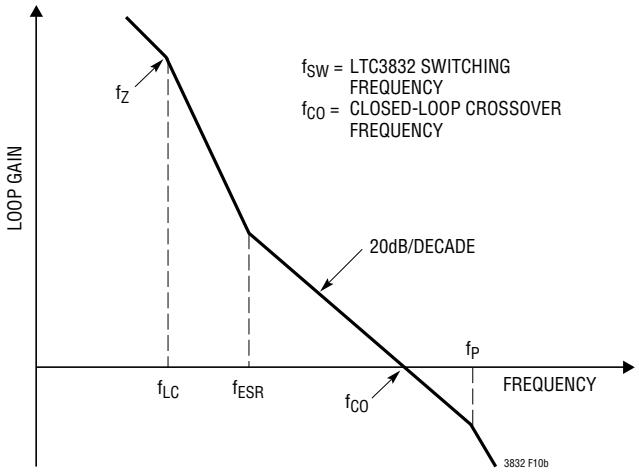

Figure 10b. Bode Plot of the LTC3832 Overall Transfer Function

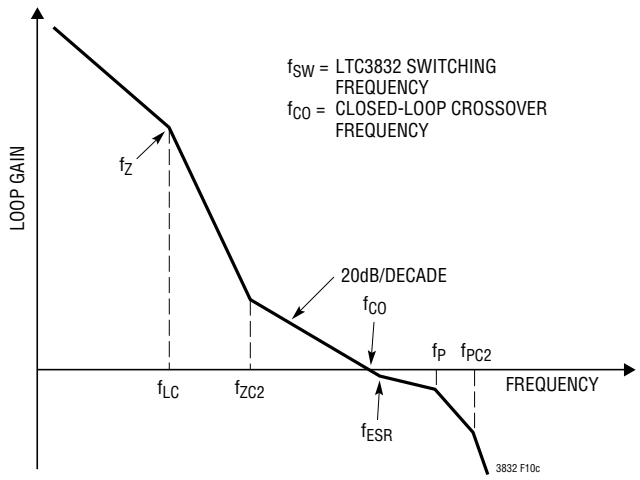

Figure 10c. Bode Plot of the LTC3832 Overall Transfer Function Using a Low ESR Output Capacitor

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between the top of the resistor divider network and the V_{FB} pin to create a pole-zero pair in the loop compensation. The zero location is prior to the pole location and thus, phase lead can be added to boost the phase margin at the loop crossover frequency. The pole and zero locations are located at:

$f_{ZC2} = 1/[2\pi(R2)(C2)]$ and

$f_{PC2} = 1/[2\pi(R1||R2)(C2)]$

where R1||R2 is the parallel combination resistance of R1 and R2. For low R2/R1 ratios there is not much separation between f_{CZ2} and f_{PC2}. In this case, use multiple capacitors with a high ESR • capacitance product to bring f_{ESR} close to f_{CO}. Choose C2 so that the zero is located at a lower frequency compared to f_{CO} and the pole location is high enough that the closed loop has enough phase margin for stability. Figure 10c shows the Bode plot using phase lead compensation around the LTC3832 resistor divider network.

Although a mathematical approach to frequency compensation can be used, the added complication of input and/or output filters, unknown capacitor ESR, and gross operating point changes with input voltage, load current variations, all suggest a more practical empirical method. This can be done by injecting a transient current at the load and using an RC network box to iterate toward the final values, or by obtaining the optimum loop response using a network analyzer to find the actual loop poles and zeros.

Table 2 shows the suggested compensation component value for 3.3V to 2.5V applications based on Sanyo OS-CON 4SP820M low ESR output capacitors.

Table 2. Recommended Compensation Network for 3.3V to 2.5V Applications Using Multiple Paralleled 820µF Sanyo OS-CON 4SP820M Output Capacitors

L1 (µH)	C_{OUT} (µF)	R_C (kΩ)	C_C (nF)	C1 (pF)	C2 (pF)
1.2	1640	9.1	4.7	560	1500
1.2	2460	15	4.7	330	1500
1.2	4100	24	3.3	270	1500
2.4	1640	22	4.7	330	1500
2.4	2460	33	3.3	220	1500
2.4	4100	43	2.2	180	1500
4.7	1640	33	3.3	120	1500
4.7	2460	56	2.2	100	1500
4.7	4100	91	2.2	100	1500

Table 3 shows the suggested compensation component values for 3.3V to 2.5V applications based on 470µF Sanyo POSCAP 4TPB470M output capacitors.

Table 3. Recommended Compensation Network for 3.3V to 2.5V Applications Using Multiple Paralleled 470µF Sanyo POSCAP 4TPB470M Output Capacitors

L1 (µH)	C_{OUT} (µF)	R_C (kΩ)	C_C (µF)	C1 (pF)
1.2	1410	13	0.0047	100
1.2	2820	27	0.0018	56
1.2	4700	51	0.0015	47
2.4	1410	33	0.0033	56
2.4	2820	62	0.0022	15
2.4	4700	82	0.001	39
4.7	1410	62	0.0022	15
4.7	2820	150	0.0015	10
4.7	4700	220	0.0015	2

Table 4 shows the suggested compensation component values for 3.3V to 2.5V applications based on 1500µF Sanyo MV-WX output capacitors.

Table 4. Recommended Compensation Network for 3.3V to 2.5V Applications Using Multiple Paralleled 1500µF Sanyo MV-WX Output Capacitors

L1 (µH)	C_{OUT} (µF)	R_C (kΩ)	C_C (µF)	C1 (pF)
1.2	4500	39	0.0042	180
1.2	6000	56	0.0033	120
1.2	9000	82	0.0033	100
2.4	4500	82	0.0033	82
2.4	6000	100	0.0022	56
2.4	9000	150	0.0022	68
4.7	4500	120	0.0022	39
4.7	6000	220	0.0022	27
4.7	9000	220	0.0015	33

LAYOUT CONSIDERATIONS

When laying out the printed circuit board, use the following checklist to ensure proper operation of the LTC3832. These items are also illustrated graphically in the layout diagram of Figure 11. The thicker lines show the high current paths. Note that at 10A current levels or above, current density in the PC board itself is a serious concern. Traces carrying high current should be as wide as possible. For example, a PCB fabricated with 2oz copper requires a minimum trace width of 0.15" to carry 10A.

APPLICATIONS INFORMATION

1. In general, layout should begin with the location of the power devices. Be sure to orient the power circuitry so that a clean power flow path is achieved. Conductor widths should be maximized and lengths minimized. After you are satisfied with the power path, the control circuitry should be laid out. It is much easier to find routes for the relatively small traces in the control circuits than it is to find circuitous routes for high current paths.

2. The GND and PGND pins should be shorted directly at the LTC3832. This helps to minimize internal ground disturbances in the LTC3832 and prevent differences in ground potential from disrupting internal circuit operation. This connection should then tie into the ground plane at a single point, preferably at a fairly quiet point in the circuit such as close to the output capacitors. This is not always practical, however, due to physical constraints. Another reasonably good point to make this connection is between the output capacitors and the source connection of the bottom MOSFET Q2. Do not tie this single point ground in the trace run between the Q2 source and the input capacitor ground, as this area of the ground plane will be very noisy.

3. The small-signal resistors and capacitors for frequency compensation and soft-start should be located very close to their respective pins and the ground ends connected to the signal ground pin through a separate trace. Do not connect these parts to the ground plane!

4. The V_{CC}, PV_{CC1} and PV_{CC2} decoupling capacitors should be as close to the LTC3832 as possible. The 4.7µF and 1µF bypass capacitors shown at V_{CC}, PV_{CC1} and PV_{CC2} will help provide optimum regulation performance.

5. The (+) plate of C_{IN} should be connected as close as possible to the drain of the upper MOSFET, Q1. An additional 1µF ceramic capacitor between V_{IN} and power ground is recommended.

6. The SENSE and V_{FB} pins are very sensitive to pickup from the switching node. Care should be taken to isolate SENSE and V_{FB} from possible capacitive coupling to the inductor switching signal. Connecting the $SENSE^+$ and $SENSE^-$ close to the load can significantly improve load regulation.

7. Kelvin sense I_{MAX} and I_{FB} at Q1's drain and source pins.

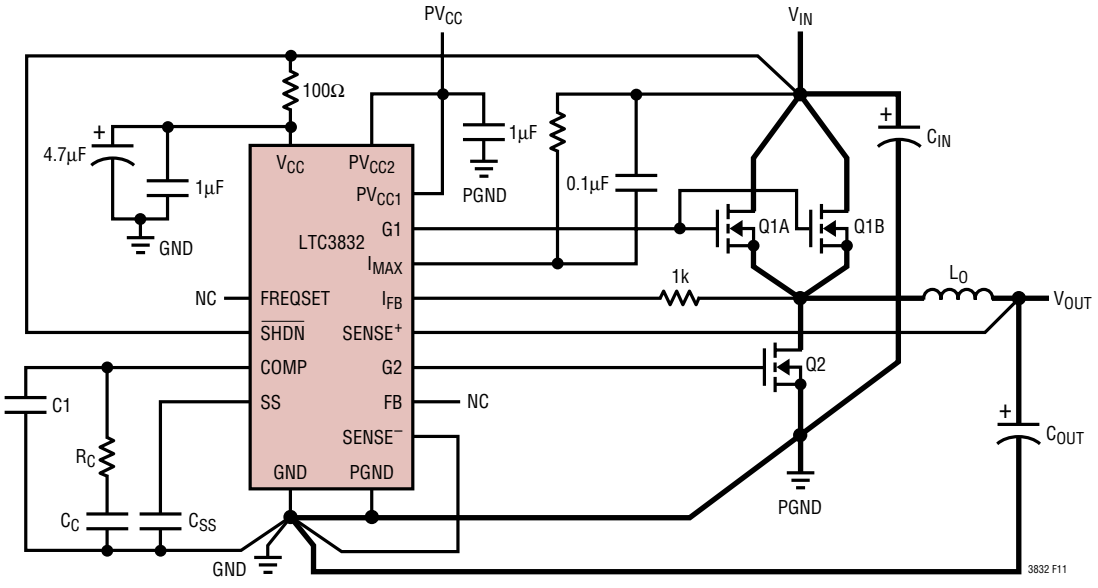


Figure 11. Typical Schematic Showing Layout Considerations

APPLICATIONS INFORMATION

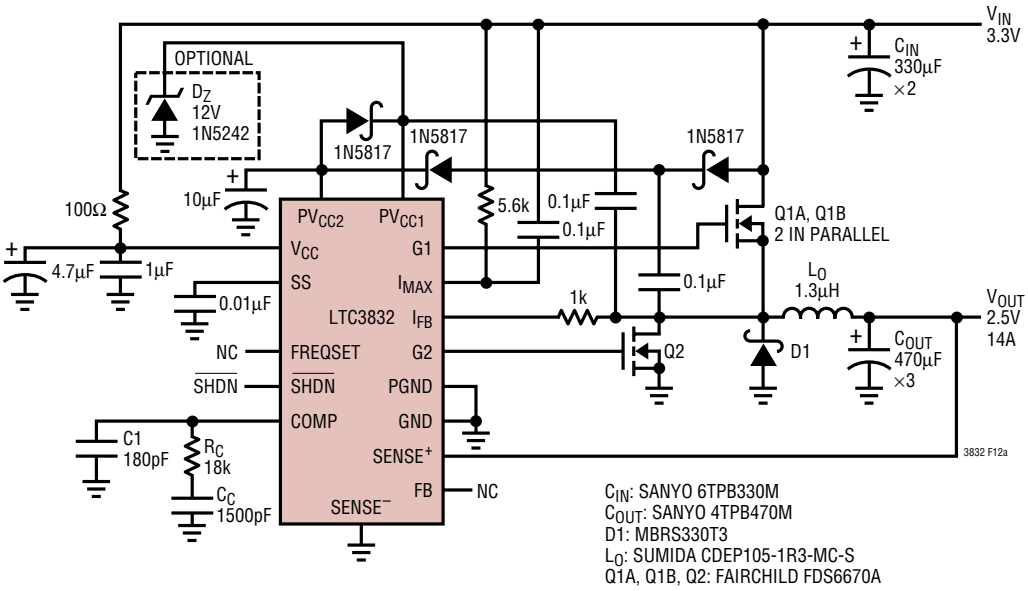
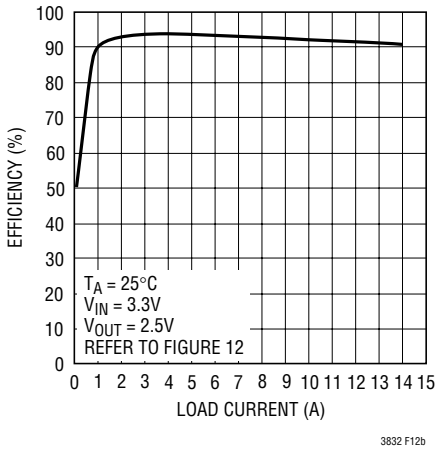


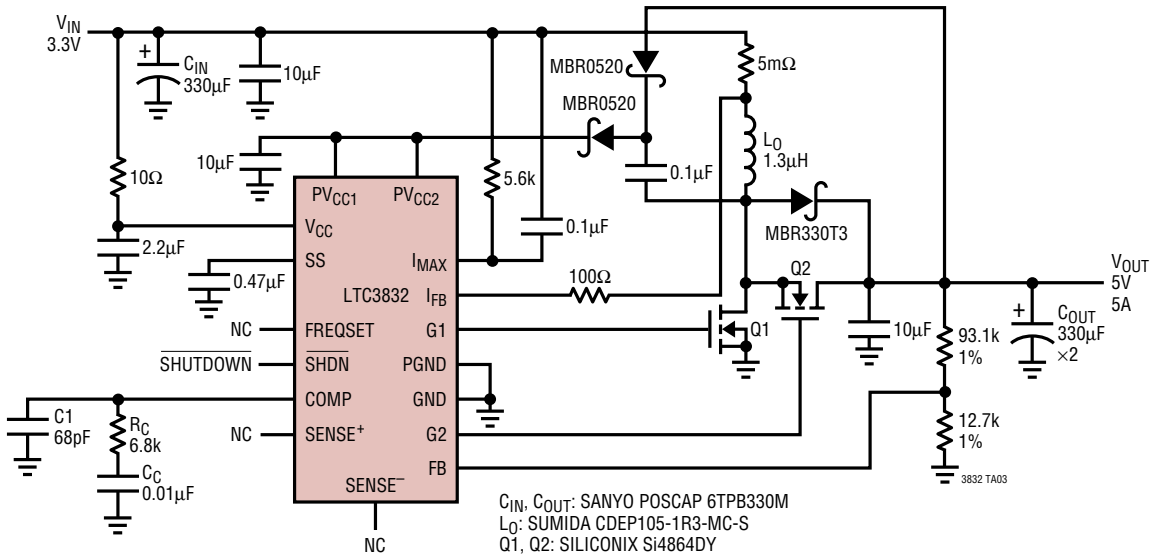
Figure 12. Typical 3.3V to 2.5V, 14A Application

Efficiency vs Load Current



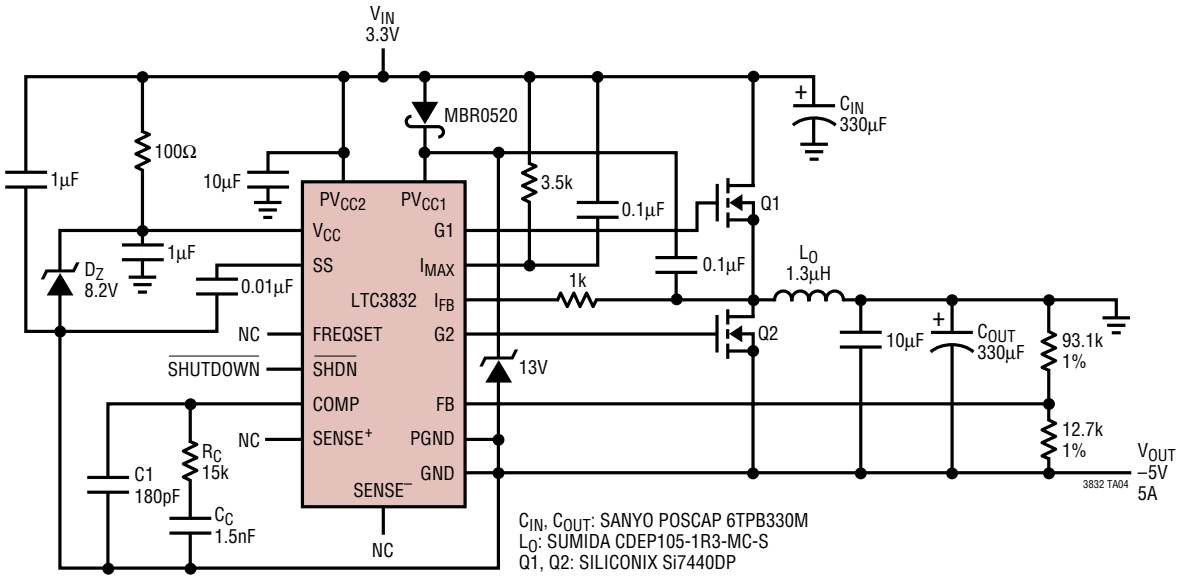
TYPICAL APPLICATIONS

Typical 3.3V to 5V, 5A Synchronous Boost Converter



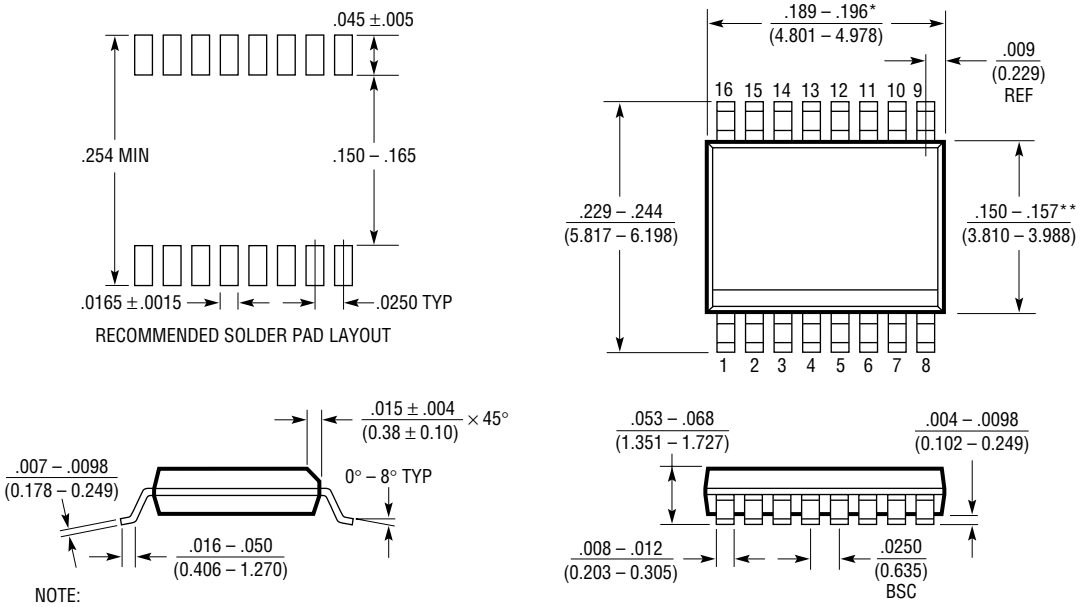
TYPICAL APPLICATIONS

Typical 3.3V to –5V, 5A Positive-to-Negative Converter



PACKAGE DESCRIPTION

GN Package
16-Lead Plastic SSOP (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1641)



NOTE:
1. CONTROLLING DIMENSION: INCHES
2. DIMENSIONS ARE IN $\frac{\text{INCHES}}{(\text{MILLIMETERS})}$
3. DRAWING NOT TO SCALE

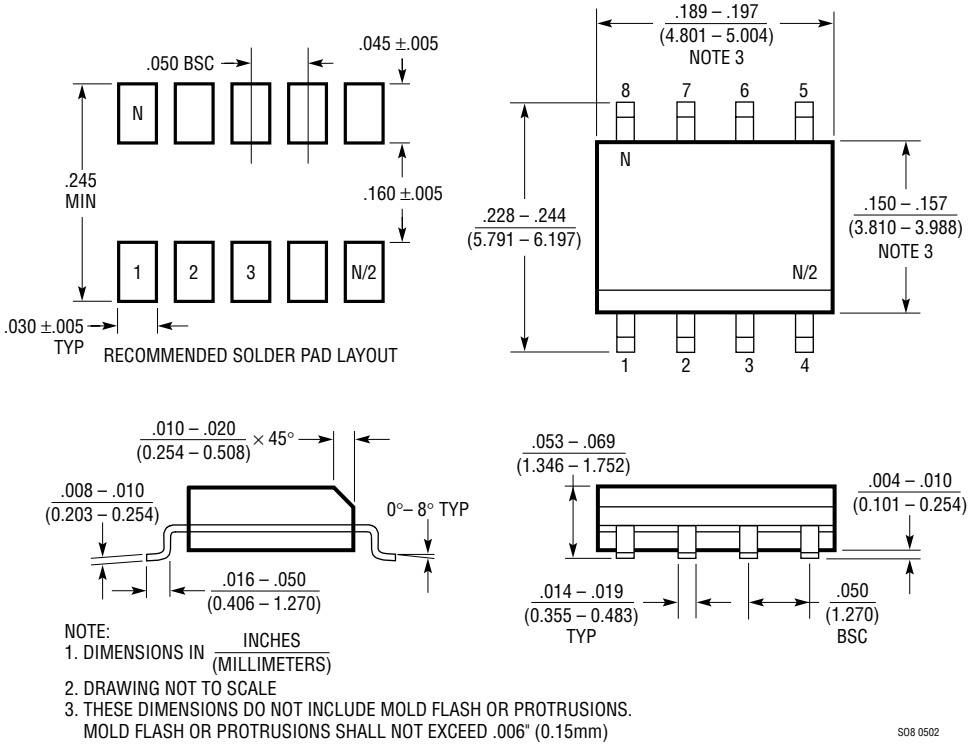
*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

GN16 (SSOP) 0502

PACKAGE DESCRIPTION

S8 Package
8-Lead Plastic Small Outline (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1610)



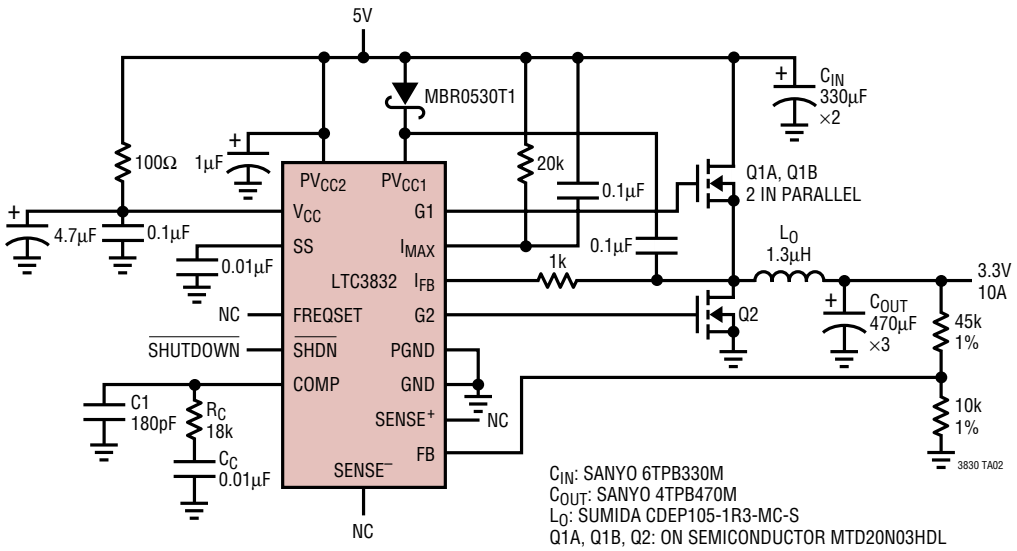
NOTE:
1. DIMENSIONS IN $\frac{\text{INCHES}}{(\text{MILLIMETERS})}$
2. DRAWING NOT TO SCALE
3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
   MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)

SO8 0502

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

TYPICAL APPLICATION

Typical 5V to 3.3V, 10A Application



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1530	High Power Synchronous Switching Regulator Controller	SO-8 with Current Limit. No R_{SENSE}™ Required
LTC1628	Dual High Efficiency 2-Phase Synchronous Step-Down Controller	Constant Frequency, Standby 5V and 3.3V LDOs, $3.5V \le V_{IN} \le 36V$
LTC1702	Dual High Efficiency 2-Phase Synchronous Step-Down Controller	550kHz, 25MHz GBW Voltage Mode, $V_{IN} \le 7V$, No R_{SENSE}
LTC1705	Dual 550kHz Synchronous 2-Phase Switching Regulator Controller with 5-Bit VID Plus LDO	Provides CPU Core, I/O and CLK Supplies for Portable Systems
LTC1709	2-Phase, 5-Bit Desktop VID Synchronous Step-Down Controller	Current Mode, V_{IN} to 36V, I_{OUT} Up to 42A
LTC1736	Synchronous Step-Down Controller with 5-Bit Mobile VID Control	Fault Protection, Power Good, 3.5V to 36V Input, Current Mode
LTC1753	5-Bit Desktop VID Programmable Synchronous Switching Regulator	1.3V to 3.5V Programmable Output Using Internal 5-Bit DAC
LTC1773	Synchronous Step-Down Controller in MS10	Up to 95% Efficiency, 550kHz, $2.65V \le V_{IN} \le 8.5V$, $0.8V \le V_{OUT} \le V_{IN}$, Synchronizable to 750kHz
LTC1778	Wide Operating Range/Step-Down Controller, No R_{SENSE}	V_{IN} Up to 36V, Current Mode, Power Good
LTC1873	Dual Synchronous Switching Regulator with 5-Bit Desktop VID	1.3V to 3.5V Programmable Core Output Plus I/O Output
LTC1876	2-Phase, Dual Step-Down Synchronous Controller with Integrated Step-Up DC/DC Regulator	Step-Down DC/DC Conversion from $3V_{IN}$, Minimum C_{IN} and C_{OUT}, Uses Logic-Level N-Channel MOSFETs
LTC1929	2-Phase, Synchronous High Efficiency Converter with Mobile VID	Current Mode Ensures Accurate Current Sensing V_{IN} Up to 36V, I_{OUT} Up to 40A
LTC3713	Low Input Voltage, High Power, No R_{SENSE}, Step-Down Synchronous Controller	Minimum V_{IN}: 1.5V, Uses Standard Logic-Level N-Channel MOSFETs
LTC3831	High Power Synchronous Switching Regulator Controller for DDR Memory Termination	V_{OUT} Tracks 1/2 of V_{IN} or External Reference

No R_{SENSE} is a trademark of Linear Technology Corporation.

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