No R_{SENSE}™, Low EMI, Synchronous DC/DC Controller

FEATURES

- **No Current Sense Resistor Required**
- **Selectable Spread Spectrum Frequency Modulation for Low Noise Operation**
- **Constant Frequency Current Mode Operation for Excellent Line and Load Transient Response**
- True PLL for Frequency Locking or Adjustment (Frequency Range: 250kHz to 750kHz)
- Wide V_{IN} Range: 2.75V to 9.8V
- Wide V_{OUT} Range: 0.6V to V_{IN}
- 0.6V ±1.5% Reference
- Low Dropout Operation: 100% Duty Cycle
- Selectable Burst Mode®/Pulse-Skipping/Forced Continuous Operation
- Auxiliary Winding Regulation
- Internal Soft-Start Circuitry
- Output Overvoltage Protection
- Micropower Shutdown: I_Q = 9µA
- Tiny Thermally Enhanced Leadless (3mm × 3mm) DFN and 10-lead MSOP Packages

APPLICATIONS

- 1- or 2-Cell Lithium-Ion Powered Devices
- Portable Instruments
- Distributed DC Power Systems

DESCRIPTION

The LTC®3809 is a synchronous step-down switching regulator controller that drives external complementary power MOSFETs using few external components. The constant frequency current mode architecture with MOSFET V_{DS} sensing eliminates the need for a current sense resistor and improves efficiency.

For noise sensitive applications, the LTC3809 can be externally synchronized from 250kHz to 750kHz. Burst Mode is inhibited during synchronization or when the SYNC/MODE pin is pulled low to reduce noise and RF interference. To further reduce EMI, the LTC3809 incorporates a novel spread spectrum frequency modulation technique.

Burst Mode operation provides high efficiency operation at light loads. 100% duty cycle provides low dropout operation, extending operating time in battery-powered systems.

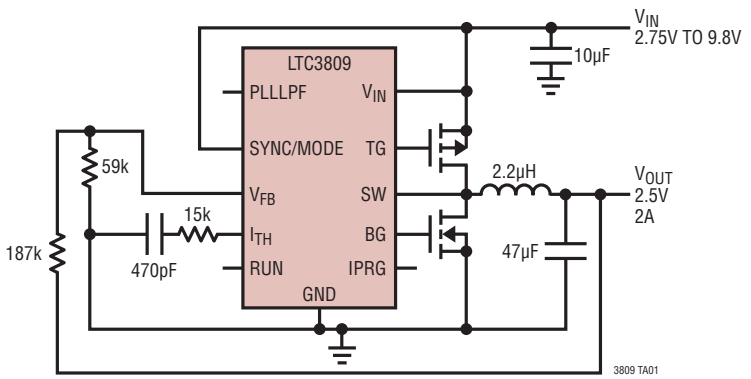
The switching frequency can be programmed up to 750kHz, allowing the use of small surface mount inductors and capacitors.

The LTC3809 is available in tiny footprint thermally enhanced DFN and 10-lead MSOP packages.

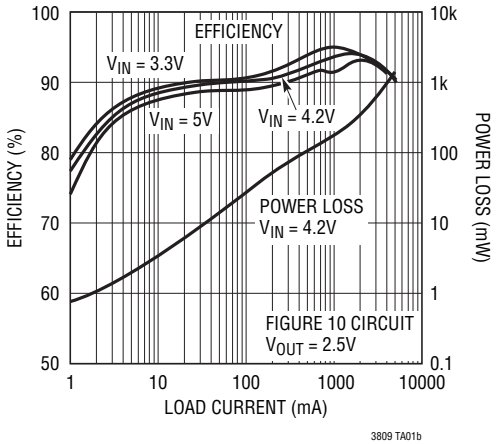
, LT, LTC, LTM and Burst Mode are registered trademarks of Linear Technology Corporation.
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All other trademarks are the property of their respective owners.
Protected by U.S. Patents including 5481178, 5929620, 6580258, 6304066, 5847554, 6611131, 6498466. Other Patents pending.

TYPICAL APPLICATION

High Efficiency, 550kHz Step-Down Converter



Efficiency and Power Loss vs Load Current

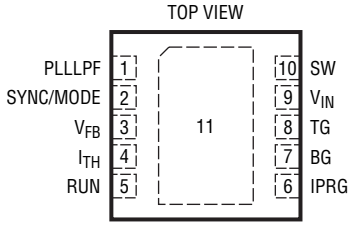


ABSOLUTE MAXIMUM RATINGS (Note 1)

Input Supply Voltage (V_{IN}) ..... –0.3V to 10V
PLLLPF, RUN, SYNC/MODE,
IPRG Voltages ..... –0.3V to (V_{IN} + 0.3V)
V_{FB}, I_{TH} Voltages ..... –0.3V to 2.4V
SW Voltage ..... –2V to V_{IN} + 1V (10V Max)
TG, BG Peak Output Current (<10µs) 1A

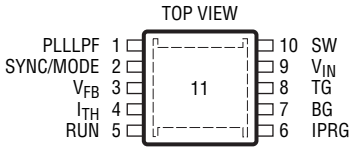
Operating Temperature Range (Note 2) ....–40°C to 85°C
Storage Temperature Range .....–65°C to 125°C
Junction Temperature (Note 3) ..... 125°C
Lead Temperature (Soldering, 10 sec)
MSOP Package ..... 300°C

PIN CONFIGURATION



DD PACKAGE
10-LEAD (3mm × 3mm) PLASTIC DFN

T_{JMAX} = 125°C, θ_{JA} = 43°C/W
EXPOSED PAD (PIN 11) IS GND
(MUST BE SOLDERED TO PCB)



MSE PACKAGE
10-LEAD PLASTIC MSOP

T_{JMAX} = 125°C, θ_{JA} = 40°C/W
EXPOSED PAD (PIN 11) IS GND
(MUST BE SOLDERED TO PCB)

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3809EDD#PBF	LTC3809EDD#TRPBF	LBQY	10-Lead (3mm × 3mm) Plastic DFN	–40°C to 85°C
LTC3809EMSE#PBF	LTC3809EMSE#TRPBF	LTBQT	10-Lead Plastic MSOP	–40°C to 85°C
LEAD BASED FINISH	**TAPE AND REEL**	**PART MARKING**	**PACKAGE DESCRIPTION**	**TEMPERATURE RANGE**
LTC3809EDD	LTC3809EDD#TR	LBQY	10-Lead (3mm × 3mm) Plastic DFN	–40°C to 85°C
LTC3809EMSE	LTC3809EMSE#TR	LTBQT	10-Lead Plastic MSOP	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 4.2V unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Main Control Loops						
Input DC Supply Current Normal Operation Sleep Mode Shutdown UVLO	(Note 4) RUN = 0V V_{IN} = UVLO Threshold – 200mV			 350 105 9 3	 500 150 20 10	 µA µA µA µA
Undervoltage Lockout Threshold (UVLO)	V_{IN} Falling V_{IN} Rising	● ●	1.95 2.15	2.25 2.45	2.55 2.75	V V
Shutdown Threshold of RUN Pin			0.8	1.1	1.4	V
Regulated Feedback Voltage	(Note 5)	●	0.591	0.6	0.609	V
Output Voltage Line Regulation	2.75V < V_{IN} < 9.8V (Note 5)			0.01	0.04	%/V
Output Voltage Load Regulation	I_{TH} = 0.9V (Note 5) I_{TH} = 1.7V			0.1 –0.1	0.5 –0.5	% %
V_{FB} Input Current	(Note 5)			9	50	nA
Overvoltage Protect Threshold	Measured at V_{FB}		0.66	0.68	0.7	V
Overvoltage Protect Hysteresis				20		mV
Auxiliary Feedback Threshold			0.325	0.4	0.475	V
Top Gate (TG) Drive Rise Time	C_L = 3000pF			40		ns
Top Gate (TG) Drive Fall Time	C_L = 3000pF			40		ns
Bottom Gate (BG) Drive Rise Time	C_L = 3000pF			50		ns
Bottom Gate (BG) Drive Fall Time	C_L = 3000pF			40		ns
Maximum Current Sense Voltage ($\Delta V_{SENSE(MAX)}$) (V_{IN} – SW)	IPRG = Floating (Note 6) IPRG = 0V (Note 6) IPRG = V_{IN} (Note 6)	● ● ●	110 70 185	125 85 204	140 100 223	mV mV mV
Soft-Start Time (Internal)	Time for V_{FB} to Ramp from 0.05V to 0.55V		0.5	0.74	0.9	ms
Oscillator and Phase-Locked Loop						
Oscillator Frequency	Unsynchronized (SYNC/MODE Not Clocked) PLLLPF = Floating PLLLPF = 0V PLLLPF = V_{IN}		 480 260 650	 550 300 750	 600 340 825	 kHz kHz kHz
Phase-Locked Loop Lock Range	SYNC/MODE Clocked Minimum Synchronizable Frequency Maximum Synchronizible Frequency		 750	 200 1000	 250 	 kHz kHz
Phase Detector Output Current Sinking Sourcing	 $f_{OSC} > f_{SYNC/MODE}$ $f_{OSC} < f_{SYNC/MODE}$			 –3 3	 	 µA µA
Spread Spectrum Frequency Range	Minimum Switching Frequency Maximum Switching Frequency			460 635		kHz kHz
SYNC/MODE Pull-Down Current	SYNC/MODE = 2.2V			2.6		µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC3809E is guaranteed to meet specified performance from 0°C to 85°C. Specifications over the –40°C to 85°C operating range are assured by design characterization, and correlation with statistical process controls.

Note 3: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formula:

$$T_J = T_A + (P_D \bullet \theta_{JA}\ °C/W)$$

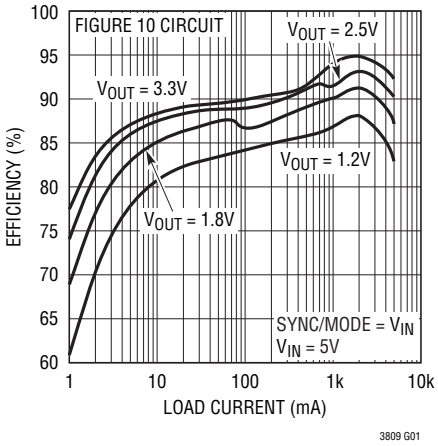
Note 4: Dynamic supply current is higher due to gate charge being delivered at the switching frequency.

Note 5: The LTC3809 is tested in a feedback loop that servos I_{TH} to a specified voltage and measures the resultant V_{FB} voltage.

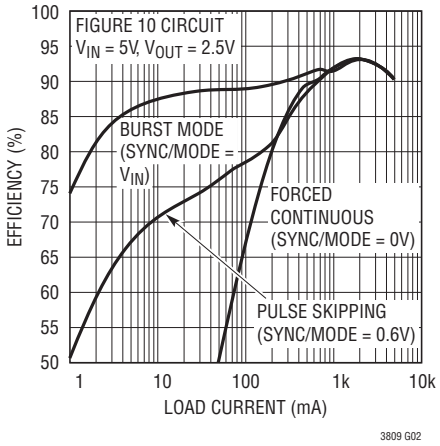
Note 6: Peak current sense voltage is reduced dependent on duty cycle to a percentage of value as shown in Figure 1.

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C unless otherwise noted.

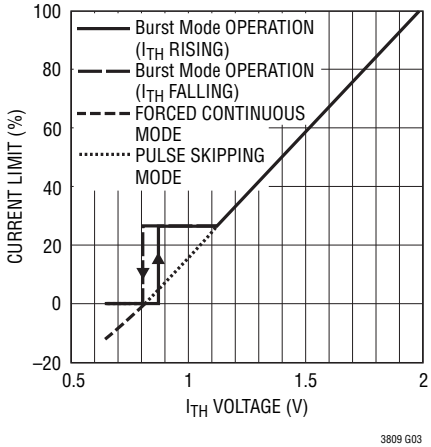
Efficiency vs Load Current



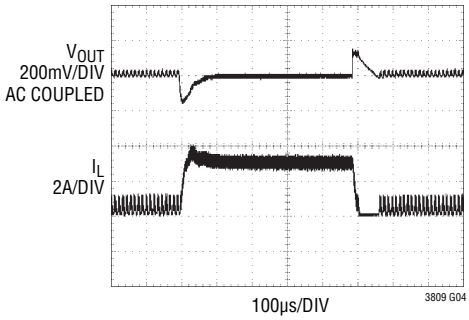
Efficiency vs Load Current



Maximum Current Sense Voltage vs I_{TH} Pin Voltage

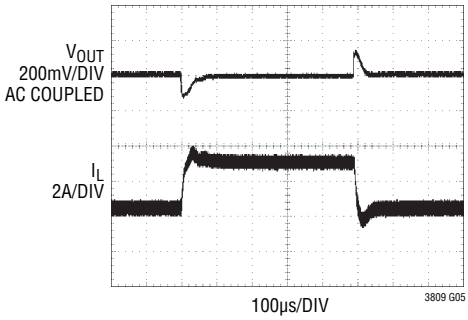


Load Step (Burst Mode Operation)



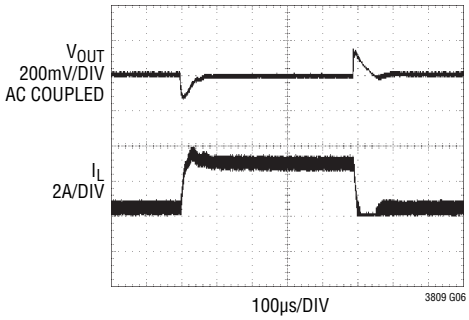
V_{IN} = 3.3V
V_{OUT} = 1.8V
I_{LOAD} = 300mA TO 3A
SYNC/MODE = V_{IN}
FIGURE 10 CIRCUIT

Load Step (Forced Continuous Mode)



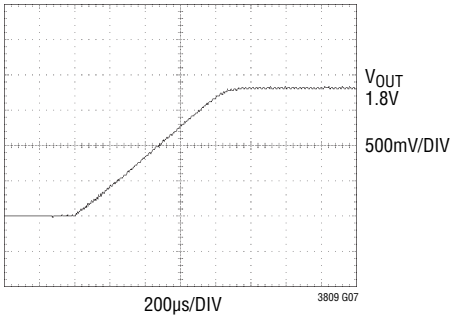
V_{IN} = 3.3V
V_{OUT} = 1.8V
I_{LOAD} = 300mA TO 3A
SYNC/MODE = 0V
FIGURE 10 CIRCUIT

Load Step (Pulse-Skipping Mode)



V_{IN} = 3.3V
V_{OUT} = 1.8V
I_{LOAD} = 300mA TO 3A
SYNC/MODE = V_{FB}
FIGURE 10 CIRCUIT

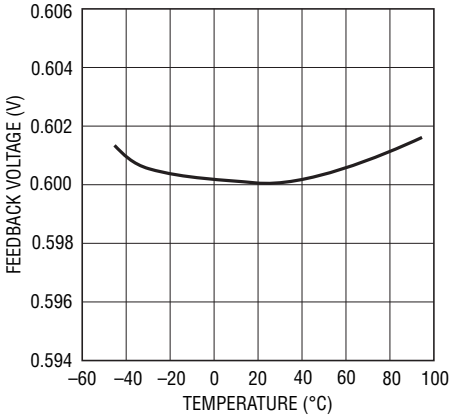
Start-Up with Internal Soft-Start



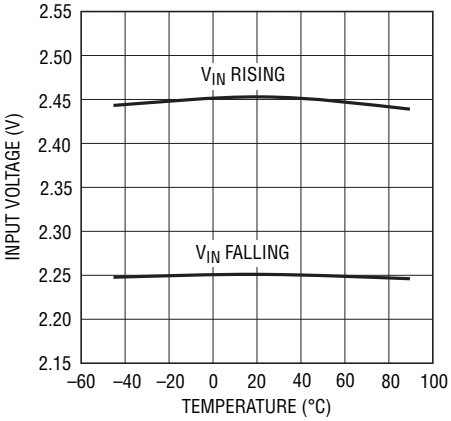
V_{IN} = 4.2V
R_{LOAD} = 1Ω
FIGURE 10 CIRCUIT

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C unless otherwise noted.

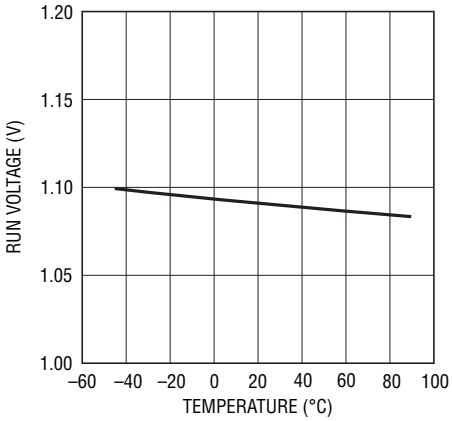
Regulated Feedback Voltage vs Temperature



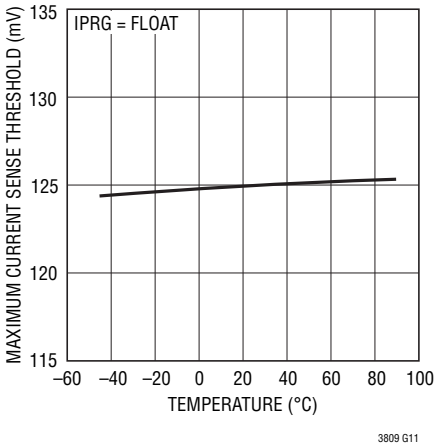
Undervoltage Lockout Threshold vs Temperature



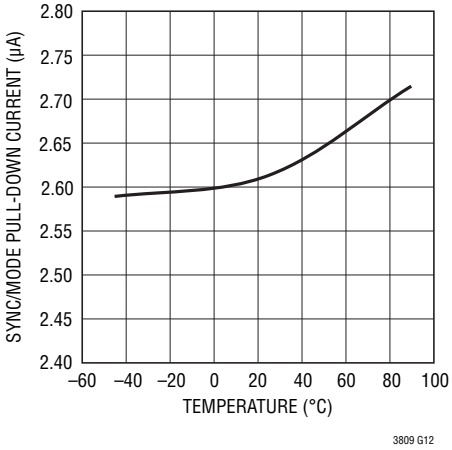
Shutdown (RUN) Threshold vs Temperature



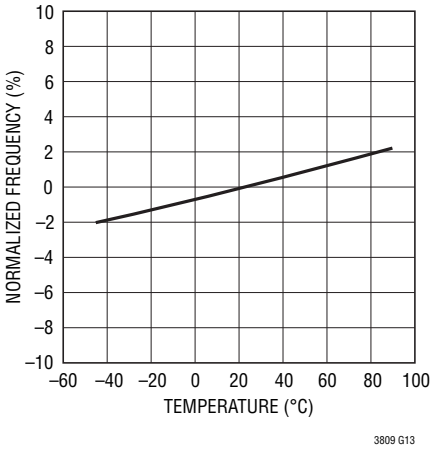
Maximum Current Sense Threshold vs Temperature



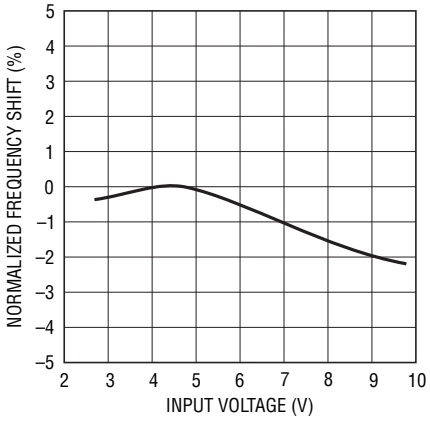
SYNC/MODE Pull-Down Current vs Temperature



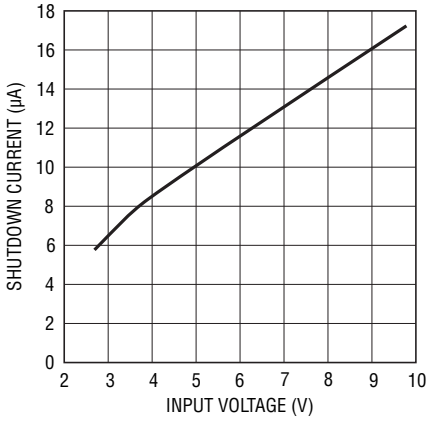
Oscillator Frequency vs Temperature



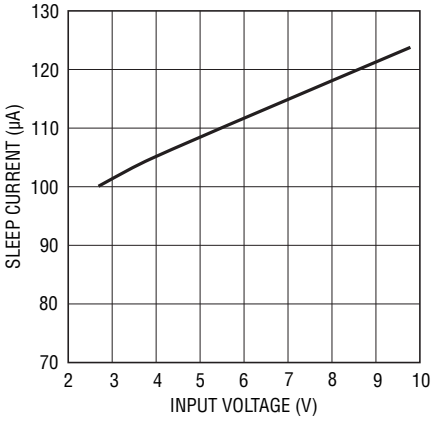
Oscillator Frequency vs Input Voltage



Shutdown Quiescent Current vs Input Voltage



Sleep Current vs Input Voltage



PIN FUNCTIONS

PLLLPF (Pin 1): Frequency Set/PLL Lowpass Filter. When synchronizing to an external clock, this pin serves as the lowpass filter point for the phase-locked loop. Normally, a series RC is connected between this pin and ground.

When not synchronizing to an external clock, this pin serves as the frequency select input. Tying this pin to GND selects 300kHz operation; tying this pin to V_{IN} selects 750kHz operation. Floating this pin selects 550kHz operation.

Connect a 2.2nF capacitor between this pin and GND, and a 1000pF capacitor between this pin and the SYNC/MODE when using spread spectrum modulation operation.

SYNC/MODE (Pin 2): This pin performs four functions: 1) auxiliary winding feedback input, 2) external clock synchronization input for phase-locked loop, 3) Burst Mode, pulse-skipping or forced continuous mode select, and 4) enable **spread spectrum** modulation operation in pulse-skipping mode. Applying a clock with frequency between 250kHz to 750kHz causes the internal oscillator to phase-lock to the external clock and disables Burst Mode operation but allows pulse-skipping at low load currents.

To select Burst Mode operation at light loads, tie this pin to V_{IN}. Grounding this pin selects forced continuous operation, which allows the inductor current to reverse. Tying this pin to V_{FB} selects pulse-skipping mode. In these cases, the frequency of the internal oscillator is set by the voltage on the PLLLPF pin. Tying to a voltage between 1.35V to V_{IN} – 0.5V enables spread spectrum modulation operation. In this case, an internal 2.6µA pull-down current source helps to set the voltage at this pin by tying a resistor with appropriate value between this pin and V_{IN}. **Do not leave this pin floating.**

V_{FB} (Pin 3): Feedback Pin. This pin receives the remotely sensed feedback voltage for the controller from an external resistor divider across the output.

ITH (Pin 4): Current Threshold and Error Amplifier Compensation Point. Nominal operating range on this pin is from 0.7V to 2V. The voltage on this pin determines the threshold of the main current comparator.

RUN (Pin 5): Run Control Input. Forcing this pin below 1.1V shuts down the chip. Driving this pin to V_{IN} or releasing this pin enables the chip to start-up with the internal soft-start.

IPRG (Pin 6): Three-State Pin to Select Maximum Peak Sense Voltage Threshold. This pin selects the maximum allowed voltage drop between the V_{IN} and SW pins (i.e., the maximum allowed drop across the external P-channel MOSFET). Tie to V_{IN}, GND or float to select 204mV, 85mV or 125mV respectively.

BG (Pin 7): Bottom (NMOS) Gate Drive Output. This pin drives the gate of the external N-channel MOSFET. This pin has an output swing from PGND to V_{IN}.

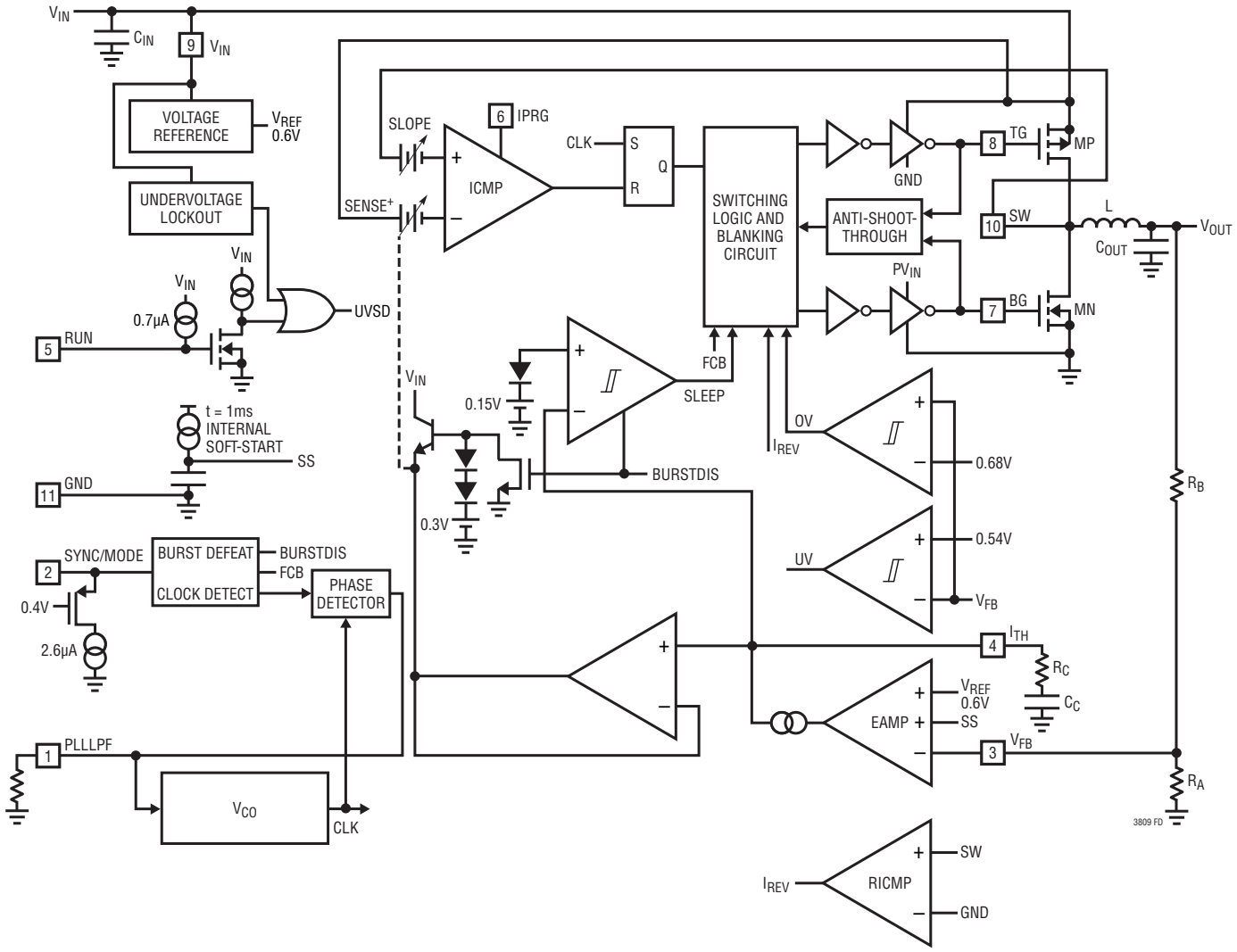
TG (Pin 8): Top (PMOS) Gate Drive Output. This pin drives the gate of the external P-channel MOSFET. This pin has an output swing from PGND to V_{IN}.

V_{IN} (Pin 9): Chip Signal Power Supply. This pin powers the entire chip, the gate drivers and serves as the positive input to the differential current comparator.

SW (Pin 10): Switch Node Connection to Inductor. This pin is also the negative input to the differential current comparator and an input to the reverse current comparator. Normally this pin is connected to the drain of the external P-channel MOSFET, the drain of the external N-channel MOSFET and the inductor.

GND (Pin 11): Exposed Pad. The Exposed Pad is ground and must be soldered to the PCB ground for electrical contact and optimum thermal performance.

FUNCTIONAL DIAGRAM



OPERATION (Refer to Functional Diagram)

Main Control Loop

The LTC3809 uses a constant frequency, current mode architecture. During normal operation, the top external P-channel power MOSFET is turned on when the clock sets the RS latch, and is turned off when the current comparator (ICMP) resets the latch. The peak inductor current at which ICMP resets the RS latch is determined by the voltage on the I_{TH} pin, which is driven by the output of the error amplifier (EAMP). The V_{FB} pin receives the output voltage feedback signal from an external resistor divider. This feedback signal is compared to the internal 0.6V reference voltage by the EAMP. When the load current increases, it causes a slight decrease in V_{FB} relative to the 0.6V reference, which in turn causes the I_{TH} voltage to increase until the average inductor current matches the new load current. While the top P-channel MOSFET is off, the bottom N-channel MOSFET is turned on until either the inductor current starts to reverse, as indicated by the current reversal comparator IRCMP, or the beginning of the next cycle.

Shutdown and Soft-Start (RUN Pin)

The LTC3809 is shut down by pulling the RUN pin low. In shutdown, all controller functions are disabled and the chip draws only 9µA. The TG output is held high (off) and the BG output low (off) in shutdown. Releasing the RUN pin allows an internal 0.7µA current source to pull up the RUN pin to V_{IN}. The controller is enabled when the RUN pin reaches 1.1V.

The start-up of V_{OUT} is controlled by the LTC3809's internal soft-start. During soft-start, the error amplifier EAMP compares the feedback signal V_{FB} to the internal soft-start ramp (instead of the 0.6V reference), which rises linearly from 0V to 0.6V in about 1ms. This allows the output voltage to rise smoothly from 0V to its final value while maintaining control of the inductor current.

Light Load Operation (Burst Mode Operation, Continuous Conduction or Pulse-Skipping Mode) (SYNC/MODE Pin)

The LTC3809 can be programmed for either high efficiency Burst Mode operation, forced continuous conduction mode or pulse-skipping mode at low load currents. To select Burst Mode operation, tie the SYNC/MODE pin to V_{IN}. To select forced continuous operation, tie the SYNC/MODE pin to a DC voltage below 0.4V (e.g., GND). Tying the SYNC/MODE to a DC voltage above 0.4V and below 1.2V (e.g., V_{FB}) enables pulse-skipping mode. The 0.4V threshold between forced continuous operation and pulse-skipping mode can be used in secondary winding regulation as described in the Auxiliary Winding Control Using SYNC/MODE Pin discussion in the Applications Information section.

When the LTC3809 is in Burst Mode operation, the peak current in the inductor is set to approximately one-fourth of the maximum sense voltage even though the voltage on the I_{TH} pin indicates a lower value. If the average inductor current is higher than the load current, the EAMP will decrease the voltage on the I_{TH} pin. When the I_{TH} voltage drops below 0.85V, the internal SLEEP signal goes high and the external MOSFET is turned off.

In sleep mode, much of the internal circuitry is turned off, reducing the quiescent current that the LTC3809 draws. The load current is supplied by the output capacitor. As the output voltage decreases, the EAMP increases the I_{TH} voltage. When the I_{TH} voltage reaches 0.925V, the SLEEP signal goes low and the controller resumes normal operation by turning on the external P-channel MOSFET on the next cycle of the internal oscillator.

When the controller is enabled for Burst Mode or pulse-skipping operation, the inductor current is not allowed to reverse. Hence, the controller operates discontinuously.

OPERATION (Refer to Functional Diagram)

The reverse current comparator RICMP senses the drain-to-source voltage of the bottom external N-channel MOSFET. This MOSFET is turned off just before the inductor current reaches zero, preventing it from going negative.

In forced continuous operation, the inductor current is allowed to reverse at light loads or under large transient conditions. The peak inductor current is determined by the voltage on the I_{TH} pin. The P-channel MOSFET is turned on every cycle (constant frequency) regardless of the I_{TH} pin voltage. In this mode, the efficiency at light loads is lower than in Burst Mode operation. However, continuous mode has the advantages of lower output ripple and no noise at audio frequencies.

When the SYNC/MODE pin is clocked by an external clock source to use the phase-locked loop (see Frequency Selection and Phase-Locked Loop), or is set to a DC voltage between 0.4V and several hundred mV below V_{IN}, the LTC3809 operates in PWM pulse-skipping mode at light loads. In this mode, the current comparator ICMP may remain tripped for several cycles and force the external P-channel MOSFET to stay off for the same number of cycles. The inductor current is not allowed to reverse (discontinuous operation). This mode, like forced continuous operation, exhibits low output ripple as well as low audio noise and reduced RF interference as compared to Burst Mode operation. However, it provides low current efficiency higher than forced continuous mode, but not nearly as high as Burst Mode operation. During start-up or an undervoltage condition ($V_{FB} \leq$ 0.54V), the LTC3809 operates in pulse-skipping mode (no current reversal allowed), regardless of the state of the SYNC/MODE pin.

Short-Circuit and Current Limit Protection

The LTC3809 monitors the voltage drop ΔV_{SC} (between the GND and SW pins) across the external N-channel MOSFET with the short-circuit current limit comparator. The allowed voltage is determined by:

$$\Delta V_{SC(MAX)} = A \bullet 90mV$$

where A is a constant determined by the state of the IPRG pin. Floating the IPRG pin selects A = 1; tying IPRG to V_{IN} selects A = 5/3; tying IPRG to GND selects A = 2/3.

The inductor current limit for short-circuit protection is determined by $\Delta V_{SC(MAX)}$ and the on-resistance of the external N-channel MOSFET:

$$I_{SC} = \frac{\Delta V_{SC(MAX)}}{R_{DS(ON)}}$$

Once the inductor current exceeds I_{SC}, the short current comparator will shut off the external P-channel MOSFET until the inductor current drops below I_{SC}.

Output Overvoltage Protection

As further protection, the overvoltage comparator (OVP) guards against transient overshoots, as well as other more serious conditions that may overvoltage the output. When the feedback voltage on the V_{FB} pin has risen 13.33% above the reference voltage of 0.6V, the external P-channel MOSFET is turned off and the N-channel MOSFET is turned on until the overvoltage is cleared.

OPERATION (Refer to Functional Diagram)

Frequency Selection and Phase-Locked Loop (PLLLPF and SYNC/MODE Pins)

The selection of switching frequency is a tradeoff between efficiency and component size. Low frequency operation increases efficiency by reducing MOSFET switching losses, but requires larger inductance and/or capacitance to maintain low output ripple voltage.

The switching frequency of the LTC3809's controllers can be selected using the PLLLPF pin. If the SYNC/MODE is not being driven by an external clock source, the PLLLPF can be floated, tied to V_{IN} or tied to GND to select 550kHz, 750kHz or 300kHz, respectively.

A phase-locked loop (PLL) is available on the LTC3809 to synchronize the internal oscillator to an external clock source that connects to the SYNC/MODE pin. In this case, a series RC should be connected between the PLLLPF pin and GND to serve as the PLL's loop filter. The LTC3809 phase detector adjusts the voltage on the PLLLPF pin to align the turn-on of the external P-channel MOSFET to the rising edge of the synchronizing signal.

The typical capture range of the LTC3809's phase-locked loop is from approximately 200kHz to 1MHz.

Spread Spectrum Modulation (SYNC/MODE and PLLLPF Pins)

Connecting the SYNC/MODE pin to a DC voltage above 1.35V and several hundred mV below V_{IN} enables spread spectrum modulation (SSM) operation. An internal 2.6µA pull-down current source at SYNC/MODE helps to set the voltage at the SYNC/MODE pin for this operation by tying a resistor with appropriate value between SYNC/MODE and V_{IN}. This mode of operation spreads the internal oscillator frequency f_{OSC} (= 550kHz) over a wider range (460kHz to 635kHz), reducing the peaks of the harmonic output on a spectral analysis of the output noise. In this case, a 2.2nF filter cap should be connected between the PLLLPF pin and GND and another 1000pF cap should be connected between PLLLPF and the SYNC/MODE pin. The controller operates in PWM pulse-skipping mode at light loads when spread spectrum modulation is selected. See the discussion of Spread Spectrum Modulation with SYNC/MODE and PLLLPF Pins in the Applications Information section.

Dropout Operation

When the input supply voltage (V_{IN}) approaches the output voltage, the rate of change of the inductor current while the external P-channel MOSFET is on (ON cycle) decreases. This reduction means that the P-channel MOSFET will remain on for more than one oscillator cycle if the inductor current has not ramped up to the threshold set by the EAMP on the I_{TH} pin. Further reduction in the input supply voltage will eventually cause the P-channel MOSFET to be turned on 100%; i.e., DC. The output voltage will then be determined by the input voltage minus the voltage drop across the P-channel MOSFET and the inductor.

Undervoltage Lockout

To prevent operation of the P-channel MOSFET below safe input voltage levels, an undervoltage lockout is incorporated in the LTC3809. When the input supply voltage (V_{IN}) drops below 2.25V, the external P- and N-channel MOSFETs and all internal circuits are turned off except for the undervoltage block, which draws only a few microamperes.

OPERATION (Refer to Functional Diagram)

Peak Current Sense Voltage Selection and Slope Compensation (IPRG Pin)

When the LTC3809 controller is operating below 20% duty cycle, the peak current sense voltage (between the V_{IN} and SW pins) allowed across the external P-channel MOSFET is determined by:

$$\Delta V_{SENSE(MAX)} = A \bullet \frac{V_{ITH} - 0.7V}{10}$$

where A is a constant determined by the state of the IPRG pin. Floating the IPRG pin selects A = 1; tying IPRG to V_{IN} selects A = 5/3; tying IPRG to GND selects A = 2/3. The maximum value of V_{ITH} is typically about 1.98V, so the maximum sense voltage allowed across the external P-channel MOSFET is 125mV, 85mV or 204mV for the three respective states of the IPRG pin.

However, once the controller's duty cycle exceeds 20%, slope compensation begins and effectively reduces the peak sense voltage by a scale factor (SF) given by the curve in Figure 1.

The peak inductor current is determined by the peak sense voltage and the on-resistance of the external P-channel MOSFET:

$$I_{PK} = \frac{\Delta V_{SENSE(MAX)}}{R_{DS(ON)}}$$

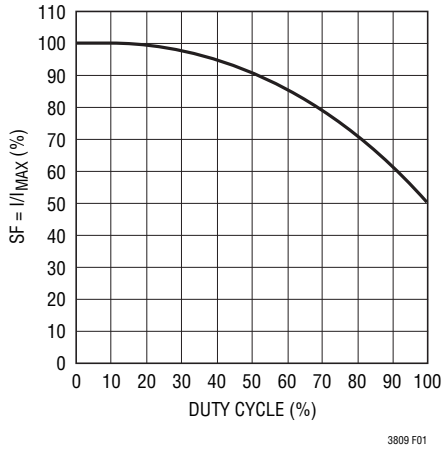


Figure 1. Maximum Peak Current vs Duty Cycle

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The typical LTC3809 application circuit is shown in Figure 10. External component selection for the controller is driven by the load requirement and begins with the selection of the inductor and the power MOSFETs.

Power MOSFET Selection

The LTC3809's controller requires two external power MOSFETs: a P-channel MOSFET for the topside (main) switch and a N-channel MOSFET for the bottom (synchronous) switch. The main selection criteria for the power MOSFETs are the breakdown voltage $V_{BR(DSS)}$, threshold voltage $V_{GS(TH)}$, on-resistance $R_{DS(ON)}$, reverse transfer capacitance C_{RSS}, turn-off delay $t_{D(OFF)}$ and the total gate charge Q_G.

The gate drive voltage is the input supply voltage. Since the LTC3809 is designed for operation down to low input voltages, a sublogic level MOSFET ($R_{DS(ON)}$ guaranteed at V_{GS} = 2.5V) is required for applications that work close to this voltage. When these MOSFETs are used, make sure that the input supply to the LTC3809 is less than the absolute maximum MOSFET V_{GS} rating, which is typically 8V.

The P-channel MOSFET's on-resistance is chosen based on the required load current. The maximum average load current $I_{OUT(MAX)}$ is equal to the peak inductor current minus half the peak-to-peak ripple current I_{RIPPLE}. The LTC3809's current comparator monitors the drain-to-source voltage V_{DS} of the top P-channel MOSFET, which is sensed between the V_{IN} and SW pins. The peak inductor current is limited by the current threshold, set by the voltage on the I_{TH} pin, of the current comparator. The voltage on the I_{TH} pin is internally clamped, which limits the maximum current sense threshold $\Delta V_{SENSE(MAX)}$ to approximately 125mV when IPRG is floating (85mV when IPRG is tied low; 204mV when IPRG is tied high).

The output current that the LTC3809 can provide is given by:

$$I_{OUT(MAX)} = \frac{\Delta V_{SENSE(MAX)}}{R_{DS(ON)}} - \frac{I_{RIPPLE}}{2}$$

where I_{RIPPLE} is the inductor peak-to-peak ripple current (see Inductor Value Calculation).

A reasonable starting point is setting ripple current I_{RIPPLE} to be 40% of $I_{OUT(MAX)}$. Rearranging the above equation yields:

$$R_{DS(ON)MAX} = \frac{5}{6} \bullet \frac{\Delta V_{SENSE(MAX)}}{I_{OUT(MAX)}} \text{ for Duty Cycle} < 20\%$$

However, for operation above 20% duty cycle, slope compensation has to be taken into consideration to select the appropriate value of $R_{DS(ON)}$ to provide the required amount of load current:

$$R_{DS(ON)MAX} = \frac{5}{6} \bullet SF \bullet \frac{\Delta V_{SENSE(MAX)}}{I_{OUT(MAX)}}$$

where SF is a scale factor whose value is obtained from the curve in Figure 1.

These must be further derated to take into account the significant variation in on-resistance with temperature. The following equation is a good guide for determining the required $R_{DS(ON)MAX}$ at 25°C (manufacturer's specification), allowing some margin for variations in the LTC3809 and external component values:

$$R_{DS(ON)MAX} = \frac{5}{6} \bullet 0.9 \bullet SF \bullet \frac{\Delta V_{SENSE(MAX)}}{I_{OUT(MAX)} \bullet \rho_T}$$

The ρ_T is a normalizing term accounting for the temperature variation in on-resistance, which is typically about 0.4%/°C, as shown in Figure 2. Junction-to-case temperature T_{JC} is about 10°C in most applications. For a maximum ambient temperature of 70°C, using $\rho_{80°C}$ ~ 1.3 in the above equation is a reasonable choice.

The N-channel MOSFET's on resistance is chosen based on the short-circuit current limit (I_{SC}). The LTC3809's short-circuit current limit comparator monitors the drain-to-source voltage V_{DS} of the bottom N-channel MOSFET, which is sensed between the GND and SW pins. The

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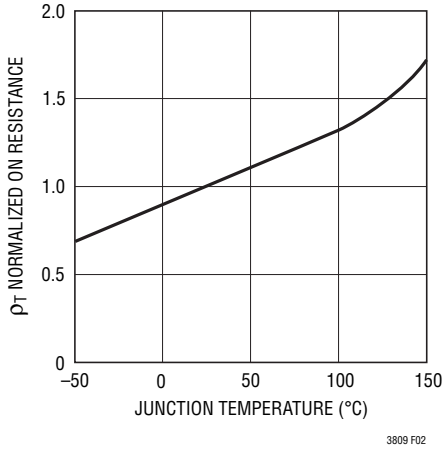


Figure 2. $R_{DS(ON)}$ vs Temperature

short-circuit current sense threshold ΔV_{SC} is set approximately 90mV when IPRG is floating (60mV when IPRG is tied low; 150mV when IPRG is tied high). The on-resistance of N-channel MOSFET is determined by:

$$R_{DS(ON)MAX} = \frac{\Delta V_{SC}}{I_{SC(PEAK)}}$$

The short-circuit current limit ($I_{SC(PEAK)}$) should be larger than the $I_{OUT(MAX)}$ with some margin to avoid interfering with the peak current sensing loop. On the other hand, in order to prevent the MOSFETs from excessive heating and the inductor from saturation, $I_{SC(PEAK)}$ should be smaller than the minimum value of their current ratings. A reasonable range is:

$$I_{OUT(MAX)} < I_{SC(PEAK)} < I_{RATING(MIN)}$$

Therefore, the on-resistance of N-channel MOSFET should be chosen within the following range:

$$\frac{\Delta V_{SC}}{I_{RATING(MIN)}} < R_{DS(ON)} < \frac{\Delta V_{SC}}{I_{OUT(MAX)}}$$

where ΔV_{SC} is 90mV, 60mV or 150mV with IPRG being floated, tied to GND or V_{IN} respectively.

The power dissipated in the MOSFET strongly depends on its respective duty cycles and load current. When the LTC3809 is operating in continuous mode, the duty cycles for the MOSFETs are:

$$\text{Top P-Channel Duty Cycle} = \frac{V_{OUT}}{V_{IN}}$$

$$\text{Bottom N-Channel Duty Cycle} = \frac{V_{IN} - V_{OUT}}{V_{IN}}$$

The MOSFET power dissipations at maximum output current are:

$$P_{TOP} = \frac{V_{OUT}}{V_{IN}} \bullet I_{OUT(MAX)}^2 \bullet \rho_T \bullet R_{DS(ON)} + 2 \bullet V_{IN}^2 \bullet I_{OUT(MAX)} \bullet C_{RSS} \bullet f$$

$$P_{BOT} = \frac{V_{IN} - V_{OUT}}{V_{IN}} \bullet I_{OUT(MAX)}^2 \bullet \rho_T \bullet R_{DS(ON)}$$

Both MOSFETs have I^2R losses and the P_{TOP} equation includes an additional term for transition losses, which are largest at high input voltages. The bottom MOSFET losses are greatest at high input voltage or during a short-circuit when the bottom duty cycle is 100%.

The LTC3809 utilizes a non-overlapping, anti-shoot-through gate drive control scheme to ensure that the P- and N-channel MOSFETs are not turned on at the same time. To function properly, the control scheme requires that the MOSFETs used are intended for DC/DC switching applications. Many power MOSFETs, particularly P-channel MOSFETs, are intended to be used as static switches and therefore are slow to turn on or off.

Reasonable starting criteria for selecting the P-channel MOSFET are that it must typically have a gate charge (Q_G) less than 25nC to 30nC (at $4.5V_{GS}$) and a turn-off delay ($t_{D(OFF)}$) of less than approximately 140ns. However, due to differences in test and specification methods of various MOSFET manufacturers, and in the variations in Q_G and $t_{D(OFF)}$ with gate drive (V_{IN}) voltage, the P-channel MOSFET ultimately should be evaluated in the actual LTC3809 application circuit to ensure proper operation.

Shoot-through between the P-channel and N-channel MOSFETs can most easily be spotted by monitoring the input supply current. As the input supply voltage increases, if the input supply current increases dramatically, then the likely cause is shoot-through. Note that some MOSFETs

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that do not work well at high input voltages (e.g., V_{IN} > 5V) may work fine at lower voltages (e.g., 3.3V).

Selecting the N-channel MOSFET is typically easier, since for a given $R_{DS(ON)}$, the gate charge and turn-on and turn-off delays are much smaller than for a P-channel MOSFET.

Operating Frequency and Synchronization

The choice of operating frequency, f_{OSC}, is a trade-off between efficiency and component size. Low frequency operation improves efficiency by reducing MOSFET switching losses, both gate charge loss and transition loss. However, lower frequency operation requires more inductance for a given amount of ripple current.

The internal oscillator for the LTC3809's controller runs at a nominal 550kHz frequency when the PLLLPF pin is left floating and the SYNC/MODE pin is not configured for spread spectrum operation. Pulling the PLLLPF to V_{IN} selects 750kHz operation; pulling the PLLLPF to GND selects 300kHz operation.

Alternatively, the LTC3809 will phase-lock to a clock signal applied to the SYNC/MODE pin with a frequency between 250kHz and 750kHz (see Phase-Locked Loop and Frequency Synchronization).

To further reduce EMI, the nominal 550kHz frequency will be spread over a range with frequencies between 460kHz and 635kHz when spread spectrum modulation is enabled (see Spread Spectrum Modulation with SYNC/MODE and PLLLPF Pins).

Inductor Value Calculation

Given the desired input and output voltages, the inductor value and operating frequency, f_{OSC}, directly determine the inductor's peak-to-peak ripple current:

$$I_{RIPPLE} = \frac{V_{OUT}}{V_{IN}} \bullet \frac{V_{IN} - V_{OUT}}{f_{OSC} \bullet L}$$

Lower ripple current reduces core losses in the inductor, ESR losses in the output capacitors and output voltage ripple. Thus, highest efficiency operation is obtained at low frequency with a small ripple current. Achieving this, however, requires a large inductor.

A reasonable starting point is to choose a ripple current that is about 40% of $I_{OUT(MAX)}$. Note that the largest ripple current occurs at the highest input voltage. To guarantee that ripple current does not exceed a specified maximum, the inductor should be chosen according to:

$$L \geq \frac{V_{IN} - V_{OUT}}{f_{OSC} \bullet I_{RIPPLE}} \bullet \frac{V_{OUT}}{V_{IN}}$$

Burst Mode Operation Considerations

The choice of $R_{DS(ON)}$ and inductor value also determines the load current at which the LTC3809 enters Burst Mode operation. When bursting, the controller clamps the peak inductor current to approximately:

$$I_{BURST(PEAK)} = \frac{1}{4} \bullet \frac{\Delta V_{SENSE(MAX)}}{R_{DS(ON)}}$$

The corresponding average current depends on the amount of ripple current. Lower inductor values (higher I_{RIPPLE}) will reduce the load current at which Burst Mode operation begins.

The ripple current is normally set so that the inductor current is continuous during the burst periods. Therefore,

$$I_{RIPPLE} \leq I_{BURST(PEAK)}$$

This implies a minimum inductance of:

$$L_{MIN} \leq \frac{V_{IN} - V_{OUT}}{f_{OSC} \bullet I_{BURST(PEAK)}} \bullet \frac{V_{OUT}}{V_{IN}}$$

A smaller value than L_{MIN} could be used in the circuit, although the inductor current will not be continuous during burst periods, which will result in slightly lower efficiency. In general, though, it is a good idea to keep I_{RIPPLE} comparable to $I_{BURST(PEAK)}$.

Inductor Core Selection

Once the value of L is known, the type of inductor must be selected. High efficiency converters generally cannot afford the core loss found in low cost powdered iron cores, forcing the use of more expensive ferrite, molypermalloy or Kool Mμ® cores. Actual core loss is independent of core

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size for a fixed inductor value, but is very dependent on the inductance selected. As inductance increases, core losses go down. Unfortunately, increased inductance requires more turns of wire and therefore copper losses will increase.

Ferrite designs have very low core losses and are preferred at high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates "hard", which means that inductance collapses abruptly when the peak design current is exceeded. Core saturation results in an abrupt increase in inductor ripple current and consequent output voltage ripple. Do not allow the core to saturate!

Molypermalloy (from Magnetics, Inc.) is a very good, low loss core material for toroids, but is more expensive than ferrite. A reasonable compromise from the same manufacturer is Kool Mμ. Toroids are very space efficient, especially when several layers of wire can be used, while inductors wound on bobbins are generally easier to surface mount. However, designs for surface mount that do not increase the height significantly are available from Coiltronics, Coilcraft, Dale and Sumida.

Schottky Diode Selection (Optional)

The schottky diode D in Figure 11 conducts current during the dead time between the conduction of the power MOSFETs. This prevents the body diode of the bottom N-channel MOSFET from turning on and storing charge during the dead time, which could cost as much as 1% in efficiency. A 1A Schottky diode is generally a good size for most LTC3809 applications, since it conducts a relatively small average current. Larger diode results in additional transition losses due to its larger junction capacitance. This diode may be omitted if the efficiency loss can be tolerated.

C_{IN} and C_{OUT} Selection

In continuous mode, the source current of the P-channel MOSFET is a square wave of duty cycle (V_{OUT}/V_{IN}). To prevent large voltage transients, a low ESR input capacitor sized for the maximum RMS current must be used. The maximum RMS capacitor current is given by:

$$C_{IN}\,Required\,I_{RMS} \approx I_{MAX} \bullet \frac{V_{OUT} \bullet (V_{IN} - V_{OUT})^{1/2}}{V_{IN}}$$

This formula has a maximum value at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that capacitor manufacturer's ripple current ratings are often based on 2000 hours of life. This makes it advisable to further derate the capacitor or to choose a capacitor rated at a higher temperature than required. Several capacitors may be paralleled to meet the size or height requirements in the design. Due to the high operating frequency of the LTC3809, ceramic capacitors can also be used for C_{IN}. Always consult the manufacturer if there is any question.

The selection of C_{OUT} is driven by the effective series resistance (ESR). Typically, once the ESR requirement is satisfied, the capacitance is adequate for filtering. The output ripple (ΔV_{OUT}) is approximated by:

$$\Delta V_{OUT} \approx I_{RIPPLE} \bullet \left(ESR + \frac{1}{8 \bullet f \bullet C_{OUT}} \right)$$

where f is the operating frequency, C_{OUT} is the output capacitance and I_{RIPPLE} is the ripple current in the inductor. The output ripple is highest at maximum input voltage since I_{RIPPLE} increase with input voltage.

Setting Output Voltage

The LTC3809 output voltage is set by an external feedback resistor divider carefully placed across the output, as shown in Figure 3. The regulated output voltage is determined by:

$$V_{OUT} = 0.6V \bullet \left(1 + \frac{R_B}{R_A} \right)$$

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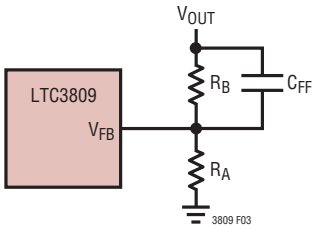


Figure 3. Settling Output Voltage

For most applications, a 59k resistor is suggested for R_A. In applications where minimizing the quiescent current is critical, R_A should be made bigger to limit the feedback divider current. If R_B then results in very high impedance, it may be beneficial to bypass R_B with a 50pF to 100pF capacitor C_{FF}.

Run and Soft-Start Functions

The LTC3809 has a low power shutdown mode which is controlled by the RUN pin. Pulling the RUN pin below 1.1V puts the LTC3809 into a low quiescent current shutdown mode (I_Q = 9µA). Releasing the RUN pin, an internal 0.7µA (at V_{IN} = 4.2V) current source will pull the RUN pin up to V_{IN}, which enables the controller. The RUN pin can be driven directly from logic as showed in Figure 4.

Once the controller is enabled, the start-up of V_{OUT} is controlled by the internal soft-start, which slowly ramps the positive reference to the error amplifier from 0V to 0.6V, allowing V_{OUT} to rise smoothly from 0V to its final value. The default internal soft-start time is around 1ms.

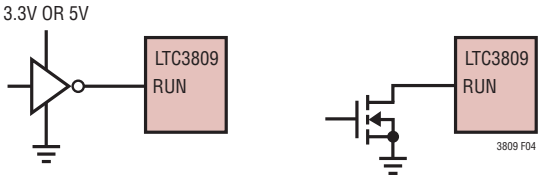


Figure 4. RUN Pin Interfacing

Phase-Locked Loop and Frequency Synchronization

The LTC3809 has a phase-locked loop (PLL) comprised of an internal voltage-controlled oscillator (VCO) and a phase detector. This allows the turn-on of the external P-channel MOSFET to be locked to the rising edge of an external clock signal applied to the SYNC/MODE pin. The phase detector is an edge sensitive digital type that provides zero degrees phase shift between the external and internal oscillators. This type of phase detector does not exhibit false lock to harmonics of the external clock.

The output of the phase detector is a pair of complementary current sources that charge or discharge the external filter network connected to the PLLLPF pin. The relationship between the voltage on the PLLLPF pin and operating frequency, when there is a clock signal applied to SYNC/MODE, is shown in Figure 5 and specified in the electrical characteristics table. Note that the LTC3809 can only be synchronized to an external clock whose frequency is within range of the LTC3809's internal VCO, which is nominally 200kHz to 1MHz. This is guaranteed, over temperature and process variations, to be between 250kHz and 750kHz. A simplified block diagram is shown in Figure 6.

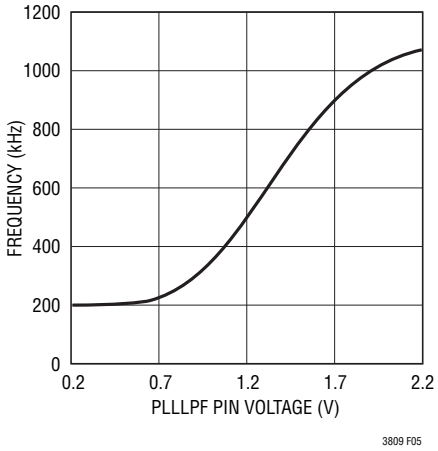


Figure 5. Relationship Between Oscillator Frequency and Voltage at the PLLLPF Pin When Synchronizing to an External Clock

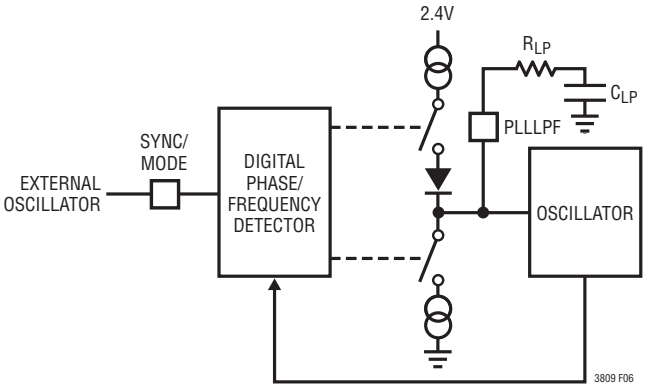


Figure 6. Phase-Locked Loop Block Diagram

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If the external clock frequency is greater than the internal oscillator's frequency, f_{OSC}, then current is sourced continuously from the phase detector output, pulling up the PLLLPF pin. When the external clock frequency is less than f_{OSC}, current is sunk continuously, pulling down the PLLLPF pin. If the external and internal frequencies are the same but exhibit a phase difference, the current sources turn on for an amount of time corresponding to the phase difference. The voltage on the PLLLPF pin is adjusted until the phase and frequency of the internal and external oscillators are identical. At the stable operating point, the phase detector output is high impedance and the filter capacitor C_{LP} holds the voltage.

The loop filter components, C_{LP} and R_{LP}, smooth out the current pulses from the phase detector and provide a stable input to the voltage-controlled oscillator. The filter components C_{LP} and R_{LP} determine how fast the loop acquires lock. Typically R_{LP} = 10k and C_{LP} is 2200pF to 0.01µF.

Typically, the external clock (on SYNC/MODE pin) input high level is 1.6V, while the input low level is 1.2V.

Table 1 summarizes the different states in which the PLLLPF pin can be used.

Table 1. The States of the PLLLPF Pin

PLLLPF PIN	SYNC/MODE PIN	FREQUENCY
0V	DC Voltage (<1.2V or V_{IN})	300kHz
Floating	DC Voltage (<1.2V or V_{IN})	550kHz
V_{IN}	DC Voltage (<1.2V or V_{IN})	750kHz
RC Loop Filter	Clock Signal	Phase-Locked to External Clock
Filter Caps	DC Voltage (>1.35V and <V_{IN} – 0.5V)	Spread Spectrum 460kHz to 635kHz

Auxiliary Winding Control Using SYNC/MODE Pin

The SYNC/MODE pin can be used as an auxiliary feedback to provide a means of regulating a flyback winding output. When this pin drops below its ground-referenced 0.4V threshold, continuous mode operation is forced.

During continuous mode, current flows continuously in the transformer primary side. The auxiliary winding draws current only when the bottom synchronous N-channel MOSFET is on. When primary load currents are low and/or the V_{IN}/V_{OUT} ratio is close to unity, the synchronous MOSFET may not be on for a sufficient amount of time to transfer power from the output capacitor to the auxiliary load. Forced continuous operation will support an auxiliary winding as long as there is a sufficient synchronous MOSFET duty factor. The SYNC/MODE input pin removes the requirement that power must be drawn from the transformer primary side in order to extract power from the auxiliary winding. With the loop in continuous mode, the auxiliary output may nominally be loaded without regard to the primary output load.

The auxiliary output voltage V_{AUX} is normally set, as shown in Figure 7, by the turns ratio N of the transformer:

$$V_{AUX} = (N + 1) \bullet V_{OUT}$$

However, if the controller goes into pulse-skipping operation and halts switching due to a light primary load current, then V_{AUX} will droop. An external resistor divider from V_{AUX} to the SYNC/MODE sets a minimum voltage $V_{AUX(MIN)}$:

$$V_{AUX(MIN)} = 0.4V \bullet \left(1 + \frac{R6}{R5}\right)$$

If V_{AUX} drops below this value, the SYNC/MODE voltage forces temporary continuous switching operation until V_{AUX} is again above its minimum.

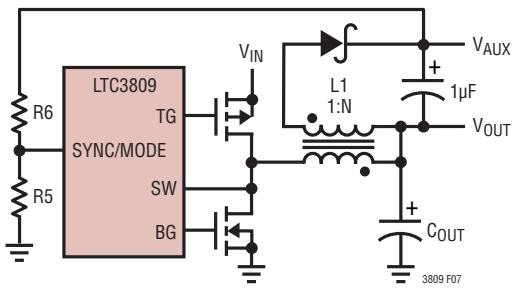


Figure 7. Auxilliary Output Loop Connection

Spread Spectrum Modulation with SYNC/MODE and PLLLPF Pins

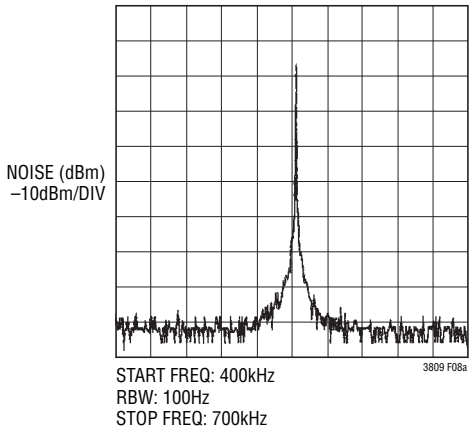
Switching regulators, which operate at fixed frequency, conduct electromagnetic interference (EMI) to their downstream load(s) with high spectral power density at this fundamental and harmonic frequencies. The peak energy

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can be lowered and distributed to other frequencies and their harmonics by modulating the PWM frequency. The LTC3809's switching noise (at 550kHz) is spread between 460kHz and 635kHz in spread spectrum modulation operation. Figure 8 shows the spectral plots of the output (V_{OUT}) noise with/without spread spectrum modulation. Note the significant reduction in peak output noise (>20dBm).

The spread spectrum modulation operation of the LTC3809 is enabled by setting SYNC/MODE pin to a DC voltage between 1.35V and several hundred mV below V_{IN} by tying a resistor between SYNC/MODE and V_{IN}.

V_{OUT} Spectrum without Spread Spectrum Modulation



V_{OUT} Spectrum with Spread Spectrum Modulation (C_{SSM} = 2200pF)

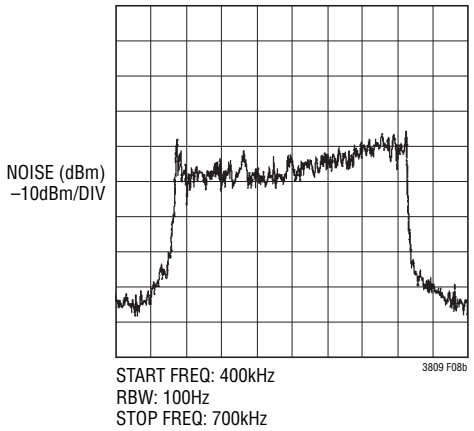


Figure 8. Spectral Response of Spread Spectrum Modulation

Table 2 summarizes the different states in which the SYNC/MODE Pin can be used.

Table 2. The States of the SYNC/MODE Pin

SYNC/MODE PIN	CONDITION
GND (0V to 0.35V)	Forced Continuous Mode Current Reversal Allowed
V_{FB} (0.45V to 1.2V)	Pulse-Skipping Mode No Current Reversal Allowed
Resistor to V_{IN} (1.35V to V_{IN} – 0.5V)	Spread Spectrum Modulation Pulse Skipping at Light Loads No Current Reversal Allowed
V_{IN}	Burst Mode Operation No Current Reversal Allowed
Feedback Resistors	Regulate an Auxiliary Winding
External Clock Signal	Enable Phase-Locked Loop (Synchronize to External Clock) Pulse Skipping at Light Load No Current Reversal Allowed

Fault Condition: Short-Circuit and Current Limit

If the LTC3809's load current exceeds the short-circuit current limit (I_{SC}), which is set by the short-circuit sense threshold (ΔV_{SC}) and the on resistance ($R_{DS(ON)}$) of bottom N-channel MOSFET, the top P-channel MOSFET is turned off and will not be turned on at the next clock cycle unless the load current decreases below I_{SC}. In this case, the controller's switching frequency is decreased and the output is regulated by short-circuit (current limit) protection.

In a hard short (V_{OUT} = 0V), the top P-channel MOSFET is turned off and kept off until the short-circuit condition is cleared. In this case, there is no current path from input supply (V_{IN}) to either V_{OUT} or GND, which prevents excessive MOSFET and inductor heating.

Low Input Supply Voltage

Although the LTC3809 can function down to below 2.4V, the maximum allowable output current is reduced as V_{IN} decreases below 3V. Figure 9 shows the amount of change as the supply is reduced down to 2.4V. Also shown is the effect on V_{REF}.

APPLICATIONS INFORMATION

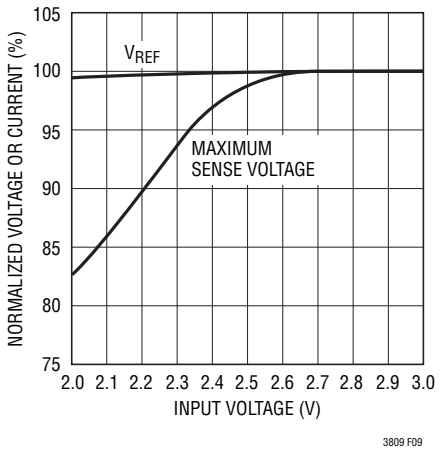


Figure 9. Line Regulation of V_{REF} and Maximum Sense Voltage

Minimum On-Time Considerations

Minimum on-time, $t_{ON(MIN)}$ is the smallest amount of time that the LTC3809 is capable of turning the top P-channel MOSFET on. It is determined by internal timing delays and the gate charge required to turn on the top MOSFET. Low duty cycle and high frequency applications may approach the minimum on-time limit and care should be taken to ensure that:

$$t_{ON(MIN)} < \frac{V_{OUT}}{f_{OSC} \bullet V_{IN}}$$

If the duty cycle falls below what can be accommodated by the minimum on-time, the LTC3809 will begin to skip cycles (unless forced continuous mode is selected). The output voltage will continue to be regulated, but the ripple current and ripple voltage will increase. The minimum on-time for the LTC3809 is typically about 210ns. However, as the peak sense voltage ($I_{L(PEAK)} \bullet R_{DS(ON)}$) decreases, the minimum on-time gradually increases up to about 260ns. This is of particular concern in forced continuous applications with low ripple current at light loads. If forced continuous mode is selected and the duty cycle falls below the minimum on time requirement, the output will be regulated by overvoltage protection.

Efficiency Considerations

The efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting efficiency and which change would produce the most improvement. Efficiency can be expressed as:

Efficiency = 100% – (L1 + L2 + L3 + …)

where L1, L2, etc. are the individual losses as a percentage of input power.

Although all dissipative elements in the circuit produce losses, four main sources usually account for most of the losses in LTC3809 circuits: 1) LTC3809 DC bias current, 2) MOSFET gate-charge current, 3) I^2R losses and 4) transition losses.

1) The V_{IN} (pin) current is the DC supply current, given in the Electrical Characteristics, which excludes MOSFET driver currents. V_{IN} current results in a small loss that increases with V_{IN}.

2) MOSFET gate-charge current results from switching the gate capacitance of the power MOSFET. Each time a MOSFET gate is switched from low to high to low again, a packet of charge dQ moves from V_{IN} to ground. The resulting dQ/dt is a current out of V_{IN}, which is typically much larger than the DC supply current. In continuous mode, $I_{GATECHG} = f \bullet Q_P$.

3) I^2R losses are calculated from the DC resistances of the MOSFETs, inductor and/or sense resistor. In continuous mode, the average output current flows through L but is "chopped" between the top P-channel MOSFET and the bottom N-channel MOSFET. The MOSFET $R_{DS(ON)}$ multiplied by duty cycle can be summed with the resistance of L to obtain I^2R losses.

4) Transition losses apply to the external MOSFET and increase with higher operating frequencies and input voltages. Transition losses can be estimated from:

Transition Loss = $2 \bullet V_{IN}^2 \bullet I_{O(MAX)} \bullet C_{RSS} \bullet f$

Other losses, including C_{IN} and C_{OUT} ESR dissipative losses and inductor core losses, generally account for less than 2% total additional loss.

Checking Transient Response

The regulator loop response can be checked by looking at the load transient response. Switching regulators take several cycles to respond to a step in load current. When a load step occurs, V_{OUT} immediately shifts by an amount

APPLICATIONS INFORMATION

equal to (ΔI_{LOAD}) • (ESR), where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT} generating a feedback error signal used by the regulator to return V_{OUT} to its steady-state value. During this recovery time, V_{OUT} can be monitored for overshoot or ringing that would indicate a stability problem. OPTI-LOOP compensation allows the transient response to be optimized over a wide range of output capacitance and ESR values.

The I_{TH} series R_C-C_C filter (see Functional Diagram) sets the dominant pole-zero loop compensation.

The I_{TH} external components showed in the figure on the first page of this data sheet will provide adequate compensation for most applications. The values can be modified slightly (from 0.2 to 5 times their suggested values) to optimize transient response once the final PC layout is done and the particular output capacitor type and value have been determined. The output capacitor needs to be decided upon because the various types and values determine the loop feedback factor gain and phase. An output current pulse of 20% to 100% of full load current having a rise time of 1µs to 10µs will produce output voltage and I_{TH} pin waveforms that will give a sense of the overall loop stability. The gain of the loop will be increased by increasing R_C and the bandwidth of the loop will be increased by decreasing C_C. The output voltage settling behavior is related to the stability of the closed-loop system and will demonstrate the actual overall supply performance. For a detailed explanation of optimizing the compensation components, including a review of control loop theory, refer to Application Note 76.

A second, more severe transient is caused by switching in loads with large (>1µF) supply bypass capacitors. The discharged bypass capacitors are effectively put in parallel with C_{OUT}, causing a rapid drop in V_{OUT}. No regulator can deliver enough current to prevent this problem if the load switch resistance is low and it is driven quickly. The only solution is to limit the rise time of the switch drive so that the load rise time is limited to approximately (25) • (C_{LOAD}). Thus a 10µF capacitor would be require a 250µs rise time, limiting the charging current to about 200mA.

Design Example

As a design example, assume V_{IN} will be operating from a maximum of 4.2V down to a minimum of 2.75V (powered by a single lithium-ion battery). Load current requirement is a maximum of 2A, but most of the time it will be in a standby mode requiring only 2mA. Efficiency at both low and high load currents is important. Burst Mode operation at light loads is desired. Output voltage is 1.8V. The IPRG pin will be left floating, so the maximum current sense threshold $\Delta V_{SENSE(MAX)}$ is approximately 125mV.

$$\text{Maximum Duty Cycle} = \frac{V_{OUT}}{V_{IN(MIN)}} = 65.5\%$$

From Figure 1, SF = 82%.

$$R_{DS(ON)MAX} = \frac{5}{6} \bullet 0.9 \bullet SF \bullet \frac{\Delta V_{SENSE(MAX)}}{I_{OUT(MAX)} \bullet \rho T} = 0.032\Omega$$

A 0.032Ω P-channel MOSFET in Si7540DP is close to this value.

The N-channel MOSFET in Si7540DP has 0.017Ω $R_{DS(ON)}$. The short circuit current is:

$$I_{SC} = \frac{90mV}{0.017\Omega} = 5.3A$$

So the inductor current rating should be higher than 5.3A.

The PLLLPF pin will be left floating, so the LTC3809 will operate at its default frequency of 550kHz. For continuous Burst Mode operation with 600mA I_{RIPPLE}, the required minimum inductor value is:

$$L_{MIN} = \frac{1.8V}{550kHz \bullet 600mA} \bullet \left(1 - \frac{1.8V}{2.75V}\right) = 1.88\mu H$$

A 6A 2.2µH inductor works well for this application.

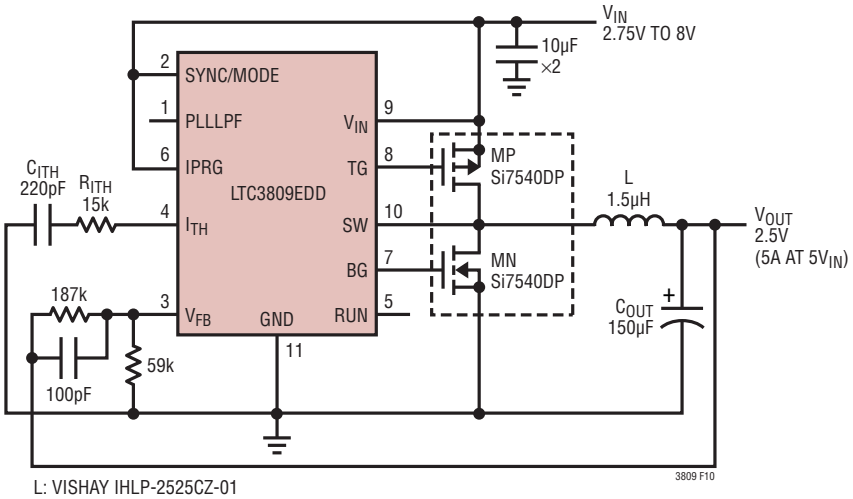
C_{IN} will require an RMS current rating of at least 1A at temperature. A C_{OUT} with 0.1Ω ESR will cause approximately 60mV output ripple.

APPLICATIONS INFORMATION

PC Board Layout Checklist

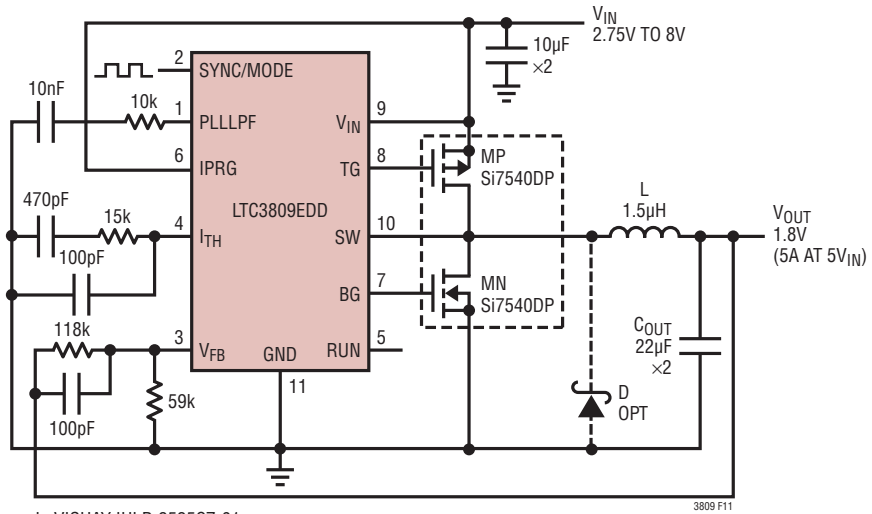
When laying out the printed circuit board, use the following checklist to ensure proper operation of the LTC3809.

- The power loop (input capacitor, MOSFET, inductor, output capacitor) should be as small as possible and isolated as much as possible from LTC3809.
- Put the feedback resistors close to the V_{FB} pins. The I_{TH} compensation components should also be very close to the LTC3809.
- The current sense traces should be Kelvin connections right at the P-channel MOSFET source and drain.
- Keeping the switch node (SW) and the gate driver nodes (TG, BG) away from the small-signal components, especially the feedback resistors, and I_{TH} compensation components.



L: VISHAY IHLP-2525CZ-01
C_{OUT}: SANYO 4TPB150MC

Figure 10. 550kHz, Synchronizable DC/DC Converter with Internal Soft-Start

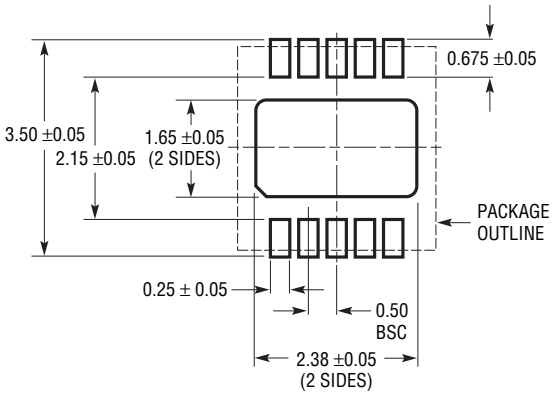


L: VISHAY IHLP-2525CZ-01
D: ON SEMI MBRM120L (OPTIONAL)

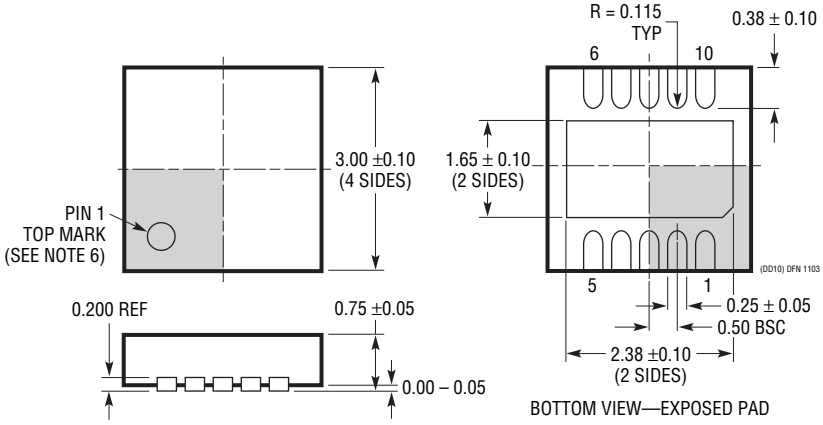
Figure 11. Synchronizable DC/DC Converter with Ceramic Output Capacitors

TYPICAL APPLICATIONS

DD Package
10-Lead Plastic DFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1699)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS

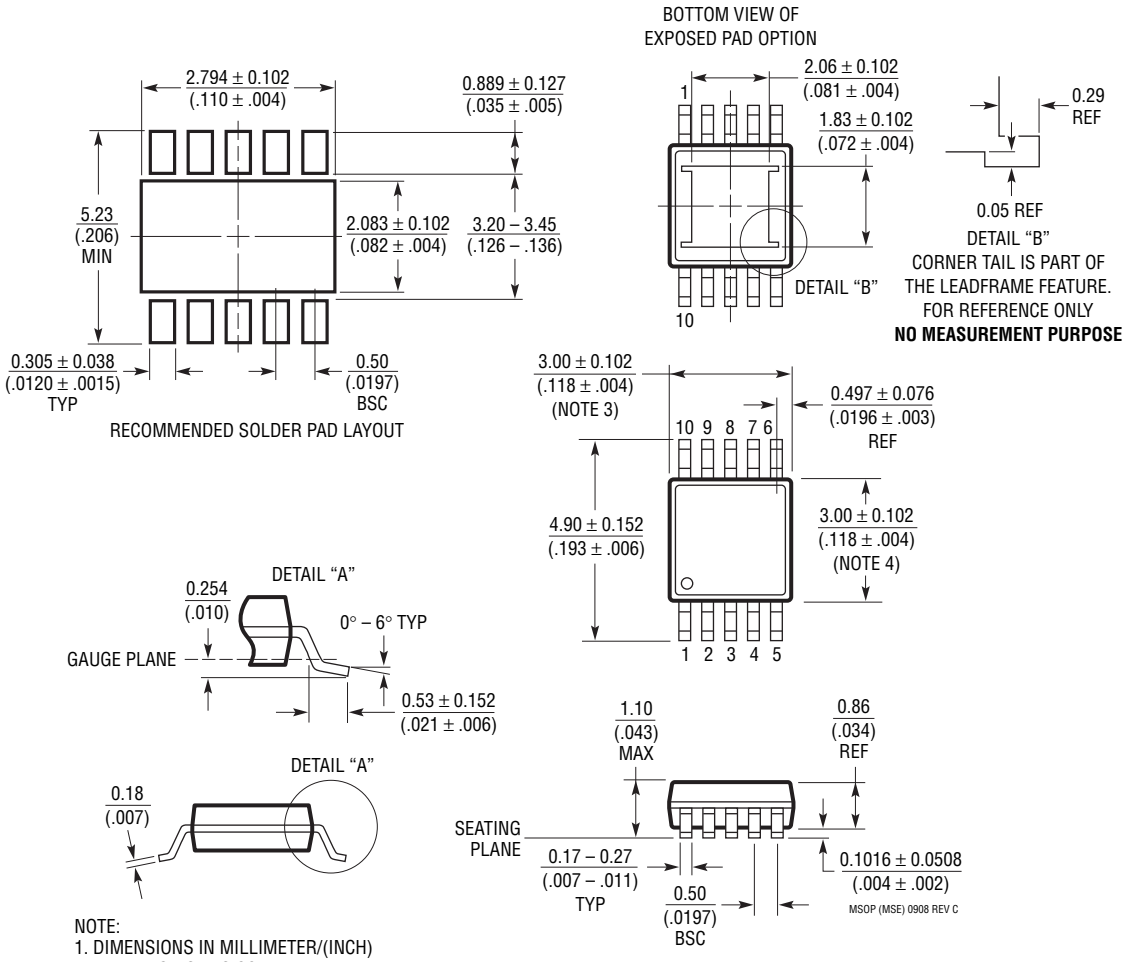


BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-2). CHECK THE LTC WEBSITE DATA SHEET FOR CURRENT STATUS OF VARIATION ASSIGNMENT
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

MSE Package
10-Lead Plastic MSOP, Exposed Die Pad
(Reference LTC DWG # 05-08-1664 Rev C)

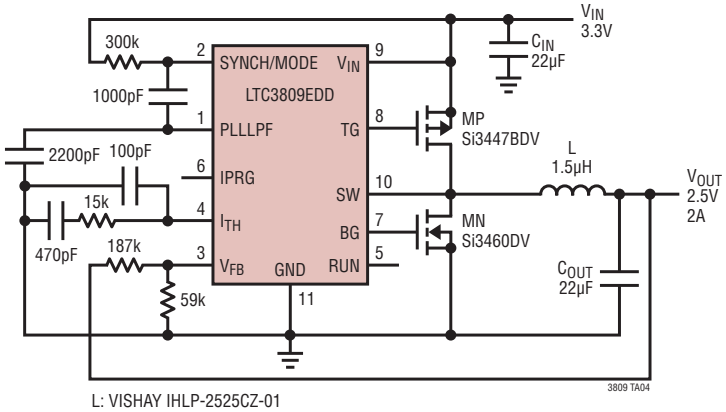


NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

TYPICAL APPLICATION

Synchronous DC/DC Converter with Spread Spectrum Modulation



L: VISHAY IHLP-2525CZ-01

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1628/LTC3728	Dual High Efficiency, 2-Phase Synchronous Step Down Controllers	Constant Frequency, Standby, 5V and 3.3V LDOs, V_{IN} to 36V, 28-Lead SSOP
LTC1735	High Efficiency Synchronous Step-Down Controller	Burst Mode Operation, 16-Pin Narrow SSOP, Fault Protection, $3.5V \le V_{IN} \le 36V$
LTC1778	No R_{SENSE}, Synchronous Step-Down Controller	Current Mode Operation Without Sense Resistor, Fast Transient Response, $4V \le V_{IN} \le 36V$
LTC3411	1.25A (I_{OUT}), 4MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 2.5V to 5.5V, $V_{OUT} \ge 0.8V$, I_Q = 60µA, I_{SD} = <1µA, MS Package
LTC3412	2.5A (I_{OUT}), 4MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 2.5V to 5.5V, $V_{OUT} \ge 0.8V$, I_Q = 60µA, I_{SD} = <1µA, TSSOP-16E Package
LTC3416	4A, 4MHz, Monolithic Synchronous Step-Down Regulator	Tracking Input to Provide Easy Supply Sequencing, $2.25V \le V_{IN} \le 5.5V$, 20-Lead TSSOP Package
LTC3418	8A, 4MHz, Synchronous Step-Down Regulator	Tracking Input to Provide Easy Supply Sequencing, $2.25V \le V_{IN} \le 5.5V$, QFN Package
LTC3708	2-Phase, No R_{SENSE}, Dual Synchronous Controller with Output Tracking	Constant On-Time Dual Controller, V_{IN} Up to 36V, Very Low Duty Cycle Operation, 5mm × 5mm QFN Package
LTC3736/LTC3736-2	2-Phase, No R_{SENSE}, Dual Synchronous Controller with Output Tracking	$2.75V \le V_{IN} \le 9.8V$, $0.6V \le V_{OUT} \le V_{IN}$, 4mm × 4mm QFN
LTC3736-1	Low EMI 2-Phase, Dual Synchronous Controller with Output Tracking	Integrated Spread Spectrum for 20dB Lower "Noise," $2.75V \le V_{IN} \le 9.8V$
LTC3737	2-Phase, No R_{SENSE}, Dual DC/DC Controller with Output Tracking	$2.75V \le V_{IN} \le 9.8V$, $0.6V \le V_{OUT} \le V_{IN}$, 4mm × 4mm QFN
LTC3772	Micropower No R_{SENSE} Step-Down DC/DC Controller	$2.75V \le V_{IN} \le 9.8V$, 3mm × 2mm DFN or 8-Lead SOT-23, 550kHz, I_Q = 40µA, Current Mode
LTC3776	Dual, 2-Phase, No R_{SENSE} Synchronous Controller for DDR/QDR Memory Termination	Provides V_{DDQ} and V_{TT} with One IC, $2.75V \le V_{IN} \le 9.8V$, Adjustable Constant Frequency with PLL Up to 850kHz, Spread Spectrum Operation, 4mm × 4mm QFN and 24-Lead SSOP Packages
LTC3808	Low EMI, Synchronous Controller with Output Tracking	$2.75V \le V_{IN} \le 9.8V$, 4mm × 3mm DFN, Spread Spectrum for 20dB Lower Peak Noise
LTC3809-1	No R_{SENSE} Synchronous Controller with Output Tracking	$2.75V \le V_{IN} \le 9.8V$, 3mm × 3mm DFN and 10-Lead MSOPE Packages

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