3-Phase, Buck Controllers for AMD CPUs

FEATURES

- **3-Phase Controller with Onboard MOSFET Drivers**
- **Current Mode Control Ensures Current Sharing**
- **Differential Amplifier Accurately Senses V_{OUT}**
- **±5% Output Current Matching Optimizes Thermal Performance and Size of Inductors and MOSFETs**
- Reduced Input and Output Capacitance
- Supports Active Voltage Positioning
- VID Programmable Output Voltage from 0.8V to 1.55V (AMD Opteron™ CPU)
- 6-Phase, 90A to 120A Operation
- Output Power Good Indicator with Adaptive Blanking
- 210kHz to 530kHz Per Phase, PLL, Fixed Frequency
- Synchronizable (LTC3733-1)
- PWM, Stage Shedding or Burst Mode® Operation
- OPTI-LOOP® Compensation Minimizes C_{OUT}
- Adjustable Soft-Start Current Ramping
- Short-Circuit Shutdown Timer with Defeat Option
- No_CPU Detection
- 36-Lead 0.209" SSOP and 38-Lead (5mm × 7mm) QFN

APPLICATIONS

- High Performance Notebook Computers
- Servers, Desktop Computers and Workstations

DESCRIPTION

The LTC®3733 family are PolyPhase® synchronous step-down switching regulator controllers that drive all N-channel external power MOSFET stages in a phase-lockable, fixed frequency architecture. The 3-phase controller drives its output stages with 120° phase separation at frequencies of up to 530kHz per phase to minimize the RMS current dissipated by the ESR of both the input and output filter capacitors. The 3-phase technique effectively triples the fundamental frequency, improving transient response while operating each phase at an optimal frequency for efficiency and ease of thermal design. Light load efficiency is optimized by using a choice of output stage shedding or Burst Mode technology.

A differential amplifier provides true remote sensing of both the high and low sides of the output voltage at load points.

Soft-start and a defeatable, timed short-circuit shutdown protect the MOSFETs and the load. A foldback current circuit also provides protection for the external MOSFETs under short-circuit or overload conditions. An all-"1" VID detector turns off the regulator after 1µs timeout.

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TYPICAL APPLICATION

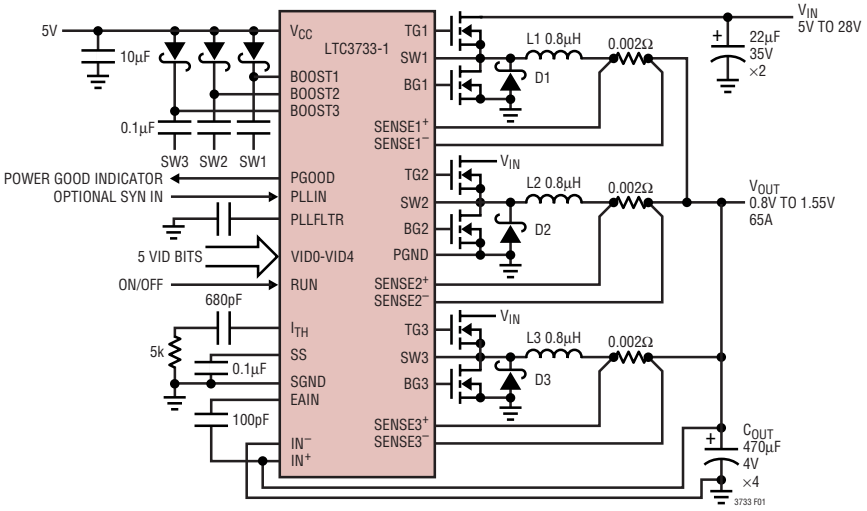


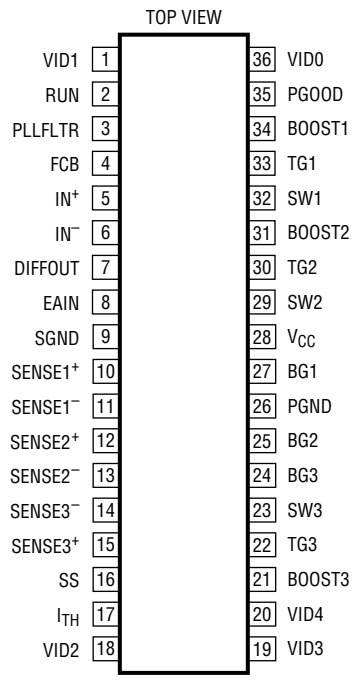
Figure 1. High Current Triple Phase Step-Down Converter

ABSOLUTE MAXIMUM RATINGS (Note 1)

Topside Driver Voltages ($BOOST_N$) ..... 38V to –0.3V
Switch Voltage (SW_N) ..... 32V to –5V
Boosted Driver Voltage ($BOOST_N – SW_N$) .... 7V to –0.3V
Peak Output Current <1ms (TG_N, BG_N) 5A
Supply Voltage (V_{CC}), PGOOD
Pin Voltages ..... 7V to –0.3V
PLLIN, RUN, SS,
PLLFLTR, FCB Voltages ..... V_{CC} to –0.3V

I_{TH} Voltage ..... 2.4V to –0.3V
Operating Ambient Temperature Range ..... 0°C to 70°C
Junction Temperature (Note 2) ..... 125°C
Storage Temperature Range
LTC3733CG ..... –65°C to 150°C
LTC3733CUHF-1 ..... –65°C to 125°C
Lead Temperature (LTC3733CG)
(Soldering, 10 sec) ..... 300°C

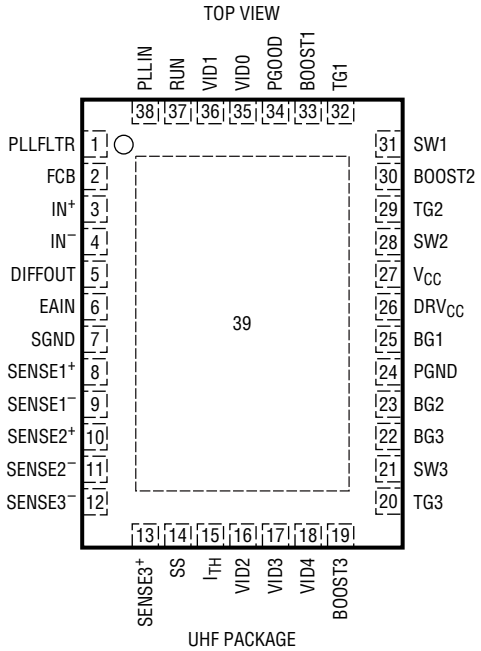
PACKAGE/ORDER INFORMATION



G PACKAGE
36-LEAD PLASTIC SSOP
T_{JMAX} = 125°C, θ_{JA} = 95°C/W

ORDER PART NUMBER

LTC3733CG



UHF PACKAGE
38-LEAD (7mm × 5mm) PLASTIC QFN
T_{JMAX} = 125°C, θ_{JA} = 34°C/W
EXPOSED PAD IS SGND (PIN 39) MUST BE SOLDERED TO PCB

ORDER PART NUMBER

LTC3733CUHF-1

UHF PART MARKING

37331

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = V_{RUN} = V_{SS} = 5V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Main Control Loop							
$V_{REGULATED}$	Regulated Voltage at IN+	(Note 3); VID Code = 10011, V_{ITH} = 1.2V		1.067	1.075	1.083	V
			●	1.064	1.075	1.086	V
$V_{SENSEMAX}$	Maximum Current Sense Threshold	V_{EAIN} = 0.5V, V_{ITH} Open, $V_{SENSE1–}$, $V_{SENSE2–}$, $V_{SENSE3–}$ = 0.8V, 1.55V		65	75	85	mV
			●	62	75	88	mV
I_{MATCH}	Current Match	Worst-Case Error at $V_{SENSE(MAX)}$		–5		5	%

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = V_{RUN} = V_{SS} = 5V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$V_{LOADREG}$	Output Voltage Load Regulation	(Note 3) Measured in Servo Loop, ΔI_{TH} Voltage = 1.2V to 0.7V Measured in Servo Loop, ΔI_{TH} Voltage = 1.2V to 2V	 ● ●		 0.1 –0.1	 0.5 –0.5	 % %
$V_{REFLNREG}$	Output Voltage Line Regulation	V_{CC} = 4.5V to 7V			0.03		%/V
g_m	Transconductance Amplifier g_m	I_{TH} = 1.2V, Sink/Source 25µA (Note 3)		2.5	3.05	3.6	mmho
g_{mOL}	Transconductance Amplifier GBW	I_{TH} = 1.2V, (g_m • Z_L, Z_L = Series 1k-100kΩ-1nF)			1.5		MHz
V_{FCB}	Forced Continuous Threshold		●	0.58	0.60	0.62	V
I_{FCB}	FCB Bias Current	V_{FCB} = 0.65V			0.2	0.7	µA
$V_{BINHIBIT}$	Burst Inhibit Threshold	Measured at FCB pin		V_{CC} – 1.5	V_{CC} – 0.7	V_{CC} – 0.3	V
UVR	Undervoltage SS Reset	V_{CC} Lowered Until the SS Pin is Pulled Low		3.3	3.8	4.5	V
I_Q	Input DC Supply Current Normal Mode Shutdown	(Note 4) V_{CC} = 5V V_{RUN} = 0V, VID0 to VID4 Open		 	 2.5 20	 100	 mA µA
V_{RUN}	RUN Pin ON Threshold	V_{RUN}, Ramping Positive		1	1.5	1.9	V
I_{SS}	Soft-Start Charge Current	V_{SS} = 1.9V		–0.8	–1.5	–2.5	µA
V_{SSARM}	SS Pin Arming Threshold	V_{SS}, Ramping Positive Until Short-Circuit Latch-Off is Armed			3.8	4.5	V
V_{SSLO}	SS Pin Latch-Off Threshold	V_{SS}, Ramping Negative			3.3		V
I_{SCL}	SS Discharge Current	Soft-Short Condition V_{EAIN} = 0.375V, V_{SS} = 4.5V		–5	–1.5		µA
I_{SDLHO}	Shutdown Latch Disable Current	V_{EAIN} = 0.375V, V_{SS} = 4.5V			1.5	5	µA
I_{SENSE}	SENSE Pins Source Current	SENSE1+, SENSE1–, SENSE2+, SENSE2–, SENSE3+, SENSE3– All Equal 1.2V; Current at Each Pin			13	20	µA
DF_{MAX}	Maximum Duty Factor	In Dropout		95	98.5		%
TG t_R, t_F	Top Gate Rise Time Top Gate Fall Time	C_{LOAD} = 3300pF C_{LOAD} = 3300pF			30 40	90 90	ns ns
BG t_R, t_F	Bottom Gate Rise Time Bottom Gate Fall Time	C_{LOAD} = 3300pF C_{LOAD} = 3300pF			30 20	90 90	ns ns
TG/BG t_{1D}	Top Gate Off to Bottom Gate On Delay Synchronous Switch-On Delay Time	All Controllers, C_{LOAD} = 3300pF Each Driver			60		ns
BG/TG t_{2D}	Bottom Gate Off to Top Gate On Delay Top Switch-On Delay Time	All Controllers, C_{LOAD} = 3300pF Each Driver			60		ns
$t_{ON(MIN)}$	Minimum On-Time	Tested with a Square Wave (Note 5)			120		ns
VID Parameters							
VID_{IL}	Maximum Low Level Input Voltage					0.8	V
VID_{IH}	Minimum High Level Input Voltage			2			V
VID_{PULLUP}	VID0 to VID4 Internal Pull-Up Resistance				150		kΩ
$ATTEN_{ERR}$	VID0 to VID4	(Note 6)	●	–0.25		0.25	%
Power Good Output Indication							
V_{PGL}	PGOOD Voltage Output Low	I_{PGOOD} = 2mA			0.1	0.3	V
I_{PGOOD}	PGOOD Output Leakage	V_{PGOOD} = 5V				±1	µA
 $V_{PGTHNEG}$ $V_{PGTHPOS}$	PGOOD Trip Thesholds $V_{DIFFOUT}$ Ramping Negative $V_{DIFFOUT}$ Ramping Positive	$V_{DIFFOUT}$ with Respect to Set Output Voltage, VID Code = 10011 PGOOD Goes Low After V_{UVDLY} Delay		 –7 7	 –10 10	 –14 14	 % %
t_{PGBLNK}	Power Good Blanking	After VID Changes Outside PGOOD Window			120		µs

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = V_{RUN} = V_{SS} = 5V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Oscillator and Phase-Locked Loop							
f_{NOM}	Nominal Frequency	$V_{PLLFLTR}$ = 1.2V		310	350	400	kHz
f_{LOW}	Lowest Frequency	$V_{PLLFLTR}$ = 0V		190	210	250	kHz
f_{HIGH}	Highest Frequency	$V_{PLLFLTR}$ = 2.4V		470	530	620	kHz
R_{PLLTH}	PLLIN Input Threshold	LTC3733-1 Only			1		V
$R_{PLL\ IN}$	PLLIN Input Resistance	LTC3733-1 Only			50		kΩ
$I_{PLL\ LPF}$	Phase Detector Output Current Sinking Capability Sourcing Capability	LTC3733-1 Only $f_{PLLIN} < f_{OSC}$ $f_{PLLIN} > f_{OSC}$			 20 20		 µA µA
R_{RELPHS}	Controller 2-Controller 1 Phase Controller 3-Controller 1 Phase				120 240		Deg Deg
No_CPU Detection							
t_{NOCPU}	No-CPU Shutdown Latency	After All VID Bits = "1"		0.5	1		µs
Differential Amplifier							
A_V	Differential Gain			0.995	1.000	1.005	V/V
V_{OS}	Input Offset Voltage	$IN^+ = IN^- = 1.2V$, I_{OUT} = 1mA, Input Referred; Gain = 1			0.5	5	mV
CM	Common Mode Input Voltage Range			0		5	V
CMRR	Common Mode Rejection Ratio	$0V < IN^+ = IN^- < 5V$, I_{OUT} = 1mA, Input Referred		50	70		dB
I_{CL}	Output Current			10	40		mA
GBP	Gain Bandwidth Product				2		MHz
SR	Slew Rate	R_L = 2k			5		V/µs
$V_{O(MAX)}$	Maximum High Output Voltage	I_{OUT} = 1mA		V_{CC} – 1.2	V_{CC} – 0.8		V
R_{IN}	Input Resistance	Measured at IN^+ Pin			80		kΩ

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formula:

LTC3733CG: $T_J = T_A + (P_D \times 95°C/W)$

LTC3733CUHF-1: $T_J = T_A + (P_D \times 34°C/W)$

Note 3: The IC is tested in a feedback loop that includes the differential amplifier in a unity-gain configuration loaded with 100µA to ground driving the VID DAC into the error amplifier and servoing the resultant voltage to the midrange point for the error amplifier (V_{ITH} = 1.2V).

Note 4: Dynamic supply current is higher due to the gate charge being delivered at the switching frequency. See Applications Information.

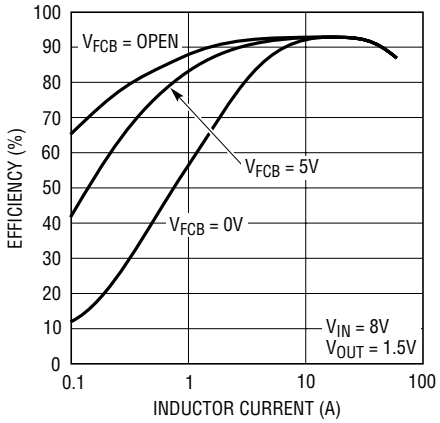
Note 5: The minimum on-time condition corresponds to an inductor peak-to-peak ripple current of ≥40% of I_{MAX} (see minimum on-time considerations in the Applications Information Section).

Note 6: $ATTEN_{ERR}$ specification is in addition to the output voltage accuracy specified at VID code 10011.

Note 7: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

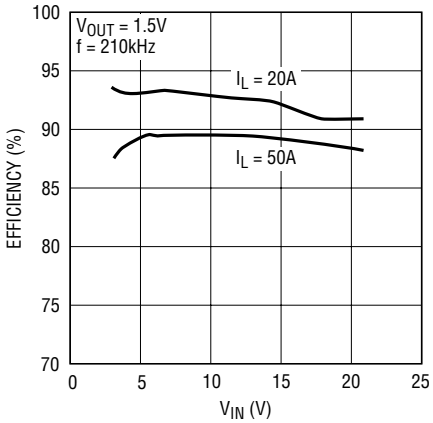
TYPICAL PERFORMANCE CHARACTERISTICS

Efficiency vs I_{OUT}



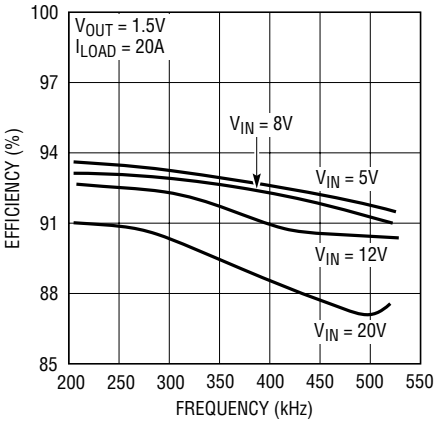
3733 G01

Efficiency vs V_{IN}



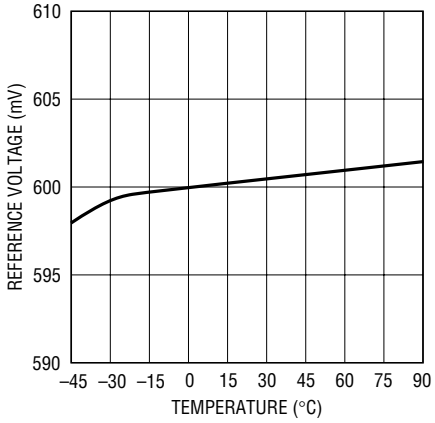
3733 G02

Efficiency vs Frequency



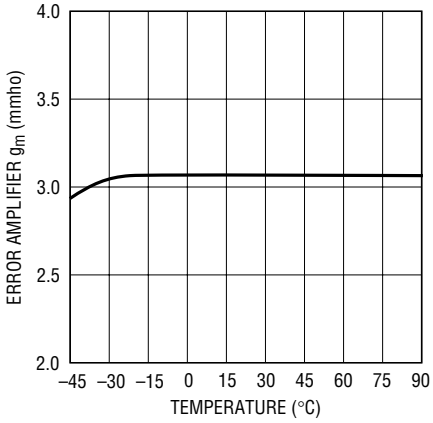
3733 G03

Reference Voltage vs Temperature



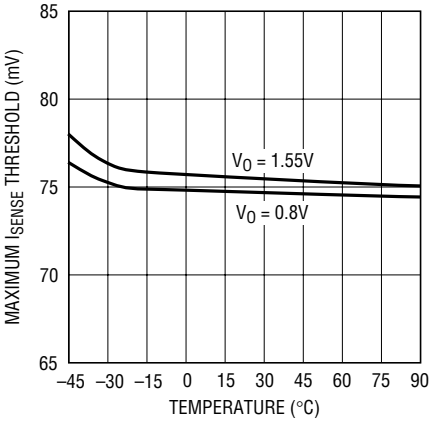
3733 G04

Error Amplifier g_m vs Temperature



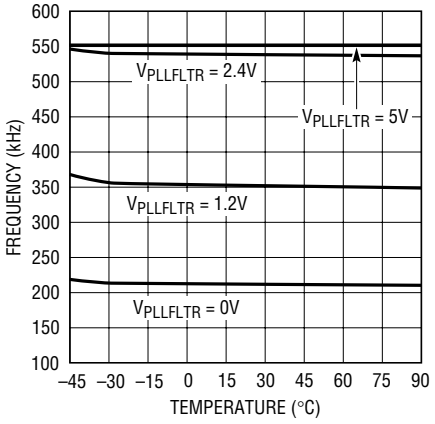
3733 G05

Maximum I_{SENSE} Threshold vs Temperature



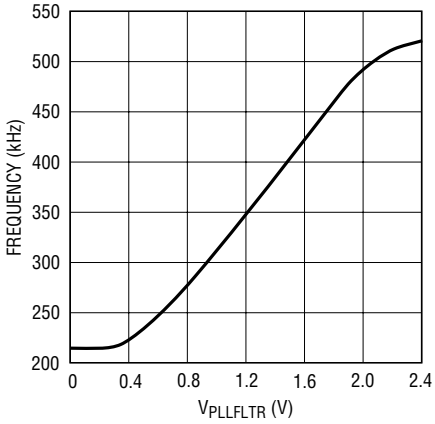
3733 G06

Oscillator Frequency vs Temperature



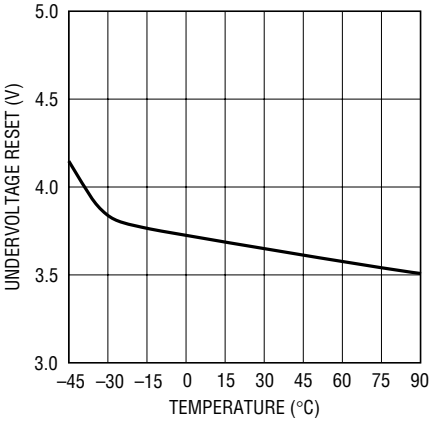
3733 G07

Oscillator Frequency vs $V_{PLLFLTR}$



3733 G08

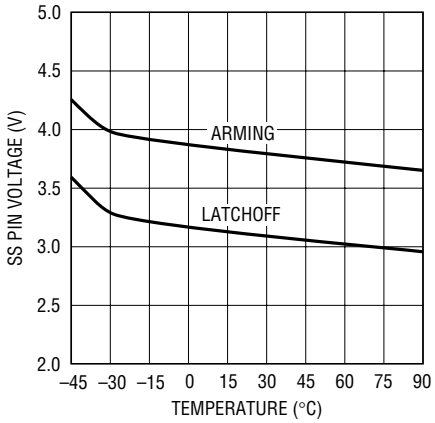
Undervoltage Reset Voltage vs Temperature



3733 G09

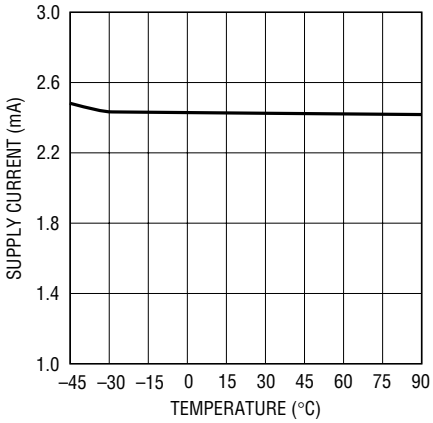
TYPICAL PERFORMANCE CHARACTERISTICS

Short-Circuit Arming and Latchoff vs Temperature



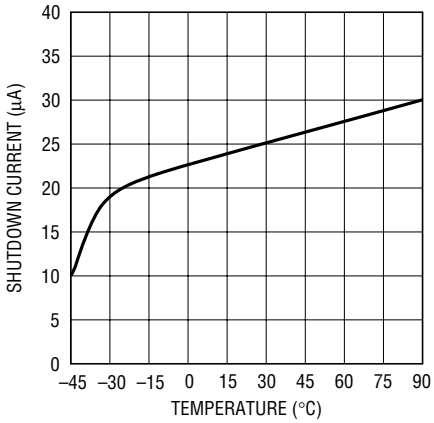
3733 G10

Supply Current vs Temperature



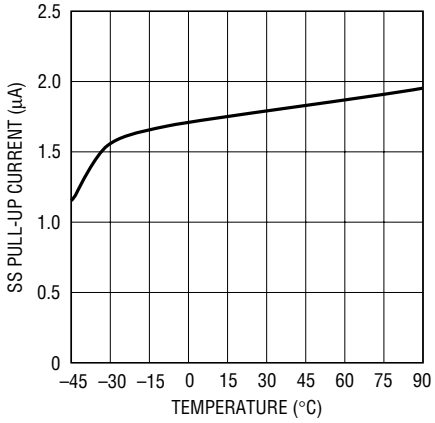
3733 G11

Shutdown Current vs Temperature



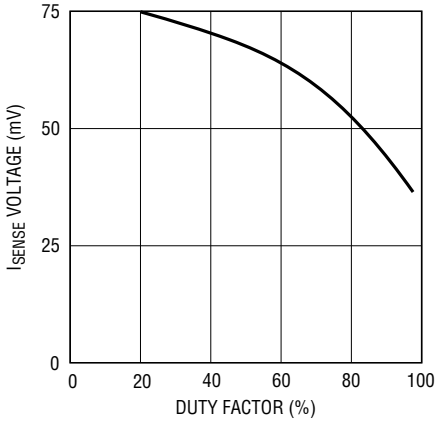
3733 G12

SS Pull-Up Current vs Temperature



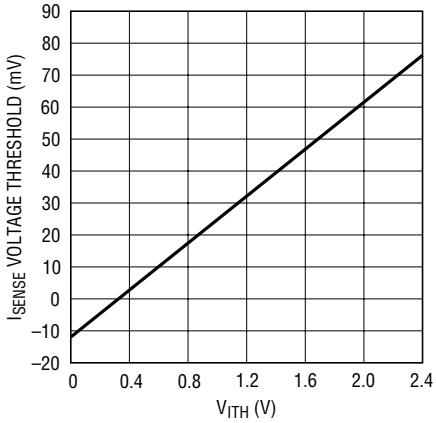
3733 G13

Maximum Current Sense Threshold vs Duty Factor



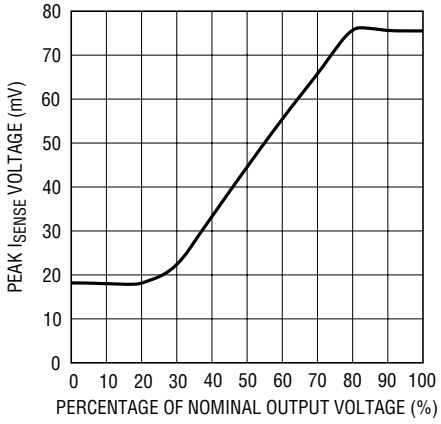
3733 G14

Peak Current Threshold vs V_{ITH}



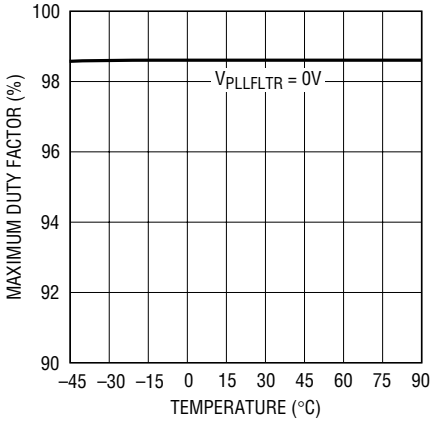
3733 G15

Percentage of Nominal Output vs Peak I_{SENSE} (Foldback)



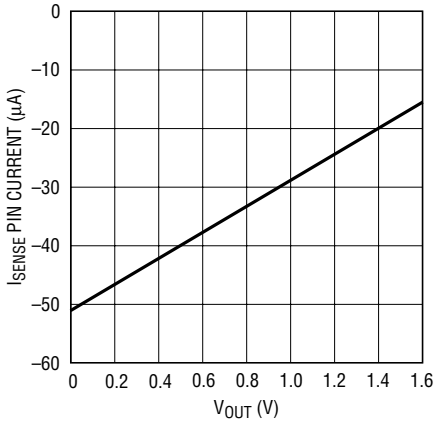
3733 G16

Maximum Duty Factors vs Temperature



3733 G17

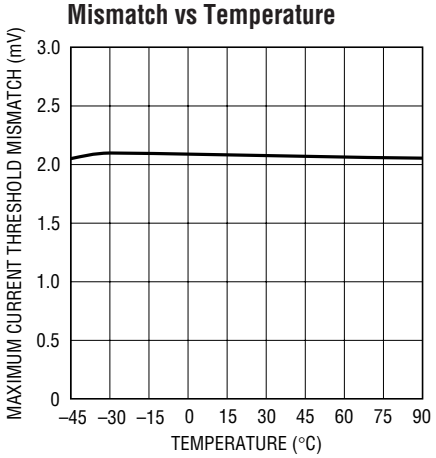
I_{SENSE} Pin Current vs V_{OUT}



3733 G18

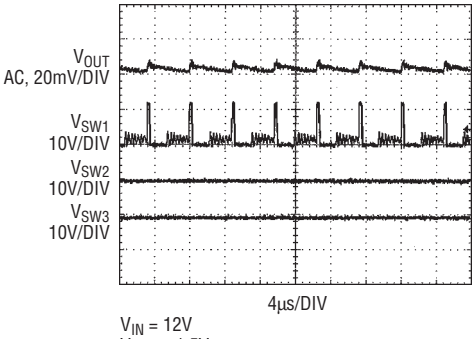
TYPICAL PERFORMANCE CHARACTERISTICS

Maximum Current Threshold Mismatch vs Temperature



3733 G19

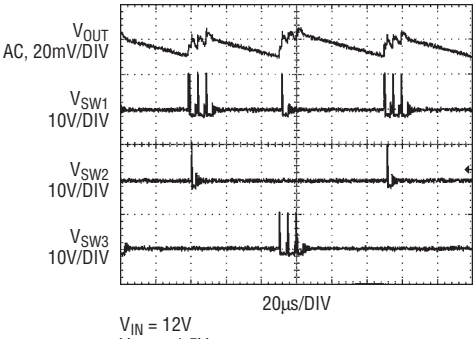
Shed Mode at 1Amp, Light Load Current



V_{IN} = 12V
V_{OUT} = 1.5V
V_{FCB} = V_{CC}
FREQUENCY = 210kHz

3733 G20

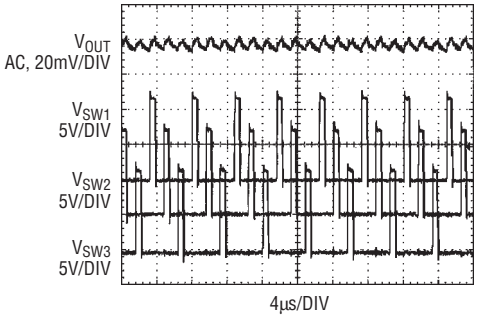
Burst Mode at 1Amp, Light Load Current



V_{IN} = 12V
V_{OUT} = 1.5V
V_{FCB} = OPEN
FREQUENCY = 210kHz

3733 G21

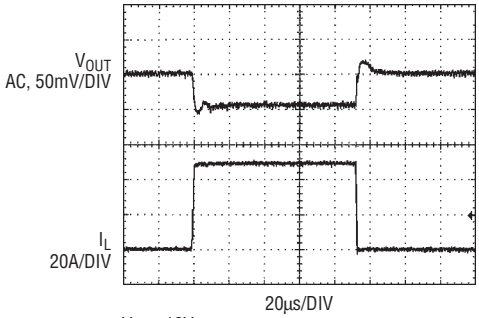
Continuous Mode at 1Amp, Light Load Current



V_{IN} = 12V
V_{OUT} = 1.5V
V_{FCB} = 0V
FREQUENCY = 210kHz

3733 G22

Transient Load Current Response: 0Amp to 50Amp



V_{IN} = 12V
V_{OUT} = 1.5V
V_{FCB} = 0V
FREQUENCY = 210kHz

3733 G23

PIN FUNCTIONS (G36/QFN)

VID0 to VID4 (Pins 36, 1, 18, 19, 20/Pins 35, 36, 16, 17, 18): Output Voltage Programming Input Pins. A 150k internal pull-up resistor is provided on each input pin. See Table 1 for details. Do not apply voltage to these pins prior to the application of voltage on the V_{CC} pin.

RUN (Pin 2/Pin 37): ON/OFF Control of the LTC3733.

PLLFLTR (Pin 3/Pin 1): The phase-locked loop's lowpass filter is tied to this pin. Alternatively, this pin can be driven with an AC or DC voltage source to vary the frequency of the internal oscillator. (Do not apply voltage to this pin prior to the application of voltage on the V_{CC} pin.)

FCB (Pin 4/Pin 2): Forced Continuous Control Input. The voltage applied to this pin sets the operating mode of the controller. The forced continuous current mode is active when the applied voltage is less than 0.6V. Burst Mode operation will be active when the pin is allowed to float and a stage shedding mode will be active if the pin is tied to the V_{CC} pin. (Do not apply voltage to this pin prior to the application of voltage on the V_{CC} pin.)

IN^+, IN^- (Pins 5, 6/Pins 3, 4): Inputs to a precision, unity-gain differential amplifier with internal precision resistors. This provides true remote sensing of both the positive and negative load terminals for precise output voltage control.

DIFFOUT (Pin 7/Pin 5): Output of the Remote Output Voltage Sensing Differential Amplifier.

EAIN (Pin 8/Pin 6): This is the input to the error amplifier which compares the VID divided, feedback voltage to the internal 0.6V reference voltage.

SGND (Pin 9/Pin 7, 39): Signal Ground. This pin must be routed separately under the IC to the PGND pin and then to the main ground plane. The exposed pad (QFN) must be soldered to the PCB for optimal thermal performance.

$SENSE1^+$, $SENSE2^+$, $SENSE3^+$, $SENSE1^-$, $SENSE2^-$, $SENSE3^-$ (Pins 10 to 15/Pins 8 to 13): The Inputs to Each Differential Current Comparator. The I_{TH} pin voltage and built-in offsets between $SENSE^-$ and $SENSE^+$ pins, in conjunction with R_{SENSE}, set the current trip threshold level.

SS (Pin 16/Pin 14): Combination of Soft-Start and Short-Circuit Detection Timer. A capacitor to ground at this pin sets the ramp time to full current output as well as the time delay prior to an output voltage short-circuit shutdown. A minimum value of 0.01µF is recommended on this pin.

I_{TH} (Pin 17/Pin 15): Error Amplifier Output and Switching Regulator Compensation Point. All three current comparator's thresholds increase with this control voltage.

PGND (Pin 26/Pin 24): Driver Power Ground. This pin connects to the sources of the bottom N-channel external MOSFETs and the (–) terminals of C_{IN}.

BG1 to BG3 (Pins 27, 25, 24/Pins 25, 23, 22): High Current Gate Drives for Bottom N-Channel MOSFETs. Voltage swing at these pins is from ground to V_{CC}.

DRV_{CC} (NA/Pin 26): High Power Supply to Drive the External MOSFET Gates in QFN Package. This pin needs to be closely decoupled to the IC's PGND pin.

V_{CC} (Pin 28/Pin 27): Main Supply Pin. This pin supplies the controller circuit power. In the G36 package, it is also the high power supply to drive the external MOSFET gates and this pin needs to be closely decoupled to the IC's PGND pin.

SW1 to SW3 (Pins 32, 29, 23/Pins 31, 28, 21): Switch Node Connections to Inductors. Voltage swing at these pins is from a Schottky diode (external) voltage drop below ground to V_{IN} (where V_{IN} is the external MOSFET supply rail).

PIN FUNCTIONS (G36/QFN)

TG1 to TG3 (Pins 33, 30, 22/Pins 32, 29, 20): High Current Gate Drives for Top N-channel MOSFETs. These are the outputs of floating drivers with a voltage swing equal to the boost voltage source superimposed on the switch node voltage SW.

BOOST1 to BOOST3 (Pins 34, 31, 21/Pins 33, 30, 19): Positive Supply Pins to the Topside Floating Drivers. Bootstrapped capacitors, charged with external Schottky diodes and a boost voltage source, are connected between the BOOST and SW pins. Voltage swing at the BOOST pins is from boost source voltage (typically V_{CC}) to this boost source voltage + V_{IN} (where V_{IN} is the external MOSFET supply rail).

PGOOD (Pin 35/Pin 34): This open-drain output is pulled low when the output voltage is outside the PGOOD tolerance window. PGOOD is blanked during VID transitions for approximately 120μs.

PLLIN (NA/Pin 38): Synchronization Input to Phase Detector. This pin is internally terminated to SGND with 50kΩ. The phase-locked loop will force the rising top gate signal of controller 1 to be synchronized with the rising edge of the PLLIN signal. This pin is not available in the G36 package.

Exposed Pad (NA/Pin 39): Signal Ground. Must be soldered to PCB.

FUNCTIONAL DIAGRAM

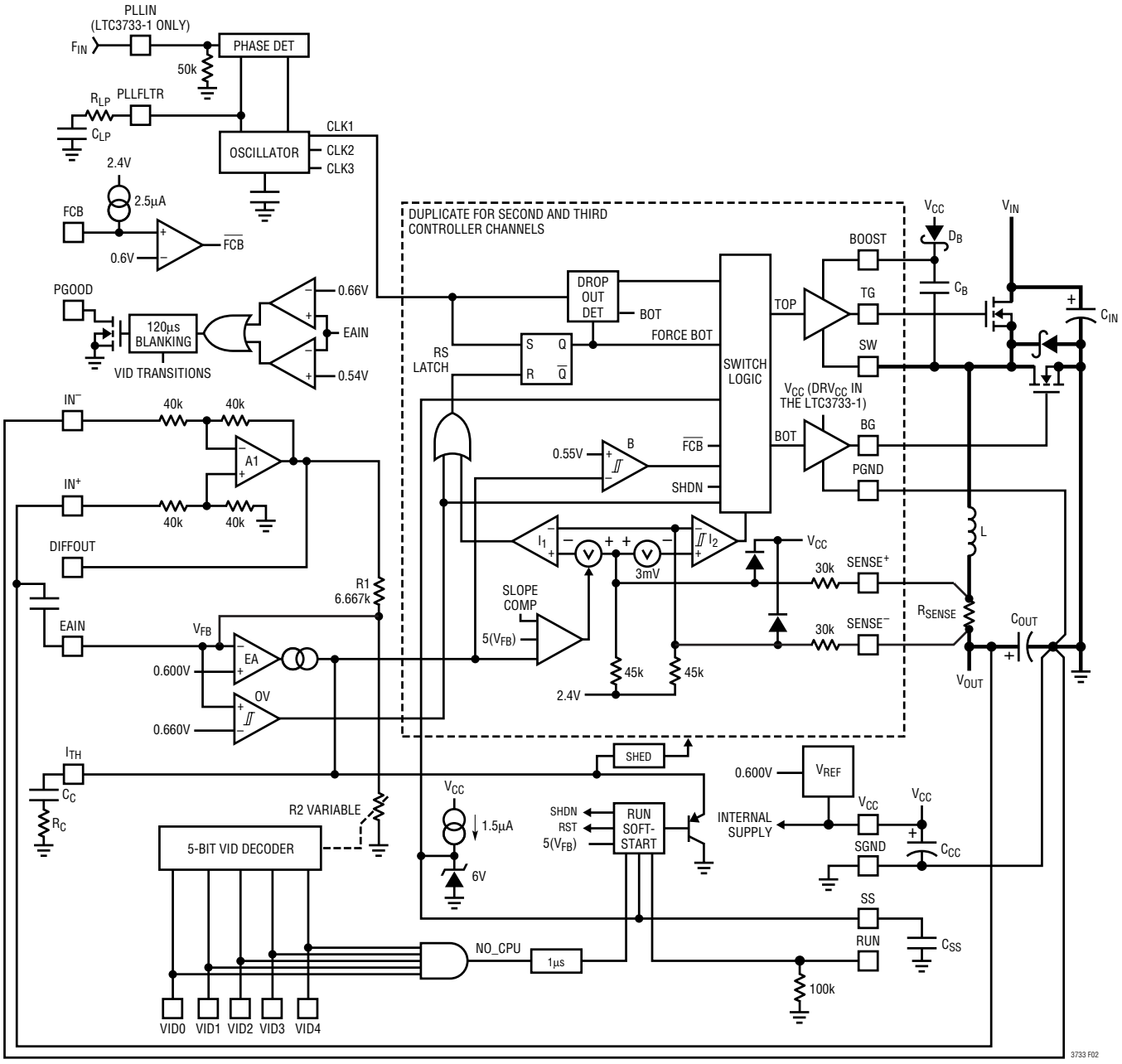


Figure 2

OPERATION (Refer to Functional Diagram)

Main Control Loop

The IC uses a constant frequency, current mode step-down architecture. During normal operation, each top MOSFET is turned on each cycle when the oscillator sets the RS latch, and turned off when the main current comparator, I_1, resets each RS latch. The peak inductor current at which I_1 resets the RS latch is controlled by the voltage on the I_{TH} pin, which is the output of the error amplifier EA. The EAIN pin receives a portion of the voltage feedback signal via the DIFFOUT pin through the internal VID DAC and is compared to the internal reference voltage. When the load current increases, it causes a slight decrease in the EAIN pin voltage relative to the 0.6V reference, which in turn causes the I_{TH} voltage to increase until each inductor's average current matches one third of the new load current (assuming all three current sensing resistors are equal). In Burst Mode operation and stage shedding mode, after each top MOSFET has turned off, the bottom MOSFET is turned on until either the inductor current starts to reverse, as indicated by current comparator I_2, or the beginning of the next cycle.

The top MOSFET drivers are biased from floating bootstrap capacitor C_B, which is normally recharged during each off cycle through an external Schottky diode. When V_{IN} decreases to a voltage close to V_{OUT}, however, the loop may enter dropout and attempt to turn on the top MOSFET continuously. The dropout detector counts the number of oscillator cycles that the bottom MOSFET remains off and periodically forces a brief on period to allow C_B to recharge.

The main control loop is shut down by pulling the RUN pin low. Releasing RUN allows an internal 1.5µA current source to charge soft-start capacitor C_{SS} at the SS pin. The internal I_{TH} voltage is then clamped to the SS voltage when C_{SS} is slowly charged up. This "soft-start" clamping prevents abrupt current from being drawn from the input power source. When the RUN pin is low, all functions are kept in a controlled state.

Low Current Operation

The FCB pin is a multifunction pin: 1) an analog comparator input to provide regulation for a secondary winding by forcing temporary forced PWM operation and 2) a logic input to select between three modes of operation.

When the FCB pin voltage is below 0.6V, the controller performs as a continuous, PWM current mode synchronous switching regulator. The top and bottom MOSFETs are alternately turned on to maintain the output voltage independent of direction of inductor current. When the FCB pin is below V_{CC} – 1V but greater than 0.6V, the controller performs as a Burst Mode switching regulator. Burst Mode operation sets a minimum output current level before turning off the top switch and turns off the synchronous MOSFET(s) when the inductor current goes negative. This combination of requirements will, at low current, force the I_{TH} pin below a voltage threshold that will temporarily shut off both output MOSFETs until the output voltage drops slightly. There is a burst comparator having 60mV of hysteresis tied to the I_{TH} pin. This hysteresis results in output signals to the MOSFETs that turn them on for several cycles, followed by a variable "sleep" interval depending upon the load current. The resultant output voltage ripple is held to a very small value by having the hysteretic comparator after the error amplifier gain block.

When the FCB pin is tied to the V_{CC} pin, Burst Mode operation is disabled and the forced minimum inductor current requirement is removed. This provides constant frequency, discontinuous current operation over the widest possible output current range. At approximately 10% of maximum designed load current, the second and third output stages are shut off and the first controller alone is active in discontinuous current mode. This "stage shedding" optimizes efficiency by eliminating the gate charging losses and switching losses of the other two output stages. Additional cycles will be skipped when the output load current drops below 1% of maximum designed load current in order to maintain the output voltage. This constant frequency operation is not as efficient as Burst Mode operation at very light loads, but does provide lower noise, constant frequency operating mode down to very light load conditions.

Tying the FCB pin to ground will force continuous current operation. This is the least efficient operating mode, but may be desirable in certain applications. The output can

OPERATION (Refer to Functional Diagram)

source or sink current in this mode. When forcing continuous operation and sinking current, this current will be forced back into the main power supply, potentially boosting the input supply to dangerous voltage levels—BEWARE!

Frequency Synchronization or Setup

The phase-locked loop allows the internal oscillator to be synchronized to an external source using the PLLIN pin. The output of the phase detector at the PLLFLTR pin is also the DC frequency control input of the oscillator which operates over a 210kHz to 530kHz range corresponding to a voltage input from 0V to 2.4V. When locked, the PLL aligns the turn on of the top MOSFET to the rising edge of the synchronizing signal. When no frequency information is supplied to the PLLIN pin, PLLFLTR goes low, forcing the oscillator to minimum frequency. A DC source can be applied to the PLLFLTR pin to externally set the desired operating frequency.

In the G36 package, the PLLIN pin is not brought out and the PLLFLTR pin is for frequency setup only.

Differential Amplifier

This amplifier provides true differential output voltage sensing. Sensing both V_{OUT}^+ and V_{OUT}^- benefits regulation in high current applications and/or applications having electrical interconnection losses. This sensing also isolates the physical power ground from the physical signal ground preventing the possibility of troublesome "ground loops" on the PC layout and prevents voltage errors caused by board-to-board interconnects, particularly helpful in VRM designs.

Power Good

The PGOOD pin is connected to the drain of an internal MOSFET. The MOSFET is turned on once the output voltage has been away from its nominal value by greater than 10%. The PGOOD signal is blanked for approximately 120μs during VID transitions. If a new VID transition occurs before the previous blanking time expires, the timer is reset.

Short-Circuit Detection

The SS capacitor is used initially to limit the inrush current from the input power source. Once the controllers have been given time, as determined by the capacitor on the SS pin, to charge up the output capacitors and provide full load current, the SS capacitor is then used as a short-circuit timeout circuit. If the output voltage falls to less than 70% of its nominal output voltage, the SS capacitor begins discharging, assuming that the output is in a severe overcurrent and/or short-circuit condition. If the condition lasts for a long enough period, as determined by the size of the SS capacitor, the controller will be shut down until the RUN pin voltage is recycled. This built-in latchoff can be overridden by providing >5μA at a compliance of 4V to the SS pin. This current shortens the soft-start period but prevents net discharge of the SS capacitor during a severe overcurrent and/or short-circuit condition. Foldback current limiting is activated when the output voltage falls below 70% of its nominal level whether or not the short-circuit latchoff circuit is enabled. Foldback current limit can be overridden by clamping the EAIN pin such that the voltage is held above the (70%)(0.6V) or 0.42V level even when the actual output voltage is low.

The SS capacitor will be reset if the input voltage, (V_{CC}) is allowed to fall below approximately 4V. The capacitor on the pin will be discharged until the short-circuit arming latch is disarmed. The SS capacitor will attempt to cycle through a normal soft-start ramp up after the V_{CC} supply rises above 4V. This circuit prevents power supply latchoff in the event of input power switching break-before-make situations.

No_CPU Detection

The LTC3733 detects the presense of CPU by monitoring all VID bits. If an all-"1" condition is detected, the controller acknowledges a No_CPU fault. If this fault condition persists for more than 1μs, the SS pin is pulled low and the controller is shut down.

APPLICATIONS INFORMATION

The basic application circuit is shown in Figure 1 on the first page of this data sheet. External component selection is driven by the load requirement, and normally begins with the selection of an inductance value based upon the desired operating frequency, inductor current and output voltage ripple requirements. Once the inductors and operating frequency have been chosen, the current sensing resistors can be calculated. Next, the power MOSFETs and Schottky diodes are selected. Finally, C_{IN} and C_{OUT} are selected according to the required voltage ripple requirements. The circuit shown in Figure 1 can be configured for operation up to a MOSFET supply voltage of 28V (limited by the external MOSFETs).

Operating Frequency

The IC uses a constant frequency architecture with the frequency determined by an internal capacitor. This capacitor is charged by a fixed current plus an additional current which is proportional to the voltage applied to the PLLFLTR pin. Refer to the Phase-Locked Loop and Frequency Synchronization and Setup sections for additional information.

A graph for the voltage applied to the PLLFLTR pin versus frequency is given in Figure 3. As the operating frequency is increased the gate charge losses will be higher, reducing efficiency (see Efficiency Considerations). The maximum switching frequency is approximately 530kHz.

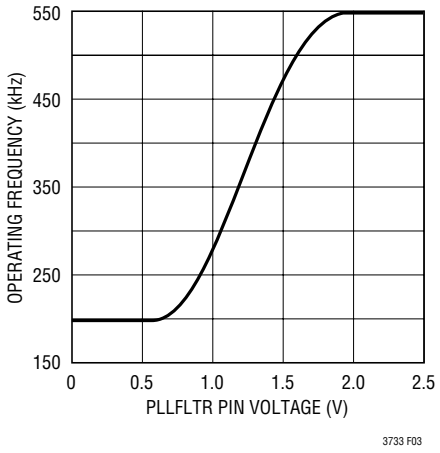


Figure 3. Operating Frequency vs $V_{PLLFLTR}$

Inductor Value Calculation and Output Ripple Current

The operating frequency and inductor selection are interrelated in that higher operating frequencies allow the use of smaller inductor and capacitor values. So why would anyone ever choose to operate at lower frequencies with larger components? The answer is efficiency. A higher frequency generally results in lower efficiency because of MOSFET gate charge and transition losses. In addition to this basic tradeoff, the effect of inductor value on ripple current and low current operation must also be considered. The PolyPhase approach reduces both input and output ripple currents while optimizing individual output stages to run at a lower fundamental frequency, enhancing efficiency.

The inductor value has a direct effect on ripple current. The inductor ripple current ΔI_L per individual section, N, decreases with higher inductance or frequency and increases with higher V_{IN} or V_{OUT}:

$$\Delta I_L = \frac{V_{OUT}}{fL}\left(1-\frac{V_{OUT}}{V_{IN}}\right)$$

where f is the individual output stage operating frequency.

In a PolyPhase converter, the net ripple current seen by the output capacitor is much smaller than the individual inductor ripple currents due to the ripple cancellation. The details on how to calculate the net output ripple current can be found in Application Note 77.

Figure 4 shows the net ripple current seen by the output capacitors for the different phase configurations. The output ripple current is plotted for a fixed output voltage as the duty factor is varied between 10% and 90% on the x-axis. The output ripple current is normalized against the inductor ripple current at zero duty factor. The graph can be used in place of tedious calculations. As shown in Figure 4, the zero output ripple current is obtained when:

$$\frac{V_{OUT}}{V_{IN}} = \frac{k}{N} \quad \text{where } k = 1, 2, ..., N-1$$

APPLICATIONS INFORMATION

So the number of phases used can be selected to minimize the output ripple current and therefore the output ripple voltage at the given input and output voltages. In applications having a highly varying input voltage, additional phases will produce the best results.

Accepting larger values of ΔI_L allows the use of low inductances but can result in higher output voltage ripple. A reasonable starting point for setting ripple current is $\Delta I_L = 0.4(I_{OUT})/N$, where N is the number of channels and I_{OUT} is the total load current. Remember, the maximum ΔI_L occurs at the maximum input voltage. The individual inductor ripple currents are constant determined by the inductor, input and output voltages.

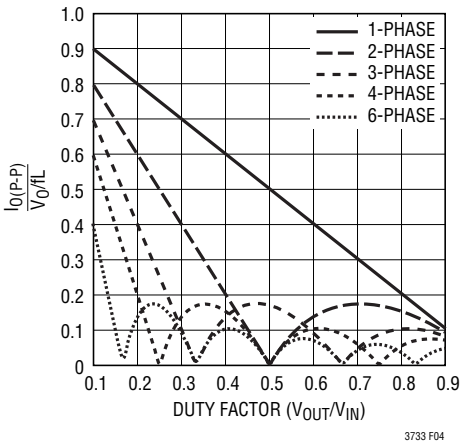


Figure 4. Normalized Peak Output Current vs Duty Factor [$I_{RMS} = 0.3(I_{O(P-P)}$]

Inductor Core Selection

Once the value for L1 to L3 is known, the type of inductor must be selected. High efficiency converters generally cannot afford the core loss found in low cost powdered iron cores, forcing the use of ferrite, molypermalloy or Kool Mμ® cores. Actual core loss is independent of core size for a fixed inductor value, but it is very dependent on inductance selected. As inductance increases, core losses go down. Unfortunately, increased inductance requires more turns of wire and therefore copper losses will increase.

Ferrite designs have very low core loss and are preferred at high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates "hard," which means that inductance collapses abruptly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current and consequent output voltage ripple. Do not allow the core to saturate!

Power MOSFET and D1, D2, D3 Selection

At least two external power MOSFETs must be selected for each of the three output sections: One N-channel MOSFET for the top (main) switch and one or more N-channel MOSFET(s) for the bottom (synchronous) switch. The number, type and "on" resistance of all MOSFETs selected take into account the voltage step-down ratio as well as the actual position (main or synchronous) in which the MOSFET will be used. A much smaller and much lower input capacitance MOSFET should be used for the top MOSFET in applications that have an output voltage that is less than 1/3 of the input voltage. In applications where $V_{IN} >> V_{OUT}$, the top MOSFETs' "on" resistance is normally less important for overall efficiency than its input capacitance at operating frequencies above 300kHz. MOSFET manufacturers have designed special purpose devices that provide reasonably low "on" resistance with significantly reduced input capacitance for the main switch application in switching regulators.

The peak-to-peak MOSFET gate drive levels are set by the voltage, V_{CC}, requiring the use of logic-level threshold MOSFETs in most applications. Pay close attention to the BV_{DSS} specification for the MOSFETs as well; many of the logic-level MOSFETs are limited to 30V or less.

Selection criteria for the power MOSFETs include the "on" resistance $R_{SD(ON)}$, input capacitance, input voltage and maximum output current.

MOSFET input capacitance is a combination of several components but can be taken from the typical "gate charge" curve included on most data sheets (Figure 5). The curve is generated by forcing a constant input current

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APPLICATIONS INFORMATION

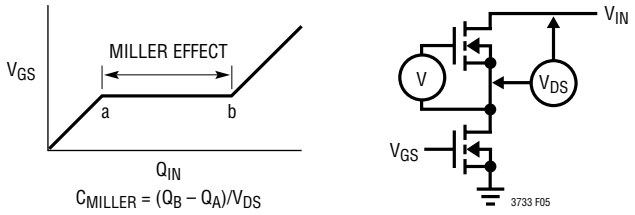


Figure 5. Gate Charge Characteristic

into the gate of a common source, current source loaded stage and then plotting the gate voltage versus time. The initial slope is the effect of the gate-to-source and the gate-to-drain capacitance. The flat portion of the curve is the result of the Miller capacitance effect of the drain-to-source capacitance as the drain drops the voltage across the current source load. The upper sloping line is due to the drain-to-gate accumulation capacitance and the gate-to-source capacitance. The Miller charge (the increase in coulombs on the horizontal axis from a to b while the curve is flat) is specified for a given V_{DS} drain voltage, but can be adjusted for different V_{DS} voltages by multiplying by the ratio of the application V_{DS} to the curve specified V_{DS} values. A way to estimate the C_{MILLER} term is to take the change in gate charge from points a and b on a manufacturers data sheet and divide by the stated V_{DS} voltage specified. C_{MILLER} is the most important selection criteria for determining the transition loss term in the top MOSFET but is not directly specified on MOSFET data sheets. C_{RSS} and C_{OS} are specified sometimes but definitions of these parameters are not included.

When the controller is operating in continuous mode the duty cycles for the top and bottom MOSFETs are given by:

$$\text{Main Switch Duty Cycle} = \frac{V_{OUT}}{V_{IN}}$$

$$\text{Synchronous Switch Duty Cycle} = \left(\frac{V_{IN} - V_{OUT}}{V_{IN}}\right)$$

The power dissipation for the main and synchronous MOSFETs at maximum output current are given by:

$$P_{MAIN} = \frac{V_{OUT}}{V_{IN}}\left(\frac{I_{MAX}}{N}\right)^2(1+\delta)R_{DS(ON)} + V_{IN}^2\frac{I_{MAX}}{2N}(R_{DR})(C_{MILLER})\bullet\left[\frac{1}{V_{CC} - V_{TH(MIN)}} + \frac{1}{V_{TH(MIN)}}\right](f)$$

$$P_{SYNC} = \frac{V_{IN} - V_{OUT}}{V_{IN}}\left(\frac{I_{MAX}}{N}\right)^2(1+\delta)R_{DS(ON)}$$

where N is the number of output stages, δ is the temperature dependency of $R_{DS(ON)}$, R_{DR} is the effective top driver resistance (approximately 2Ω at $V_{GS} = V_{MILLER}$), V_{IN} is the drain potential *and* the change in drain potential in the particular application. $V_{TH(MIN)}$ is the data sheet specified typical gate threshold voltage specified in the power MOSFET data sheet. C_{MILLER} is the calculated capacitance using the gate charge curve from the MOSFET data sheet and the technique described above.

Both MOSFETs have I^2R losses while the topside N-channel equation includes an additional term for transition losses, which peak at the highest input voltage. For $V_{IN} < 12V$, the high current efficiency generally improves with larger MOSFETs, while for $V_{IN} > 12V$, the transition losses rapidly increase to the point that the use of a higher $R_{DS(ON)}$ device with lower C_{RSS} actually provides higher efficiency. The synchronous MOSFET losses are greatest at high input voltage when the top switch duty factor is low or during a short circuit when the synchronous switch is on close to 100% of the period.

The term (1 + δ) is generally given for a MOSFET in the form of a normalized $R_{DS(ON)}$ vs temperature curve, but

APPLICATIONS INFORMATION

δ = 0.005/°C can be used as an approximation for low voltage MOSFETs.

The Schottky diodes, D1 to D3 shown in Figure 1 conduct during the dead time between the conduction of the two large power MOSFETs. This prevents the body diode of the bottom MOSFET from turning on, storing charge during the dead time and requiring a reverse recovery period which could cost as much as several percent in efficiency. A 2A to 8A Schottky is generally a good compromise for both regions of operation due to the relatively small average current. Larger diodes result in additional transition losses due to their larger junction capacitance.

C_{IN} and C_{OUT} Selection

Input capacitance ESR requirements and efficiency losses are reduced substantially in a multiphase architecture because the peak current drawn from the input capacitor is effectively divided by the number of phases used and power loss is proportional to the RMS current squared. A 3-stage, single output voltage implementation can reduce input path power loss by 90%.

In continuous mode, the source current of each top N-channel MOSFET is a square wave of duty cycle V_{OUT}/V_{IN}. A low ESR input capacitor sized for the maximum RMS current must be used. The details of a close form equation can be found in Application Note 77. Figure 6 shows the input capacitor ripple current for different phase configurations with the output voltage fixed and input voltage varied. The input ripple current is normalized against the DC output current. The graph can be used in place of tedious calculations. The minimum input ripple current can be achieved when the product of phase number and output voltage, $N(V_{OUT})$, is approximately equal to the input voltage V_{IN} or:

$$\frac{V_{OUT}}{V_{IN}} = \frac{k}{N} \text{ where } k = 1, 2, ..., N-1$$

So the phase number can be chosen to minimize the input capacitor size for the given input and output voltages.

In the graph of Figure 6, the local maximum input RMS capacitor currents are reached when:

$$\frac{V_{OUT}}{V_{IN}} = \frac{2k-1}{N} \text{ where } k = 1, 2, ..., N$$

These worst-case conditions are commonly used for design because even significant deviations do not offer much relief. Note that capacitor manufacturer's ripple current ratings are often based on only 2000 hours of life. This makes it advisable to further derate the capacitor or to choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design. Always consult the capacitor manufacturer if there is any question.

The Figure 6 graph shows that the peak RMS input current is reduced linearly, inversely proportional to the number N of stages used. It is important to note that the efficiency loss is proportional to the input RMS current squared and therefore a 3-stage implementation results in 90% less power loss when compared to a single phase design. Battery/input protection fuse resistance (if used), PC

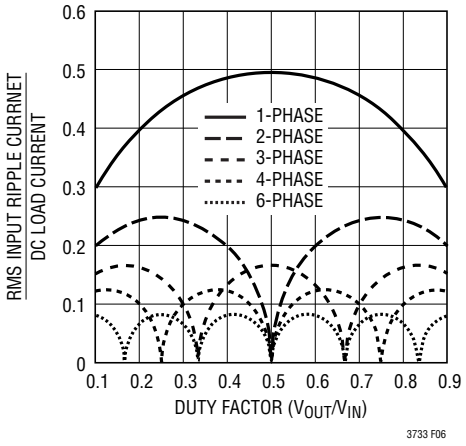


Figure 6. Normalized Input RMS Ripple Current vs Duty Factor for One to Six Output Stages

APPLICATIONS INFORMATION

board trace and connector resistance losses are also reduced by the reduction of the input ripple current in a PolyPhase system. The required amount of input capacitance is further reduced by the factor, N, due to the effective increase in the frequency of the current pulses.

Ceramic capacitors are becoming very popular for small designs but several cautions should be observed. "X7R", "X5R" and "Y5V" are examples of a few of the ceramic materials used as the dielectric layer, and these different dielectrics have very different effect on the capacitance value due to the voltage and temperature conditions applied. Physically, if the capacitance value changes due to applied voltage change, there is a concommitant piezo effect which results in radiating sound! A load that draws varying current at an audible rate may cause an attendant varying input voltage on a ceramic capacitor, resulting in an audible signal. A secondary issue relates to the energy flowing back into a ceramic capacitor whose capacitance value is being reduced by the increasing charge. The voltage can increase at a considerably higher rate than the constant current being supplied because the capacitance value is decreasing as the voltage is increasing! Ceramic capacitors, when properly selected and used however, can provide the lowest overall loss due to their extremely low ESR.

The selection of C_{OUT} is driven by the required effective series resistance (ESR). Typically once the ESR requirement is satisfied the capacitance is adequate for filtering. The steady-state output ripple (ΔV_{OUT}) is determined by:

$$\Delta V_{OUT} \approx \Delta I_{RIPPLE}\left(ESR + \frac{1}{8NfC_{OUT}}\right)$$

where f = operating frequency of each stage, N is the number of output stages, C_{OUT} = output capacitance and ΔI_L = ripple current in each inductor. The output ripple is highest at maximum input voltage since ΔI_L increases with input voltage. The output ripple will be less than 50mV at max V_{IN} with $\Delta I_L = 0.4I_{OUT(MAX)}$ assuming:

C_{OUT} required ESR < N • R_{SENSE}

and

$C_{OUT} > 1/(8Nf)(R_{SENSE})$

The emergence of very low ESR capacitors in small, surface mount packages makes very small physical implementations possible. The ability to externally compensate the switching regulator loop using the I_{TH} pin allows a much wider selection of output capacitor types. The impedance characteristics of each capacitor type is significantly different than an ideal capacitor and therefore requires accurate modeling or bench evaluation during design.

Manufacturers such as Nichicon, United Chemicon and Sanyo should be considered for high performance through-hole capacitors. The OS-CON semiconductor dielectric capacitor available from Sanyo and the Panasonic SP surface mount types have a good (ESR)(size) product. Once the ESR requirement for C_{OUT} has been met, the RMS current rating generally far exceeds the $I_{RIPPLE(P-P)}$ requirement. Ceramic capacitors from AVX, Taiyo Yuden, Murata and Tokin offer high capacitance value and very low ESR, especially applicable for low output voltage applications.

In surface mount applications, multiple capacitors may have to be paralleled to meet the ESR or RMS current handling requirements of the application. Aluminum electrolytic and dry tantalum capacitors are both available in surface mount configurations. New special polymer surface mount capacitors offer very low ESR also but have much lower capacitive density per unit volume. In the case of tantalum, it is critical that the capacitors are surge tested for use in switching power supplies. Several excellent choices are the AVX TPS, AVX TPSV, the KEMET T510

APPLICATIONS INFORMATION

series of surface-mount tantalums or the Panasonic SP series of surface mount special polymer capacitors available in case heights ranging from 2mm to 4mm. Other capacitor types include Sanyo POS-CAP, Sanyo OS-CON, Nichicon PL series and Sprague 595D series. Consult the manufacturer for other specific recommendations.

R_{SENSE} Selection for Output Current

Once the frequency and inductor have been chosen, R_{SENSE1}, R_{SENSE2}, R_{SENSE3} are determined based on the required peak inductor current. The current comparator has a maximum threshold of 75mV/R_{SENSE} and an input common mode range of SGND to (1.1) • V_{CC}. The current comparator threshold sets the peak inductor current, yielding a maximum average output current I_{MAX} equal to the peak value less half the peak-to-peak ripple current, ΔI_L.

Allowing a margin for variations in the IC and external component values yields:

$$R_{SENSE} = N\frac{50mV}{I_{MAX}}$$

The IC works well with values of R_{SENSE} from 0.001Ω to 0.02Ω.

V_{CC} Decoupling

The V_{CC} pin supples power not only the internal circuits of the controller but also the top and bottom gate drivers and therefore must be bypassed very carefully to ground with a ceramic capacitor, type X7R or X5R (depending upon the operating temperature environment) of *at least 1µF immediately next to the IC* and preferably an additional 10µF placed very close to the IC due to the extremely high instantaneous currents involved. The total capacitance, taking into account the voltage coefficient of ceramic capacitors, should be 100 times as large as the total combined gate charge capacitance of ALL of the MOSFETs being driven. Good bypassing close to the IC is necessary to supply the high transient currents required by the MOSFET gate drivers while keeping the 5V supply quiet enough so as not to disturb the very small-signal high bandwidth of the current comparators.

Topside MOSFET Driver Supply (C_B, D_B)

External bootstrap capacitors, C_B, connected to the BOOST pins, supply the gate drive voltages for the topside MOSFETs. Capacitor C_B in the Functional Diagram is charged though diode D_B from V_{CC} when the SW pin is low. When one of the topside MOSFETs turns on, the driver places the C_B voltage across the gate-source of the desired MOSFET. This enhances the MOSFET and turns on the topside switch. The switch node voltage, SW, rises to V_{IN} and the BOOST pin follows. With the topside MOSFET on, the boost voltage is above the input supply (V_{BOOST} = V_{CC} + V_{IN}). The value of the boost capacitor C_B needs to be 30 to 100 times that of the total input capacitance of the topside MOSFET(s). The reverse breakdown of D_B must be greater than $V_{IN(MAX)}$.

Differential Amplifier

The IC has a true remote voltage sense capability. The sensing connections should be returned from the load, back to the differential amplifier's inputs through a common, tightly coupled pair of PC traces. The differential amplifier rejects common mode signals capacitively or inductively radiated into the feedback PC traces as well as ground loop disturbances. The differential amplifier output signal is divided down through the VID DAC and is compared with the internal, precision 0.6V voltage reference by the error amplifier.

The amplifier has a 0 to V_{CC} common mode input range and an output swing range of 0 to V_{CC} – 1.2V. The output uses an NPN emitter follower with 80kΩ feedback resistance. A DC resistive load to ground is required in order to sink more current.

APPLICATIONS INFORMATION

Output Voltage

The IC includes a digitally controlled 5-bit attenuator producing output voltages as defined in Table 1. Output voltages with 25mV increments are produced from 0.8V to 1.55V.

Each VID digital input is pulled up to a logical high with an internal 150k resistor. The input logic threshold is approximately 1.2V but the input circuit can withstand an input voltage of up to 7V.

ON/OFF Control

The RUN pin provides simple ON/OFF control for the LTC3733. Driving the RUN pin above 1.5V permits the controller to start operating. Pulling RUN below 0.8V puts the LTC3733 into low current shutdown ($I_Q \approx 20\mu A$).

Soft-Start Function

The SS pin provides two functions: 1) soft-start and 2) a defeatable short-circuit latch off timer. Soft-start reduces the input power sources' surge currents by gradually increasing the controller's current limit (proportional to an internal buffered and clamped V_{ITH}). The latchoff timer prevents very short, extreme load transients from tripping the overcurrent latch. A small pull-up current (>5µA) supplied to the SS pin will prevent the overcurrent latch from operating. The following explanation describes how this function operates.

An internal 1.5µA current source charges up the C_{SS} capacitor. As the voltage on SS increases from 0V to 2.4V, the internal current limit is increased from 0V/R_{SENSE} to 75mV/R_{SENSE}. The output current limit ramps up slowly, taking 1.6s/µF to reach full current. The output current thus ramps up slowly, eliminating the starting surge current required from the input power supply.

$$t_{IRAMP} = \frac{2.4V - 0V}{1.5\mu A} C_{SS} = (1.6s/\mu F) C_{SS}$$

The SS pin has an internal 6V zener clamp (see the Functional Diagram).

Table 1. VID Output Voltage Programming

VID4	VID3	VID2	VID1	VID0	V_{OUT}
0	0	0	0	0	1.550
0	0	0	0	1	1.525
0	0	0	1	0	1.500
0	0	0	1	1	1.475
0	0	1	0	0	1.450
0	0	1	0	1	1.425
0	0	1	1	0	1.400
0	0	1	1	1	1.375
0	1	0	0	0	1.350
0	1	0	0	1	1.325
0	1	0	1	0	1.300
0	1	0	1	1	1.275
0	1	1	0	0	1.250
0	1	1	0	1	1.225
0	1	1	1	0	1.200
0	1	1	1	1	1.175
1	0	0	0	0	1.150
1	0	0	0	1	1.125
1	0	0	1	0	1.100
1	0	0	1	1	1.075
1	0	1	0	0	1.050
1	0	1	0	1	1.025
1	0	1	1	0	1.000
1	0	1	1	1	0.975
1	1	0	0	0	0.950
1	1	0	0	1	0.925
1	1	0	1	0	0.900
1	1	0	1	1	0.875
1	1	1	0	0	0.850
1	1	1	0	1	0.825
1	1	1	1	0	0.800
1	1	1	1	1	Shutdown

APPLICATIONS INFORMATION

Fault Conditions: Overcurrent Latchoff

The SS pin also provides the ability to latch off the controllers when an overcurrent condition is detected. The SS capacitor is used initially to limit the inrush current of all three output stages. After the controllers have been given adequate time to charge up the output capacitor and provide full load current, the SS capacitor is used for a short-circuit timer. If the output voltage falls to less than 70% of its nominal value, the SS capacitor begins discharging on the assumption that the output is in an overcurrent condition. If the condition lasts for a long enough period, as determined by the size of the SS capacitor, the controller will be shut down until the RUN pin voltage is recycled. If the overload occurs during start-up, the time can be approximated by:

$$t_{LO1} >> (C_{SS} \bullet 0.6V)/(1.5\mu A) = 4 \bullet 10^5 (C_{SS})$$

If the overload occurs after start-up, the voltage on the SS capacitor will continue charging and will provide additional time before latching off:

$$t_{LO2} >> (C_{SS} \bullet 3V)/(1.5\mu A) = 2 \bullet 10^6 (C_{SS})$$

This built-in overcurrent latchoff can be overridden by providing a pull-up resistor to the SS pin from V_{CC} as shown in Figure 7. When V_{CC} is 5V, a 200k resistance will prevent the discharge of the SS capacitor during an overcurrent condition but also shortens the soft-start period, so a larger SS capacitor value will be required.

Why should you defeat overcurrent latchoff? During the prototyping stage of a design, there may be a problem with noise pick-up or poor layout causing the protection circuit to latch off the controller. Defeating this feature allows troubleshooting of the circuit and PC layout. The internal foldback current limiting still remains active, thereby protecting the power supply system from failure. A decision can be made after the design is complete whether to rely solely on foldback current limiting or to enable the latchoff feature by removing the pull-up resistor.

The value of the soft-start capacitor C_{SS} may need to be scaled with output current, output capacitance and load current characteristics. The minimum soft-start capacitance is given by:

$$C_{SS} > (C_{OUT})(V_{OUT})(10^{-4})(R_{SENSE})$$

The minimum recommended soft-start capacitor of C_{SS} = 0.1µF will be sufficient for most applications.

Current Foldback

In certain applications, it may be desirable to defeat the internal current foldback function. A negative impedance is experienced when powering a switching regulator. That is, the input current is higher at a lower V_{IN} and decreases as V_{IN} is increased. Current foldback is designed to accommodate a normal, resistive load having increasing current draw with increasing voltage. The EAIN pin should be artificially held 70% above its nominal operating level of 0.6V, or 0.42V in order to prevent the IC from "folding back" the peak current level. A suggested circuit is shown in Figure 8.

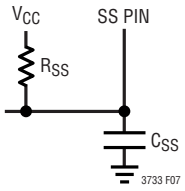


Figure 7. Defeating Overcurrent Latchoff

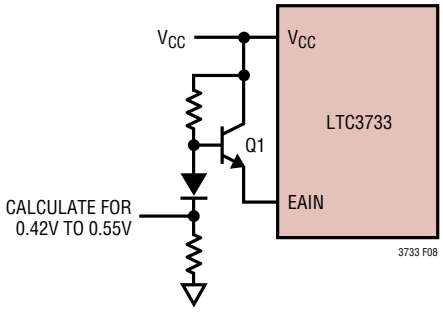


Figure 8. Foldback Current Elimination

APPLICATIONS INFORMATION

The emitter of Q1 will hold up the EAIN pin to a voltage in the absence of V_{OUT} that will prevent the internal sensing circuitry from reducing the peak output current. Removing the function in this manner eliminates the external MOSFET's protective feature under short-circuit conditions. This technique will also prevent the short-circuit latchoff function from turning off the part during a short-circuit event and the output current will only be limited to $N \bullet 75mV/R_{SENSE}$.

Undervoltage Reset

In the event that the input power source to the IC (V_{CC}) drops below 4V, the SS capacitor will be discharged to ground and the controller will be shut down. When V_{CC} rises above 4V, the SS capacitor will be allowed to recharge and initiate another soft-start turn-on attempt. This may be useful in applications that switch between two supplies that are not diode connected, but note that this cannot make up for the resultant interruption of the regulated output.

Phase-Locked Loop and Frequency Synchronization (LTC3733-1)

The IC has a phase-locked loop comprised of an internal voltage controlled oscillator and phase detector. This allows the top MOSFET of output stage 1's turn-on to be locked to the rising edge of an external source. The frequency range of the voltage controlled oscillator is ±50% around the center frequency f_O. A voltage applied to the PLLFLTR pin of 1.2V corresponds to a frequency of approximately 350kHz. The nominal operating frequency range of the IC is 210kHz to 530kHz.

The phase detector used is an edge sensitive digital type that provides zero degrees phase shift between the external and internal oscillators. This type of phase detector will not lock the internal oscillator to harmonics of the input frequency. The PLL hold-in range, Δf_H, is equal to the capture range, Δf_C:

$$\Delta f_H = \Delta f_C = \pm 0.5\ f_O$$

The output of the phase detector is a complementary pair of current sources charging or discharging the external filter components on the PLLFLTR pin. A simplified block diagram is shown in Figure 9.

If the external frequency (f_{PLLIN}) is greater than the oscillator frequency, f_{OSC}, current is sourced continuously, pulling up the PLLFLTR pin. When the external frequency is less than f_{OSC}, current is sunk continuously, pulling down the PLLFLTR pin. If the external and internal frequencies are the same, but exhibit a phase difference, the current sources turn on for an amount of time corresponding to the phase difference. Thus, the voltage on the PLLFLTR pin is adjusted until the phase and frequency of the external and internal oscillators are identical. At this stable operating point, the phase comparator output is open and the filter capacitor C_{LP} holds the voltage. The IC PLLIN pin must be driven from a low impedance source such as a logic gate located close to the pin. When using multiple ICs for a phase-locked system, the PLLFLTR pin of the master oscillator should be biased at a voltage that will guarantee the slave oscillator(s) ability to lock onto the master's frequency. A voltage of 1.7V or below applied to the master oscillator's PLLFLTR pin is recommended in order to meet this requirement. The resultant operating frequency will be approximately 500kHz for 1.7V.

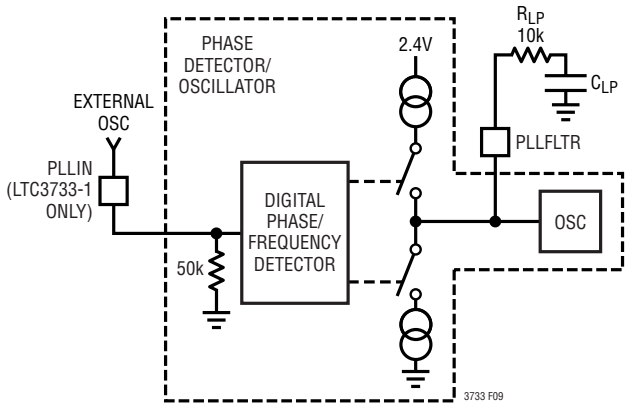


Figure 9. Phase-Locked Loop Block Diagram

APPLICATIONS INFORMATION

The loop filter components (C_{LP}, R_{LP}) smooth out the current pulses from the phase detector and provide a stable input to the voltage controlled oscillator. The filter components C_{LP} and R_{LP} determine how fast the loop acquires lock. Typically R_{LP} =10k and C_{LP} ranges from 0.01µF to 0.1µF.

Minimum On-Time Considerations

Minimum on-time, $t_{ON(MIN)}$, is the smallest time duration that the IC is capable of turning on the top MOSFET. It is determined by internal timing delays and the gate charge of the top MOSFET. Low duty cycle applications may approach this minimum on-time limit and care should be taken to ensure that:

$$t_{ON(MIN)} < \frac{V_{OUT}}{V_{IN}(f)}$$

If the duty cycle falls below what can be accommodated by the minimum on-time, the IC will begin to skip every other cycle, resulting in half-frequency operation. The output voltage will continue to be regulated, but the ripple current and ripple voltage will increase.

The minimum on-time for the IC is generally about 120ns. However, as the peak sense voltage decreases the minimum on-time gradually increases. This is of particular concern in forced continuous applications with low ripple current at light loads. If the duty cycle drops below the minimum on-time limit in this situation, a significant amount of cycle skipping can occur with correspondingly larger current and voltage ripple.

If an application can operate close to the minimum on-time limit, an inductor must be chosen that is low enough in value to provide sufficient ripple amplitude to meet the minimum on-time requirement. *As a general rule, keep the inductor ripple current equal to or greater than 30% of $I_{OUT(MAX)}$ at $V_{IN(MAX)}$.*

Efficiency Considerations

The percent efficiency of a switching regulator is equal to the output power divided by the input power times 100%.

It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Percent efficiency can be expressed as:

%Efficiency = 100% – (L1 + L2 + L3 + ...)

where L1, L2, etc. are the individual losses as a percentage of input power.

Checking Transient Response

The regulator loop response can be checked by looking at the load transient response. Switching regulators take several cycles to respond to a step in DC (resistive) load current. When a load step occurs, V_{OUT} shifts by an amount equal to ΔI_{LOAD} • ESR, where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT}, generating the feedback error signal that forces the regulator to adapt to the current change and return V_{OUT} to its steady-state value. During this recovery time, V_{OUT} can be monitored for excessive overshoot or ringing, which would indicate a stability problem. **The availability of the I_{TH} pin not only allows optimization of control loop behavior, but also provides a DC coupled and AC filtered closed-loop response test point. The DC step, rise time and settling at this test point truly reflects the closed-loop response**. Assuming a predominantly second order system, phase margin and/or damping factor can be estimated using the percentage of overshoot seen at this pin. The bandwidth can also be estimated by examining the rise time at the pin. The I_{TH} external components shown in the Figure 1 circuit will provide an adequate starting point for most applications.

APPLICATIONS INFORMATION

The I_{TH} series R_C-C_C filter sets the dominant pole-zero loop compensation. The values can be modified slightly (from 0.2 to 5 times their suggested values) to maximize transient response once the final PC layout is done and the particular output capacitor type and value have been determined. The output capacitors need to be decided upon because the various types and values determine the loop feedback factor gain and phase. An output current pulse of 20% to 80% of full load current having a rise time of <2µs will produce output voltage and I_{TH} pin waveforms that will give a sense of the overall loop stability without breaking the feedback loop. The initial output voltage step, resulting from the step change in output current, may not be within the bandwidth of the feedback loop, so this signal cannot be used to determine phase margin. This is why it is better to look at the I_{TH} pin signal which is in the feedback loop and is the filtered and compensated control loop response. The gain of the loop will be increased by increasing R_C and the bandwidth of the loop will be increased by decreasing C_C. If R_C is increased by the same factor that C_C is decreased, the zero frequency will be kept the same, thereby keeping the phase the same in the most critical frequency range of the feedback loop. The output voltage settling behavior is related to the stability of the closed-loop system and will demonstrate the actual overall supply performance.

A second, more severe transient is caused by switching in loads with large (>1µF) supply bypass capacitors. The discharged bypass capacitors are effectively put in parallel with C_{OUT}, causing a rapid drop in V_{OUT}. No regulator can alter its delivery of current quickly enough to prevent this sudden step change in output voltage if the load switch resistance is low and it is driven quickly. If C_{LOAD} is greater than 2% of C_{OUT}, the switch rise time should be controlled so that the load rise time is limited to approximately $1000 \bullet R_{SENSE} \bullet C_{LOAD}$. Thus a 250µF capacitor and a 2mΩ R_{SENSE} resistor would require a 500µs rise time, limiting the charging current to about 1A.

Design Example (Using Three Phases)

As a design example, assume V_{IN} = 12V(nominal), V_{IN} = 20V(max), V_{OUT} = 1.3V, I_{MAX} = 45A and f = 400kHz. The inductance value is chosen first based upon a 30% ripple current assumption. The highest value of ripple current in each output stage occurs at the maximum input voltage.

$$L = \frac{V_{OUT}}{f(\Delta I)}\left(1-\frac{V_{OUT}}{V_{IN}}\right)$$
$$= \frac{1.3V}{(400kHz)(30\%)(15A)}\left(1-\frac{1.3V}{20V}\right)$$
$$\geq 0.68\mu H$$

Using L = 0.6µH, a commonly available value results in 34% ripple current. The worst-case output ripple for the three stages operating in parallel will be less than 11% of the peak output current.

R_{SENSE1}, R_{SENSE2} and R_{SENSE3} can be calculated by using a conservative maximum sense current threshold of 65mV and taking into account half of the ripple current:

$$R_{SENSE} = \frac{65mV}{15A\left(1+\frac{34\%}{2}\right)} = 0.0037\Omega$$

Use a commonly available 0.003Ω sense resistor.

Next verify the minimum on-time is not violated. The minimum on-time occurs at maximum V_{CC}:

$$t_{ON(MIN)} = \frac{V_{OUT}}{V_{IN(MAX)}(f)} = \frac{1.3V}{20V(400kHz)} = 162ns$$

APPLICATIONS INFORMATION

The output voltage will be set by the VID code according to Table 1.

The power dissipation on the topside MOSFET can be estimated. Using a Fairchild FDS6688 for example, $R_{DS(ON)}$ = 7mΩ, C_{MILLER} = 15nC/15V = 1000pF. At maximum input voltage with T(estimated) = 50°C:

$$P_{MAIN} \approx \frac{1.8V}{20V}(15)^2\left[1+(0.005)(50°C-25°C)\right]$$
$$0.007\Omega+(20)^2\left(\frac{45A}{(2)(3)}\right)(2\Omega)(1000pF)$$
$$\left(\frac{1}{5V-1.8V}+\frac{1}{1.8V}\right)(400kHz)=2.2W$$

The worst-case power dissipation by the synchronous MOSFET under normal operating conditions at elevated ambient temperature and estimated 50°C junction temperature rise is:

$$P_{SYNC}=\frac{20V-1.3V}{20V}(15A)^2(1.25)(0.007\Omega)=1.84W$$

A short circuit to ground will result in a folded back current of:

$$I_{SC} \approx \frac{25mV}{(2+3)m\Omega}+\frac{1}{2}\left(\frac{150ns(20V)}{0.6\mu H}\right)=7.5A$$

with a typical value of $R_{DS(ON)}$ and d = (0.005/°C)(50°C) = 0.25. The resulting power dissipated in the bottom MOSFET is:

$$P_{SYNC} = (7.5A)^2(1.25)(0.007\Omega) \approx 0.5W$$

which is less than one third of the normal, full load conditions. Incidentally, since the load no longer dissipates any power, total system power is decreased by over 90%. Therefore, the system actually cools significantly during a shorted condition!

PC Board Layout Checklist

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the IC. These items are also illustrated graphically in the layout diagram of Figure 10. Check the following in the PC layout:

1) Are the signal and power ground paths isolated? Keep the SGND at one end of a printed circuit path thus preventing MOSFET currents from traveling under the IC. The IC signal ground pin should be used to hook up all control circuitry on one side of the IC, routing the copper through SGND, under the IC covering the "shadow" of the package, connecting to the PGND pin and then continuing on to the (–) plates of C_{IN} and C_{OUT}. The V_{CC} decoupling capacitor should be placed immediately adjacent to the IC between the V_{CC} pin and PGND. A 1µF ceramic capacitor of the X7R or X5R type is small enough to fit very close to the IC to minimize the ill effects of the large current pulses drawn to drive the bottom MOSFETs. An additional 5µF to 10uF of ceramic, tantalum or other very low ESR capacitance is recommended in order to keep the internal IC supply quiet. The power ground returns to the sources of the bottom N-channel MOSFETs, anodes of the Schottky diodes and (–) plates of C_{IN}, which should have as short lead lengths as possible.

2) Does the IC IN^+ pin connect to the (+) plates of C_{OUT}? A 30pF to 300pF feedforward capacitor between the DIFFOUT and EAIN pins should be placed as close as possible to the IC.

3) Are the $SENSE^-$ and $SENSE^+$ printed circuit traces for each channel routed together with minimum PC trace spacing? The filter capacitors between $SENSE^+$ and $SENSE^-$ for each channel should be as close as possible to the pins of the IC. Connect the $SENSE^-$ and $SENSE^+$ pins to the pads of the sense resistor as illustrated in Figure 11.

4) Do the (+) plates of C_{IN} connect to the drains of the topside MOSFETs as closely as possible? This capacitor provides the pulsed current to the MOSFETs.

5) Keep the switching nodes, SWITCH, BOOST and TG away from sensitive small-signal nodes. Ideally the SWITCH, BOOST and TG printed circuit traces should be routed away and separated from the IC and the "quiet" side of the IC.

6) The filter capacitors between the I_{TH} and SGND pins should be as close as possible to the pins of the IC.

APPLICATIONS INFORMATION

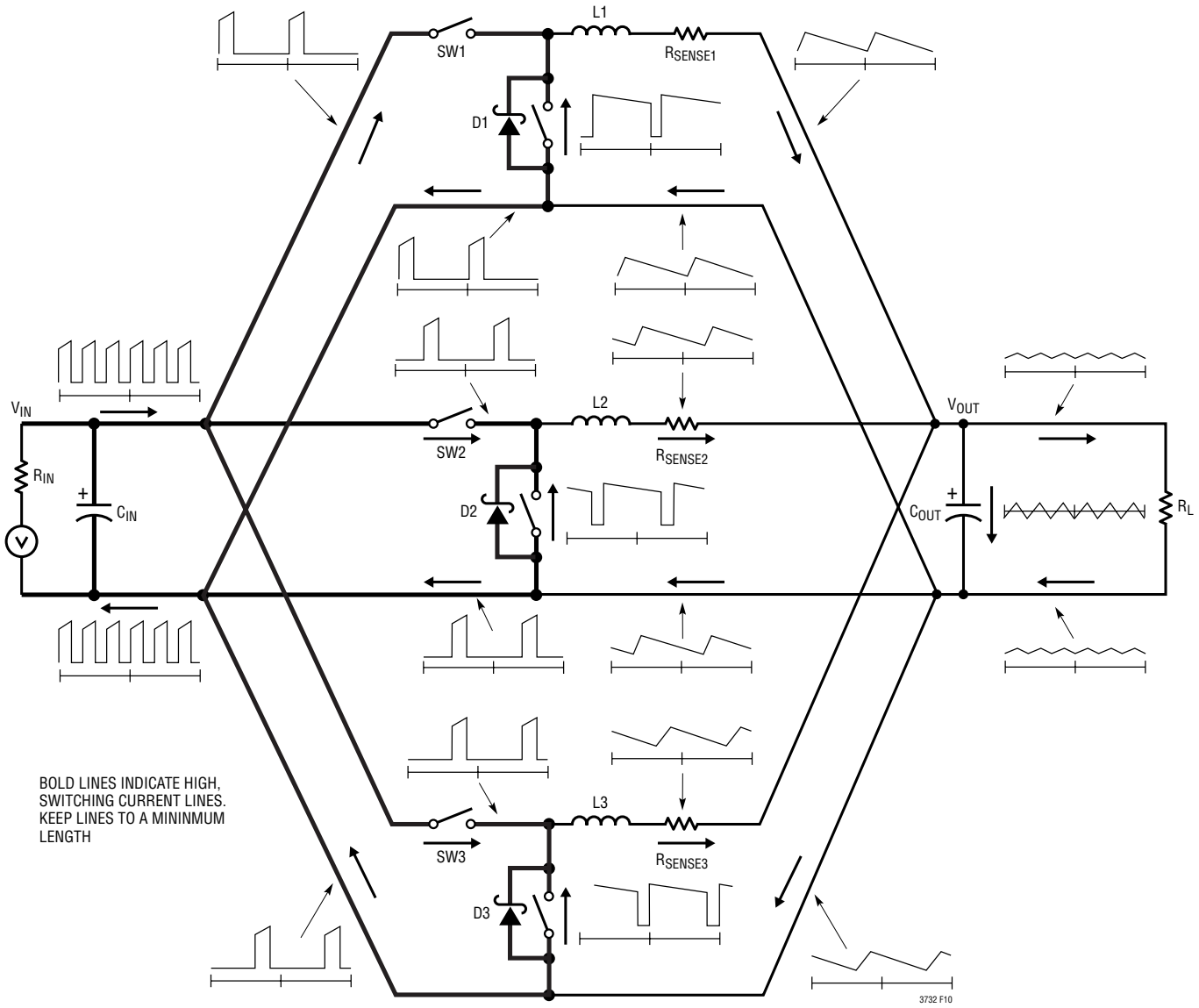


Figure 10. Branch Current Waveforms

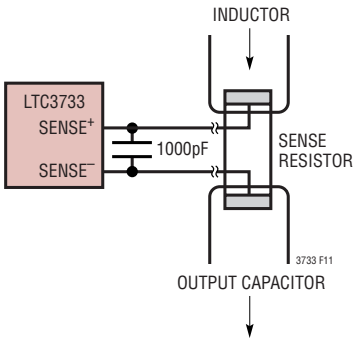


Figure 11. Kelvin Sensing R_{SENSE}

APPLICATIONS INFORMATION

Figure 10 illustrates all branch currents in a three-phase switching regulator. It becomes very clear after studying the current waveforms why it is critical to keep the high switching current paths to a small physical size. High electric and magnetic fields will radiate from these "loops" just as radio stations transmit signals. The output capacitor ground should return to the negative terminal of the input capacitor and not share a common ground path with any switched current paths. The left half of the circuit gives rise to the "noise" generated by a switching regulator. The ground terminations of the synchronous MOSFETs and Schottky diodes should return to the bottom plate(s) of the input capacitor(s) with a short isolated PC trace since very high switched currents are present. A separate isolated path from the bottom plate(s) of the input and output capacitor(s) should be used to tie in the IC power ground pin (PGND). This technique keeps inherent signals generated by high current pulses taking alternate current paths that have finite impedances during the total period of the switching regulator. External OPTI-LOOP compensation allows overcompensation for PC layouts which are not optimized but this is not the recommended design procedure.

Simplified Visual Explanation of How a 3-Phase Controller Reduces Both Input and Output RMS Ripple Current

The effect of multiphase power supply design significantly reduces the amount of ripple current in both the input and output capacitors. The RMS input ripple current is divided by, and the effective ripple frequency is multiplied up by the number of phases used (assuming that the input voltage is greater than the number of phases used times the output voltage). The output ripple amplitude is also reduced by, and the effective ripple frequency is increased by the number of phases used. Figure 12 graphically illustrates the principle.

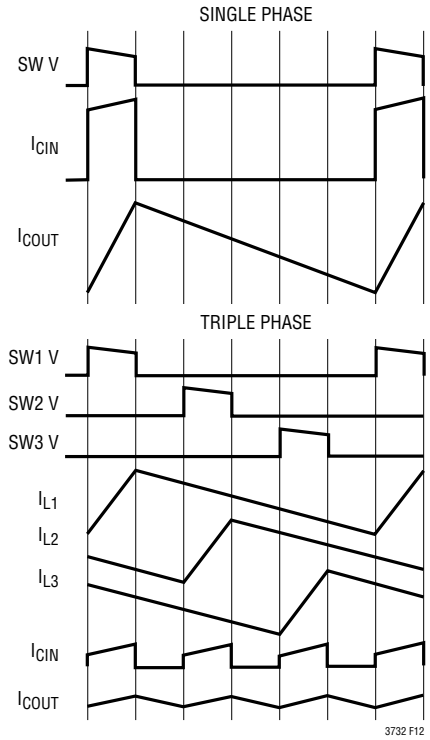


Figure 12. Single and Polyphase Current Waveforms

APPLICATIONS INFORMATION

The worst-case input RMS ripple current for a single stage design peaks at twice the value of the output voltage. The worst-case input RMS ripple current for a two stage design results in peaks at 1/4 and 3/4 of the input voltage, and the worst-case input RMS ripple current for a three stage design results in peaks at 1/6, 1/2, and 5/6 of the input voltage. The peaks, however, are at ever decreasing levels with the addition of more phases. A higher effective duty factor results because the duty factors "add" as long as the currents in each stage are balanced. Refer to AN19 for a detailed description of how to calculate RMS current for the single stage switching regulator.

Figure 6 illustrates the RMS input current drawn from the input capacitance versus the duty cycle as determined by the ration of input and output voltage. The peak input RMS current level of the single phase system is reduced by 2/3 in a 3-phase solution due to the current splitting between the three stages.

The output ripple current is reduced significantly when compared to the single phase solution using the same inductance value because the V_{OUT}/L discharge currents term from the stages that has their bottom MOSFETs on subtract current from the $(V_{CC} – V_{OUT})/L$ charging current resulting from the stage which has its top MOSFET on. The output ripple current for a 3-phase design is:

$$I_{P-P} = \frac{V_{OUT}}{(f)(L)}(1-3DC) \quad V_{IN} > 3V_{OUT}$$

The ripple frequency is also increased by three, further reducing the required output capacitance when $V_{CC} < 3V_{OUT}$ as illustrated in Figure 4.

Efficiency Calculation

To estimate efficiency, the DC loss terms include the input and output capacitor ESR, each MOSFET $R_{DS(ON)}$, inductor resistance R_L, the sense resistance R_{SENSE} and the forward drop of the Schottky rectifier at the operating output current and temperature. Typical values for the design example given previously in this data sheet are:

Main MOSFET $R_{DS(ON)}$ = 7mΩ (9mΩ at 90°C)
Sync MOSFET $R_{DS(ON)}$ = 7mΩ (9mΩ at 90°C)
C_{INESR} = 20mΩ
C_{OUTESR} = 3mΩ
R_L = 2.5mΩ
R_{SENSE} = 3mΩ
$V_{SCHOTTKY}$ = 0.8V at 15A (0.7V at 90°C)
V_{OUT} = 1.3V
V_{IN} = 12V
I_{MAX} = 0.8V at 15A (0.7V at 90°C)
δ = 0.01%°C
N = 3
f = 400kHz

The main MOSFET is on for the duty factor V_{OUT}/V_{IN} and the synchronous MOSFET is on for the rest of the period or simply $(1 – V_{OUT}/V_{IN})$. Assuming the ripple current is small, the AC loss in the inductor can be made small if a good quality inductor is chosen. The average current, I_{OUT} is used to simplify the calaculations. The equation below is not exact but should provide a good technique for the comparison of selected components and give a result that is within 10% to 20% of the final application.

APPLICATIONS INFORMATION

The temperature of the MOSFET's die temperature may require interative calculations if one is not familiar typical performance. A maximum operating junction temperature of 90° to 100°C for the MOSFETs is recommended for high reliability applications.

Common output path DC loss:

$$P_{COMPATH} \approx N\left(\frac{I_{MAX}}{N}\right)^2 (R_L + R_{SENSE}) + C_{OUTESR}\ Loss$$

This totals 3.375W + C_{OUTESR} loss.

Total of all three main MOSFET's DC loss:

$$P_{MAIN} = N\left(\frac{V_{OUT}}{V_{IN}}\right)\left(\frac{I_{MAX}}{N}\right)^2 (1+\delta)R_{DS(ON)} + C_{INESR}\ Loss$$

This totals 0.83W + C_{INESR} loss.

Total of all three synchronous MOSFET's DC loss:

$$P_{SYNC} = N\left(1-\frac{V_{OUT}}{V_{IN}}\right)\left(\frac{I_{MAX}}{N}\right)^2 (1+\delta)R_{DS(ON)}$$

This totals 5.4W.

Total of all three main MOSFET's AC loss:

$$P_{MAIN} \approx 3(V_{IN})^2 \frac{45A}{(2)(3)}(2\Omega)(1000pF)\left(\frac{1}{5V-1.8V}+\frac{1}{1.8V}\right)(400kHz) = 6.3W$$

This totals 1W at V_{IN} = 8V, 2.25W at V_{IN} = 12V and 6.25W at V_{IN} = 20V.

Total of all three synchronous MOSFET's AC loss:

$$(3)Q_G \frac{V_{IN}}{V_{DSSPEC}}(f) = (6)(15nC)\frac{V_{IN}}{V_{DSSPEC}}(4E5)$$

This totals 0.08W at V_{IN} = 8V, 0.12W at V_{IN} = 12V and 0.19W at V_{IN} = 20V. The bottom MOSFET does not experience the Miller capacitance dissipation issue that the main switch does because the bottom switch turns on when its drain is close to ground.

The Schottky rectifier loss assuming 50ns nonoverlap time:

$2 \bullet 3(0.7V)(15A)(50ns)(4E5)$

This totals 1.26W.

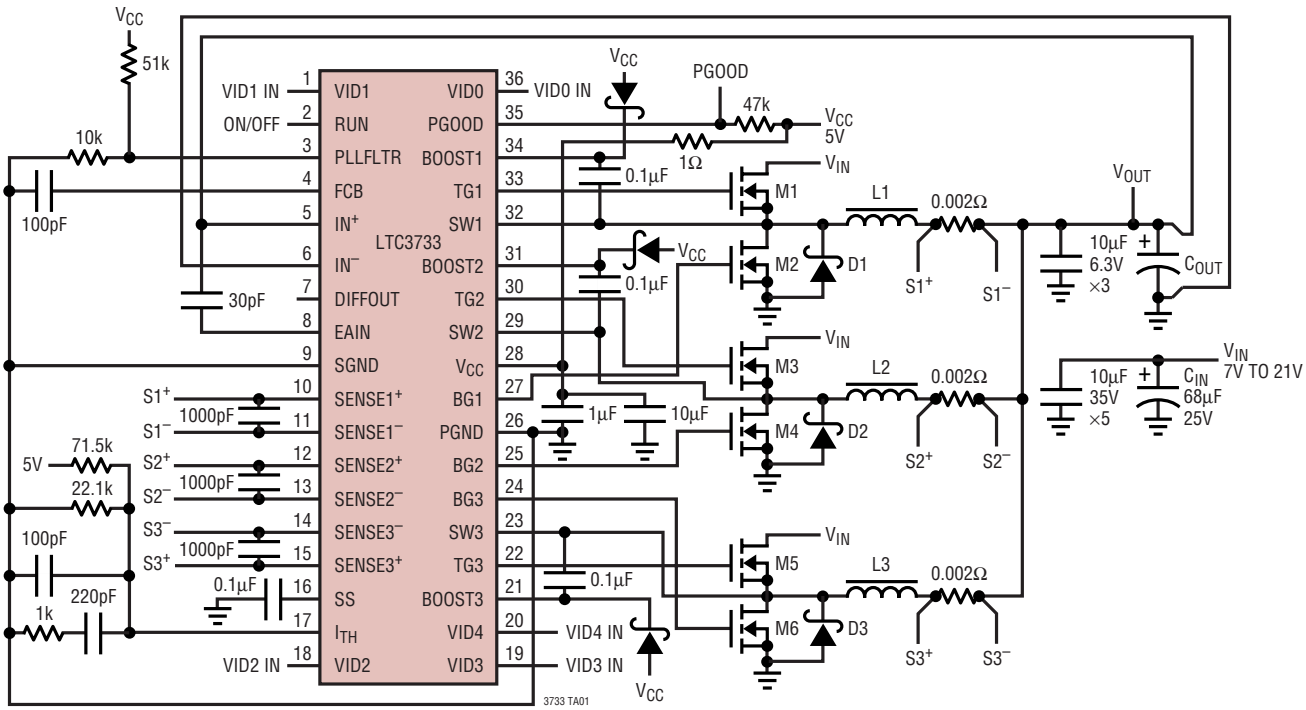
The total output power is (1.3V)(45A) = 58.5W and the total input power is approximately 60W so the % loss of each component is as follows:

Main switch AC loss (V_{IN} = 12V)	2.25W	3.75%
Main switch DC loss	0.83W	1.4%
Synchronous switch AC loss	0.19W	0.3%
Synchronous switch DC loss	5.4W	9%
Power path loss	3.375W	5.6%

The numbers above represent the values at V_{IN} = 12V. It can be seen from this simple example that two things can be done to improve efficiency: 1) Use two MOSFETs on the synchronous side and 2) use a smaller MOSFET for the main switch with smaller C_{MILLER} to better balance the AC loss with the DC loss. A smaller, less expensive MOSFET can actually perform better in the task of the main switch.

TYPICAL APPLICATION

65A Power Supply for AMD Opteron Processors

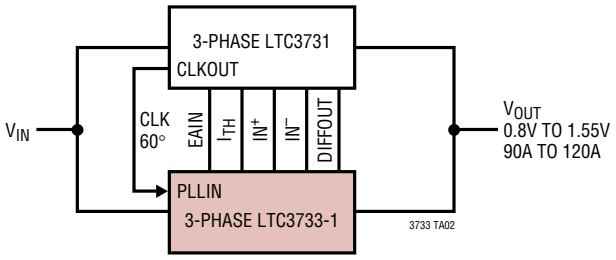


V_{IN}: 7V TO 21V
V_{OUT}: 0.8V TO 1.55V, 65A
SWITCHING FREQUENCY: 300kHz

C_{IN}: SANYO OS-CON 25SP68M
C_{OUT}: 330µF/2.5V ×10 SANYO POSCAP 2R5TPE330M9
D1 TO D3: MBRS340T3

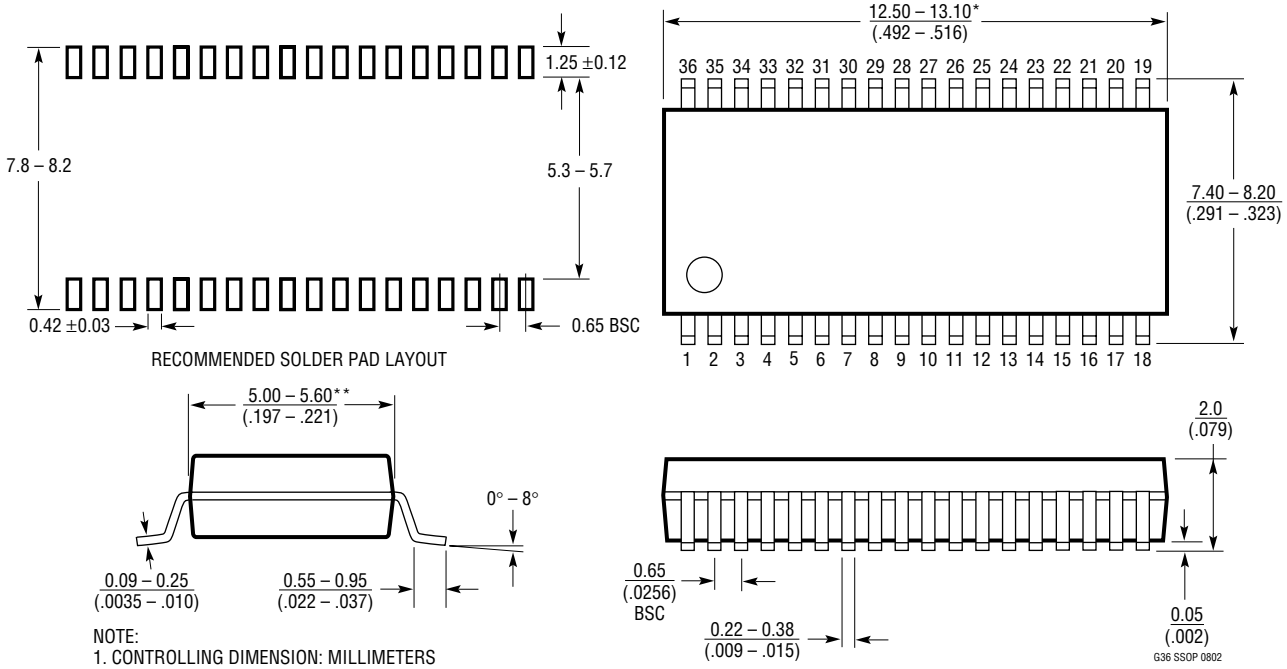
L1 TO L3: 0.68µH SUMIDA CEP125-0R6
M1, M3, M5: HAT2168H ×1 OR IRF7811W ×2 OR Si7860DP ×1
M2, M4, M6: HAT2165H ×2 OR IRF7822 ×2 OR Si7892DP ×2

Block Diagram—6-Phase LTC3731/LTC3733-1 Supply



PACKAGE DESCRIPTION

G Package
36-Lead Plastic SSOP (5.3mm)
(Reference LTC DWG # 05-08-1640)



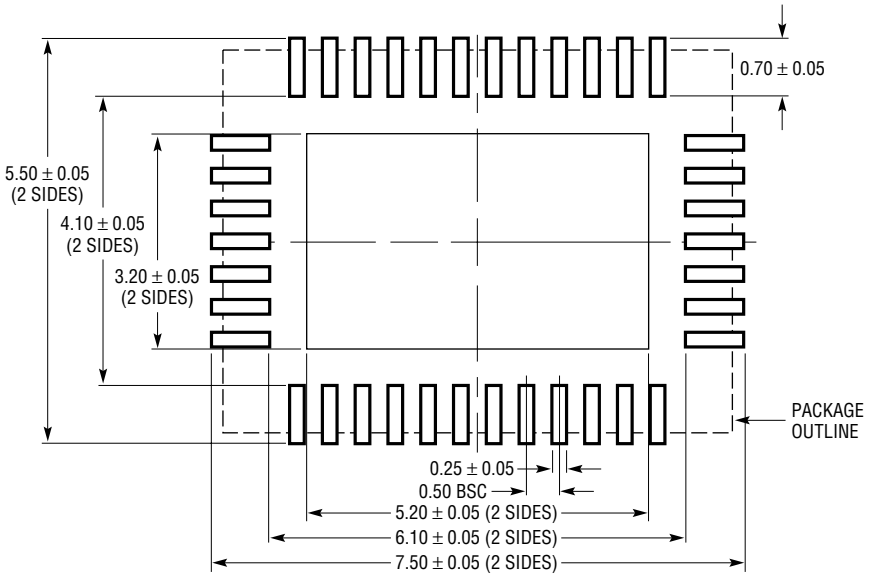
NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN $\frac{\text{MILLIMETERS}}{(\text{INCHES})}$
3. DRAWING NOT TO SCALE

*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .152mm (.006") PER SIDE

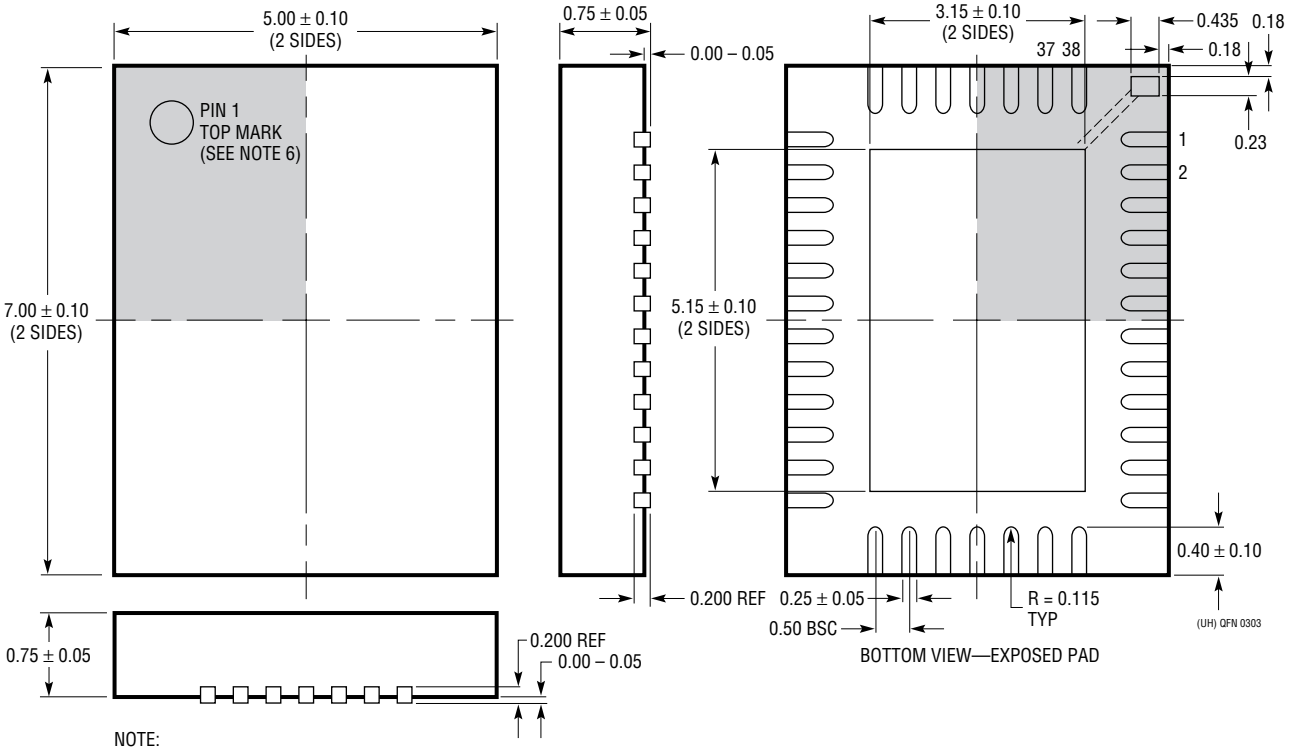
**DIMENSIONS DO NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED .254mm (.010") PER SIDE

PACKAGE DESCRIPTION

UHF Package
38-Lead Plastic QFN (7mm × 5mm)
(Reference LTC DWG # 05-08-1701)



RECOMMENDED SOLDER PAD LAYOUT



NOTE:
1. DRAWING CONFORMS TO JEDEC PACKAGE OUTLINE M0-220 VARIATION WHKD
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1628	2-Phase, Dual Output Synchronous Step-Down DC/DC Controllers	Reduces C_{IN} and C_{OUT}, Power Good Output Signal, Synchronizable, $3.5V \le V_{IN} \le 36V$, I_{OUT} up to 20A, $0.8V \le V_{OUT} \le 5V$
LTC1629/ LTC1629-PG	20A to 200A PolyPhase Synchronous Controllers	Expandable from 2-Phase to 12-Phase, Uses All Surface Mount Components, No Heat Sink, V_{IN} up to 36V
LTC1702	No R_{SENSE}™ 2-Phase Dual Synchronous Step-Down Controller	550kHz, No Sense Resistor
LTC1703	No R_{SENSE} 2-Phase Dual Synchronous Step-Down Controller with 5-Bit Mobile VID Control	Mobile Pentium® III Processors, 550kHz, $V_{IN} \le 7V$
LTC1708-PG	2-Phase, Dual Synchronous Controller with Mobile VID	$3.5V \le V_{IN} \le 36V$, VID Sets V_{OUT1}, PGOOD
LT®1709/ LT1709-8	High Efficiency, 2-Phase Synchronous Step-Down Switching Regulators with 5-Bit VID	$1.3V \le V_{OUT} \le 3.5V$, Current Mode Ensures Accurate Current Sharing, $3.5V \le V_{IN} \le 36V$
LTC1735	High Efficiency Synchronous Step-Down Switching Regulator	Output Fault Protection, 16-Pin SSOP
LTC1736	High Efficiency Synchronous Controller with 5-Bit Mobile VID Control	Output Fault Protection, 24-Pin SSOP, $3.5V \le V_{IN} \le 36V$
LTC1778	No R_{SENSE} Current Mode Synchronous Step-Down Controller	Up to 97% Efficiency, $4V \le V_{IN} \le 36V$, $0.8V \le V_{OUT} \le (0.9)(V_{IN})$, I_{OUT} up to 20A
LTC1929/ LTC1929-PG	2-Phase Synchronous Controllers	Up to 42A, Uses All Surface Mount Components, No Heat Sinks, $3.5V \le V_{IN} \le 36V$
LTC3708	Dual, 2-Phase, No R_{SENSE} Synchronous Buck with Output Tracking	Up/Down Output Voltage Tracking, Track Up to 8 Supplies, Fast Transient Response
LTC3711	No R_{SENSE} Current Mode Synchronous Step-Down Controller with Digital 5-Bit Interface	Up to 97% Efficiency, Ideal for Pentium III Processors, $0.925V \le V_{OUT} \le 2V$, $4V \le V_{IN} \le 36V$, I_{OUT} up to 20A
LTC3719	2-Phase, 5-Bit VID Current Mode, High Efficiency Synchronous Step-Down Controller	AMD Hammer-K8 Processors, Wide V_{IN} Range: 4V to 36V Operation
LTC3729	20A to 200A, 550kHz PolyPhase Synchronous Controller	Expandable from 2-Phase to 12-Phase, Uses all Surface Mount Components, V_{IN} up to 36V
LTC3731	3-Phase, 600kHz Synchronous Buck Switching Regulator Controller	Expandable from 3-Phase to 12-Phase, Uses all Surface Mount Components, V_{IN} up to 36V
LTC3732	3-Phase, 5-Bit VID, 600kHz Synchronous Buck Switching Regulator Controller	VRM9.0 and VRM9.1 (VID = 1.1V to 1.85V)

No R_{SENSE} is a trademark of Linear Technology Corporation. Pentium is a registered trademark of Intel Corporation.

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