15V Dual 3A Monolithic Step-Down Regulator for DDR Power

FEATURES

- **3.6V to 15V Input Voltage Range**
- **±3A Output Current per Channel**
- **Up to 95% Efficiency**
- **Selectable 90°/180° Phase Shift Between Channels**
- **Adjustable Switching Frequency: 500kHz to 4MHz**
- VTTR = $V_{DDQ}/2 = V_{TT}$ Reference
- ±1.6% Accurate VTTR at 0.75V
- Optimal V_{OUT} Range: 0.6V to 3V
- ±10mA Buffered Output Supplies V_{REF} Reference Voltage
- Current Mode Operation for Excellent Line and Load Transient Response
- External Clock Synchronization
- Short-Circuit Protected
- Input Overvoltage and Overtemperature Protection
- Power Good Status Outputs
- Available in (4mm × 5mm) QFN-28 and Thermally Enhanced 28-Lead TSSOP Packages

APPLICATIONS

- DDR Memory Power Supplies

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DESCRIPTION

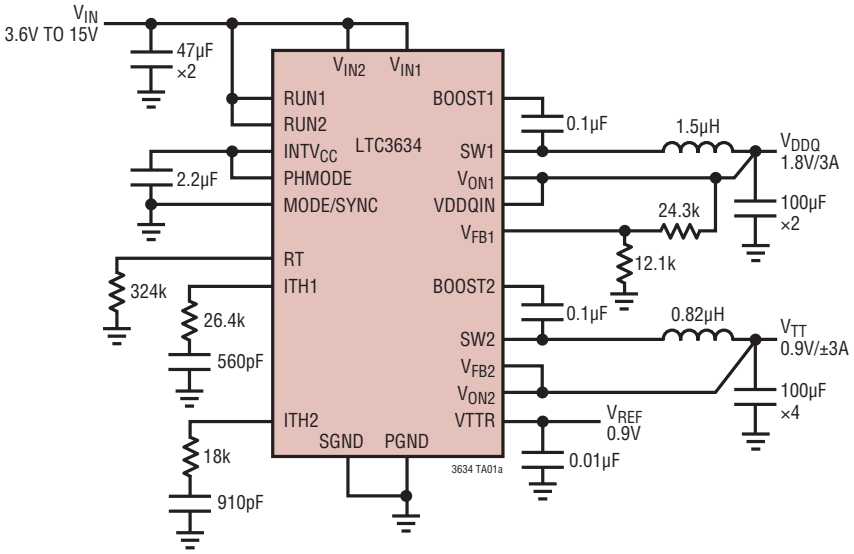
The LTC®3634 is a high efficiency, dual-channel monolithic synchronous step-down regulator which provides power supply and bus termination rails for DDR1, DDR2, and DDR3 SDRAM controllers. The operating input voltage range is 3.6V to 15V, making it suitable for point-of-load power supply applications from a 5V or 12V input, as well as various battery powered systems.

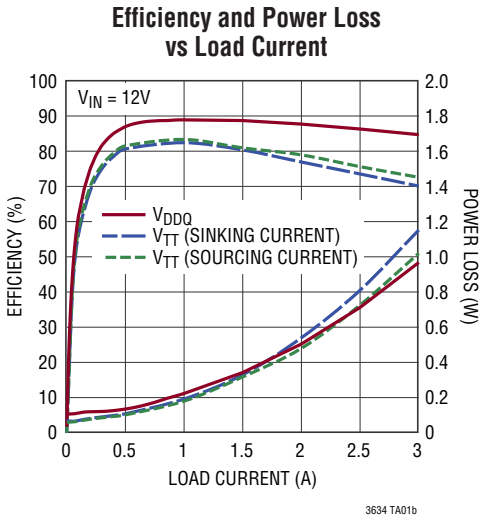
The V_{TT} regulated output voltage is equal to VDDQIN•0.5. An on-chip buffer capable of driving a 10mA load provides a low noise reference output (VTTR) also equal to VDDQIN•0.5.

The operating frequency is programmable and synchronizable from 500kHz to 4MHz with an external resistor. The two channels can operate 180° out-of-phase, which relaxes the requirements for input and output capacitance. The unique controlled on-time architecture is ideal for powering DDR applications from a 12V supply at high switching frequencies, allowing the use of smaller external components.

The LTC3634 is offered in both 28-pin 4mm × 5mm QFN and 28-pin exposed pad TSSOP packages.

TYPICAL APPLICATION

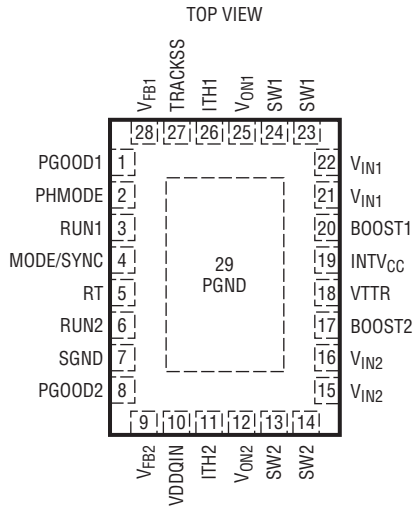




ABSOLUTE MAXIMUM RATINGS (Note 1)

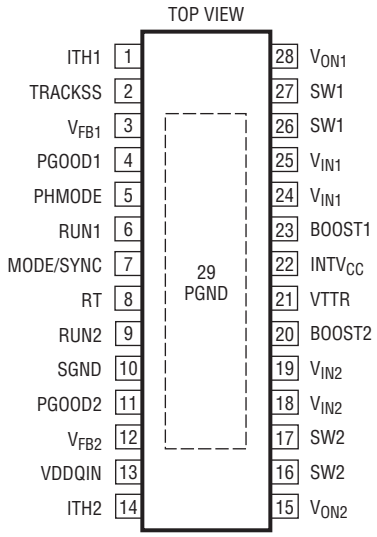
V_{IN1}, V_{IN2} ..... –0.3V to 16V
V_{IN1}, V_{IN2} Transient (Note 2) 18V
PGOOD1, PGOOD2, V_{ON1}, V_{ON2}..... –0.3V to 16V
VTTR, $INTV_{CC}$, TRACKSS, VDDQIN ..... –0.3V to 3.6V
ITH1, ITH2, RT, MODE/SYNC .....–0.3V to $INTV_{CC}$ + 0.3V
V_{FB1}, V_{FB2}, PHMODE.....–0.3V to $INTV_{CC}$ + 0.3V
BOOST1-SW1, BOOST2-SW2..... –0.3V to 3.6V
BOOST1, BOOST2 .....–0.3V to 19.6V
RUN1, RUN2 ..... –0.3V to V_{IN} + 0.3V
SW Source and Sink Current (DC) (Note 3) 3A
Operating Junction Temperature Range (Notes 4, 5, 8)
LTC3634E, LTC3634I ..... –40°C to 125°C
LTC3634H..... –40°C to 150°C
LTC3634MP..... –55°C to 150°C
Storage Temperature Range .....–65°C to 150°C
Lead Temperature
(Soldering, 10 sec, TSSOP Package)..... 260°C

PIN CONFIGURATION



UFD PACKAGE
28-LEAD (4mm × 5mm) PLASTIC QFN

T_{JMAX} = 150°C, θ_{JA} = 43°C/W
EXPOSED PAD (PIN 29) IS PGND, MUST BE SOLDERED TO PCB



FE PACKAGE
28-LEAD PLASTIC TSSOP

T_{JMAX} = 150°C, θ_{JA} = 25°C/W
EXPOSED PAD (PIN 29) IS PGND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3634EUFD#PBF	LTC3634EUFD#TRPBF	3634	28-Lead (5mm × 4mm) Plastic QFN	–40°C to 125°C
LTC3634IUFD#PBF	LTC3634IUFD#TRPBF	3634	28-Lead (5mm × 4mm) Plastic QFN	–40°C to 125°C
LTC3634HUFD#PBF	LTC3634HUFD#TRPBF	3634	28-Lead (5mm × 4mm) Plastic QFN	–40°C to 150°C
LTC3634MPUFD#PBF	LTC3634MPUFD#TRPBF	3634	28-Lead (5mm × 4mm) Plastic QFN	–55°C to 150°C
LTC3634EFE#PBF	LTC3634EFE#TRPBF	LTC3634FE	28-Lead Plastic TSSOP	–40°C to 125°C
LTC3634IFE#PBF	LTC3634IFE#TRPBF	LTC3634FE	28-Lead Plastic TSSOP	–40°C to 125°C
LTC3634HFE#PBF	LTC3634HFE#TRPBF	LTC3634FE	28-Lead Plastic TSSOP	–40°C to 150°C
LTC3634MPFE#PBF	LTC3634MPFE#TRPBF	LTC3634FE	28-Lead Plastic TSSOP	–55°C to 150°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified junction temperature range, otherwise specifications are at T_A = 25°C (Note 4). V_{IN} = 12V, $INTV_{CC}$ = 3.3V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	V_{IN1}, Operating Supply Range V_{IN2}, Operating Supply Range	 V_{IN1} > 3.6V	● ●	3.6 1.4		15 15	V V
	Output Voltage Range	V_{ON} = V_{OUT} (Note 6)		0.6		3	V
I_Q	Input DC Supply Current (V_{IN1} + V_{IN2}) Active (Note 7) Shutdown	 RUN1 = RUN2 = V_{IN} RUN1 = RUN2 = 0V			 1.3 15		 mA µA
V_{FBREG1}	Feedback Reference Voltage	3.6V < V_{IN} < 15V, 0.5V < ITH < 1.8V 0°C < T_A < 85°C –55°C < T_A < 150°C	 ● ●	 0.594 0.592	 0.6 0.6	 0.606 0.606	 V V
V_{FBREG2}	Feedback Reference Voltage	3.6V < V_{IN} < 15V, 0.5V < ITH < 1.8V	●	VTTR – 6	VTTR	VTTR + 6	mV
VTTR	VTTR Voltage Reference	1.5V < VDDQIN < 2.6V I_{LOAD} = ±10mA, C_{LOAD} < 10nF	●	0.492 • VDDQIN	0.50 • VDDQIN	0.508 • VDDQIN	V
I_{FB}	Feedback Pin Input Current					±30	nA
$g_{m(EA)}$	Error Amplifier Transconductance	ITH = 1.2V			1.0		mS
$t_{ON(MIN)}$	Minimum On-Time	V_{ON} = 0.5V, V_{IN} = 4V			20		ns
$t_{OFF(MIN)}$	Minimum Off-Time	V_{IN} = 6V			40	60	ns
f_{OSC}	Oscillator Frequency	V_{RT} = $INTV_{CC}$ R_T = 162k R_T = 80.6k		1.4 1.7 3.4	2 2 4	2.6 2.3 4.6	MHz MHz MHz
I_{LIM1}	Channel 1 Valley Switch Current Limit Positive Limit Negative Limit			3.3	4.4 8	5.5	 A A
I_{LIM2}	Channel 2 Valley Switch Current Limit Positive Limit Negative Limit			3.3	4.4 8	5.5	 A A
$R_{DS(ON)}$	Channel 1 Top Switch On-Resistance Bottom Switch On-Resistance Channel 2 Top Switch On-Resistance Bottom Switch On-Resistance				 130 65 130 65		 mΩ mΩ mΩ mΩ

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating temperature range, otherwise specifications are at T_A = 25°C (Note 4). V_{IN} = 12V, $INTV_{CC}$ = 3.3V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	Switch Leakage Current	V_{IN} = 15V, V_{RUN} = 0V			0.01	±1	µA
	V_{IN} Overvoltage Lockout Threshold	V_{IN} Rising V_{IN} Falling		16.8 15.8	17.5 16.5	18 17	V V
	$INTV_{CC}$ Voltage	3.6V < V_{IN} < 15V, 0mA Load		3.1	3.3	3.5	V
	$INTV_{CC}$ Load Regulation	0mA to 50mA Load, V_{IN} = 4V to 15V			0.7		%
	RUN Threshold Rising RUN Threshold Falling		● ●	1.18 0.98	1.22 1.01	1.26 1.04	V V
	RUN Leakage Current				0	±1	µA
	PGOOD Good-to-Bad Threshold	V_{FB} Rising V_{FB} Falling			8 –8	10 –10	% %
	PGOOD Hysteresis	V_{FB} from Bad-to-Good			15		mV
R_{PGOOD}	PGOOD Pull-Down Resistance	10mA Load			15		Ω
	Power Good Filter Time			20	40		µs
t_{SS1}	Channel 1 Internal Soft-Start Ramp Rate			0.7	1.2		V/ms
t_{SS2}	Channel 2 Internal Soft-Start Ramp Rate			1.5	2.2		V/ms
	V_{FB1} During Tracking	TRACKSS = 0.3V		0.28	0.3	0.315	V
$I_{TRACKSS}$	TRACKSS Pull-Up Current				1.4		µA
	Phase Shift Between Channel 1 and Channel 2	PHMODE = 0V PHMODE = $INTV_{CC}$			90 180		deg deg
	PHMODE Threshold Voltage	V_{IH} V_{IL}		1		 0.3	V V
	MODE/SYNC Threshold Voltage	V_{IH} V_{IL}		1		 0.4	V V
	SYNC Threshold Voltage	V_{IH}		0.95			V
	MODE/SYNC Input Current	MODE = 0V MODE = $INTV_{CC}$			1.5 –1.5		µA µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Transient event duration must be < 1% of total lifetime of the part.

Note 3: Guaranteed by long term current density limitations.

Note 4: The LTC3634 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC3634E is guaranteed to meet specified performance from 0°C to 85°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3634I is guaranteed to meet specifications over the –40°C to 125°C operating junction temperature range. The LTC3634H is guaranteed over the –40°C to 150°C operating junction temperature range and the LTC3634MP is tested and guaranteed over the –55°C to 150°C operating junction temperature range. High junction temperatures degrade operating lifetimes; operating lifetime is derated for junction temperatures greater than 125°C. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors.

Note 5: The junction temperature (T_J, in °C) is calculated from the ambient temperature (T_A, in °C), package thermal impedance (θ_{JA}, in °C/W), and power dissipation (P_D, in Watts) according to the formula: $T_J = T_A + P_D \bullet \theta_{JA}$.

Note 6: Output voltage settings above 3V are not optimized for controlled on-time operation. For designs that set output voltages above 3V, please refer to the Applications Information section for information on device operation outside the optimized range.

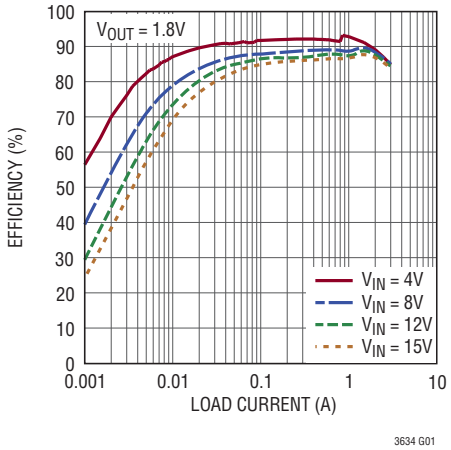
Note 7: Dynamic supply current is higher due to the internal gate charge being delivered at the switching frequency.

Note 8: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 150°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

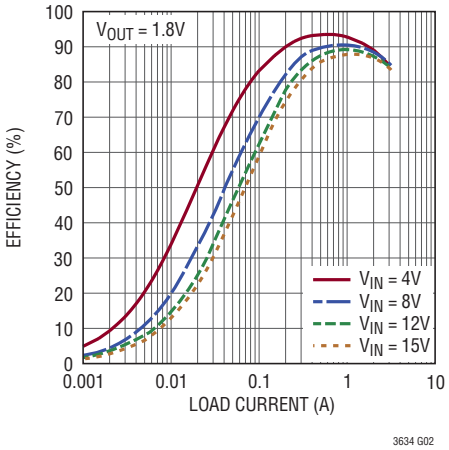
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{IN} = 12V, f_{SW} = 1MHz, L = 1.5µH unless otherwise noted.

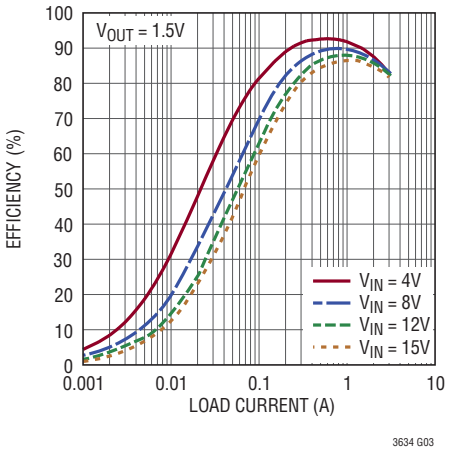
Efficiency vs Load Current (Burst Mode Operation)



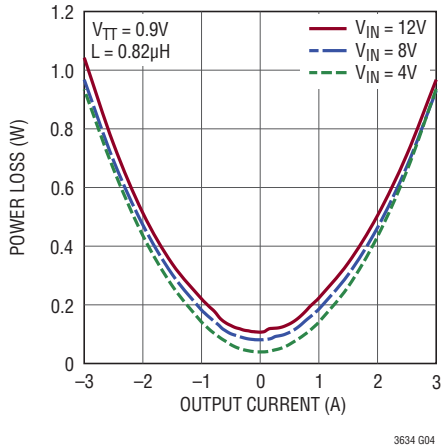
Efficiency vs Load Current (Forced Continuous)



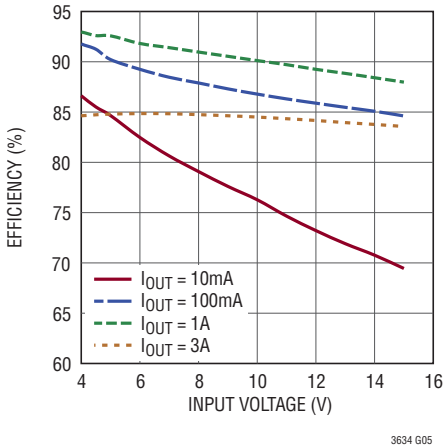
Efficiency vs Load Current (Forced Continuous)



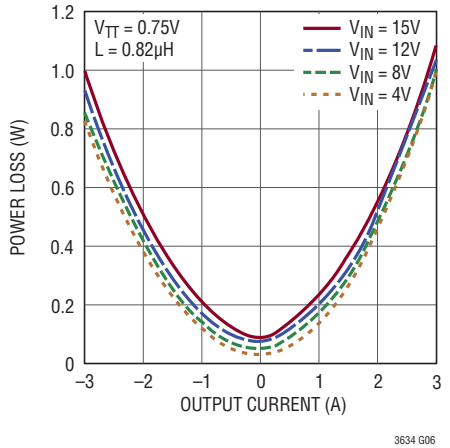
V_{TT} Power Loss vs Load Current, Sourcing and Sinking



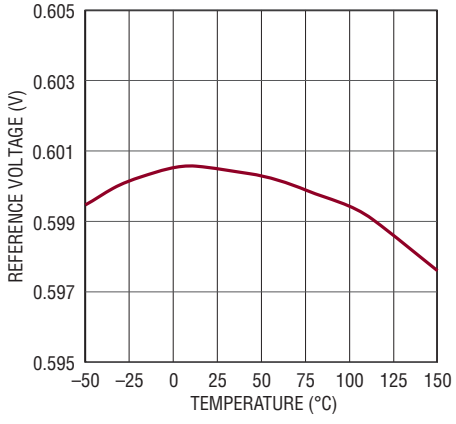
Efficiency vs Input Voltage



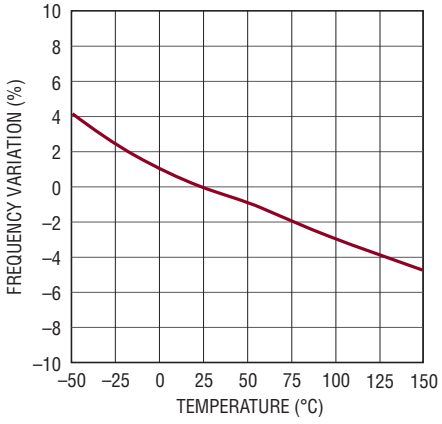
V_{TT} Power Loss vs Load Current



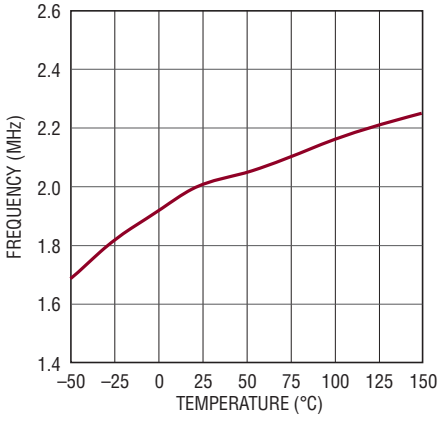
Reference Voltage vs Temperature



Oscillator Frequency vs Temperature



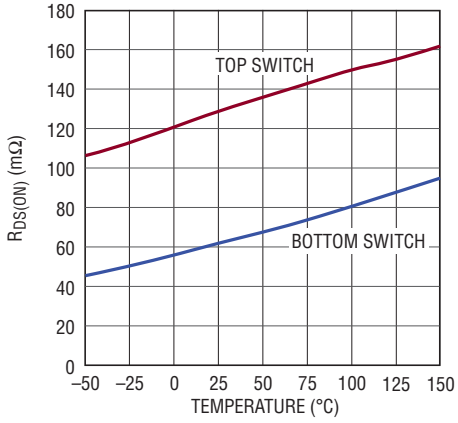
Oscillator Internal Set Frequency vs Temperature



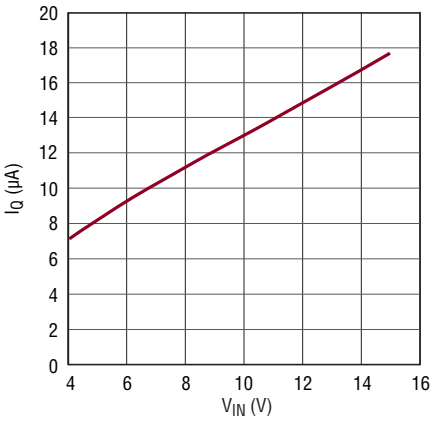
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{IN} = 12V, f_{SW} = 1MHz, L = 1.5µH unless otherwise noted.

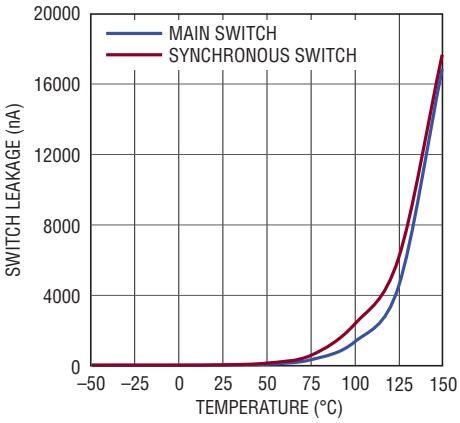
$R_{DS(ON)}$ vs Temperature



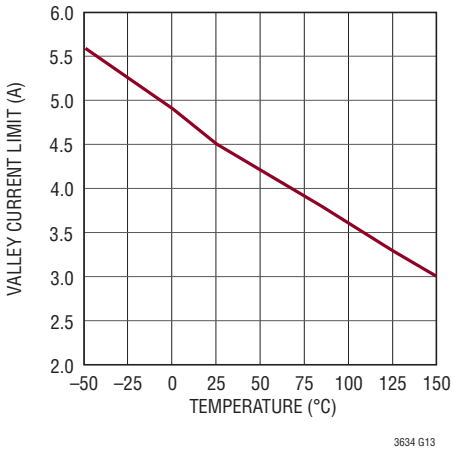
Shutdown Current vs V_{IN}



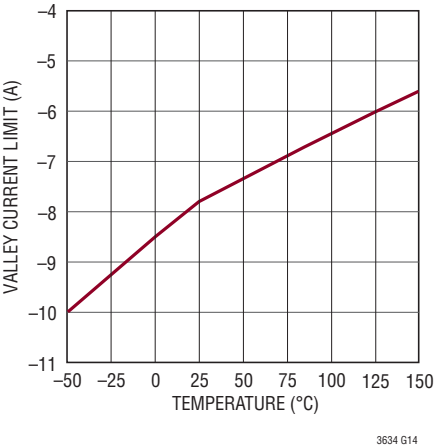
Switch Leakage vs Temperature



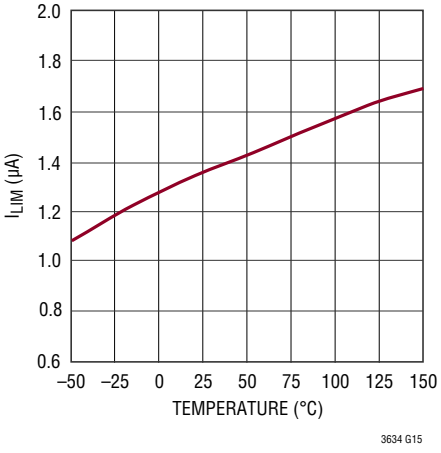
Valley Current Positive Limit vs Temperature



Valley Current Negative Limit vs Temperature



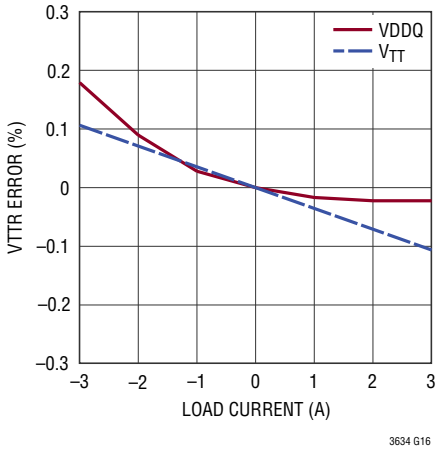
TRACKSS Pull-Up Current vs Temperature



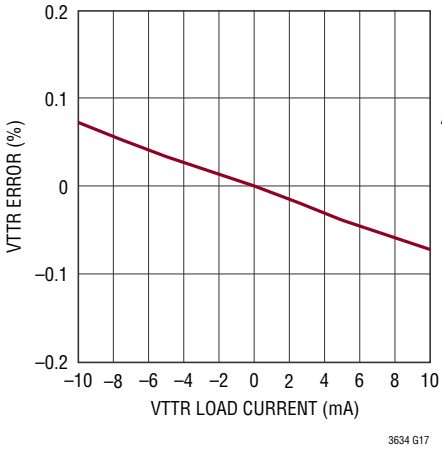
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{IN} = 12V, f_{SW} = 1MHz, L = 1.5µH unless otherwise noted.

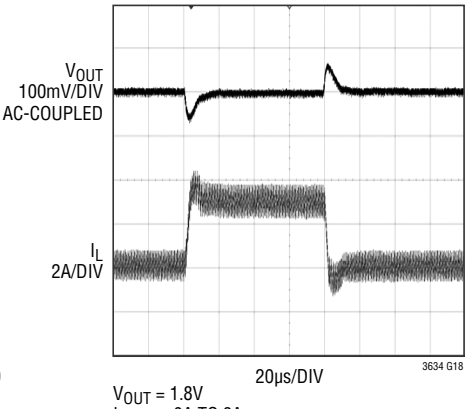
Load Regulation



VTTR Load Regulation

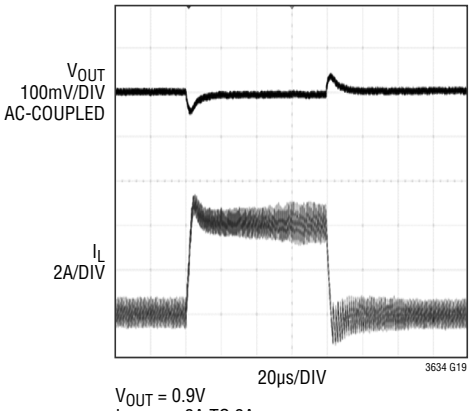


V_{DDQ} Load Step



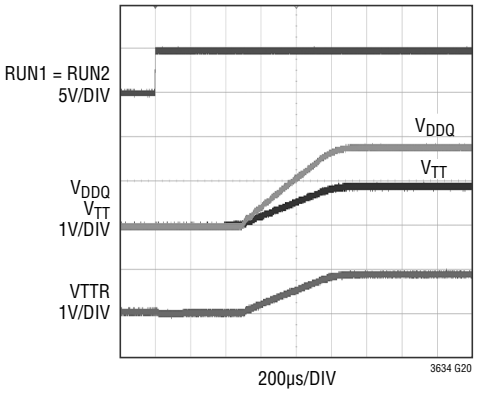
V_{OUT} = 1.8V
I_{LOAD} = 0A TO 3A

V_{TT} Load Step

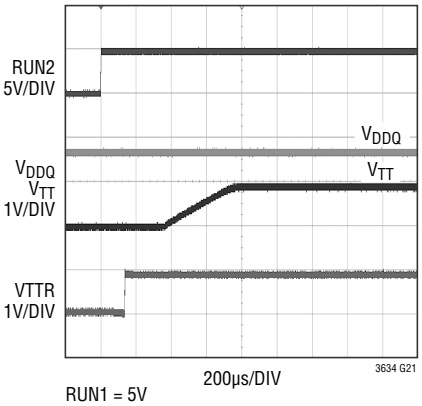


V_{OUT} = 0.9V
I_{LOAD} = –2A TO 2A

Start-Up



Start-Up (Channel 2)



RUN1 = 5V

PIN FUNCTIONS (QFN/TSSOP)

PGOOD1 (Pin 1/Pin 4): Channel 1 Open-Drain Power Good Output Pin. PGOOD1 is pulled to ground when the voltage on the V_{FB1} pin is not within ±8% (typical) of the internal 0.6V reference. This threshold has 15mV of hysteresis.

PHMODE (Pin 2/Pin 5): Phase Select Input. Tie this pin to ground to force both channels to switch 90° out-of-phase. Tie this pin to $INTV_{CC}$ to force both channels to switch 180° out-of-phase. Do not float this pin.

RUN1 (Pin 3/Pin 6): Channel 1 Regulator Enable Pin. Enables channel 1 operation by tying RUN1 above 1.22V. Tying it below 1V places Channel 1 into shutdown. Do not float this pin.

MODE/SYNC (Pin 4/Pin 7): Channel 1 Mode Select and External Synchronization Input. Tie this pin to ground to force continuous synchronous operation on Channel 1. Floating this pin or tying it to $INTV_{CC}$ enables high efficiency Burst Mode® operation at light loads. Channel 2 operation is forced continuous regardless of the state of this pin. Drive this pin with a clock to synchronize the LTC3634 switching frequency. An internal phase-locked loop will force the bottom power NMOS's turn-on signal to be synchronized with the rising edge of the CLKIN signal. When this pin is driven with a clock, forced continuous mode is automatically selected.

RT (Pin 5/Pin 8): Oscillator Frequency Program Pin. Connect an external resistor (between 80k to 640k) from this pin to SGND in order to program the frequency from 500kHz to 4MHz. When RT is tied to $INTV_{CC}$, the switching frequency will default to 2MHz. See the Applications Information section.

RUN2 (Pin 6/Pin 9): Channel 2 Regulator Enable Pin. Enables channel 2 operation by tying RUN2 above 1.22V. Tying it below 1V places Channel 2 into shutdown. Do not float this pin.

SGND (Pin 7/Pin 10): Signal Ground Pin. This pin should have a low noise connection to reference ground. The feedback resistor network, external compensation network, and R_T resistor should be connected to this ground.

PGOOD2 (Pin 8/Pin 11): Channel 2 Open-Drain Power Good Output Pin. PGOOD2 is pulled to ground when the voltage on the V_{FB2} pin is not within 8% (typical) of VDDQIN • 0.5. This threshold has 15mV of hysteresis.

V_{FB2} (Pin 9/Pin 12): Channel 2 Output Feedback Voltage Pin. Input to the error amplifier that compares the feedback voltage to VTTR. Connect this pin directly to the output in order to set V_{OUT2} equal to VTTR.

VDDQIN (Pin 10/Pin 13): External Reference Input for Channel 2. An internal resistor divider sets the VTTR pin voltage to be equal to half the voltage applied to this input. Channel 2 uses the VTTR pin voltage as its error amplifier reference.

ITH2 (Pin 11/Pin 14): Channel 2 Error Amplifier Output and Switching Regulator Compensation Pin. Connect this pin to appropriate external components to compensate the regulator loop frequency response. See the Applications Information section for guidelines on component selection.

V_{ON2} (Pin 12/Pin 15): On-Time Voltage Input for Channel 2. This pin sets the voltage trip point for the on-time comparator. Tying this pin to the output voltage makes the on-time proportional to V_{OUT2} when V_{OUT2} < 3V. When V_{OUT2} > 3V, switching frequency may become higher than the set frequency (see the Applications Information section). The pin impedance is nominally 150kΩ.

SW2 (Pins 13, 14/Pins 16, 17): Channel 2 Switch Node Connection to External Inductor. Voltage swing of SW is from a diode voltage below ground to a diode voltage above V_{IN2}.

V_{IN2} (Pins 15, 16/Pins 18, 19): Power Supply Input for Channel 2. Input voltage to the on-chip power MOSFETs on channel 2. This input is capable of operating from a supply voltage separate from V_{IN1}.

BOOST2 (Pin 17/Pin 20): Boosted Floating Driver Supply for Channel 2. The (+) terminal of the bootstrap capacitor connects to this pin while the (–) terminal connects to the SW pin. The normal operation voltage swing of this pin ranges from a diode voltage drop below $INTV_{CC}$ up to V_{IN2} + $INTV_{CC}$.

PIN FUNCTIONS (QFN/TSSOP)

VTTR (Pin 18/Pin 21): Reference Output. This output is used to supply the V_{REF} voltage for DDR memory. An on-chip buffer amplifier outputs a low noise reference voltage equal to VDDQIN/2. This output is capable of supplying 10mA. The buffer output can drive capacitive loads up to 0.01µF. A small series resistance (1Ω) between the output and the load further increases the amount of capacitance that the amplifier can drive. The error amplifier for channel 2 uses this voltage as its reference voltage.

$INTV_{CC}$ (Pin 19/Pin 22): Internal 3.3V Regulator Output. The internal gate drivers and control circuits are powered from this voltage. Decouple this pin to power ground with a minimum of 1µF low ESR ceramic capacitor. The internal regulator is disabled when both Channel 1 and Channel 2 are disabled with the RUN1/RUN2 inputs.

BOOST1 (Pin 20/Pin 23): Boosted Floating Driver Supply for Channel 1. The (+) terminal of the bootstrap capacitor connects to this pin while the (–) terminal connects to the SW pin. The normal operation voltage swing of this pin ranges from a diode voltage drop below $INTV_{CC}$ up to V_{IN1} + $INTV_{CC}$.

V_{IN1} (Pins 21, 22/Pins 24, 25): Power Supply Input for Channel 1. Input voltage to the on-chip power MOSFETs on channel 1. The internal LDO for $INTV_{CC}$ is powered from this pin.

SW1 (Pins 23, 24/Pins 26, 27): Channel 1 Switch Node Connection to External Inductor. Voltage swing of SW is from a diode voltage drop below ground to a diode voltage above V_{IN1}.

V_{ON1} (Pin 25/Pin 28): On-Time Voltage Input for Channel 1. This pin sets the voltage trip point for the on-time comparator. Tying this pin to the regulated output voltage makes the on-time proportional to V_{OUT1} when V_{OUT1} < 3V. When V_{OUT1} > 3V, switching frequency may become higher than the set frequency (see the Applications Information section). The pin impedance is nominally 150kΩ.

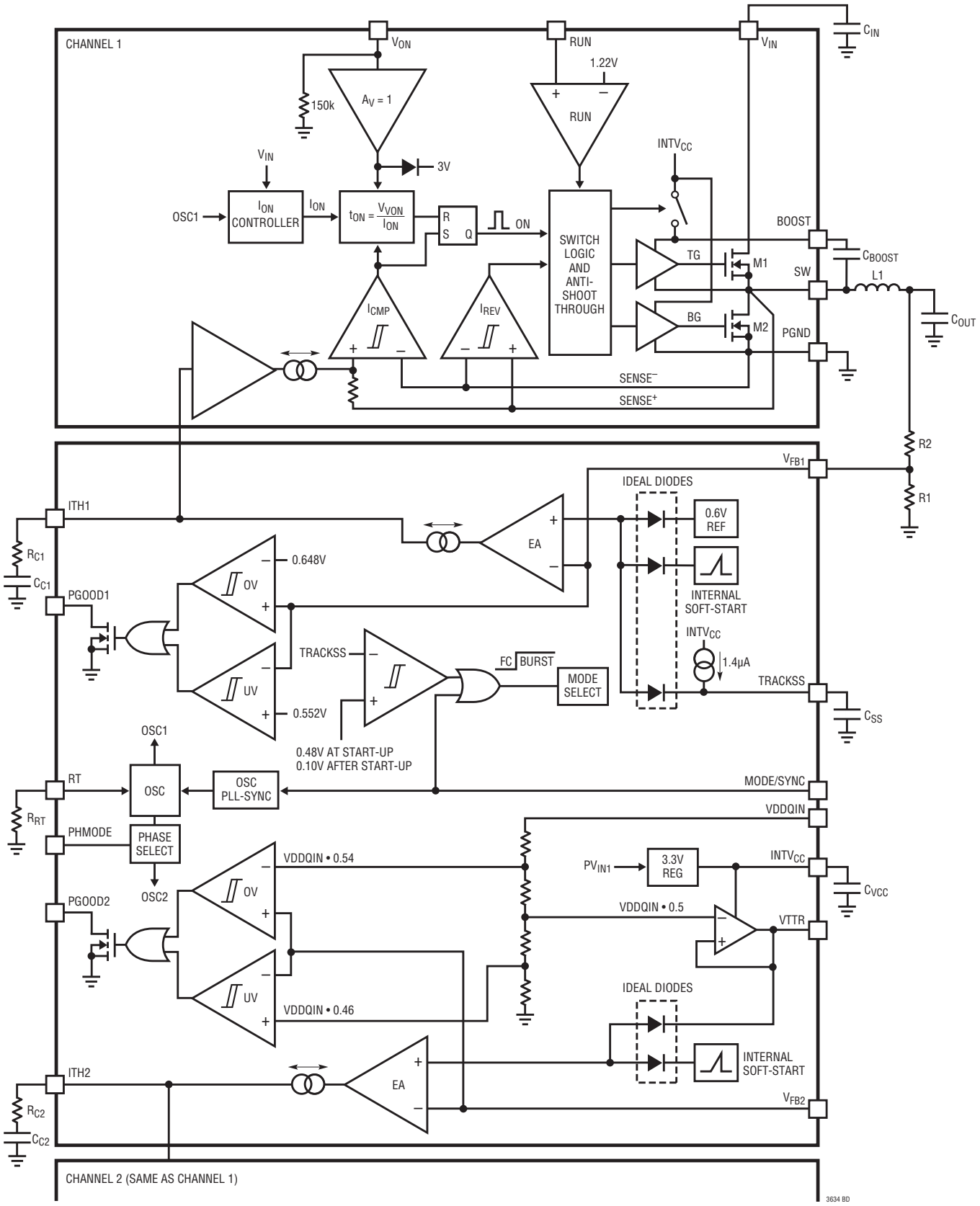
ITH1 (Pin 26/Pin 1): Channel 1 Error Amplifier Output and Switching Regulator Compensation Pin. Connect this pin to appropriate external components to compensate the regulator loop frequency response. See the Applications Information section for guidelines on component selection.

TRACKSS (Pin 27/Pin 2): Output Tracking and Soft-Start Input Pin for Channel 1. Forcing a voltage below 0.6V on this pin bypasses the internal reference input to the error amplifier. The LTC3634 will servo the FB pin to the TRACK voltage. Above 0.6V, the tracking function stops and the internal reference resumes control of the error amplifier. An internal 1.4µA pull-up current from $INTV_{CC}$ allows a soft-start function to be implemented by connecting a capacitor between this pin and SGND.

V_{FB1} (Pin 28/Pin 3): Channel 1 Output Feedback Voltage Pin. Input to the error amplifier that compares the feedback voltage to the internal 0.6V reference voltage. Connect this pin to a resistor divider network to program the desired output voltage. Connecting this pin to $INTV_{CC}$ configures the LTC3634 for 2-phase, single output operation; see the Applications Information section for full discussion.

PGND (Exposed Pad Pin 29/Exposed Pad Pin 29): Power Ground Pin. The (–) terminal of the input bypass capacitor, C_{IN}, and the (–) terminal of the output capacitor, C_{OUT}, should be tied to this pin with a low impedance connection. This pin must be soldered to the PCB to provide a low impedance electrical contact to power ground and good thermal contact to the PCB.

BLOCK DIAGRAM



OPERATION

The LTC3634 is a dual-channel, current mode monolithic step-down regulator designed to provide high efficiency power conversion for DDR memory supplies and bus termination. Its unique controlled on-time architecture allows extremely low step-down ratios while maintaining a fast, constant switching frequency. Each channel is enabled by raising the voltage on the RUN pin above 1.22V nominally.

Main Control Loop

In normal operation, the internal top power MOSFET is turned on for a fixed interval determined by a one-shot timer (ON signal in the Block Diagram). When the top power MOSFET turns off, the bottom power MOSFET turns on until the current comparator I_{CMP} trips, thus restarting the one-shot timer and initiating the next cycle. Inductor current is measured by sensing the voltage drop across the bottom power MOSFET. The voltage on the ITH pin sets the comparator threshold corresponding to inductor valley current. The error amplifier EA adjusts this ITH voltage by comparing the feedback signal V_{FB} (derived from the output voltage) to an internal 0.6V reference voltage (channel 1) or the VTTR voltage (channel 2). If the load current increases, it causes a drop in the feedback voltage relative to the reference voltage. The ITH voltage then rises until the average inductor current matches that of the load current.

The switching frequency is determined by the value of the R_T resistor, which programs the current for the internal oscillator. An internal phase-locked loop servos the one-shot timer (ON signal) such that the internal oscillator edge phase-locks to the SW node edge, thus forcing a constant switching frequency. This unique controlled on-time architecture also allows the switching frequency to be synchronized to an external clock source when it is applied to the MODE/SYNC pin. Channel 1 defaults to forced continuous operation once the clock signal is applied (channel 2 is always in forced continuous operation).

VTTR Output Buffer

The VTTR pin outputs a voltage equal to one half of VDDQIN. It is capable of sourcing/sinking 10mA and driving capacitive loads up to 0.01µF. A small series resistance (1Ω) between the output and the load further increases the amount of capacitance that the amplifier can drive. The error amplifier for channel 2 uses this voltage as its reference voltage.

High Efficiency Burst Mode Operation

At light load currents, the inductor current can drop to zero and become negative. In Burst Mode operation (available only on channel 1), a current reversal comparator (I_{REV}) detects the negative inductor current and shuts off the bottom power MOSFET, resulting in discontinuous operation and increased efficiency. Both power MOSFETs will remain off until the ITH voltage rises above the zero current level to initiate another cycle. During this time, the output capacitor supplies the load current and the part is placed into a low current sleep mode. Burst Mode operation is disabled by tying the MODE/SYNC pin to ground, which forces continuous synchronous operation regardless of output load current.

Power Good Status Output

The PGOOD open-drain output will be pulled low if the regulator output exits a ±8% window around the regulation point. This threshold has 15mV of hysteresis relative to the V_{FB} pin. To prevent unwanted PGOOD glitches during transients or dynamic V_{OUT} changes, the LTC3634 PGOOD falling edge includes a filter time of approximately 40µs. For the V_{TT} output (channel 2), VTTR is the regulation point. The PGOOD2 pin will always be low when the VTTR output voltage is less than 300mV.

V_{IN} Overvoltage Protection

In order to protect the internal power MOSFET devices against long transient voltage events, the LTC3634 constantly monitors each V_{IN} pin for an overvoltage condition. When V_{IN} rises above 17.5V, the regulator suspends operation by shutting off both power MOSFETs on the corresponding channel. Once V_{IN} drops below 16.5V, the regulator immediately resumes normal operation. The regulator does not execute its soft-start function when exiting an overvoltage condition.

Out-Of-Phase Operation

Tying the PHMODE pin high sets the SW2 falling edge to be 180° out-of-phase with the SW1 falling edge. There is

OPERATION

a significant advantage to running both channels out-of-phase. When running the channels in phase, both topside MOSFETs are on simultaneously, causing large current pulses to be drawn from the input capacitor and supply at the same time. When running the LTC3634 channels out-of-phase, the large current pulses are interleaved, effectively reducing the amount of time the pulses overlap. Thus, the total RMS input current is decreased, which both relaxes the capacitance requirements for the V_{IN} bypass capacitors and reduces the voltage noise on the supply line. One potential disadvantage to this configuration occurs when one channel is operating at 50% duty cycle. In this situation, SW node transitions can potentially couple from one channel to the other, resulting in frequency jitter on one or both channels. This effect can be mitigated with a well designed board layout. Alternatively, tying PHMODE low changes the phase difference to be 90°, which may prevent SW1 and SW2 from transitioning at the same point in time.

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A general LTC3634 application circuit is shown in Figure 1. External component selection is largely driven by the load requirement and switching frequency. Component selection typically begins with selecting the feedback resistors to set the desired output voltage. Next the inductor L and resistor R_T are selected. Once the inductor is chosen, the input capacitor (C_{IN}) and the output capacitor (C_{OUT}) can be selected. Finally, the loop compensation components may be selected to stabilize the step-down regulator. The remaining optional external components can then be selected for functions such as loop compensation, TRACKSS, V_{IN}, UVLO, and PGOOD.

Programming Switching Frequency

Selection of the switching frequency is a trade-off between efficiency and component size. High frequency operation allows the use of smaller inductor and capacitor values. Operation at lower frequencies improves efficiency by reducing internal gate charge losses but generally requires larger inductance and capacitance values to maintain low output ripple voltage. Connecting a resistor from the RT pin to SGND programs the switching frequency (f) between 500kHz and 4MHz according to the following formula:

$$R_{RT} = \frac{3.2E^{11}}{f}$$

where R_{RT} is in Ω and f is in Hz.

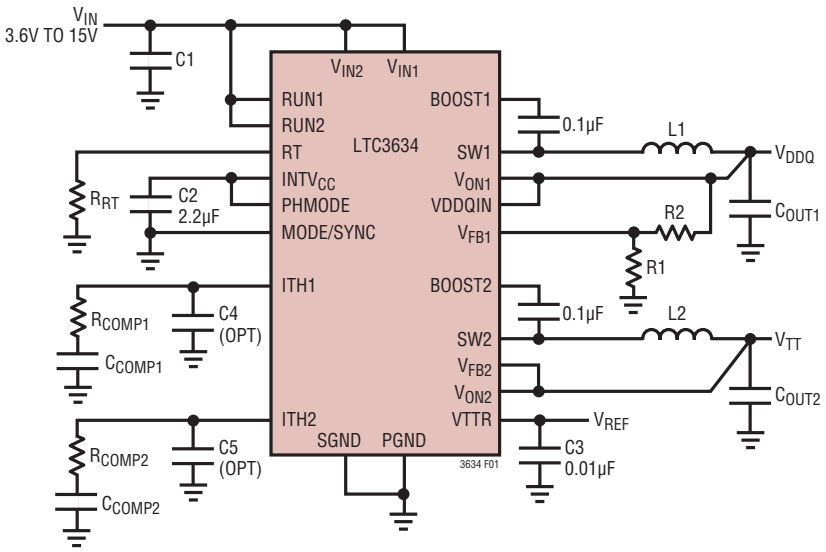

Figure 1. Typical Application Circuit for DDR Memory Supply

APPLICATIONS INFORMATION

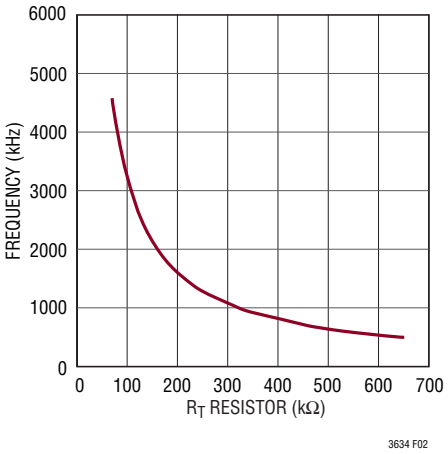

Figure 2. Switching Frequency vs R_T

When RT is tied to $INTV_{CC}$, the switching frequency will default to approximately 2MHz, as set by an internal resistor. This internal resistor is more sensitive to process and temperature variations than an external resistor (see the Typical Performance Characteristics section) and is best used for applications where switching frequency accuracy is not critical.

Output Voltage Programming

Each regulator's output voltage is set by an external resistive divider according to the following equation:

$$V_{OUT} = V_{FBREG}\left(1+\frac{R2}{R1}\right)$$

where V_{FBREG} is the reference voltage as specified in the Electrical Characteristics Table. The reference voltage is 600mV for channel 1; for channel 2 the reference voltage is equal to the VTTR pin voltage. The desired output voltage is set by appropriate selection of resistors R1 and R2 as shown in Figure 3.

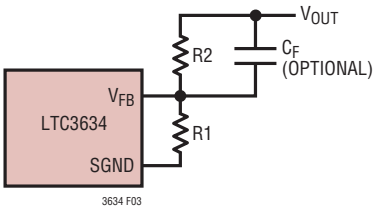

Figure 3. Setting the Output Voltage

The buffered output voltage on the VTTR pin is nominally equal to half of the VDDQIN voltage; thus configuring V_{OUT2} as a V_{TT} bus termination supply for DDR memory is as simple as shorting V_{OUT2} to V_{FB2} and connecting VDDQIN directly to the V_{OUT1} (the V_{DDQ} supply).

Choosing large values for R1 and R2 will result in improved zero-load efficiency but may lead to undesirable noise coupling or phase margin reduction due to stray capacitances at the V_{FB} node. Care should be taken to route the V_{FB} trace away from any noise source, such as the SW trace.

The LTC3634 controlled on-time architecture is optimized for an output voltage range of 0.6V to 3V, which is suitable for powering DDR memory. The LTC3634 is capable of regulating higher output voltages; however, controlled on-time behavior is not ensured. When the output voltage is greater than 3V, the step-down regulator is forced to increase the switching frequency in order to achieve output regulation. Furthermore, external clock synchronization is no longer possible, and channel 2 cannot maintain 90°/180° phase operation with respect to channel 1. In short, the LTC3634 will behave like a constant on-time regulator instead of a controlled on-time regulator. Therefore, output voltages greater than 3V should only be used in applications where switching frequency and channel-to-channel phase-locking are not critical performance characteristics.

Inductor Selection

For a given input and output voltage, the inductor value and operating frequency determine the inductor ripple current. More specifically, the inductor ripple current decreases with higher inductor value or higher operating frequency according to the following equation:

$$\Delta I_L = \left(\frac{V_{OUT}}{f \bullet L}\right)\left(1-\frac{V_{OUT}}{V_{IN}}\right)$$

where ΔI_L = inductor ripple current, f = operating frequency and L = inductor value. A trade-off between component size, efficiency and operating frequency can be seen from this equation. Accepting larger values of ΔI_L allows the use of lower value inductors but results in greater inductor

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core loss, greater ESR loss in the output capacitor, and larger output voltage ripple. Generally, highest efficiency operation is obtained at low operating frequency with small ripple current.

A reasonable starting point is to choose a ripple current somewhere between 600mA and 1.2A peak-to-peak. Note that the largest ripple current occurs at the highest V_{IN}. Exceeding 1.8A is not recommended in order to minimize output voltage ripple. To guarantee that ripple current does not exceed a specified maximum, the inductance should be chosen according to:

$$L = \left(\frac{V_{OUT}}{f \bullet \Delta I_{L(MAX)}}\right)\left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right)$$

Once the value for L is known, the type of inductor must be selected. Actual core loss is independent of core size for a fixed inductor value, but is very dependent on the inductance selected. As the inductance increases, core losses decrease. Unfortunately, increased inductance requires more turns of wire, leading to increased DCR and copper loss.

Ferrite designs exhibit very low core loss and are preferred at high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates "hard", which means that inductance collapses abruptly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current, so it is important to ensure that the core will not saturate.

Different core materials and shapes will change the size/current and price/current relationship of an inductor. Toroid or shielded pot cores in ferrite or permalloy materials are small and don't radiate much energy, but generally cost more than powdered iron core inductors with similar characteristics. The choice of which style inductor to use mainly depends on the price versus size requirements and any radiated field/EMI requirements. Table 1 gives a sampling of available surface mount inductors.

Table 1. Inductor Selection Table

INDUCTANCE (µH)	DCR (mΩ)	MAX CURRENT (A)	DIMENSIONS (mm)	HEIGHT (mm)
Würth Electronik WE-HC 744310 Series				
0.24	2.1	18.0	7 × 7	3.3
0.55	3.8	14.0		
0.95	6.4	11.0		
1.15	9.0	8.5		
2.00	14.0	6.5		
Vishay IHLP-2020BZ-01 Series				
0.22	5.2	15	5.2 × 5.5	2
0.33	8.2	12		
0.47	8.8	11.5		
0.68	12.4	10		
1	20	7		
Toko FDV0620 Series				
0.20	4.5	12.4	7 × 7.7	2.0
0.47	8.3	9.0		
1.0	18.3	5.7		
Coilcraft D01813H Series				
0.33	4	10	6 × 8.9	5.0
0.56	10	7.7		
1.2	17	5.3		
TDK RLF7030 Series				
1.0	8.8	6.4	6.9 × 7.3	3.2
1.5	9.6	6.1		

C_{IN} and C_{OUT} Selection

The input capacitance, C_{IN}, is needed to filter the trapezoidal wave current at the drain of the top power MOSFET. To prevent large voltage transients from occurring, a low ESR input capacitor sized for the maximum RMS current is recommended. The maximum RMS current for a single regulator is given by:

$$I_{RMS} = I_{OUT(MAX)} \frac{\sqrt{V_{OUT}\left(V_{IN} - V_{OUT}\right)}}{V_{IN}}$$

When both regulators are active, the input current waveform is significantly different. Furthermore, the input RMS current varies depending on each output's load current as well as whether V_{TT} is sinking or sourcing current.

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When SW1 and SW2 operate 180° out-of-phase, the worst-case input RMS current occurs when the V_{TT} supply is sinking current and V_{DDQ} is sourcing the same amount of current. Knowing that V_{OUT2} = one-half V_{OUT1} in the DDR application, the input RMS current in this case is given by:

$$I_{RMS} = I_{OUT(MAX)}\sqrt{D1\left(1.5-\frac{D1}{4}\right)} \text{ for } D1 < 0.5$$

$$I_{RMS} = I_{OUT(MAX)}\sqrt{1-\frac{3}{4}D1} \text{ for } D1 > 0.5$$

where D1 is the duty cycle of channel 1 (V_{DDQ} supply). These equations show that maximum I_{RMS} occurs at 50% duty cycle ($V_{IN} = 2 \bullet V_{OUT1}$). This simple worst-case condition may be used for design as deviations in duty cycle do not offer significant relief. Note that ripple current ratings from capacitor manufacturers are often based on only 2000 hours of life which makes it advisable to further derate the capacitor, or choose a capacitor rated at a higher temperature than required.

Several capacitors may also be paralleled to meet size or height requirements in the design. For low input voltage applications, sufficient bulk input capacitance is needed to minimize transient effects during output load changes. Even though the LTC3634 design includes an overvoltage protection circuit, care must always be taken to ensure input voltage transients do not pose an overvoltage hazard to the part.

The selection of C_{OUT} is determined by the effective series resistance (ESR) that is required to minimize voltage ripple and load step transients as well as the amount of bulk capacitance that is necessary to ensure that the control loop is stable. Loop stability can be checked by viewing the load transient response. The output ripple, ΔV_{OUT}, is approximated by:

$$\Delta V_{OUT} < \Delta I_L\left(ESR+\frac{1}{8 \bullet f \bullet C_{OUT}}\right)$$

When using low-ESR ceramic capacitors, it is more useful to choose the output capacitor value to fulfill a charge storage requirement. During a load step, the output capacitor must instantaneously supply the current to support the load until the feedback loop raises the switch current enough to support the load. The time required for the feedback loop to respond is dependent on the compensation and the output capacitor size. Typically, three to four cycles are required to respond to a load step, but only in the first cycle does the output drop linearly. The output droop, V_{DROOP}, is usually about three times the linear drop of the first cycle, provided the loop crossover frequency is maximized. Thus, a good place to start is with the output capacitor size of approximately:

$$C_{OUT} \approx \frac{3 \bullet \Delta I_{OUT}}{f \bullet V_{DROOP}}$$

Though this equation provides a good approximation, more capacitance may be required depending on the duty cycle and load step requirements. The actual V_{DROOP} should be verified by applying a load step to the output.

Using Ceramic Input and Output Capacitors

Higher values, lower cost ceramic capacitors are available in small case sizes. Their high ripple current, high voltage rating and low ESR make them ideal for switching regulator applications. However, due to the self-resonant and high-Q characteristics of some types of ceramic capacitors, care must be taken when these capacitors are used at the input. When a ceramic capacitor is used at the input and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the V_{IN} input. At best, this ringing can couple to the output and be mistaken as loop instability. At worst, a sudden inrush of current through the long wires can potentially cause a voltage spike at V_{IN} large enough to damage the part. For a more detailed discussion, refer to Application Note 88.

When choosing the input and output ceramic capacitors, choose the X5R and X7R dielectric formulations. These dielectrics have the best temperature and voltage characteristics of all the ceramics for a given value and size.

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Choosing Compensation Components

Loop compensation is a complicated subject and Application Note 76 is recommended reading for a full discussion on maximizing loop bandwidth in a current mode switching regulator. This section will provide a quick method on choosing proper components to compensate the LTC3634 regulators.

Figure 4 shows the recommended components to be connected to the ITH pin, and Figure 5 shows an approximate bode plot of the buck regulator loop using these components. It is assumed that the major poles in the system (the output capacitor pole and the error amplifier output pole) are located at a frequency lower than the crossover frequency.

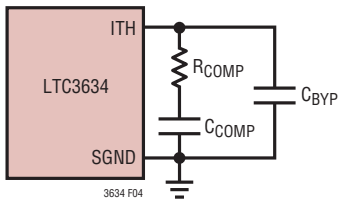

Figure 4. Compensation and Filtering Components

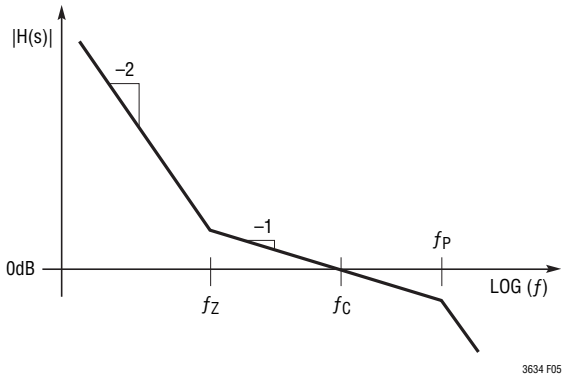

Figure 5. Bode Plot of Regulator Loop

The first step is to choose the crossover frequency f_C. Higher crossover frequencies will result in a faster loop transient response; however, in order to avoid higher order loop dynamics from the switching power stage, it is recommended that f_C not exceed one-tenth the switching frequency (f_{SW}).

Once f_C is chosen, the value of R_{COMP} that sets this crossover frequency can be calculated by the following equation:

$$R_{COMP} = \left(\frac{2\pi \bullet f_C \bullet C_{OUT}}{g_{m(EA)} \bullet g_{m(MOD)}}\right)\left(\frac{V_{OUT}}{V_{FBREG}}\right)$$

where $g_{m(EA)}$ is the error amplifier transconductance (see the Electrical Characteristics section), and $g_{m(MOD)}$ is the modulator transconductance (the transfer function from ITH voltage to current comparator threshold). For the LTC3634, this transconductance is nominally $7\Omega^{-1}$.

Once R_{COMP} is determined, C_{COMP} can be chosen to set the zero frequency (f_Z):

$$f_Z = \frac{1}{2\pi \bullet C_{COMP} \bullet R_{COMP}}$$

For 90° of phase margin, f_Z should be chosen to be less than one-tenth of f_C.

Since the ITH node is sensitive to noise coupling, a small bypass capacitor (C_{BYP}) may be used to filter out board noise. However, this cap contributes a pole at f_P and may introduce some phase loss at the crossover frequency:

$$f_P = \frac{1}{2\pi \bullet C_{BYP} \bullet R_{COMP}}$$

For best results, f_P should be set high enough such that phase margin is not significantly affected.

If necessary, a capacitor C_F (as shown in Figure 3) may be used to add some phase lead.

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Checking Transient Response

The regulator loop response can be checked by observing the response of the system to a load step. The ITH pin not only allows optimization of the control loop behavior but also provides a DC-coupled and AC filtered closed loop response test point. The DC step, rise time, and settling behavior at this test point reflect the closed loop response. Assuming a predominantly second order system, phase margin and/or damping factor can be estimated using the percentage of overshoot seen at this pin.

After choosing compensation values as discussed in the previous section, the design should be tested to verify stability. The component values may be modified slightly to optimize transient response once the final PC layout is done and the particular output capacitor type and value have been determined. The output capacitors need to be selected because their various types and values determine the loop gain and phase. An output current pulse of 20% to 100% of full load current having a rise time of ~1µs will produce output voltage and ITH pin waveforms that will give a sense of the overall loop stability without breaking the feedback loop.

Switching regulators take several cycles to respond to a step in load current. When a load step occurs, V_{OUT} immediately shifts by an amount equal to $\Delta I_{LOAD} \bullet ESR$, where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT}, generating a feedback error signal used by the regulator to return V_{OUT} to its steady-state value. During this recovery time, V_{OUT} can be monitored for overshoot or ringing that would indicate a stability problem.

When observing the response of V_{OUT} to a load step, the initial output voltage step may not be within the bandwidth of the feedback loop, so the standard second order overshoot/DC ratio cannot be used to determine phase margin. The output voltage settling behavior is related to the stability of the closed-loop system and will demonstrate the actual overall supply performance. For a detailed explanation of optimizing the compensation components, including a review of control loop theory, refer to Application Note 76.

In some applications, a more severe transient can be caused by switching in loads with large (>10µF) input capacitors. The discharged input capacitors are effectively put in parallel with C_{OUT}, causing a rapid drop in V_{OUT}. No regulator can deliver enough current to prevent this problem, if the switch connecting the load has low resistance and is driven quickly. The solution is to limit the turn-on speed of the load switch driver. A Hot Swap™ controller is designed specifically for this purpose and usually incorporates current limiting, short-circuit protection, and soft-starting.

$INTV_{CC}$ Regulator Bypass Capacitor

An internal low dropout (LDO) regulator produces the 3.3V supply that powers the internal bias circuitry and drives the gate of the internal MOSFET switches. The $INTV_{CC}$ pin connects to the output of this regulator and must have a minimum of 1µF ceramic bypass capacitance to ground. This capacitor should have low impedance electrical connections to the $INTV_{CC}$ and PGND pins to provide the transient currents required by the LTC3634. This supply is intended only to supply additional DC load currents as desired and not intended to regulate large transient or AC behavior, as this may impact LTC3634 operation.

Boost Capacitor

The LTC3634 uses a bootstrap circuit to create a voltage rail above the applied input voltage V_{IN}. Specifically, a boost capacitor, C_{BOOST}, is charged to a voltage approximately equal to $INTV_{CC}$ each time the bottom power MOSFET is turned on. The charge on this capacitor is then used to supply the required transient current during the remainder of the switching cycle. When the top MOSFET is turned on, the BOOST pin voltage will be equal to approximately V_{IN} + 3.3V. For most applications, a 0.1µF ceramic capacitor closely connected between the BOOST and SW pins will provide adequate performance.

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Minimum Off-Time/On-Time Considerations

The minimum off-time is the smallest amount of time that the LTC3634 can turn on the bottom power MOSFET, trip the current comparator and turn the power MOSFET back off. This time is typically 40ns. For the controlled on-time control architecture, the minimum off-time limit imposes a maximum duty cycle of:

$$DC_{MAX} = 1 - f \bullet (t_{OFF(MIN)} + 2 \bullet t_{DEAD})$$

where f is the switching frequency, t_{DEAD} is the nonoverlap time of the switches, or dead time (typically 15ns), and $t_{OFF(MIN)}$ is the minimum off-time. If the maximum duty cycle is surpassed, due to a decreasing input voltage for example, the output will drop out of regulation. The minimum input voltage to avoid this dropout condition is:

$$V_{IN(MIN)} = \frac{V_{OUT}}{1 - f \bullet \left(t_{OFF(MIN)} + 2 \bullet t_{DEAD}\right)}$$

Conversely, the minimum on-time is the smallest duration of time in which the top power MOSFET can be in its ON state. This time is typically 20ns. In continuous mode operation, the minimum on-time limit imposes a minimum duty cycle of:

$$DC_{MIN} = (f \bullet t_{ON(MIN)})$$

where $t_{ON(MIN)}$ is the minimum on-time. As the equation shows, reducing the operating frequency will alleviate the minimum duty cycle constraint.

When the regulator output is sinking current, the effective minimum on-time of the converter will be increased by the non-overlap time of the power MOSFETs (or the "dead-time") during each SW node transition. This "dead-time" is nominally 15ns, so when sinking current, the minimum on-time is effectively 15ns + 15ns + 20ns = 50ns.

If the minimum on-time constraint is violated, the converter will automatically reduce its own switching frequency in order to maintain output regulation. Once the converter reduces its switching frequency, the phase information is lost and the two channels will switch asynchronously.

Furthermore, the regulator may need to be compensated more conservatively due to the lower switching frequency.

MODE/SYNC Operation

The MODE/SYNC pin is a multipurpose pin allowing both mode selection and operating frequency synchronization. Floating this pin or connecting it to $INTV_{CC}$ enables Burst Mode operation on channel 1 for superior efficiency at light load currents at the expense of slightly higher output voltage ripple. When the MODE/SYNC pin is tied to ground, forced continuous mode operation is selected, creating the lowest fixed output ripple at the expense of light load efficiency.

The LTC3634 will detect the presence of the external clock signal on the MODE/SYNC pin and synchronize the internal oscillator to the phase and frequency of the incoming clock. The presence of an external clock will place both regulators into forced continuous mode operation. Although the R_T resistor is not strictly necessary when synchronizing to an external clock, it is recommended to use a R_T resistor that matches the nominal external clock frequency in order to keep the switching regulator biased correctly whenever the external clock signal is suddenly removed or reapplied.

Channel 1 Output Voltage Tracking and Soft-Start

The LTC3634 allows the user to control the output voltage ramp rate of channel 1 by means of the TRACKSS pin. From 0 to 0.6V, the TRACKSS voltage will override the internal 0.6V reference input to the error amplifier, thus regulating the feedback voltage to that of the TRACKSS pin. When TRACKSS is above 0.6V, tracking is disabled and the feedback voltage will regulate to the internal reference voltage.

The voltage at the TRACKSS pin may be driven from an external source, or alternatively, the user may leverage the internal 1.4µA pull-up current source to implement a soft-start function by connecting an external capacitor (C_{SS}) from the TRACKSS pin to ground. The relationship between output rise time and TRACKSS capacitance is given by:

$$t_{SS} = 430000\Omega \bullet C_{SS}$$

APPLICATIONS INFORMATION

A default internal soft-start ramp forces a minimum soft-start time of 400µs by overriding the TRACKSS pin input during this time period. Hence, capacitance values less than approximately 1000pF will not significantly affect soft-start behavior.

Start-Up Behavior

Upon start-up, both channels immediately default to discontinuous operation. Channel 1 will remain in discontinuous Burst Mode operation until its output rises to greater than 80% of its final value (V_{FB} > 480mV). Once the output exceeds this voltage, the operating mode of the regulator switches to the mode selected by the MODE/SYNC pin as described above. During normal operation, if the output drops below 10% of its final value (as it may when tracking down, for instance), the regulator will automatically switch to Burst Mode operation to prevent inductor saturation and improve TRACKSS pin accuracy.

Channel 2 (the V_{TT} termination supply) remains in discontinuous operation until its output rises above 300mV, at which point it will automatically switch to forced continuous operation. This ensures that the regulator output has sufficient voltage to discharge the inductor in continuous mode and prevent excessive build-up of energy in the inductor.

Output Power Good

The PGOOD output of the LTC3634 is driven by a 15Ω (typical) open-drain pull-down device. If the output voltage exits an 8% (typical) regulation window around the target regulation point, the open-drain output will pull down with 15Ω output resistance to ground, thus dropping the PGOOD pin voltage. This pull-down device will not shut off until the output re-enters this window and overcomes a small amount of hysteresis. This behavior is described in Figure 6.

A filter time of 40µs (typical) acts to prevent unwanted PGOOD output changes during V_{OUT} transient events. As a result, the output voltage must exit the 8% regulation window for 40µs before the PGOOD pin pulls to ground. Conversely, the output voltage must be within the target regulation window for 40µs before the PGOOD pin pulls high.

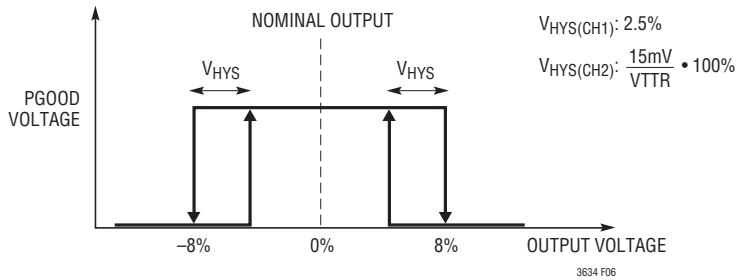

Figure 6. PGOOD Pin Behavior

APPLICATIONS INFORMATION

2-Phase, Single V_{TT} Output Configuration

The two regulators on the LTC3634 can be easily combined to provide a single 2-phase V_{TT} termination supply capable of sourcing and sinking up to 6A. The circuit is shown in Figure 7.

In this circuit, V_{FB1} is tied to $INTV_{CC}$ to put the LTC3634 into 2-phase operation. When set up for 2-phase operation, the inputs to channel 1's transconductance error amplifier are switched to be the same as channel 2's inputs (V_{FB2} and VTTR), allowing it to be paralleled with channel 2's error amplifier. The ITH1 and ITH2 pins should be tied together externally to force equal current sharing between both channels.

Only one compensation network is needed on the ITH node, although separate filter caps for each ITH pin may be helpful depending on the board layout. In this parallel configuration, it is important to note that the effective $g_{m(EA)}$ and $g_{m(MOD)}$ are twice as large as that of a single channel.

One advantage to this 2-phase configuration is that both input and output current ripple is significantly reduced compared to a single phase 6A converter solution, because the current waveforms from each regulator are interleaved. Refer to Application Note 77 for a full discussion and analysis on PolyPhase® converters.

V_{IN1} and V_{IN2} may be powered from separate supply voltages (see Figure 12). This is useful in cases where power needs to be shared between two different sources. It is important to note that when the V_{TT} output sinks current, it will backfeed through the converter and out of the V_{IN} pins. Care must be taken to ensure that the input supplies are able to handle this condition.

Efficiency Considerations

The percent efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Percent efficiency can be expressed as:

$$\% \text{ Efficiency} = 100\% - (L1 + L2 + L3 + \ldots)$$

where L1, L2, etc. are the individual losses as a percentage of input power. Although all dissipative elements in the circuit produce losses, three main sources usually account for most of the losses in LTC3634 circuits: 1) conduction losses, 2) switching losses and quiescent power loss 3) transition losses and other losses.

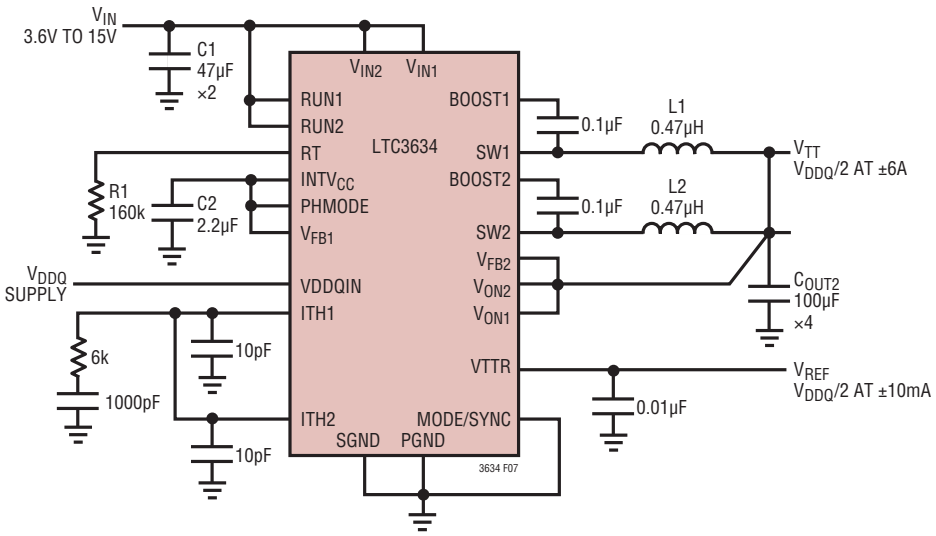

Figure 7. Application Circuit for a 2-Phase, ±6A Single V_{TT} Output

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1. Conduction losses are calculated from the DC resistances of the internal switches, R_{SW}, and external inductor, R_L. In continuous mode, the average output current flows through inductor L but is "chopped" between the internal top and bottom power MOSFETs. Thus, the series resistance looking into the SW pin is a function of both top and bottom MOSFET $R_{DS(ON)}$ and the duty cycle (DC) as follows:

   $$R_{SW} = (R_{DS(ON)TOP})(DC) + (R_{DS(ON)BOT})(1 – DC)$$

   The $R_{DS(ON)}$ for both the top and bottom MOSFETs can be obtained from the Typical Performance Characteristics curves. So to calculate conduction losses:

   $$\text{Conduction Loss} = I_{OUT}^2 (R_{SW} + R_L)$$

2. The internal LDO supplies the power to the $INTV_{CC}$ rail. The total power loss here is the sum of the switching losses and quiescent current losses from the control circuitry.

   Each time a power MOSFET gate is switched from low to high to low again, a packet of charge dQ moves from V_{IN} to ground. The resulting dQ/dt is a current out of $INTV_{CC}$ that is typically much larger than the DC control bias current. In continuous mode, $I_{GATECHG} = f \bullet (Q_T + Q_B)$, where Q_T and Q_B are the gate charges of the internal top and bottom power MOSFETs and f is the switching frequency. For estimation purposes, $(Q_T + Q_B)$ on each LTC3634 regulator channel is approximately 2.3nC.

   To calculate the total power loss from the LDO load, simply add the gate charge current and quiescent current and multiply by V_{IN}:

   $$P_{LDO} = (I_{GATECHG} + I_Q) \bullet V_{IN}$$

3. Other hidden losses such as transition loss, copper trace resistances, and internal load currents can account for additional efficiency degradations in the overall power system. Transition loss arises from the brief amount of time the top power MOSFET spends in the saturated region during switch node transitions. The LTC3634 internal power devices switch quickly enough that these losses are not significant compared to other sources. Other losses, including diode conduction losses during dead-time and inductor core losses, generally account for less than 2% total additional loss.

Thermal Considerations

The LTC3634 requires the exposed package back-plane metal (PGND) to be well soldered to the PC board to provide good thermal contact. This gives the QFN and TSSOP packages exceptional thermal properties, which are necessary to prevent excessive self-heating of the part in normal operation.

In a majority of applications, the LTC3634 does not dissipate much heat due to its high efficiency and low thermal resistance of its exposed-back QFN package. However, in applications where the LTC3634 is running at high ambient temperature, high V_{IN}, high switching frequency, and maximum output current load, the heat dissipated may exceed the maximum junction temperature of the part. If the junction temperature reaches approximately 170°C, both power switches will be turned off until the temperature returns to 160°C.

To prevent the LTC3634 from exceeding the maximum junction temperature of 125°C, the user will need to do some thermal analysis. The goal of the thermal analysis is to determine whether the power dissipated exceeds the maximum junction temperature of the part. The temperature rise is given by:

$$T_{RISE} = P_D \bullet \theta_{JA}$$

As an example, consider the case when the LTC3634 is used to power DDR2 SDRAM and is used in an application where maximum ambient temperature is 70°C, V_{IN} = 12V, frequency = 1MHz, V_{DDQ} = 1.8V, V_{TT} = 0.9V, and I_{LOAD} = 2A for both channels.

From the $R_{DS(ON)}$ graphs in the Typical Performance Characteristics section, the top switch on-resistance is nominally 140mΩ and the bottom switch on-resistance is nominally 75mΩ at 70°C ambient. For the V_{DDQ} supply, the equivalent power MOSFET resistance R_{SW1} is:

$$R_{DS(ON)TOP} \bullet \frac{1.8V}{12V} + R_{DS(ON)BOT} \bullet \frac{10.2V}{12V} = 84.8m\Omega$$

The same calculation to the V_{TT} supply (0.9V), yields R_{SW2} = 79.9mΩ.

From the previous section's discussion on gate drive, we estimate the total gate charge current for each regulator to

APPLICATIONS INFORMATION

be 1MHz • 2.3nC = 2.3mA, and the total I_Q of both channels is 1.3mA (see the Electrical Characteristics section). Therefore, the total power dissipated by both regulators is:

$$P_D = \left[(I_{OUT1})^2 \bullet R_{SW1}\right] + \left[(I_{OUT2})^2 \bullet R_{SW2}\right] + V_{IN} \bullet (I_{GATECHG} + I_Q)$$

$$P_D = (2A)^2 \bullet 0.0848\Omega + (2A)^2 \bullet 0.0799\Omega + 12V \bullet \left[(2.3mA \bullet 2) + 1.3mA\right] = 0.730W$$

The QFN 4mm × 5mm package junction-to-ambient thermal resistance, θ_{JA}, is around 43°C/W. Therefore, the junction temperature of the regulator operating in a 70°C ambient temperature is approximately:

T_J = 0.730W • 43°C/W + 70°C = 101°C

which is below the maximum junction temperature of 125°C. With higher ambient temperatures, a heat sink or cooling fan should be considered to drop the junction-to-ambient thermal resistance. Alternatively, the exposed pad TSSOP package may be a better choice for high power applications, since it has better thermal properties than the QFN package.

Remembering that the above junction temperature is obtained from a $R_{DS(ON)}$ at 70°C, we might recalculate the junction temperature based on a higher $R_{DS(ON)}$ since it increases with temperature. Redoing the calculation assuming that R_{SW} increased 12% at 101°C yields a new junction temperature of 105°C.

Figure 8 is a temperature derating curve based on the DC1708 demo board (QFN package). It can be used as a guideline to estimate the maximum allowable ambient temperature for given DC load currents in order to avoid exceeding the maximum operating junction temperature of 125°C.

Junction Temperature Measurement

The junction-to-ambient thermal resistance will vary depending on the size and amount of heat sinking copper on the PCB board where the part is mounted, as well as the amount of air flow on the device. In order to properly evaluate this thermal resistance, the junction temperature needs to be measured. A clever way to measure the junction temperature directly is to use the internal junction diode on one of the PGOOD pins to measure its diode voltage change based on ambient temperature change.

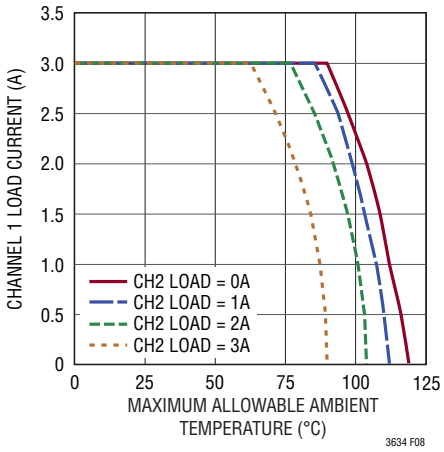

Figure 8. Temperature Derating Curve for DC1708 Demo Circuit

First remove any external passive component on the PGOOD pin, then pull out 100µA from the PGOOD pin to turn on its internal junction diode and bias the PGOOD pin to a negative voltage. With no output current load, measure the PGOOD voltage at an ambient temperature of 25°C, 75°C and 125°C to establish a slope relationship between the voltage on PGOOD and ambient temperature. Once this slope is established, then the junction temperature rise can be measured as a function of power loss in the package with corresponding output load current. Although making this measurement with this method does violate absolute maximum voltage ratings on the PGOOD pin, the applied power is so low that there should be no significant risk of damaging the device.

Board Layout Considerations

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the LTC3634. Check the following in your layout:

1. Do the input capacitors connect to the V_{IN} and PGND pins as close as possible? These capacitors provide the AC current to the internal power MOSFETs and their drivers.
2. The output capacitor, C_{OUT}, and inductor L should be closely connected to minimize loss. The (–) plate of

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C_{OUT} should be closely connected to both PGND and the (–) plate of C_{IN}.

3. The resistive divider, (e.g. R1 and R2 in Figure 1) must be connected between the (+) plate of C_{OUT} and a ground line terminated near SGND. The feedback signal V_{FB} should be routed away from noisy components and traces, such as the SW line, and its trace length should be minimized. In addition, the R_T resistor and loop compensation components should be terminated to SGND.
4. Keep sensitive components away from the SW pin. The R_T resistor, the compensation components, the feedback resistors, and the $INTV_{CC}$ bypass capacitor should all be routed away from the SW trace and the inductor L.
5. A ground plane is preferred, but if not available, the signal and power grounds should be segregated with both connecting to a common, low noise reference point. The connection to the PGND pin should be made with a minimal resistance trace from the reference point.
6. Flood all unused areas on all layers with copper in order to reduce the temperature rise of power components. These copper areas should be connected to the exposed backside of the package (PGND). Refer to Figures 10 and 11 for board layout examples.

Design Example

As a design example, consider using the LTC3634 (as shown in Figure 1) to power DDR2 SDRAM with the following specifications: $V_{IN(MAX)}$ = 13.2V, $I_{OUT(MAX)}$ = ±2A, f = 1MHz, $V_{DROOP(VDDQ)}$ < 60mV, $V_{DROOP(VTT)}$ < 30mV. The following discussion will use equations from the previous sections.

First, the correct R_T resistor value for 1MHz switching frequency must be chosen. Based on previous discussions, R_T is calculated to be

$$R_T = \left(\frac{3.2E^{11}}{f}\right) = 320k\Omega$$

The closest standard value is 324k.

Next, select values for R1 and R2 to set channel 1 (V_{DDQ}) to be 1.8V for DDR2 SDRAM. Choosing R1 to be 12.1k, R2 is calculated to be:

$$R2 = 12.1k \bullet \left(\frac{1.8V}{0.6V} - 1\right) = 24.2k$$

The closest standard value is 24.3k. Tying VDDQIN to V_{OUT1} sets V_{OUT2} to be half of V_{OUT1}.

Next, we can pick inductor values for both the V_{DDQ} and V_{TT} outputs. Choosing inductor current ripple to be 1A at maximum V_{IN}:

$$L1 = \left(\frac{1.8V}{1MHz \bullet 1A}\right)\left(1 - \frac{1.8V}{13.2V}\right) = 1.55\mu H$$

$$L2 = \left(\frac{0.9V}{1MHz \bullet 1A}\right)\left(1 - \frac{0.9V}{13.2V}\right) = 0.838\mu H$$

Standard values of 1.5µH and 0.82µH should be used.

Ceramic caps will be used for C_{OUT} and will be selected based on the charge storage requirement. Assuming a worst case 4A load step (–2A to 2A):

$$C_{OUT1} \approx \frac{3 \bullet 4A}{1MHz \bullet 60mV} = 200\mu F$$

$$C_{OUT2} \approx \frac{3 \bullet 4A}{1MHz \bullet 30mV} = 400\mu F$$

Lastly, we will choose compensation components. Choosing the crossover frequency f_C = 50kHz:

$$R_{COMP1} = \left(\frac{2\pi \bullet 50kHz \bullet 200\mu F}{1m\Omega^{-1} \bullet 7\Omega^{-1}}\right)\left(\frac{1.8V}{0.6V}\right) = 27k\Omega$$

$$R_{COMP2} = \left(\frac{2\pi \bullet 50kHz \bullet 400\mu F}{1m\Omega^{-1} \bullet 7\Omega^{-1}}\right)\left(\frac{0.9V}{0.9V}\right) = 18k\Omega$$

Choosing the zero frequency to be 10kHz yields C_{COMP1} = 589pF and C_{COMP2} = 884pF. The closest standard values for the compensation components are 26.7k, 18k, 560pF and 910pF, respectively.

The final circuit is shown in Figure 9.

APPLICATIONS INFORMATION

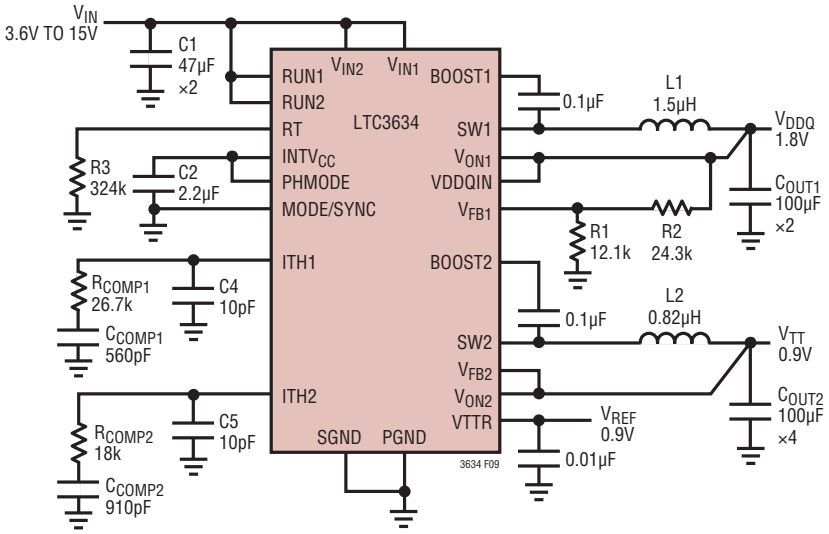


Figure 9. Design Example Circuit

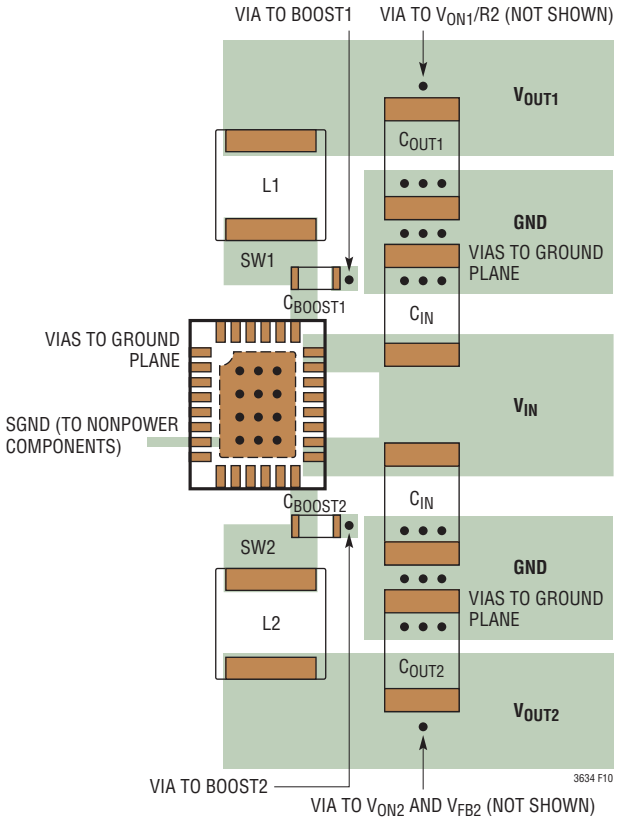


Figure 10. Example of Power Component Layout for QFN Package

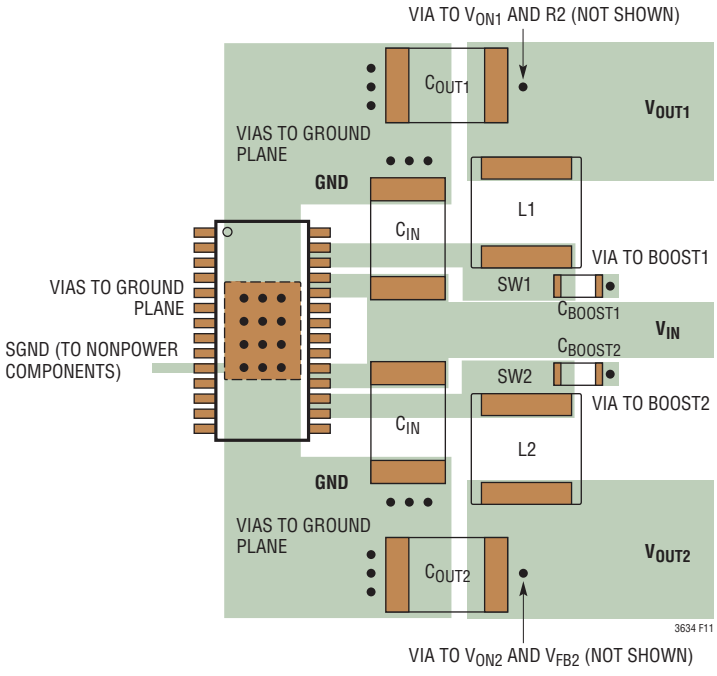
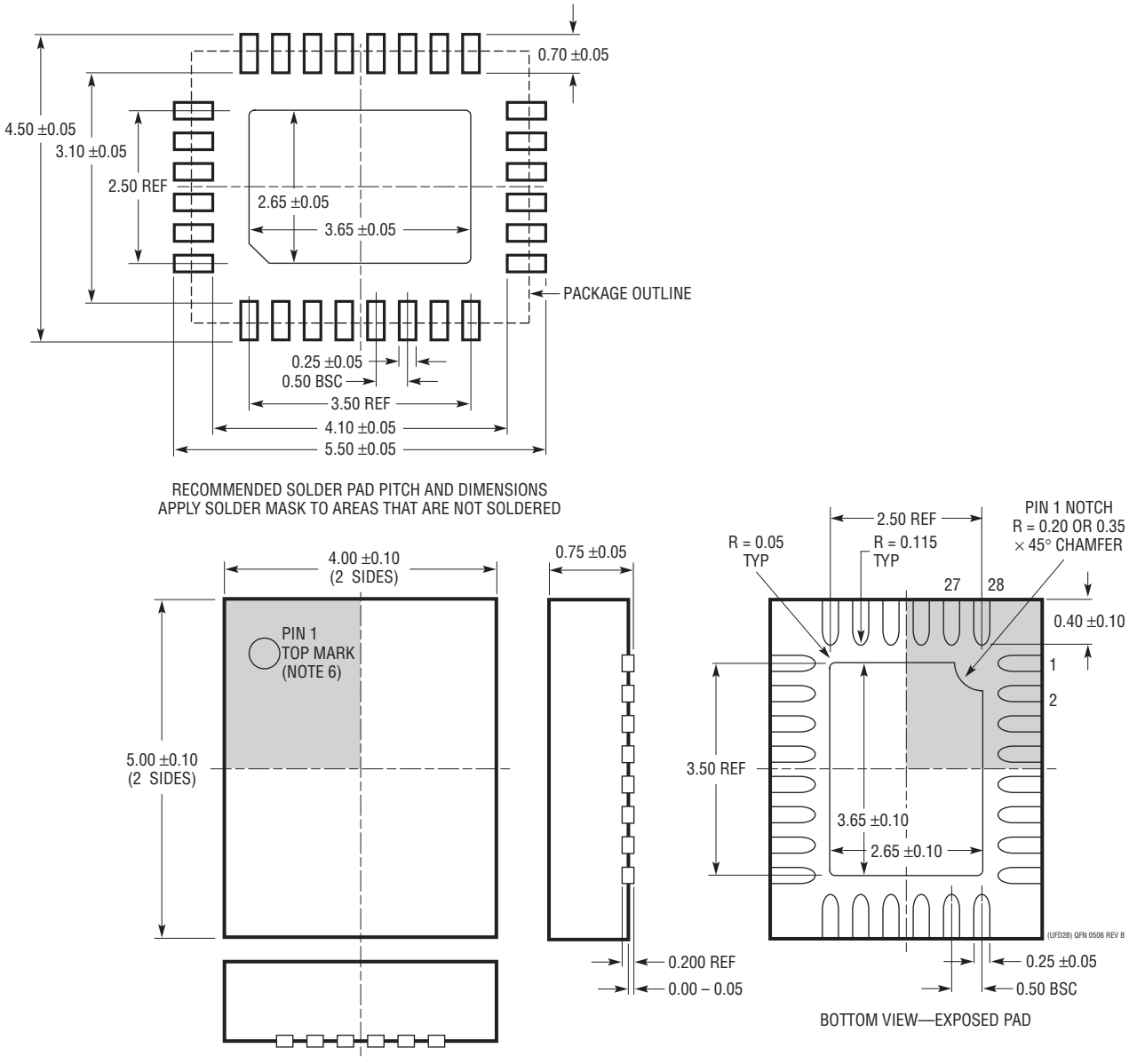


Figure 11. Example of Power Component Layout for TSSOP Package

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LTC3634#packaging for the most recent package drawings.

UFD Package
28-Lead Plastic QFN (4mm × 5mm)
(Reference LTC DWG # 05-08-1712 Rev B)

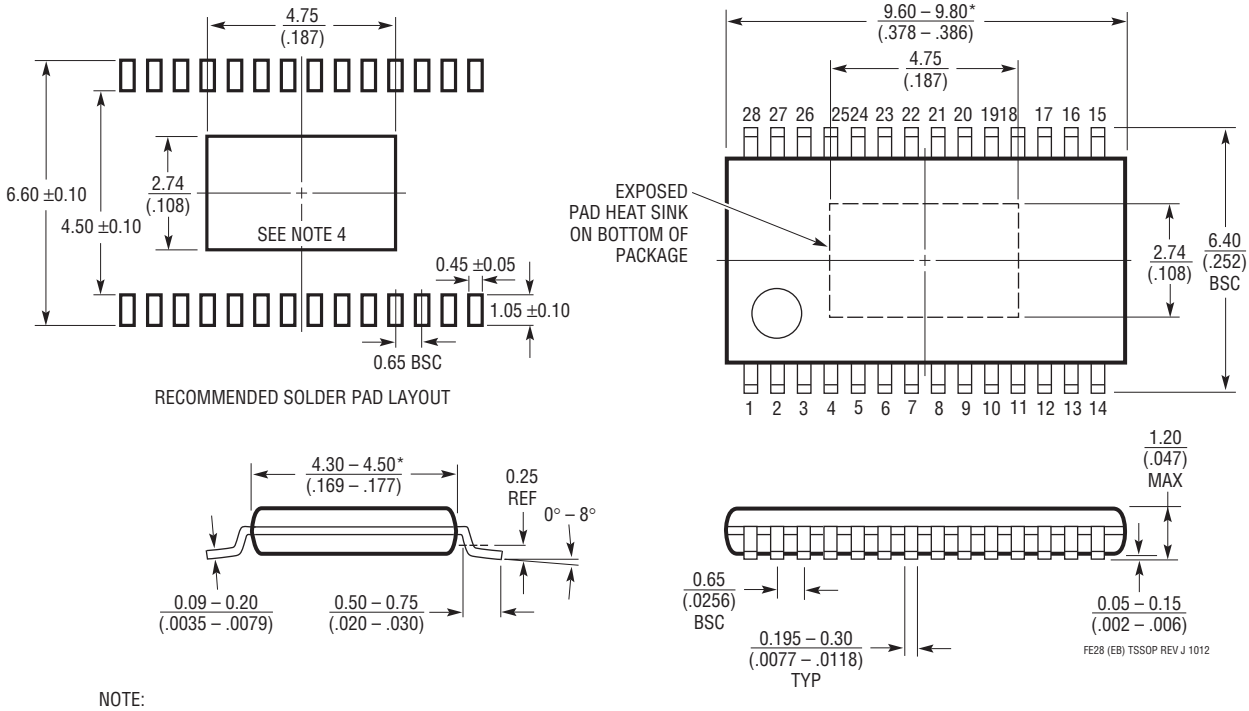


NOTE:
1. DRAWING PROPOSED TO BE MADE A JEDEC PACKAGE OUTLINE MO-220 VARIATION (WXXX-X).
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LTC3634#packaging for the most recent package drawings.

FE Package
28-Lead Plastic TSSOP (4.4mm)
(Reference LTC DWG # 05-08-1663 Rev J)
Exposed Pad Variation EB



NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN MILLIMETERS (INCHES)
3. DRAWING NOT TO SCALE
4. RECOMMENDED MINIMUM PCB METAL SIZE FOR EXPOSED PAD ATTACHMENT
*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.150mm (.006") PER SIDE

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	09/13	Clarified Absolute Maximum Ratings, added H and MP grades to Order Information.	2
		Clarified parametric data.	3, 4
		Clarified graphs.	5, 6
		Clarified RUN1, RUN2 pin function, $INTV_{CC}$.	7, 8
		Clarified minimum on-time description.	18
		Clarified maximum junction temperature in Thermal Considerations.	21
		Clarified Related Parts, added LTC3786 and LTC3633A.	28
B	12/13	Clarified dead-time from 10ns to 15ns.	18
C	01/16	Added package option for mini reels Expanded VTTR pin description Expanded description in VTTR Output Buffer	2 9 11

LINEAR TECHNOLOGY

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

TYPICAL APPLICATION

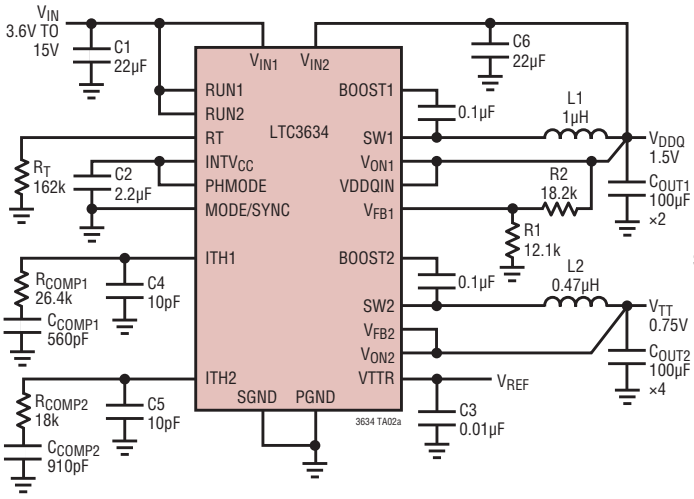


Figure 12a. V_{TT} Powered from V_{DDQ}

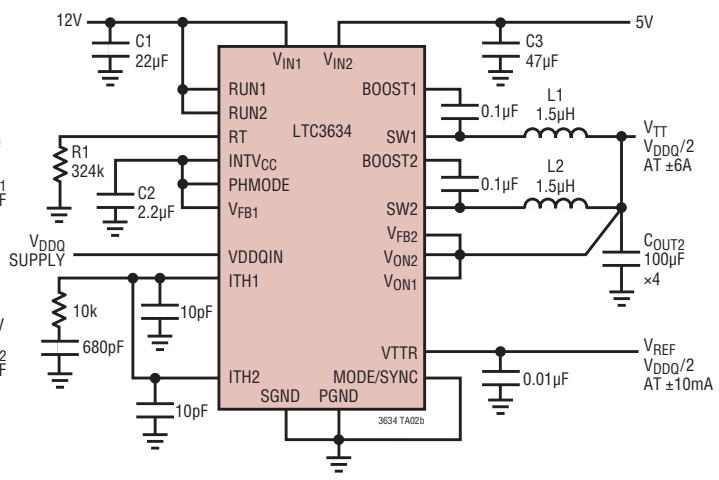


Figure 12b. 2-Phase V_{TT} Termination Using Two Input Supplies

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC3633	15V, Dual 3A (I_{OUT}), 4MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, $V_{IN(MIN)}$ = 3.6V, $V_{IN(MAX)}$ = 15V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 500µA, I_{SD} <15µA, 4mm × 5mm QFN-28, TSSOP-28E Package
LTC3605	15V, 5A (I_{OUT}), 4MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, $V_{IN(MIN)}$ = 4V, $V_{IN(MAX)}$ = 15V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 2mA, I_{SD} <15µA, 4mm × 4mm QFN-24 Package
LTC3604	15V, 2.5A (I_{OUT}), 4MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, $V_{IN(MIN)}$ = 3.6V, $V_{IN(MAX)}$ = 15V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 300µA, I_{SD} <15µA, 4mm × 4mm QFN-20, MSOP-16E Package
LTC3603	15V, 2.5A (I_{OUT}), 3MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, $V_{IN(MIN)}$ = 4.5V, $V_{IN(MAX)}$ = 15V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 75µA, I_{SD} <1µA, 4mm × 4mm QFN-20 MSOP-16E Package
LTC3601	15V, 1.5A (I_{OUT}), 4MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, $V_{IN(MIN)}$ = 4V, $V_{IN(MAX)}$ = 15V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 300µA, I_{SD} <15µA, 4mm × 4mm QFN-20, MSOP-16E Package
LTC3413	5.5V, 3A (I_{OUT} Sink/Source), 2MHz, Monolithic Synchronous Regulator for DDR/QDR Memory Termination	90% Efficiency, $V_{IN(MIN)}$ = 2.25V, $V_{IN(MAX)}$ = 5.5V, $V_{OUT(MIN)}$= V_{REF}/2, I_Q = 280µA, I_{SD} <1µA, TSSOP16E Package
LTC3612	5.5V, 3A, 4MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, $V_{IN(MIN)}$ = 2.25V, $V_{IN(MAX)}$ = 5.5V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 75µA, I_{SD} <1µA, 3mm × 4mm QFN-20 TSSOP-20E Package
LTC3614	5.5V, 4A, 4MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, $V_{IN(MIN)}$ = 2.25V, $V_{IN(MAX)}$ = 5.5V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 75µA, I_{SD} <1µA, 3mm × 5mm QFN-24 Package
LTC3616	5.5V, 6A, 4MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, $V_{IN(MIN)}$ = 2.25V, $V_{IN(MAX)}$ = 5.5V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 75µA, I_{SD} <1µA, 3mm × 5mm QFN-24 Package
LTC3615	5.5V, Dual 3A, 4MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, $V_{IN(MIN)}$ = 2.25V, $V_{IN(MAX)}$ = 5.5V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 130µA, I_{SD} <1µA, 4mm × 4mm QFN-24 TSSOP-24E Package
LTC3876	38V Dual DC/DC Controller for DDR Power with V_{TT} Reference	95% Efficiency, $V_{IN(MIN)}$ = 4.5V, $V_{IN(MAX)}$ = 38V, V_{PPQ} = 1V to 2.5V, V_{TT} = 1/2 V_{PPQ}, 5mm × 7mm QFN-38, TSSOP-38
LTC3633A	20V, Dual 3A (I_{OUT}), 4MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, $V_{IN(MIN)}$ = 3.6V, $V_{IN(MAX)}$ = 20V, I_Q = 500µA, I_{SD} <15µA, 4mm × 5mm QFN-28, TSSOP-28E Package

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