17V, Dual 1A Synchronous Step-Down Regulator with Ultralow Quiescent Current

FEATURES

- **Dual Step-Down Outputs: 1A Per Channel**
- **Wide V_{IN} Range: 2.7V to 17V**
- **Wide V_{OUT} Range: 0.6V to V_{IN}**
- **Up to 95% Efficiency**
- **No-Load I_Q = 5µA with Both Channels Enabled; I_Q < 4µA with Only One Channel Enabled**
- **High Efficiency, Low Dropout Operation (100% Duty Cycle)**
- **Constant Frequency (1MHz/2.25MHz) with External Frequency Synchronization**
- ±1% Output Voltage Accuracy
- Current Mode Operation for Excellent Line and Load Transient Response
- Phase Shift Programmable with External Clock
- Selectable Current Limit
- Internal Compensation and Soft-Start
- Compact 14-Pin DFN (3mm × 4mm) and 16-Lead MSOP Packages

APPLICATIONS

- Battery Powered Systems
- Point-of-Load Supplies
- Portable – Handheld Scanners

DESCRIPTION

The LTC®3622 is a dual 1A output, high efficiency synchronous monolithic step-down regulator capable of operating from input supplies up to 17V. The switching frequency is fixed to 1MHz or 2.25MHz with a ±50% synchronization range to an external clock. The regulator features ultralow quiescent current and high efficiency over a wide output voltage range.

The step-down regulators operate from an input voltage range of 2.7V to 17V and provide an adjustable output from 0.6V to V_{IN} while delivering up to 1A of output current. A user-selectable mode input is provided to allow the user to trade off ripple noise for light load efficiency. Burst Mode® operation provides the highest efficiency at light loads, while pulse-skipping mode provides the lowest ripple noise. The switching regulators can be synchronized to an external clock. Furthermore, fixed V_{OUT} options are available to eliminate the external feedback resistors.

List of LTC3622 Options

PART NAME	FREQUENCY	V_{OUT}
LTC3622	1.00MHz	Adjustable
LTC3622-2	2.25MHz	Adjustable
LTC3622-23/5	2.25MHZ	5V/3.3V

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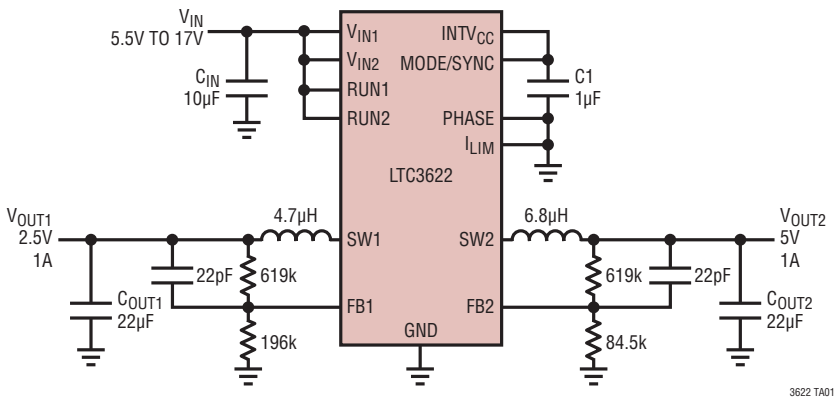
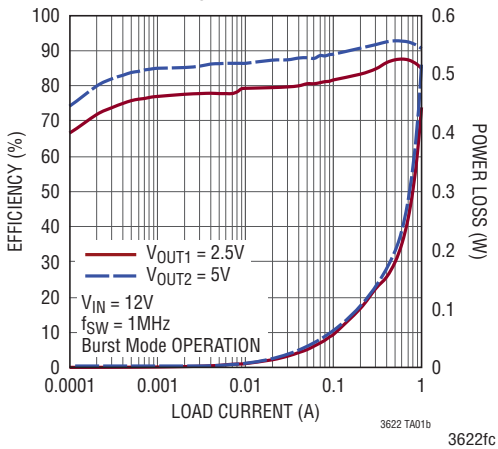
TYPICAL APPLICATION

2.5V/5V V_{OUT} Application, f_{SW} = 1MHz



Efficiency vs Load Current

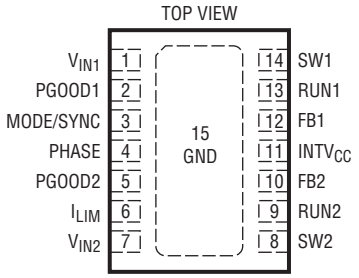


ABSOLUTE MAXIMUM RATINGS (Note 1)

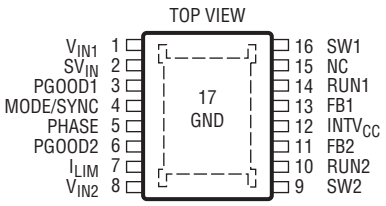
V_{IN1}, V_{IN2}, SV_{IN} (MSOP Only) (Note 2)..... –0.3V to 17V
RUN1, RUN2 .....–0.3V to V_{IN1}
MODE/SYNC, FB1, FB2 ..... –0.3V to 6V
PGOOD1, PGOOD2, I_{LIM}, PHASE..... –0.3V to 6V

Operating Junction Temperature Range (Note 3)
LTC3622E ..... –40°C to 125°C
LTC3622I ..... –40°C to 125°C
LTC3622H..... –40°C to 150°C
Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



DE PACKAGE
14-LEAD (4mm × 3mm) PLASTIC DFN
T_{JMAX} = 150°C, θ_{JA} = 40°C/W, θ_{JC} = 4.4°C/W
EXPOSED PAD (PIN 15) IS GND, MUST BE SOLDERED TO PCB



MSE PACKAGE
16-LEAD PLASTIC MSE
T_{JMAX} = 150°C, θ_{JA} = 40°C/W, θ_{JC} = 10°C/W
EXPOSED PAD (PIN 17) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

http://www.linear.com/product/LTC3622#orderinfo

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3622EDE#PBF	LTC3622EDE#TRPBF	3622	14-Lead (3mm x 4mm) Plastic DFN	–40°C to 125°C
LTC3622IDE#PBF	LTC3622IDE#TRPBF	3622	14-Lead (3mm x 4mm) Plastic DFN	–40°C to 125°C
LTC3622HDE#PBF	LTC3622HDE#TRPBF	3622	14-Lead (3mm x 4mm) Plastic DFN	–40°C to 150°C
LTC3622EMSE#PBF	LTC3622EMSE#TRPBF	3622	16-Lead Plastic MSOP	–40°C to 125°C
LTC3622IMSE#PBF	LTC3622IMSE#TRPBF	3622	16-Lead Plastic MSOP	–40°C to 125°C
LTC3622HMSE#PBF	LTC3622HMSE#TRPBF	3622	16-Lead Plastic MSOP	–40°C to 150°C
LTC3622EDE-2#PBF	LTC3622EDE-2#TRPBF	36222	14-Lead (3mm x 4mm) Plastic DFN	–40°C to 125°C
LTC3622IDE-2#PBF	LTC3622IDE-2#TRPBF	36222	14-Lead (3mm x 4mm) Plastic DFN	–40°C to 125°C
LTC3622HDE-2#PBF	LTC3622HDE-2#TRPBF	36222	14-Lead (3mm x 4mm) Plastic DFN	–40°C to 150°C
LTC3622EMSE-2#PBF	LTC3622EMSE-2#TRPBF	36222	16-Lead Plastic MSOP	–40°C to 125°C
LTC3622IMSE-2#PBF	LTC3622IMSE-2#TRPBF	36222	16-Lead Plastic MSOP	–40°C to 125°C
LTC3622HMSE-2#PBF	LTC3622HMSE-2#TRPBF	36222	16-Lead Plastic MSOP	–40°C to 150°C
LTC3622EDE-23/5#PBF	LTC3622EDE-23/5#TRPBF	223/5	14-Lead (3mm x 4mm) Plastic DFN	–40°C to 125°C
LTC3622IDE-23/5#PBF	LTC3622IDE-23/5#TRPBF	223/5	14-Lead (3mm x 4mm) Plastic DFN	–40°C to 125°C
LTC3622HDE-23/5#PBF	LTC3622HDE-23/5#TRPBF	223/5	14-Lead (3mm x 4mm) Plastic DFN	–40°C to 150°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C. V_{IN1} = V_{IN2} = 12V, unless otherwise noted. (Notes 3, 6)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	V_{IN1}, V_{IN2} Operating Voltage			2.7		17	V
	SV_{IN} Operating Voltage	MSOP Package		2.7		17	V
	V_{OUT} Operating Voltage			0.6		V_{IN}	V
I_Q	Input Quiescent Current	Active Mode, V_{RUN1} = V_{RUN2} = 2V (Note 4) Burst Mode Operation, V_{RUN1} = V_{RUN2} = 2V, MODE/SYNC = 3V, No Load Shutdown Mode; V_{RUN1} = V_{RUN2} = 0V			3 5 0.1	 10 ±1	mA µA µA
V_{FB}	Regulated Feedback Voltage	LTC3622/LTC3622-2	 ●	0.594 0.591	0.6 0.6	0.606 0.609	V
I_{FB}	FB Input Current	LTC3622/LTC3622-2				10	nA
V_{OUT1}	Regulated Fixed Output Voltage (Channel 1)	LTC3622-23/5	 ●	4.950 4.925	5.0 5.0	5.050 5.075	V V
V_{OUT2}	Regulated Fixed Output Voltage (Channel 2)	LTC3622-23/5	 ●	3.267 3.250	3.3 3.3	3.333 3.350	V V
$I_{FB(VOUT)}$	Feedback Input Leakage Current	LTC3622-23/5			1	5	µA
	Reference Voltage Line Regulation	V_{IN} = 2.7V to 17V (Note 5)			0.01	0.015	%/V
	Output Voltage Load Regulation	(Note 5)			0.1		%
	NMOS Switch Leakage PMOS Switch Leakage				0.1 0.1	1 1	µA µA
$R_{DS(ON)}$	NMOS On-Resistance PMOS On-Resistance	V_{IN} = 5V			0.15 0.37		Ω Ω
	Maximum Duty Cycle	V_{FB} = 0V	●		100		%
$t_{ON(MIN)}$	Minimum On-Time	V_{FB} = 0.7V, V_{IN1} = V_{IN2} = 5			75		ns
V_{RUN}	RUN Input High RUN Input Low			 0.35		1.0	V V
	RUN Input Current	V_{RUN} = 12V			0.1	±20	nA
V_{MODE}	Pulse-Skipping Mode Burst Mode Operation			 V_{INTVCC}–0.4		0.15	V V
	PHASE Input Threshold	Input Low Input High		 2.0		0.4	V V
	I_{LIM} Input Threshold	Input Low Input High		 V_{INTVCC}–0.1		0.1 $INTV_{CC}$	V V
t_{SS}	Soft Start Time				0.5		ms
I_{LIM}	Peak Current Limit	V_{IN} > 5V V_{ILIM} = 0.1V (Both Channels) V_{ILIM} = $INTV_{CC}$ – 0.1V (Both Channels) V_{ILIM} = Floating, Channel 1 V_{ILIM} = Floating, Channel 2		 1.6 0.8 1.6 0.8	 1.8 1.0 1.8 1.0	 2.0 1.2 2.0 1.2	A A A A
	V_{INTVCC} Undervoltage Lockout	V_{IN} Ramping Up		2.3	2.5	2.65	V
	V_{INTVCC} Undervoltage Lockout Hysteresis				160		mV
	V_{IN} Overvoltage Lockout Rising		●	18	19	20	V
	V_{IN} Overvoltage Lockout Hysteresis				300		mV

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C. V_{IN1} = V_{IN2} = 12V, unless otherwise noted. (Notes 3, 6)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
f_{OSC}	Oscillator Frequency	LTC3622-2/LTC3622-23/5 –40°C ≤ T_A ≤ 150°C LTC3622 –40°C ≤ T_A ≤ 125°C LTC3622 –40°C ≤ T_A ≤ 150°C	● ● ●	1.8 0.82 0.75	2.25 1.00 1.00	2.6 1.16 1.16	MHz MHz MHz
	External CLK Amplitude			0.4		V_{INTVCC}–0.3	V
	SYNC Capture Range	% of Programmed Frequency		50		150	%
V_{INTVCC}	$INTV_{CC}$ Voltage			3.3	3.6	3.9	V
	Power Good Range	V_{IN} > 4V			–7.5	–11	%
R_{PGOOD}	Power Good Resistance	PGOOD $R_{DS(ON)}$ at 2mA			275	350	Ω
t_{PGOOD}	PGOOD Delay	PGOOD Low to High PGOOD High to Low			0 32		Cycles Cycles
	Phase Shift Between Channel 1 and Channel 2	V_{PHASE} = 0V V_{PHASE} = $INTV_{CC}$, $V_{MODE/SYNC}$ = 0V			0 180		Deg Deg

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2. Transient Absolute Maximum Voltages should not be applied for more than 4% of the switching duty cycle.

Note 3. The LTC3622 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC3622E is guaranteed to meet specified performance from 0°C to 85°C. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3622I is guaranteed over the –40°C to 125°C operating junction temperature range and the LTC3622H is guaranteed over the -40°C to 150°C operating junction temperature range. High junction temperatures degrade operating lifetimes; operating lifetime is derated for junction temperatures greater than 125°C. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environment factors.

Note 4. The quiescent current in active mode does not include switching loss of the power FETs.

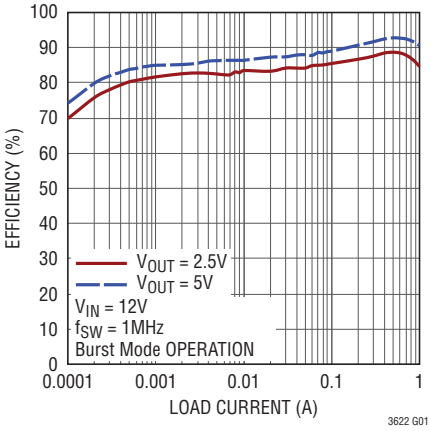
Note 5. The LTC3622 is tested in a proprietary test mode that connects V_{FB} to the output of error amplifier.

Note 6. T_J is calculated from the ambient T_A and power dissipation P_D according to the following formula: $T_J = T_A + (P_D \bullet \theta_{JA})$

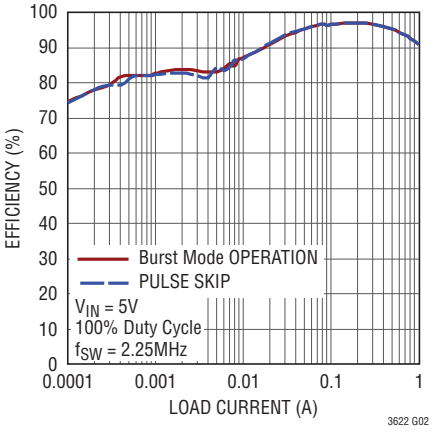
TYPICAL PERFORMANCE CHARACTERISTICS

$V_{IN1} = V_{IN2} = 12V$, $T_A = 25°C$, unless otherwise noted.

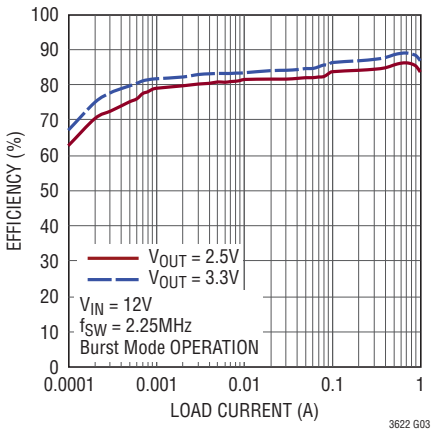
Efficiency vs Load Current



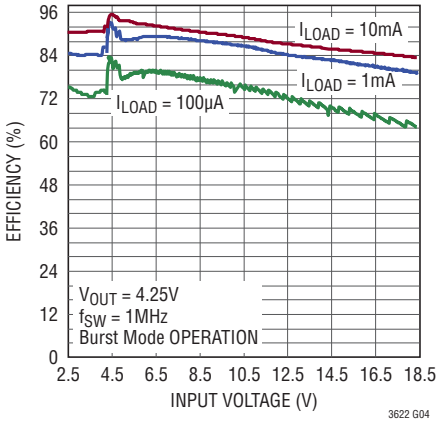
Efficiency vs Load Current at Dropout Operation



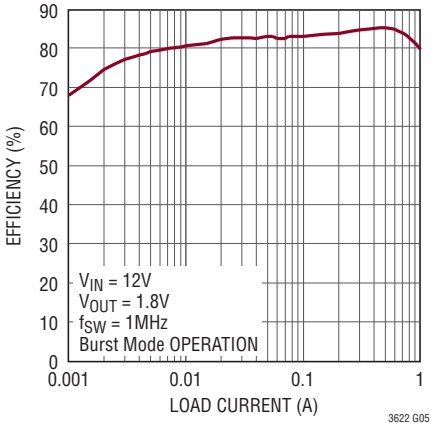
Efficiency vs Load Current



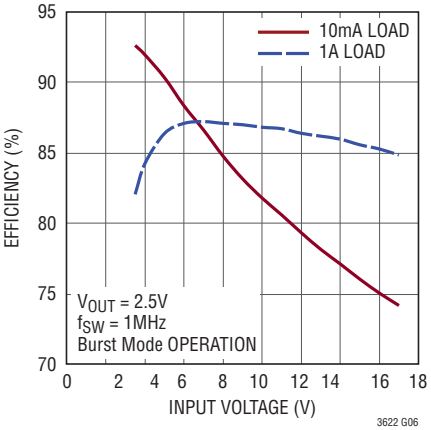
VOUT Efficiency vs Input Voltage Above and Below Dropout



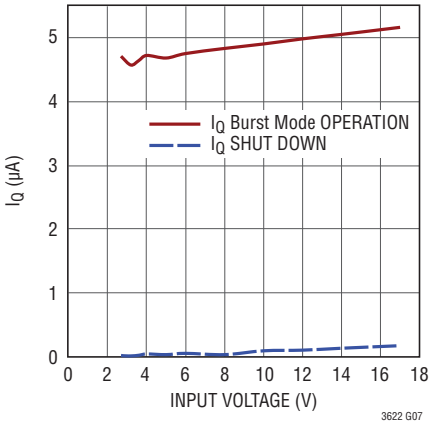
Efficiency vs Load Current



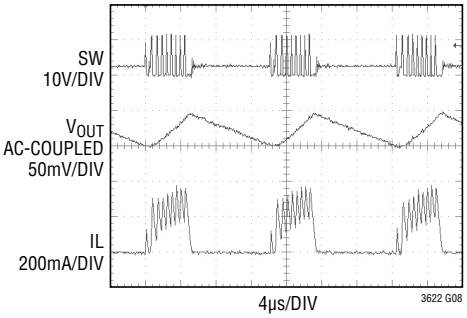
Efficiency vs Input Voltage



IQ vs VIN

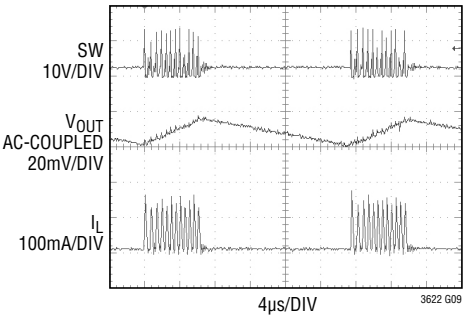


Burst Mode Operation



V_{IN} = 12V
V_{OUT} = 2.5V
Burst Mode OPERATION
I_{OUT} = 75mA

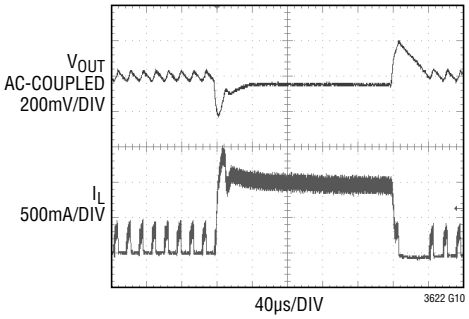
Pulse-Skipping Mode Operation



V_{IN} = 12V
V_{OUT} = 2.5V
PULSE-SKIPPING MODE
I_{OUT} = 10mA

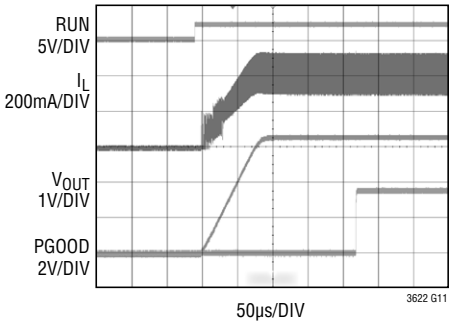
TYPICAL PERFORMANCE CHARACTERISTICS $V_{IN1} = V_{IN2} = 12V$, $T_A = 25°C$, unless otherwise noted.

Load Step

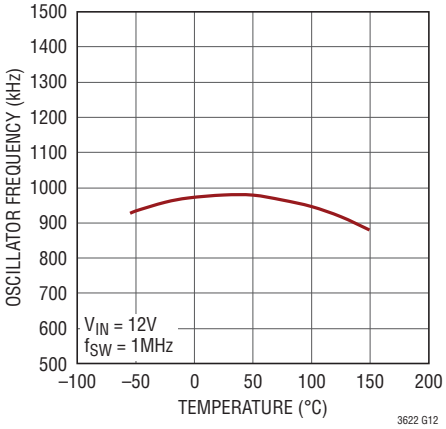


V_{IN} = 12V
V_{OUT} = 3.3V
Burst Mode OPERATION
LOAD STEP FROM 100mA TO 1A

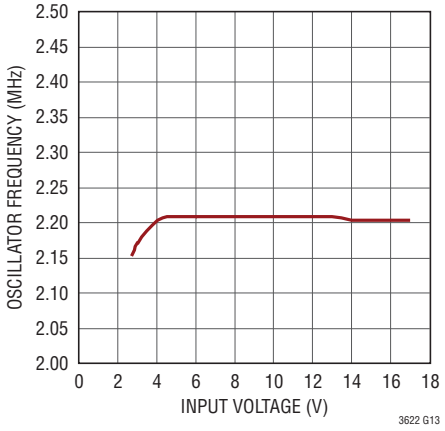
Start-Up Operation



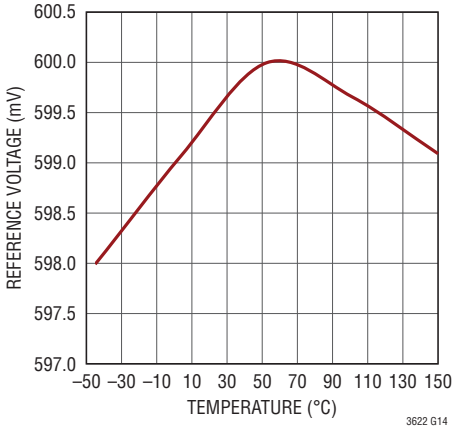
Oscillator Frequency vs Temperature



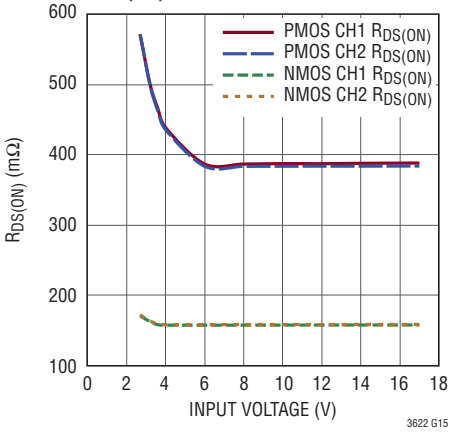
Oscillator Frequency vs Supply Voltage



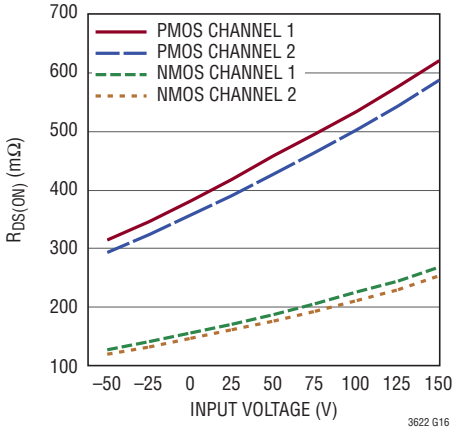
Reference Voltage vs Temperature



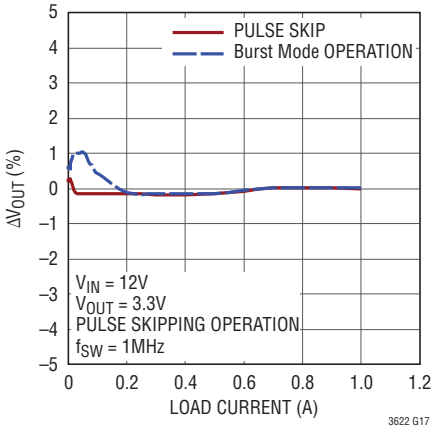
$R_{DS(ON)}$ vs Input Voltage



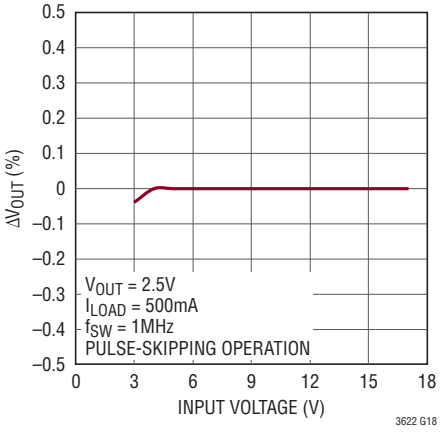
$R_{DS(ON)}$ vs Temperature



Load Regulation



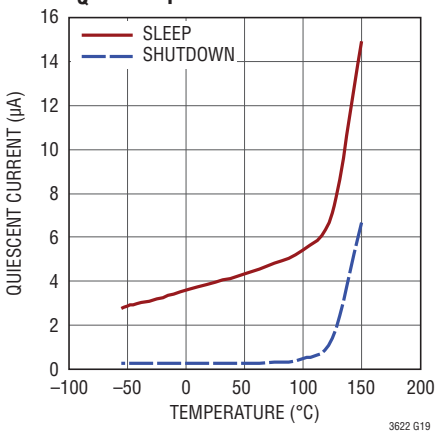
Line Regulation



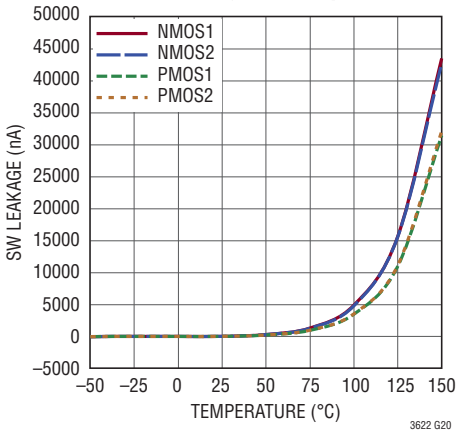
TYPICAL PERFORMANCE CHARACTERISTICS

$V_{IN1} = V_{IN2} = 12V$, $T_A = 25°C$, unless otherwise noted.

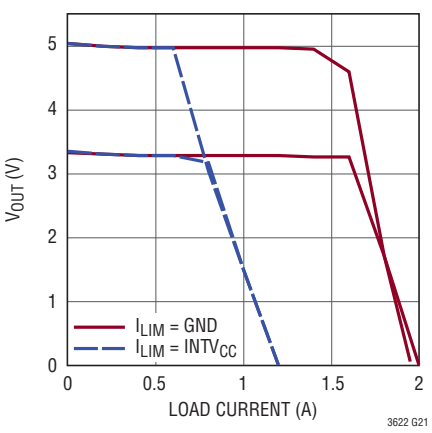
I_Q vs Temperature



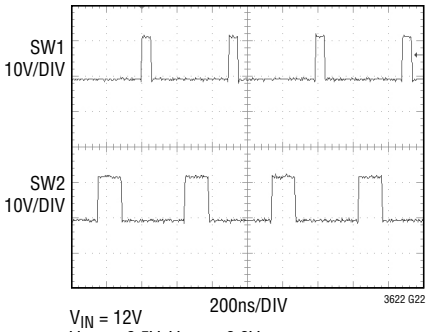
Switch Leakage vs Temperature



V_{OUT} vs Load Current

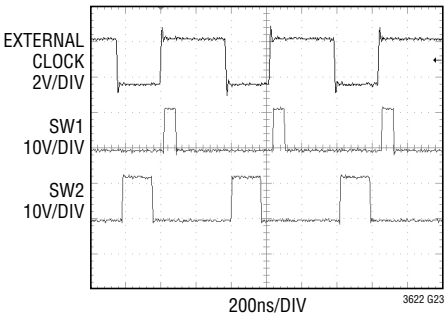


Out-Of-Phase Operation



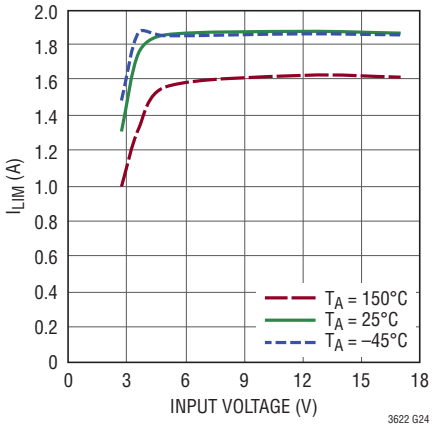
V_{IN} = 12V
V_{OUT} = 2.5V, V_{OUT} = 3.3V
L1 = 4.7µH, L2 = 3.3µH
OUT-OF-PHASE OPERATION

Sync Mode Out-Of-Phase Operation



SYNC MODE OPERATION
EXTERNAL CLOCK PULSE WIDTH
CONTROLS PHASE SHIFT

I_{LIM} vs Input Voltage



PIN FUNCTIONS (DFN/MSOP)

VIN1 (Pin 1/Pin 1): Input Voltage of Channel 1 Step-Down Regulator. This input also powers the $INTV_{CC}$ LDO.

PGOOD1 (Pin 2/Pin 3): Open Drain Power Good Indicator for Channel 1.

MODE/SYNC (Pin 3/Pin 4): Burst Mode Select and External Clock Synchronization of the Step-Down Regulator. Tie MODE/SYNC to $INTV_{CC}$ for Burst Mode operation with a 400mA peak current clamp. Tie MODE/SYNC to GND for pulse-skipping operation. Furthermore, connecting this pin to an external clock will synchronize the switch clock to the external clock and put the part in pulse-skipping mode.

PHASE (Pin 4/Pin 5): Phase Select Pin. Tie this pin to ground to run the regulators in phase (0° phase shift) between SW rising edge of channel 1 and channel 2. Tie this pin to $INTV_{CC}$ to set 180° phase shift between channels. When this pin is high, the phase shift may also be set by modulating the duty cycle of external clock on the MODE/SYNC pin (channel 1 edge synced to rising edge of external clock, channel 2 edge synced to falling edge of external clock). See Applications Section for more details.

PGOOD2 (Pin 5/Pin 6): Open Drain Power Good Indicator for Channel 2.

ILIM (Pin 6/Pin 7): Current Limit Select Pin. Tying this pin to ground sets the full current limit for both channels. Tying this pin to $INTV_{CC}$ drops the current limit by a factor of 2 for both channels. Biasing this pin to 1V sets the current on channel 1 to be the full amount, and the current on channel 2 to be dropped by a factor of 2.

VIN2 (Pin 7/Pin 8): Input Voltage of Channel 2 Step-Down Regulator. May be a different voltage than V_{IN1}.

SW2 (Pin 8/Pin 9): Switch Node Connection to the Inductor of Channel 2 Step-Down Regulator.

RUN2 (Pin 9/Pin 10): Logic Controlled RUN Input to Channel 2. Do not leave this pin floating. Logic high activates the step-down regulator.

FB2 (Pin 10/Pin 11): Feedback Input to the Error Amplifier of Channel 2 Step-Down Regulator. Connect resistor divider tap to this pin. The output voltage can be adjusted from 0.6V to V_{IN} by: $V_{OUT} = 0.6V \bullet [1 + (R2/R1)]$. (Figure 2) For fixed V_{OUT} options, connect the FB pin directly to V_{OUT}.

$INTV_{CC}$ (Pin 11/Pin 12): Low Dropout Regulator. Bypass with a low ESR capacitor of at least 1µF to ground.

FB1 (Pin 12/Pin 13): Feedback Input to the Error Amplifier of Channel 1 Step-Down Regulator. Connect resistor divider tap to this pin. The output voltage can be adjusted from 0.6V to V_{IN} by: $V_{OUT} = 0.6V \bullet [1 + (R2/R1)]$. (Figure 2) For fixed V_{OUT} options, connect the FB pin directly to V_{OUT}.

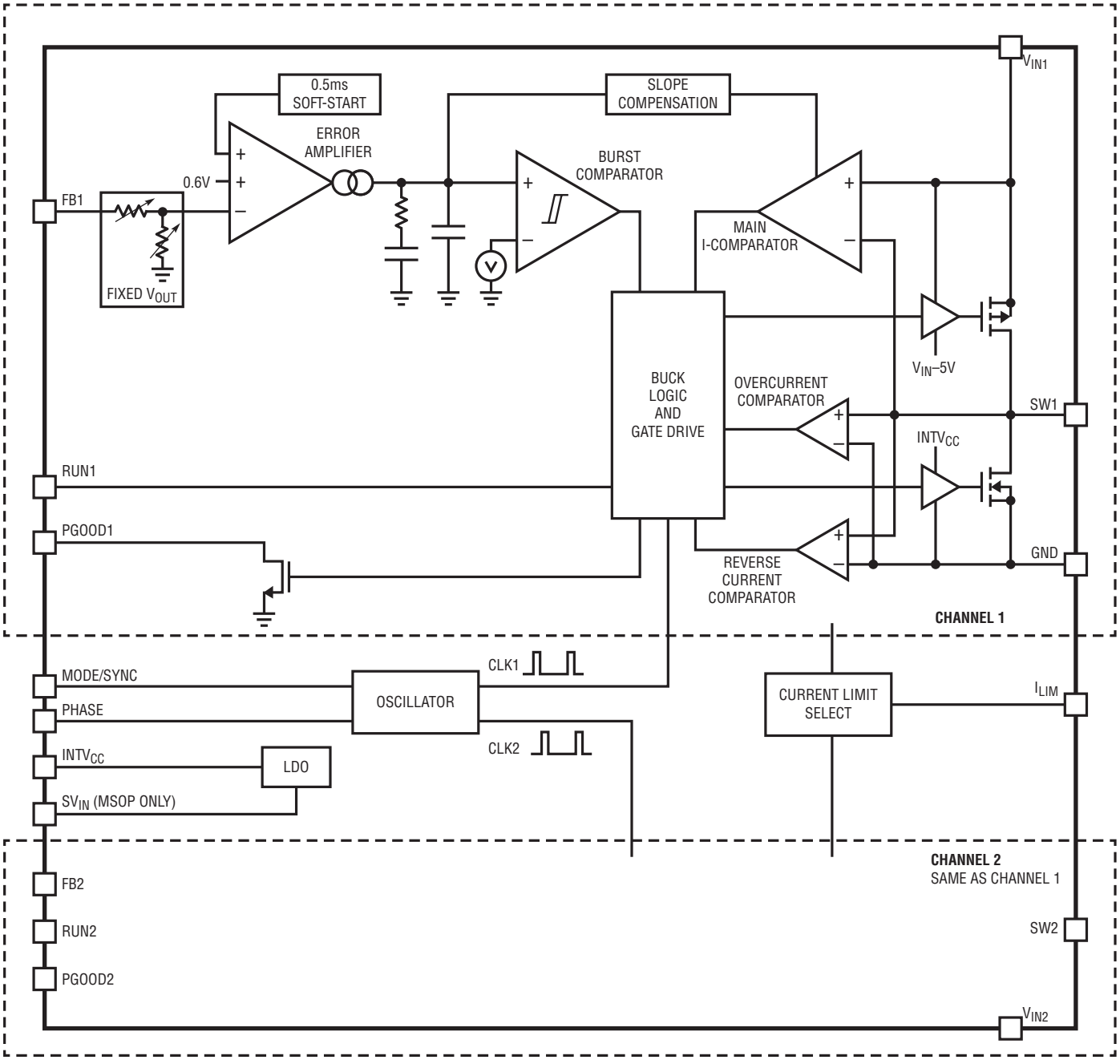
RUN1 (Pin 13/Pin 14): Logic Controlled RUN Input to Channel 1. Do not leave this pin floating. Logic high activates the step-down regulator.

SW1 (Pin 14/Pin 16): Switch Node Connection to the Inductor of Channel 1 Step-Down Regulator.

GND (Pin 15/Pin 17): Ground for Power and Signal Ground. The exposed pad must be connected to PCB ground for rated electrical and rated thermal performance.

SV_{IN} (NA/Pin 2): Signal V_{IN} Pin. This input powers the $INTV_{CC}$. May be a different voltage than either V_{IN1} or V_{IN2}. Connect SV_{IN} to either V_{IN1} or V_{IN2} , whichever one is higher. For applications where it is not known which V_{IN} is higher, connect external diode between SV_{IN} to both V_{IN1} and V_{IN2} to ensure that SV_{IN} is less than a diode drop from the higher of V_{IN1} or V_{IN2}.

BLOCK DIAGRAM



OPERATION

The LTC3622 is a dual high efficiency monolithic step-down regulator, which uses a constant frequency, peak current mode architecture. It operates through a wide V_{IN} range and regulates with ultralow quiescent current. The operation frequency is set at either 2.25MHz or 1MHz and can be synchronized to an external oscillator ±50% of the inherent frequency. To suit a variety of applications, the selectable MODE/SYNC pin allows the user to trade off output ripple for efficiency.

For each channel, the output voltage is set by an external divider returned to the FB pin. An error amplifier compares the divided output voltage with a reference voltage of 0.6V and adjusts the peak inductor current accordingly. Overvoltage and undervoltage comparators will pull the PGOOD output low if the output voltage is not within 7.5% of the programmed value. The PGOOD output will go high immediately after achieving regulation and will go low 32 clock cycles after falling out of regulation.

Main Control Loop

During normal operation, the top power switch (P-channel MOSFET) is turned on at the beginning of a clock cycle. The inductor current is allowed to ramp up to a peak level. Once the level is reached, the top power switch is turned off and the bottom switch (N-channel MOSFET) is turned on until the next clock cycle. The peak current level is controlled by the internally compensated I_{TH} voltage, which is the output of the error amplifier. This amplifier compares the FB voltage to the 0.6V internal reference. When the load current increases, the FB voltage decreases slightly below the reference, which causes the error amplifier to increase the I_{TH} voltage until the average inductor current matches the new load current.

The main control loop is shut down by pulling the RUN pin to ground.

Low Current Operation

Two discontinuous conduction modes (DCM) are available to control the operation of the LTC3622 at low currents. Both modes, Burst Mode operation and pulse-skipping mode, automatically switch from continuous operation to the selected mode when the load current is low.

To optimize efficiency, Burst Mode operation can be selected by tying the MODE/SYNC pin to $INTV_{CC}$. In Burst Mode operation, the peak inductor current is set to be at least 400mA, even if the output of the error amplifier demands less. Thus, when the switcher is on at relatively light output loads, FB voltage will rise and cause the I_{TH} voltage to drop. Once the I_{TH} voltage drops low enough, the switcher goes into sleep mode with both power switches off. The switchers remain in this sleep state until the external load pulls the output voltage below its regulation point. When both channels are in sleep mode, the part draws an ultralow 5µA of quiescent current from V_{IN}.

To minimize V_{OUT} ripple, pulse-skipping mode can be selected by grounding the MODE/SYNC pin. In LTC3622, pulse-skipping mode is implemented similarly to Burst Mode operation with the peak inductor current set to be at above 66mA. This results in lower ripple than in Burst Mode operation with the trade-off being slightly lower efficiency.

High Duty Cycle/Dropout Operation

When the input supply voltage decreases towards the output voltage, the duty cycle increases and slope compensation is required to maintain the fixed switching frequency. The LTC3622 has internal circuitry to accurately maintain the peak current limit (I_{LIM}) of 1.8A even at high duty cycles.

As the duty cycle approaches 100%, the LTC3622 enters dropout operation. During dropout, the part will transition in and out of sleep mode depending on the output load current. This significantly reduces the quiescent current, thus prolonging the use of the input supply.

OPERATION

V_{IN} Overvoltage Protection

In order to protect the internal power MOSFET devices against transient voltage events, the LTC3622 constantly monitors the V_{IN1} and V_{IN2} pins for an overvoltage condition. When V_{IN1} or V_{IN2} rise above 18.5V, both regulators suspend operation by shutting off both power MOSFETs. Once V_{IN} drops below 18.2V, the regulator immediately resumes normal operation. The regulators execute soft-start when exiting an overvoltage condition.

Low Supply Operation

The LTC3622 incorporates undervoltage lockout circuits which shut down the part when the input voltages drop below 2.5V. As the input voltages rise slightly above the undervoltage threshold, the switchers will begin basic operation. However, the $R_{DS(ON)}$ of the top and bottom switch of each channel will be slightly higher than that specified in the electrical characteristics due to lack of gate drive. Refer to graph of $R_{DS(ON)}$ versus V_{IN} for more details.

Phase Selection

The two channels of LTC3622 can operate in phase, 180° out-of-phase (anti-phase) depending on the state of PHASE pin- low, or high, respectively. Anti-phase generally reduces input voltage and current ripple. Crosstalk between switch nodes SW1, SW2 and components or sensitive lines connected to FBx, can sometimes cause unstable switching waveforms and unexpectedly large input and output voltage ripple.

The situation improves if rising and falling edges of the switch nodes are timed carefully not to coincide. Depending on the duty cycle of the two channels, choose the phase difference between the channels to keep edges as far away from each other as possible.

Crosstalk can generally be avoided by carefully choosing the phase shift such that the SW edges do not coincide. However, there are often situations where this is unavoidable, such as when both channels are operating at near 50% duty cycle. In such cases, the optimized phase shift can be set by modulating the duty cycle of external clock on the MODE/SYNC pin (channel 1 edge synced to rising edge of external clock, channel 2 edge synced to falling edge of external clock), while keeping the PHASE pin voltage high. Figure 1 shows a 90° phase shifting between two channels. Table 1 shows the phase selection by the PHASE pin.

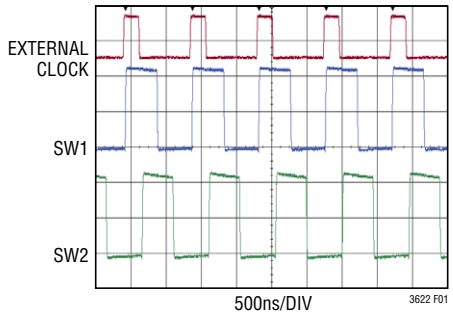


Figure 1. 90° Phase Shift Set by External Clock

Table 1. Phase Selection

	NO EXTERNAL CLK	EXTERNAL CLK
PHASE = 0	0° Phase Shift	0° Phase Shift
PHASE = $INTV_{CC}$	180° Phase Shift	Phase Shift Determined by Clock Edges

Soft-Start

The LTC3622 has a 500µs soft-start ramp for each channel when enabled. During soft-start operation, the switchers operate in pulse-skipping mode.

APPLICATIONS INFORMATION

Output Voltage Programming

For non-fixed output voltage parts, the output voltage is set by external resistive dividers according to the following equation:

$$V_{OUT} = 0.6V \bullet \left(1 + \frac{R2}{R1}\right)$$

The resistive divider allows the FB pin to sense a fraction of the output voltage as shown in Figure 2.

For fixed V_{OUT} parts, tie FB directly to V_{OUT}, as R2 and R1 are matched internal resistors.

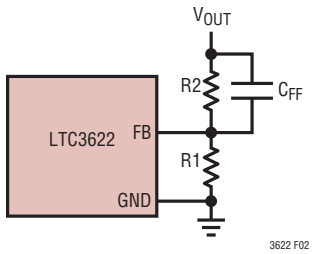


Figure 2. Setting the Output Voltage

Input Capacitor (C_{IN}) Selection

The input capacitance, C_{IN}, is needed to filter the square wave current at the drain of the top power MOSFET. To prevent large voltage transients from occurring, a low ESR input capacitor sized for the maximum RMS current should be used. The RMS current calculation is different if the part is used in in-phase or out-of-phase.

For "in phase", when $V_{OUT1} = V_{OUT2}$

$$\frac{\sqrt{V_{OUT}(V_{IN} - V_{OUT})}}{V_{IN}}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$. This simple worst case is commonly used to determine the highest I_{RMS}.

For out-of-phase case, the ripple current can be lower than the "in phase" current. The maximum current typically occurs when $V_{OUT1} – V_{IN}/2 = V_{OUT2}$ or when $V_{OUT2} – V_{IN}/2 = V_{OUT1}$. As a good rule of thumb, the amount of worst case ripple is about 75% of the worst case ripple in the in-phase mode. Also note that when $V_{OUT1} = V_{OUT2} = V_{IN}/2$ and I1 = I2, the input current ripple is at its minimum.

Note that ripple current ratings from capacitor manufacturers are often based on only 2000 hours of life which makes it advisable to further derate the capacitor, or choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design. For low input voltage applications, sufficient bulk input capacitance may be needed to minimize transient effects during output load changes.

Output Capacitor (C_{OUT}) Selection

The selection of C_{OUT} is determined by the effective series resistance (ESR) that is required to minimize voltage ripple and load step transients as well as the amount of bulk capacitance that is necessary to ensure that the control loop is stable. Loop stability can be checked by viewing the load transient response. The output ripple, ΔV_{OUT}, is determined by:

$$\Delta V_{OUT} < \Delta I_L \left(\frac{1}{8 \bullet f \bullet C_{OUT}} + ESR\right)$$

The output ripple is highest at maximum input voltage since ΔI_L increases with input voltage. Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirements. Dry tantalum, special polymer and hybrid conductive polymer capacitors are very low ESR but have lower capacitance density than other types. Tantalum capacitors have the highest capacitance density but it is importance to only use types that have been surge tested for use in switching power supplies. Aluminum electrolytic capacitors have significantly higher ESR, but can be used in cost-sensitive applications provided that consideration is given to ripple current ratings and long-term reliability. Ceramic capacitors have excellent low ESR characteristics and small footprints.

Using Ceramic Input and Output Capacitors

Higher capacitance value, lower cost ceramic capacitors are now becoming available in smaller case sizes. Their high ripple current, high voltage rating and low ESR make them ideal for switching regulator applications. However, care must be taken when these capacitors are used at the input and output. When a ceramic capacitor is used

APPLICATIONS INFORMATION

at the input and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the V_{IN} input. At best, this ringing can couple to the output and be mistaken as loop instability. At worst, a sudden inrush of current through the long wires can potentially cause a voltage spike at V_{IN} large enough to damage the part.

When choosing the input and output ceramic capacitors, choose the X5R and X7R dielectric formulations. These dielectrics have the best temperature and voltage characteristics of all the ceramics for a given value and size.

Since the ESR of a ceramic capacitor is so low, the input and output capacitor must instead fulfill a charge storage requirement. During a load step, the output capacitor must instantaneously supply the current to support the load until the feedback loop raises the switch current enough to support the load. Typically, five cycles are required to respond to a load step, but only in the first cycle does the output voltage drop linearly. The output droop, V_{DROOP}, is usually about three times the linear drop of the first cycle.

Thus, a good place to start with the output capacitor value is approximately:

$$C_{OUT} = 3\frac{\Delta I_{OUT}}{f_O \bullet V_{DROOP}}$$

More capacitance may be required depending on the duty cycle and load step requirements. In most applications, the input capacitor is merely required to supply high frequency bypassing, since the impedance to the supply is very low. A 10µF ceramic capacitor is usually enough for these conditions. Place this input capacitor as close to the V_{IN1} and V_{IN2} pins as possible.

Output Power Good

When the LTC3622's output voltages are within the ±7.5% window of the regulation point, the output voltages are good and the PGOOD pins are pulled high with external resistors. Otherwise, internal open-drain pull-down devices (275Ω) will pull the PGOOD pins low. To prevent unwanted PGOOD glitches during transients or dynamic V_{OUT} changes, the LTC3622's PGOOD falling edge includes a blanking delay of approximately 32 switching cycles.

Frequency Synchronization Capability

The LTC3622 has the capability to synchronize to a ±50% range of the internal programmed frequency. It takes several cycles of external clock to engage the sync mode, and roughly 2µs for the part to detect the absence of the external clock signal. Once engaged in sync, the LTC3622 immediately runs at the external clock frequency.

Inductor Selection

Given the desired input and output voltages, the inductor value and operating frequency determine the ripple current:

$$\Delta I_L = \frac{V_{OUT}}{f \bullet L}\left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right)$$

Lower ripple current reduces power losses in the inductor, ESR losses in the output capacitors and output voltage ripple. Highest efficiency operation is obtained at low frequency with small ripple current. However, achieving this requires a large inductor. There is a trade-off between component size, efficiency and operating frequency.

A reasonable starting point is to choose a ripple current that is about 50% of $I_{OUT(MAX)}$. To guarantee that ripple current does not exceed a specified maximum, the inductance should be chosen according to:

$$L = \frac{V_{OUT}}{f \bullet \Delta I_{L(MAX)}}\left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right)$$

Once the value for L is known, the type of inductor must be selected. Actual core loss is independent of core size for a fixed inductor value, but is very dependent on the inductance selected. As the inductance or frequency increases, core loss decreases. Unfortunately, increased inductance requires more turns of wire and therefore copper losses increase.

Ferrite designs have very low core losses and are preferred at high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates "hard," which means that inductance collapses abruptly when the peak design current is exceeded. This results in an abrupt increase in inductor

APPLICATIONS INFORMATION

ripple current and consequent output voltage ripple. Do not allow the core to saturate!

Different core materials and shapes change the size/current and price/current relationship of an inductor. Toroid or shielded pot cores in ferrite or permalloy materials are small and don't radiate much energy, but generally cost more than powdered iron core inductors with similar characteristics. The choice of which style inductor to use mainly depends on the price versus size requirements and any radiated field/EMI requirements. New designs for surface mount inductors are available from Toko, Vishay, NEC/Tokin, Cooper, TDK and Würth Elektronik. Refer to Table 2 for more details.

Checking Transient Response

The regulator loop response can be checked by looking at the load transient response. Switching regulators take several cycles to respond to a step in load current. When a load step occurs, V_{OUT} immediately shifts by an amount equal to the $\Delta I_{LOAD} \bullet$ ESR, where ESR is the effective series

Table 2. Inductor Selection Table

INDUCTOR	INDUCTANCE (µH)	DCR (mΩ)	MAX CURRENT (A)	DIMENSIONS (mm)	HEIGHT (mm)	MANUFACTURER
IHLP-1616BZ-11 Series	1.0 2.2 4.7	24 61 95	4.5 3.25 1.7	4.3 × 4.7 4.3 × 4.7 4.3 × 4.7	2 2 2	Vishay www.vishay.com
IHLP-2020BZ-01 Series	1 2.2 3.3 4.7 5.6 6.8	18.9 45.6 79.2 108 113 139	7 4.2 3.3 2.8 2.5 2.4	5.4 × 5.7 5.4 × 5.7 5.4 × 5.7 5.4 × 5.7 5.4 × 5.7 5.4 × 5.7	2 2 2 2 2 2	
FDV0620 Series	1 2.2 3.3 4.7	18 37 51 68	5.7 4 3.2 2.8	6.7 × 7.4 6.7 × 7.4 6.7 × 7.4 6.7 × 7.4	2 2 2 2	Toko www.toko.com
MPLC0525L Series	1 1.5 2.2	16 24 40	6.4 5.2 4.1	6.2 × 5.4 6.2 × 5.4 6.2 × 5.4	2.5 2.5 2.5	NEC/Tokin www.nec-tokin.com
HCM0703 Series	1 1.5 2.2 3.3 4.7	9 14 18 28 37	11 9 8 6 5.5	7 × 7.4 7 × 7.4 7 × 7.4 7 × 7.4 7 × 7.4	3 3 3 3 3	Cooper Bussmann www.cooperbussmann.com
RLF7030 Series	1 1.5 2.2 3.3 4.7 6.8	8.8 9.6 12 20 31 45	6.4 6.1 5.4 4.1 3.4 2.8	6.9 × 7.3 6.9 × 7.3 6.9 × 7.3 6.9 × 7.3 6.9 × 7.3 6.9 × 7.3	3.2 3.2 3.2 3.2 3.2 3.2	TDK www.tdk.com
WE-TPC 4828 Series	1.2 1.8 2.2 2.7 3.3 3.9 4.7	17 20 23 27 30 47 52	3.1 2.7 2.5 2.35 2.15 1.72 1.55	4.8 × 4.8 4.8 × 4.8 4.8 × 4.8 4.8 × 4.8 4.8 × 4.8 4.8 × 4.8 4.8 × 4.8	2.8 2.8 2.8 2.8 2.8 2.8 2.8	Würth Elektronik www.we-online.com
XFL4020 Series	1.0 1.5 2.2 3.3 4.7	10.8 14.4 21.35 34.8 52.2	8 6.7 6.0 3.9 3.6	4 × 4 4 × 4 4 × 4 4 × 4 4 × 4	2 2 2 2 2	Coilcraft www.coilcraft.com

APPLICATIONS INFORMATION

resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT} generating a feedback error signal used by the regulator to return V_{OUT} to its steady state value. During this recovery time, V_{OUT} can be monitored for overshoot or ringing that indicates a stability problem.

The initial output voltage step may not be within the bandwidth of the feedback loop, so the standard second order overshoot/DC ratio cannot be used to determine phase margin. In addition, a feedforward capacitor can be added to improve the high frequency response, shown in Figure 2. Capacitor C_{FF} provides phase lead by creating a high frequency zero with R2, which improves the phase margin.

The output voltage settling behavior is related to the stability of the closed-loop system and demonstrates the actual overall supply performance. For a detailed explanation of optimizing the compensation components, including a review of control loop theory, refer to Application Note 76.

In some applications, a more severe transient can be caused by switching in loads with large (>1µF) input capacitors. The discharge input capacitors are effectively put in parallel with C_{OUT}, causing a rapid drop in V_{OUT}. No regulator can deliver enough current to prevent this problem if the switch connecting to load has low resistance and is driven quickly. The solution is to limit the turn-on speed of the load switch driver. A Hot Swap controller is designed specifically for this purpose and usually incorporates current limiting, short-circuit protection and soft-starting.

Efficiency Considerations

The percent efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Percent efficiency can be expressed as:

$$\% \text{ Efficiency} = 100\% - (L1 + L2 + L3 + \ldots)$$

where L1, L2 etc. are the individual losses as a percentage of input power. Although all dissipative elements in the circuit produce losses, three main sources usually account for most of the losses in LTC3622 circuit: 1) I^2R losses, 2) switching and biasing losses, 3) other losses.

1. I^2R losses are calculated from the DC resistances of the internal switches, R_{SW}, and external inductor, R_L. In continuous mode, the average output current flows through inductor L but is "chopped" between the internal top and bottom power MOSFETs. Thus, the series resistance looking into the SW pin is a function of both top and bottom MOSFET $R_{DS(ON)}$ and the duty cycle (DC) as follows:

   $$R_{SW} = (R_{DS(ON)TOP})(DC) + (R_{DS(ON)BOT})(1 - DC)$$

   The $R_{DS(ON)}$ for both the top and bottom MOSFETs can be obtained from the Typical Performance Characteristics curves. Thus to obtain I^2R losses:

   $$I^2R \text{ Losses} = I_{OUT}^2(R_{SW} + R_L)$$

2. The switching current is the sum of the MOSFET driver and control currents. The power MOSFET driver current results from switching the gate capacitance of the power MOSFETs. Each time a power MOSFET gate is switched from low to high to low again, a packet of charge dQ moves from V_{IN} to ground. The resulting dQ/dt is a current out of V_{IN} that is typically much larger than the DC control bias current. In continuous mode, $I_{GATECHG} = f_{OSC}(Q_T + Q_B)$, where Q_T and Q_B are the gate charges of the internal top and bottom power MOSFETs and f_{OSC} is the switching frequency. The power loss is thus:

   $$\text{Switching Loss} = I_{GATECHG} \bullet V_{IN}$$

   The gate charge loss is proportional to V_{IN} and f_{OSC} and thus their effects will be more pronounced at higher supply voltages and higher frequencies.

3. Other "hidden" losses such as transition loss and copper trace and internal load resistances can account for additional efficiency degradations in the overall power system. It is very important to include these "system" level losses in the design of a system. Transition loss arises from the brief amount of time the top power MOSFET spends in the saturated region during switch node transitions. The LTC3622 internal power devices switch quickly enough that these loses are not significant compared to other sources. These losses plus other losses, including diode conduction losses during dead time and inductor core losses, generally account for less than 2% total additional loss.

APPLICATIONS INFORMATION

Thermal Conditions

In a majority of applications, the LTC3622 does not dissipate much heat due to its high efficiency. However, in applications where the LTC3622 is running at high ambient temperature, high V_{IN}, high switching frequency, and maximum output current load, the heat dissipated may exceed the maximum junction temperature of the part. If the junction temperature reaches approximately 160°C, all power switches will be turned off until the temperature drops about 15°C cooler.

To prevent the LTC3622 from exceeding the maximum junction temperature, the user needs to do some thermal analysis. The goal of the thermal analysis is to determine whether the power dissipated exceeds the maximum junction temperature of the part. The temperature rise is given by:

$$T_{RISE} = P_D \bullet \theta_{JA}$$

As an example, consider the case when the LTC3622 is used in applications where V_{IN} = 12V, $I_{OUT} = I_{OUT1} = I_{OUT2}$ = 1A, f = 2.25MHz, $V_{OUT} = V_{OUT1} = V_{OUT2}$ = 1.8V. The equivalent power MOSFET resistance R_{SW} is:

$$R_{SW} = R_{DS(ON)TOP} \bullet \frac{V_{OUT}}{V_{IN}} + R_{DS(ON)BOT} \bullet \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

$$= 370m\Omega \bullet \frac{1.8V}{12V} + 150m\Omega \bullet \left(1 - \frac{1.8V}{12V}\right) = 183m\Omega$$

The active current through V_{IN} at 2.25MHz without load is about 10mA, which includes switching and internal biasing current loss, and transition loss. Therefore, the total power dissipated by the part is:

$$P_D = 2 \bullet I_{OUT}^2 \bullet R_{SW} + V_{IN} \bullet I_{IN(Q)}$$

$$= 2 \bullet 1A^2 \bullet 183m\Omega + 12V \bullet 10mA$$

$$= 486mW$$

For the DFN package, the θ_{JA} is 40°C/W. Therefore, the junction temperature of the regulator operating at 25°C ambient temperature is approximately:

$$T_J = 486mW \bullet 40°C/W + 25°C = 44.4°C$$

Remembering that the above junction temperature is obtained from an $R_{DS(ON)}$ at 25°C, we might recalculate the junction temperature based on a higher $R_{DS(ON)}$ since it increases with temperature. Redoing the calculation assuming that R_{SW} increased 5% at 44.4°C yields a new junction temperature of 45.4°C. If the application calls for a higher ambient temperature and/or higher switching frequency, care should be taken to reduce the temperature rise of the part by using a heat sink or air flow.

APPLICATIONS INFORMATION

Board Layout Considerations

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the LTC3622 (refer to Figure 3). Check the following in the layout:

1. Do the capacitors C_{IN} connect to the V_{IN} and GND as close as possible? These capacitors provide the AC current to the internal power MOSFETs and their drivers. Does C_{VCC} connect to $INTV_{CC}$ as close as possible?
2. Are C_{OUT} and L closely connected? The (–) plate of C_{OUT} returns current to GND and the (–) plate of C_{IN}.
3. The resistive divider, R1 and R2, must be connected between the (+) plate of C_{OUT} and a ground line terminated near GND. The feedback signal V_{FB} should be routed away from noisy components and traces, such as the SW line, and its trace should be minimized. Keep R1 and R2 close to the IC.
4. Solder the exposed pad (Pin 15 for DFN, Pin 17 for MSOP) on the bottom of the package to the GND plane. Connect this GND plane to other layers with thermal vias to help dissipate heat from the LTC3622.
5. Keep sensitive components away from the SW pin. The input capacitor, C_{IN}, feedback resistors, and $INTV_{CC}$ bypass capacitors should be routed away from the SW trace and the inductor.
6. A ground plane is highly recommended.
7. Flood all unused areas on all layers with copper, which reduces the temperature rise of power components. These copper areas should be connected to GND.

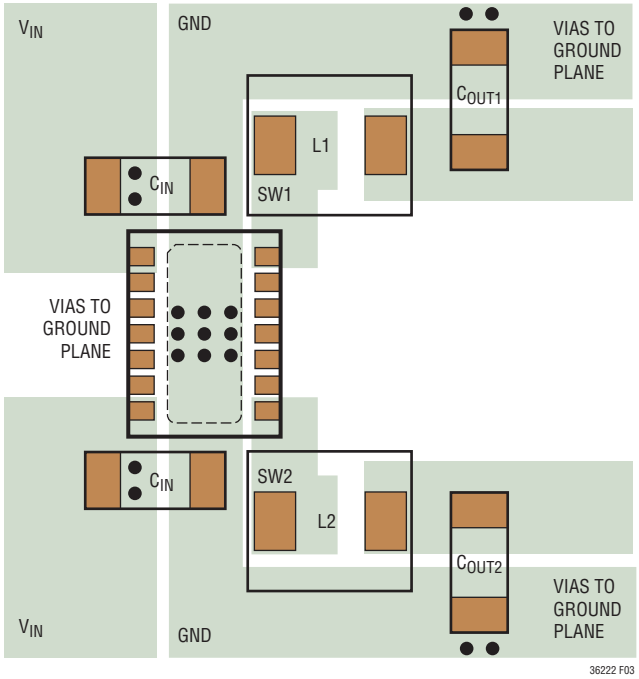


Figure 3. Layout Diagram

APPLICATIONS INFORMATION

Design Example

As a design example, consider using the LTC3622 in an application with the following specifications:

$V_{IN1} = V_{IN1} = 10.8V$ to $13.2V$
$V_{OUT1} = 5V$
$V_{OUT2} = 3.3V$
$I_{OUT1(MAX)} = 1A$
$I_{OUT2(MAX)} = 1A$
$I_{OUT(MIN)} = 0$
$f_{SW} = 2.25MHz$

Because efficiency is important at both high and low load current, Burst Mode operation will be utilized.

Given the internal oscillator of 2.25MHz, we can calculate the inductors value for about 40% ripple current at maximum V_{IN}:

$$L1 = \left(\frac{5V}{2.25MHz \bullet 0.4A}\right)\left(1-\frac{5V}{13.2V}\right) = 3.4\mu H$$

$$L2 = \left(\frac{3.3V}{2.25MHz \bullet 0.4A}\right)\left(1-\frac{3.3V}{13.2V}\right) = 2.75\mu H$$

Using standard value of 3.3µH and 2.7µH for inductors results in maximum ripple currents of:

$$\Delta I_{L1} = \frac{5V}{2.25MHz \bullet 3.3\mu H}\left(1-\frac{5V}{13.2V}\right) = 0.42A$$

$$\Delta I_{L2} = \frac{3.3V}{2.25MHz \bullet 2.7\mu H}\left(1-\frac{3.3V}{13.2V}\right) = 0.41A$$

C_{OUT} will be selected based on the ESR that is required to satisfy the output voltage ripple requirement and the bulk capacitance needed for loop stability. For this design, a 22µF ceramic capacitor will be used.

C_{IN} should be sized for a maximum current rating of:

$$I_{RMS1} = 1A\left(\frac{5}{13.2}\right)\sqrt{\frac{13.2}{5}-1} = 0.49A$$

$$I_{RMS2} = 1A\left(\frac{3.3}{13.2}\right)\sqrt{\frac{13.2}{3.3}-1} = 0.43A$$

Decoupling the V_{IN1} and V_{IN2} pins with 10µF ceramic capacitors is adequate for most applications.

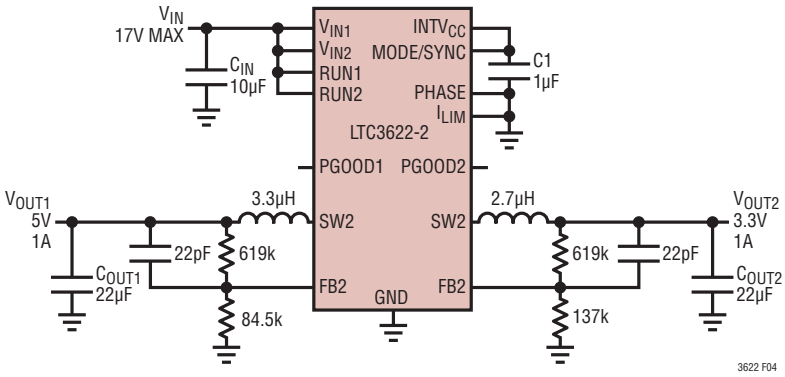
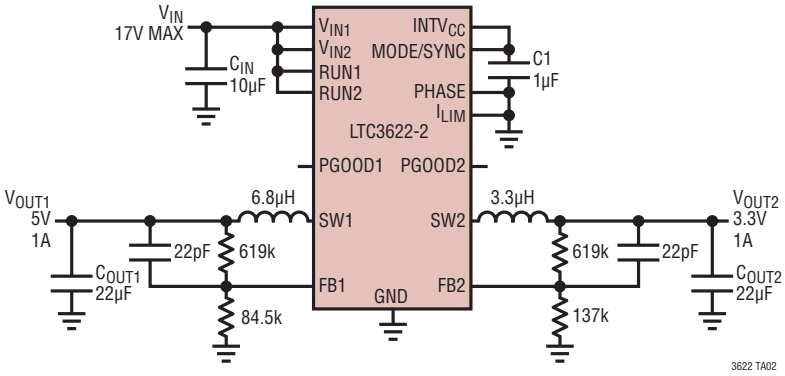


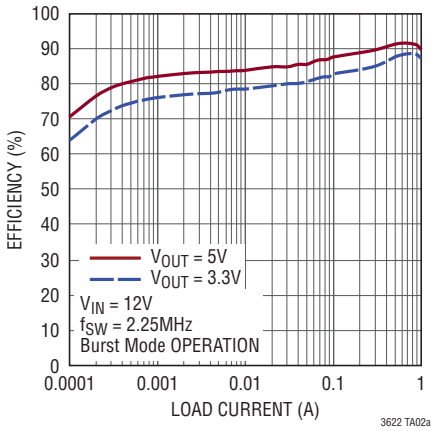
Figure 4. 5V/3.3V V_{OUT} Burst Mode Operation Application

TYPICAL APPLICATIONS

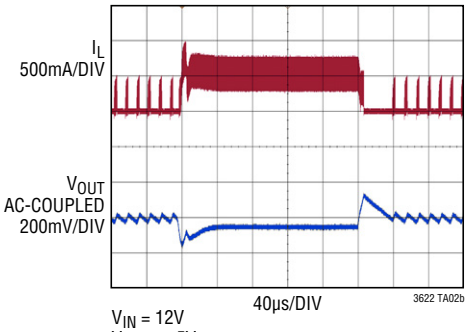
5V/3.3V V_{OUT}, Burst Mode Operation, In-Phase Switching



Efficiency vs Load



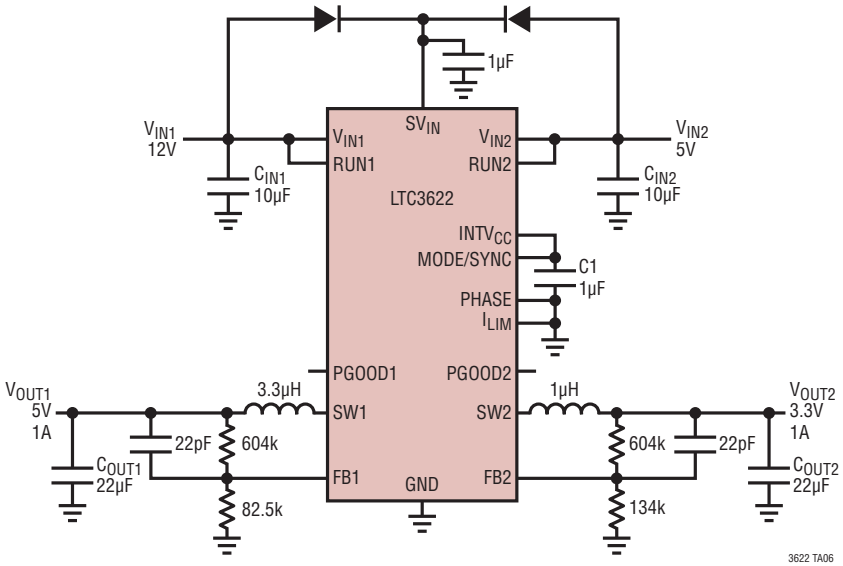
Load Step Waveform



VIN = 12V
VOUT1 = 5V
ILOAD = 5mA → 500mA
Burst Mode OPERATION
fSW = 2.25MHz

TYPICAL APPLICATIONS

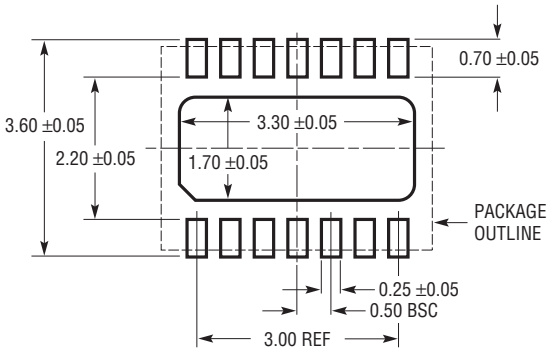
Dual Output Regulators from Multiple Input Sources



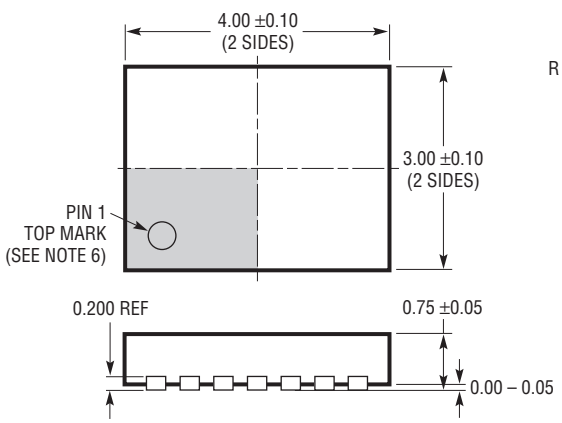
PACKAGE DESCRIPTION

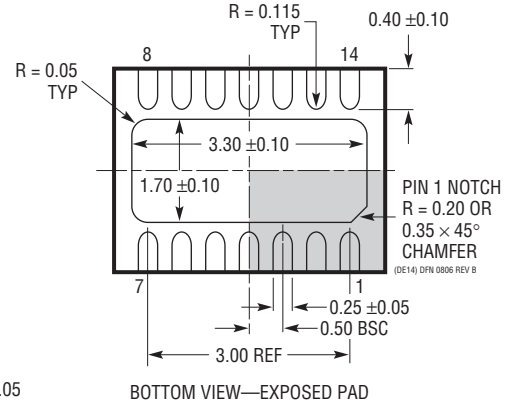
Please refer to http://www.linear.com/product/LTC3622#packaging for the most recent package drawings.

DE Package
14-Lead Plastic DFN (4mm × 3mm)
(Reference LTC DWG # 05-08-1708 Rev B)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED





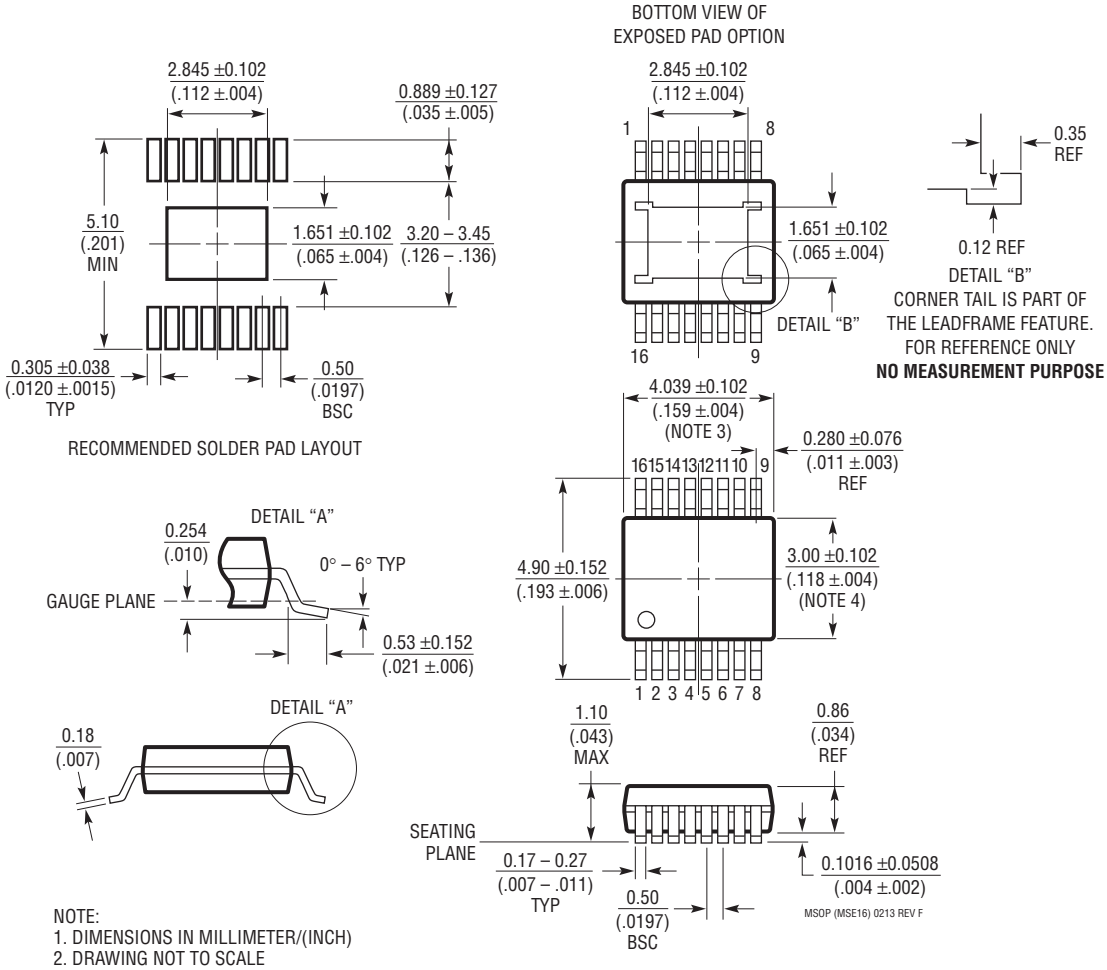
BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING PROPOSED TO BE MADE VARIATION OF VERSION (WGED-3) IN JEDEC PACKAGE OUTLINE MO-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LTC3622#packaging for the most recent package drawings.

MSE Package
16-Lead Plastic MSOP, Exposed Die Pad
(Reference LTC DWG # 05-08-1667 Rev F)



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX
6. EXPOSED PAD DIMENSION DOES INCLUDE MOLD FLASH. MOLD FLASH ON E-PAD SHALL
   NOT EXCEED 0.254mm (.010") PER SIDE.

REVISION HISTORY

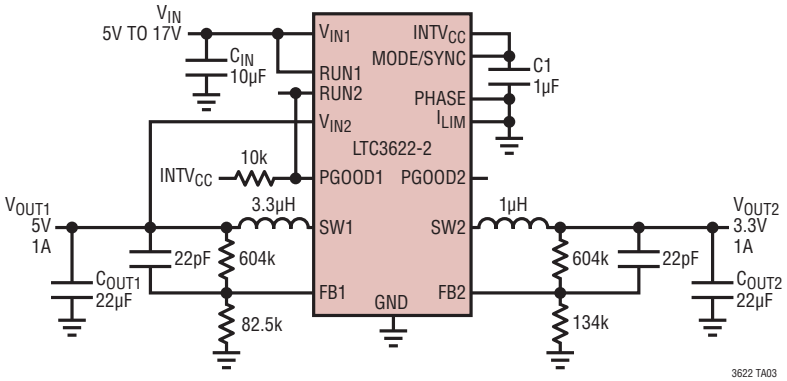
REV	DATE	DESCRIPTION	PAGE NUMBER
A	03/15	Added LTC3622-23/5 Options in Header.	All
		Added LTC3622-23/5 to Options Table.	1
		Added LTC3622-23/5 to Electrical Characteristics.	3
		Added MSOP-16E Package Options.	1, 2, 3, 22
		Added H-Grade Options.	2, 3, 4
		Clarified Pin Functions.	8
		Clarified Table 2.	14
		Added MSOP-16E in #4.	17
B	8/15	Clarified package description to MSE.	2
		Clarified Package Description to MSE, 16-Lead MSOP, exposed die pad.	22
C	6/16	Changed ABS Max Rating of RUN1 and RUN2 pins.	2

LINEAR TECHNOLOGY

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

TYPICAL APPLICATION

5V/3.3V Series Output, Burst Mode Operation



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC3621/ LTC3621-2	1A, 17V, 1/2.25MHz, Synchronous Step-Down Regulator	95% Efficiency, V_{IN}: 2.7V to 17V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 3.5µA, I_{SD} < 1µA, 2mm × 3mm DFN-6, MSOP-8E
LTC3600	1.5A, 15V, 4MHz Synchronous Rail-to-Rail Single Resistor Step-Down Regulator	95% Efficiency, V_{IN}: 4V to 15V, $V_{OUT(MIN)}$ = 0V, I_Q = 700µA, I_{SD} < 1µA, 3mm × 3mm DFN-12, MSOP-12E Packages
LTC3601	15V, 1.5A (I_{OUT}) 4MHz Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 4.5V to 15V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 300µA, I_{SD} < 1µA, 4mm × 4mm QFN-20, MSOP-16E Packages
LTC3603	15V, 2.5A (I_{OUT}) 3MHz Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 4.5V to 15V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 75µA, I_{SD} < 1µA, 4mm × 4mm QFN-20, MSOP-16E Packages
LTC3633A	20V, Dual 3A (I_{OUT}) 4MHz Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 3.6V to 20V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 500µA, I_{SD} < 15µA, 4mm × 5mm QFN-28, TSSOP-28E Packages. A Version Up to 20V_{IN}
LTC3605A	20V, 5A (I_{OUT}) 4MHz Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 4V to 20V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 2mA, I_{SD} < 15µA, 4mm × 4mm QFN-24 Package. A Version Up to 20V_{IN}
LTC3604	15V, 2.5A (I_{OUT}) 4MHz Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 3.6V to 15V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 300µA, I_{SD} < 14µA, 3mm × 3mm QFN-16, MSOP-16E Packages
LTC3624/ LTC3624-2	2A, 17V, 1MHz/2.25MHz Synchronous Step-Down Regulator	95% Efficiency, V_{IN}: 2.7V to 17V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 3.5µA, I_{SD} < 1µA, 3mm × 3mm DFN-8 Package

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