Dual 600mA 15V Monolithic Synchronous Step-Down DC/DC Regulator

FEATURES

- **High Efficiency: Up to 96%**
- **Very Low Quiescent Current: 55µA Total**
- **2.25MHz Constant Frequency Operation**
- **Low Dropout Operation: 100% Duty Cycle**
- **Low-Ripple (Typical 30mV$_{P-P}$) Burst Mode® Operation**
- Peak Current-Mode Control Architecture for Excellent Line and Load Transient Response
- Wide Voltage Input Range: 4.5V to 15V
- 600mA/Channel Rated Output Current
- 0.6V Reference Allows Low Output Voltages
- ±1.5% Output Voltage Accuracy
- Ultralow Shutdown Current: I_Q < 1µA
- Internal Compensation
- Power Good Outputs
- Externally Frequency Synchronization (1MHz to 4MHz)
- Independent Internal Soft-Start for Each Channel
- Small 16-Lead Thermally Enhanced Thin QFN (3mm × 3mm) and MSE Packages

APPLICATIONS

- Dual Lithium-Ion Battery Supplies
- Automotive Applications
- Servers

DESCRIPTION

The LTC®3607 is a 15V dual 600mA monolithic synchronous step-down regulator which has only 55µA quiescent current. Intended for a variety of applications, including dual lithium-ion battery products, it operates from a wide 4.5V to 15V input voltage range. It features a constant 2.25MHz switching frequency, enabling the use of tiny, low cost capacitors and inductors 1mm or less in height. Each output voltage is adjustable from 0.6V to V_{IN}. The internal synchronous power switches provide high efficiency without the need for external Schottky diodes.

A user selectable mode input is provided to allow the user to trade off ripple noise for light load efficiency; Burst Mode operation provides the highest efficiency at light loads, while pulse-skipping mode provides the lowest ripple noise.

To further the maximize battery run time, the P-channel MOSFETs are turned on continuously in dropout (100% duty cycle). In shutdown, the device draws <1µA.

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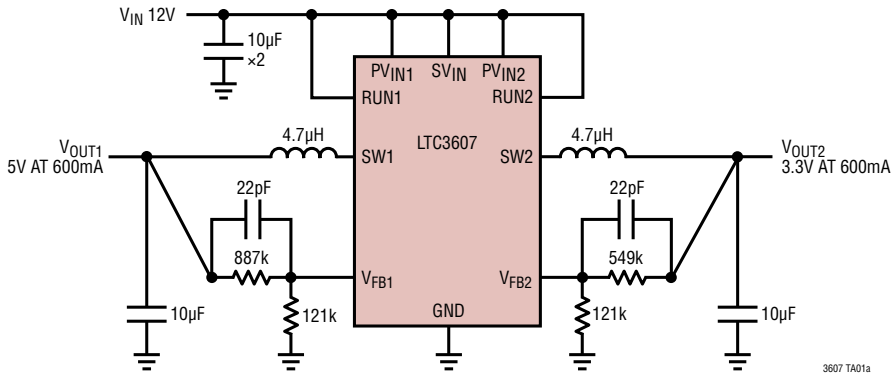
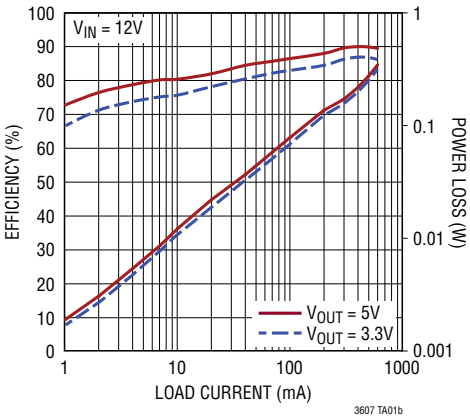
TYPICAL APPLICATION



Efficiency and Power Loss vs Load Current



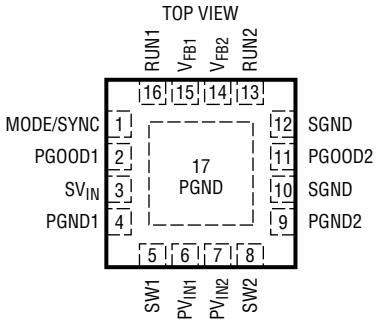
ABSOLUTE MAXIMUM RATINGS

(Note 1)

PV_{IN}, SV_{IN} Voltages ..... –0.3V to 15V
RUN1, RUN2 Voltages ..... –0.3V to (SV_{IN} + 0.3V)
V_{FB1}, V_{FB2} Voltages ..... –0.3V to 3.6V
MODE/SYNC Voltage ..... –0.3V to 3.6V
PGOOD1, PGOOD2 Voltages ..... –0.3V to 15V

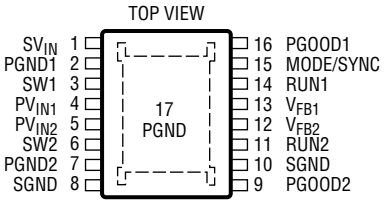
Operating Junction Temperature Range
(Notes 2, 7) ..... –40°C to 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)
MSOP Package ..... 300°C

PIN CONFIGURATION



UD PACKAGE
16-LEAD (3mm × 3mm) PLASTIC QFN

T_{JMAX} = 125°C, θ_{JA} = 68°C/W, θ_{JC} = 7.5°C/W
EXPOSED PAD (PIN 17) IS PGND, MUST BE SOLDERED TO PCB



MSE PACKAGE
16-LEAD PLASTIC MSOP

T_{JMAX} = 125°C, θ_{JA} = 37°C/W, θ_{JC} = 10°C/W
EXPOSED PAD (PIN 17) IS PGND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3607EUD#PBF	LTC3607EUD#TRPBF	LFNB	16-Lead (3mm × 3mm) Plastic QFN	–40°C to 125°C (Note 2)
LTC3607IUD#PBF	LTC3607IUD#TRPBF	LFNB	16-Lead (3mm × 3mm) Plastic QFN	–40°C to 125°C (Note 2)
LTC3607EMSE#PBF	LTC3607EMSE#TRPBF	3607	16-Lead Plastic MSOP	–40°C to 125°C (Note 2)
LTC3607IMSE#PBF	LTC3607IMSE#TRPBF	3607	16-Lead Plastic MSOP	–40°C to 125°C (Note 2)

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 12V, unless otherwise specified. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
SV_{IN}	Operating Voltage Range		●	4.5		15	V
PV_{IN}	Operating Voltage Range		●	4.5		15	V
V_{OUT}	Output Voltage Range			0.6		PV_{IN}	V
V_{FB}	Feedback Voltage (Note 3)		 ●	0.591 0.588	0.6 0.6	0.609 0.612	V V
I_{FB}	Feedback Pin Input Current					30	nA
$\Delta V_{LINE\ REG}$	Reference Voltage Line Regulation	V_{IN} = 4.5V to 15V (Note 3)			0.1	0.15	%/V
$\Delta V_{LOAD\ REG}$	Output Voltage Load Regulation	MODE/SYNC = 0V (Note 3)			0.5		%
I_S	Input DC Supply Current Active Mode Sleep Mode (Both Channels) Sleep Mode (Single Channel) Shutdown	(Note 4) $V_{FB1} = V_{FB2}$ = 0.5V $V_{FB1} = V_{FB2}$ = 0.64V $V_{FB(1\ or\ 2)}$ = 0.64V RUN1 = RUN2 = 0V			 3.2 55 35 0.1	 90 60 1	 mA µA µA µA
f_{OSC}	Oscillator Frequency	$V_{FB1,\ 2}$ = 0.6V	●	1.8	2.25	2.7	MHz
f_{SYNC}	Synchronization Frequency			1.0		4.0	MHz
I_{LIM}	Peak Switch Current Limit	$V_{FB1,\ 2}$ = 0.5V, Duty Cycle < 35%		0.75	1	1.25	A
$R_{DS(ON)}$	Top Switch On-Resistance Bottom Switch On-Resistance	(Note 6) (Note 6)			0.6 0.25		Ω Ω
UVLO	SV_{IN} Undervoltage Lockout Threshold	SV_{IN} Rising			3.4	4.3	V
PGOOD	PGOOD1/2 Overvoltage Threshold	$V_{FB1,\ 2}$ Rising $V_{FB1,\ 2}$ Hysteresis			8.5 –3	11	% %
	PGOOD1/2 Undervoltage Threshold	$V_{FB1,\ 2}$ Ramping Down $V_{FB1,\ 2}$ Hysteresis		–11	–8.5 3		% %
	PGOOD1/2 On-Resistance	Channel 1 or Channel 2 Active RUN1 = RUN2 = 0V			70 700		Ω Ω
t_{PGOOD}	Power Good Blanking Time				64		Cycles
I_{PGOOD}	PGOOD Leakage					1	µA
V_{RUN}	RUN1/2 V_{IL} RUN1/2 V_{IH}		 ●	0.55		 3.0	V V
I_{RUN}	RUN1/2 Leakage Current		●		0.01	1	µA
$V_{MODE/SYNC}$	MODE/SYNC V_{IL} MODE/SYNC V_{IH}		● ●	0.3		 1.0	V V
$t_{SOFTSTART}$	Internal Soft-Start Time	V_{FB} from 10% to 90% Full Scale $PV_{IN1} = PV_{IN2} = SV_{IN}$ = 4.5V			0.35		ms

Note 1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2. The LTC3607 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC3607E is guaranteed to meet specifications from 0°C to 85°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3607I is guaranteed over the full –40°C to 125°C operating junction temperature range.

The junction temperature (T_J) is calculated from the ambient temperature (T_A) and power dissipation (P_D) according to the formula:

$$T_J = T_A + (P_D \bullet \theta_{JA}°C/W)$$

where θ_{JA} is the package thermal impedance. Note that the maximum ambient temperature is consistent with these specifications determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance and other environmental factors.

Note 3. The LTC3607 is tested in a proprietary test mode that connects V_{FB} to the output of the error amplifier to an external servo loop.

Note 4. Dynamic supply current is higher due to the internal gate charge being delivered at the switching frequency.

Note 5. T_J is calculated from the ambient T_A and power dissipation P_D according to the following formula: $T_J = T_A + (PD \bullet \theta_{JA})$.

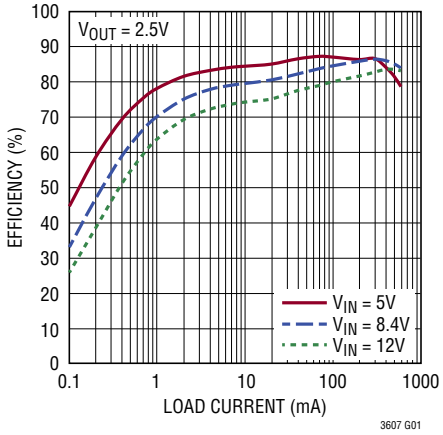
Note 6. The QFN switch on-resistance is guaranteed by correlation to wafer level measurements.

Note 7. This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C when overtemperature protection is active Continuous operation above the specified maximum operating junction temperature may impair device reliability.

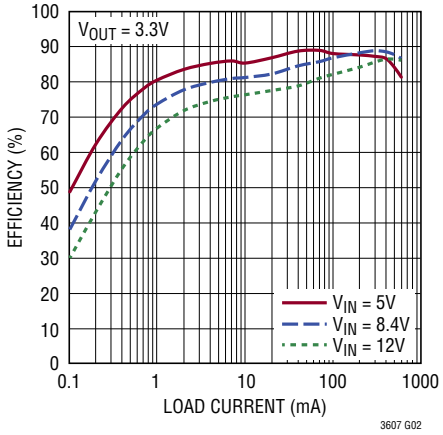
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

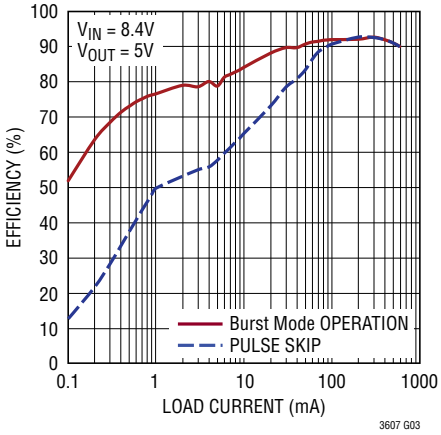
Efficiency vs Load Current Burst Mode Operation



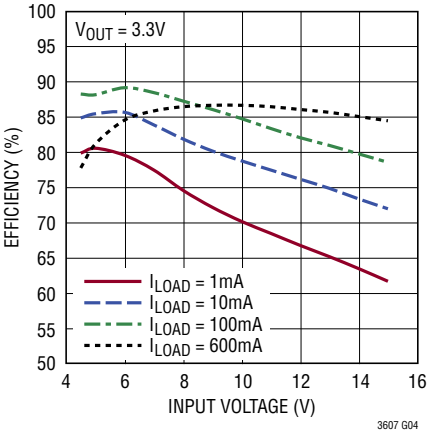
Efficiency vs Load Current Burst Mode Operation



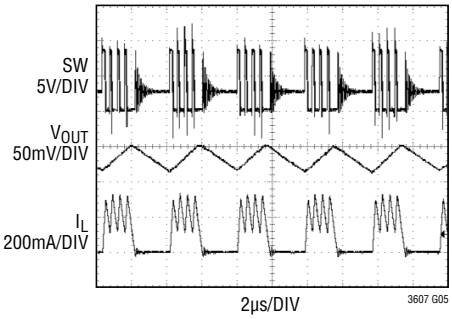
Efficiency vs Load Current



Efficiency vs Input Voltage Burst Mode Operation

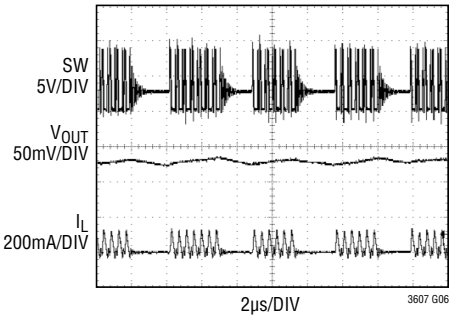


Burst Mode Operation



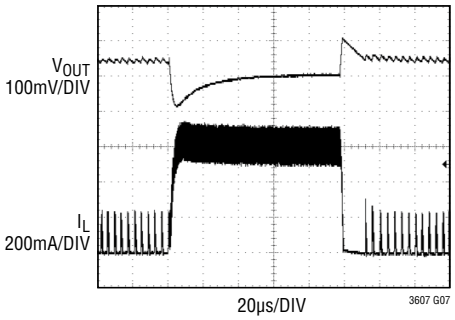
V_{IN} = 8.4V
V_{OUT} = 2.5V
I_{LOAD} = 100mA

Pulse-Skipping Mode



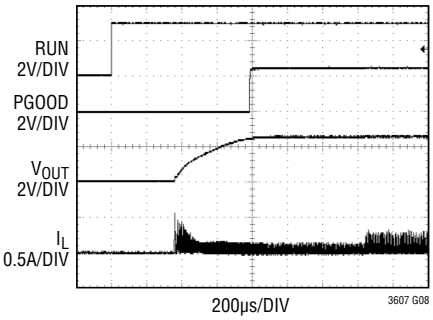
V_{IN} = 8.4V
V_{OUT} = 2.5V
I_{LOAD} = 20mA

Load Step in Burst Mode Operation



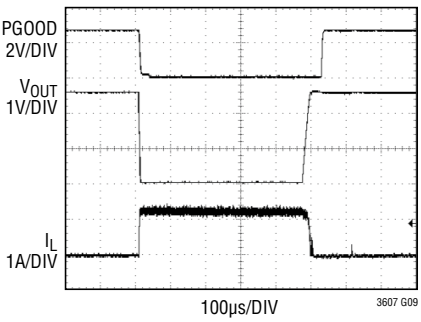
V_{IN} = 8.4V
V_{OUT} = 2.5V
I_{LOAD} = 30mA TO 600mA

Start-Up (Burst Mode Operation)



V_{IN} = 8.4V
V_{OUT} = 2.5V
I_{LOAD} = 20mA

V_{OUT} Short to GND (Burst Mode Operation)

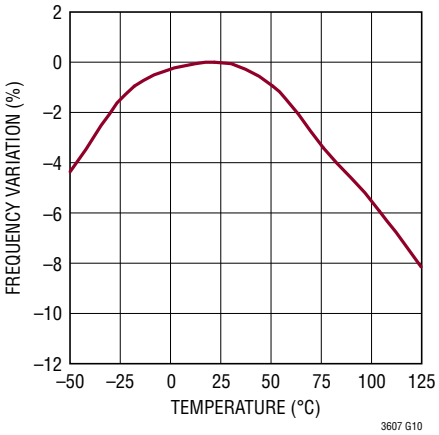


V_{IN} = 8.4V
V_{OUT} = 2.5V
I_{LOAD} = 0A

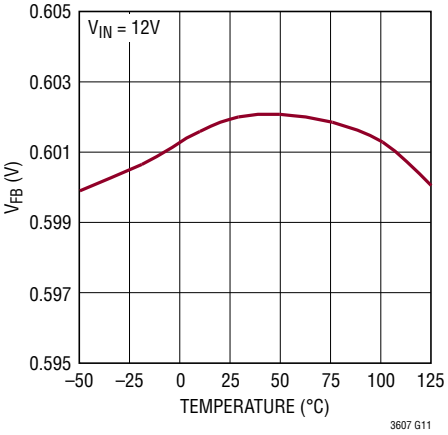
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

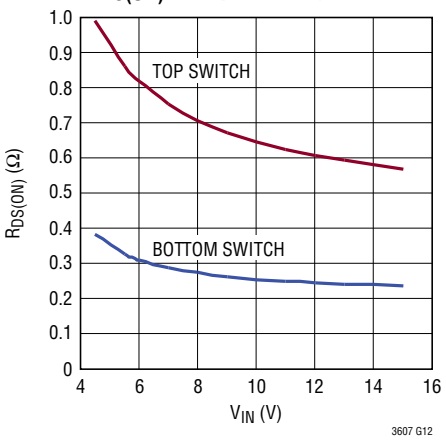
Oscillator Frequency vs Temperature



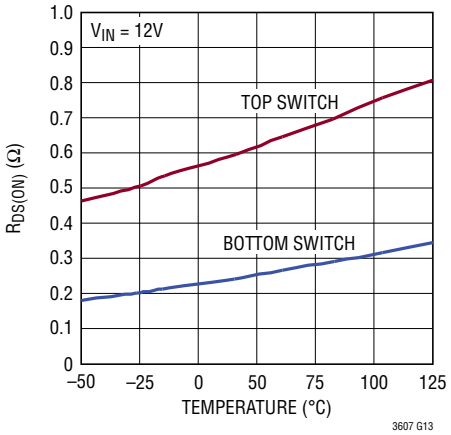
Reference Voltage vs Temperature



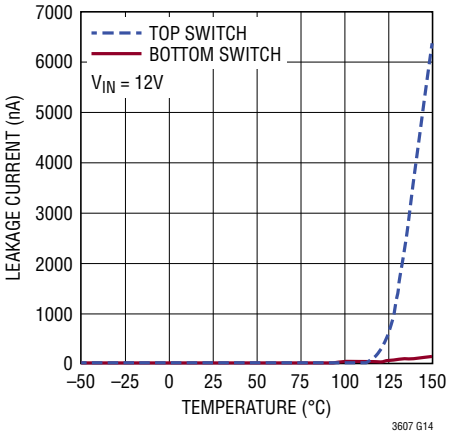
$R_{DS(ON)}$ vs Input Voltage



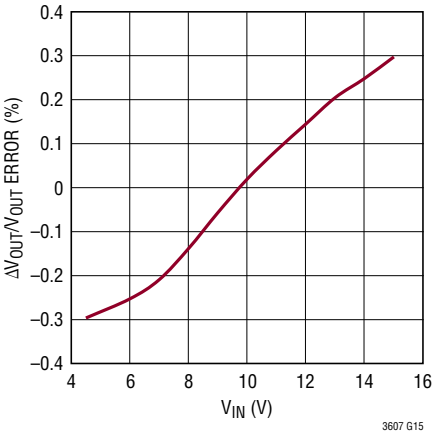
$R_{DS(ON)}$ vs Temperature



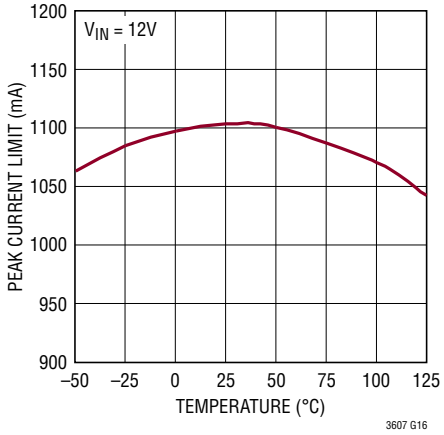
Switch Leakage vs Temperature



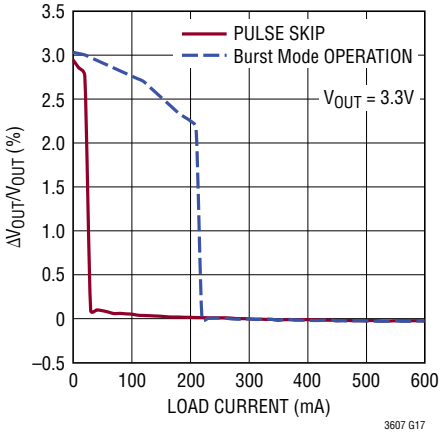
Line Regulation



Peak Current Limit vs Temperature



Load Regulation



PIN FUNCTIONS (QFN/MSE)

PV_{IN1}, PV_{IN2}, SV_{IN} (Pins 6, 7, 3/Pins 4, 5, 1): Main Power Supply. Must be closely decoupled to GND. These inputs may each be powered from different supply voltages. Connect SV_{IN} to either PV_{IN1} or PV_{IN2}, whichever one is higher. For applications where it's not known which $PV_{IN(1 or 2)}$ is higher, connect external diodes between SV_{IN} to both PV_{IN1} and PV_{IN2} to ensure that SV_{IN} is less than a diode drop from the higher of PV_{IN1} or PV_{IN2}.

PGND1, PGND2, SGND, PGND (Pins 4, 9, 10, 12, Exposed Pad Pin 17/Pins 2, 7, 8, 10, Exposed Pad Pin 17): Main Ground. Connect to the (–) terminals of C_{OUT1}, C_{OUT2}, and C_{IN}. The exposed pad must be soldered to PCB ground for electrical contact and rated thermal performance. All SGND and PGND pins must be externally connected to ground.

V_{FB1} (Pin 15/Pin 13): Regulator 1 Output Feedback. Receives the feedback voltage from the external resistor divider across the regulator 1 output. Nominal voltage for this pin is 0.6V.

SW1 (Pin 5/Pin 3): Regulator 1 Switch Node Connection to the Inductor. This pin switches from PV_{IN1} to PGND1.

RUN1 (Pin 16/Pin 14): Regulator 1 Enable. Forcing this pin high (above 3V) enables regulator 1, while forcing it to SGND causes regulator 1 to shut down. It is possible to use a 3.3V source to drive this pin, or tie it to SV_{IN}. An internal soft-start limits the rise time to a minimum of 0.35ms.

PGOOD1 (Pin 2/Pin 16): Regulator 1 Power Good. This common-drain logic output is pulled to SGND when the channel 1 output voltage is not within ±8.5% of regulation.

V_{FB2} (Pin 14/Pin 12): Regulator 2 Output Feedback. Receives the feedback voltage from the external resistor divider across the regulator 2 output. Nominal voltage for this pin is 0.6V.

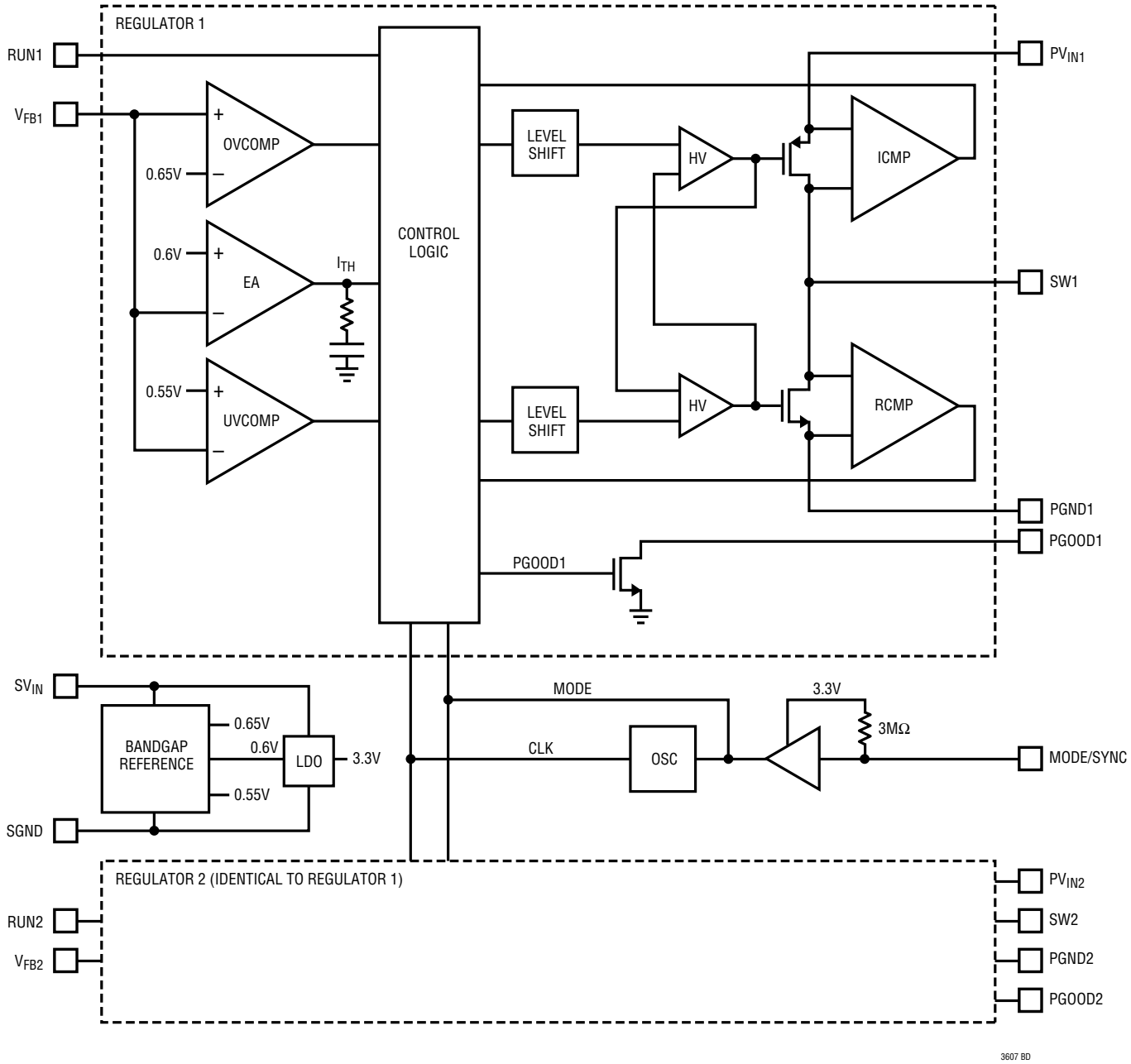
SW2 (Pin 8/Pin 6): Regulator 2 Switch Node Connection to the Inductor. This pin switches from PV_{IN2} to PGND2.

RUN2 (Pin 13/Pin 11): Regulator 2 Enable. Forcing this pin high (above 3.0V) enables regulator 2, while forcing it to SGND causes regulator 2 to shut down. It is possible to use a 3.3V source to drive this pin, or tie it to SV_{IN}. An internal soft-start limits the rise time to a minimum of 0.35ms.

PGOOD2 (Pin 11/Pin 9): Regulator 2 Power Good. This common-drain logic output is pulled to SGND when the channel 2 output voltage is not within ±8.5% of regulation.

MODE/SYNC (Pin 1/Pin 15): Combination Mode Selection and Oscillator Synchronization. This pin controls the light-load behavior of the device. Forcing this pin to SGND selects pulse-skipping mode. Floating this pin or forcing it above 1V selects Burst Mode operation. The internal oscillation frequency can be synchronized to an external oscillator applied to this pin and pulse-skipping mode is automatically selected.

BLOCK DIAGRAM



OPERATION

The LTC3607 uses a constant-frequency, peak current mode architecture. The operating frequency is set at 2.25MHz and can be synchronized to an external oscillator between 1MHz and 4MHz. Both channels share the same clock and run in-phase. To suit a variety of applications, the selectable MODE/SYNC pin allows the user to trade-off ripple for efficiency.

The output voltage is set by an external divider returned to the V_{FB} pins. An error amplifier compares the divided output voltage with a reference voltage of 0.6V and adjusts the peak inductor current accordingly. Overvoltage and undervoltage comparators will pull the independent PGOOD outputs low if the output voltage is not within ±8.5%. The PGOOD outputs will go high 64 clock cycles after achieving regulation and will go low 64 cycles after falling out of regulation.

Whether in Burst Mode or pulse-skipping operation, the overvoltage protection circuit is still enabled when the rest of the regulator is asleep. Hence, if V_{OUT} rises above the overvoltage threshold, the regulator is forced out of sleep.

Main Control Loop

During normal operation, the top power switch (P-channel MOSFET) is turned on at the beginning of a clock cycle when the V_{FB} voltage is below the reference voltage. The current into the inductor and the load increases until the current limit is reached. The switch turns off and energy stored in the inductor flows through the bottom switch (N-channel MOSFET) into the load until the next clock cycle. The peak inductor current is controlled by the internally compensated ITH voltage, which is the output of the error amplifier. This amplifier compares the V_{FB} pin to the 0.6V internal reference. When the load current increases, the V_{FB} voltage decreases slightly below the reference. This decrease causes the error amplifier to increase the ITH voltage until the average inductor current matches the new load current.

The main control loop is shut down by pulling the RUN pin to ground.

Low Current Operation

Two discontinuous-conduction modes (DCMs) are available to control the operation of the LTC3607 at low output currents. Both modes, Burst Mode operation and pulse-skipping, automatically switch from continuous operation to the selected mode when the load current is low.

To optimize efficiency, Burst Mode operation can be selected by floating the MODE/SYNC pin or setting it to 1V or greater. When the load is relatively light, the LTC3607 automatically switches into Burst Mode operation in which the PMOS switch operates intermittently based on load demand with a fixed peak inductor current. By running cycles periodically, the switching losses, which are dominated by the gate charge losses of the power MOSFETs, are minimized. The main control loop is interrupted when the output voltage reaches the desired regulated value. A voltage comparator trips when the ITH voltage drops below an internal clamp voltage, shutting off the switch and reducing the power. The output capacitor and the inductor supply the power to the load until ITH exceeds an internal clamp voltage, turning on the switch and the main control loop, which starts another cycle.

To optimize ripple, pulse-skipping mode can be selected by grounding the MODE/SYNC pin. In the LTC3607, pulse-skipping mode is implemented similarly to Burst Mode operation with the ITH clamp set to a lower internal clamp voltage. This results in lower ripple than in Burst Mode operation with the trade-off being slightly lower efficiency.

Dropout Operation

When the input supply voltage decreases toward the output voltage, the duty cycle increases to 100% which is the dropout condition. In dropout, the PMOS switch is turned on continuously with the output voltage being equal to the input voltage minus the voltage drops across the internal P-channel MOSFET and the inductor.

APPLICATIONS INFORMATION

An important design consideration is that the $R_{DS(ON)}$ of the P-channel switch increases with decreasing input supply voltage (see Typical Performance Characteristics). Therefore, the user should calculate the power dissipation when the LTC3607 is used at 100% duty cycle with low input voltage (see Thermal Considerations in the Applications Information section).

Low/High Supply Operation

The LTC3607 incorporates an undervoltage lockout circuit which shuts down the part when the input voltage drops below about 3.7V to prevent unstable operation.

A general LTC3607 application circuit is shown in Figure 1. External component selection is driven by the load requirement, and begins with the selection of the inductor L. Once the inductor is chosen, C_{IN} and C_{OUT} can be selected.

Inductor Selection

The operating frequency directly effects both the inductor value, and the ripple current. The inductor ripple current ΔI_L decreases with higher frequency and/or inductance and increases with higher V_{IN}:

$$\Delta I_L = \frac{V_{OUT}}{f_O \bullet L} \bullet \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Accepting larger values of ΔI_L allows the use of low inductances, but results in higher output voltage ripple, greater core losses, and lower output current capability. A reasonable starting point for setting ripple current is $\Delta I_L = 0.4 \bullet I_{O(MAX)}$, where $I_{O(MAX)}$ is the maximum rated output current. The largest ripple current ΔI_L occurs at the maximum input voltage. To guarantee that the ripple current stays below a specified maximum, the inductor value should be chosen according to the following equation:

$$L = \frac{V_{OUT}}{f_O \bullet \Delta I_L} \bullet \left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right)$$

The inductor value will also have an effect on Burst Mode operation. The transition from low current operation begins when the peak inductor current falls below a level set by the burst clamp. Lower inductor values result in higher ripple current which causes this transition to occur at lower load currents. This causes a dip in efficiency in the upper range of low current operation. In Burst Mode operation, lower inductance values will cause the burst frequency to increase.

Inductor Core Selection

Different core materials and shapes will change the size/current and price/current relationship of an inductor. Toroid or shielded pot cores in ferrite or permalloy materials are small and don't radiate much energy, but generally cost more than powdered iron core inductors with similar electrical characteristics. The choice of which style inductor to use often depends more on the price vs size requirements and any radiated field/EMI requirements than on what the LTC3607 requires to operate. Table 1 shows the websites of several surface mount inductor manufacturers.

Table 1. Inductor Manufacturer

Coilcraft	http://www.coilcraft.com/powersel_lowl.html
Cooper Bussmann	http://www.cooperindustries.com/content/public/en/bussmann/electronics/products/coiltronics_inductorandtransformermagnetics.html
Würth Electronic	http://katalog.we-online.com/en/pbs/browse/Power-Magnetics/Speicherdrosseln
Murata	http://www.murata.com/products/inductor/index.html
TDK	http://www.tdk.co.jp/tefe02/coil.htm
Vishay	http://www.vishay.com/inductors/power-inductors/
Sumida	http://www.sumida.com/en/products/power_main.php

APPLICATIONS INFORMATION

Input Capacitor (C_{IN}) Selection

In continuous mode, the input current of the converter is a square wave with a duty cycle of approximately V_{OUT}/V_{IN}. To prevent large voltage transients, a low equivalent series resistance (ESR) input capacitor sized for the maximum RMS current must be used. The maximum RMS capacitor current is given by:

$$I_{RMS} \approx I_{OUT(MAX)} \frac{\sqrt{V_{OUT}(V_{IN}-V_{OUT})}}{V_{IN}}$$

where the maximum average output current I_{MAX} equals the peak current minus half the peak-to-peak ripple current, $I_{MAX} = I_{LIM} – \Delta I_L/2$.

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst-case is commonly used to design because even significant deviations do not offer much relief. Note that capacitor manufacturer's ripple current ratings are often based on only 2000 hours lifetime. This makes it advisable to further derate the capacitor, or choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet the size or height requirements of the design. An additional 0.1µF to 1µF ceramic capacitor is also recommended on V_{IN} for high frequency decoupling, when not using an all ceramic capacitor solution.

Output Capacitor (C_{OUT}) Selection

The selection of C_{OUT} is driven by the required ESR to minimize voltage ripple and load step transients. Typically, once the ESR requirement is satisfied, the capacitance is adequate for filtering. The output ripple (ΔV_{OUT}) is determined by:

$$\Delta V_{OUT} \approx \Delta I_L \left(ESR + \frac{1}{8 f_O C_{OUT}} \right)$$

where f_O = operating frequency, C_{OUT} = output capacitance and ΔI_L = ripple current in the inductor. The output ripple is highest at maximum input voltage since ΔI_L increases with input voltage. With ΔI_L = 240mA the output ripple will be less than 100mV at maximum V_{IN} and f_O = 2.25MHz with: $ESR_{COUT} < 150m\Omega$.

Once the ESR requirements for C_{OUT} have been met, the RMS current rating generally far exceeds the $I_{RIPPLE(P-P)}$ requirement, except for an all ceramic solution.

Since the ESR of a ceramic capacitor is so low, the input and output capacitor must instead fulfill a charge storage requirement. During a load step, the output capacitor must instantaneously supply the current to support the load until the feedback loop raises the switch current enough to support the load. The time required for the feedback loop to respond is dependent on the compensation and the output capacitor size. Typically, 3 to 4 cycles are required to respond to a load step, but only in the first cycle does the output drop linearly. The output droop, V_{DROOP}, is usually about five times the linear drop of the first cycle. Thus, a good place to start is with the output capacitor size of approximately:

$$C_{OUT} \approx 5 \frac{\Delta I_{OUT}}{f_O \bullet V_{DROOP}}$$

Though this equation provides a good approximation, more capacitance may be required depending on the duty cycle and load step requirements.

Ceramic Input and Output Capacitors

High value, low cost ceramic capacitors are available in small case sizes. Their high ripple current, high voltage rating, and low ESR make them ideal for switching regulator applications. However, due to the self-resonant and high-Q characteristics of some types of ceramic capacitors, care must be taken when these capacitors are used at the input.

When a ceramic capacitor is used at the input and the power is being supplied through long wires, such as from a wall adapter, a load step at the output can induce ringing at the V_{IN} pin. At best, this ringing can couple to the output and be mistaken as loop instability. At worst, the ringing at the input can be large enough to damage the part. For a more detailed discussion, refer to Application Note 88.

APPLICATIONS INFORMATION

Setting the Output Voltage

The LTC3607 develops a 0.6V reference voltage between the feedback pins, V_{FB1} and V_{FB2}, and ground as shown in Figure 1. The output voltage is set by a resistive divider according to the following formula:

$$V_{OUT} = 0.6V\left(1+\frac{R1}{R2}\right)$$

Keeping the current small (<5μA) in these resistors maximizes efficiency, but making them too small may allow stray capacitance to cause noise problems and reduce the phase margin of the error amp loop.

To improve the frequency response, a feed-forward capacitor C_{FF} may also be used. Great care should be taken to route the V_{FB} traces away from noise sources, such as the inductor or the SW traces.

For continuous mode operation with a fixed maximum input voltage, the minimum value that the output voltage can be reduced to is set by the minimum on-time, which is approximately 65ns. For fixed frequency (2.25MHz) applications, the relation between minimum output voltage and maximum input voltage is:

$$V_{OUT(MIN)} = 0.14625 \bullet V_{IN(MAX)}$$

If the output voltage drops below that limit, the output will still regulate, but the part will skip cycles.

Power Good Outputs

The PGOOD1 and PGOOD2 are open-drain outputs which pull low when a regulator is out of regulation. When the output voltage is within ±8.5% of regulation, a timer is started which releases the relevant PGOOD pin after 64 clock cycles.

Mode Selection & Frequency Synchronization

The MODE/SYNC pin is a multipurpose pin which provides mode selection and frequency synchronization. Floating this pin or connecting it to a 3.3V source enables Burst Mode operation, which provides optimal light load efficiency at the cost of a slightly higher output voltage ripple. When this pin is connected to ground, pulse-skipping operation is selected. This mode provides the lowest output ripple, at the cost of slightly lower light load efficiency.

The LTC3607 can also be synchronized to another LTC3607 by the MODE/SYNC pin. During synchronization, the mode is set to pulse-skipping and the top switch turn-on is synchronized to the rising edge of the external clock. Pulse-skipping mode is also the default mode during start-up.

Checking Transient Response

The regulator loop response can be checked by looking at the load transient response. Switching regulators take several cycles to respond to a step in load current. When a load step occurs, V_{OUT} immediately shifts by an amount equal to ΔI_{LOAD} • ESR, where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT} generating a feedback error signal used by the regulator to return V_{OUT} to its steady-state value. During this recovery time, V_{OUT} can be monitored for overshoot or ringing that would indicate a stability problem.

The initial output voltage step may not be within the bandwidth of the feedback loop, so the standard second order overshoot/DC ratio cannot be used to determine phase margin. In addition, a feed-forward capacitor can be added to improve the high frequency response, as shown in Figure 1. Capacitors C1 and C2 provide phase lead by creating high frequency zeros with R1 and R3 respectively, which improve the phase margin.

The output voltage settling behavior is related to the stability of the closed-loop system and will demonstrate the actual overall supply performance.

In some applications, a more severe transient can be caused by switching in loads with large (>1μF) input capacitors. The discharged input capacitors are effectively put in parallel with C_{OUT}, causing a rapid drop in V_{OUT}. No regulator can deliver enough current to prevent this problem if the switch connecting the load has low resistance and is driven quickly. The solution is to limit the turn-on speed of the load switch driver. A Hot Swap™ controller is designed specifically for this purpose and usually incorporates current limiting, short-circuit protection, and soft-starting.

APPLICATIONS INFORMATION

Efficiency Considerations

The percent efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Percent efficiency can be expressed as:

%Efficiency = 100% - (L1 + L2 + L3 + ...)

where L1, L2, etc. are the individual losses as a percentage of input power. Although all dissipative elements in the circuit produce losses, four main sources usually account for most of the losses in LTC3607 circuits: 1) V_{IN} quiescent current, 2) switching losses, 3) I^2R losses, 4) other losses.

1) The V_{IN} current is the DC supply current given in the Electrical Characteristics which excludes MOSFET driver and control currents. V_{IN} current results in a small loss that increases with V_{IN}, even at no load.

2) The switching current is the sum of the MOSFET driver and control currents. The MOSFET driver current results from switching the gate capacitance of the power MOSFETs. Each time a MOSFET gate is switched from low to high to low again, a packet of charge dQ moves from V_{IN} to ground. The resulting dQ/dt is a current out of V_{IN} that is typically much larger than the DC bias current. In continuous mode, $I_{GATECHG} = f_O(Q_T + Q_B)$, where Q_T and Q_B are the gate charges of the internal top and bottom MOSFET switches. The gate charge losses are proportional to V_{IN} and thus their effects will be more pronounced at higher supply voltages.

3) I^2R losses are calculated from the DC resistances of the internal switches, R_{SW}, and external inductor, R_L. In continuous mode, the average output current flows through inductor L, but is *chopped* between the internal top and bottom switches. Thus, the series resistance looking into the SW pin is a function of both top and bottom MOSFET $R_{DS(ON)}$ and the duty cycle (D) as follows:

$$R_{SW} = (R_{DS(ON)TOP})(D) + (R_{DS(ON)BOT})(1 - D)$$

The $R_{DS(ON)}$ for both the top and bottom MOSFETs can be obtained from the Typical Performance Characteristics curves. Thus, to obtain I^2R losses:

$$I^2R \text{ losses} = I_{OUT}{}^2(R_{SW} + R_L)$$

4) Other *hidden* losses such as copper trace and internal battery resistances can account for additional efficiency degradations in portable systems. It is very important to include these *system* level losses in the design of a system. The internal battery and fuse resistance losses can be minimized by making sure that C_{IN} has adequate charge storage and very low ESR at the switching frequency. Other losses including diode conduction losses during dead-time and inductor core losses generally account for less than 2% total additional loss.

Thermal Considerations

In a majority of applications, the LTC3607 does not dissipate much heat due to its high efficiency. However, in applications where the LTC3607 is running at high ambient temperature with low supply voltage and high duty cycles, such as in dropout, the heat dissipated may exceed the maximum junction temperature of the part. If the junction temperature reaches approximately 150°C, both power switches for each channel will be turned off and the SW nodes will become high impedance.

To prevent the LTC3607 from exceeding the maximum junction temperature, the user will need to do some thermal analysis. The goal of the thermal analysis is to determine whether the power dissipated exceeds the maximum junction temperature of the part. The temperature rise is given by:

$$T_{RISE} = P_D \bullet \theta_{JA}$$

where P_D is the power dissipated by the regulator and θ_{JA} is the thermal resistance from the junction of the die to the ambient temperature.

The junction temperature, T_J, is given by:

$$T_J = T_{RISE} + T_{AMBIENT}$$

APPLICATIONS INFORMATION

As an example, consider the case when the LTC3607 is in dropout on both channels at an input voltage of 5V with a load current of 600mA and an ambient temperature of 25°C. From the Typical Performance Characteristics graph of Switch Resistance, the $R_{DS(ON)}$ resistance of the main switch is 0.9Ω. Therefore, power dissipated by each channel is:

$$P_D = I^2 \bullet R_{DS(ON)} = 324mW$$

Running the two regulator channels under the same conditions will result in a total power dissipation of 0.648W. The MSE package junction-to-ambient thermal resistance, θ_{JA}, is 37°C/W. Therefore, the junction temperature of the regulator operating in a 25°C ambient temperature is approximately:

$$T_J = 0.648W \bullet 37°C/W + 25°C = 49°C$$

Design Example

As a design example, consider using the LTC3607 in a portable application with a dual lithium-ion battery. The battery provides a V_{IN} = 5.6V to 8.4V. The loads require a maximum of 600mA in active mode and 2mA in standby mode. The output voltages are V_{OUT1} = 3.3V and V_{OUT2} = 2.5V. Since the load still needs power in standby, Burst Mode operation is selected for good light load efficiency.

First, calculate the inductor values for about 240mA ripple current at maximum V_{IN}:

$$L1 = \frac{3.3V}{2.25MHz \bullet 240mA} \bullet \left(1 - \frac{3.3V}{8.4V}\right) = 3.7\mu H$$

Choosing the closest standardized inductor value of 3.3µH results in a maximum ripple current of:

$$\Delta I_{L1} = \frac{3.3V}{2.25MHz \bullet 3.3\mu H} \bullet \left(1 - \frac{3.3V}{8.4V}\right) = 270mA$$

The same calculations for L2 result in a standard inductor value of 3.3µH and a maximum current ripple of 236mA.

For cost reasons, a ceramic capacitor will be used. C_{OUT} selection is then based on load step droop instead of ESR requirements. For a 5% output droop:

$$C_{OUT1} \approx 5 \bullet \frac{600mA}{2.25MHz \bullet (5\% \bullet 3.3V)} = 8.1\,\mu F$$

$$C_{OUT2} \approx 5 \bullet \frac{600mA}{2.25MHz \bullet (5\% \bullet 2.5V)} = 10.7\,\mu F$$

For both outputs, a close standard value is 10µF. Since the output impedance of a lithium-ion battery is very low, each C_{IN} is chosen to be 10µF also.

The output voltages can now be programmed by choosing the values of R1 thru R4. To maintain high efficiency, the current in these resistors should be kept small. Choosing 5µA with the 0.6V feedback voltage makes R2 and R4 ~ 120k. Close standard 1% resistor values is 121k and then R1 and R3 are 549k and 383k, respectively.

The PGOOD pins are common drain outputs, thus requiring pull-up resistors. Two 100k resistors are used for adequate speed.

Figure 1 shows the complete schematic for this design example. The specific passive components chosen allow for a 1mm height power supply that maintains a high efficiency across load.

Board Layout Considerations

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the LTC3607. These items are also illustrated graphically in the layout diagram of Figure 2. Check the following in your layout:

1. Do the input capacitors C_{IN} connect to PV_{IN1}, PV_{IN2}, PGND1, and PGND2 as closely as possible? These capacitors provides the AC current to the internal power MOSFETs and their drivers.
2. Are C_{OUT} and L closely connected? The (–) plate of C_{OUT} returns current to GND and the (–) plate of C_{IN}.

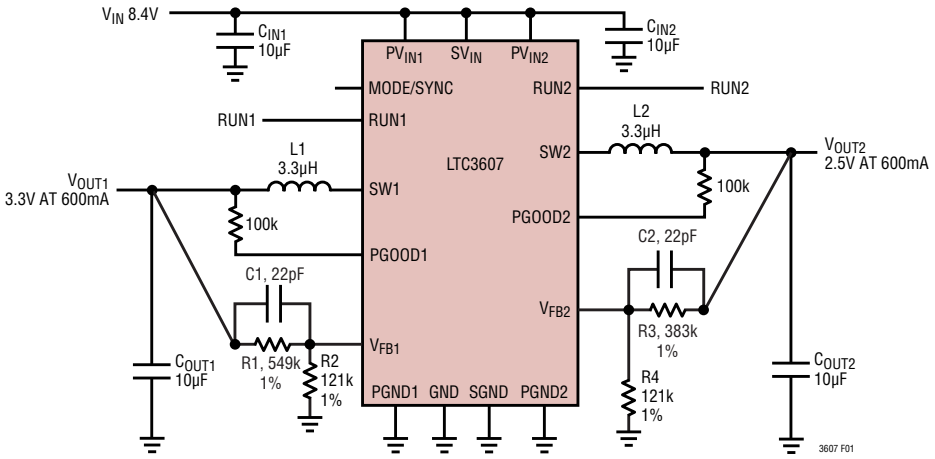
APPLICATIONS INFORMATION

3. The resistor divider formed by R1 and R2 must be connected between the (+) plate of C_{OUT} and a ground sense line terminated near GND (exposed pad). The feedback signals V_{FB1} and V_{FB2} should be routed away from noisy components and traces (such as the SW lines) and their traces should be minimized.

4. Keep sensitive components away from the SW pins. The feedback resistors R1 to R4 should be routed away from the SW traces and the inductors.

5. A ground plane is preferred, but if not available keep the signal and power grounds segregated with small signal components returning to the GND pin at one point. Additionally, the two grounds should not share the high current paths of C_{IN} or C_{OUT}.

6. Flood all unused areas on all layers with copper. Flooding with copper will reduce the temperature rise of power components. These copper areas should be connected to V_{IN} or GND. Refer to Figures 2 and 3 for board layout examples.



C1: TDK C2012X5R1C106K/1.25
C_{OUT1}, C_{OUT2}: C2012X5R0J106K/1.25
L1, L2: WÜRTH ELEKTRONIK 744025003

Figure 1. Design Example Circuit

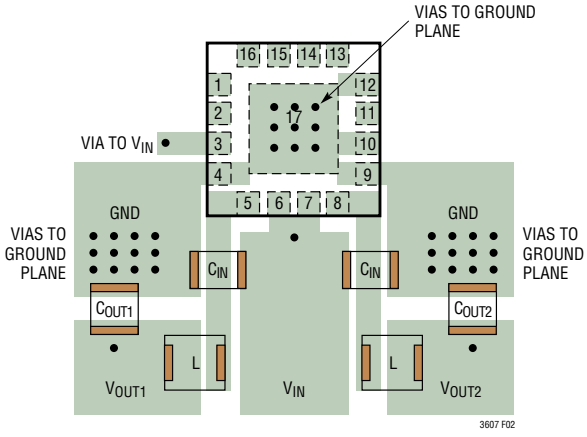


Figure 2. Example of Power Component Layout for QFN Package

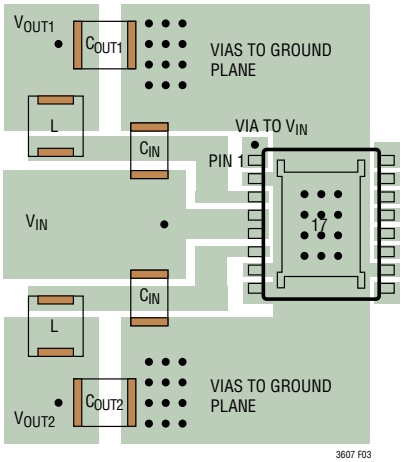
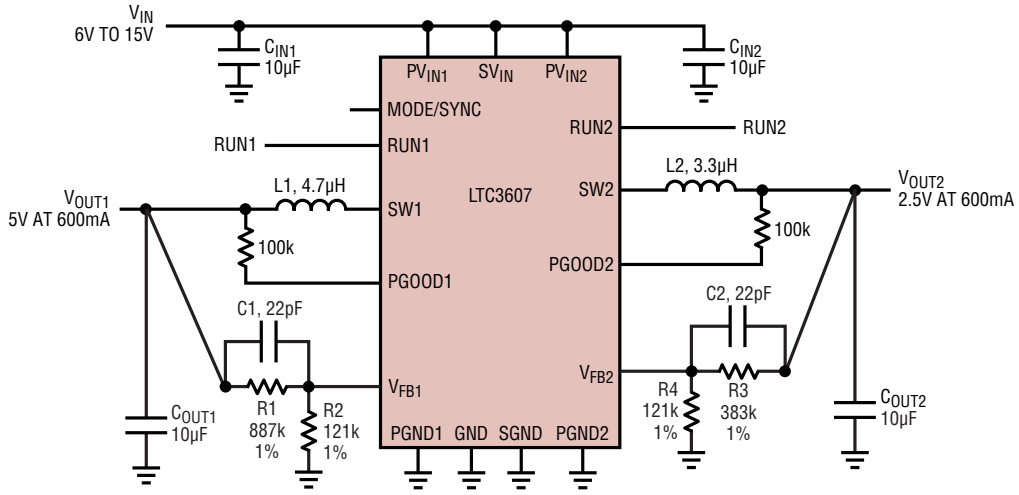


Figure 3. Example of Power Component Layout for MSE Package

TYPICAL APPLICATIONS

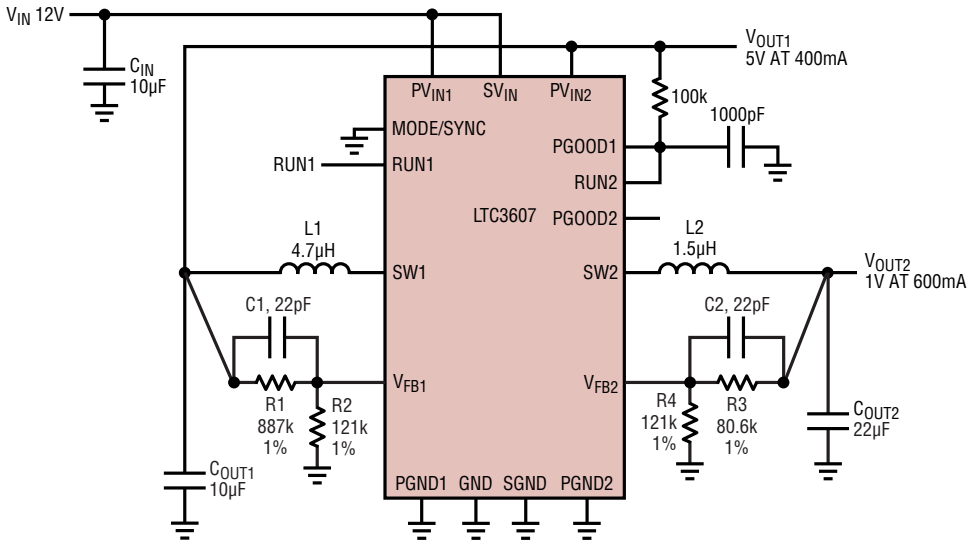
5V/2.5V 2.25MHz Buck Regulator



L1: SUMIDA CDRH3D16/HPNP-4R7NC
L2: SUMIDA CDRH3D16/HPNP-3R3NC

3607 TA02

Low Output Voltage and Main Supply

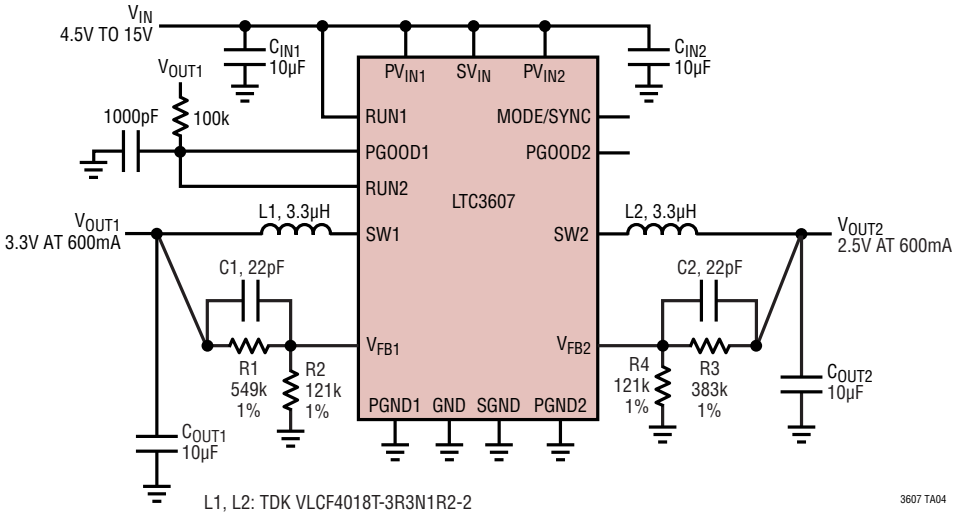


L1: VISHAY IHLP1616BZER4R7M11
L2: VISHAY IHLP1616ABER1R5M11

3607 TA03

TYPICAL APPLICATIONS

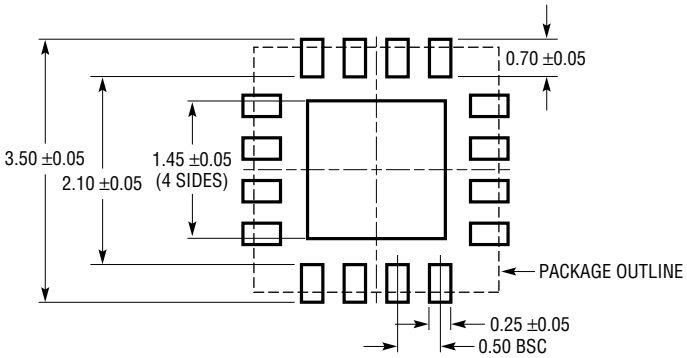
Sequenced Power Supplies



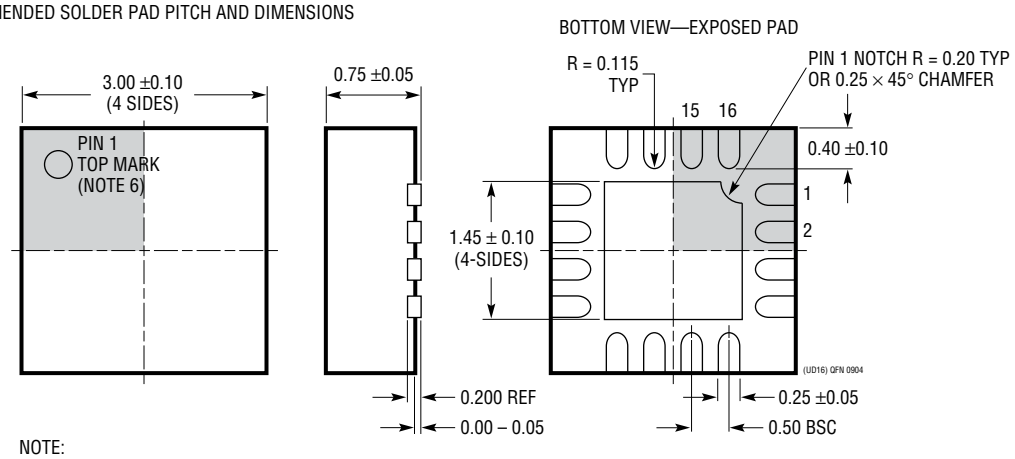
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

UD Package
16-Lead Plastic QFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1691 Rev Ø)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS

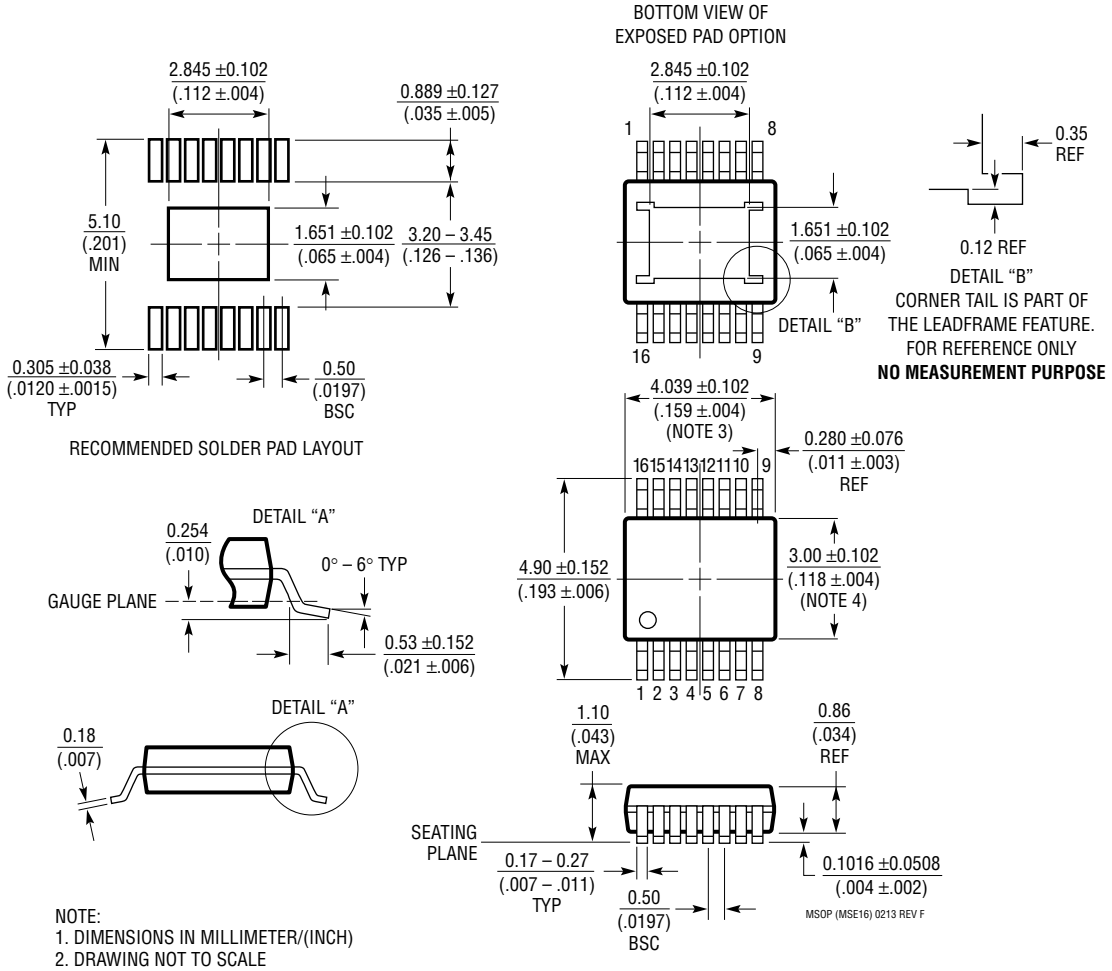


NOTE:
1. DRAWING CONFORMS TO JEDEC PACKAGE OUTLINE MO-220 VARIATION (WEED-2)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

MSE Package
16-Lead Plastic MSOP, Exposed Die Pad
(Reference LTC DWG # 05-08-1667 Rev F)



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX
6. EXPOSED PAD DIMENSION DOES INCLUDE MOLD FLASH. MOLD FLASH ON E-PAD SHALL
   NOT EXCEED 0.254mm (.010") PER SIDE.

REVISION HISTORY

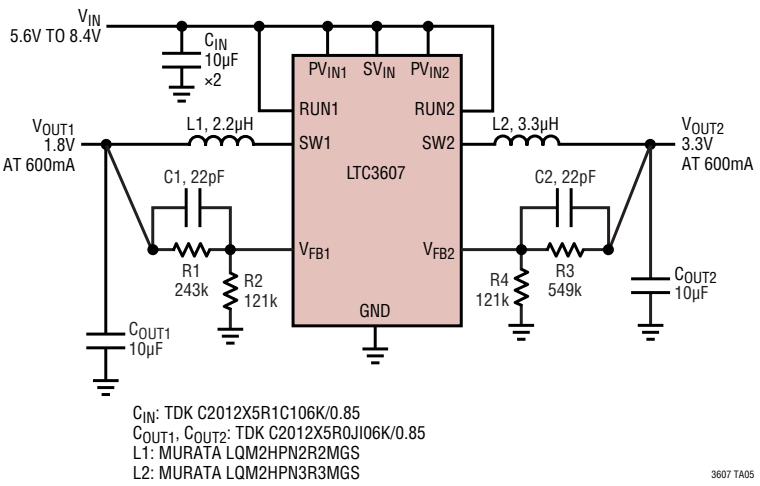
REV	DATE	DESCRIPTION	PAGE NUMBER
A	11/13	Clarified RUN 1/2 voltages	2
		Clarified Electrical table	3
		Clarified Pin Function descriptions	6
B	8/14	Clarified ripple feature	1
		Clarified Electrical Characteristics table	3
		Clarified Output Voltage formula	11

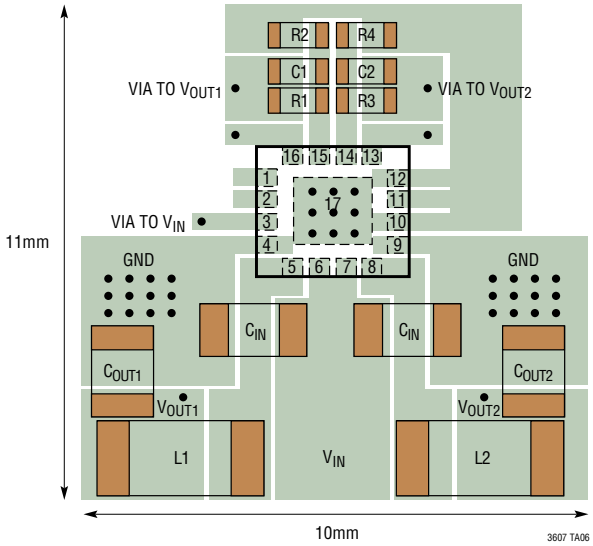
LINEAR TECHNOLOGY

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

TYPICAL APPLICATION

1mm Height, 1.8V/3.3V Buck Regulator Using Chip Inductors





RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC3601	15V, 1.5A (I_{OUT}), 4MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 4.5V to 15V, 3mm × 3mm QFN-16, MSOP-16E
LTC3603	15V, 2.5A (I_{OUT}), 3MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 4.5V to 15V, 4mm × 4mm QFN-20, MSOP-16E
LTC3633	15V, Dual 3A (I_{OUT}), 4MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 3.6V to 15V, 4mm × 5mm QFN-28, TSSOP-28E
LTC3605	15V, 5A (I_{OUT}), 4MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 4V to 15V, 4mm × 4mm QFN-24
LTC3604	15V, 2.5A (I_{OUT}), 4MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 3.6V to 15V, 3mm × 3mm QFN-16, MSOP-16E
LTC3417A-2	5.5V, Dual 1.5A/1A, 4MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN} = 2.3V, 3mm × 5mm DFN-16, TSSOP-16E
LTC3407A/-2	5.5V, Dual 600mA/600mA 1.5MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN} = 2.5V, 3mm × 3mm DFN-10, MS-10E
LTC3419/-1	5.5V, Dual 600mA/600mA 2.25MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN} = 2.5V, 3mm × 3mm DFN-10, MS-10
LTC3548A-1/-2	5.5V, Dual 400mA and 800mA I_{OUT}, 2.25MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN} = 2.5V, 3mm × 3mm DFN-10, MS-10E
LTC3547/ LTC3547B	5.5V, Dual Monolithic 300mA, 2.25MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN} = 2.5V, I_Q = 40µA, I_{SD} < 1µA, 3mm × 2mm DFN-8
LTC3621	17V, 1A (I_{OUT}), 2.25MHz Synchronous Step-Down DC/DC Converter with 3.5µA I_Q	95% Efficiency, V_{IN} = 2.7V to 17V, 3mm × 2mm DFN-6, MS-8E

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