Switching Power Manager with USB On-the-Go + Triple Step-Down DC/DCs

FEATURES

- **Bidirectional Switching Regulator with Bat-Track™ Adaptive Output Control Provides Efficient Charging and a 5V Output for USB On-The-Go**
- **Bat-Track Control of External High Voltage Step-Down Switching Regulator**
- **Overvoltage Protection Guards Against Damage**
- **Instant-On Operation with Discharged Battery**
- Triple Step-Down Switching Regulators with I^2C Adjustable Outputs (1A/400mA/400mA I_{OUT})
- 180mΩ Internal Ideal Diode + External Ideal Diode Controller Powers the Load in Battery Mode
- Li-Ion/Polymer Battery Charger (1.5A Max I_{CHG})
- Battery Float Voltage: 4.2V (LTC3576), 4.1V (LTC3576-1)
- Compact (4mm × 6mm × 0.75mm) 38-Pin QFN Package

APPLICATIONS

- HDD-Based Media Players
- GPS, PDAs, Digital Cameras, Smart Phones
- Automotive Compatible Portable Electronics

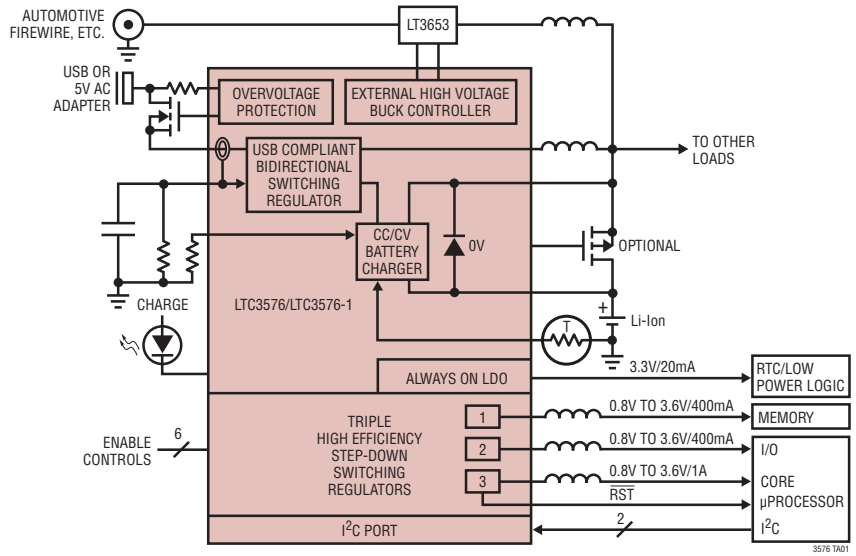
DESCRIPTION

The LTC®3576/LTC3576-1 are highly integrated power management and battery charger ICs for Li-Ion/Polymer battery applications. They each include a high efficiency, bidirectional switching PowerPath™ manager with automatic load prioritization, a battery charger, an ideal diode, a controller for an external high voltage switching regulator and three general purpose step-down switching regulators with I^2C adjustable output voltages. The internal switching regulators automatically limit input current for USB compatibility and can also generate 5V at 500mA for USB on-the-go applications when powered from the battery. Both the USB and external switching regulator power paths feature Bat-Track optimized charging to provide maximum power to the application from supplies as high as 38V. An overvoltage circuit protects the LTC3576/LTC3576-1 from damage due to high voltage on the V_{BUS} or WALL pins with just two external components. The LTC3576/LTC3576-1 are available in a low profile 38-pin (4mm × 6mm × 0.75mm) QFN package.

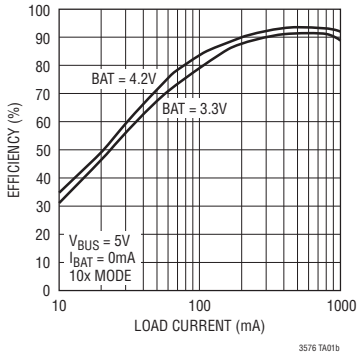
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TYPICAL APPLICATION

High Efficiency PowerPath Manager with Overvoltage Protection and Triple Step-Down Regulator



PowerPath Switching Regulator Efficiency to System Load (P_{VOUT}/P_{VBUS})

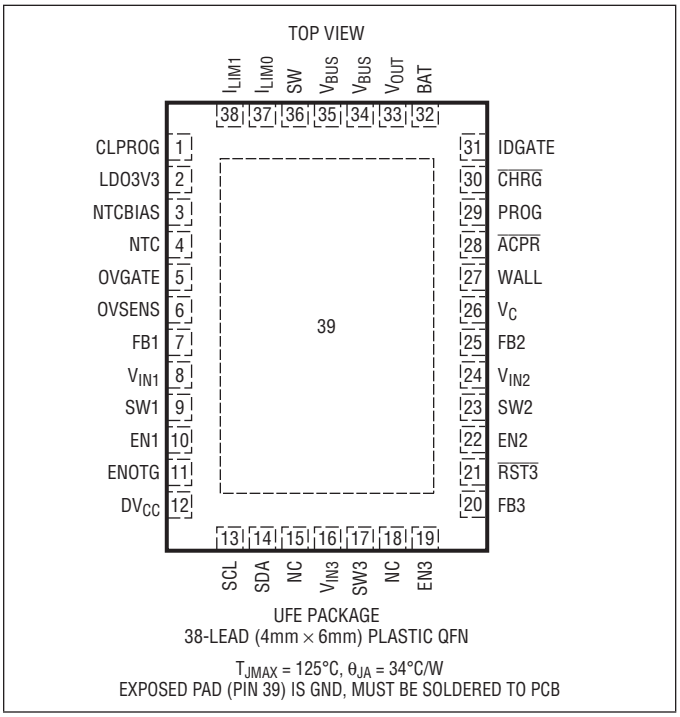


ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2, 3)

V_{BUS}, WALL (Transient) t < 1ms, Duty Cycle < 1% ..... –0.3V to 7V
V_{BUS}, WALL (Static), BAT, V_{IN1}, V_{IN2}, V_{IN3}, V_{OUT}, ENOTG, NTC, SDA, SCL, DV_{CC}, $\overline{RST3}$, $\overline{CHRG}$ ..... –0.3V to 6V
I_{LIM0}, I_{ILIM1} ..... –0.3V to Max(V_{BUS}, V_{OUT}, BAT) + 0.3V
EN1, EN2, EN3 ..... –0.3V to V_{OUT} + 0.3V
FBx (x = 1, 2, 3) ..... –0.3V to V_{INx} + 0.3V
I_{OVSENS} 10mA
I_{CLPROG} 3mA
$I_{\overline{CHRG}}$, $I_{\overline{RST3}}$ 50mA
I_{PROG} 2mA
I_{LDO3V3} 30mA
I_{SW1}, I_{SW2} (Continuous) 600mA
I_{SW}, I_{SW3}, I_{BAT}, I_{VOUT} (Continuous) 2A
Maximum Junction Temperature ..... 125°C
Operating Temperature Range ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 125°C

PIN CONFIGURATION



UFE PACKAGE
38-LEAD (4mm × 6mm) PLASTIC QFN

T_{JMAX} = 125°C, θ_{JA} = 34°C/W
EXPOSED PAD (PIN 39) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3576EUFE#PBF	LTC3576EUFE#TRPBF	3576	38-Lead (4mm × 6mm) Plastic QFN	–40°C to 85°C
LTC3576EUFE-1#PBF	LTC3576EUFE-1#TRPBF	35761	38-Lead (4mm × 6mm) Plastic QFN	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{BUS} = 5V, BAT = 3.8V, DV_{CC} = 3.3V, R_{CLPROG} = 3.01k, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
PowerPath Switching Regulator—Step-Down Mode							
V_{BUS}	Input Supply Voltage			4.35		5.5	V
$I_{VBUS(LIM)}$	Total Input Current	1× Mode	●	82	90	100	mA
		5× Mode	●	440	472	500	mA
		10× Mode	●	800	880	1000	mA
		Low Power Suspend Mode	●	0.32	0.39	0.5	mA
		High Power Suspend Mode	●	1.6	2.05	2.5	mA
I_{VBUSQ} (Note 4)	Input Quiescent Current	1× Mode			7		mA
		5×, 10× Modes			17		mA
		Low/High Power Suspend Modes			0.045		mA

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SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
h_{CLPROG} (Note 4)	Ratio of Measured V_{BUS} Current to CLPROG Program Current	1× Mode 5× Mode 10× Mode Low Power Suspend Mode High Power Suspend Mode			210 1160 2200 9.6 56		mA/mA mA/mA mA/mA mA/mA mA/mA
$I_{VOUT(POWERPATH)}$	V_{OUT} Current Available Before Discharging Battery	1× Mode, BAT = 3.3V 5× Mode, BAT = 3.3V 10× Mode, BAT = 3.3V Low Power Suspend Mode High Power Suspend Mode		 0.26 1.6	121 667 1217 0.31 2	 0.41 2.4	mA mA mA mA mA
V_{CLPROG}	CLPROG Servo Voltage in Current Limit	Switching Modes Suspend Modes			1.18 100		V mV
V_{UVLO}	V_{BUS} Undervoltage Lockout	Rising Threshold Falling Threshold		 3.95	4.30 4.00	4.35 	V V
V_{DUVLO}	V_{BUS} to BAT Differential Undervoltage Lockout	Rising Threshold Falling Threshold			200 50		mV mV
V_{OUT}	V_{OUT} Voltage	1×, 5×, 10× Modes, 0V < BAT < 4.2V, I_{VOUT} = 0mA, Battery Charger Off USB Suspend Modes, I_{VOUT} = 250µA		3.4 4.5	BAT + 0.3 4.6	4.7 4.7	V V
f_{OSC}	Switching Frequency			1.8	2.25	2.7	MHz
$R_{PMOS_POWERPATH}$	PMOS On-Resistance				0.18		Ω
$R_{NMOS_POWERPATH}$	NMOS On-Resistance				0.30		Ω
$I_{PEAK_POWERPATH}$	Peak Inductor Current Limit	1× Mode (Note 5) 5× Mode (Note 5) 10× Mode (Note 5)			1 2 3		A A A
R_{SUSP}	Suspend LDO Output Resistance	Closed Loop			10		Ω
PowerPath Switching Regulator—Step-Up Mode (USB On-the-Go)							
V_{BUS}	Output Voltage	0mA ≤ I_{VBUS} ≤ 500mA, V_{OUT} > 3.2V		4.75		5.25	V
V_{OUT}	Input Voltage			2.9		5.5	V
I_{VBUS}	Output Current Limit		●	550	680		mA
I_{PEAK}	Peak Inductor Current Limit	(Note 5)			1.8		A
I_{OTGQ}	V_{OUT} Quiescent Current	V_{OUT} = 3.8V, I_{VBUS} = 0mA (Note 6)			1.38		mA
V_{CLPROG}	Output Current Limit Servo Voltage				1.15		V
$V_{OUT(UVLO)}$	V_{OUT} UVLO—V_{OUT} Falling V_{OUT} UVLO—V_{OUT} Rising			2.5 	2.6 2.8	 2.9	V V
$t_{SCFAULT}$	Short-Circuit Fault Delay	V_{BUS} < 4V and PMOS Switch Off			7.2		ms
Bat-Track Switching Regulator Control							
V_{WALL}	Absolute WALL Input Threshold	Rising Threshold Hysteresis		4.2 	4.3 1.1	4.4 	V V
ΔV_{WALL}	Differential WALL Input Threshold	WALL-BAT Falling Hysteresis		0 	30 60	45 	mV mV
V_{OUT}	Regulation Target Under V_C Control			3.55	BAT + 0.3		V
I_{WALLQ}	WALL Quiescent Current				400		µA
$R_{\overline{ACPR}}$	$\overline{ACPR}$ Pull-Down Strength				150		Ω
$V_{H\overline{ACPR}}$	$\overline{ACPR}$ High Voltage				V_{OUT}		V
$V_{L\overline{ACPR}}$	$\overline{ACPR}$ Low Voltage				0		V

ELECTRICAL CHARACTERISTICS

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SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Overvoltage Protection							
$V_{OVCUTOFF}$	Overvoltage Protection Threshold	With 6.2k Series Resistor		6.1	6.35	6.7	V
V_{OVGATE}	OVGATE Output Voltage	V_{OVSENS} < $V_{OVCUTOFF}$ V_{OVSENS} > $V_{OVCUTOFF}$			1.88•V_{OVSENS} 0	12	V V
t_{RISE}	OVGATE Time to Reach Regulation	OVGATE C_{LOAD} = 1nF			2.2		ms
Battery Charger							
V_{FLOAT}	BAT Regulated Output Voltage	LTC3576		4.179	4.200	4.221	V
			●	4.165	4.200	4.235	V
		LTC3576-1		4.079	4.100	4.121	V
			●	4.065	4.100	4.135	V
I_{CHG}	Constant Current Mode Charger Current	R_{PROG} = 1k R_{PROG} = 5k		980 185	1030 206	1065 223	mA mA
I_{BAT}	Battery Drain Current	V_{BUS} > V_{UVLO}, Suspend Mode, I_{VOUT} = 0µA			3.6	6	µA
		V_{BUS} = 0V, I_{VOUT} = 0µA (Ideal Diode Mode)			28	45	µA
V_{PROG}	PROG Pin Servo Voltage				1.000		V
V_{PROG_TRKL}	PROG Pin Servo Voltage in Trickle Charge	BAT < V_{TRKL}			0.100		V
$V_{C/10}$	C/10 Threshold Voltage at PROG				100		mV
h_{PROG}	Ratio of I_{BAT} to PROG Pin Current				1030		mA/mA
I_{TRKL}	Trickle Charge Current	BAT < V_{TRKL}, R_{PROG} = 1k			100		mA
V_{TRKL}	Trickle Charge Threshold Voltage	BAT Rising		2.7	2.85	3.0	V
ΔV_{TRKL}	Trickle Charge Hysteresis Voltage				135		mV
ΔV_{RECHRG}	Recharge Battery Threshold Voltage	Threshold Voltage Relative to V_{FLOAT}		–75	–100	–125	mV
t_{TERM}	Safety Timer Termination Period	Timer Starts When V_{BAT} = V_{FLOAT}		3.3	4	5	Hour
t_{BADBAT}	Bad Battery Termination Time	BAT < V_{TRKL}		0.4	0.5	0.6	Hour
$h_{C/10}$	End of Charge Current Ratio	(Note 7)		0.085	0.1	0.112	mA/mA
$V_{\overline{CHRG}}$	$\overline{CHRG}$ Pin Output Low Voltage	$I_{\overline{CHRG}}$ = 5mA			65	100	mV
$I_{\overline{CHRG}}$	$\overline{CHRG}$ Pin Leakage Current	$V_{\overline{CHRG}}$ = 5V				1	µA
R_{ON_CHG}	Battery Charger Power FET On-Resistance (Between V_{OUT} and BAT)				0.18		Ω
T_{LIM}	Junction Temperature in Constant Temperature Mode				110		°C
NTC							
V_{COLD}	Cold Temperature Fault Threshold Voltage	Rising Threshold Hysteresis		75	76.5 1.6	78	%NTCBIAS %NTCBIAS
V_{HOT}	Hot Temperature Fault Threshold Voltage	Falling Threshold Hysteresis		33.4	34.9 1.5	36.4	%NTCBIAS %NTCBIAS
V_{DIS}	NTC Disable Threshold Voltage	Falling Threshold Hysteresis		0.7	1.7 50	2.7	%NTCBIAS mV
I_{NTC}	NTC Leakage Current	NTC = NTCBIAS = 5V		–50		50	nA
Ideal Diode							
V_{FWD}	Forward Voltage	I_{VOUT} = 10mA			15		mV
$R_{DROPOUT}$	Internal Diode On-Resistance Dropout	I_{VOUT} = 200mA			0.18		Ω
I_{MAX_DIODE}	Diode Current Limit			2			A

ELECTRICAL CHARACTERISTICS

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SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Always On 3.3V LDO Supply							
V_{LDO3V3}	Regulated Output Voltage	0mA < I_{LDO3V3} < 20mA		3.1	3.3	3.5	V
R_{CL_LDO3V3}	Closed-Loop Output Resistance				2.7		Ω
R_{OL_LDO3V3}	Dropout Output Resistance				23		Ω
Logic (I_{LIM0}, I_{LIM1}, EN1, EN2, EN3, ENOTG, and SCL, SDA when DV_{CC} = 0V)							
V_{IL}	Logic Low Input Voltage					0.4	V
V_{IH}	Logic High Input Voltage			1.2			V
I_{PD1}	I_{LIM0}, I_{LIM1}, EN1, EN2, EN3, ENOTG, SCL, SDA Pull-Down Current				2		µA
I^2C Port							
DV_{CC}	Input Supply			1.6		5.5	V
I_{DVCC}	DV_{CC} Current	SCL/SDA = 0kHz, DV_{CC} = 3.3V			0.5		µA
$V_{DVCC(UVLO)}$	DV_{CC} UVLO				1.0		V
ADDRESS	I^2C Address				0001001[0]		
V_{IH}, SDA, SCL	Input High Threshold			70			$\%DV_{CC}$
V_{IL}, SDA, SCL	Input Low Threshold					30	$\%DV_{CC}$
I_{PD2}, SDA, SCL	Pull-Down Current				2		µA
V_{OL}	Digital Output Low (SDA)	I_{SDA} = 3mA				0.4	V
f_{SCL}	Clock Operating Frequency					400	kHz
t_{BUF}	Bus Free Time Between Stop and Start Condition			1.3			µs
t_{HD_STA}	Hold Time After (Repeated) Start Condition			0.6			µs
t_{SU_STA}	Repeated Start Condition Setup Time			0.6			µs
t_{SU_STO}	Stop Condition Setup Time			0.6			µs
$t_{HD_DAT(O)}$	Data Hold Time Output			0		900	ns
$t_{HD_DAT(I)}$	Data Hold Time Input			0			ns
t_{SU_DAT}	Data Setup Time			100			ns
t_{LOW}	SCL Low Period			1.3			µs
t_{HIGH}	SCL High Period			0.6			µs
t_f	SDA/SCL Fall Time			20		300	ns
t_r	SDA/SCL Rise Time			20		300	ns
t_{SP}	Input Spike Suppression Pulse Width					50	ns
General Purpose Switching Regulators 1, 2 and 3							
$V_{IN1,2,3}$	Input Supply Voltage	(Note 8)		2.7		5.5	V
$V_{OUT(UVLO)}$	V_{OUT} UVLO—V_{OUT} Falling V_{OUT} UVLO—V_{OUT} Rising	$V_{IN1,2,3}$ Connected to V_{OUT} Through Low Impedance. Switching Regulators are Disabled in UVLO		2.5	2.6 2.8	 2.9	V V
f_{OSC}	Switching Frequency			1.8	2.25	2.7	MHz
$I_{FB1,2,3}$	FBx Input Current	$V_{FB1,2,3}$ = 0.85V		–50		50	nA
D1,2,3	Maximum Duty Cycle			100			%
$R_{SW1,2,3_PD}$	SWx Pull-Down in Shutdown				10		kΩ

ELECTRICAL CHARACTERISTICS

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SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$I_{VIN1,2,3}$	Pulse-Skipping Mode Input Current	$I_{OUT1,2,3}$ = 0µA (Note 9)			90		µA
	Burst Mode® Input Current	$I_{OUT1,2,3}$ = 0µA (Note 9)			20	35	µA
	LDO Mode Input Current	$I_{OUT1,2,3}$ = 0µA (Note 9)			15	25	µA
	Shutdown Input Current Limit	$I_{OUT1,2,3}$ = 0µA, FB1,2,3 = 0V				1	µA
$V_{FBHIGH1,2,3}$	Maximum Servo Voltage	Full Scale (1,1,1,1) (Note 10)	●	0.78	0.80	0.82	V
$V_{FBLOW1,2,3}$	Minimum Servo Voltage	Zero Scale (0,0,0,0) (Note 10)		0.405	0.425	0.445	V
$V_{LSB1,2,3}$	$V_{FB1,2}$ Servo Voltage Step Size				25		mV
$R_{LDO_CL1,2,3}$	LDO Mode Closed-Loop R_{OUT}	$V_{FB1,2,3}$ = $V_{OUT1,2\,3}$ = 0.8V			0.25		Ω
$R_{LDO_OL1,2,3}$	LDO Mode Open-Loop R_{OUT}	(Note 11)			2.5		Ω
General Purpose Switching Regulator 1 and 2							
$I_{LIM1,2}$	PMOS Switch Current Limit	Pulse-Skipping/Burst Mode Operation (Note 5)		600	900	1300	mA
$I_{OUT1,2}$	Available Output Current	LDO Mode		50			mA
$R_{P1,2}$	PMOS $R_{DS(ON)}$				0.6		Ω
$R_{N1,2}$	NMOS $R_{DS(ON)}$				0.7		Ω
General Purpose Switching Regulator 3							
I_{LIM3}	PMOS Switch Current Limit	Pulse-Skipping/Burst Mode Operation (Note 5)		1300	1800	2800	mA
I_{OUT3}	Available Output Current	LDO Mode		50			mA
R_{P3}	PMOS $R_{DS(ON)}$				0.18		Ω
R_{N3}	NMOS $R_{DS(ON)}$				0.3		Ω
$t_{\overline{RST3}}$	Power-On Reset Time for Switching Regulator	V_{FB3} Within 92% of Final Value to $\overline{RST3}$ Hi-Z			230		ms

Burst Mode is a registered trademark of Linear Technology Corporation.

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC3576E/LTC3576E-1 are guaranteed to meet performance specifications from 0°C to 85°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls.

Note 3: The LTC3576E/LTC3576E-1 include overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

Note 4: Total input current is the sum of quiescent current, I_{VBUSQ}, and measured current given by $V_{CLPROG}/R_{CLPROG} \bullet (h_{CLPROG} + 1)$.

Note 5: The current limit features of this part are intended to protect the IC from short term or intermittent fault conditions. Continuous operation above the maximum specified pin current rating may result in device degradation or failure.

Note 6: The bidirectional switcher's supply current is bootstrapped to V_{BUS} and in the application will reflect back to V_{OUT} by $(V_{BUS}/V_{OUT}) \bullet$ 1/efficiency. Total quiescent current is the sum of the current into the V_{OUT} pin plus the reflected current.

Note 7: $h_{C/10}$ is expressed as a fraction of the measured full charge current with indicated PROG resistor.

Note 8: V_{OUT} not in UVLO.

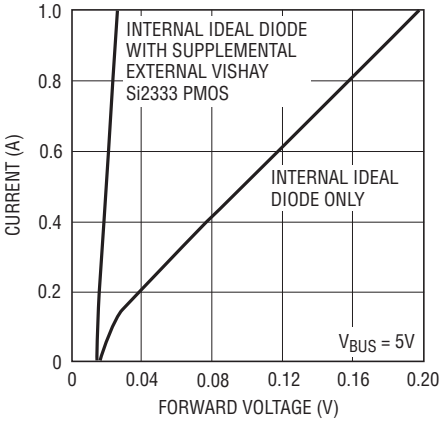
Note 9: FBx above regulation such that regulator is in sleep. Specification does not include resistive divider current reflected back to V_{INx}.

Note 10: Applies to pulse-skipping and Burst Mode operation only.

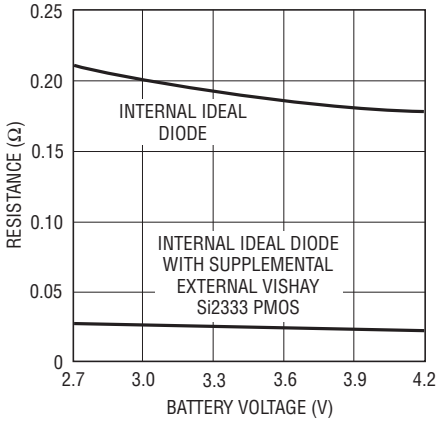
Note 11: Inductor series resistance adds to open-loop R_{OUT}.

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C unless otherwise specified.

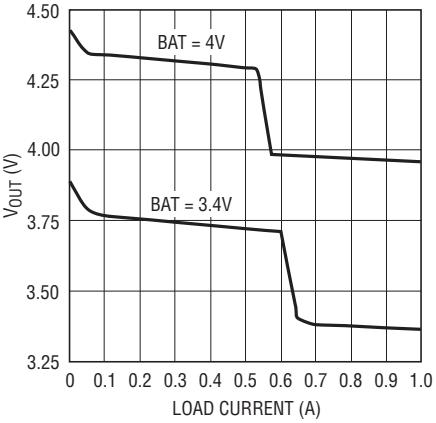
Ideal Diode V-I Characteristics



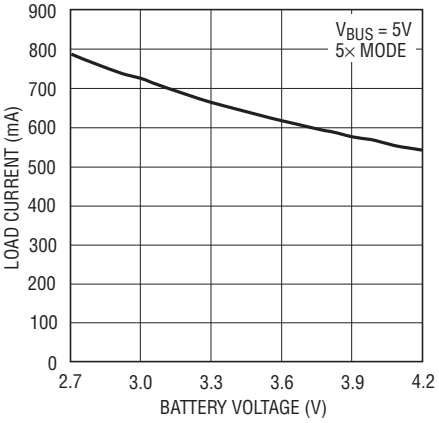
Ideal Diode Resistance vs Battery Voltage



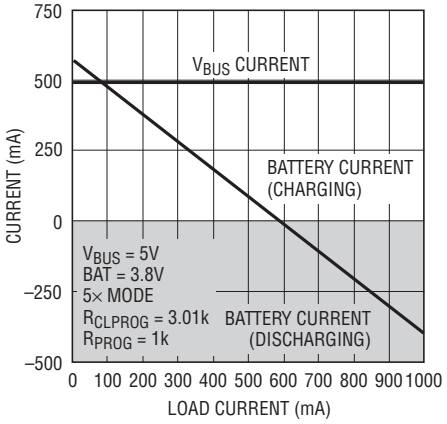
V_{OUT} Voltage vs Load Current (Battery Charger Disabled)



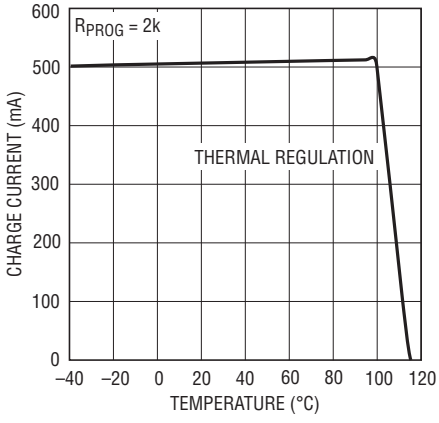
USB Limited Load Current vs Battery Voltage (Battery Charger Disabled)



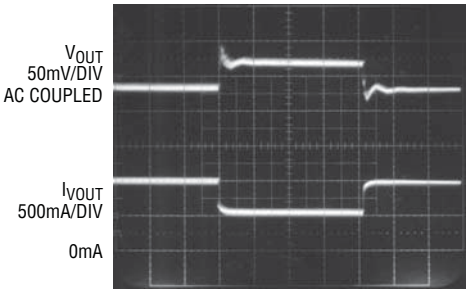
Battery and V_{BUS} Currents vs Load Current



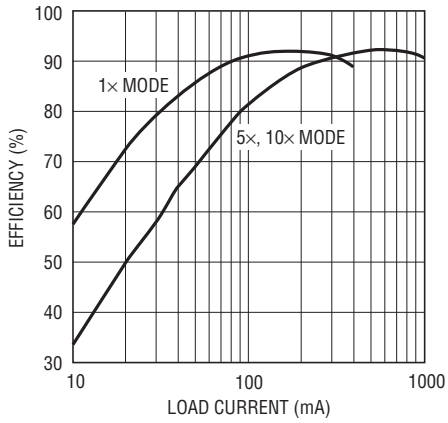
Battery Charge Current vs Temperature



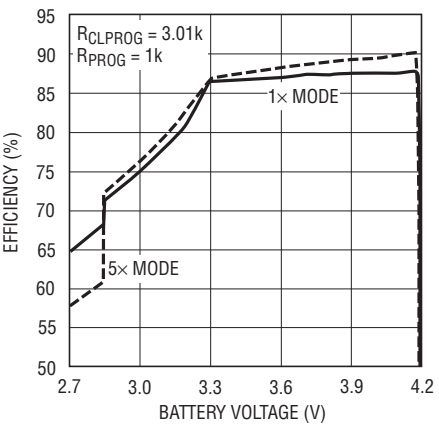
PowerPath Switching Regulator Transient Response



PowerPath Switching Regulator Efficiency vs Load Current

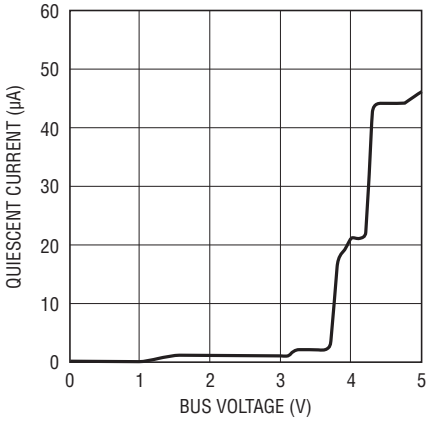


Battery Charging Efficiency vs Battery Voltage with No External Load (P_{BAT}/P_{VBUS})



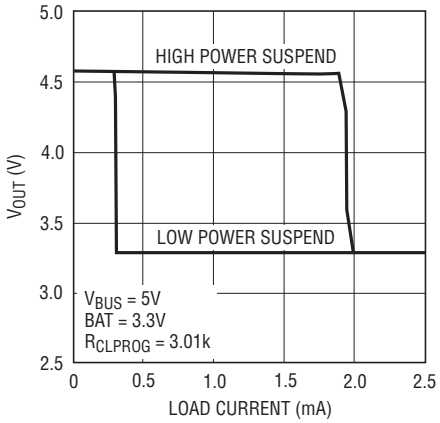
TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C unless otherwise specified.

V_{BUS} Quiescent Current vs V_{BUS} Voltage (Suspend)



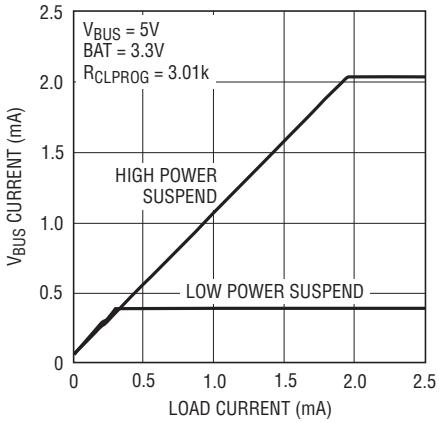
3576 G10

V_{OUT} Voltage vs Load Current in Suspend



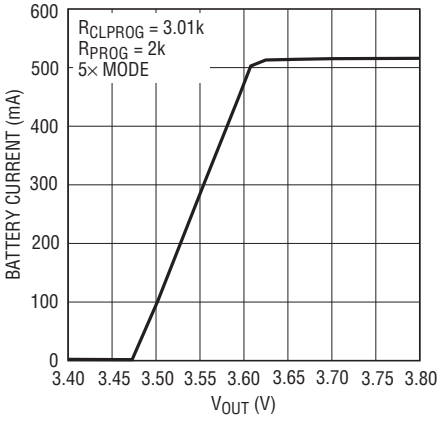
3576 G11

V_{BUS} Current vs Load Current in Suspend



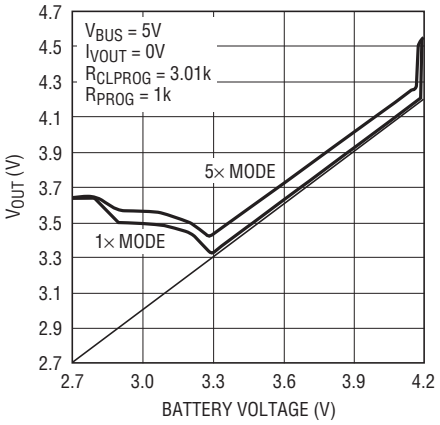
3576 G12

Battery Charge Current vs V_{OUT} Voltage



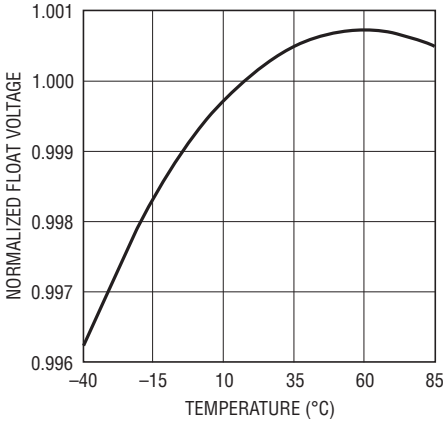
3576 G13

V_{OUT} Voltage vs Battery Voltage (Charger Overprogrammed)



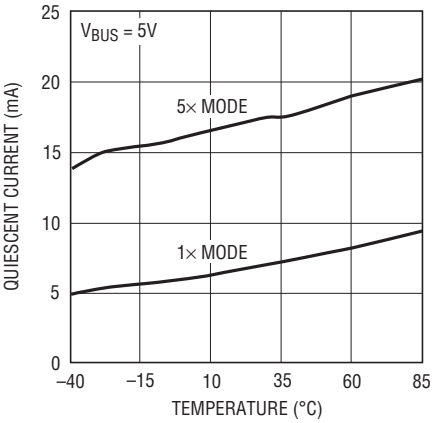
3576 G14

Normalized Battery Charger Float Voltage vs Temperature



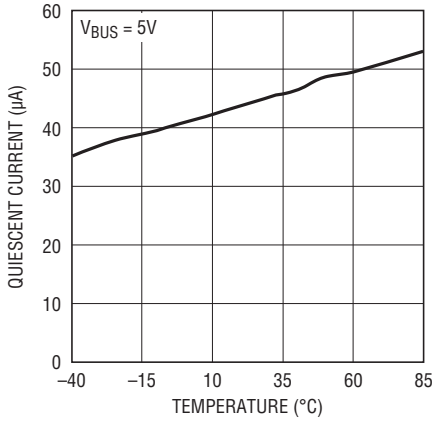
3576 G15

V_{BUS} Quiescent Current vs Temperature



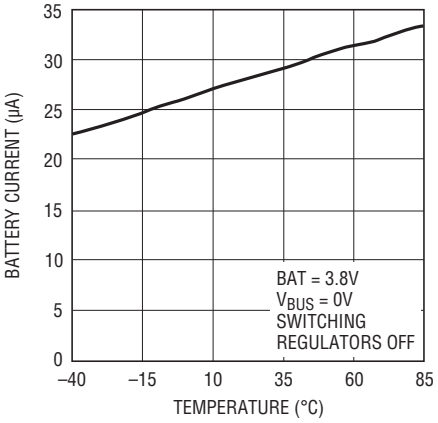
3576 G16

V_{BUS} Quiescent Current in Suspend vs Temperature



3576 G17

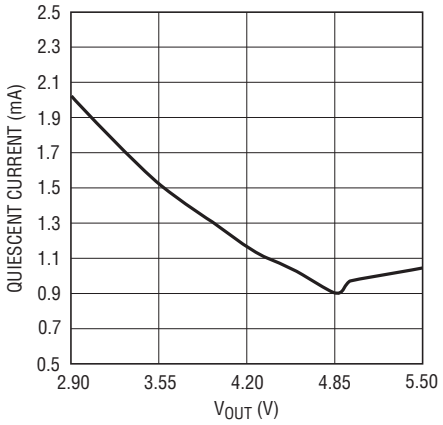
Battery Drain Current vs Temperature



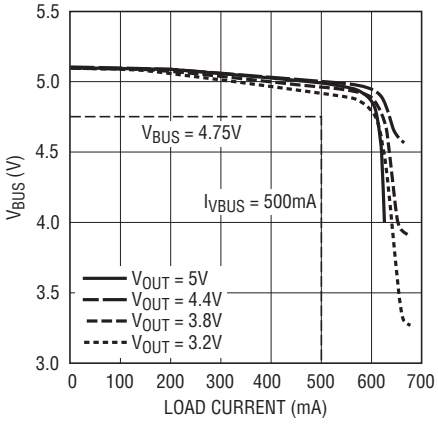
3576 G18

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C unless otherwise specified.

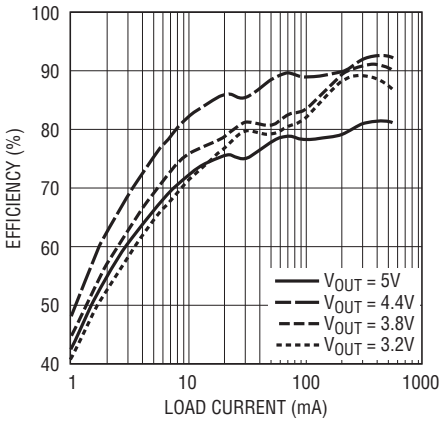
OTG Boost Quiescent Current vs V_{OUT} Voltage



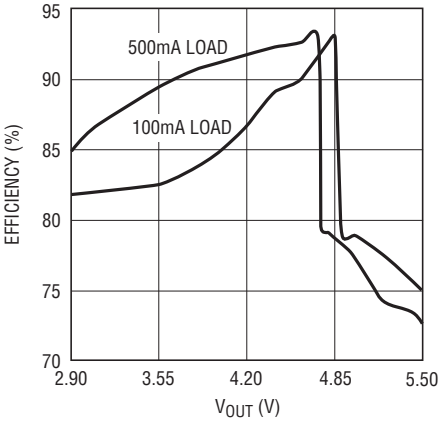
OTG Boost V_{BUS} Voltage vs Load Current



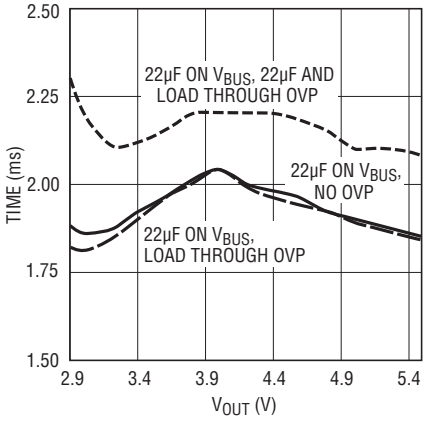
OTG Boost Efficiency vs Load Current



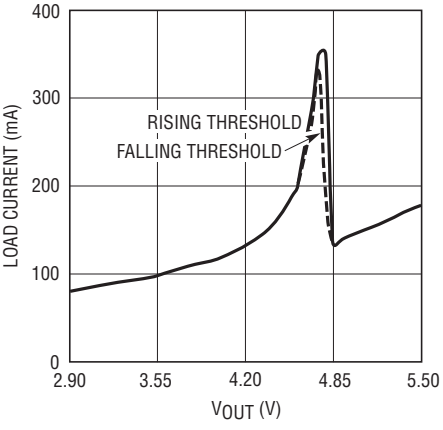
OTG Boost Efficiency vs V_{OUT} Voltage



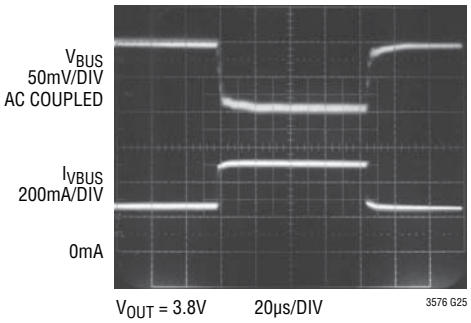
OTG Boost Start-Up Time into Current Source Load vs V_{OUT} Voltage



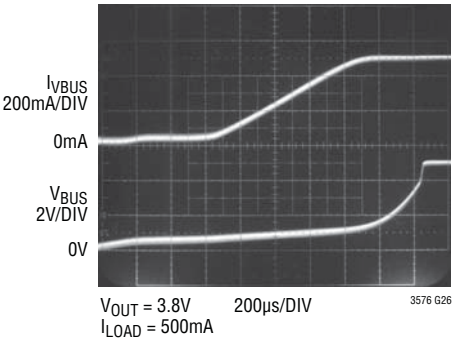
OTG Boost Burst Mode Current Threshold vs V_{OUT} Voltage



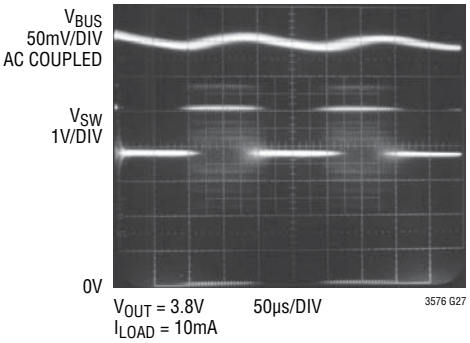
OTG Boost Transient Response



OTG Boost Start-Up into Current Source Load

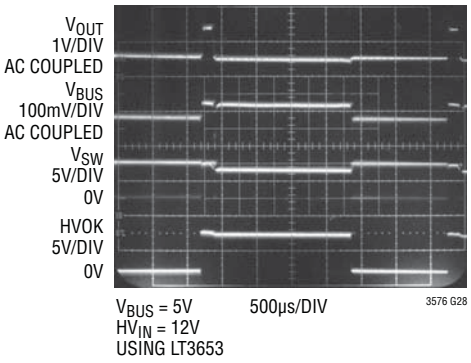


OTG Boost Burst Mode Operation

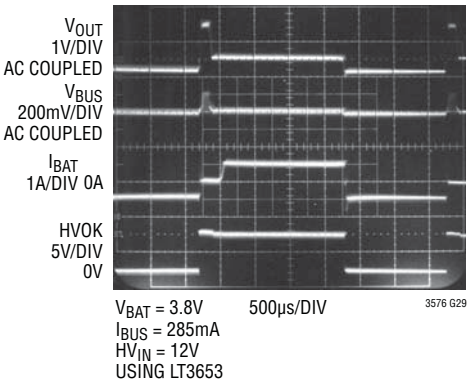


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C unless otherwise specified.

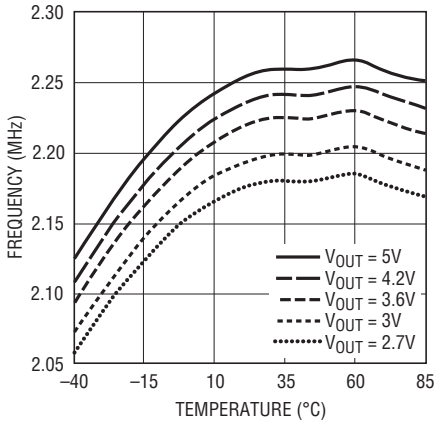
Battery Charging from USB-HV BUCK-USB



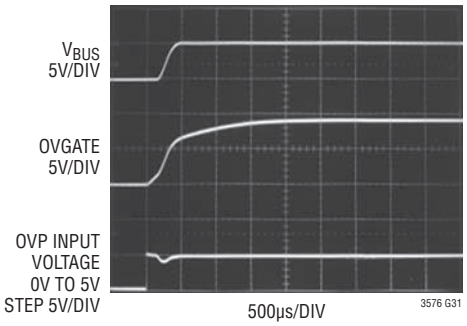
USB OTG from BAT-HV BUCK-BAT



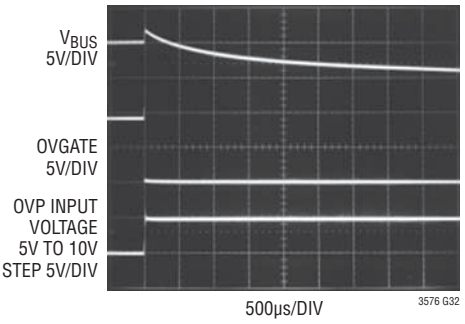
Oscillator Frequency vs Temperature



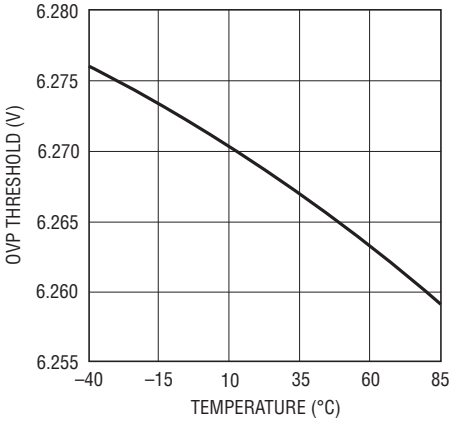
OVP Connect Waveform



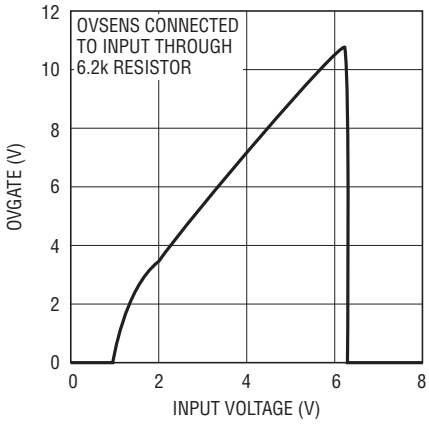
OVP Disconnect Waveform



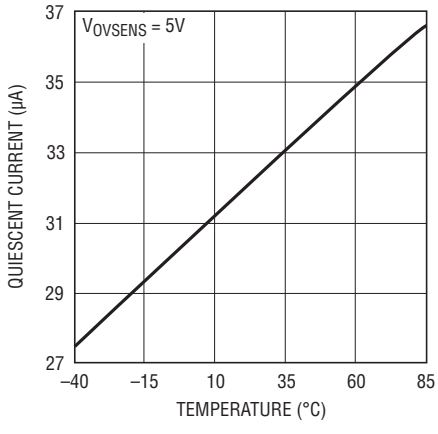
Rising OVP Threshold vs Temperature



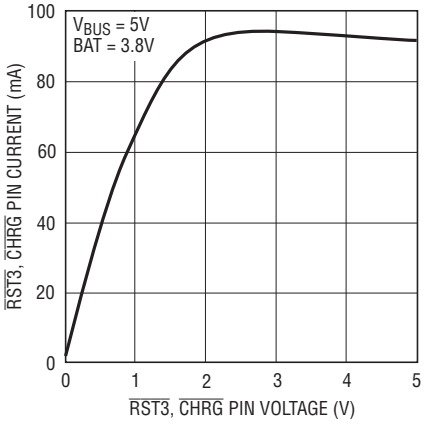
OVGATE vs OVSENS



OVGATE Quiescent Current vs Temperature

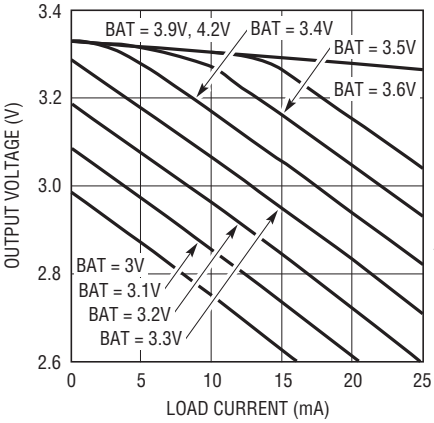


$\overline{RST3}$, $\overline{CHRG}$ Pin Current vs Voltage (Pull-Down State)



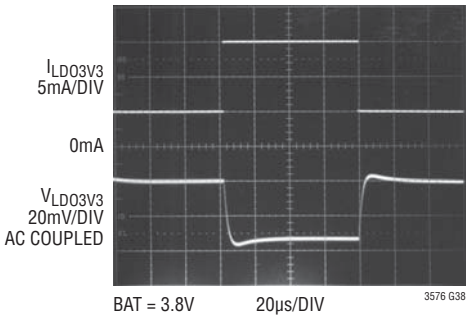
TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C unless otherwise specified.

3.3V LDO Output Voltage vs Load Current, V_{BUS} = 0V



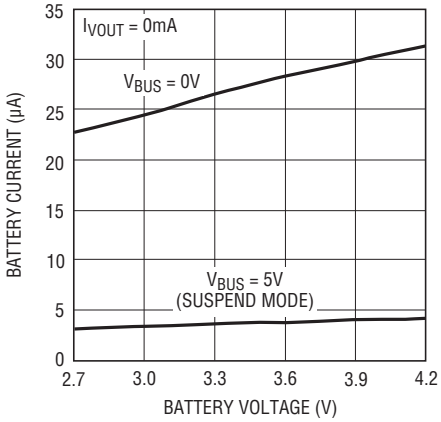
3576 G37

3.3V LDO Step Response (5mA to 15mA)



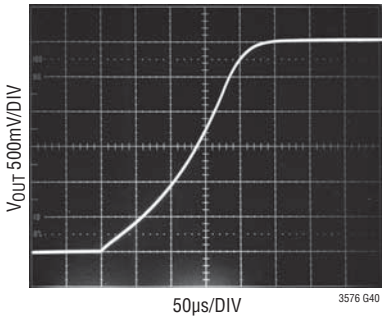
3576 G38

Battery Drain Current vs Battery Voltage



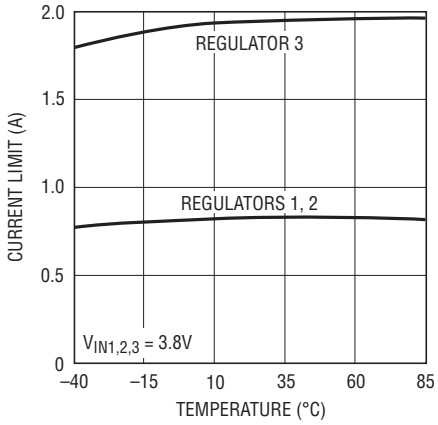
3576 G39

Switching Regulator Soft-Start Waveform



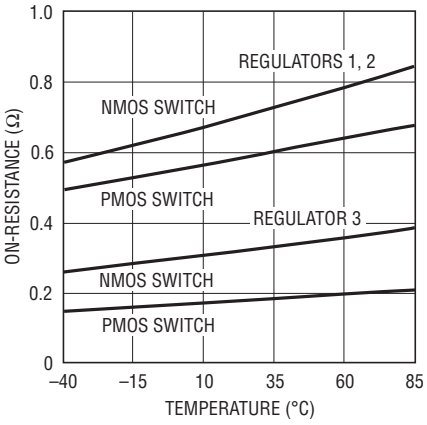
3576 G40

Switching Regulator Current Limit vs Temperature



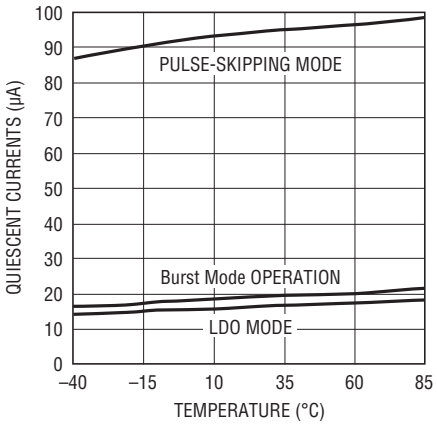
3576 G41

$R_{DS(ON)}$ for Switching Regulator Power Switches vs Temperature



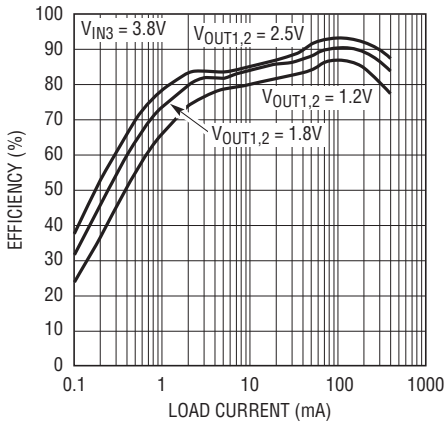
3576 G42

Switching Regulator Low Power Quiescent Currents vs Temperature



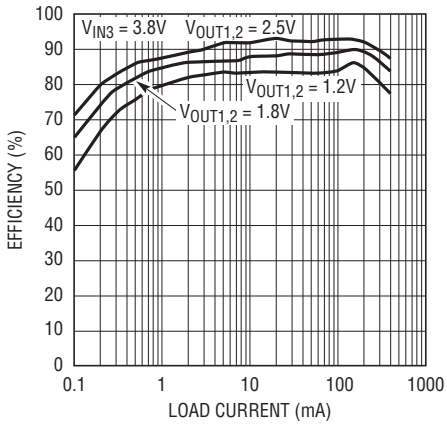
3576 G43

Switching Regulators 1, 2 Pulse-Skipping Mode Efficiency



3576 G44

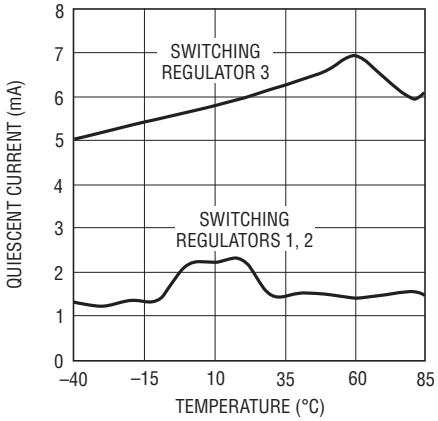
Switching Regulators 1, 2 Burst Mode Efficiency



3576 G45

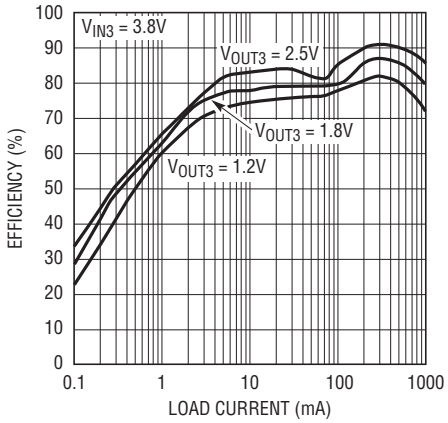
TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C unless otherwise specified.

Switching Regulator Constant Frequency Quiescent Currents



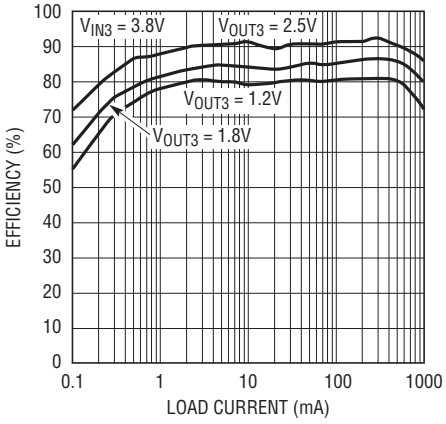
3576 G46

Switching Regulator 3 Pulse-Skipping Mode Efficiency



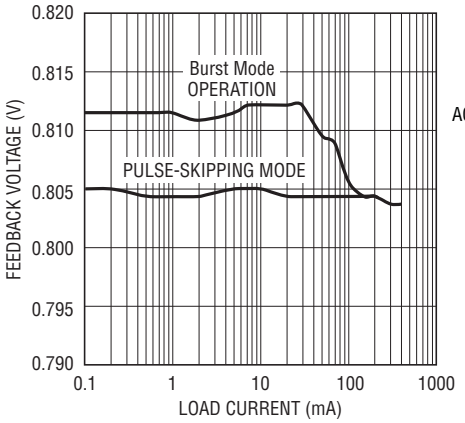
3576 G47

Switching Regulator 3 Burst Mode Efficiency



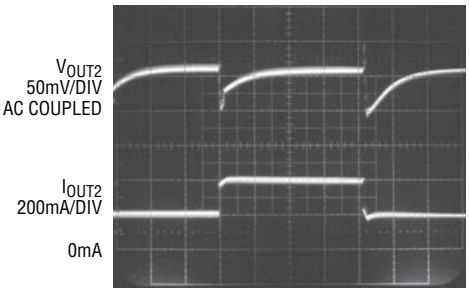
3576 G48

Switching Regulators 1, 2 Feedback Voltage vs Load Current



3576 G49

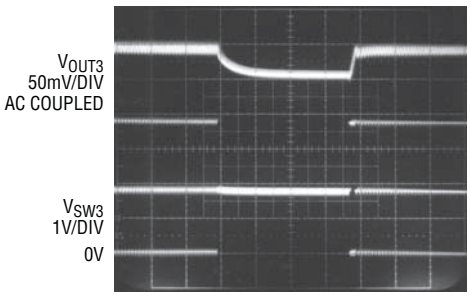
Switching Regulators 1, 2 Transient Response



V_{IN2} = 3.8V
V_{OUT2} = 3.4V
50µs/DIV

3576 G50

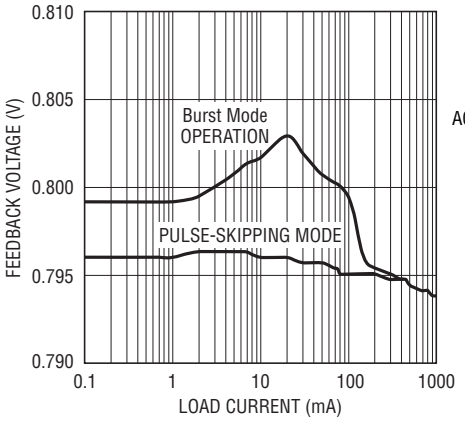
Switching Regulator Mode Transition, Pulse-Skipping-LDO-Pulse-Skipping



V_{IN3} = 3.8V
V_{OUT3} = 1.8V
I_{OUT3} = 50mA
50µs/DIV

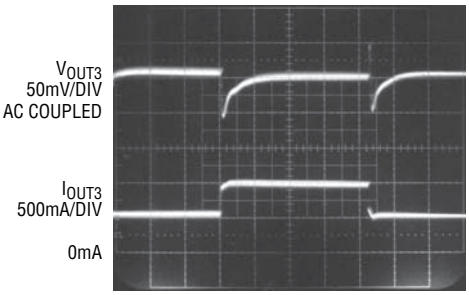
3576 G51

Switching Regulator 3 Feedback Voltage vs Load Current



3576 G52

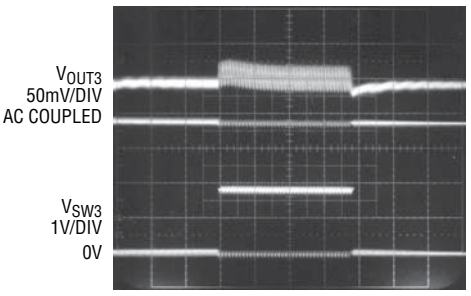
Switching Regulator 3 Transient Response



V_{IN3} = 3.8V
V_{OUT3} = 1.8V
50µs/DIV

3576 G53

Switching Regulator Mode Transition, Pulse-Skipping–Burst Mode Operation–Pulse-Skipping



V_{IN3} = 3.8V
V_{OUT3} = 1.8V
I_{OUT3} = 100mA
50µs/DIV

3576 G54

PIN FUNCTIONS

CLPROG (Pin 1): USB Current Limit Program and Monitor Pin. A 1% resistor from CLPROG to ground determines the upper limit of the current drawn or sourced from the V_{BUS} pins. A precise fraction, h_{CLPROG}, of the V_{BUS} current is sent to the CLPROG pin when the PMOS switch of the PowerPath switching regulator is on. The switching regulator delivers power until the CLPROG pin reaches 1.18V in step-down mode and 1.15V in step-up mode. When the switching regulator is in step-down mode, CLPROG is used to regulate the average input current. Several V_{BUS} current limit settings are available via user input which will typically correspond to the 500mA and 100mA USB specifications. When the switching regulator is in step-up mode (USB on-the-go), CLPROG is used to limit the average output current to 680mA. A multilayer ceramic averaging capacitor or R-C network is required at CLPROG for filtering.

LDO3V3 (Pin 2): 3.3V LDO Output Pin. This pin provides a regulated always-on 3.3V supply voltage. LDO3V3 gets its power from V_{OUT}. It may be used for light loads such as a watchdog microprocessor or real time clock. A 1µF capacitor is required from LDO3V3 to ground. If the LDO3V3 output is not used it should be disabled by connecting it to V_{OUT}.

NTCBIAS (Pin 3): NTC Thermistor Bias Output. If NTC operation is desired, connect a bias resistor between NTCBIAS and NTC, and an NTC thermistor between NTC and GND. To disable NTC operation, connect NTC to GND and leave NTCBIAS open.

NTC (Pin 4): Input to the Thermistor Monitoring Circuits. The NTC pin connects to a negative temperature coefficient thermistor, which is typically co-packaged with the battery, to determine if the battery is too hot or too cold to charge. If the battery's temperature is out of range, charging is paused until it re-enters the valid range. A low drift bias resistor is required from NTCBIAS to NTC and a thermistor is required from NTC to ground. To disable NTC operation, connect NTC to GND and leave NTCBIAS open.

OVGATE (Pin 5): Overvoltage Protection Gate Output. Connect OVGATE to the gate pin of an external N-channel MOS pass transistor. The source of the transistor should be connected to V_{BUS} and the drain should be connected to the product's DC input connector. In the absence of an overvoltage condition, this pin is connected to an internal charge pump capable of creating sufficient overdrive to fully enhance the pass transistor. If an overvoltage condition is detected, OVGATE is brought rapidly to GND to prevent damage to the LTC3576/LTC3576-1. OVGATE works in conjunction with OVSENS to provide this protection.

OVSENS (Pin 6): Overvoltage Protection Sense Input. OVSENS should be connected through a 6.2k resistor to the input power connector and the drain of an external N-channel MOS pass transistor. When the voltage on this pin exceeds $V_{OVCUTOFF}$, the OVGATE pin will be pulled to GND to disable the pass transistor and protect the LTC3576/LTC3576-1. The OVSENS pin shunts current during an overvoltage transient in order to keep the pin voltage at 6V.

FB1 (Pin 7): Feedback Input for Switching Regulator 1. When regulator 1's control loop is complete, this pin servos to 1 of 16 possible set points based on the commanded value from the I^2C serial port. See Table 4.

V_{IN1} (Pin 8): Power Input for Switching Regulator 1. This pin will generally be connected to V_{OUT}. A 1µF MLCC capacitor is recommended on this pin.

SW1 (Pin 9): Power Transmission Pin for Switching Regulator 1.

EN1 (Pin 10): Logic Input. This logic input pin independently enables switching regulator 1. Active high. This pin is logically ORed with its corresponding bit in the I^2C serial port. See Table 3. Has a 2µA internal pull-down current source.

ENOTG (Pin 11): Logic Input. This logic input pin independently enables the bidirectional switching regulator to step up the voltage on V_{OUT} and provide a 5V output on V_{BUS} for USB on-the-go applications. Active high. This pin is logically ORed with its corresponding bit in the I^2C serial port. See Table 3. Has a 2µA internal pull-down current source.

PIN FUNCTIONS

DV_{CC} (Pin 12): Logic Supply for the I^2C Serial Port. If the serial port is not needed, it can be disabled by grounding DV_{CC}. When DV_{CC} is grounded, the I^2C bits are set to their default values. See Table 3.

SCL (Pin 13): Clock Input Pin for the I^2C Serial Port. The I^2C logic levels are scaled with respect to DV_{CC}. If DV_{CC} is grounded, the SCL pin is equivalent to the C2, C4 and C6 bits in the I^2C serial port. SCL in conjunction with SDA determine the operating modes of switching regulators 1, 2 and 3 when DV_{CC} is grounded. See Tables 3 and 5. Has a 2µA internal pull-down current source.

SDA (Pin 14): Data Input Pin for the I^2C Serial Port. The I^2C logic levels are scaled with respect to DV_{CC}. If DV_{CC} is grounded, the SDA pin is equivalent to the C3, C5 and C7 bits in the I^2C serial port. SDA in conjunction with SCL determine the operating modes of switching regulators 1, 2 and 3 when DV_{CC} is grounded. See Tables 3 and 5. Has a 2µA internal pull-down current source.

NC (Pin 15): Unconnected Pin. This pin is not connected internally to the part. It is permissible to tie this pin to V_{IN3} in order to make the V_{IN3} PCB trace wider.

V_{IN3} (Pin 16): Power Input for Switching Regulator 3. This pin will generally be connected to V_{OUT}. A 1µF MLCC capacitor is recommended on this pin.

SW3 (Pin 17): Power Transmission Pin for Switching Regulator 3.

NC (Pin 18): Unconnected Pin. This pin is not connected internally to the part. It is permissible to tie this pin to SW3 in order to make the SW3 PCB trace wider.

EN3 (Pin 19): Logic Input. This logic input pin independently enables switching regulator 3. Active high. This pin is logically ORed with its corresponding bit in the I^2C serial port. See Table 3. Has a 2µA internal pull-down current source.

FB3 (Pin 20): Feedback Input for Switching Regulator 3. When regulator 3's control loop is complete, this pin servos to 1 of 16 possible set points based on the commanded value from the I^2C serial port. See Table 4.

$\overline{RST3}$ (Pin 21): Logic Output. This in an open-drain output which indicates that switching regulator 3 has settled to its final value. It can be used as a power-on reset for the primary microprocessor or to enable the other switching regulators for supply sequencing.

EN2 (Pin 22): Logic Input. This logic input pin independently enables switching regulator 2. Active high. This pin is logically ORed with its corresponding bit in the I^2C serial port. See Table 3. Has a 2µA internal pull-down current source.

SW2 (Pin 23): Power Transmission Pin for Switching Regulator 2.

V_{IN2} (Pin 24): Power Input for Switching Regulator 2. This pin will generally be connected to V_{OUT}. A 1µF MLCC capacitor is recommended on this pin.

FB2 (Pin 25): Feedback Input for Switching Regulator 2. When regulator 2's control loop is complete, this pin servos to 1 of 16 possible set points based on the commanded value from the I^2C serial port. See Table 4.

V_C (Pin 26): Bat-Track External Switching Regulator Control Output. This pin drives the V_C pin of an external Linear Technology step-down switching regulator. An external P-channel MOSFET is sometimes required to provide power to V_{OUT} with its gate tied to the $\overline{ACPR}$ pin (see the Applications Information section). In concert with WALL and $\overline{ACPR}$, it will regulate V_{OUT} to maximize battery charger efficiency

WALL (Pin 27): External Power Source Sense Input. WALL should be connected to the output of the external high voltage switching regulator and to the drain of an external P-channel MOSFET if used. It is used to determine when power is applied to the external regulator. When power is detected, $\overline{ACPR}$ is driven low and the USB input is automatically disabled. Pulling this pin above 4.3V enables the V_C pin.

PIN FUNCTIONS

$\overline{ACPR}$ (Pin 28): External Power Source Present Output (Active Low). $\overline{ACPR}$ indicates that the output of the external high voltage step-down switching regulator is suitable for use by the LTC3576/LTC3576-1. It should be connected to the gate of an external P-channel MOSFET whose source is connected to V_{OUT} and whose drain is connected to WALL. $\overline{ACPR}$ has a high level of V_{OUT} and a low level of GND. The USB bidirectional switcher is disabled when $\overline{ACPR}$ is low.

PROG (Pin 29): Charge Current Program and Charge Current Monitor Pin. Connecting a 1% resistor from PROG to ground programs the charge current. If sufficient input power is available in constant-current mode, this pin servos to 1V. The voltage on this pin always represents the actual charge current by using the following formula:

$$I_{BAT} = \frac{V_{PROG}}{R_{PROG}} \bullet 1030$$

$\overline{CHRG}$ (Pin 30): Open-Drain Charge Status Output. The $\overline{CHRG}$ pin indicates the status of the battery charger. Four possible charger states are represented by $\overline{CHRG}$: charging, not charging, unresponsive battery and battery temperature out of range. In addition, $\overline{CHRG}$ is used to indicate whether there is a short-circuit condition on V_{BUS} when the bidirectional switching regulator is in step-up mode (on-the-go). $\overline{CHRG}$ is modulated at 35kHz and switches between a low and a high duty cycle for easy recognition by either humans or microprocessors. See Table 1. $\overline{CHRG}$ requires a pull-up resistor and/or LED to provide indication.

IDGATE (Pin 31): Ideal Diode Amplifier Output. This pin controls the gate of an optional external P-channel MOSFET used as an ideal diode between V_{OUT} and BAT. The external ideal diode operates in parallel with the internal ideal diode. The source of the P-channel MOSFET should be connected to V_{OUT} and the drain should be connected to BAT. If the external ideal diode MOSFET is not used, IDGATE should be left floating.

BAT (Pin 32): Single Cell Li-Ion Battery Pin. Depending on available V_{BUS} power, a Li-Ion battery on BAT will either deliver power to V_{OUT} through the ideal diode or be charged from V_{OUT} via the battery charger.

V_{OUT} (Pin 33): Output Voltage of the Bidirectional PowerPath Switching Regulator in step-down mode and Input Voltage of the Battery Charger. The majority of the portable product should be powered from V_{OUT}. The LTC3576/LTC3576-1 will partition the available power between the external load on V_{OUT} and the internal battery charger. Priority is given to the external load and any extra power is used to charge the battery. An ideal diode from BAT to V_{OUT} ensures that V_{OUT} is powered even if the load exceeds the allotted power from V_{BUS} or if the V_{BUS} power source is removed. In on-the-go mode, this pin delivers power to V_{BUS} via the SW pin. V_{OUT} should be bypassed with a low impedance ceramic capacitor.

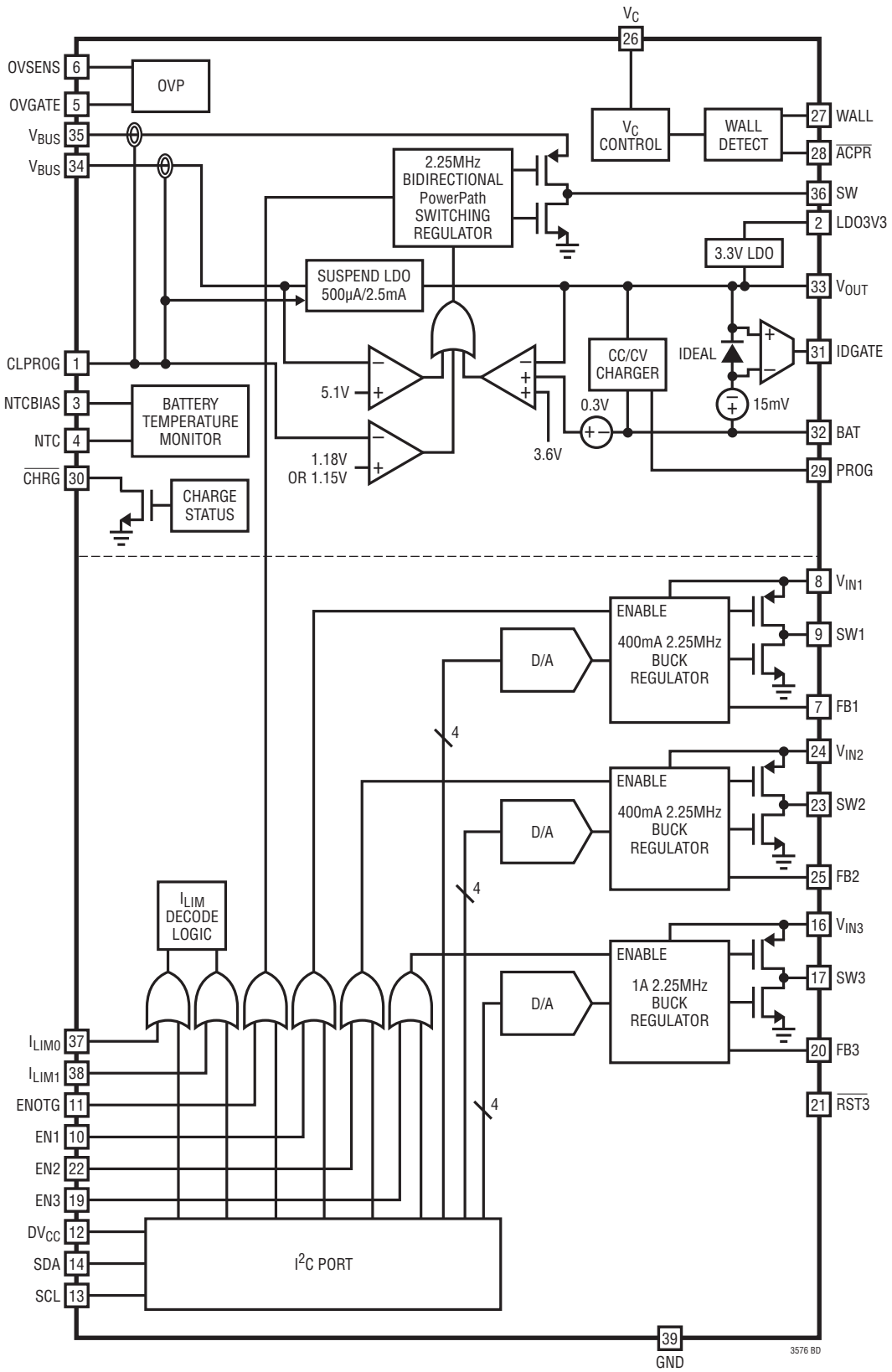
V_{BUS} (Pins 34, 35): Power Pins. These pins deliver power to V_{OUT} via the SW pin by drawing controlled current from a DC source such as a USB port or DC output wall adapter. In on-the-go mode these pins provide power to external loads. Tie the two V_{BUS} pins together at the part and bypass with a low impedance multilayer ceramic capacitor.

SW (Pin 36): The SW pin transfers power between V_{BUS} and V_{OUT} via the bidirectional switching regulator. See the Applications Information section for a discussion of inductance value and current rating.

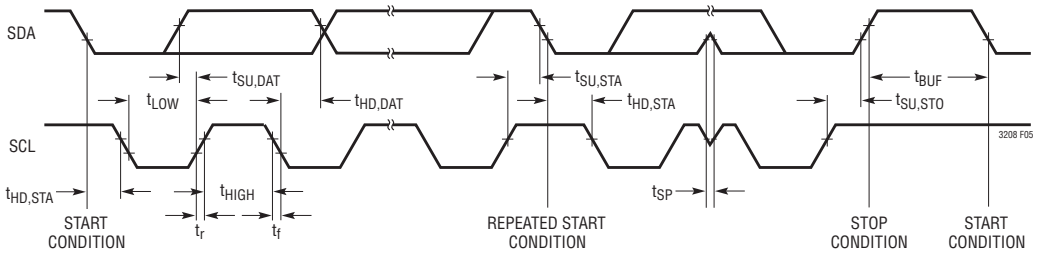
I_{LIM0}, I_{LIM1} (Pins 37, 38): I_{LIM0} and I_{LIM1} control the current limit of the PowerPath switching regulator. See Table 1. Both the I_{LIM0} and I_{LIM1} pins are logically ORed with their corresponding bits in the I^2C serial port. See Tables 3 and 6. Each has a 2µA internal pull-down current source.

Exposed Pad (Pin 39): Ground. The Exposed Pad should be connected to a continuous ground plane on the second layer of the printed circuit board by several vias directly under the LTC3576/LTC3576-1.

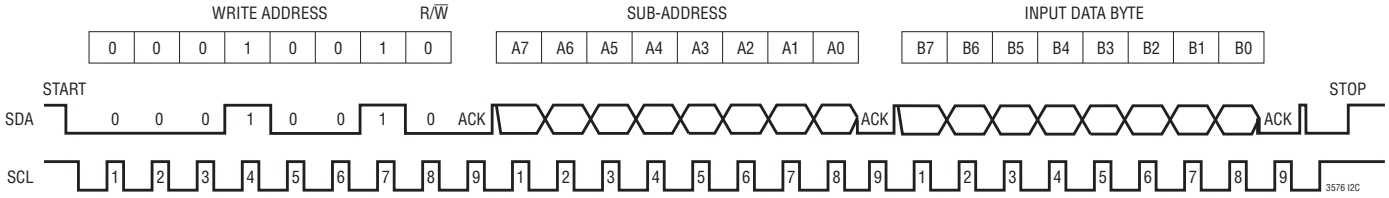
BLOCK DIAGRAM



TIMING DIAGRAM



I²C WRITE PROTOCOL



OPERATION

Introduction

The LTC3576/LTC3576-1 are highly integrated power management ICs designed to make optimal use of the power available from a variety of sources, while minimizing power dissipation and easing thermal budgeting constraints. They include a high efficiency bidirectional PowerPath switching regulator, a controller for an external high voltage step-down switching regulator, a battery charger, an ideal diode, an always-on LDO, an overvoltage protection circuit and three general purpose step-down switching regulators. The entire chip is controlled by either direct digital control or by an I^2C serial port or both.

The innovative PowerPath architecture ensures that the application is powered immediately after external voltage is applied, even with a completely dead battery, by prioritizing power to the application.

When acting as a step-down converter, the LTC3576/LTC3576-1's bidirectional switching regulator takes power from USB, wall adapters, or other 5V sources and provides power to the application and efficiently charges the battery using Bat-Track. Because power is conserved the LTC3576/LTC3576-1 allow the load current on V_{OUT} to exceed the current drawn by the USB port making maximum use of the allowable USB power for battery charging. For USB compatibility the switching regulator includes a precision average input current limit. The PowerPath switching regulator and battery charger communicate to ensure that the average input current never exceeds the USB specifications.

Additionally, the bidirectional switching regulator can also operate as a 5V synchronous step-up converter taking power from V_{OUT} and delivering up to 500mA to V_{BUS} without the need for any additional external components. This enables systems with USB dual-role transceivers to function as USB on-the-go dual-role devices. True output disconnect and average output current limit features are included for short-circuit protection.

For automotive, firewire, and other high voltage applications, the LTC3576/LTC3576-1 provide Bat-Track control of an external LTC step-down switching regulator to maximize battery charger efficiency and minimize heat production. When power is available from both the USB and an auxiliary input, the auxiliary input is given priority.

The LTC3576/LTC3576-1 contain both an internal 180mΩ ideal diode as well as an ideal diode controller for use with an optional external P-channel MOSFET. The ideal diode(s) from BAT to V_{OUT} guarantee that ample power is always available to V_{OUT} even if there is insufficient or absent power at V_{BUS} or WALL.

An always-on LDO provides a regulated 3.3V from available power at V_{OUT}. Drawing very little quiescent current, this LDO will be on at all times and can be used to supply 20mA.

The LTC3576/LTC3576-1 feature an overvoltage protection circuit which is designed to work with an external N-channel MOSFET to prevent damage to their inputs caused by accidental application of high voltage.

To prevent battery drain when a device is connected to a suspended USB port, an LDO from V_{BUS} to V_{OUT} provides either low power or high power USB suspend current to the application.

The three general purpose switching regulators can be independently enabled either by direct digital control or by operating the I^2C serial port. Under I^2C control, all three switching regulators have adjustable set points so that voltages can be reduced when high processor performance is not needed. Along with constant frequency PWM mode, all three switching regulators have automatic Burst Mode operation and LDO modes for significantly reduced quiescent current under light load conditions.

OPERATION

Bidirectional PowerPath Switching Regulator—Step-Down Mode

The power delivered from V_{BUS} to V_{OUT} is controlled by a 2.25MHz constant frequency bidirectional switching regulator operating in step-down mode. V_{OUT} drives the combination of the external load (step-down switching regulators 1, 2 and 3) and the battery charger. To meet the maximum USB load specification, the switching regulator contains a measurement and control system that ensures that the average input current remains below the level programmed at CLPROG.

If the combined load does not cause the switching regulator to reach the programmed input current limit, V_{OUT} will track approximately 0.3V above the battery voltage. By keeping the voltage across the battery charger at this low level, power lost to the battery charger is minimized. Figure 1 shows the power flow in step-down mode.

If the combined external load plus battery charge current is large enough to cause the switching regulator to reach the programmed input current limit, the battery charger will reduce its charge current by precisely the amount necessary to enable the external load to be satisfied. Even if the battery charge current is programmed to exceed the allowable USB current, the USB specification for average input current will not be violated; the battery charger will reduce its current as needed. Furthermore, if the load current at V_{OUT} exceeds the programmed power from V_{BUS}, load current will be drawn from the battery via the ideal diode(s) even when the battery charger is enabled.

The current out of CLPROG is a precise fraction of the V_{BUS} current. When a programming resistor and an averaging capacitor are connected from CLPROG to GND, the voltage on CLPROG represents the average input current of the switching regulator. As the input current approaches the programmed limit, CLPROG reaches 1.18V and power delivered by the switching regulator is held constant.

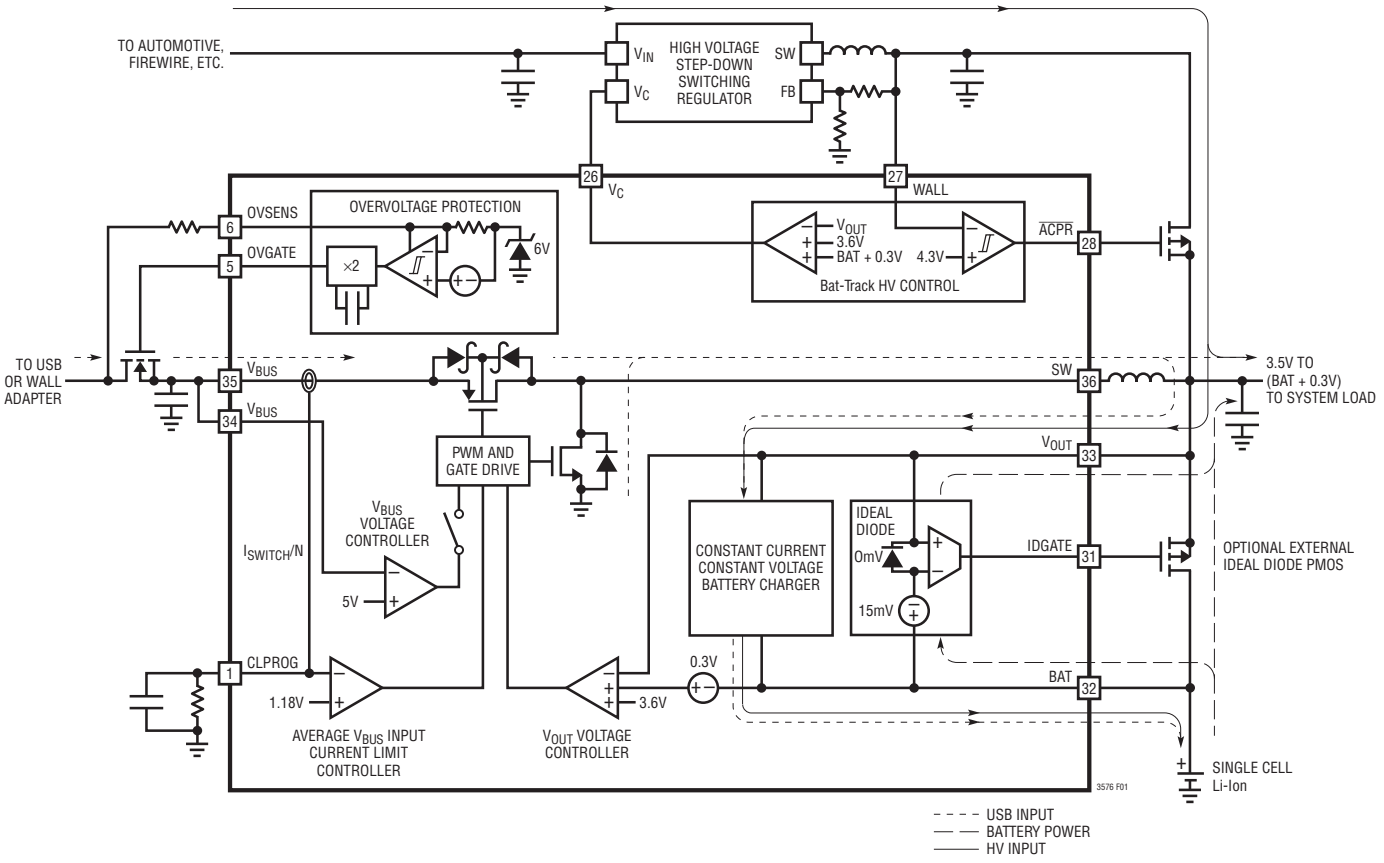


Figure 1. PowerPath Block Diagram—Power Available from USB/Wall Adapter

OPERATION

The input current limit is programmed by the I_{LIM0} and I_{LIM1} pins or by the I^2C serial port. The input current limit has five possible settings ranging from the USB suspend limit of 500µA up to 1A for wall adapter applications. Two of these settings are specifically intended for use in the 100mA and 500mA USB applications. Refer to Table 1 for current limit settings using the I_{LIM0} and I_{LIM1} pins and Table 6 for current limit settings using the I^2C port.

Table 1. USB Current Limit Settings Using I_{LIM0} and I_{LIM1}

I_{LIM1}	I_{LIM0}	USB SETTING
0	0	1× Mode (USB 100mA Limit)
0	1	10× Mode (Wall 1A Limit)
1	0	Low Power Suspend (USB 500µA Limit)
1	1	5× Mode (USB 500mA Limit)

When the switching regulator is activated, the average input current will be limited by the CLPROG programming resistor according to the following expression:

$$I_{VBUS} = I_{VBUSQ} + \frac{V_{CLPROG}}{R_{CLPROG}} \bullet \left(h_{CLPROG} + 1\right)$$

where I_{VBUSQ} is the quiescent current of the LTC3576/LTC3576-1, V_{CLPROG} is the CLPROG servo voltage in current limit, R_{CLPROG} is the value of the programming resistor and h_{CLPROG} is the ratio of the measured current at V_{BUS} to the sample current delivered to CLPROG. Refer to the Electrical Characteristics table for values of h_{CLPROG}, V_{CLPROG} and I_{VBUSQ}. Given worst-case circuit tolerances, the USB specification for the average input current in 100mA or 500mA mode will not be violated, provided that R_{CLPROG} is 3.01k or greater.

While not in current limit, the switching regulator's Bat-Track feature will set V_{OUT} to approximately 300mV above the voltage at BAT. However, if the voltage at BAT is below 3.3V, and the load requirement does not cause the switching regulator to exceed its current limit, V_{OUT} will regulate at a fixed 3.6V as shown in Figure 2. This instant-on operation will allow a portable product to run immediately when power is applied without waiting for the battery to charge. If the load does exceed the current limit at V_{BUS}, V_{OUT} will range between the no-load voltage and slightly below the battery voltage, indicated by the shaded region of Figure 2.

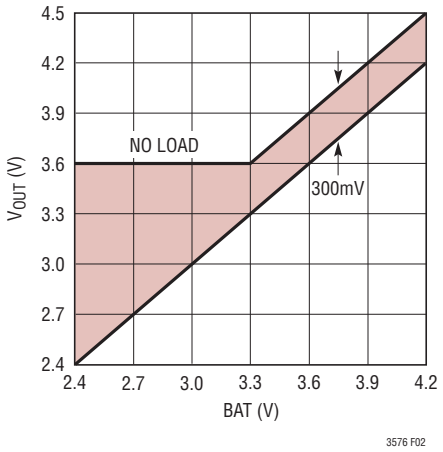


Figure 2. V_{OUT} vs BAT

For very low-battery voltages, the battery charger acts like a load and, due to limited input power, its current will tend to pull V_{OUT} below the 3.6V instant-on voltage. To prevent V_{OUT} from falling below this level, an undervoltage circuit automatically detects that V_{OUT} is falling and reduces the battery charge current as needed. This reduction ensures that load current and voltage are always prioritized while allowing as much battery charge current as possible. See Battery Charger Over Programming in the Applications Information section.

The voltage regulation loop is compensated by the capacitance on V_{OUT}. A 10µF MLCC capacitor is required for loop stability. Additional capacitance beyond this value will improve transient response.

An internal undervoltage lockout circuit monitors V_{BUS} and keeps the switching regulator off until V_{BUS} rises above 4.30V and is about 200mV above the battery voltage. Hysteresis on the UVLO turns off the regulator if V_{BUS} falls below 4V or to within 50mV of the battery voltage. When this happens, system power at V_{OUT} will be drawn from the battery via the ideal diode(s).

Bidirectional PowerPath Switching Regulator—Step-Up Mode

For USB on-the-go applications, the bidirectional PowerPath switching regulator acts as a step-up converter to deliver power from V_{OUT} to V_{BUS}. The power from V_{OUT} can come from the battery or the output of the external

OPERATION

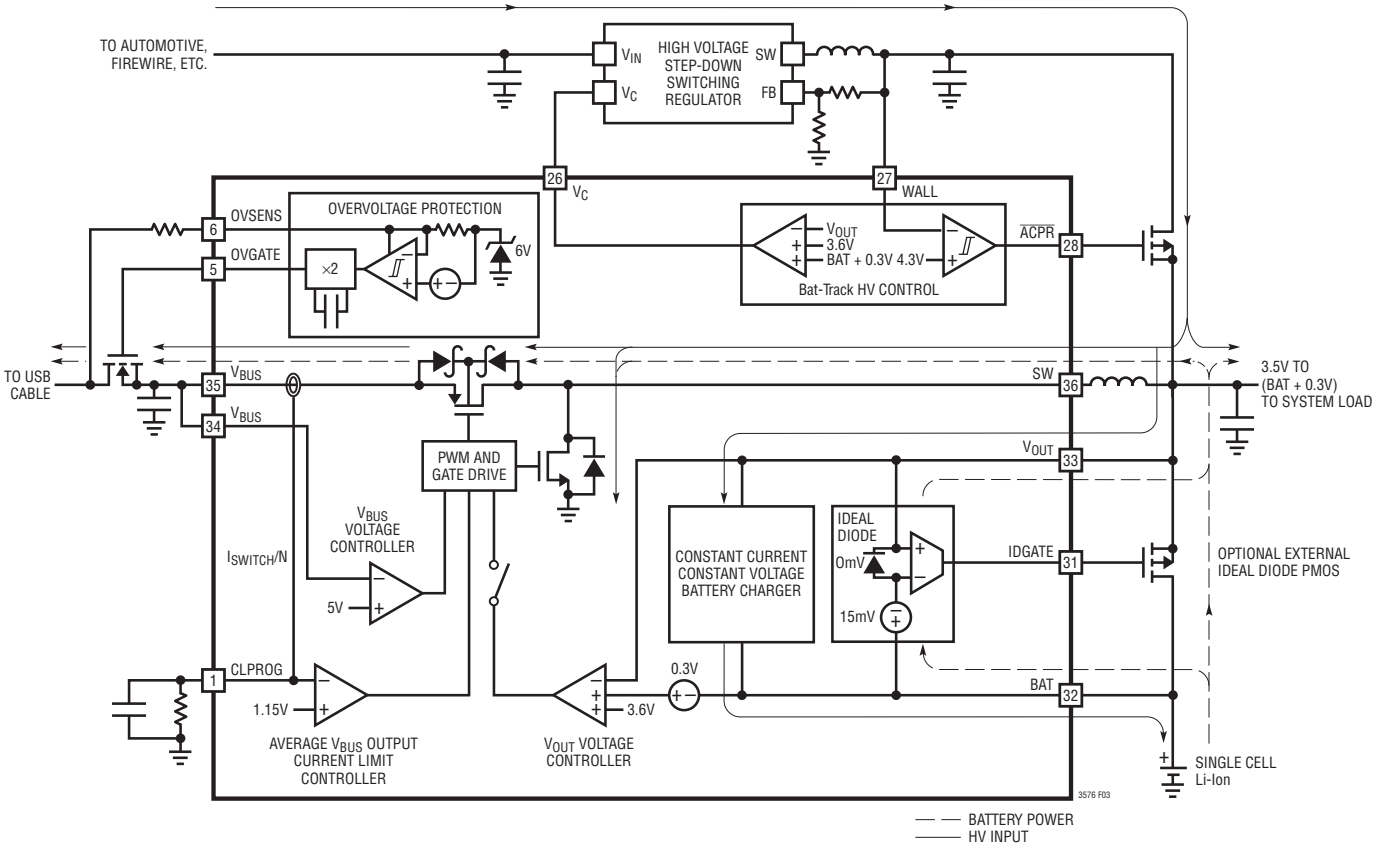


Figure 3. PowerPath Block Diagram—USB On-the-Go

high voltage switching regulator. As a step-up converter, the bidirectional switching regulator produces 5V on V_{BUS} and is capable of delivering at least 500mA. USB on-the-go can be enabled by either the external control pin, ENOTG, or via I^2C. Figure 3 shows the power flow in step-up mode.

An undervoltage lockout circuit monitors V_{OUT} and prevents step-up conversion until V_{OUT} rises above 2.8V. To prevent backdriving of V_{BUS} when input power is available, the V_{BUS} undervoltage lockout circuit prevents step-up conversion if V_{BUS} is greater than 4.3V at the time step-up mode is enabled. The switching regulator is also designed to allow true output disconnect by eliminating body diode conduction of the internal PMOS switch. This allows V_{BUS} to go to zero volts during a short-circuit condition or while shut down, drawing zero current from V_{OUT}.

The voltage regulation loop is compensated by the capacitance on V_{BUS}. A 4.7µF MLCC is required for loop stability. Additional capacitance beyond this value will improve transient response. The V_{BUS} voltage has approximately 3% load regulation up to an output current of 500mA. At light loads, the switching regulator goes into Burst Mode operation. The regulator will deliver power to V_{BUS} until it reaches 5.1V after which the NMOS and PMOS switches shut off. The regulator delivers power again to V_{BUS} once it falls below 5.1V.

The switching regulator features both peak inductor and average output current limit. The peak current mode architecture limits peak inductor current on a cycle-by-cycle basis. The peak current limit is equal to $V_{BUS}/2\Omega$ to a maximum of 1.8A so that in the event of a sudden short circuit, the current limit will fold back to a lower value. In step-up mode, the voltage on CLPROG represents the average output current of the switching regulator when a programming resistor and an averaging capacitor are connected from CLPROG to GND. With a 3.01k resistor on CLPROG, the bidirectional switching regulator has an output current limit of 680mA. As the output current ap-

OPERATION

proaches this limit CLPROG servos to 1.15V and V_{BUS} falls rapidly to V_{OUT}. When V_{BUS} is close to V_{OUT} there may not be sufficient negative slope on the inductor current when the PMOS switch is on to balance the rise in the inductor current when the NMOS switch is on. This will cause the inductor current to run away and the voltage on CLPROG to rise. When CLPROG reaches 1.2V the switching of the synchronous PMOS is terminated and V_{OUT} is applied statically to its gate. This ensures that the inductor current will have sufficient negative slope during the time current is flowing to the output. The PMOS will resume switching when CLPROG drops down to 1.15V.

The LTC3576/LTC3576-1 maintain voltage regulation even if V_{OUT} is above V_{BUS}. This is achieved by disabling the PMOS switch. The PMOS switch is enabled when V_{BUS} rises above V_{OUT} + 180mV and is disabled when it falls below V_{OUT} + 70mV to prevent the inductor current from running away when not in current limit. Since the PMOS no longer acts as a low impedance switch in this mode, there will be more power dissipation within the IC. This will cause a sharp drop in efficiency.

If V_{BUS} is less than 4V and the PMOS switch is disabled for more than 7.2ms a short-circuit fault will be declared and the part will shut off. The $\overline{CHRG}$ pin will blink at 35kHz with a duty cycle that varies between 12% and 88% at a 4Hz rate. See Table 2. To re-enable step-up mode, the ENOTG pin or, with ENOTG grounded, the B0 bit in the I^2C port must be cycled low and then high.

Bat-Track Auxiliary High Voltage Switching Regulator Control

The WALL, $\overline{ACPR}$ and V_C pins can be used in conjunction with an external high voltage step-down switching regulator such as the LT®3480 or the LT3653 to minimize heat production when operating from higher voltage sources, as shown in Figures 1 and 3. Bat-Track control circuitry regulates the external switching regulator's output voltage to the larger of (BAT + 300mV) or 3.6V. This maximizes battery charger efficiency while still allowing instant-on operation when the battery is deeply discharged.

The feedback network of the high voltage regulator should be set to generate an output voltage between 4.5V and 5.5V. When high voltage is applied to the external regulator, WALL will rise toward this programmed output voltage. When WALL exceeds approximately 4.3V, $\overline{ACPR}$ is brought low and the Bat-Track control of the LTC3576/LTC3576-1 overdrives the local V_C control of the external high voltage step-down switching regulator. Therefore, once the Bat-Track control is enabled, the output voltage is set independent of the switching regulator feedback network.

Bat-Track control provides a significant efficiency advantage over the simple use of a 5V switching regulator output to drive the battery charger. With a 5V output driving V_{OUT}, battery charger efficiency is approximately:

$$\eta_{TOTAL} = \eta_{BUCK} \bullet \frac{V_{BAT}}{5V}$$

where η_{BUCK} is the efficiency of the high voltage switching regulator and 5V is the output voltage of the switching regulator. With a typical switching regulator efficiency of 87% and a typical battery voltage of 3.8V, the total battery charger efficiency is approximately 66%. Assuming a 1A charge current, 1.7W of power is dissipated just to charge the battery!

With Bat-Track, battery charger efficiency is approximately:

$$\eta_{TOTAL} = \eta_{BUCK} \bullet \frac{V_{BAT}}{V_{BAT} + 0.3V}$$

With the same assumptions as above, the total battery charger efficiency is approximately 81%. This example works out to less than 1W of power dissipation, or almost 60% less heat.

See the Typical Applications section for complete circuits using the LT3480 and the LT3653 with Bat-Track control.

Ideal Diode(s) from BAT to V_{OUT}

The LTC3576/LTC3576-1 each have an internal ideal diode as well as a controller for an optional external ideal diode. Both the internal and the external ideal diodes are always on and will respond quickly whenever V_{OUT} drops below BAT.

If the load current increases beyond the power allowed from the switching regulator, additional power will be pulled from the battery via the ideal diode(s). Furthermore, if power to V_{BUS} (USB or wall adapter) is removed,

OPERATION

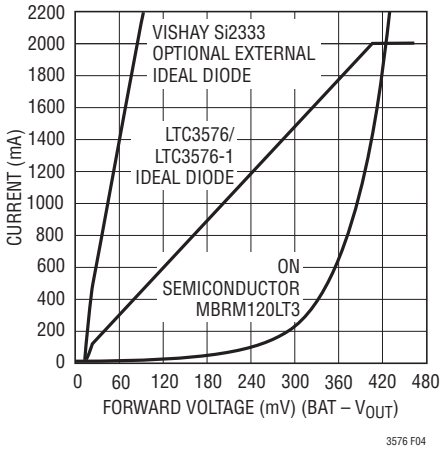


Figure 4. Ideal Diode V-I Characteristics

then all of the application power will be provided by the battery via the ideal diodes. The ideal diode(s) will be fast enough to keep V_{OUT} from drooping with only the storage capacitance required for the switching regulator. The internal ideal diode consists of a precision amplifier that activates a large on-chip P-channel MOSFET whenever the voltage at V_{OUT} is approximately 15mV (V_{FWD}) below the voltage at BAT. Within the amplifier's linear range, the small-signal resistance of the ideal diode will be quite low, keeping the forward drop near 15mV. At higher current levels, the MOSFET will be in full conduction.

To supplement the internal ideal diode, an external P-channel MOSFET may be added from BAT to V_{OUT}. The IDGATE pin of the LTC3576/LTC3576-1 drives the gate of the external P-channel MOSFET for automatic ideal diode control. The source of the external P-channel MOSFET should be connected to V_{OUT} and the drain should be connected to BAT. Capable of driving a 1nF load, the IDGATE pin can control an external P-channel MOSFET transistor having an on-resistance of 30mΩ or lower.

Suspend LDO

If the LTC3576/LTC3576-1 are configured for USB suspend mode, the bidirectional switching regulator is disabled and the suspend LDO provides power to the V_{OUT} pin (presuming there is power available to V_{BUS}). This LDO will prevent the battery from running down when the portable product has access to a suspended USB port. Regulating at 4.6V, this LDO only becomes active when the switching converter is disabled (suspended). The suspend LDO sends a scaled copy of the V_{BUS} current to the CLPROG pin, which will servo to approximately 100mV in this mode. To remain compliant with the USB specification, the input to the LDO is current limited so that it will not exceed the low power or high power suspend specification. If the load on V_{OUT} exceeds the suspend current limit, the additional current will come from the battery via the ideal diode(s).

3.3V Always-On LDO Supply

The LTC3576/LTC3576-1 include a low quiescent current low dropout regulator that is always powered. This LDO can be used to provide power to a system pushbutton controller, standby microcontroller or real time clock. Designed to deliver up to 20mA, the always-on LDO requires at least a 1µF low impedance ceramic bypass capacitor for compensation. The LDO is powered from V_{OUT}, and therefore will enter dropout at loads less than 20mA as V_{OUT} falls near 3.3V. If the LDO3V3 output is not used, it should be disabled by connecting it to V_{OUT}.

Battery Charger

The LTC3576/LTC3576-1 include a constant-current/constant-voltage battery charger with automatic recharge, automatic termination by safety timer, low voltage trickle charging, bad cell detection and thermistor sensor input for out-of-temperature charge pausing.

Battery Preconditioning

When a battery charge cycle begins, the battery charger first determines if the battery is deeply discharged. If the battery voltage is below V_{TRKL}, typically 2.85V, an automatic trickle charge feature sets the battery charge current to 10% of the programmed value. If the low voltage persists for more than 1/2 hour, the battery charger automatically terminates and indicates via the $\overline{CHRG}$ pin that the battery was unresponsive.

Once the battery voltage is above 2.85V, the charger begins charging in full power constant-current mode. The current delivered to the battery will try to reach $1030/R_{PROG}$. Depending on available input power and external load conditions, the battery charger may or may not be able to charge at the full programmed rate. The external load will always be prioritized over the battery charge current.

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Likewise, the USB current limit programming will always be observed and only additional power will be available to charge the battery. When system loads are light, battery charge current will be maximized.

Charge Termination

The battery charger has a built-in safety timer. When the voltage on the battery reaches the pre-programmed float voltage, the battery charger will regulate the battery voltage and the charge current will decrease naturally. Once the battery charger detects that the battery has reached the float voltage, the four hour safety timer is started. After the safety timer expires, charging of the battery will discontinue and no more current will be delivered.

Automatic Recharge

After the battery charger terminates, it will remain off drawing only microamperes of current from the battery. If the portable product remains in this state long enough, the battery will eventually self discharge. To ensure that the battery is always topped off, a charge cycle will automatically begin when the battery voltage falls below the recharge threshold which is typically 100mV less than the charger's float voltage. In the event that the safety timer is running when the battery voltage falls below the recharge threshold, it will reset back to zero. To prevent brief excursions below the recharge threshold from resetting the safety timer, the battery voltage must be below the recharge threshold for more than 1ms. The charge cycle and safety timer will also restart if the V_{BUS} UVLO cycles low and then high (e.g., V_{BUS} is removed and then replaced), or if the battery charger is cycled on and off by the I^2C port.

Charge Current

The charge current is programmed using a single resistor from PROG to ground. 1/1030th of the battery charge current is sent to PROG which will attempt to servo to 1.000V. Thus, the battery charge current will try to reach 1030 times the current in the PROG pin. The program resistor and the charge current are calculated using the following equation:

$$I_{CHG} = \frac{V_{PROG}}{R_{PROG}} \bullet 1030$$

In either the constant-current or constant-voltage charging modes, the voltage at the PROG pin will be proportional to the actual charge current delivered to the battery. Therefore, the actual charge current can be determined at any time by monitoring the PROG pin voltage and using the following equation:

$$I_{BAT} = \frac{V_{PROG}}{R_{PROG}} \bullet 1030$$

In many cases, the actual battery charge current, I_{BAT}, will be lower than I_{CHG} due to limited input power available and prioritization with the system load drawn from V_{OUT}.

The Battery Charger Flow Chart illustrates the battery charger's algorithm.

Charge Status Indication

The $\overline{CHRG}$ pin indicates the status of the battery charger. Four possible states are represented by $\overline{CHRG}$ which include charging, not charging, unresponsive battery and battery temperature out of range.

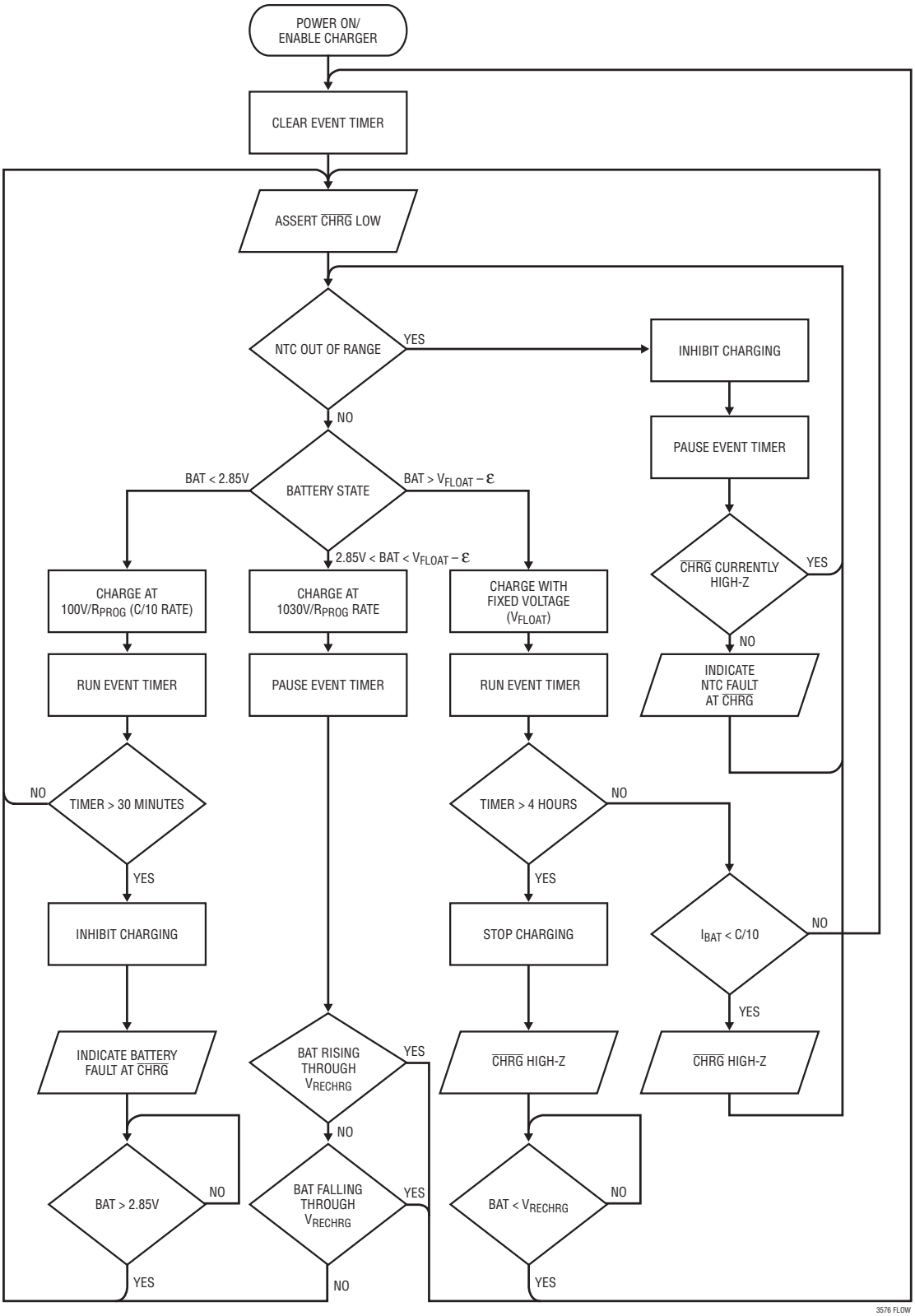
The signal at the $\overline{CHRG}$ pin can be easily recognized as one of the above four states by either a human or a microprocessor. An open-drain output, the $\overline{CHRG}$ pin can drive an indicator LED through a current limiting resistor for human interfacing or simply a pull-up resistor for microprocessor interfacing.

To make the $\overline{CHRG}$ pin easily recognized by both humans and microprocessors, the pin is either low for charging, high for not charging, or it is switched at high frequency (35kHz) to indicate the two possible faults, unresponsive battery and battery temperature out of range.

When charging begins, $\overline{CHRG}$ is pulled low and remains low for the duration of a normal charge cycle. When charging is complete, i.e., the BAT pin reaches the float voltage and the charge current has dropped to one-tenth of the programmed value, the $\overline{CHRG}$ pin is released (Hi-Z). If a fault occurs, the pin is switched at 35kHz. While switching, its duty cycle is modulated between a high and low value at a very low frequency. The low and high duty cycles are disparate enough to make an LED appear to be on or off thus giving the appearance of "blinking".

OPERATION

Battery Charger Flow Chart



OPERATION

Each of the two faults has its own unique "blink" rate for human recognition as well as two unique duty cycles for machine recognition.

The $\overline{CHRG}$ pin does not respond to the C/10 threshold if the LTC3576/LTC3576-1 is in V_{BUS} current limit. This prevents false end of charge indications due to insufficient power available to the battery charger.

Table 2 illustrates the four possible states of the $\overline{CHRG}$ pin when the battery charger is active.

Table 2. $\overline{CHRG}$ Signal

STATUS	FREQUENCY	MODULATION (BLINK) FREQUENCY	DUTY CYCLES
Charging	0Hz	0Hz (Low-Z)	100%
Not Charging	0Hz	0Hz (Hi-Z)	0%
NTC Fault	35kHz	1Hz at 50%	6%, 94%
Bad Battery or On-The-Go Short-Circuit Fault	35kHz	4Hz at 50%	12%, 88%

An NTC fault is represented by a 35kHz pulse train whose duty cycle alternates between 6% and 94% at a 1Hz rate. A human will easily recognize the 1Hz rate as a "slow" blinking which indicates the out-of-range battery temperature while a microprocessor will be able to decode either the 6% or 94% duty cycles as an NTC fault.

If a battery is found to be unresponsive to charging (i.e., its voltage remains below 2.85V for 1/2 hour), the $\overline{CHRG}$ pin gives the bad battery fault indication. For this fault, a human would easily recognize the 4Hz "fast" blink of the LED while a microprocessor would be able to decode either the 12% or 88% duty cycles as a bad battery fault.

Note that the LTC3576/LTC3576-1 are 3-terminal PowerPath products where system load is always prioritized over battery charging. Due to excessive system load, there may not be sufficient power to charge the battery beyond the trickle charge threshold voltage within the bad battery timeout period. In this case, the battery charger will falsely indicate a bad battery. System software may then reduce the load and reset the battery charger to try again.

In addition to charge status, the $\overline{CHRG}$ pin is also used to indicate whether there is a short-circuit condition on V_{BUS} when the bidirectional switching regulator is in on-the-go mode. When a short-circuit condition is detected, $\overline{CHRG}$ will blink with the same modulation frequency and duty cycle as a bad battery fault. If the charger is on at the same time that on-the-go is enabled, a 4Hz modulation of 12% and 88% duty cycles on $\overline{CHRG}$ could indicate a bad battery or a short-circuit fault on V_{BUS}. System software should turn off the charger or on-the-go to determine which fault has occurred.

Although very improbable, it is possible that a duty cycle reading could be taken at the bright-dim transition (low duty cycle to high duty cycle). When this happens the duty cycle reading will be precisely 50%. If the duty cycle reading is 50%, system software should disqualify it and take a new duty cycle reading.

NTC Thermistor

The battery temperature is measured by placing a negative temperature coefficient (NTC) thermistor close to the battery pack.

To use this feature connect the NTC thermistor, R_{NTC}, between the NTC pin and ground and a bias resistor, R_{NOM}, from NTCBIAS to NTC. R_{NOM} should be a 1% 200ppm resistor with a value equal to the value of the chosen NTC thermistor at 25°C (R25).

The LTC3576/LTC3576-1 pauses charging when the resistance of the NTC thermistor drops to 0.54 times the value of R25 or approximately 54k for a 100k thermistor. For a Vishay Curve 1 thermistor, this corresponds to approximately 40°C. If the battery charger is in constant voltage (float) mode, the safety timer also pauses until the thermistor indicates a return to a valid temperature. As the temperature drops, the resistance of the NTC thermistor rises. The LTC3576/LTC3576-1 are also designed to pause charging when the value of the NTC thermistor increases to 3.25 times the value of R25. For a Vishay Curve 1 100k thermistor, this resistance, 325k, corresponds to approximately 0°C. The hot and cold comparators each have approximately 3°C of hysteresis to prevent oscillation about the trip point. Grounding the NTC pin disables all NTC functionality.

OPERATION

Thermal Regulation

To prevent thermal damage to the LTC3576/LTC3576-1 or surrounding components, an internal thermal feedback loop will automatically decrease the programmed charge current if the die temperature rises to 105°C. This thermal regulation technique protects the LTC3576/LTC3576-1 from excessive temperature due to high power operation or high ambient thermal conditions, and allows the user to push the limits of the power handling capability with a given circuit board design. The benefit of the LTC3576/LTC3576-1 thermal regulation loop is that charge current can be set according to actual conditions rather than worst-case conditions for a given application with the assurance that the charger will automatically reduce the current in worst-case conditions.

Overvoltage Protection

The LTC3576/LTC3576-1 can protect itself from the inadvertent application of excessive voltage to V_{BUS} or WALL with just two external components: an N-channel MOSFET and a 6.2k resistor. The maximum safe overvoltage magnitude will be determined by the choice of the external MOSFET and its associated drain breakdown voltage.

The overvoltage protection module consists of two pins. The first, OVSENS, is used to measure the externally applied voltage through an external resistor. The second, OVGATE, is an output used to drive the gate pin of the external MOSFET. When OVSENS is below 6V, an internal charge pump will drive OVGATE to approximately 1.88 × OVSENS. This will enhance the N-channel MOSFET and provide a low impedance connection to V_{BUS} or WALL which will, in turn, power the LTC3576/LTC3576-1. If OVSENS should rise above 6V due to a fault or use of an incorrect wall adapter, OVGATE will be pulled to GND disabling the external MOSFET and therefore protecting downstream circuitry. When the voltage drops below 6V again, the external MOSFET will be re-enabled.

When USB on-the-go is enabled, the bidirectional switching regulator powers up the overvoltage protection circuit through the body diode of the external MOSFET, thus providing protection to the part even when V_{BUS} is sourcing power. When high voltage is applied to the drain of the external MOSFET, V_{BUS} will remain at 5V. Once the high voltage is removed, the drain of the external MOSFET will return to 5V.

The charge pump output on OVGATE has limited output drive capability. Care must be taken to avoid leakage on this pin as it may adversely affect operation.

See the Applications Information section for resistor power dissipation rating calculations, a table of recommended components, and examples of dual-input and reverse input protection.

I²C Interface

The LTC3576/LTC3576-1 may receive commands from a host (master) using the standard 2-wire I²C interface. The Timing Diagram shows the timing relationship of the signals on the bus. The two bus lines, SDA and SCL, must be HIGH when the bus is not in use. External pull-up resistors or current sources, such as the LTC1694 I²C accelerator, are required on these lines. The LTC3576/LTC3576-1are receive-only slave devices. The I²C control signals, SDA and SCL are scaled internally to the DV_{CC} supply. DV_{CC} should be connected to the same power supply as the microcontroller generating the I²C signals.

The I²C port has an undervoltage lockout on the DV_{CC} pin. When DV_{CC} is below approximately 1V, the I²C serial port is cleared and switching regulators 1, 2 and 3 are set to full scale.

Bus Speed

The I²C port is designed to be operated at speeds of up to 400kHz. It has built-in timing delays to ensure correct operation when addressed from an I²C compliant master device. It also contains input filters designed to suppress glitches should the bus become corrupted.

Start and Stop Conditions

A bus master signals the beginning of a communication to a slave device by transmitting a START condition. A START condition is generated by transitioning SDA from high to LOW while SCL is HIGH. When the master has finished communicating with the slave, it issues a STOP condition by transitioning SDA from LOW to HIGH while SCL is high. The bus is then free for communication with another I²C device.

OPERATION

Byte Format

Each byte sent to the LTC3576/LTC3576-1 must be eight bits long followed by an extra clock cycle for the acknowledge bit. The data should be sent to the LTC3576/LTC3576-1 with the most significant bit (MSB) first.

Acknowledge

The acknowledge signal is used for handshaking between the master and the slave. An acknowledge (active low) generated by the slave (LTC3576/LTC3576-1) lets the master know that the latest byte of information was received. The acknowledge related clock pulse is generated by the master. The master releases the SDA line (HIGH) during the acknowledge clock cycle. The slave-receiver must pull down the SDA line during the acknowledge clock pulse so that it remains a stable LOW during the HIGH period of this clock pulse.

Slave Address

The address byte consists of the 7-bit address and the read/$\overline{\text{write}}$ (R/$\overline{W}$) bit. The LTC3576/LTC3576-1 respond to only one 7-bit address which has been factory programmed to 0001001. The R/$\overline{W}$ bit is the least significant bit of the address byte. It must be 0 for the LTC3576/LTC3576-1 to recognize the address since they are write only devices. Thus the address byte is 0x12. If the correct seven bit address is given but the R/$\overline{W}$ bit is 1, the LTC3576/LTC3576-1 will not respond.

Sub-Addressed Writing

The LTC3576/LTC3576-1 have four command registers for control input. They are accessed by the I^2C port via a sub-addressed writing system.

Each write to the LTC3576/LTC3576-1 consists of three bytes. The first byte is always the LTC3576/LTC3576-1's write address. The second byte represents the LTC3576/LTC3576-1's sub-address. The sub-address acts as pointer to direct the subsequent data byte within the LTC3576/LTC3576-1. The third byte consists of the data to be written to the location pointed to by the sub-address. The LTC3576/LTC3576-1 contain four sub-addresses at locations 0x00, 0x01, 0x02 and 0x03.

Bus Write Operation

The master initiates communication with the LTC3576/LTC3576-1 with a START condition and a 7-bit address followed by the R/$\overline{W}$ bit = 0. If the address matches that of the LTC3576/LTC3576-1, the LTC3576/LTC3576-1 return an acknowledge. The master should then deliver the sub-address. Again the LTC3576/LTC3576-1 acknowledge and the cycle is repeated for the data byte. The data byte is transferred to an internal holding latch upon the return of its acknowledge by the LTC3576/LTC3576-1. This procedure must be repeated for each sub-address that requires new data. After one or more data bytes have been transferred to the LTC3576/LTC3576-1, the master may terminate the communication with a STOP condition. Alternatively, a repeated START condition can be initiated by the master and another chip on the I^2C bus can be addressed. This cycle can continue indefinitely and the LTC3576/LTC3576-1 remembers the last input of valid data that it received. Once all chips on the bus have been addressed and sent valid data, a global STOP condition can be sent and the LTC3576/LTC3576-1 will update their command latches with the data that they have received.

In certain circumstances the data on the I^2C bus may become corrupted. In these cases, the LTC3576/LTC3576-1 respond appropriately by preserving only the last set of complete data that they have received. For example, assume the LTC3576/LTC3576-1 have been successfully addressed and are receiving data when a STOP condition mistakenly occurs. The LTC3576/LTC3576-1 will ignore this STOP condition and will not respond until a new START condition, correct address and sub-address, new set of data and STOP condition are transmitted.

Likewise, with only one exception, if the LTC3576/LTC3576-1 were previously addressed and sent valid data but not updated with a STOP, they will respond to any STOP that appears on the bus, independent of the number of repeated STARTs that have occurred. If a repeated START is given and the LTC3576/LTC3576-1 successfully acknowledge their address and sub-address, they will not respond to a STOP until a full byte of the new data has been received and acknowledged.

OPERATION

Input Data

Table 3 illustrates the four data bytes that may be written to the LTC3576/LTC3576-1.

The first byte at sub-address 0 controls the servo voltage for switching regulators 1 and 2. The second byte at sub-address 1 controls the servo voltage of switching regulator 3 and the enable signals for all three switching regulators, as well as the enable signal for the PowerPath switching regulator to power up V_{BUS} for USB on-the-go. The servo voltages are decoded in Table 4. The default servo voltage is 0.8V.

Table 3. I²C Serial Port Mapping*

	A7	A6	A5	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0
	Switching Regulator 1 Voltage (See Table 4)				Switching Regulator 2 Voltage (See Table 4)				Switching Regulator 3 Voltage (See Table 4)				ENABLE 3	ENABLE 2	ENABLE 1	ENABLE OTG
Reset Value	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0
	C7	C6	C5	C4	C3	C2	C1	C0	D7	D6	D5	D4	D3	D2	D1	D0
	Switching Regulator 1 Modes (See Table 5)		Switching Regulator 2 Modes (See Table 5)		Switching Regulator 3 Modes (See Table 5)		Input Current Limit (See Table 6)		DISABLE BATTERY CHARGER	HIGH POWER SUSPEND	Unused					
Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

*The A7-A0 and B7-B4 bits default to 1 and all other bits default to 0 when the chip is powered and DV_{CC} = 0.

Table 4. Switching Regulator Servo Voltage

A7	A6	A5	A4	Switching Regulator 1 Servo Voltage
A3	A2	A1	A0	Switching Regulator 2 Servo Voltage
B7	B6	B5	B4	Switching Regulator 3 Servo Voltage
0	0	0	0	0.425
0	0	0	1	0.450
0	0	1	0	0.475
0	0	1	1	0.500
0	1	0	0	0.525
0	1	0	1	0.550
0	1	1	0	0.575
0	1	1	1	0.600
1	0	0	0	0.625
1	0	0	1	0.650
1	0	1	0	0.675
1	0	1	1	0.700
1	1	0	0	0.725
1	1	0	1	0.750
1	1	1	0	0.775
1	1	1	1	0.800

OPERATION

The third data byte at sub-address 2 controls the operating modes of each switching regulator as well as the input current limit settings. Each switching regulator can be independently set to one of three operating modes listed in Table 5.

Table 5. General Purpose Switching Regulator Modes

C7 (SDA)*	C6 (SCL)*	Switching Regulator 1 Mode
C5 (SDA)*	C4 (SCL)*	Switching Regulator 2 Mode
C3 (SDA)*	C2 (SCL)*	Switching Regulator 3 Mode
0	X	Pulse-Skipping Mode
1	0	LDO Mode
1	1	Burst Mode Operation

*SDA and SCL take on this context only when DV_{CC} = 0V.

The input current limit settings are decoded according to Table 6. This table indicates the maximum current that will be drawn from the V_{BUS} pin in the event that the load at V_{OUT} (battery charger plus system load) exceeds the power available. Any additional power will be drawn from the battery. The start-up state for the input current limit setting is 00 representing the low power 100mA USB setting.

Table 6. USB Current Limit Settings

D6	C1 (I_{LIM1})*	C0 (I_{LIM0})*	USB SETTING
X	0	0	1× Mode (USB 100mA Limit)
X	0	1	10× Mode (Wall 1A Limit)
0	1	0	Low Power Suspend (USB 500µA Limit)
1	1	0	High Power Suspend (USB 2.5mA Limit)
X	1	1	5× Mode (USB 500mA Limit)

*I_{LIM1} and I_{LIM0} can only be used to enable the low power suspend mode and are logically ORed with C1 and C0, respectively.

The fourth and final byte of input data at sub-address 3 provides bits for disabling the battery charger and enabling the high power suspend mode current limit of 2.5mA.

Disabling the I²C Port

The I²C serial port can be disabled by grounding the DV_{CC} pin. In this mode, the LTC3576/LTC3576-1 are controlled through the individual logic input pins EN1, EN2, EN3, ENOTG, I_{LIM0}, I_{LIM1}, SDA and SCL. Some functionality is not available in this mode such as the programmability of switching regulators 1, 2 and 3's output voltage, the battery charger disable feature and the high power suspend mode. In this mode, the programmable switching regulators have a fixed servo voltage of 0.8V. Because the SDA and SCL pins have no other context when DV_{CC} is grounded, these pins are re-mapped to control the switching regulator mode bits C2 to C7. SCL maps to C2, C4 and C6 while SDA maps to C3, C5 and C7.

$\overline{RST3}$ Pin

The $\overline{RST3}$ pin is an open-drain output used to indicate that switching regulator 3 has been enabled and has reached its final voltage. $\overline{RST3}$ remains low impedance until regulator 3 reaches 92% of its regulation value.

A 230ms delay is included to allow a system microcontroller ample time to reset itself. $\overline{RST3}$ may be used as a power-on reset to the microprocessor powered by regulator 3 or may be used to enable regulators 1 and/or 2 for supply sequencing. $\overline{RST3}$ is an open-drain output and requires a pull-up resistor to the output voltage of regulator 3 or another appropriate power source.

Shutdown Mode

The bidirectional USB switching regulator in step-down mode is enabled whenever V_{BUS} is above V_{UVLO} and the LTC3576/LTC3576-1are not in one of the two USB suspend modes (500µA or 2.5mA). When power is available from both the USB and auxiliary inputs, the auxiliary input is given priority and the USB switching regulator is disabled.

The ideal diode(s) are enabled at all times and cannot be disabled.

OPERATION

Step-Down Switching Regulators

The LTC3576/LTC3576-1 contain three general purpose 2.25MHz step-down constant-frequency current mode switching regulators. Two regulators provide up to 400mA and a third switching regulator can provide up to 1A. All three switching regulators can be programmed for a minimum start-up output voltage of 0.8V and can be used to power a microcontroller core, microcontroller I/O, memory, disk drive or other logic circuitry. All three switching regulators have I^2C programmable set points for on-the-fly power savings. They also support 100% duty cycle operation (low dropout mode) when their input voltage drops very close to their output voltage. To suit a variety of applications, selectable mode functions can be used to trade off noise for efficiency. Three modes are available to control the operation of the LTC3576/LTC3576-1's general purpose switching regulators. At moderate to heavy loads, the pulse skip mode provides the lowest noise switching solution. At lighter loads, Burst Mode operation or LDO mode may be selected. The switching regulators include soft-start to limit inrush current when powering on, short-circuit current protection and switch node slew limiting circuitry to reduce radiated EMI. No external compensation components are required. The operating mode of the regulators may be set by either I^2C control or by manual control of the SDA and SCL pins if the I^2C port is not used. Each converter may be individually enabled by either their external control pins EN1, EN2, EN3 or by the I^2C port. All three switching regulators have individual programmable feedback servo voltages via I^2C control. The switching regulator input supplies V_{IN1}, V_{IN2} and V_{IN3} will generally be connected to the system load pin V_{OUT}.

Step-Down Switching Regulator Operating Modes

The LTC3576/LTC3576-1's general purpose switching regulators include three possible operating modes to meet the noise/power needs of a variety of applications.

In pulse-skipping mode, an internal latch is set at the start of every cycle which turns on the main P-channel MOSFET switch. During each cycle, a current comparator compares the peak inductor current to the output of an error amplifier. The output of the current comparator resets the internal latch which causes the main P-channel MOSFET switch to turn off and the N-channel MOSFET synchronous rectifier to turn on. The N-channel MOSFET synchronous rectifier turns off at the end of the 2.25MHz cycle or if the current through the N-channel MOSFET synchronous rectifier drops to zero. Using this method of operation, the error amplifier adjusts the peak inductor current to deliver the required output power. All necessary compensation is internal to the switching regulator requiring only a single ceramic output capacitor for stability. At light loads in PWM mode, the inductor current may reach zero on each pulse which will turn off the N-channel MOSFET synchronous rectifier. In this case, the switch node (SW) goes high impedance and the switch node voltage will "ring". This is discontinuous mode operation, and is normal behavior for a switching regulator. At very light loads in pulse-skipping mode, the switching regulators will automatically skip pulses as needed to maintain output regulation.

At high duty cycles ($V_{OUTx} > V_{INx}/2$) it is possible for the inductor current to reverse, causing the regulator to operate continuously at light loads. This is normal and regulation is maintained, but the supply current will increase to several mA due to continuous switching.

OPERATION

In Burst Mode operation, the switching regulator automatically switches between fixed frequency PWM operation and hysteretic control as a function of the load current. At light loads, the regulator operates in hysteretic mode and uses a constant current algorithm to control the inductor current. While in Burst Mode operation, the output capacitor is charged to a voltage slightly higher than the regulation point. The step-down switching regulator then goes into sleep mode, during which the output capacitor provides the load current. In sleep mode, most of the regulator's circuitry is powered down, conserving battery power. When the output voltage drops below a pre-determined value, the switching regulator circuitry is powered on and another burst cycle begins. The duration for which the regulator operates in sleep mode depends on the load current. The sleep time decreases as the load current increases. Burst Mode operation provides a significant improvement in efficiency at light loads at the expense of higher output ripple when compared to pulse-skipping mode. At heavy loads Burst Mode operation functions in the same manner as pulse-skipping mode.

Finally, the switching regulators have an LDO mode that gives a DC option for regulating their output voltages. In LDO mode, the switching regulators are converted to linear regulators and deliver continuous power from their SWx pins through their respective inductors. This mode gives the lowest possible output noise as well as low quiescent current at light loads.

The step-down switching regulators allow on-the-fly mode transitions, providing seamless transition between modes even under load. This allows the user to switch back and forth between modes to reduce output ripple or increase low current efficiency as needed.

Step-Down Switching Regulator Dropout Operation

It is possible for a switching regulator's input voltage, V_{INx}, to approach its programmed output voltage (e.g., a battery voltage of 3.4V with a programmed output voltage of 3.3V). When this happens, the PMOS switch duty cycle increases until it is turned on continuously at 100%. In this dropout condition, the respective output voltage equals the regulator's input voltage minus the voltage drops across the internal P-channel MOSFET and the inductor.

Step-Down Switching Regulator Low Supply Operation

The LTC3576/LTC3576-1 incorporate an undervoltage lockout circuit on V_{OUT} which shuts down the general purpose switching regulators when V_{OUT} drops below $V_{OUT(UVLO)}$. This UVLO prevents unstable operation.

Step-Down Switching Regulator Soft-Start Operation

Soft-start is accomplished by gradually increasing the peak inductor current for each switching regulator over a 500µs period. This allows each output to rise slowly, helping minimize the battery surge current. A soft-start cycle occurs whenever a given switching regulator is enabled, or after a fault condition has occurred (thermal shutdown or UVLO). A soft-start cycle is not triggered by changing operating modes. This allows seamless output operation when transitioning between Burst Mode operation, pulse-skipping mode or LDO mode.

Step-Down Switching Regulator Switching Slew Rate Control

The step-down switching regulators contain new patent pending circuitry to limit the slew rate of the switch node (SWx). This new circuitry is designed to transition the switch node over a period of a couple of nanoseconds, significantly reducing radiated EMI and conducted supply noise.

Step-Down Switching Regulator in Shutdown

The step-down switching regulators are in shutdown when not enabled for operation. In shutdown, all circuitry in the step-down switching regulator is disconnected from the switching regulator input supply leaving only a few nanoamperes of leakage current. The step-down switching regulator outputs are individually pulled to ground through a 10k resistor on their SWx pins when in shutdown.

APPLICATIONS INFORMATION

Bidirectional PowerPath Switching Regulator CLPROG Resistor and Capacitor Selection

As described in the Bidirectional Switching Regulator—Step-Down Mode section, the resistor on the CLPROG pin determines the average V_{BUS} input current limit when the switching regulator is set to either the 1× mode (USB 100mA), the 5× mode (USB 500mA) or the 10× mode. The V_{BUS} input current will be comprised of two components, the current that is used to drive V_{OUT} and the quiescent current of the switching regulator. To ensure that the USB specification is strictly met, both components of the input current should be considered. The Electrical Characteristics table gives the typical values for quiescent currents in all settings as well as current limit programming accuracy. To get as close to the 500mA or 100mA specifications as possible, a precision resistor should be used. Recall that:

$$I_{VBUS} = I_{VBUSQ} + V_{CLPROG}/R_{CLPPROG} \bullet (h_{CLPROG} + 1).$$

An averaging capacitor is required in parallel with the resistor so that the switching regulator can determine the average input current. This capacitor also provides the dominant pole for the feedback loop when current limit is reached. To ensure stability, the capacitor on CLPROG should be 0.1µF or larger.

Bidirectional PowerPath Switching Regulator Inductor Selection

Because the input voltage range and output voltage range of the PowerPath switching regulator are both fairly narrow, the LTC3576/LTC3576-1 were designed for a specific inductance value of 3.3µH. Some inductors which may be suitable for this application are listed in Table 7.

Table 7. Recommended PowerPath Inductors for the LTC3576

INDUCTOR TYPE	L (µH)	MAX I_{DC} (A)	MAX DCR (Ω)	SIZE IN mm (L × W × H)	MANUFACTURER
LPS4018	3.3	2.2	0.08	3.9 × 3.9 × 1.7	Coilcraft www.coilcraft.com
D53LC DB318C	3.3 3.3	2.26 1.55	0.034 0.070	5 × 5 × 3 3.8 × 3.8 × 1.8	Toko www.toko.com
WE-TPC Type M1	3.3	1.95	0.065	4.8 × 4.8 × 1.8	Wurth Electronik www.we-online.com
CDRH6D12 CDRH6D38	3.3 3.3	2.2 3.5	0.063 0.020	6.7 × 6.7 × 1.5 7 × 7 × 4	Sumida www.sumida.com

Bidirectional PowerPath Switching Regulator V_{BUS} and V_{OUT} Bypass Capacitor Selection

The type and value of capacitors used with the LTC3576/LTC3576-1 determine several important parameters such as regulator control-loop stability and input voltage ripple. Because the LTC3576/LTC3576-1 use a bidirectional switching regulator between V_{BUS} and V_{OUT}, the V_{BUS} current waveform contains high frequency components. It is strongly recommended that a low equivalent series resistance (ESR) multilayer ceramic capacitor (MLCC) be used to bypass V_{BUS}. Tantalum and aluminum capacitors are not recommended because of their high ESR. The value of the capacitor on V_{BUS} directly controls the amount of input ripple for a given load current. Increasing the size of this capacitor will reduce the input ripple.

The inrush current limit specification for USB devices is calculated in terms of the total number of Coulombs needed to charge the V_{BUS} bypass capacitor to 5V. The maximum inrush charge for USB on-the-go devices is 33µC. This places a limit of 6.5µF of capacitance on V_{BUS} assuming a linear capacitor. However, most ceramic capacitors have a capacitance that varies with bias voltage. The average capacitance needs to be less than 6.5µF over a 0V to 5V bias voltage range to meet the inrush current limit specification. A 10µF capacitor in a 0805 package, such as the Murata GRM21BR71A106KE51L would be a suitable V_{BUS} bypass capacitor. If more capacitance is required for better noise performance and stability it should be connected directly to the V_{BUS} pin when using the overvoltage protection circuit. This extra capacitance will be soft-connected over several milliseconds to limit inrush current and avoid excessive transient voltage drops on V_{BUS}.

To prevent large V_{OUT} voltage steps during transient load conditions, it is also recommended that an MLCC be used to bypass V_{OUT}. The output capacitor is used in the compensation of the switching regulator. At least 10µF with low ESR are required on V_{OUT}. Additional capacitance will improve load transient performance and stability.

MLCCs typically have exceptional ESR performance. MLCCs combined with a tight board layout and an unbroken ground plane will yield very good performance and low EMI emissions.

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There are MLCCs available with several types of dielectrics each having considerably different characteristics. For example, X7R MLCCs have the best voltage and temperature stability. X5R MLCCs have apparently higher packing density but poorer performance over their rated voltage and temperature ranges. Y5V MLCCs have the highest packing density, but must be used with caution, because of their extreme nonlinear characteristic of capacitance versus voltage. The actual in-circuit capacitance of a ceramic capacitor should be measured with a small AC signal and DC bias as is expected in-circuit. Many vendors specify the capacitance versus voltage with a $1V_{RMS}$ AC test signal and, as a result, over state the capacitance that the capacitor will present in the application. Using similar operating conditions as the application, the user must measure or request from the vendor the actual capacitance to determine if the selected capacitor meets the minimum capacitance that the application requires.

Step-Down Switching Regulator Output Voltage Programming

All three switching regulators have I^2C programmable set points and can be programmed for start-up output voltages of at least 0.8V. The full-scale output voltage for each switching regulator is programmed using a resistor divider from the switching regulator output connected to the FBx pins such that:

$$V_{OUTx} = V_{FBx}\left(\frac{R1}{R2}+1\right)$$

where V_{FBx} ranges from 0.425V to 0.8V. See Figure 5.

Typical values for R1 are in the range of 40k to 1M. The capacitor C_{FB} cancels the pole created by feedback resistors and the input capacitance of the FBx pin and also helps to improve transient response for output voltages much greater than 0.8V. A variety of capacitor sizes can be used for C_{FB} but a value of 10pF is recommended for most applications. Experimentation with capacitor sizes between 2pF and 22pF may yield improved transient response.

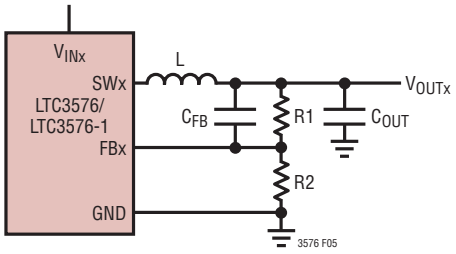


Figure 5. Buck Converter Application Circuit

Step-Down Switching Regulator Inductor Selection

Many different sizes and shapes of inductors are available from numerous manufacturers. Choosing the right inductor from such a large selection of devices can be overwhelming, but following a few basic guidelines will make the selection process much simpler.

The general purpose step-down converters are designed to work with inductors in the range of 2µH to 10µH. For most applications a 4.7µH inductor is suggested for the lower current switching regulators 1 and 2 and 2µH is recommended for the higher current switching regulator 3. Larger value inductors reduce ripple current which improves output ripple voltage. Lower value inductors result in higher ripple current and improved transient response time. To maximize efficiency, choose an inductor with a low DC resistance. For a 1.2V output, efficiency is reduced about 2% for 100mΩ series resistance at 400mA load current, and about 2% for 300mΩ series resistance at 100mA load current. Choose an inductor with a DC current rating at least 1.5 times larger than the maximum load current to ensure that the inductor does not saturate during normal operation. If output short circuit is a possible condition, the inductor should be rated to handle the maximum peak current specified for the step-down converters. Different core materials and shapes will change the size/current and price/current relationship of an inductor. Toroid or shielded pot cores in ferrite or Permalloy materials are small and don't radiate much energy, but generally cost more than powdered iron core inductors with similar electrical characteristics. Inductors that are very thin or have a very small volume typically have much higher core and DCR losses, and will not give the best efficiency. The choice of which style inductor to use often depends more on the price vs size, performance and any radiated EMI requirements than on what the LTC3576/LTC3576-1 require to operate.

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The inductor value also has an effect on Burst Mode operation. Lower inductor values will cause the Burst Mode operation switching frequency to increase.

Table 8 shows several inductors that work well with the LTC3576/LTC3576-1's general purpose regulators. These inductors offer a good compromise in current rating, DCR and physical size. Consult each manufacturer for detailed information on their entire selection of inductors.

Table 8. Recommended Inductors

INDUCTOR TYPE	L (µH)	MAX I_{DC} (A)	MAX DCR (Ω)	SIZE IN mm (L × W × H)	MANUFACTURER
DE2818C	4.7	1.25	0.072	3.0 × 2.8 × 1.8	Toko
	3.3	1.45	0.053	3.0 × 2.8 × 1.8	www.toko.comm
D312C	4.7	0.79	0.24	3.6 × 3.6 × 1.2	
	3.3	0.90	0.20	3.6 × 3.6 × 1.2	
	2.2	1.14	0.14	3.6 × 3.6 × 1.2	
DE2812C	4.7	1.2	1.13*	3.0 × 2.8 × 1.2	
	3.3	1.4	0.10*	3.0 × 2.8 × 1.2	
	2.0	1.8	0.067*	3.0 × 2.8 × 1.2	
CDRH3D16	4.7	0.9	0.11	4.0 × 4.0 × 1.8	Sumida
	3.3	1.1	0.085	4.0 × 4.0 × 1.8	www.sumida.com
	2.2	1.2	0.072	4.0 × 4.0 × 1.8	
CDRH2D11	4.7	0.5	0.17	3.2 × 3.2 × 1.2	
	3.3	0.6	0.123	3.2 × 3.2 × 1.2	
	2.2	0.78	0.098	3.2 × 3.2 × 1.2	
CLS4D09	4.7	0.75	0.19	4.9 × 4.9 × 1.0	
SD3118	4.7	1.3	0.162	3.1 × 3.1 × 1.8	Cooper
	3.3	1.59	0.113	3.1 × 3.1 × 1.8	www.cooperet.com
	2.2	2.0	0.074	3.1 × 3.1 × 1.8	
SD3112	4.7	0.8	0.246	3.1 × 3.1 × 1.2	
	3.3	0.97	0.165	3.1 × 3.1 × 1.2	
	2.2	1.12	0.14	3.1 × 3.1 × 1.2	
SD12	4.7	1.29	0.117*	5.2 × 5.2 × 1.2	
	3.3	1.42	0.104*	5.2 × 5.2 × 1.2	
	2.2	1.80	0.075*	5.2 × 5.2 × 1.2	
SD10	4.7	1.08	0.153*	5.2 × 5.2 × 1.0	
	3.3	1.31	0.108*	5.2 × 5.2 × 1.0	
	2.2	1.65	0.091*	5.2 × 5.2 × 1.0	
LPS3015	4.7	1.1	0.2	3.0 × 3.0 × 1.5	Coilcraft
	3.3	1.3	0.13	3.0 × 3.0 × 1.5	www.coilcraft.com
	2.2	1.5	0.11	3.0 × 3.0 × 1.5	

*Typical DCR

Step-Down Switching Regulator Input/Output Bypass Capacitor Selection

Low ESR (equivalent series resistance) MLCCs should be used at each switching regulator output as well as at each switching regulator input supply (V_{INx}). Only X5R or X7R ceramic capacitors should be used because they retain their capacitance over wider voltage and temperature ranges than other ceramic types. A 10µF output capacitor is sufficient for most applications. For good transient response and stability the output capacitor should retain at least 4µF of capacitance over operating temperature and bias voltage. Each switching regulator input supply should be bypassed with a 1µF capacitor. Consult with capacitor manufacturers for detailed information on their selection and specifications of ceramic capacitors. Many manufacturers now offer very thin (<1mm tall) ceramic capacitors ideal for use in height-restricted designs. Table 9 shows a list of several ceramic capacitor manufacturers.

Table 9. Recommended Ceramic Capacitor Manufacturers

AVX	www.avxcorp.com
Murata	www.murata.com
Taiyo Yuden	www.t-yuden.com
Vishay Siliconix	www.vishay.com
TDK	www.tdk.com

Overvoltage Protection

V_{BUS} can be protected from overvoltage damage with two additional components, a resistor R1 and an N-channel MOSFET MN1, as shown in Figure 6. Suitable choices for MN1 are listed in Table 10.

Table 10. Recommended N-channel MOSFETs for the Overvoltage Protection Circuit

PART NUMBER	BVDSS	R_{ON}	PACKAGE
Si1472DH	30V	82mΩ	SC70-6
Si2302ADS	20V	60mΩ	SOT-23
Si2306BDS	30V	65mΩ	SOT-23
Si2316BDS	30V	80mΩ	SOT-23
IRLML2502	20V	35mΩ	SOT-23
FDN372S	30V	50mΩ	SOT-23
NTLJS4114N	30V	35mΩ	WDFN6

R1 is a 6.2k resistor and must be rated for the power dissipated during maximum overvoltage. In an overvoltage condition the OVSENS pin will be clamped at 6V. R1 must be sized appropriately to dissipate the resultant power. For example, a 1/10W 6.2k resistor can have at most $\sqrt{P_{MAX} \bullet 6.2k\Omega} = 25V$ applied across its terminals. With the 6V at OVSENS, the maximum overvoltage magnitude that this resistor can withstand is 31V. A 1/4W 6.2k resistor raises this value to 45V. OVSENS's absolute maximum current rating of 10mA imposes an upper limit of 68V protection.

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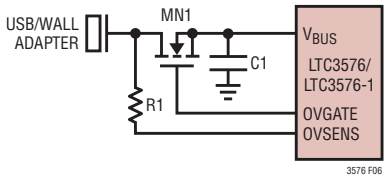


Figure 6. Overvoltage Protection

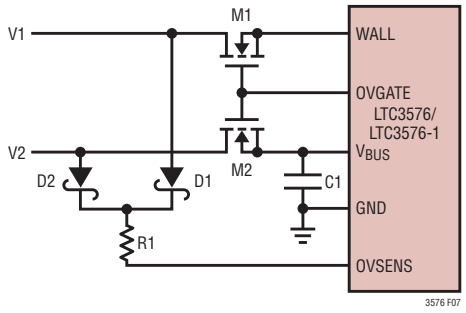


Figure 7. Dual-Input Overvoltage Protection

It is possible to protect both V_{BUS} and WALL from overvoltage damage with several additional components, as shown in Figure 7. Schottky diodes D1 and D2 pass the larger of V1 and V2 to R1 and OVSENS. If either V1 or V2 exceeds 6V plus V_F (Schottky), OVGATE will be pulled to GND and both the WALL and USB inputs will be protected. Each input is protected up to the drain-source breakdown, BVDSS, of MN1 and MN2. R1 must also be rated for the power dissipated during maximum overvoltage.

Reverse Voltage Protection

The LTC3576/LTC3576-1 can also be easily protected against the application of reverse voltages, as shown in Figure 8. D1 and R1 are necessary to limit the maximum V_{GS} seen by MP1 during positive overvoltage events. D1's breakdown voltage must be safely below MP1's BVGS. The circuit shown in Figure 8 offers forward voltage protection up to MN1's BVDSS and reverse voltage protection up to MP1's BVDSS.

Battery Charger Over Programming

The USB high power specification allows for up to 2.5W to be drawn from the USB port. The LTC3576/LTC3576-1's bidirectional switching regulator in step-down mode

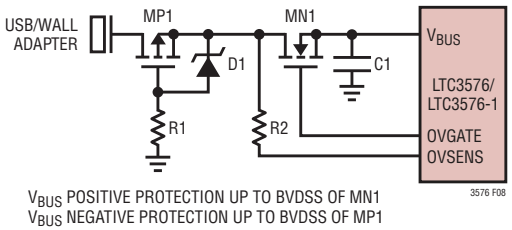


Figure 8. Dual Polarity Voltage Protection

transforms the voltage at V_{BUS} to a voltage just above the level at BAT, while limiting power to less than the amount programmed at CLPROG. The charger should be programmed (with the PROG pin) to deliver the maximum safe charging current without regard to the USB specifications. If there is insufficient current available to charge the battery at the programmed rate, it will reduce charge current until the system load on V_{OUT} is satisfied and the V_{BUS} current limit is satisfied. Programming the charger for more current than is available will not cause the average input current limit to be violated. It will merely allow the battery charger to make use of all available power to charge the battery as quickly as possible, and with minimal dissipation within the charger.

Battery Charger Stability Considerations

The LTC3576/LTC3576-1's battery charger contains both a constant-voltage and a constant-current control loop. The constant-voltage loop is stable without any compensation when a battery is connected with low impedance leads. Excessive lead length, however, may add enough series inductance to require a bypass capacitor of at least 1µF from BAT to GND.

High value, low ESR MLCCs reduce the constant-voltage loop phase margin, possibly resulting in instability. Up to 22µF may be used in parallel with a battery, but larger capacitors should be decoupled with 0.2Ω to 1Ω of series resistance.

Furthermore, a 100µF MLCC in series with a 0.3Ω resistor from BAT to GND is required to prevent oscillation when the battery is disconnected.

In constant-current mode, the PROG pin is in the feedback loop rather than the battery voltage. Because of the additional pole created by any PROG pin capacitance,

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capacitance on this pin must be kept to a minimum. With no additional capacitance on the PROG pin, the charger is stable with program resistor values as high as 25k. However, additional capacitance on this node reduces the maximum allowed program resistor. The pole frequency at the PROG pin should be kept above 100kHz. Therefore, if the PROG pin has a parasitic capacitance, C_{PROG}, the following equation should be used to calculate the maximum resistance value for R_{PROG}:

$$R_{PROG} \leq \frac{1}{2\pi \bullet 100kHz \bullet C_{PROG}}$$

Alternate NTC Thermistors and Biasing

The LTC3576/LTC3576-1 provide temperature qualified charging if a grounded thermistor and a bias resistor are connected to NTC. By using a bias resistor whose value is equal to the room temperature resistance of the thermistor (R25) the upper and lower temperatures are pre-programmed to approximately 40°C and 0°C respectively assuming a Vishay Curve 1 thermistor.

The upper and lower temperature thresholds can be adjusted by either a modification of the bias resistor value or by adding a second adjustment resistor to the circuit. If only the bias resistor is adjusted, then either the upper or the lower threshold can be modified but not both. The other trip point will be determined by the characteristics of the thermistor. Using the bias resistor in addition to an adjustment resistor, both the upper and the lower temperature trip points can be independently programmed with the constraint that the difference between the upper and lower temperature thresholds cannot decrease. Examples of each technique are given below.

NTC thermistors have temperature characteristics which are indicated on resistance-temperature conversion tables. The Vishay-Dale thermistor NTHS0603N011-N1003F, used in the following examples, has a nominal value of 100k and follows the Vishay Curve 1 resistance-temperature characteristic.

In the explanation below, the following notation is used.

R25 = Value of the Thermistor at 25°C

$R_{NTC|COLD}$ = Value of thermistor at the cold trip point

$R_{NTC|HOT}$ = Value of the thermistor at the hot trip point

r_{COLD} = Ratio of $R_{NTC|COLD}$ to R25

r_{HOT} = Ratio of $R_{NTC|HOT}$ to R25

R_{NOM} – Primary thermistor bias resistor (see Figure 9)

R1 = Optional temperature range adjustment resistor (see Figure 10)

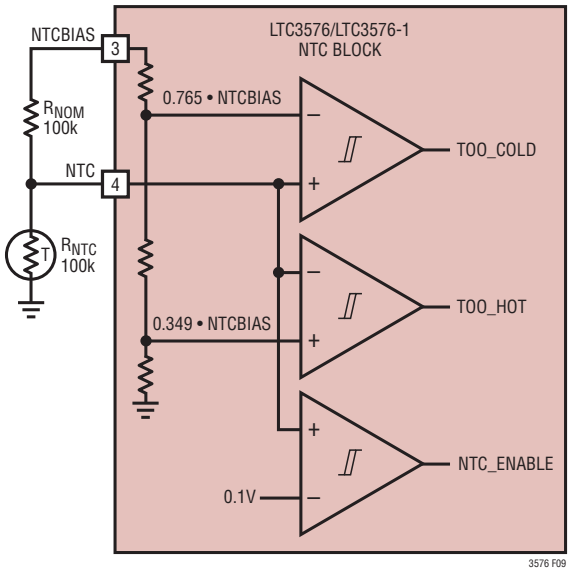


Figure 9. Standard NTC Configuration

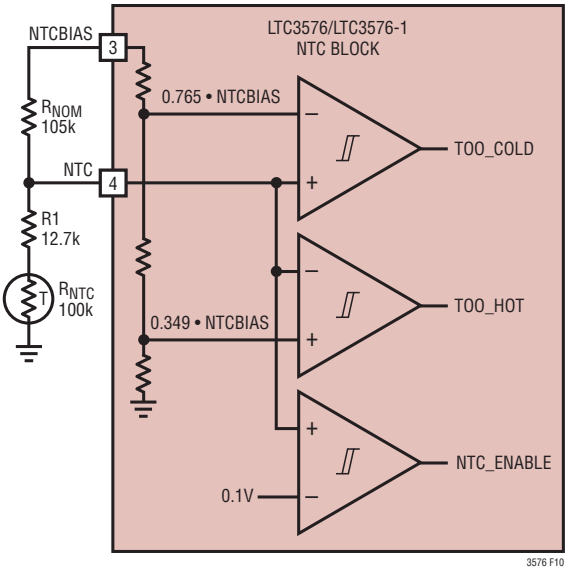


Figure 10. Modified NTC Configuration

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The trip points for the LTC3576/LTC3576-1's temperature qualification are internally programmed at 0.349 • NTCBIAS for the hot threshold and 0.765 • NTCBIAS for the cold threshold.

Therefore, the hot trip point is set when:

$$\frac{R_{NTC|HOT}}{R_{NOM}+R_{NTC|HOT}} \bullet NTCBIAS = 0.349 \bullet NTCBIAS$$

And the cold trip point is set when:

$$\frac{R_{NTC|COLD}}{R_{NOM}+R_{NTC|COLD}} \bullet NTCBIAS = 0.765 \bullet NTCBIAS$$

Solving these equations for $R_{NTC|COLD}$ and $R_{NTC|HOT}$ results in the following:

$$R_{NTC|HOT} = 0.536 \bullet R_{NOM}$$

and

$$R_{NTC|COLD} = 3.25 \bullet R_{NOM}$$

By setting R_{NOM} equal to R25, the above equations result in $r_{HOT} = 0.536$ and $r_{COLD} = 3.25$. Referencing these ratios to the Vishay Resistance-Temperature Curve 1 chart gives a hot trip point of about 40°C and a cold trip point of about 0°C. The difference between the hot and cold trip points is approximately 40°C.

By using a bias resistor, R_{NOM}, different in value from R25, the hot and cold trip points can be moved in either direction. The temperature span will change somewhat due to the nonlinear behavior of the thermistor. The following equations can be used to calculate a new value for the bias resistor:

$$R_{NOM} = \frac{r_{HOT}}{0.536} \bullet R25$$

$$R_{NOM} = \frac{r_{COLD}}{3.25} \bullet R25$$

where r_{HOT} and r_{COLD} are the resistance ratios at the desired hot and cold trip points. Note that these equations are linked. Therefore, only one of the two trip points can be chosen, the other is determined by the default ratios designed in the IC. Consider an example where a 60°C hot trip point is desired.

From the Vishay Curve 1 R-T characteristics, r_{HOT} is 0.2488 at 60°C. Using the above equation, R_{NOM} should be set to 46.4k. With this value of R_{NOM}, r_{COLD} is 1.436 and the cold trip point is about 16°C. Notice that the span is now 44°C rather than the previous 40°C. This is due to the decrease in "temperature gain" of the thermistor as absolute temperature increases.

The upper and lower temperature trip points can be independently programmed by using an additional bias resistor as shown in Figure 10. The following formulas can be used to compute the values of R_{NOM} and R1:

$$R_{NOM} = \frac{r_{COLD} - r_{HOT}}{2.714} \bullet R25$$

$$R1 = 0.536 \bullet R_{NOM} - r_{HOT} \bullet R25$$

For example, to set the trip points to 0°C and 45°C with a Vishay Curve 1 thermistor choose:

$$R_{NOM} = \frac{3.266 - 0.4368}{2.714} \bullet 100k = 104.2k$$

the nearest 1% value is 105k:

$$R1 = 0.536 \bullet 105k - 0.4368 \bullet 100k = 12.6k$$

the nearest 1% value is 12.7k. The final solution is shown in Figure 10 and results in an upper trip point of 45°C and a lower trip point of 0°C.

Hot Plugging and USB Inrush Current Limiting

The overvoltage protection circuit provides inrush current limiting due to the long time it takes for OVGATE to fully enhance the N-channel MOSFET. This prevents the current from building up in the cable too quickly thus dampening out any resonant overshoot on V_{BUS}. It is possible to observe voltage overshoot on V_{BUS} when connecting the LTC3576/LTC3576-1 to a lab power supply if the overvoltage protection circuit is not used. This overshoot is caused by the inductance of the long leads from the power supply to V_{BUS}. Twisting the wires together from the supply to V_{BUS} can greatly reduce the parasitic inductance of these long leads keeping the voltage at V_{BUS} to safe levels. USB cables are generally manufactured with the power leads in close proximity, and thus have fairly low parasitic inductance.

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Hot Plugging and USB On-the-Go

If there is more than 4.3V on V_{BUS} when on-the-go is enabled, the bidirectional switching regulator will not try to drive V_{BUS}. If USB on-the-go is enabled and an external supply is then connected to V_{BUS}, one of three things will happen depending on the properties of the external supply. If the external supply has a regulation voltage higher than 5.1V, the bidirectional switching regulator will stop switching and V_{BUS} will be held at the regulation voltage of the external supply. If the external supply has a lower regulation voltage and is capable of only sourcing current then V_{BUS} will be regulated to 5.1V. The external supply will not source current to V_{BUS}.

For a supply that can also sink current and has a regulation voltage less than 5.1V, the bidirectional switching regulator will source current into the external supply in an attempt to bring V_{BUS} up to 5.1V. As long as the external supply holds V_{BUS} to more than 4V or V_{OUT} + 70mV, the bidirectional switching regulator will source up to 680mA into the supply. If V_{BUS} is held to a voltage that is less than 4V and V_{OUT} + 70mV then the short circuit timer will shut off the switching regulator after 7.2ms. The $\overline{CHRG}$ pin will then blink indicating a short circuit current fault.

V_{BUS} Bypass Capacitance and USB On-The-Go Session Request Protocol

When two on-the-go devices are connected, one will be the A device and the other will be the B device depending on whether the device is connected to a micro A or micro B plug. The A device provides power to the B device and starts as the host. To prolong battery life, the A device can power down V_{BUS} when the bus is not being used. If the A device has powered down V_{BUS}, the B device can request the A device to power up V_{BUS} and start a new session using the session request protocol (SRP). The SRP consists of data-line pulsing and V_{BUS} pulsing. The B device must first pulse the D^+ or D^- data line. The B device must then pulse V_{BUS} only if the A device does not respond to the data-line pulse. The A device is required to respond to only one of the pulsing methods. A devices that never power down V_{BUS} are not required to respond to the SRP.

For V_{BUS} pulsing, the limit on the V_{BUS} capacitance on the A device allows a B device to differentiate between a powered down on-the-go device and a powered down standard host. The B device will send out a pulse of current that will raise V_{BUS} to a voltage between 2.1V and 5.25V if connected to an on-the-go A device which must have no more than 6.5µF. An on-the-go A device must drive V_{BUS} as soon as the current pulse raises V_{BUS} above 2.1V if the device is capable of responding to V_{BUS} pulsing.

This same current pulse must not raise V_{BUS} any higher than 2V when connected to a standard host which must have at least 96µF. The 96µF for a standard host represents the minimum capacitance with V_{BUS} between 4.75V and 5.25V. Since the SRP pulse must not drive V_{BUS} greater than 2V, the capacitance seen at these voltage levels can be greater than 96µF, especially if MLCCs are used. Therefore, the 96µF represents a lower bound on the standard host bypass capacitance for determining the amplitude and duration of the current pulse. More capacitance will only decrease the maximum level that V_{BUS} will rise to for a given current pulse.

Figure 11 shows an on-the-go device using the LTC3576/LTC3576-1 acting as the A device. Additional capacitance can be placed on the V_{BUS} pin of the LTC3576/LTC3576-1 when using the overvoltage protection circuit. A B device may not be able to distinguish between a powered down LTC3576/LTC3576-1 with overvoltage protection and a powered down standard host because of this extra capacitance. In addition, if the SRP pulse raises V_{BUS} above its UVLO threshold of 4.3V the LTC3576/LTC3576-1 will assume input power is available and will not attempt to drive V_{BUS}. Therefore, it is recommended that an on-the-go device using the LTC3576/LTC3576-1 respond to data-line pulsing.

When an on-the-go device using the LTC3576/LTC3576-1 becomes the B device, as in Figure 12, it must send out a data line pulse followed by a V_{BUS} pulse to request a session from the A device. The on-the-go device designer can choose how much capacitance will be placed on the V_{BUS} pin of the LTC3576/LTC3576-1 and then generate a V_{BUS} pulse that can distinguish between a powered

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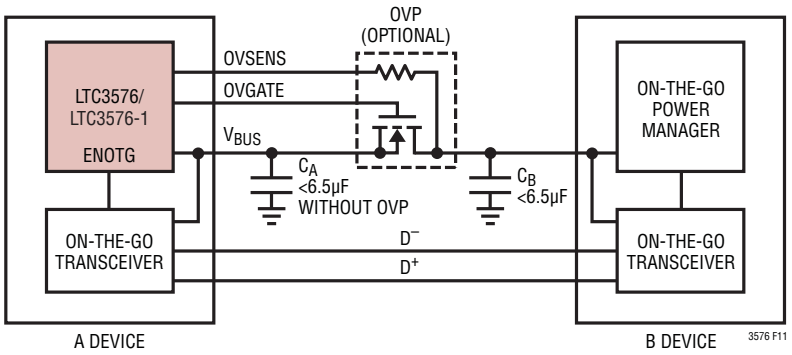


Figure 11. LTC3576/LTC3576-1 as the A Device

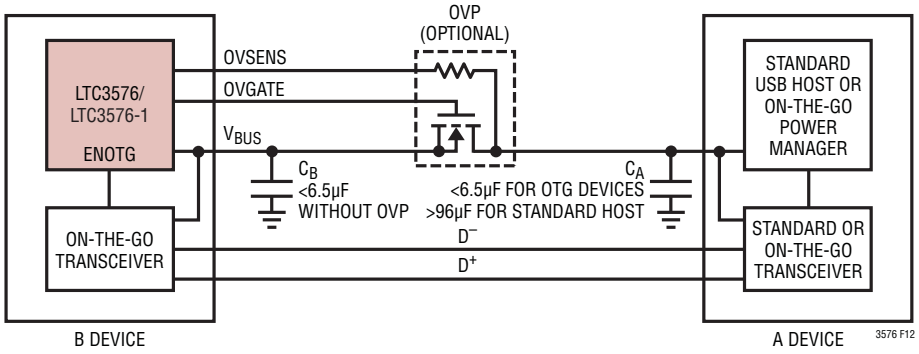


Figure 12. LTC3576/LTC3576-1 as the B Device

down on-the-go A device and a powered down standard host. A suitable pulse can be generated because of the disparity in the bypass capacitances of an on-the-go A device and a standard host even if there is somewhat more than 6.5µF capacitance connected to the V_{BUS} pin of the LTC3576/LTC3576-1.

Board Layout Considerations

The Exposed Pad on the backside of the LTC3576/LTC3576-1 package must be securely soldered to the PC board ground. This is the primary ground pin in the package, and it serves as the return path for both the control circuitry and the N-channel MOSFET switches.

Furthermore, due to its high frequency switching circuitry, it is imperative that the input capacitor, inductor, and output capacitor be as close to the LTC3576/LTC3576-1 as possible and that there be an unbroken ground plane under the LTC3576/LTC3576-1 and all of their external high frequency components. High frequency currents, such as the V_{BUS}, V_{IN1}, V_{IN2} and V_{IN3} currents tend to find their way on the ground plane along a mirror path directly beneath the incident path on the top of the board. If there are slits or cuts in the ground plane due to other traces on that layer, the current will be forced to go around the slits. If high frequency currents are not allowed to flow back through their natural least-area path, excessive voltage will build up and radiated emissions will occur (see Figure 13). There should be a group of vias directly under the grounded backside leading directly down to an internal ground plane. To minimize parasitic inductance, the ground plane should be as close as possible to the top plane of the PC board (layer 2).

The IDGATE pin for the external ideal diode controller has extremely limited drive current. Care must be taken to minimize leakage to adjacent PC board traces. 100nA of leakage from this pin will introduce an additional offset to

APPLICATIONS INFORMATION

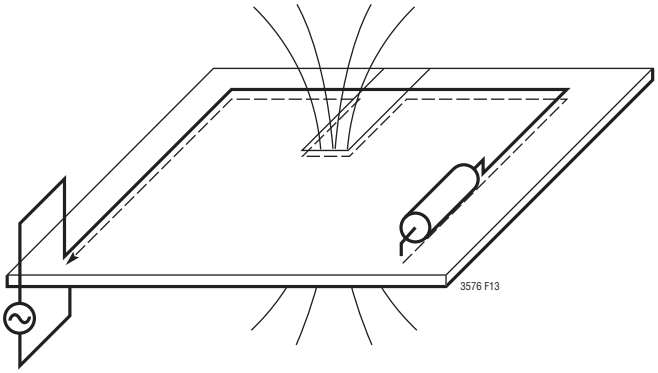


Figure 13. Higher Frequency Ground Current Follow Their Incident Path. Slices in the Ground Plane Create Large Loop Areas. The Large Loop Areas Increase the Inductance of the Path Leading to Higher System Noise

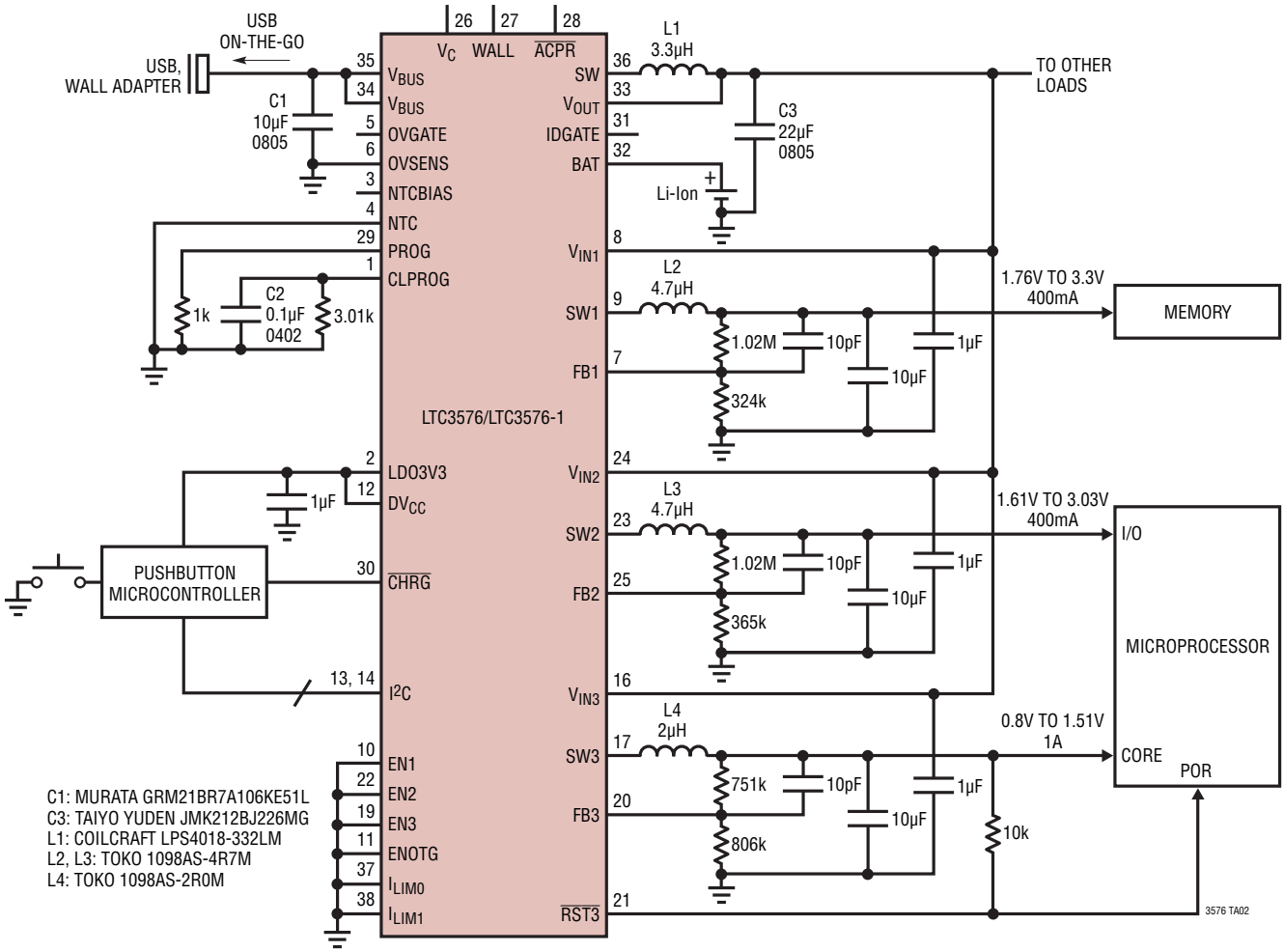
the ideal diode of approximately 10mV. To minimize leakage, the trace can be guarded on the PC board by surrounding it with V_{OUT} connected metal, which should generally be less than one volt higher than IDGATE.

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the LTC3576/LTC3576-1:

1. The Exposed Pad of the package (Pin 39) should connect directly to a large ground plane to minimize thermal and electrical impedance.
2. The traces connecting V_{BUS}, V_{IN1}, V_{IN2}, V_{IN3} and V_{IN} of the external step-down switching regulator to their respective decoupling capacitors should be as short as possible. The GND side of these capacitors should connect directly to the ground plane of the part. These capacitors provide the AC current to the internal power MOSFETs and their drivers. It is critical to minimize inductance from these capacitors to the LTC3576/LTC3576-1 and external step-down switching regulator.
3. Connections between the step-down switching regulator (both internal and external) inductors and their respective output capacitors should be kept as short as possible. Use area fills whenever possible. This also applies to the PowerPath switching regulator inductor and the output capacitor on V_{OUT}. The GND side of the output capacitors should connect directly to the thermal ground plane of the part.
4. The switching power traces connecting SW, SW1, SW2, SW3 and the switch node of the external step-down switching regulator to their respective inductors should be minimized to reduce radiated EMI and parasitic coupling. Due to the large voltage swing of the switching nodes, sensitive nodes such as the feedback nodes (FB1, FB2 and FB3) should be kept far away or shielded from the switching nodes or poor performance could result.
5. Keep the feedback pin traces (FB1, FB2, FB3 and FB of the external step-down switching regulator) as short as possible. Minimize any parasitic capacitance between the feedback traces and any switching node (i.e., SW, SW1, SW2, SW3 and logic signals). If necessary shield the feedback nodes with a GND trace
6. Connect V_{IN1}, V_{IN2} and V_{IN3} to V_{OUT} through a short low impedance trace.

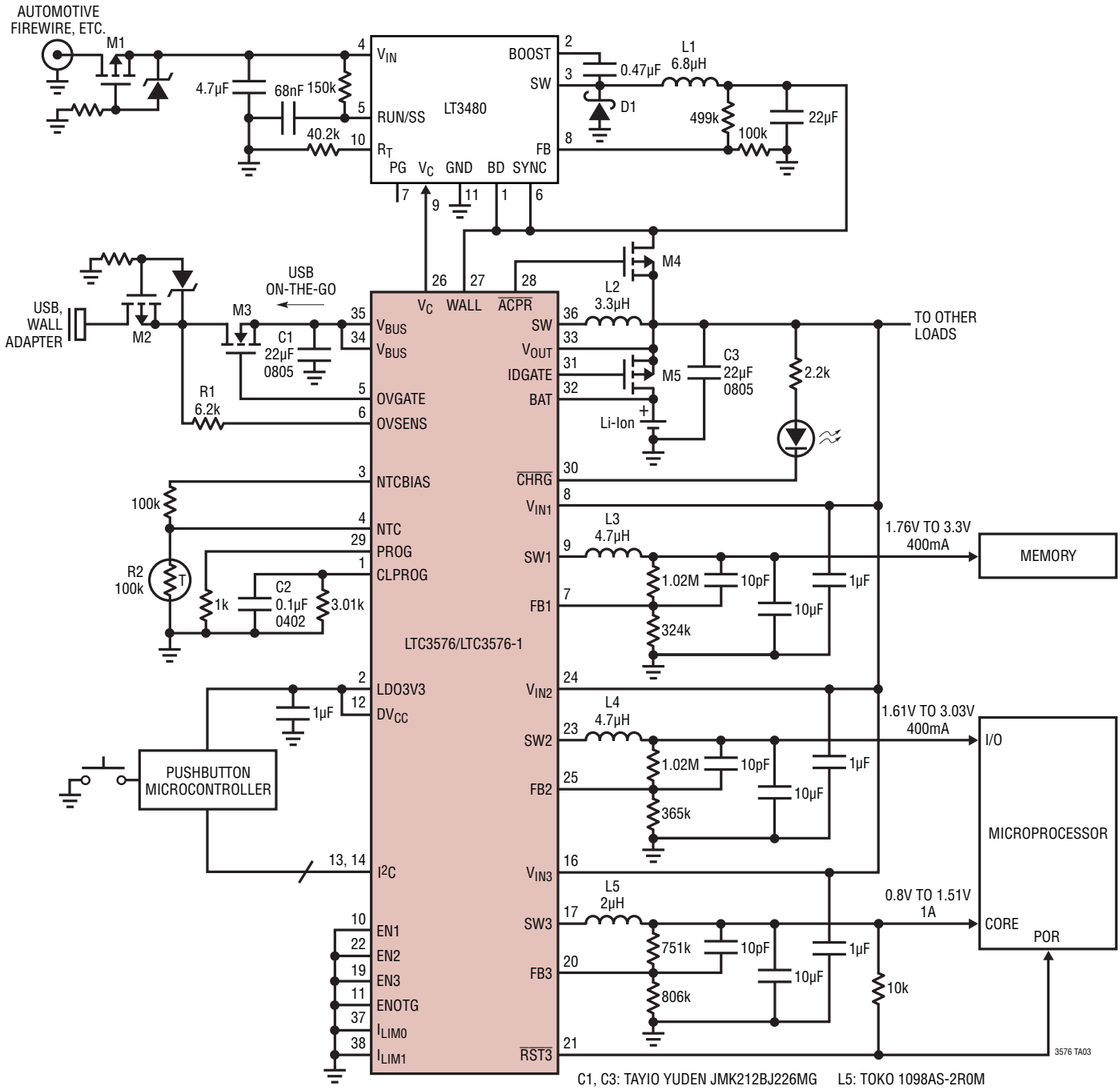
TYPICAL APPLICATIONS

Minimum Parts Count USB Power Manager with Low-Battery Start-Up and USB On-the-Go



TYPICAL APPLICATIONS

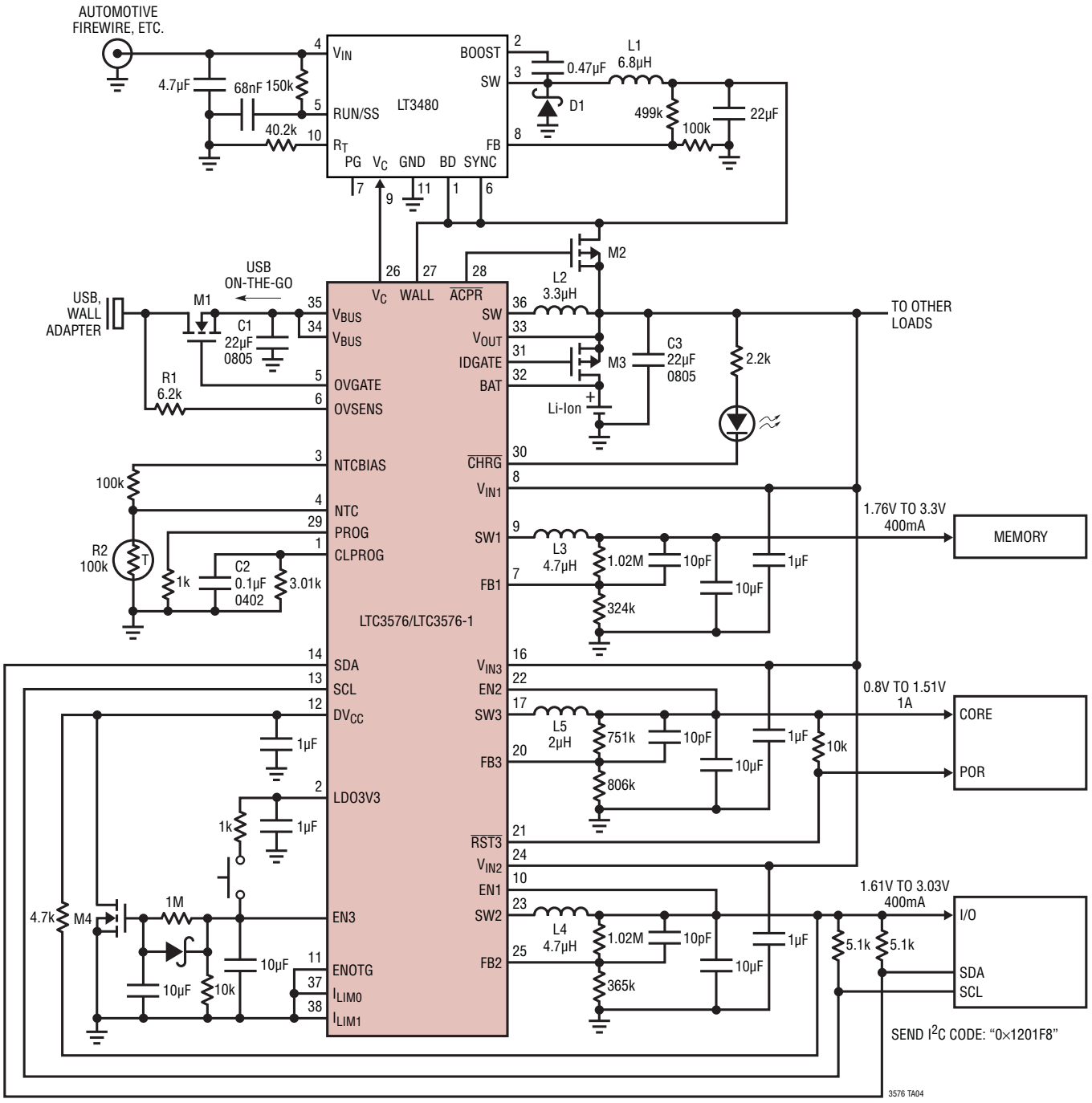
High Efficiency USB/Automotive Power Manager with Overvoltage Protection, Reverse-Voltage Protection, Low-Battery Start-Up and USB On-the-Go



C1, C3: TAYIO YUDEN JMK212BJ226MG
D1: DIODES INC. DFLS240L
L1: TAIYO YUDEN NP06DZB6R8M
L2: COILCRAFT LPS4018-332LM
L3, L4: TOKO 1098AS-4R7M
L5: TOKO 1098AS-2R0M
M1,M2,M4, M5: SILICONIX Si2333DS
M3: ON SEMICONDUCTOR NTLJS4114N
R1: 1/10W RESISTOR
R2: CURVE 1

TYPICAL APPLICATIONS

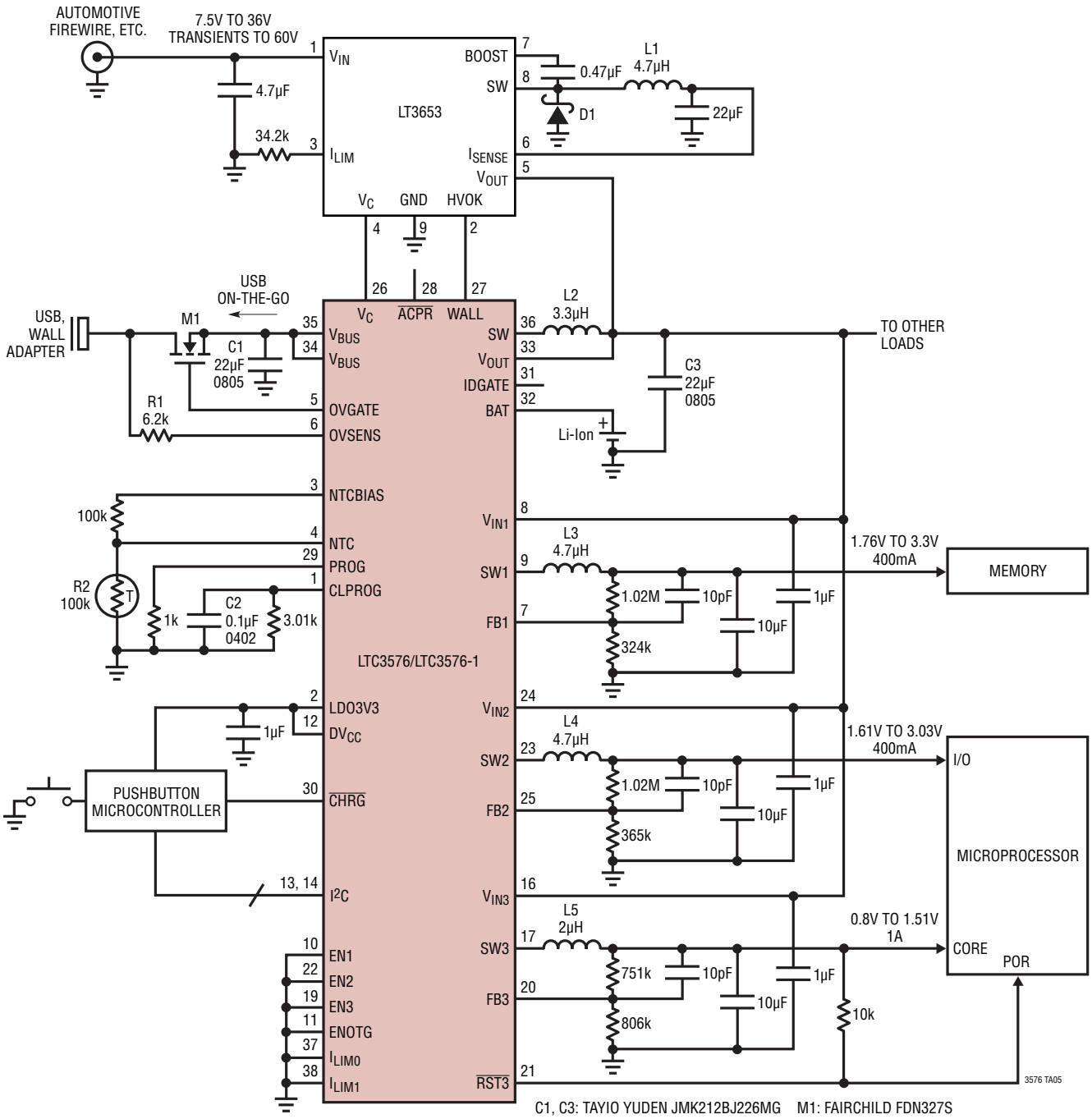
High Efficiency USB/Automotive Power Manager with Overvoltage Protection, USB On-the-Go, Pushbutton Start, Automatic Supply Sequencing and 10 Second Push-and-Hold Hard Shutdown



C1, C3: TAYIO YUDEN JMK212BJ226MG
D1: DIODES INC. DFLS240L
L1: TAIYO YUDEN NP06DZB6R8M
L2: COILCRAFT LPS4018-332LM
L3, L4: TOKO 1098AS-4R7M
L5: TOKO 1098AS-2R0M
M1: ON SEMICONDUCTOR NTLJS4114N
M2, M3: SILICONIX Si2333DS
M4: 2N7002
R1: 1/10W RESISTOR
R2: CURVE 1

TYPICAL APPLICATIONS

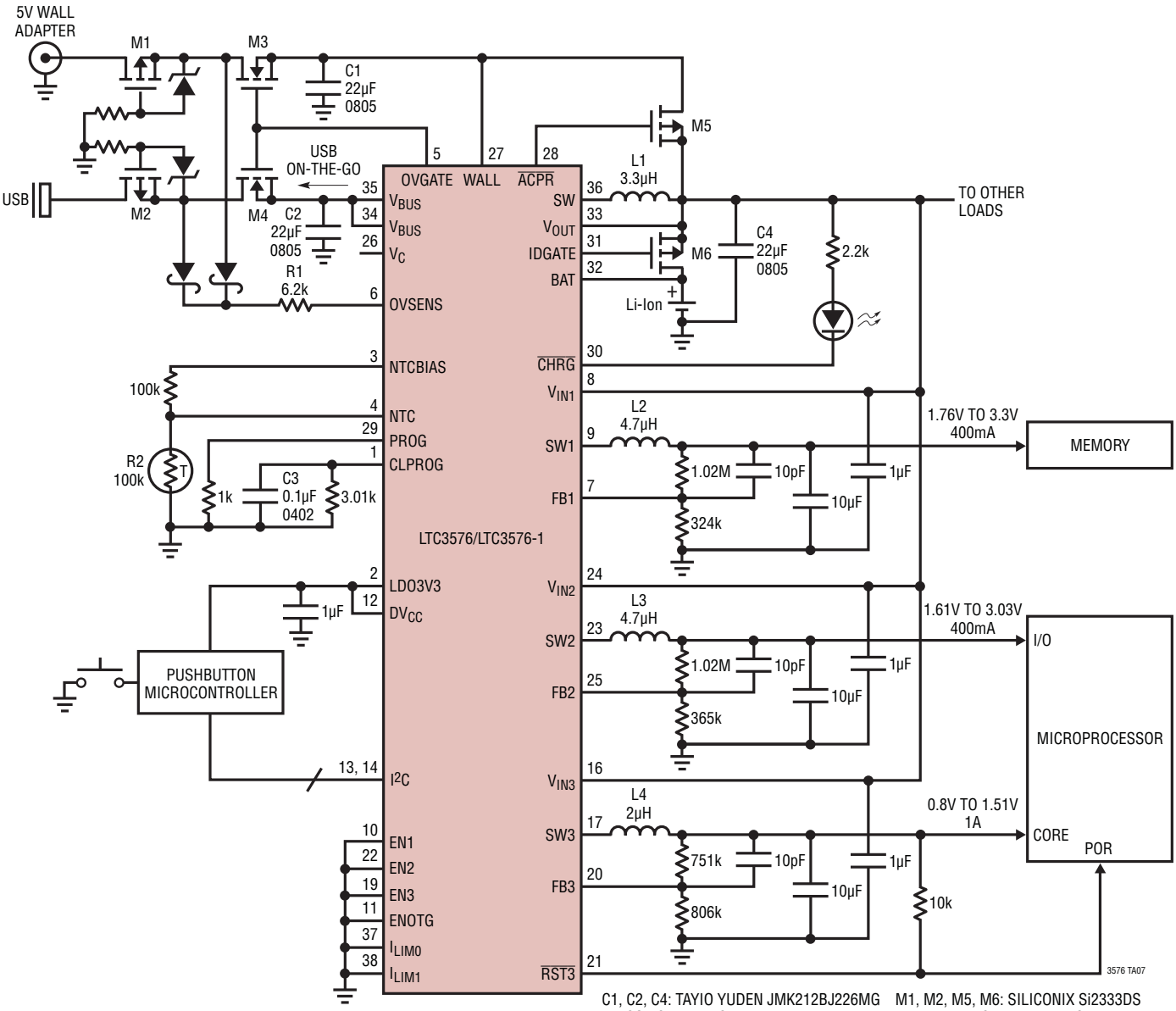
High Efficiency USB/Automotive Power Manager with Current Limiting and Overvoltage Protection on Both Inputs, Low-Battery Start-Up and USB On-the-Go



C1, C3: TAYIO YUDEN JMK212BJ226MG
D1: DIODES INC. DFLS140
L1: COILCRAFT MSS6132-472MLC
L2: COILCRAFT LPS4018-332LM
L3, L4: TOKO 1098AS-4R7M
L5: TOKO 1098AS-2R0M
M1: FAIRCHILD FDN327S
R1: 1/10W RESISTOR
R2: CURVE 1

TYPICAL APPLICATIONS

High Efficiency USB/Wall Power Manager with Dual Overvoltage Protection, Reverse-Voltage Protection, Low-Battery Start-Up and USB On-The-Go

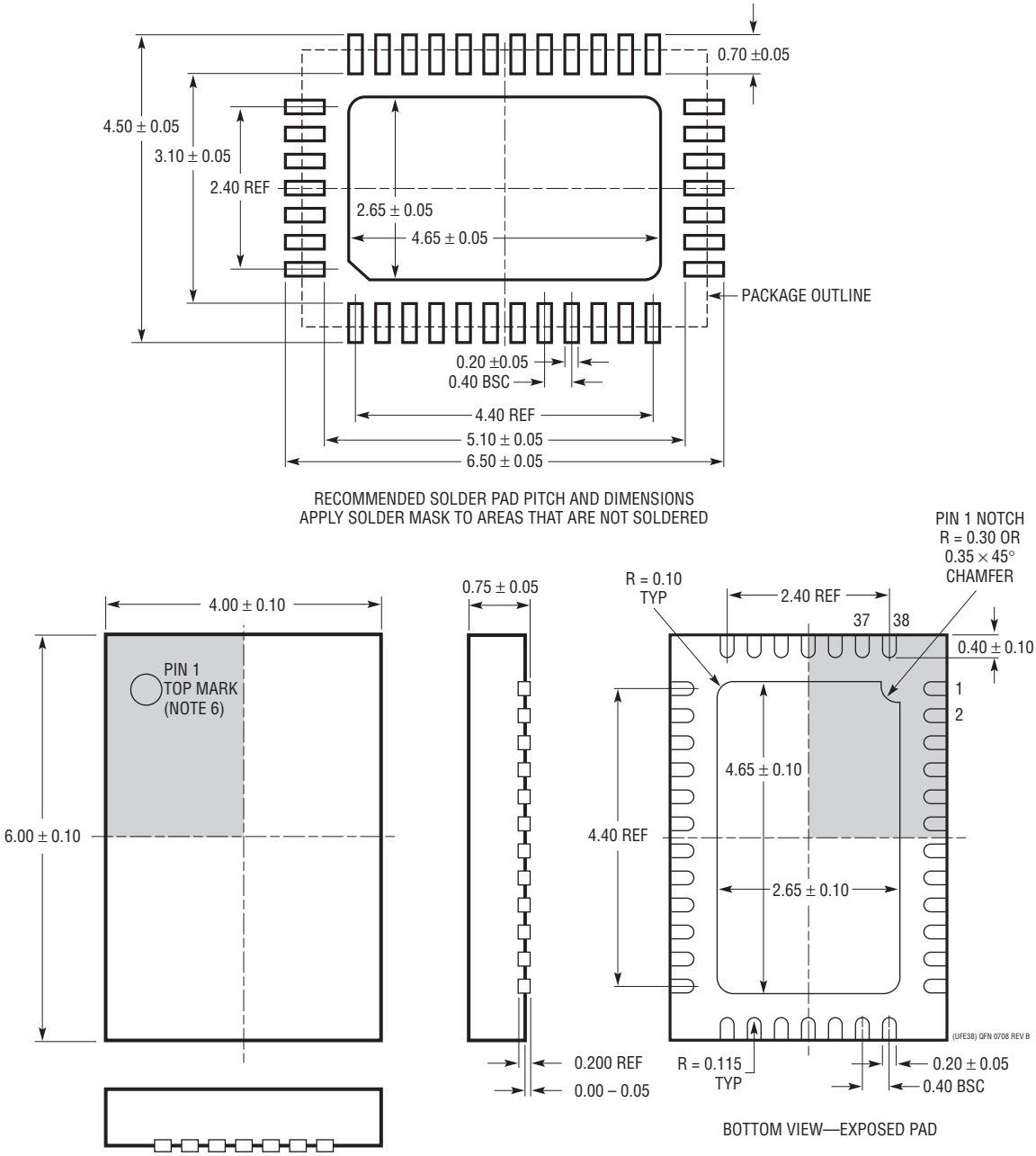


C1, C2, C4: TAYIO YUDEN JMK212BJ226MG
L1: COILCRAFT LPS4018-332LM
L2, L3: TOKO 1098AS-4R7M
L4: TOKO 1098AS-2R0M

M1, M2, M5, M6: SILICONIX Si2333DS
M3, M4: FAIRCHILD FDN327S
R1: 1/10W RESISTOR
R2: CURVE 1

PACKAGE DESCRIPTION

UFE Package
38-Lead Plastic QFN (4mm × 6mm)
(Reference LTC DWG # 05-08-1750 Rev B)

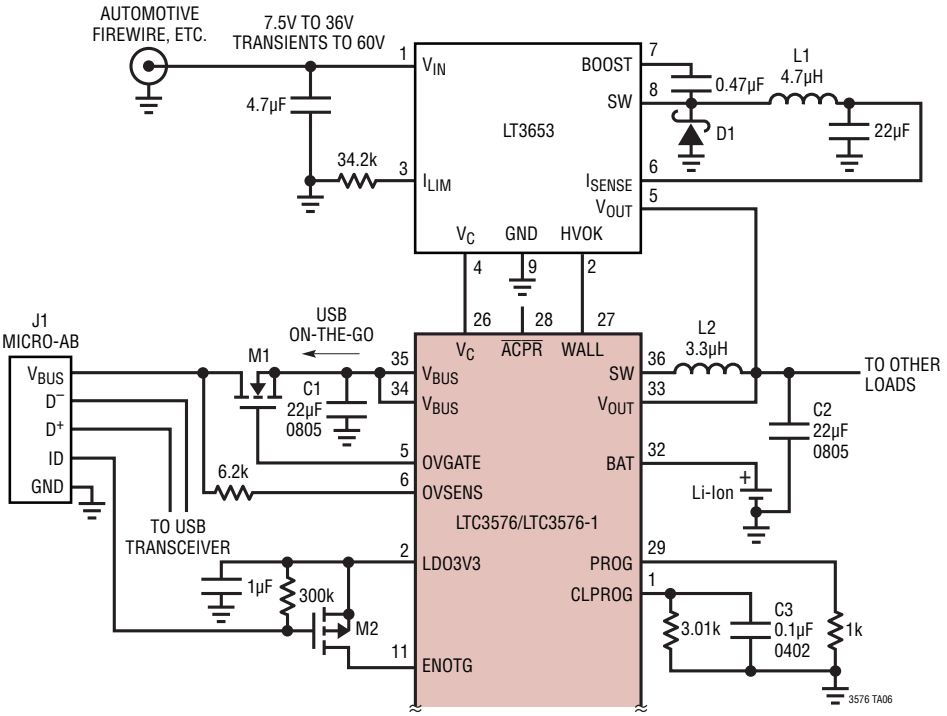


NOTE:
1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

TYPICAL APPLICATION

Firewire/Automotive Battery Charger with Automatic USB On-the-Go and Overvoltage Protection



V_{BUS} POWERS UP WHEN ID PIN HAS LESS THAN 10Ω TO GND (MICRO-A PLUG CONNECTED)

C1, C2: TAIYO YUDEN JMK212BJ226MG
D1: DIODES INC. DFLS140
J1: HIROSE ZX62-AB-5PA
L1: COILCRAFT MSS6132-472MLC
L2: COILCRAFT LPS4018-332LM
M1: FAIRCHILD FDN372S
M2: SILICONIX Si2333DS

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
Power Management		
LTC3555/LTC3555-1 LTC3555-3	Switching USB Power Manager with Li-Ion/Polymer Chargers Plus Triple Buck DC/DC	Maximizes Available Power from USB Port, Bat-Track, 1.5A Max Charge Current, 180mΩ Ideal Diode with <50mΩ Option, 3.3V/25mA Always-On LDO, Two 400mA and One 1A Buck Regulators, Instant-On Operation (LTC3555-1), Instant-On Operation and 4.1V Float Votlage (LTC3555-3), 4mm × 5mm 28-Pin QFN Package
LTC3556	Switching USB Power Manager with Li-Ion/Polymer Charger Plus Dual Buck Plus Buck-Boost DC/DC	Maximizes Available Power from USB Port, Bat-Track, Instant-On Operation, 1.5A Max Charge Current, 180mΩ Ideal Diode with <50mΩ Option, 3.3V/25mA Always-On LDO, Two 400mA Buck Regulators, One 1A Buck-Boost Regulator, 4mm × 5mm 28-Pin QFN Package
LTC3586	Switching USB Power Manager with Li-Ion/Polymer Charger Plus Dual Buck Plus Buck-Boost Plus Boost DC/DC	Maximizes Available Power from USB Port, Bat-Track, Instant-On Operation, 1.5A Max Charge Current, 180mΩ Ideal Diode with <50mΩ Option, 3.3V/25mA Always-On LDO, Two 400mA Synchronous Buck Regulators, One 1A Buck-Boost Regulator, One 600mA Boost Regulator, 4mm × 6mm 38-Pin QFN Package
LTC4098/LTC4098-1	Switching USB Power Manager and Battery Chargers with Overvoltage Protection	Maximizes Available Power from USB Port, Bat-Track, Instant-On Operation, 1.5A Max Charge Current, 180mΩ Ideal Diode with <50mΩ Option, Controller for External High Voltage Buck Regulator, Protection Against Transients of Up to 60V, 3.3V/25mA Always-On LDO,4.1V Float Voltage (LTC4098-1), 4mm × 3mm 14-Pin DFN Package

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