2.6µA Quiescent Current, 15V, 300mA Synchronous Step-Down DC/DC Converter and 10mA LDO

FEATURES

- **Ultralow Quiescent Current: 2.6µA**
- **Synchronous Rectification Efficiency Up to 95%**
- **Wide V_{IN} Range: 2.5V to 15V**
- **Wide V_{OUT} Range: 0.6V to 13.8V**
- **300mA Output Current**
- **User-Selectable Automatic Burst Mode® Operation or Forced Continuous Operation**
- Accurate and Programmable RUN Pin Threshold
- 1.2MHz Fixed Frequency PWM
- Internal Compensation
- Power Good Status Output for V_{OUT}
- 10mA Adjustable LDO
- Available in Thermally Enhanced 3mm × 4mm × 0.75mm, 14-Lead DFN and 16-Lead MSOP Packages

APPLICATIONS

- Remote Sensor Networks
- Distributed Power Systems
- Multicell Battery or SuperCap Regulator
- Energy Harvesters
- Portable Instruments
- Low Power Wireless Systems

DESCRIPTION

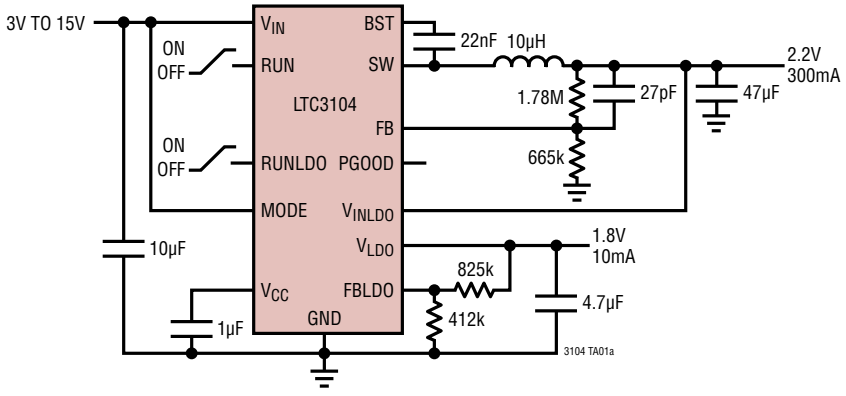
The LTC®3104 is a high efficiency, monolithic synchronous step-down converter using a current mode architecture capable of supplying 300mA of output current. The LTC3104 includes an integrated, adjustable 10mA LDO to power noise sensitive functions.

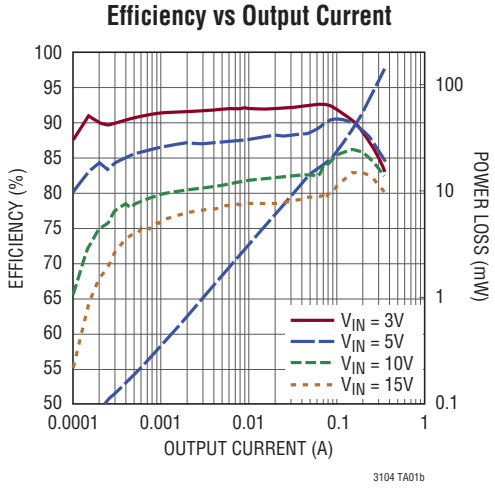
The LTC3104 offers two operational modes: automatic Burst Mode operation and forced continuous mode allowing the user to optimize output voltage ripple, noise and light load efficiency. With Burst Mode operation enabled, the typical DC input supply current at no load drops to 2.6µA, maximizing the efficiency for light loads. Selection of forced continuous mode provides very low noise constant frequency, 1.2MHz operation.

Additionally, the LTC3104 includes an accurate RUN comparator, thermal overload protection, a power good output and an integrated soft-start feature to guarantee that the power system start-up is well controlled.

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TYPICAL APPLICATION



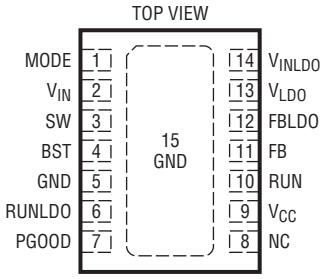


ABSOLUTE MAXIMUM RATINGS (Note 1)

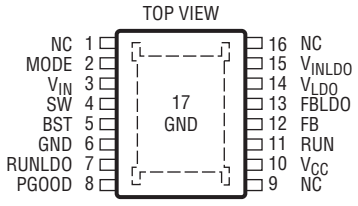
V_{IN} ..... –0.3V to 18V
SW ..... –0.3V to (V_{IN} + 0.3V)
FB, FBLDO ..... –0.3V to 6V
BST ..... (SW – 0.3V) to (SW + 6V)
V_{INLDO} ..... –0.3V to 17V
V_{LDO} ..... –0.3V to 17V
RUN, MODE, RUNLDO ..... –0.3V to V_{IN}
V_{CC}, PGOOD ..... –0.3V to 6V

Operating Junction Temperature Range
(Notes 2, 3) ..... –40°C to 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)
MSE Only ..... 300°C

PIN CONFIGURATION



DE PACKAGE
14-LEAD (4mm × 3mm) PLASTIC DFN
T_{JMAX} = 125°C, θ_{JA} = 53°C/W, θ_{JC} = 10°C/W
EXPOSED PAD (PIN 15) IS GND, MUST BE SOLDERED TO PCB



MSE PACKAGE
16-LEAD PLASTIC MSOP
T_{JMAX} = 125°C, θ_{JA} = 40°C/W, θ_{JC} = 10°C/W
EXPOSED PAD (PIN 17) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

http://www.linear.com/product/LTC3104#orderinfo

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3104EDE#PBF	LTC3104EDE#TRPBF	3104	14-Lead (4mm × 3mm) Plastic DFN	–40°C to 125°C
LTC3104IDE#PBF	LTC3104IDE#TRPBF	3104	14-Lead (4mm × 3mm) Plastic DFN	–40°C to 125°C
LTC3104EMSE#PBF	LTC3104EMSE#TRPBF	3104	16-Lead Plastic MSOP	–40°C to 125°C
LTC3104IMSE#PBF	LTC3104IMSE#TRPBF	3104	16-Lead Plastic MSOP	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel//. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{IN} = V_{INLDO} = 10V unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Step-Down Converter						
Input Voltage Range	 After Start-Up	● ●	2.6 2.5		15	V
Input Undervoltage Lockout Threshold	V_{IN} Rising V_{IN} Rising, T_J = 0°C to 85°C (Note 4)	●		2.1 2.1	2.6 2.5	V V
Input Undervoltage Lockout Hysteresis	(Note 4)			0.4		V
Feedback Voltage	(Note 5)	●	0.588	0.6	0.612	V
Feedback Voltage Line Regulation	V_{IN} = 2.5V to 15V (Note 5)			0.02	0.05	%/V
Feedback Input Current	(Note 5)	●		1	20	nA
Oscillator Frequency	 T_J = 0°C to 85°C (Note 4)	●	0.93 1.0	1.2 1.2	1.55 1.45	MHz MHz
Quiescent Current, V_{IN}—Active	RUN = V_{IN}, RUNLDO = V_{IN}, MODE = 0V, FB > 0.612, Nonswitching			600		µA
Quiescent Current, V_{IN}—Sleep	T_J = 0°C to 85°C, RUN = MODE = V_{IN}, FB > 0.612 RUNLDO = V_{IN} (Note 4) RUNLDO = 0V (Note 4)			 2.6 1.8	 3.3 2.6	 µA µA
	RUN = MODE = V_{IN}, FB > 0.612 RUNLDO = V_{IN} RUNLDO = 0V	 ● ●		 2.8 1.8	 5.5 4.5	 µA µA
Quiescent Current, V_{IN}—Shutdown	 RUN = 0V, RUNLDO = 0V, T_J = 0°C to 85°C (Note 4) RUN = 0V, RUNLDO = 0V	 ●		 1 1	 1.7 3.3	 µA µA
N-Channel MOSFET Synchronous Rectifier Leakage Current	V_{IN} = V_{SW} =15V, V_{RUN} = 0V			0.01	0.3	µA
N-Channel MOSFET Switch Leakage Current	V_{IN} =15V, V_{SW} = 0V, V_{RUN} = 0V			0.01	0.3	µA
N-Channel MOSFET Synchronous Rectifier $R_{DS(ON)}$	I_{SW} = 200mA			0.85		Ω
N-Channel MOSFET Switch $R_{DS(ON)}$	I_{SW} = –200mA			0.65		Ω
Peak Current Limit		●	0.40	0.50	0.75	A
PGOOD Threshold	FB Falling, Percentage Below FB		–14	–10	–5	%
PGOOD Hysteresis	Percentage of FB			2		%
PGOOD Voltage Low	I_{PGOOD} = 100µA			0.2		V
PGOOD Leakage Current	V_{PGOOD} = 5V			0.01	0.3	µA
Maximum Duty Cycle		●	89	92		%
Switch Minimum Off Time ($t_{OFF(MIN)}$)	(Note 4)			65		ns
Synchronous Rectifier Minimum On Time ($t_{ON(MIN)}$)	(Note 4)			70		ns
RUN Pin Threshold	RUN Pin Rising	●	0.76	0.8	0.85	V
RUN Pin Hysteresis				0.06		V
RUN Input Current	RUN = 1.2V	●		0.01	0.4	µA
MODE Threshold		●	0.5	0.8	1.2	V
MODE Input Current	MODE = 1.2V			0.1	4	µA
Soft-Start Time	V_{IN} = 5V		0.7	1.4	2.5	ms
LDO Regulator						
LDO Input Voltage Range ($V_{IN(LDO)}$)		●	2.5		15	V
LDO Output Voltage Range (V_{LDO})	I_{LDO} = 1mA	●	0.6		14.5	V
LDO Feedback Voltage		●	0.576	0.6	0.624	V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{IN} = V_{INLDO} = 10V unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
LDO Feedback Input Current		●		1	20	nA
Dropout Voltage (V_{DO})	I_{LDO} = 10mA			150		mV
Output Current		●	10			mA
Output Current—Short Circuit	V_{LDO} = 0V	●	15	20		mA
Quiescent Current, V_{INLDO}	V_{IN} = V_{INLDO} = RUNLDO = 10V			0.3		µA
Line Regulation	V_{INLDO} = 2.5V to 15V, I_{LDO} = 1mA			0.1		%
Load Regulation	I_{LDO} = 1mA to 10mA			0.75		%
RUNLDO Threshold		●	0.5	0.8	1.2	V
RUNLDO Input Current	RUNLDO = 1.2V			0.01	0.3	µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC3104 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC3104E is guaranteed to meet specifications from 0°C to 85°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3104I is guaranteed over the full –40°C to 125°C operating junction temperature range. The junction temperature (T_J) is calculated from the ambient temperature (T_A) and power dissipation (P_D) according to the formula:

$$T_J = T_A + (P_D)(\theta_{JA}°C/W)$$

where θ_{JA} is the package thermal impedance. Note the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance and other environmental factors.

Note 3: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. The maximum rated junction temperature will be exceeded when this protection is active. Continuous operation above the specified absolute maximum operating junction temperature may impair device reliability or permanently damage the device.

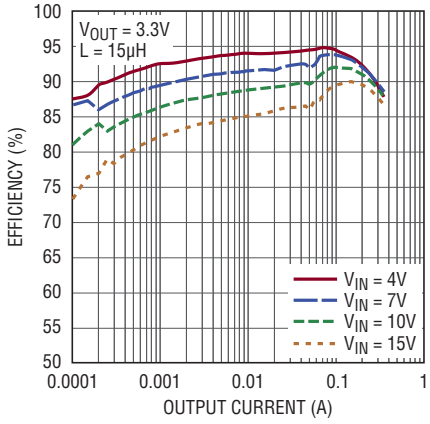
Note 4: Specification is guaranteed by design.

Note 5: The LTC3104 has a proprietary test mode that allows testing in a feedback loop which servos V_{FB} to the balance point for the error amplifier.

TYPICAL PERFORMANCE CHARACTERISTICS

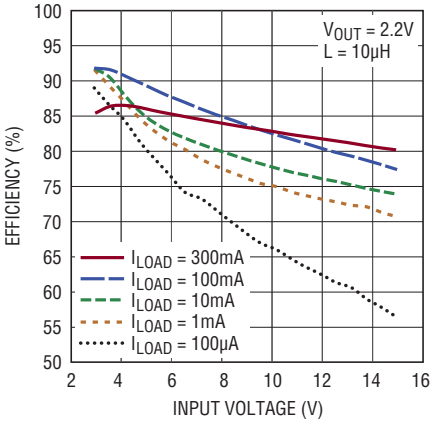
T_A = 25°C unless otherwise noted

Efficiency vs Output Current



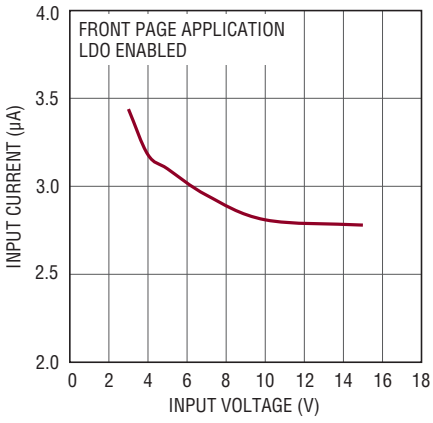
3104 G01

Efficiency vs Input Voltage (Automatic Burst Mode Operation)



3104 G02

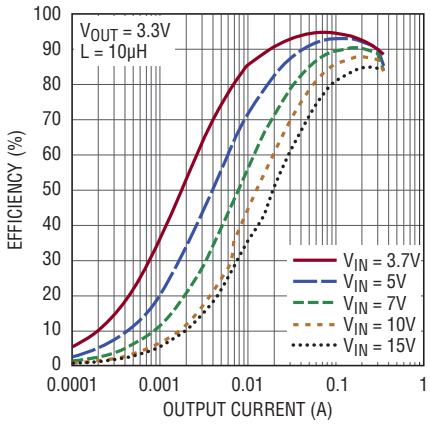
Application No-Load Input Current vs Supply Voltage (Automatic Burst Mode Operation)



3104 G03

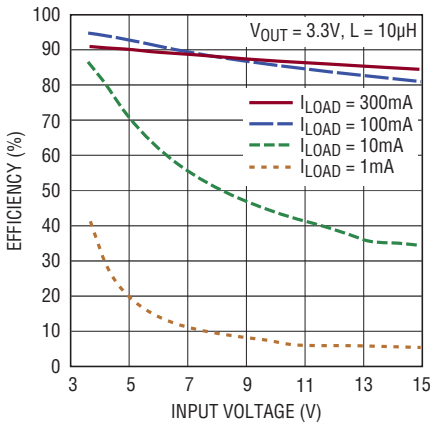
TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C unless otherwise noted

Efficiency vs Output Current (Forced Continuous Operation)



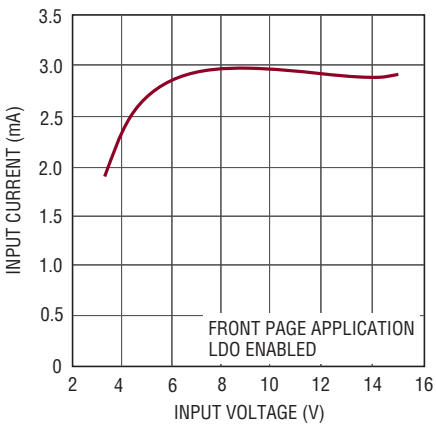
3104 G04

Efficiency vs Input Voltage (Forced Continuous Operation)



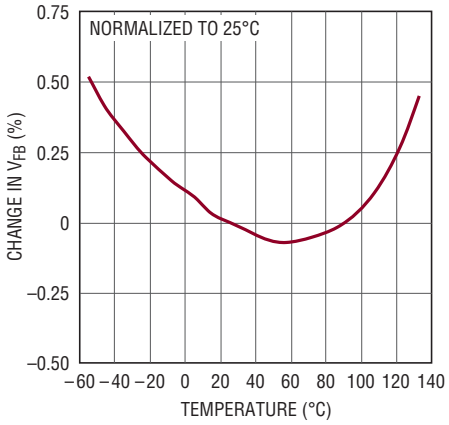
3104 G05

Application No-Load Input Current vs Supply Voltage (Forced Continuous Operation)



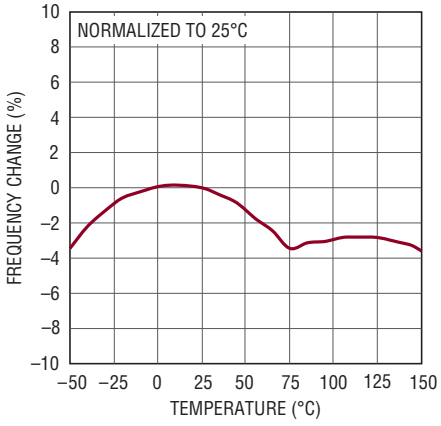
3104 G06

Feedback Voltage vs Temperature



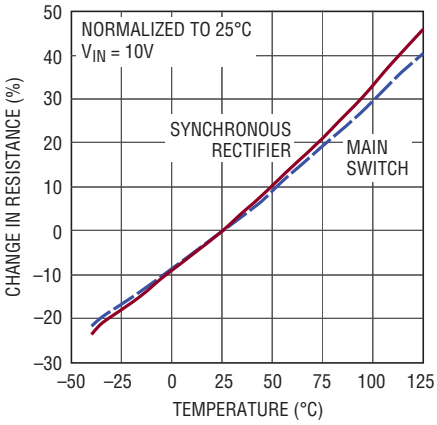
3104 G07

Oscillator Frequency vs Temperature



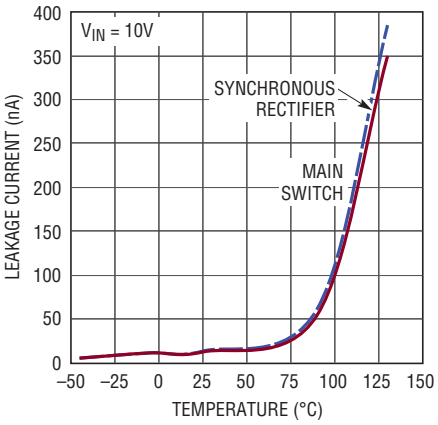
3104 G08

RDS(ON) vs Temperature



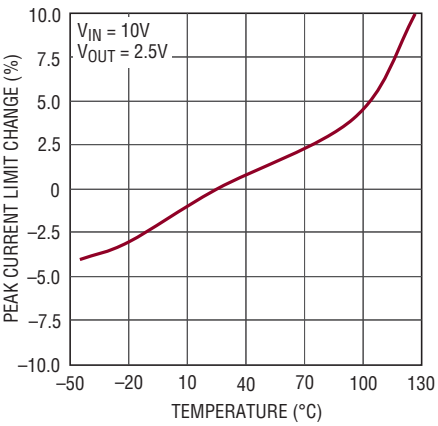
3104 G09

SW Leakage vs Temperature



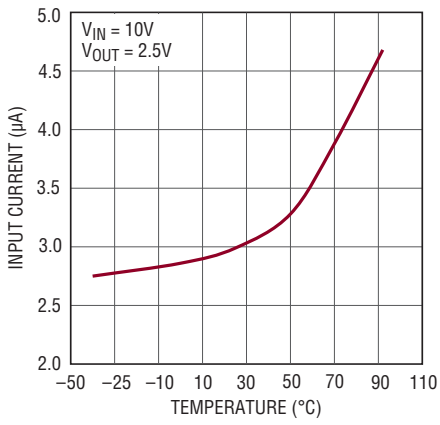
3104 G10

Peak Current Limit vs Temperature



3104 G11

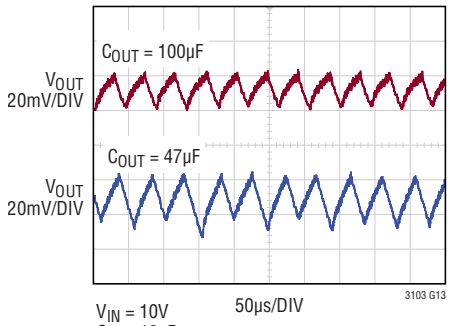
Application No-Load Input Current vs Temperature (Automatic Burst Mode Operation)



3104 G12

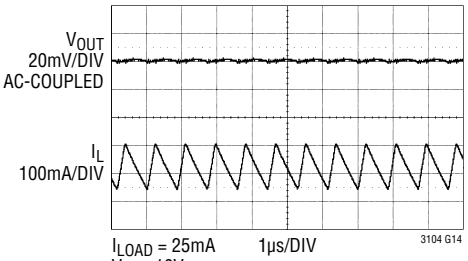
TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C unless otherwise noted

Automatic Burst Mode Operation



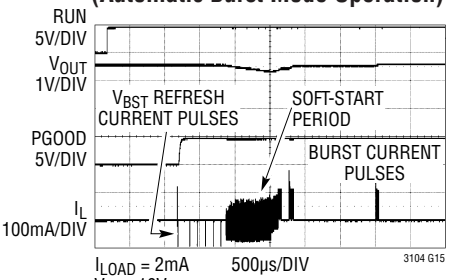
V_{IN} = 10V
C_{IN} = 10µF
L = 10µH
V_{OUT} = 2.2V

Forced Continuous Operation



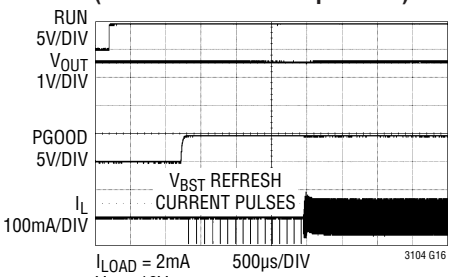
I_{LOAD} = 25mA
V_{IN} = 10V
C_{IN} = 10µF
L = 10µH
V_{OUT} = 2.5V
C_{OUT} = 22µF

Start-Up into Pre-Biased Output (Automatic Burst Mode Operation)



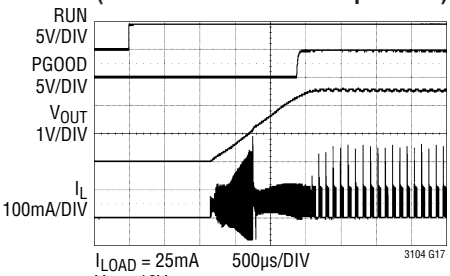
I_{LOAD} = 2mA
V_{IN} = 10V
C_{IN} = 10µF
L = 10µH
V_{OUT} = 2.5V
C_{OUT} = 47µF

Start-Up into Pre-Biased Output (Forced Continuous Operation)



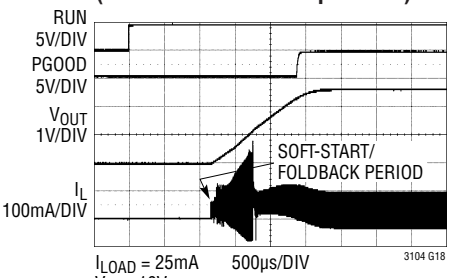
I_{LOAD} = 2mA
V_{IN} = 10V
L = 10µH
V_{OUT} = 2.5V

Start-Up from Shutdown (Automatic Burst Mode Operation)



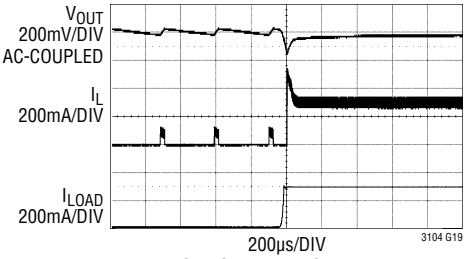
I_{LOAD} = 25mA
V_{IN} = 10V
L = 10µH
V_{OUT} = 2.5V

Start-Up from Shutdown (Forced Continuous Operation)



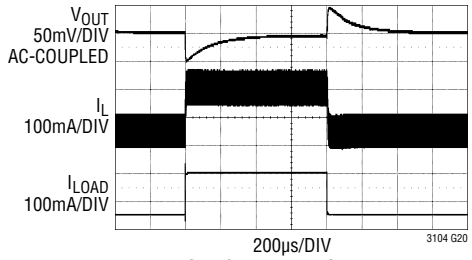
I_{LOAD} = 25mA
V_{IN} = 10V
L = 10µH
V_{OUT} = 2.5V

Load Step (Automatic Burst Mode Operation)



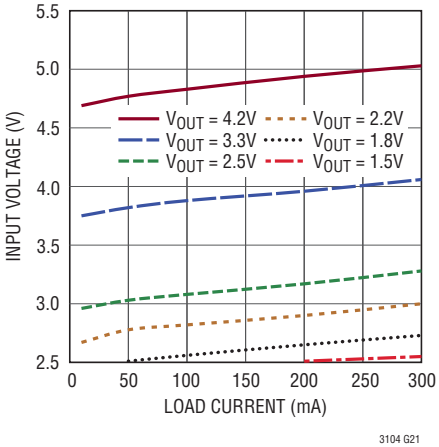
I_{LOAD} = LOAD STEP, 5mA TO 300mA
V_{IN} = 10V
C_{IN} = 10µF
L = 10µH
V_{OUT} = 2.5V
C_{OUT} = 47µF

Load Step (Forced Continuous Operation)



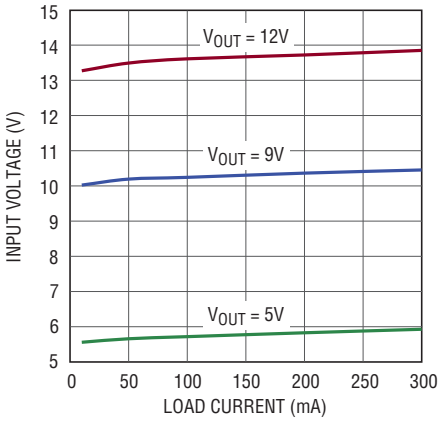
I_{LOAD} = LOAD STEP, 50mA TO 200mA
V_{IN} = 10V
L = 10µH
V_{OUT} = 2.5V
C_{OUT} = 22µF

Minimum Input Voltage at Maximum Duty Cycle vs Load Current



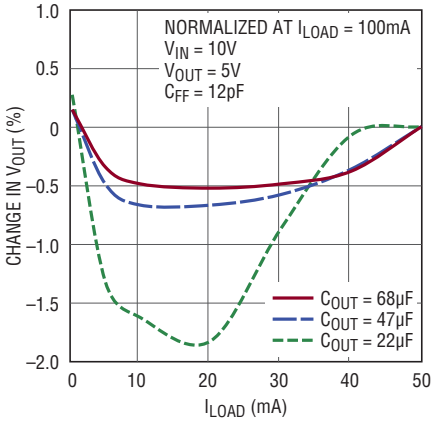
TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C unless otherwise noted

Minimum Input Voltage at Maximum Duty Cycle vs Load Current



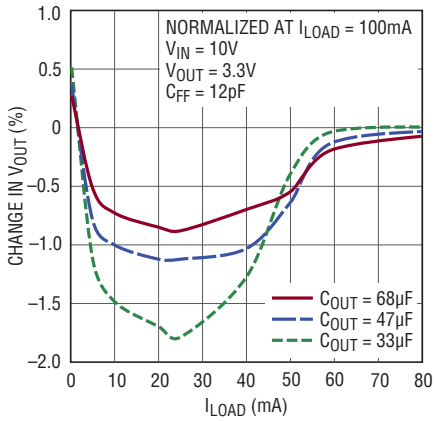
3104 G22

Load Regulation (Automatic Burst Mode Operation)



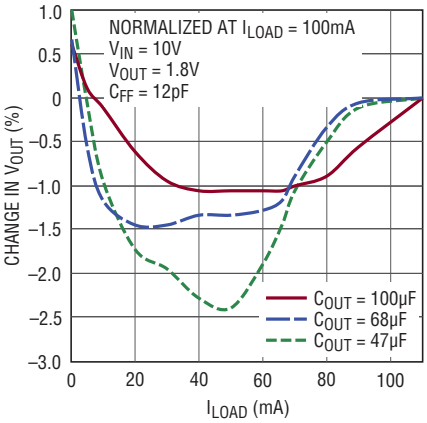
3104 G23

Load Regulation (Automatic Burst Mode Operation)



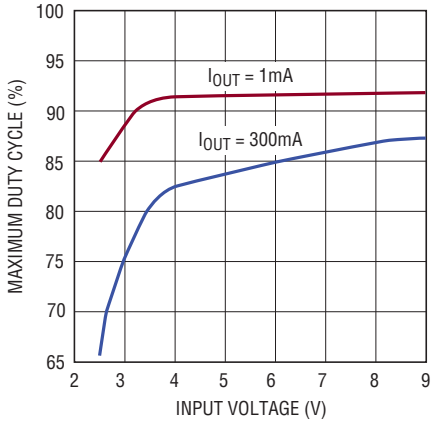
3104 G24

Load Regulation (Automatic Burst Mode Operation)



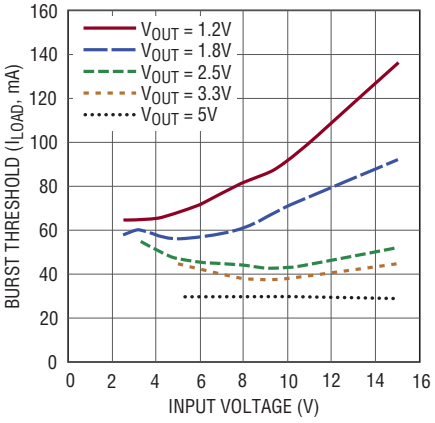
3104 G25

Maximum Duty Cycle vs Input Voltage



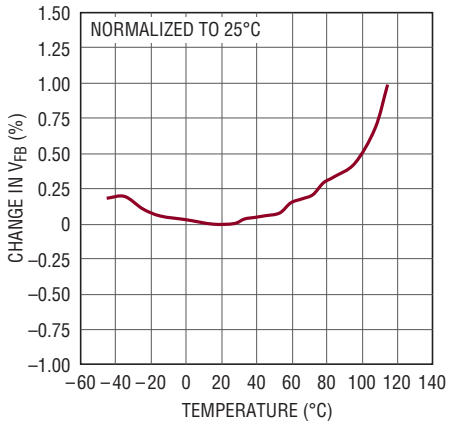
3104 G26

Automatic Burst Mode Threshold vs Supply Voltage



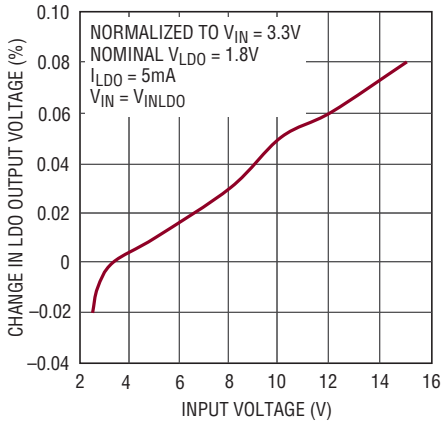
3104 G27

LDO Feedback Voltage vs Temperature



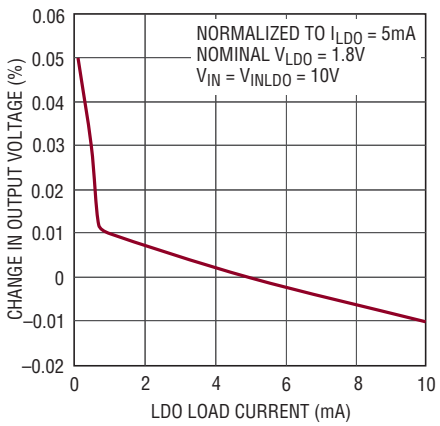
3104 G28

LDO Output Voltage vs $V_{IN(LDO)}$ Supply Voltage



3104 G29

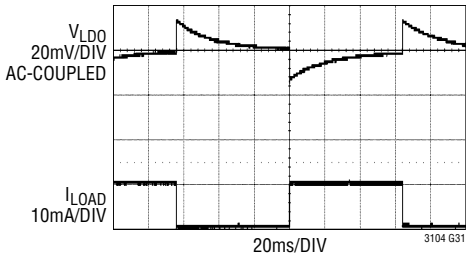
LDO Output Voltage vs Load Current



3104 G30

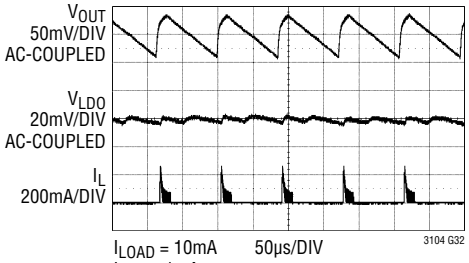
TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C unless otherwise noted

LDO Output Voltage Load Step



I_{LOAD} = LOAD STEP, NO LOAD TO 10mA
V_{LDO} = 1.8V
$V_{IN(LDO)}$ = V_{IN} = 10V
C_{IN} = 10µF
C_{OUT} = 10µF

LDO Ripple Rejection (Automatic Burst Mode Operation)



I_{LDO} = 1mA
V_{LDO} = 1.8V, V_{IN} = 10V
$V_{IN(LDO)}$ = V_{OUT} = 2.5V
C_{IN} = 10µF, C_{OUT} = 22µF
C_{LDO} = 4.7µF, L = 10µH

PIN FUNCTIONS (DFN/MSOP)

MODE (Pin 1/Pin 2): Logic-Controlled Input to Select Mode of Operation. Forcing this pin high commands high efficiency automatic Burst Mode operation where the buck will automatically transition from PWM operation at heavy load to Burst Mode operation at light loads. Forcing this pin low commands low noise, fixed frequency, forced continuous operation.

V_{IN} (Pin 2/Pin 3): Main Supply Pin. Decouple with a 10µF or larger ceramic capacitor. The capacitor should be as close to the part as possible.

SW (Pin 3/Pin 4): Switch Pin Connects to the Inductor. This pin connects to the drains of the internal main and synchronous power MOSFET switches.

BST (Pin 4/Pin 5): Bootstrapped Floating Supply for High Side Gate Drive. Connect to SW through a 22nF (minimum) capacitor. The capacitor must be connected between BST and SW and be located as close as possible to the part as possible.

GND (Pin 5/Pin 6): Power Ground.

RUNLDO (Pin 6/Pin 7): Logic-Controlled LDO Enable Pin. This pin may be tied to V_{IN} to enable the LDO.

PGOOD (Pin 7/Pin 8): Open-drain output that is pulled to ground when the feedback voltage falls 10% (typical) below the regulation point, during a thermal shutdown event or if the converter is disabled. The PGOOD output is valid 1ms after the buck converter is enabled.

NC (Pin 8/Pins 1, 9, 16): No Connect Pin(s) Must Be Tied to GND.

V_{CC} (Pin 9/Pin 10): Internally Regulated Supply Rail. Internal power rail regulated off of V_{IN} to power control circuitry. Decouple with a 1µF or larger ceramic capacitor placed as close to the part as possible.

RUN (Pin 10/Pin 11): Run Pin Comparator Input. A voltage greater than 0.85V will enable the IC. Tie this pin to V_{IN} to enable the IC or connect to an external resistor divider from V_{IN} to provide an accurate undervoltage lockout threshold. 60mV of hysteresis is provided internally.

FB (Pin 11/Pin 12): Feedback Input to Error Amplifier. The resistor divider connected to this pin sets the buck converter output voltage.

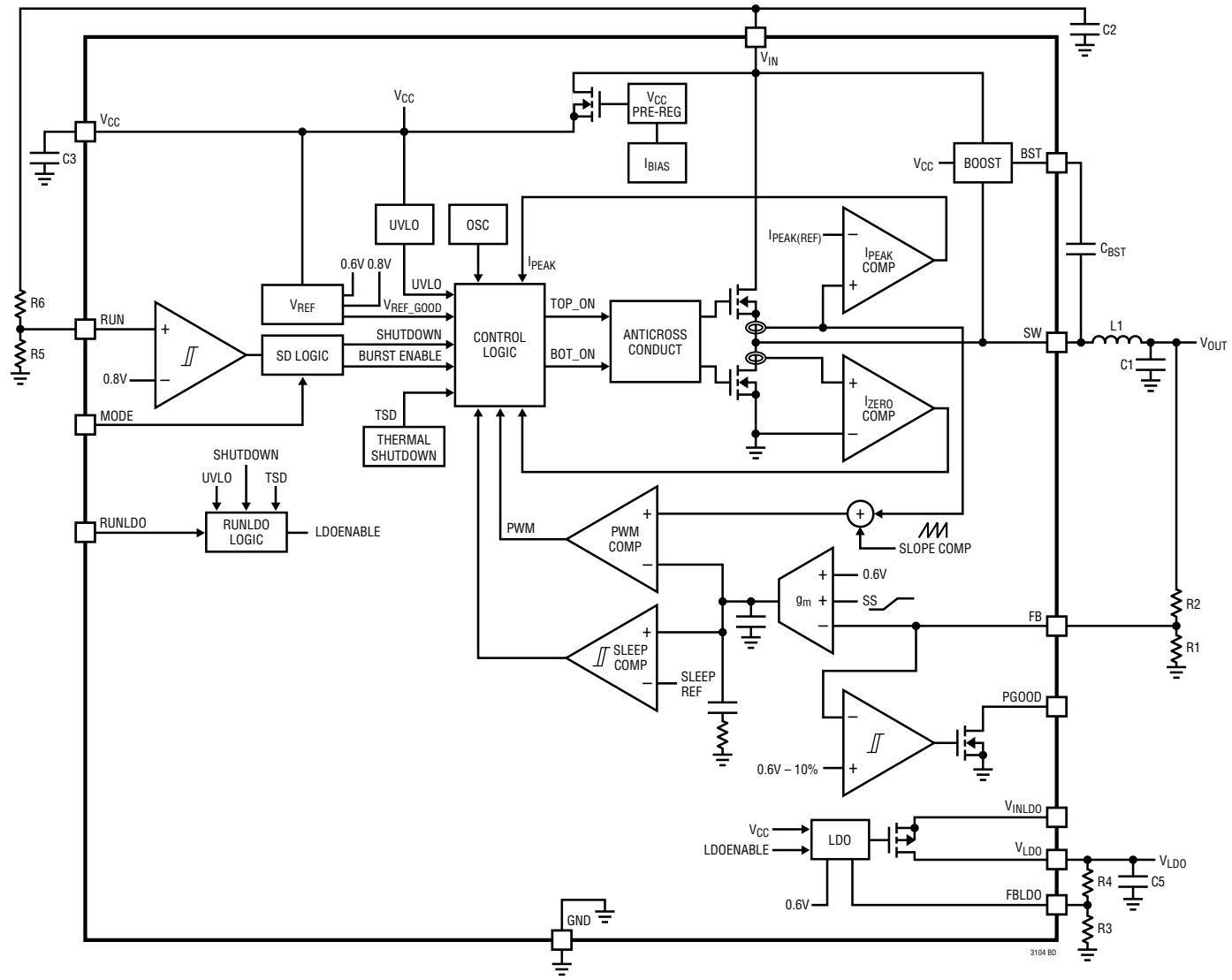
FBLDO (Pin 12/Pin 13): Feedback Input to the LDO Error Amplifier. The resistor divider on this pin sets the LDO output voltage.

V_{LDO} (Pin 13/Pin 14): LDO Regulator Output. Decouple with a 4.7µF or larger ceramic capacitor placed as close to the part as possible.

V_{INLDO} (Pin 14/Pin 15): LDO Supply Pin (15V Maximum). Decouple with a 10µF or larger ceramic capacitor.

GND (Exposed Pad Pin 15/Exposed Pad Pin 17): Back-pad Ground Common. This pad must be soldered to the PC board and connected to the ground plane for optimal thermal performance.

BLOCK DIAGRAM



OPERATION

The LTC3104 step-down DC/DC converter is capable of supplying 300mA to the load. The output voltage is adjustable over a broad range and can be set as low as 0.6V. Both the power and the synchronous rectifier switches are internal N-channel MOSFETs. The converter uses a constant-frequency, current mode architecture and may be configured using automatic Burst Mode operation for highly efficient light load operation or for low noise forced continuous conduction operation where the converter is optimized to operate over a broad range of step-down ratios without pulse skipping. With the automatic Burst Mode feature and the LDO enabled, the typical DC supply current drops to only 2.6µA with no load. The LTC3104 also includes an independent, 10mA LDO regulator with a V_{IN} range of 2.5V to 15V.

Main Control Loop

During normal operation, the internal top power MOSFET is turned on at the beginning of each cycle and turned off when the PWM current comparator trips. The peak

OPERATION

inductor current where the comparator trips is controlled by the voltage on the output of the error amplifier. The FB pin allows the internally compensated error amplifier to receive an output feedback voltage from an external resistive divider from V_{OUT}. When the load current increases, the output begins to fall causing a slight decrease in the feedback voltage relative to the 0.6V reference, this in turn, causes the control voltage to increase until the average inductor current matches the new load current. While the top MOSFET is off, the bottom MOSFET is turned on until either the inductor current starts to reverse as indicated by the current reversal comparator, I_{ZERO}, or the beginning of the next clock cycle. I_{ZERO} is set to 40mA (typical) in automatic Burst Mode operation and –110mA (typical) in forced continuous mode.

Forced Continuous Mode

Grounding MODE enables forced continuous operation and disables Burst Mode operation. At light loads, forced continuous mode minimizes output voltage ripple and noise but is less efficient than Burst Mode operation. Forced continuous operation may be desirable for use in applications that are sensitive to the Burst Mode output voltage ripple or its harmonics. The LTC3104 offers a broad range of possible step down ratios without pulse skipping but for very small step-down ratios, the minimum on-time of the main switch will be reached and the converter will begin turning off for multiple cycles in order to maintain regulation.

Burst Mode Operation

Holding the MODE pin above 1.2V will enable automatic Burst Mode operation and disable forced continuous operation. As the load current increases, the converter will automatically transition between Burst Mode and PWM operation. Conversely the converter will automatically transition from PWM operation to Burst Mode operation as the load decreases. Between bursts the converter is not active (i.e., both switches are off) and most of the internal circuitry is disabled to reduce the quiescent current to 2.6µA. Burst Mode entry and exit is determined by the peak inductor current and therefore the load current at which Burst Mode operation will be entered or exited depends on the input voltage, the output voltage and the inductor value. Typical curves for Burst Mode entry threshold are provided in the Typical Performance Characteristics section of this data sheet.

Soft-Start

The converter has an internal closed-loop soft-start circuit with a nominal duration of 1.4ms. The converter remains in regulation during soft-start and will therefore respond to output load transients that occur during this time. In addition, the output voltage rise time has minimal dependency on the size of the output capacitor or load current.

Thermal Shutdown

If the die temperature exceeds 150°C (typical) the converter and LDO will be disabled. All power devices will be turned off and the switch node will be forced into a high impedance state. The soft-start circuit is reset during thermal shutdown to provide a smooth recovery once the overtemperature condition is eliminated. If enabled, the converter and the LDO will restart when the die temperature drops to approximately 130°C.

Power Good Status Output

The PGOOD pin is an open-drain output which indicates the output voltage status of the step-down converter. If the output voltage falls 10% below the regulation voltage, the PGOOD open-drain output will pull low. A built-in deglitching delay prevents false trips due to voltage transients on load steps. The output voltage must rise 2% above the falling threshold before the pull-down will turn off. The PGOOD output will also pull low during overtemperature shutdown and undervoltage lockout to indicate these fault conditions. The PGOOD output is valid 1ms after the buck converter is enabled. When the converter is disabled the open-drain device is forced on into a low impedance state. The PGOOD pull-up voltage must be below the 6V absolute maximum voltage rating of the pin.

Current Limit

The peak inductor current limit comparator shuts off the buck switch once the internal limit threshold is reached. Peak switch current is no less than 400mA.

OPERATION

Slope Compensation

Current mode control requires the use of slope compensation to prevent sub-harmonic oscillations in the inductor current waveform at high duty cycle operation. In some current mode ICs, current limiting is performed by clamping the error amplifier voltage to a fixed maximum which leads to a reduced output current capability at low step-down ratios. Slope compensation is accomplished on the LTC3104 internally through the addition of a compensating ramp to the current sense signal. The current limiting function is completed prior to the addition of the compensation ramp and therefore achieves a peak inductor current limit that is independent of duty cycle.

Short-Circuit Protection

When the output is shorted to ground, the error amplifier will saturate high and the high side switch will turn on at the start of each cycle and remain on until the current limit trips. During this minimum on-time, the inductor current will increase rapidly and will decrease very slowly during the remainder of the period due to the very small reverse voltage produced by a hard output short. To eliminate the possibility of inductor current runaway in this situation, the switching frequency is reduced to approximately 300kHz when the voltage on FB falls below 0.3V.

BST Pin Function

The input switch driver operates from the voltage generated on the BST pin. An external capacitor between the SW and BST pins and an internal synchronous PMOS boost switch are used to generate a voltage that is higher than the input voltage. When the synchronous rectifier is on (SW is low) the internal boost switch connects one side of the capacitor to V_{CC} replenishing its charge. When the synchronous rectifier is turned off the input switch is turned on forcing SW high and the BST pin is at a potential equal to V_{CC} + SW, relative to ground.

A comparator ensures there is sufficient voltage across the boost capacitor to guarantee start-up after long sleep periods or if starting up into a pre-biased output.

Undervoltage Lockout

The LTC3104 has an internal UVLO which disables the converter if the supply voltage decreases below 2.1V (typical). The soft-start for the converter will be reset during undervoltage lockout to provide a smooth restart once the input voltage increases above the undervoltage lockout threshold. The RUN pin can alternatively be configured as a precise undervoltage lockout (UVLO) on the V_{IN} supply with a resistive divider connected to the RUN pin.

V_{LDO} OUTPUT

The V_{LDO} output utilizes an internal PMOS pass device that is guaranteed to support a 10mA load with a typical dropout voltage of 150mV. The LDO is powered by the V_{INLDO} input which can be tied to an independent power source or to the V_{OUT} of the step-down converter. V_{INLDO} can be tied to V_{IN} only if V_{IN} is guaranteed to be within the absolute maximum ratings of the V_{INLDO} pin. The quiescent current will increase by about 0.3µA when V_{INLDO} is tied to V_{IN}. The V_{LDO} output is only active when V_{IN} is greater than the UVLO threshold and the RUNLDO pin is high but can be disabled independently by bringing RUNLDO below 0.5V.

The LDO is specifically designed to be stable with a small 4.7µF capacitor, but to also maintain stable operation with arbitrarily large capacitance values without requiring a series resistor. The LDO output is current-limit protected to 20mA (typ). During an undervoltage or overtemperature fault, the LDO is disabled until the fault condition clears.

APPLICATIONS INFORMATION

The basic LTC3104 application circuit is shown as the Typical Application on the front page of this data sheet. The external component selection is determined by the desired output voltage, output current, desired noise immunity and ripple voltage requirements for each particular application. However, basic guidelines and considerations for the design process are provided in this section.

Inductor Selection

The choice of inductor value influences both the efficiency and the magnitude of the output voltage ripple. Larger inductance values will reduce inductor current ripple and will therefore lead to lower output voltage ripple. For a fixed DC resistance, a larger value inductor will yield higher efficiency by lowering the peak current to be closer to the average. However, a larger value inductor within the same family will generally have a greater series resistance, thereby offsetting this efficiency advantage. Given a desired peak to peak current ripple, ΔI_L (A), the required inductance can be calculated via the following expression:

$$L \geq \frac{V_{OUT}}{1.2 \bullet \Delta I_L} \bullet \left(1 - \frac{V_{OUT}}{V_{IN}}\right) (\mu H)$$

A reasonable choice for ripple current is ΔI_L = 120mA which represents 40% of the maximum 300mA load current. The DC current rating of the inductor should be at least equal to the maximum load current plus half the ripple current in order to prevent core saturation and loss of efficiency during operation. To optimize efficiency the inductor should have a low series resistance. In particularly space restricted applications it may be advantageous to use a much smaller value inductor at the expense of larger ripple current. In such cases, the converter will operate in discontinuous conduction for a wider range of output loads and efficiency will be reduced. In addition, there is a minimum inductor value required to maintain stability of the current loop (given the fixed internal slope compensation). Specifically, if the buck converter is going to be utilized at duty cycles greater than 40%, the inductance value must be at least L_{MIN} as given by the following equation:

$$L_{MIN} \geq 2.5 \bullet V_{OUT} (\mu H)$$

Table 1 depicts the minimum required inductance for several common output voltages using standard inductor values.

Table 1. Minimum Inductance

OUTPUT VOLTAGE (V)	MINIMUM INDUCTANCE (µH)
0.8	2.2
1.2	3.3
2.0	5.6
2.7	6.8
3.3	8.3
5.0	15

A large variety of low ESR, power inductors are available that are well suited to the LTC3104 converter applications. The trade-off generally involves PCB area, application height, required output current and efficiency. Table 2 provides a representative sampling of small surface mount inductors that are well suited for use with the LTC3104 buck converter. The inductor specifications listed are for comparison purposes but other values within these inductor families are generally well suited to this application as well. Within each family (i.e., at a fixed inductor size), the DC resistance generally increases and the maximum current generally decreases with increased inductance.

Output Capacitor Selection

A low ESR output capacitor should be utilized at the buck output in order to minimize voltage ripple. Multilayer ceramic capacitors are an excellent choice as they have low ESR and are available in small footprints. In addition to controlling the output ripple magnitude, the value of the output capacitor also sets the loop crossover frequency and therefore can impact loop stability. There is both a minimum and maximum capacitance value required to

APPLICATIONS INFORMATION

Table 2. Representative Inductor Selection

PART NUMBER	VALUE (µH)	DCR (Ω)	MAX DC CURRENT (A)	SIZE (MM) W × L × H
Coilcraft				
EPL3015	6.8	0.19	1.00	3.0 × 3.0 × 1.5
LPS3314	10	0.33	0.70	3.3 × 3.3 × 1.3
LPS4018	15	0.26	1.12	4.0 × 4.0 × 1.8
Cooper-Bussman				
SD3114	6.8	0.30	0.98	3.1 × 3.1 × 1.4
SD3118	10	0.3	0.75	3.2 × 3.2 × 1.8
Murata				
LQH3NPN	6.8	0.20	1.25	3.0 × 3.0 × 1.4
LQH44PN	10	0.16	1.10	4.0 × 4.0 × 1.7
Sumida				
CDRH3D16	6.8	0.17	0.73	3.8 × 3.8 × 1.8
CDRH3D16	10	0.21	0.55	3.8 × 3.8 × 1.8
Taiyo-Yuden				
CBC3225	6.8	0.16	0.93	3.2 × 2.5 × 2.5
NR3015	10	0.23	0.70	3.0 × 3.0 × 1.5
NR4018	15	0.30	0.65	4.0 × 4.0 × 1.8
Würth				
744029006	6.8	0.25	0.95	2.8 × 2.8 × 1.4
744031006	6.8	0.16	0.85	3.8 × 3.8 × 1.7
744031100	10	0.19	0.74	3.8 × 3.8 × 1.7
744031100	15	0.26	0.62	3.8 × 3.8 × 1.7
Panasonic				
ELLVGG6R8N	6.8	0.23	1.00	3.0 × 3.0 × 1.5
ELL4LG100MA	10	0.20	0.80	3.8 × 3.8 × 1.8
TDK				
VLF3012	6.8	0.18	0.78	3.0 × 2.8 × 1.2
VLC4018	10	0.16	0.85	4.0 × 4.0 × 1.8

ensure stability of the loop. If the output capacitance is too small, the loop crossover frequency will increase to the point where switching delay and the high frequency parasitic poles of the error amplifier will degrade the phase margin. In addition, the wider bandwidth produced by a small output capacitor will make the loop more susceptible to switching noise. At the other extreme, if the output capacitor is too large, the crossover frequency can decrease too far below the compensation zero and also lead to degraded phase margin. Table 3 provides a guideline for the range of allowable values of low ESR output capacitors assuming a feedforward capacitor is used. See the Output Voltage Programming section for more details on selecting a feedforward capacitor. Larger value output capacitors can be accommodated provided they have sufficient ESR to stabilize the loop, or by increasing the value of the feedforward capacitor in parallel with the upper resistor divider resistor.

In Burst Mode operation, the output capacitor stores energy to satisfy the load current when the LTC3104 is in a low current sleep state between the burst pulses. It can take several cycles to respond to a large load step during a sleep period. If large transient load currents are required then a larger capacitor can be used at the output to minimize output voltage droop until the part transitions from Burst Mode operation to continuous mode operation.

Note that even X5R and X7R type ceramic capacitors have a DC bias effect which reduces their capacitance when a DC voltage is applied. It is not uncommon for capacitors offered in the smallest case sizes to lose more than 50% of their capacitance when operated near their rated voltage. As a result it is sometimes necessary to use a larger capacitance value or use a higher voltage rating in order to realize the intended capacitance value. Consult the manufacturer's data for the capacitor you select to be assured of having the necessary capacitance in your application.

Table 3. Recommended Output Capacitor Limits

OUTPUT VOLTAGE (V)	C_{MIN} (µF)	C_{MAX} (µF)
0.8	22.0	220
1.2	15.0	220
2.0	12.0	100
2.7	6.8	68
3.3	4.7	47
5.0	4.7	47

APPLICATIONS INFORMATION

Input Capacitor Selection

The V_{IN} and V_{INLDO} pins provide current to the power stages of the buck converter and the LDO, respectively. It is recommended that a low ESR ceramic capacitor with a value of at least 10µF be used to bypass each of these pins. These capacitors should be placed as close to the respective pin as possible and should have a short return path to the GND pin.

Output Voltage Programming

The output voltage is set by a resistive divider according to the following formula:

$$V_{OUT} = 0.6V \bullet \left(1 + \frac{R2}{R1}\right)$$

The external divider is connected to the output as shown in Figure 1. Note that FB divider current is not included in the LTC3104 quiescent current specification. For improved transient response, a feedforward capacitor, C_{FF}, may be placed in parallel with resistor R2. The capacitor modifies the loop dynamics by adding a pole-zero pair to the loop dynamics which generates a phase boost that can improve the phase margin and increase the speed of the transient response, resulting in smaller voltage deviation on load transients. The zero frequency depends not only on the value of the feed forward capacitor, but also on the upper resistor divider resistor. Specifically, the zero frequency, f_{ZERO}, is given by the following equation:

$$f_{ZERO} = \frac{1}{2 \bullet \pi \bullet R2 \bullet C_{FF}}$$

For R2 resistor values of ~1M a 12pF ceramic capacitor will suffice, however that value may be increased or decreased to optimize the converter's response for a given set of application parameters. In a Burst Mode application for instance, a C_{FF} = 27pF will lower output voltage ripple at light load.

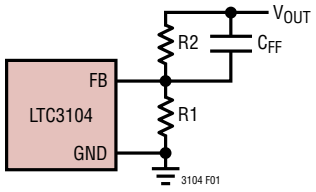


Figure 1. Setting the Output Voltage

Minimum Off-Time/On-Time Considerations

The maximum duty cycle is limited in the LTC3104 by the boost capacitor refresh time, the rise/fall times of the switch as well as propagation delays in the PWM comparator, the level shifts and the gate drive. This minimum off-time is typically 65ns which imposes a maximum duty cycle of:

$$DC_{MAX} = 1 - (f \bullet t_{OFF(MIN)})$$

where f is the 1.2MHz switching frequency and $t_{OFF(MIN)}$ is the minimum off-time. If the maximum duty cycle is surpassed, due to a dropping input voltage for example, the output will drop out of regulation. The minimum input voltage to avoid this dropout condition is:

$$V_{IN(MIN)} = \frac{V_{OUT}}{1 - \left(f \bullet t_{OFF(MIN)}\right)}$$

Conversely, the minimum on-time is the smallest duration of time in which the buck switch can be in its "on" state. This time is limited by similar factors and is typically 70ns. In forced continuous operation, the minimum on-time limit imposes a minimum duty cycle of:

$$DC_{MIN} = f \bullet t_{ON(MIN)}$$

where $t_{ON(MIN)}$ is the minimum on-time. In extreme step-down ratios where the minimum duty cycle is surpassed, the output voltage will still be in regulation but the rectifier switch will remain on for more than one cycle and sub-harmonic switching will occur to provide a higher effective duty cycle. The result is higher output voltage ripple. This is an acceptable result in many applications so this constraint may not be of critical importance in some cases.

Precise Undervoltage Lockout

The LTC3104 is in shutdown when the RUN pin is low and active when the pin is higher than the RUN pin threshold. The rising threshold of the RUN pin comparator is an accurate 0.8V, with 60mV of hysteresis. This threshold is enabled when V_{IN} is above the 2.5V minimum value. If V_{IN} is lower than 2.5V, an internal undervoltage monitor puts the part in shutdown independent of the RUN pin state.

APPLICATIONS INFORMATION

The RUN pin can be configured as a precise undervoltage lockout (UVLO) on the V_{IN} supply with a resistive divider tied to the RUN pin as shown in Figure 2 to meet specific V_{IN} voltage requirements. If used, note that the external divider current is not included in the LTC3104 quiescent current specification.

The rising UVLO threshold can be calculated using the following equation:

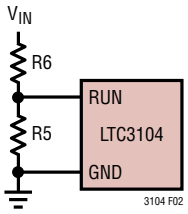


Figure 2. Setting the Undervoltage Lockout Threshold

$$V_{UVLO} = 0.8V \bullet \left(1 + \frac{R6}{R5}\right)$$

Internal V_{CC} Regulator

The LTC3104 uses an internal NMOS source follower regulator off of V_{IN} to generate a low voltage internal rail, V_{CC}. The regulator is designed to deliver current only to the internal drivers and other internal control circuits and not to an external load. The V_{CC} pin should be bypassed with a 1µF or larger ceramic capacitor.

Boost Capacitor Selection

The LTC3104 uses a bootstrapped supply to power the buck switch gate drivers. When the synchronous rectifier turns on, an internal PMOS switch turns on synchronously to charge the boost capacitor, C_{BST}, to the voltage on V_{CC}. For most applications a 0.022µF will suffice. The capacitor should be placed as close to the respective pins as possible.

LDO Output Capacitor Selection

The LDO is designed to be stable with a minimum 4.7µF output capacitor. No series resistor is required when using low ESR capacitors. For most applications, a 10µF ceramic capacitor is recommended. Larger values will improve transient response and raise the power supply rejection ratio (PSRR) of the LDO.

LDO Output Voltage Programming

The output voltage is set by a resistive divider according to the following formula:

$$V_{LDO} = 0.6V \bullet \left(1 + \frac{R4}{R3}\right)$$

The external divider is connected to the LDO output, V_{LDO}, as shown in Figure 3. Similar to the buck feedback network, a feedforward capacitor may be placed in parallel with resistor R4 for improved transient response. For resistor values of ~1M a 12pF ceramic capacitor will suffice.

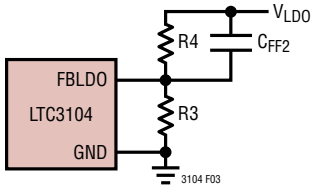


Figure 3. Setting the LDO Output Voltage

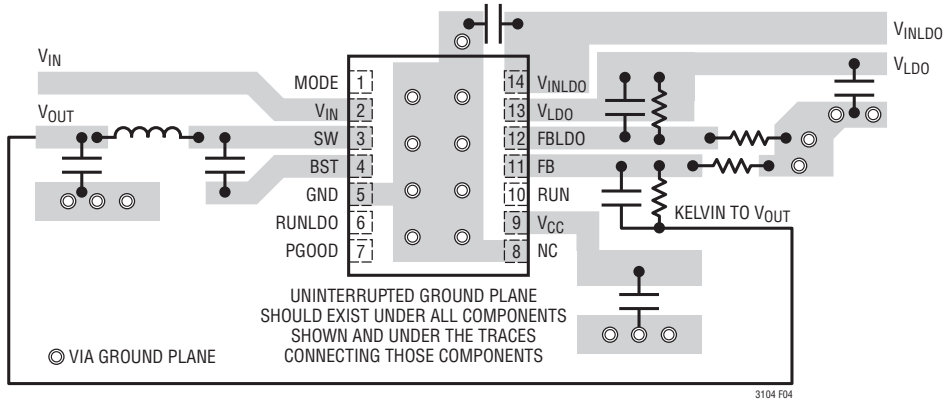
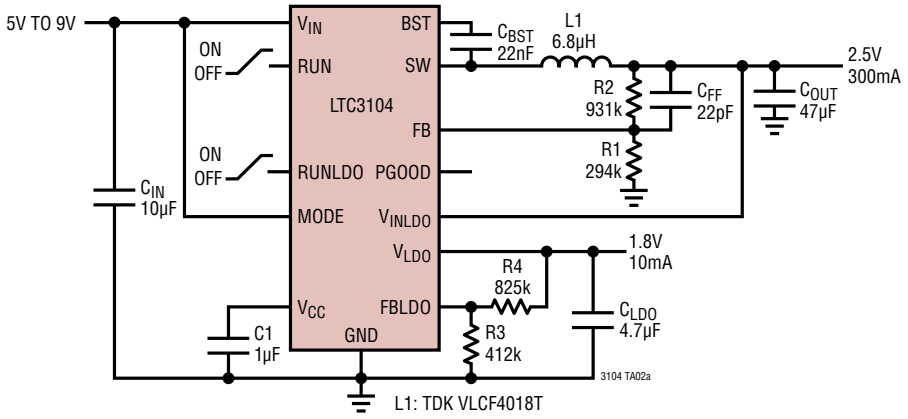


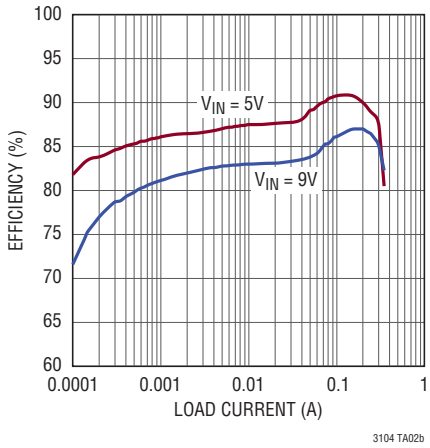
Figure 4. PCB Layout Recommendations

TYPICAL APPLICATIONS

Dual Lithium-Ion to 2.5V/300mA Regulator with 1.8V /10mA LDO

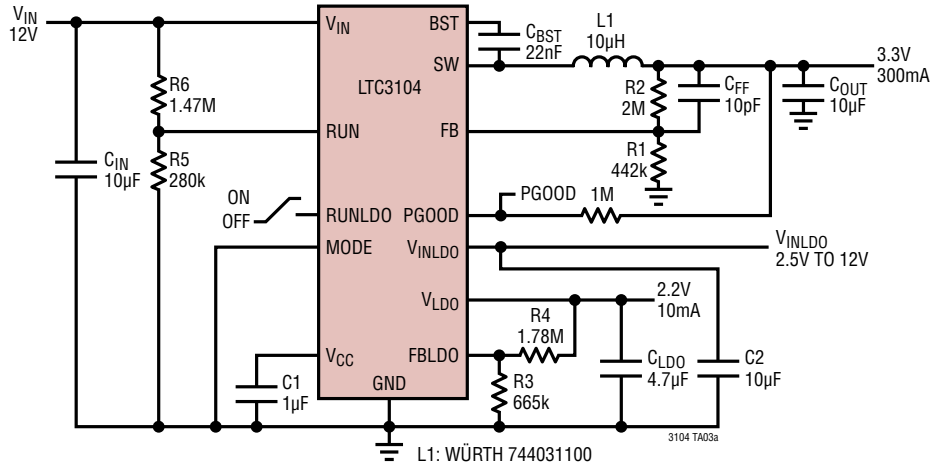


Efficiency vs Output Current

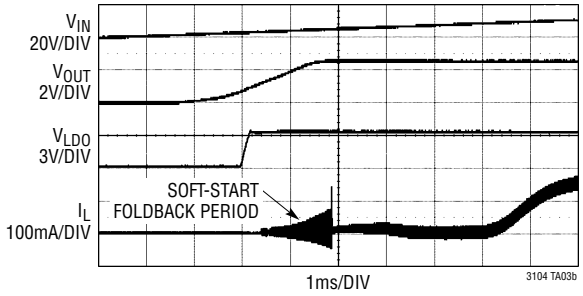


TYPICAL APPLICATIONS

12V to 3.3V/300mA Regulator with Accurate 5V UVLO, Forced Continuous Operation and Independently Powered LDO

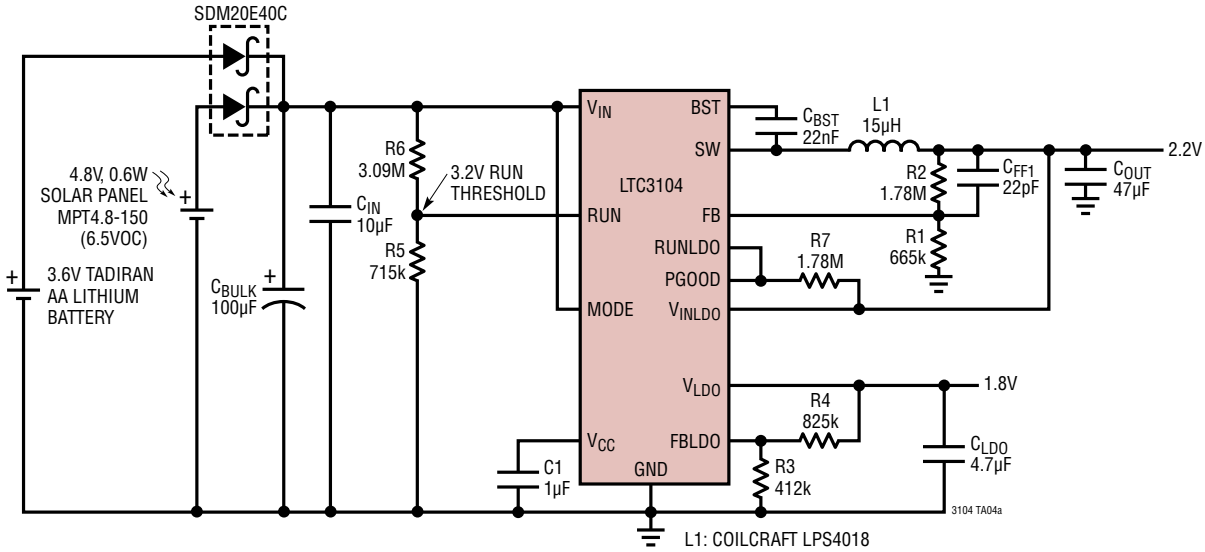


Start-Up with Ramped Input Power into 100mA Load on V_{OUT}



TYPICAL APPLICATIONS

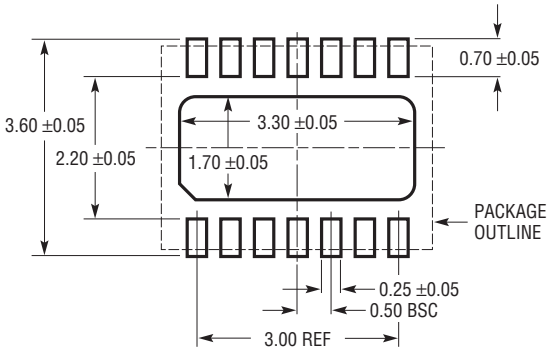
Solar-Powered 2.2V Supply and 1.8V LDO with Li Battery Backup and Run Threshold Set to Battery Minimum Voltage



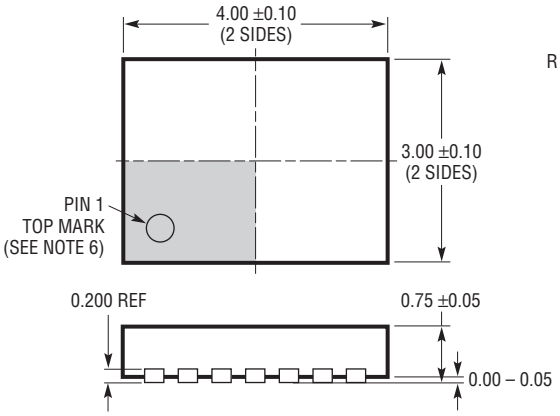
PACKAGE DESCRIPTION

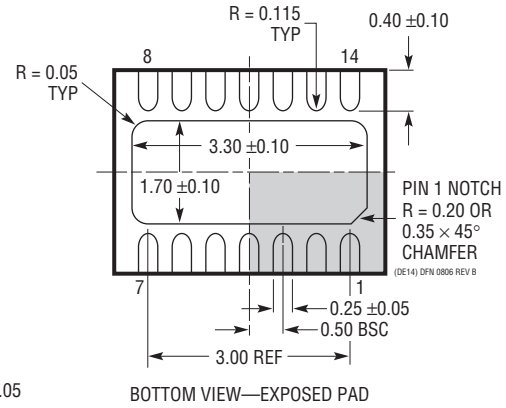
Please refer to http://www.linear.com/product/LTC3104#packaging for the most recent package drawings.

DE Package
14-Lead Plastic DFN (4mm × 3mm)
(Reference LTC DWG # 05-08-1708 Rev B)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED





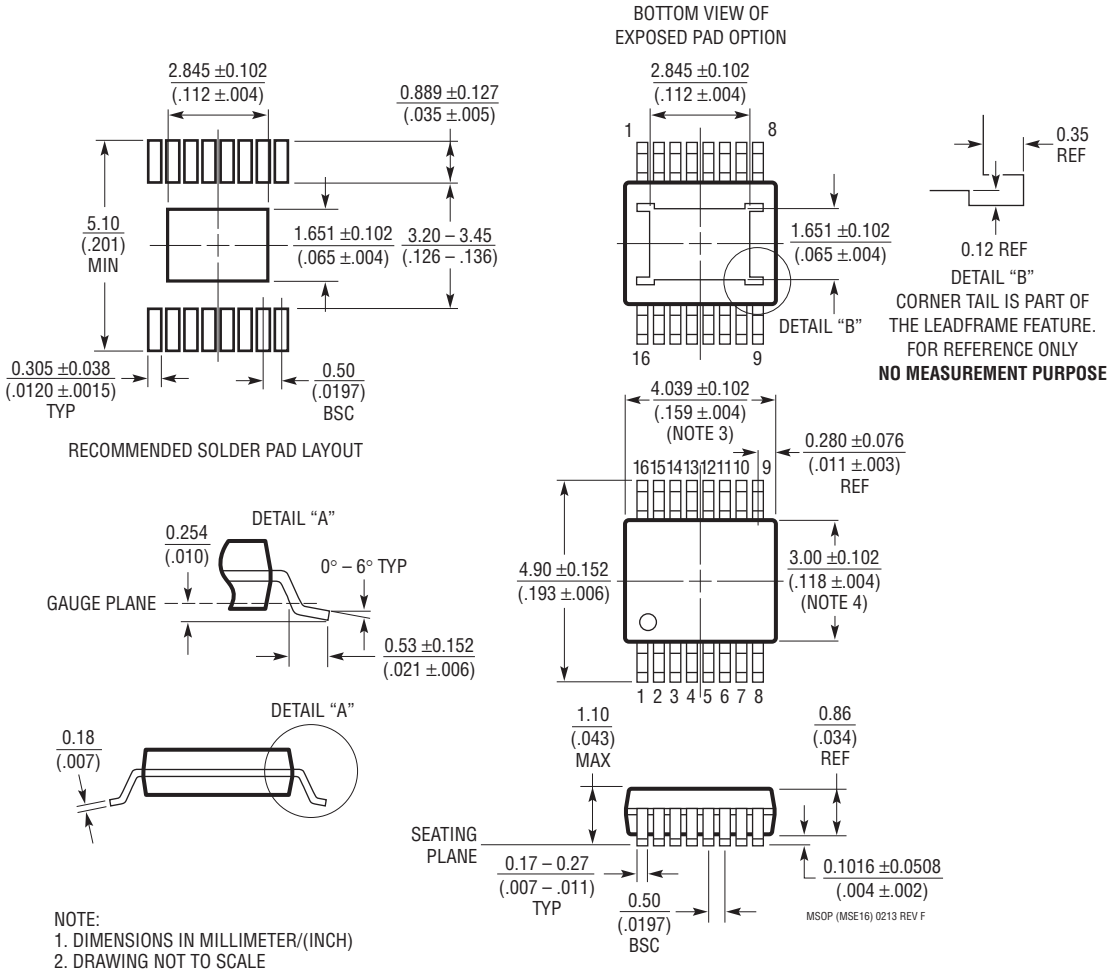
BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING PROPOSED TO BE MADE VARIATION OF VERSION (WGED-3) IN JEDEC PACKAGE OUTLINE MO-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LTC3104#packaging for the most recent package drawings.

MSE Package
16-Lead Plastic MSOP, Exposed Die Pad
(Reference LTC DWG # 05-08-1667 Rev F)



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX
6. EXPOSED PAD DIMENSION DOES INCLUDE MOLD FLASH. MOLD FLASH ON E-PAD SHALL
   NOT EXCEED 0.254mm (.010") PER SIDE.

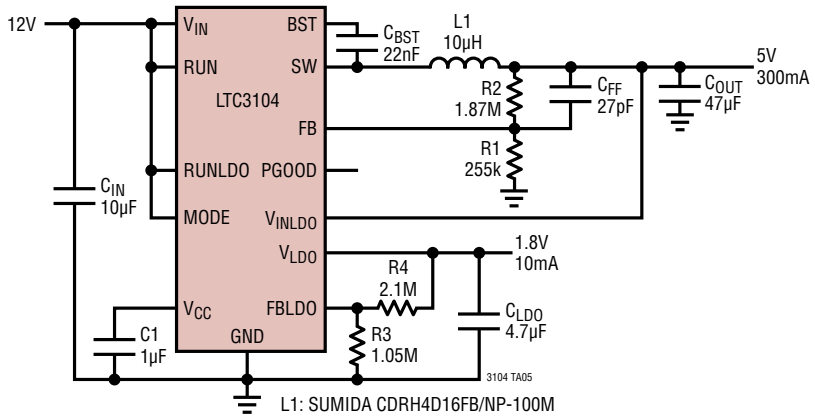
REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	07/16	Updated Typical Application circuit. Updated Input Voltage Range condition to include After Start-Up. Added another line for Start-Up. Updated Soft-Start Time condition to include V_{IN} = 5V. Replaced G13. Corrected RUN Pin Function description. Replaced Block Diagram, V_{CC} regulator pass element PMOS with NMOS. Updated Application Information. Updated application circuits.	1 3 3 6 8 9 14 16, 28, 22

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

TYPICAL APPLICATION

12V to 5V/300mA Regulator with High Efficiency, Ultralow I_Q (2.8µA with V_{OUT} in Regulation, No Load) and 1.8V/10mA LDO



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC3103	15V, 300mA Synchronous Step-Down DC/DC Converter with Ultralow Quiescent Current	V_{IN}: 2.5V to 15V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 1.8µA, I_{SD} = 1µA, 3mm × 3mm DFN-10, MSOP-10
LTC3642	45V (Transient to 60V) 50mA Synchronous Step-Down DC/DC Converter	V_{IN}: 4.5V to 45V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 12µA, I_{SD} < 1µA, 3mm × 3mm DFN-8, MSOP-8
LTC3631	45V (Transient to 60V) 100mA Synchronous Step-Down DC/DC Converter	V_{IN}: 4.5V to 45V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 12µA, I_{SD} < 1µA, 3mm × 3mm DFN-8, MSOP-8
LTC3632	50V (Transient to 60V) 20mA Synchronous Step-Down DC/DC Converter	V_{IN}: 4.5V to 50V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 12µA, I_{SD} < 1µA, 3mm × 3mm DFN-8, MSOP-8
LTC3388-1/LTC3388-3	20V, 50mA High Efficiency Nano Power Step-Down Regulators	V_{IN}: 2.7V to 20V, $V_{OUT(MIN)}$ Fixed 1.1V to 5.5V, I_Q = 720nA, I_{SD} = 400nA, 3mm × 3mm DFN-10, MSOP-10
LTC3108/LTC3108-1	Ultralow Voltage Step-Up Converter and Power Managers	V_{IN}: 0.02V to 1V, $V_{OUT(MIN)}$ Fixed 2.35V to 5V, I_Q = 6µA, I_{SD} < 1µA, 3mm × 4mm DFN-12, SSOP-16
LTC3109	Auto-Polarity, Ultralow Voltage Step-Up Converter and Power Manager	V_{IN}: 0.03V to 1V, $V_{OUT(MIN)}$ Fixed 2.35V to 5V, I_Q = 7µA, I_{SD} < 1µA, 4mm × 4mm QFN-20, SSOP-20
LTC4071	Li-Ion/Polymer Shunt Battery Charger System with Low Battery Disconnect	Charger Plus Pack Protection in One IC Low Operating Current (550nA), 50mA Internal Shunt Current, Pin Selectable Float Voltages (4.0V, 4.1V, 4.2V), 8-Lead, 2mm × 3mm, DFN and MSOP Packages
LTC4070	Li-Ion/Polymer Low Current Shunt Battery Charger System	Selectable V_{FLOAT} = 4.0V, 4.1V, 4.2V, Max Shunt Current = 50mA, I_{CCQ} = 450nA to 1.04mA, I_{CCQLB} = 300nA, 2mm × 3mm DFN-8, MSOP-8
LTC1877	10V, 600mA High Efficiency Synchronous Step-Down DC/DC Converter	V_{IN}: 2.65V to 10V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 10µA, I_{SD} < 1µA, MSOP-8
LTC3105	5V, 400mA, MPPC Step-Down Converter with 250mV Start-Up	V_{IN}: 0.225V to 5V, $V_{OUT(MAX)}$ = 5.25V, I_Q = 24µA, I_{SD} = 10µA, 3mm × 3mm DFN-10, MSOP-12

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