4-Channel PMBus Power System Manager Featuring Accurate Output Current Measurement

FEATURES

- **Sequence, Trim, Margin and Supervise Four Power Supplies**
- **Manage Faults, Monitor Telemetry and Create Fault Logs**
- **PMBus™ Compliant Command Set**
- **Supported by LTpowerPlay® GUI**
- **Margin or Trim Supplies to within 0.25% of Target**
- **Fast OV/UV Supervisors Per Channel**
- **Fast Output Current Supervisors Per Channel**
- **Coordinate Sequencing and Fault Management Across Multiple LTC PSM Devices**
- **Automatic Fault Logging to Internal EEPROM**
- **Operate Autonomously without Additional Software**
- External Temperature and Input Voltage Supervisors
- Accurate Monitoring of Four Output Voltages, Four Output Currents, Four External Temperatures, Input Voltage and Internal Die Temperature
- I^2C/SMBus Serial Interface
- Can Be Powered from 3.3V, or 4.5V to 15V
- Available in 64-Lead 9mm × 9mm QFN Package

APPLICATIONS

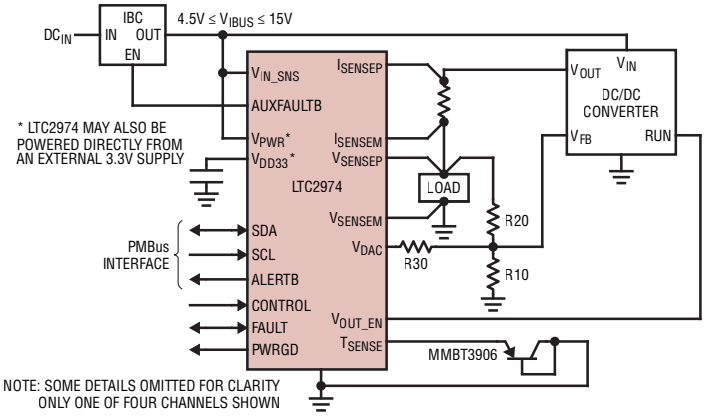
- Computers and Network Servers
- Industrial Test and Measurement
- High Reliability Systems
- Medical Imaging
- Video

DESCRIPTION

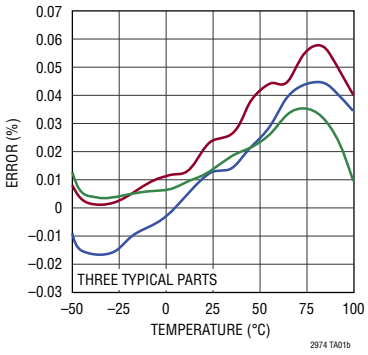
The LTC®2974 is a 4-channel Power System Manager used to sequence, trim (servo), margin, supervise, manage faults, provide telemetry and create fault logs. PMBus commands support power supply sequencing, precision point-of-load voltage adjustment and margining. DACs use a proprietary soft-connect algorithm to minimize supply disturbances. Supervisory functions include over and under current, voltage and temperature threshold limits for four power supply output channels as well as over and under voltage threshold limits for a single power supply input channel. Programmable fault responses can disable the power supplies with optional retry after a fault is detected. Faults that disable a power supply can automatically trigger black box EEPROM storage of fault status and associated telemetry. An internal 16-bit ADC monitors four output voltages, four output currents, four external temperatures, one input voltage and die temperature. Output power is also calculated. A programmable watchdog timer monitors microprocessor activity for a stalled condition and resets the microprocessor if necessary. A single wire bus synchronizes power supplies across multiple LTC Power System Management (PSM) devices. Configuration EEPROM with ECC supports autonomous operation without additional software.

TYPICAL APPLICATION

4-Channel PMBus Power System Manager



ADC Total Unadjusted Error vs Temperature



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ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

Supply Voltages:
- V_{PWR} ..... –0.3V to 15V
- V_{DD33} ..... –0.3V to 3.6V
- V_{DD25} ..... –0.3V to 2.75V

Digital Input/Output Voltages:
- ALERTB, SDA, SCL, CONTROL0, CONTROL1, CONTROL2, CONTROL3 ..... –0.3V to 3.6V
- PWRGD, SHARE_CLK, WDI/RESETB, WP, FAULTB0, FAULTB1 ..... –0.3V to 3.6 V
- ASEL0, ASEL1 ..... –0.3V to 3.6V

Analog Voltages:
- REFP ..... –0.3V to 1.35V
- REFM ..... –0.3V to 0.3V
- V_{IN_SNS} ..... –0.3V to 15V
- $V_{SENSEP[3:0]}$ ..... –0.3V to 6V
- $V_{SENSEM[3:0]}$ ..... –0.3V to 6V
- $I_{SENSEP[3:0]}$ ..... –0.3V to 6V
- $I_{SENSEM[3:0]}$ ..... –0.3V to 6V
- $V_{OUT\_EN[3:0]}$, AUXFAULTB ..... –0.3V to 15V
- $V_{DAC[3:0]}$ ..... –0.3V to 6V
- $T_{SENSE[3:0]}$ ..... –0.3V to 3.6V

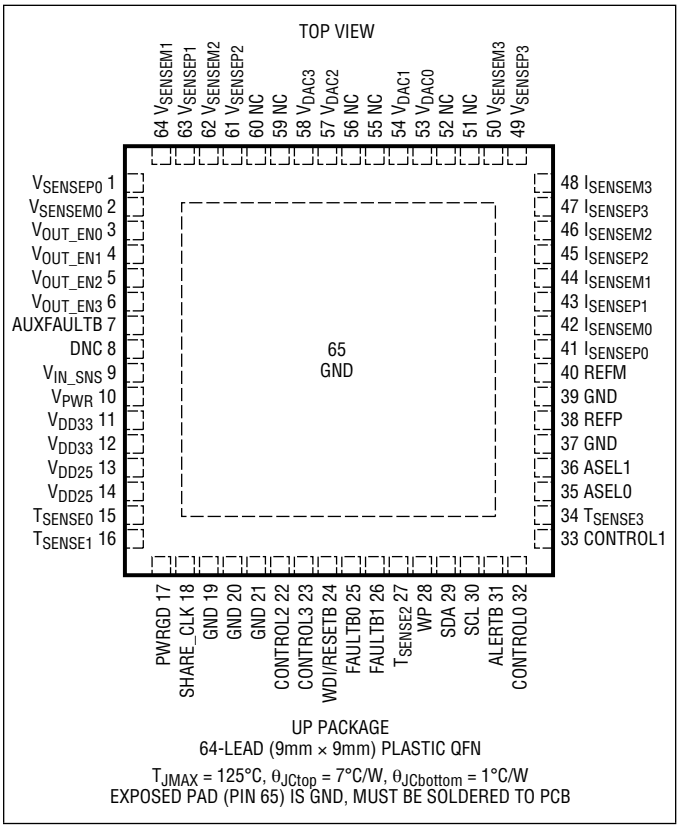
Operating Junction Temperature Range:
- LTC2974C ..... 0°C to 70°C
- LTC2974I ..... –40°C to 105°C

Storage Temperature Range ..... –65°C to 150°C*

Maximum Junction Temperature ..... 125°C*

*See OPERATION section for detailed EEPROM de-rating information for junction temperatures in excess of 105°C.

PIN CONFIGURATION



UP PACKAGE
64-LEAD (9mm × 9mm) PLASTIC QFN

T_{JMAX} = 125°C, θ_{JCtop} = 7°C/W, $\theta_{JCbottom}$ = 1°C/W
EXPOSED PAD (PIN 65) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC2974CUP#PBF	LTC2974CUP#TRPBF	LTC2974UP	64-Lead (9mm × 9mm) Plastic QFN	0°C to 70°C
LTC2974IUP#PBF	LTC2974IUP#TRPBF	LTC2974UP	64-Lead (9mm × 9mm) Plastic QFN	–40°C to 105°C

Contact the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_J = 25°C. V_{PWR} = V_{IN_SNS} = 12V, V_{DD33}, V_{DD25}, REFP and REFM pins floating, unless otherwise indicated. C_{VDD33} = 100nF, C_{VDD25} = 100nF and C_{REF} = 100nF. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Power Supply Characteristics							
V_{PWR}	V_{PWR} Supply Input Operating Range	V_{DD33} Floating	●	4.5		15	V
I_{PWR}	V_{PWR} Supply Current	4.5V ≤ V_{PWR} ≤ 15V, V_{DD33} Floating	●		10	13	mA
I_{VDD33}	V_{DD33} Supply Current	3.13V ≤ V_{DD33} ≤ 3.47V, V_{PWR} = V_{DD33}	●		10	13	mA
V_{UVLO_VDD33}	V_{DD33} Undervoltage Lockout	V_{DD33} Ramping Up, V_{PWR} = V_{DD33}	●	2.25	2.55	2.8	V
	V_{DD33} Undervoltage Lockout Hysteresis				120		mV
V_{DD33}	Supply Input Operating Range	V_{PWR} = V_{DD33}	●	3.13		3.47	V
	Regulator Output Voltage	4.5V ≤ V_{PWR} ≤ 15V	●	3.13	3.26	3.47	V
	Regulator Output Short-Circuit Current	V_{PWR} = 4.5V, V_{DD33} = 0V	●	75	90	140	mA
V_{DD25}	Regulator Output Voltage	3.13V ≤ V_{DD33} ≤ 3.47V	●	2.35	2.5	2.6	V
	Regulator Output Short-Circuit Current	V_{PWR} = V_{DD33} = 3.47V, V_{DD25} = 0V	●	30	55	80	mA
t_{INIT}	Initialization Time	Time from V_{IN} applied until the TON_DELAY timer starts			30		ms
Voltage Reference Characteristics							
V_{REF}	Output Voltage (Note 3)	V_{REF} = V_{REFP} – V_{REFM}, 0 < I_{REFP} < 100µA	●	1.220	1.232	1.244	V
	Temperature Coefficient				3		ppm/°C
	Hysteresis	(Note 4)			100		ppm
ADC Characteristics							
V_{IN_ADC}	Voltage Sense Input Range	Differential Voltage: V_{IN_ADC} = ($V_{SENSEPn}$ – $V_{SENSEMn}$)	●	0		6	V
		Single-Ended Voltage: $V_{SENSEMn}$	●	–0.1		0.1	V
	Current Sense Input Range	Single-Ended Voltage: $I_{SENSEPn}$, $I_{SENSEMn}$	●	–0.1		6	V
		Differential Current Sense Voltage: V_{IN_ADC} = ($I_{SENSEPn}$ – $I_{SENSEMn}$)	●	–170		170	mV
N_ADC	Voltage Sense Resolution	0V ≤ V_{IN_ADC} ≤ 6V, READ_VOUT			122		µV/LSB
	Current Sense Resolution	0mV ≤ |V_{IN_ADC}| < 16mV (Note 5) 16mV ≤ |V_{IN_ADC}| < 32mV 32mV ≤ |V_{IN_ADC}| < 63.9mV 63.9mV ≤ |V_{IN_ADC}| < 127.9mV 127.9mV ≤ |V_{IN_ADC}| IOUT_CAL_GAIN = 1000mΩ			15.625 31.25 62.5 125 250		µA/LSB µA/LSB µA/LSB µA/LSB µA/LSB
TUE_ADC_VOLT_SNS	Total Unadjusted Error (Note 3)	Voltage Sense Inputs V_{IN_ADC} ≥ 1V	●			±0.25	% of Reading
		Voltage Sense Inputs 0 ≤ V_{IN_ADC} ≤ 1V	●			±2.5	mV
TUE_ADC_CURR_SNS	Total Unadjusted Error (Note 3)	Current Sense Inputs 20mV ≤ |V_{IN_ADC}| ≤ 170mV	●			±0.3	% of Reading
		Current Sense Inputs |V_{IN_ADC}| ≤ 20mV	●			±60	µV
V_{OS_ADC}	Offset Error	$I_{SENSEPn}$ and $I_{SENSEMn}$ Inputs, V_{OS} • IOUT_CAL_GAIN, IOUT_CAL_GAIN = 1Ω	●			±35	µV
t_{CONV_ADC}	Conversion Time	$V_{SENSEPn}$, $V_{SENSEMn}$, V_{IN_SNS} Inputs (Note 6)			6.15		ms
		$I_{SENSEPn}$ and $I_{SENSEMn}$ Inputs (Note 6)			24.6		ms
		Internal Temperature (READ_TEMPERATURE_2) (Note 6)			24.6		ms
t_{UPDATE_ADC}	Update Time	(Note 6)			160		ms
C_{IN_ADC}	Input Sampling Capacitance				1		pF
f_{IN_ADC}	Input Sampling Frequency				62.5		kHz

ELECTRICAL CHARACTERISTICS

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SYMBOL	PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
Sense Input Current Characteristics (Note 11)								
I_{IN_VSENSE}	Input Current	$V_{SENSEPn}$ and $V_{SENSEMn}$ Inputs		●			±15	µA
	Differential Input Current	$V_{SENSEPn}$ and $V_{SENSEMn}$ Inputs, V_{IN_DIFF} = 6V		●			±30	µA
I_{IN_ISENSE}	Input Current	$I_{SENSEPn}$ and $I_{SENSEMn}$ Inputs		●			±3	µA
	Differential Input Current	$I_{SENSEPn}$ and $I_{SENSEMn}$ Inputs, $\|V_{IN\_DIFF}\|$ = 170mV		●			±5	µA
DAC Output Characteristics								
N_V_{DAC}	Resolution					10		Bits
V_{FS_VDAC}	Full-Scale Output Voltage (Programmable)	DAC Code = 0x3FF DAC Polarity = 1	Buffer Gain Setting_0 Buffer Gain Setting_1	● ●	1.3 2.5	1.38 2.65	1.44 2.77	V V
INL_V_{DAC}	Integral Nonlinearity	(Note 7)		●			±2	LSB
DNL_V_{DAC}	Differential Nonlinearity	(Note 7)		●			±2.4	LSB
V_{OS_VDAC}	Offset Voltage	(Note 7)		●			±12	mV
V_{DAC}	Load Regulation	V_{DACn} = 2.65V, I_{VDACn} Sourcing = 2mA				100		ppm/mA
		V_{DACn} = 0.1V, I_{VDACn} Sinking = 2mA				100		ppm/mA
	PSRR	DC: 3.13V ≤ V_{DD33} ≤ 3.47V, V_{PWR} = V_{DD33}				60		dB
	Leakage Current	V_{DACn} Hi-Z, 0V ≤ V_{DACn} ≤ 6V		●			±100	nA
	Short-Circuit Current Low	V_{DACn} Shorted to GND		●	–12		–4	mA
	Short-Circuit Current High	V_{DACn} Shorted to V_{DD33}		●	4		12	mA
C_{OUT}	Output Capacitance	V_{DACn} Hi-Z				10		pF
t_{S_VDAC}	DAC Output Update Rate	Fast Servo Mode				250		µs
Voltage Supervisor Characteristics								
V_{IN_VS}	Input Voltage Range (Programmable)	V_{IN_VS} = ($V_{SENSEPn}$ – $V_{SENSEMn}$)	Low Resolution Mode High Resolution Mode	● ●	0 0		6 3.8	V V
		Single-Ended Voltage: $V_{SENSEMn}$		●	–0.1		0.1	V
N_VS	Voltage Sensing Resolution	0V to 3.8V Range: High Resolution Mode				4		mV/LSB
		0V to 6V Range: Low Resolution Mode				8		mV/LSB
TUE_VS	Total Unadjusted Error	2V ≤ V_{IN_VS} ≤ 6V, Low Resolution Mode		●			±1.25	% of Reading
		1.5V < V_{IN_VS} ≤ 3.8V, High Resolution Mode		●			±1.0	% of Reading
		0.8V ≤ V_{IN_VS} ≤ 1.5V, High Resolution Mode		●			±1.5	% of Reading
t_{S_VS}	Update Period					12.21		µs
Current Supervisor Characteristics								
V_{IN_CS}	Current Sense Input Range	Single-Ended Voltage: $I_{SENSEPn}$, $I_{SENSEMn}$		●	–0.1		6	V
		Differential Voltage: V_{IN_CS} = ($I_{SENSEPn}$ – $I_{SENSEMn}$)		●	–170		170	mV
N_CS	Current Sense Resolution	IOUT_OC_FAULT_LIMIT • IOUT_CAL_GAIN IOUT_UC_FAULT_LIMIT • IOUT_CAL_GAIN				400		µV/LSB
TUE_CS	Total Unadjusted Error	50mV ≤ $\|V_{IN\_CS}\|$ ≤ 170mV		●			±3	% of Reading
		$\|V_{IN\_CS}\|$ < 50mV		●			±1.5	mV
V_{OS_CS}	Offset Error	V_{IN_CS} = 0.8mV		●			±600	µV
t_{S_CS}	Update Period					12.21		µs

ELECTRICAL CHARACTERISTICS

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SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN_SNS} Input Characteristics							
V_{IN_SNS}	V_{IN_SNS} Input Voltage Range		●	0		15	V
R_{VIN_SNS}	V_{IN_SNS} Input Resistance		●	70	90	110	kΩ
TUE_{VIN_SNS}	VIN_ON, VIN_OFF Threshold Total Unadjusted Error	3V ≤ V_{IN_SNS} ≤ 8V	●			±2.0	% of Reading
		V_{IN_SNS} > 8V	●			±1.0	% of Reading
	READ_VIN Total Unadjusted Error	3V ≤ V_{IN_SNS} ≤ 8V	●			±1.5	% of Reading
		V_{IN_SNS} > 8V	●			±1.0	% of Reading
DAC Soft-Connect Comparator Characteristics							
V_{OS_CMP}	Offset Voltage	$V_{DACP n}$ = 0.2V	●		±1	±18	mV
		$V_{DACP n}$ = 1.3V	●		±2	±26	mV
		$V_{DACP n}$ = 2.65V	●		±3	±52	mV
External Temperature Sensor Characteristics (READ_TEMPERATURE_1)							
t_{CONV_TSENSE}	Conversion Time	For One Channel, (Total Latency For All Channels Is 4 • 66ms)			66		ms
I_{TSENSE_HI}	T_{SENSE} High Level Current		●	–90	–64	–40	µA
I_{TSENSE_LOW}	T_{SENSE} Low Level Current		●	–5.5	–4	–2.5	µA
TUE_TS	Total Unadjusted Error	Ideal Diode Assumed	●			±3	°C
N_TS	Maximum Ideality Factor	READ_TEMPERATURE_1 = 175°C MFR_TEMP1_GAIN = 1/N_TS				1.10	
Internal Temperature Sensor Characteristics (READ_TEMPERATURE_2)							
TUE_TS2	Total Unadjusted Error				±1		°C
V_{OUT} Enable Output ($V_{OUT\_EN[3:0]}$) Characteristics							
$V_{VOUT\_EN n}$	Output High Voltage	$I_{VOUT\_EN n}$ = –5µA, V_{DD33} = 3.13V	●	10	13	14.7	V
$I_{VOUT\_EN n}$	Output Sourcing Current	$V_{VOUT\_EN n}$ Pull-Up Enabled, $V_{VOUT\_EN n}$ = 1V	●	–5	–7	–9	µA
	Output Sinking Current	Strong Pull-Down Enabled, $V_{VOUT\_EN n}$ = 0.4V	●	3	5	8	mA
		Weak Pull-Down Enabled, $V_{VOUT\_EN n}$ = 0.4V	●	33	50	65	µA
	Output Leakage Current	Internal Pull-Up Disabled, 0V ≤ V_{VOUT_ENn} ≤ 15V	●			±1	µA
V_{VOUT_VALID}	Minimum V_{DD33} when $V_{OUT\_EN n}$ Valid	$V_{VOUT\_EN n}$ ≤ 0.4V	●			1.1	V
General Purpose Output (AUXFAULTB) Characteristics							
$V_{AUXFAULTB}$	Output High Voltage	$I_{AUXFAULTB}$ = –5µA, V_{DD33} = 3.13V	●	10	13	14.7	V
$I_{AUXFAULTB}$	Output Sourcing Current	AUXFAULTB Pull-Up Enabled, $V_{AUXFAULTB}$ = 1V	●	–5	–7	–9	µA
	Output Sinking Current	Strong Pull-Down Enabled, $V_{AUXFAULTB}$ = 0.4V	●	3	5	8	mA
	Output Leakage Current	Internal Pull-Up Disabled, 0V ≤ $V_{AUXFAULTB}$ ≤ 15V	●			±1	µA
EEPROM Characteristics							
Endurance	(Note 8)	0°C < T_J < 85°C During EEPROM Write Operations	●	10,000			Cycles
Retention	(Note 8)	T_J < 105°C	●	10			Years
t_{MASS_WRITE}	Mass Write Operation Time (Note 9)	STORE_USER_ALL, 0°C < T_J < 85°C During EEPROM Write Operations	●		440	4100	ms

ELECTRICAL CHARACTERISTICS

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SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Digital Inputs SCL, SDA, CONTROL0, CONTROL1, CONTROL2, CONTROL3, WDI/RESETB, FAULTB0, FAULTB1, WP							
V_{IH}	High Level Input Voltage	FAULTB0, FAULTB1, SDA, SCL, WDI/RESETB, WP	●	2.1			V
		CONTROL*n*	●	1.85			V
V_{IL}	Low Level Input Voltage	FAULTB0, FAULTB1, SDA, SCL, WDI/RESETB, WP	●			1.5	V
		CONTROL*n*	●			1.6	V
V_{HYST}	Input Hysteresis				20		mV
I_{LEAK}	Input Leakage Current	0V ≤ V_{PIN} ≤ 3.6V	●			±2	µA
t_{SP}	Pulse Width of Spike Suppressed	FAULTB0, FAULTB1, CONTROL*n*			10		µs
		SDA, SCL			98		ns
t_{FAULT_MIN}	Minimum Low Pulse Width for Externally Generated Faults			180			ms
t_{RESETB}	Pulse Width to Assert Reset	$V_{WDI/RESETB}$ ≤ 1.5V	●	300			µs
t_{WDI}	Pulse Width to Reset Watchdog Timer	$V_{WDI/RESETB}$ ≤ 1.5V	●	0.3		200	µs
f_{WDI}	Watchdog Timer Interrupt Input Frequency		●			1	MHz
C_{IN}	Input Capacitance				10		pF
Digital Input SHARE_CLK							
V_{IH}	High Level Input Voltage		●	1.6			V
V_{IL}	Low Level Input Voltage		●			0.8	V
$f_{SHARE\_CLK\_IN}$	Input Frequency Operating Range		●	90		110	kHz
t_{LOW}	Assertion Low Time	V_{SHARE_CLK} < 0.8V	●	0.825		1.11	µs
t_{RISE}	Rise Time	V_{SHARE_CLK} < 0.8V to V_{SHARE_CLK} > 1.6V	●			450	ns
I_{LEAK}	Input Leakage Current	0V ≤ V_{SHARE_CLK} ≤ V_{DD33} + 0.3V	●			±1	µA
C_{IN}	Input Capacitance				10		pF
Digital Outputs SDA, ALERTB, SHARE_CLK, FAULTB0, FAULTB1, PWRGD							
V_{OL}	Digital Output Low Voltage	I_{SINK} = 3mA	●			0.4	V
$f_{SHARE\_CLK\_OUT}$	Output Frequency Operating Range	5.49kΩ Pull-Up to V_{DD33}	●	90	100	110	kHz
Digital Inputs ASEL0,ASEL1							
V_{IH}	Input High Threshold Voltage		●	V_{DD33} – 0.5			V
V_{IL}	Input Low Threshold Voltage		●			0.5	V
$I_{IH,IL}$	High, Low Input Current	ASEL[1:0] = 0, V_{DD33}	●			±95	µA
I_{HIZ}	Hi-Z Input Current		●			±24	µA
C_{IN}	Input Capacitance				10		pF
Serial Bus Timing Characteristics							
f_{SCL}	Serial Clock Frequency (Note 10)		●	10		400	kHz
t_{LOW}	Serial Clock Low Period (Note 10)		●	1.3			µs
t_{HIGH}	Serial Clock High Period (Note 10)		●	0.6			µs
t_{BUF}	Bus Free Time Between Stop and Start (Note 10)		●	1.3			µs
$t_{HD,STA}$	Start Condition Hold Time (Note 10)		●	600			ns
$t_{SU,STA}$	Start Condition Setup Time (Note 10)		●	600			ns

ELECTRICAL CHARACTERISTICS

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SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$t_{SU,STO}$	Stop Condition Setup Time (Note 10)		●	600			ns
$t_{HD,DAT}$	Data Hold Time (LTC2974 Receiving Data) (Note 10)		●	0			ns
	Data Hold Time (LTC2974 Transmitting Data) (Note 10)		●	300		900	ns
$t_{SU,DAT}$	Data Setup Time (Note 10)		●	100			ns
t_{SP}	Pulse Width of Spike Suppressed (Note 10)				98		ns
$t_{TIMEOUT\_BUS}$	Time Allowed to Complete any PMBus Command After Which Time SDA Will Be Released and Command Terminated	Mfr_config_all_longer_pmbus_timeout = 0 Mfr_config_all_longer_pmbus_timeout = 1	● ●		25 200	35 280	ms ms
Additional Digital Timing Characteristics							
t_{OFF_MIN}	Minimum Off Time for Any Channel				100		ms

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All currents into device pins are positive. All currents out of device pins are negative. All voltages are referenced to GND unless otherwise specified. If power is supplied to the chip via the V_{DD33} pin only, connect V_{PWR} and V_{DD33} pins together.

Note 3: The ADC total unadjusted error includes all error sources. First, a two-point analog trim is performed to achieve a flat reference voltage (V_{REF}) over temperature. This results in minimal temperature coefficient, but the absolute voltage can still vary. To compensate for this, a high-resolution, drift-free, and noiseless digital trim is applied at the output of the ADC, resulting in a very high accuracy measurement.

Note 4: Hysteresis in the output voltage is created by package stress that differs depending on whether IC was previously at a higher or lower temperature. Output voltage is always measured at 25°C, but the IC is cycled to 105°C or –40°C before successive measurements. Hysteresis is roughly proportional to the square of the temperature change.

Note 5: The current sense resolution is determined by the L11 format, the value of IOUT_CAL_GAIN, and the magnitude of the current being measured. See Table 2 for details.

Note 6: The nominal time between successive ADC conversions (latency of the ADC) for any given channel is t_{UPDATE_ADC}.

Note 7: Nonlinearity is defined from the first code that is greater than or equal to the maximum offset specification to full-scale code, 1023.

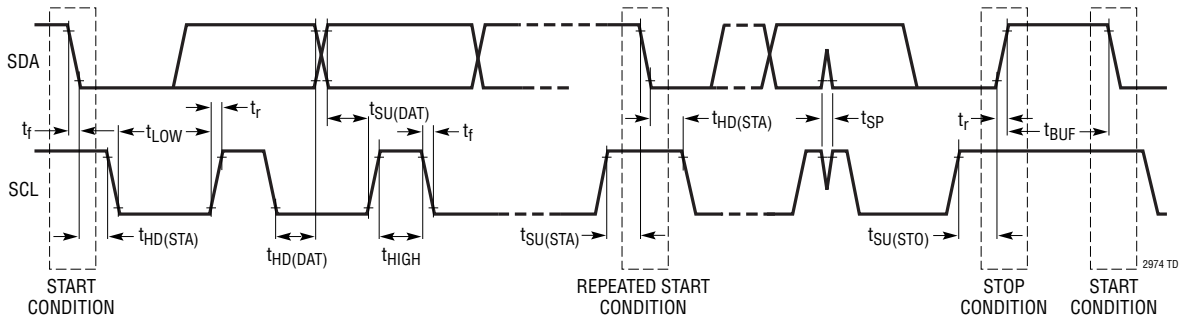
Note 8: EEPROM endurance and retention are guaranteed by design, characterization and correlation with statistical process controls. The minimum retention specification applies for devices whose EEPROM has been cycled less than the minimum endurance specification.

Note 9: The LTC2974 will not acknowledge any PMBus commands, except for MFR_COMMON, when a STORE_USER_ALL command is being executed. See also OPERATION section.

Note 10: Maximum capacitive load, C_B, for SCL and SDA is 400pF. Data and clock risetime (t_r) and falltime (t_f) are: (20 + 0.1• C_B) (ns) < t_r < 300ns and (20 + 0.1 • C_B) (ns) < t_f < 300ns. C_B = capacitance of one bus line in pF. SCL and SDA external pull-up voltage, V_{IO}, is 3.13V < V_{IO} < 3.6V.

Note 11: V_{SENSE} and I_{SENSE} input currents are characterized by input current and input differential current. Input current is defined as current into a single device pin (see Note 2). Input differential current is defined as ($I^+ – I^–$) where I^+ is the current into the positive device pin and $I^–$ is the current into the negative device pin.

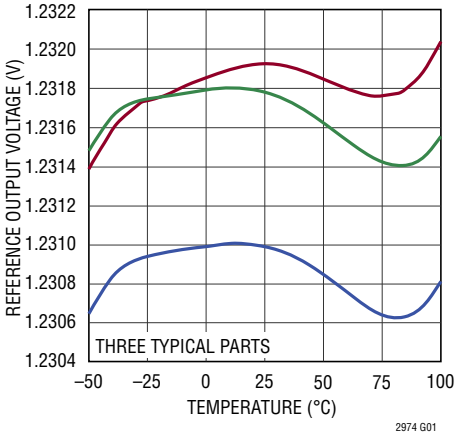
PMBUS TIMING DIAGRAM



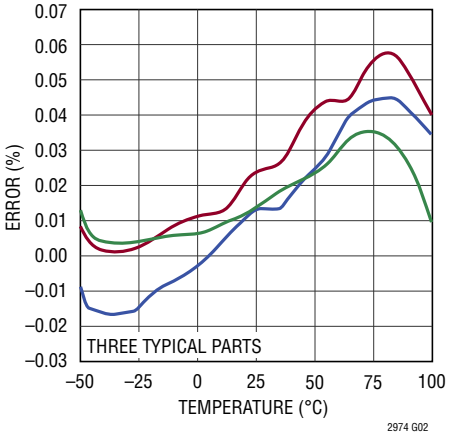
Rev. E

TYPICAL PERFORMANCE CHARACTERISTICS

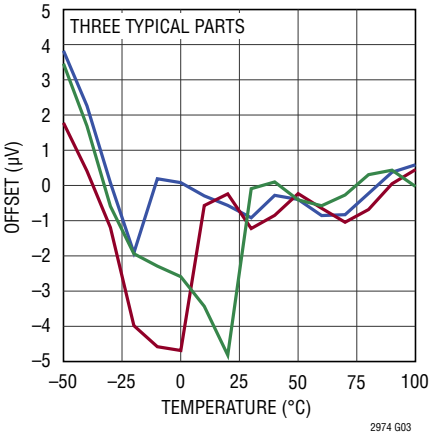
Reference Voltage vs Temperature



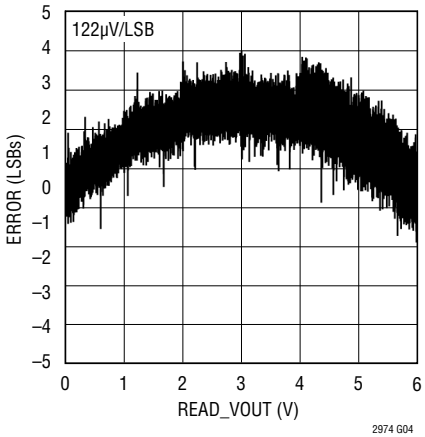
ADC READ_VOUT Total Unadjusted Error vs Temperature



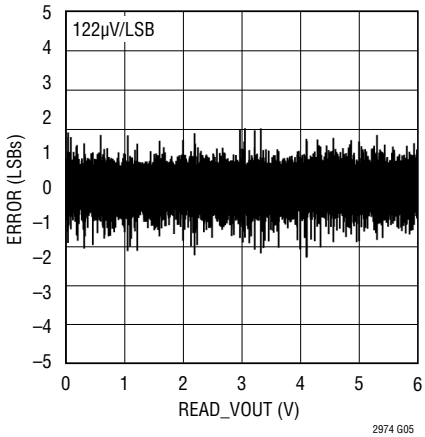
ADC READ_IOUT Input Referred Offset Voltage vs Temperature



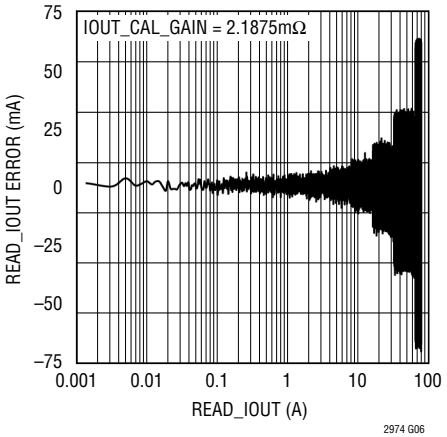
ADC READ_VOUT-INL



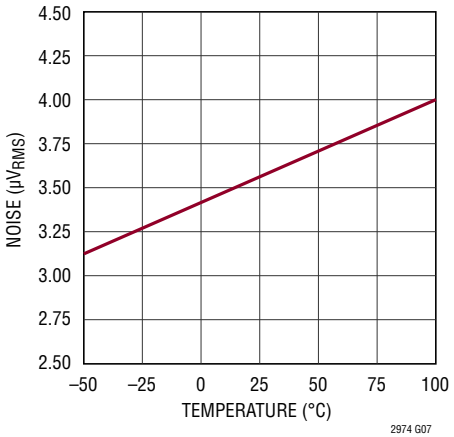
ADC READ_VOUT-DNL



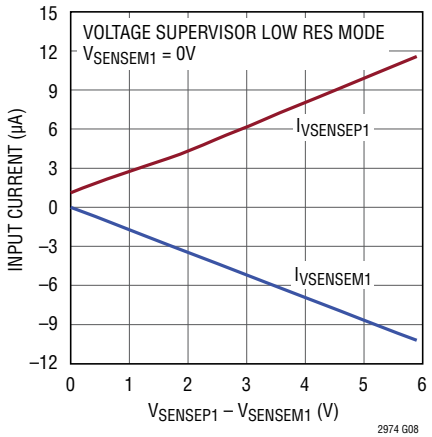
ADC READ_IOUT Error vs READ_IOUT



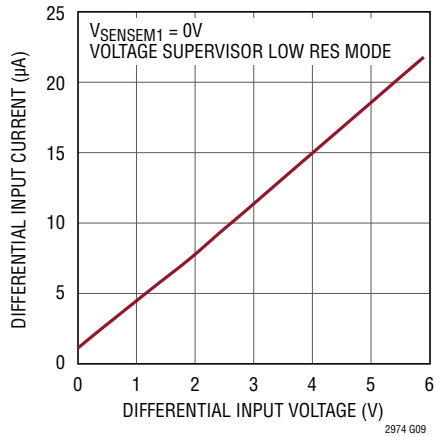
ADC READ_IOUT Input Referred Noise vs Temperature



Voltage Sense Input Currents vs Differential Input Voltage



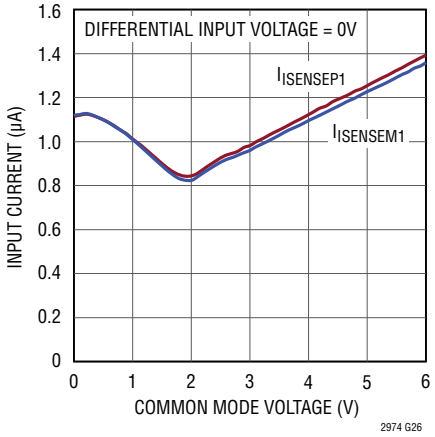
Voltage Sense Differential Input Current vs Differential Input Voltage



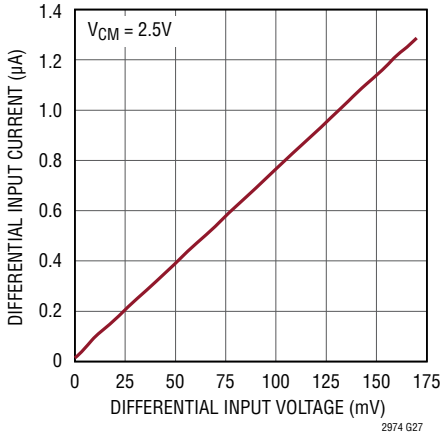
Rev. E

TYPICAL PERFORMANCE CHARACTERISTICS

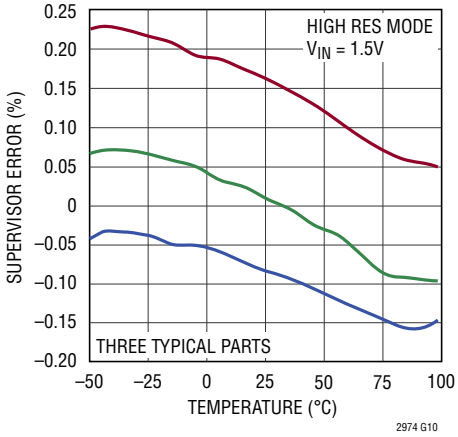
Current Sense Input Current vs Common Mode Voltage



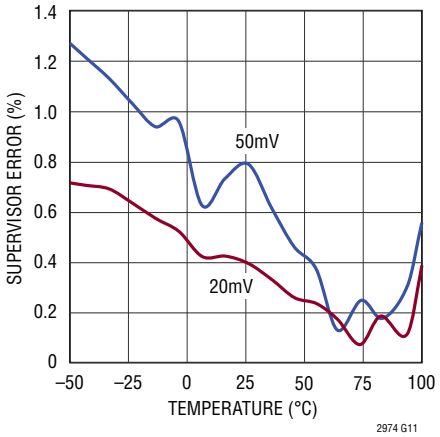
Current Sense Differential Input Current vs Differential Input Voltage



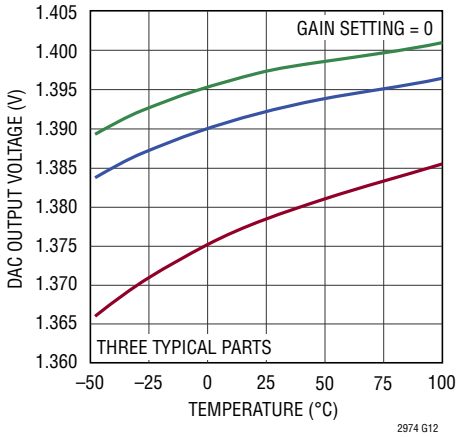
Voltage Supervisor Total Unadjusted Error vs Temperature



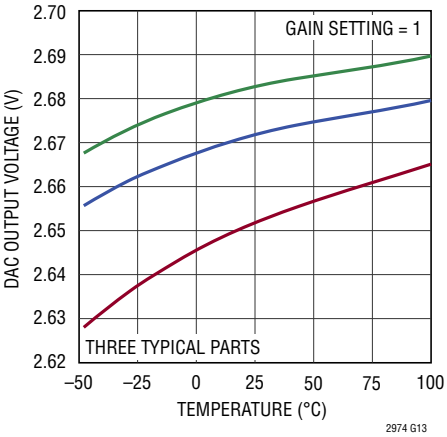
Current Supervisor Total Unadjusted Error vs Temperature



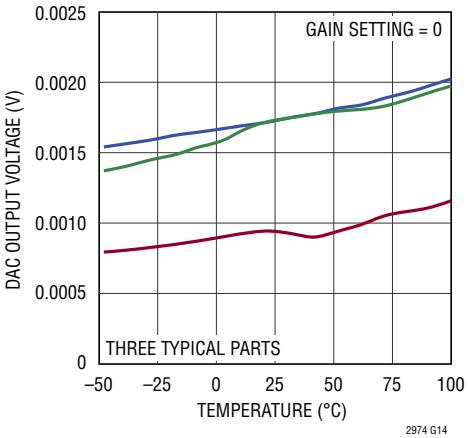
DAC Full-Scale Voltage vs Temperature, Gain Setting = 0



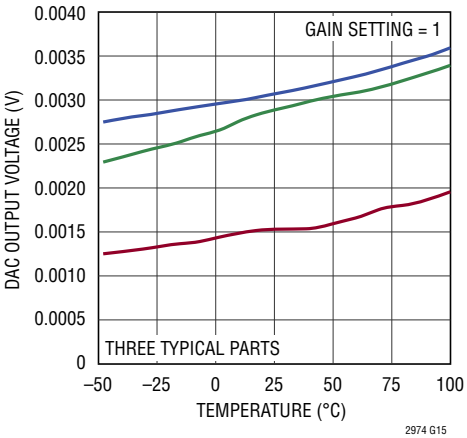
DAC Full-Scale Voltage vs Temperature, Gain Setting = 1



DAC Offset Voltage vs Temperature, Gain Setting = 0

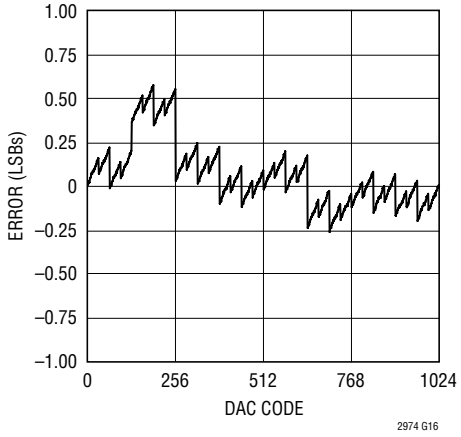


DAC Offset Voltage vs Temperature, Gain Setting = 1

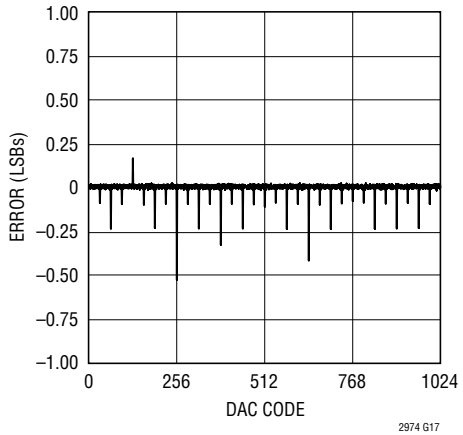


TYPICAL PERFORMANCE CHARACTERISTICS

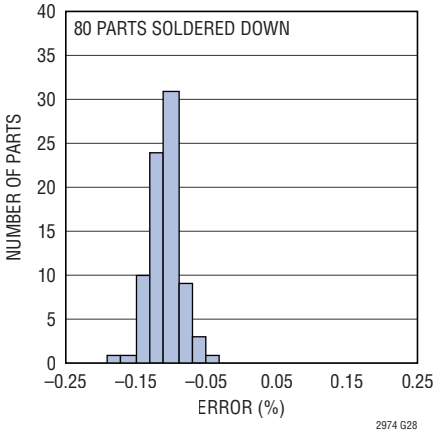
DAC-INL



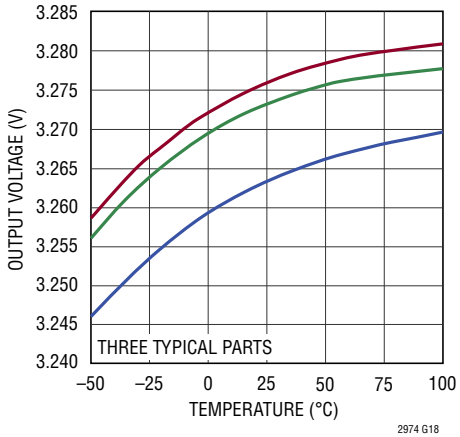
DAC-DNL



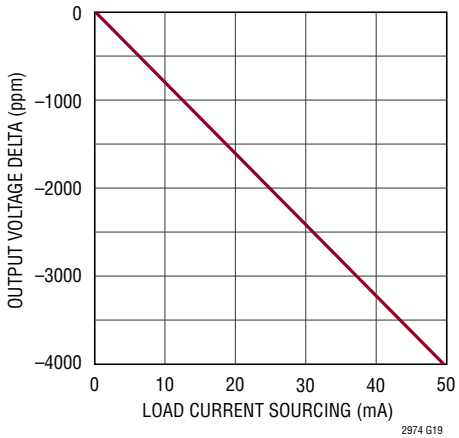
Closed-Loop Servo Error



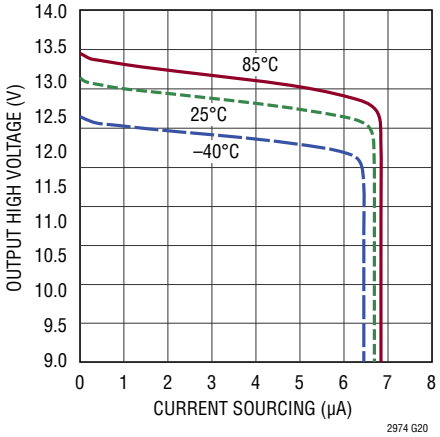
V_{DD33} Regulator Output Voltage vs Temperature



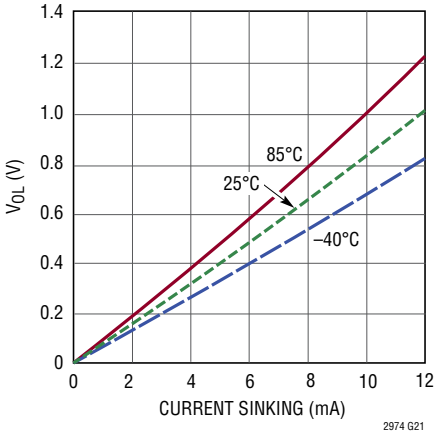
V_{DD33} Regulator Load Regulation



V_{VOUT_ENn} and $V_{AUXFAULTB}$ Output V_{OH} vs Current Sourcing

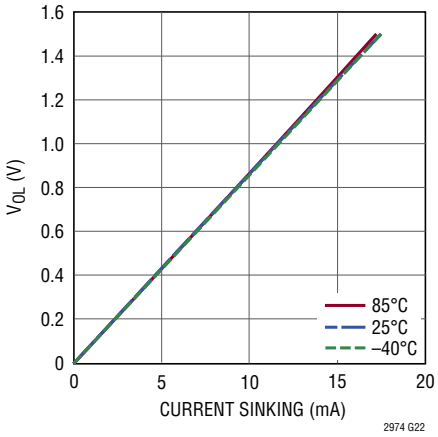


V_{VOUT_ENn} and $V_{AUXFAULTB}$ Output V_{OL} vs Current Sinking

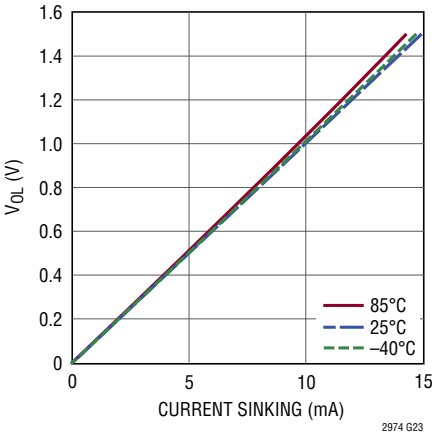


TYPICAL PERFORMANCE CHARACTERISTICS

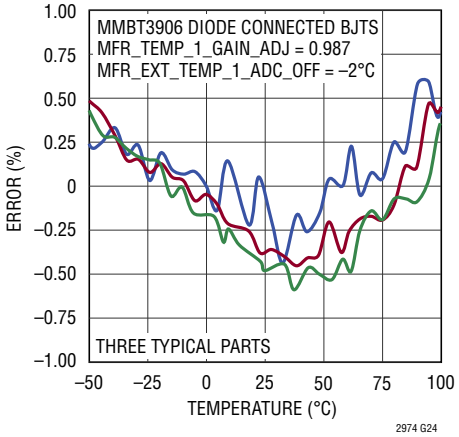
PWRGD and FAULTB*n* V_{OL} vs Current Sinking



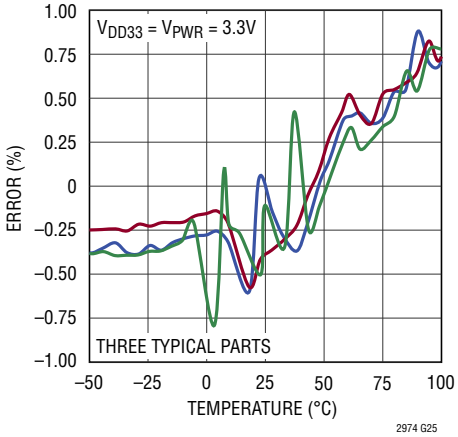
ALERTB V_{OL} vs Current Sinking



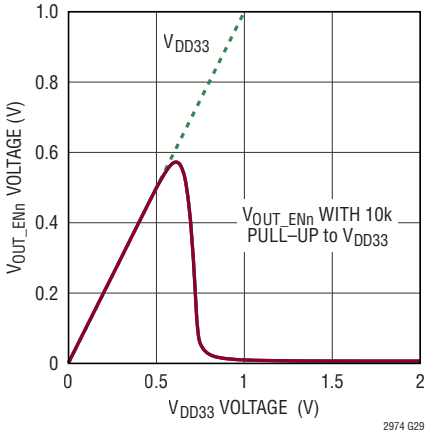
External Temperature READ_ TEMPERATURE_1 Error vs Temperature



READ_TEMPERATURE_2 Error vs Temperature



$V_{OUT\_EN[3:0]}$ Output Voltage vs V_{DD33}



PIN FUNCTIONS

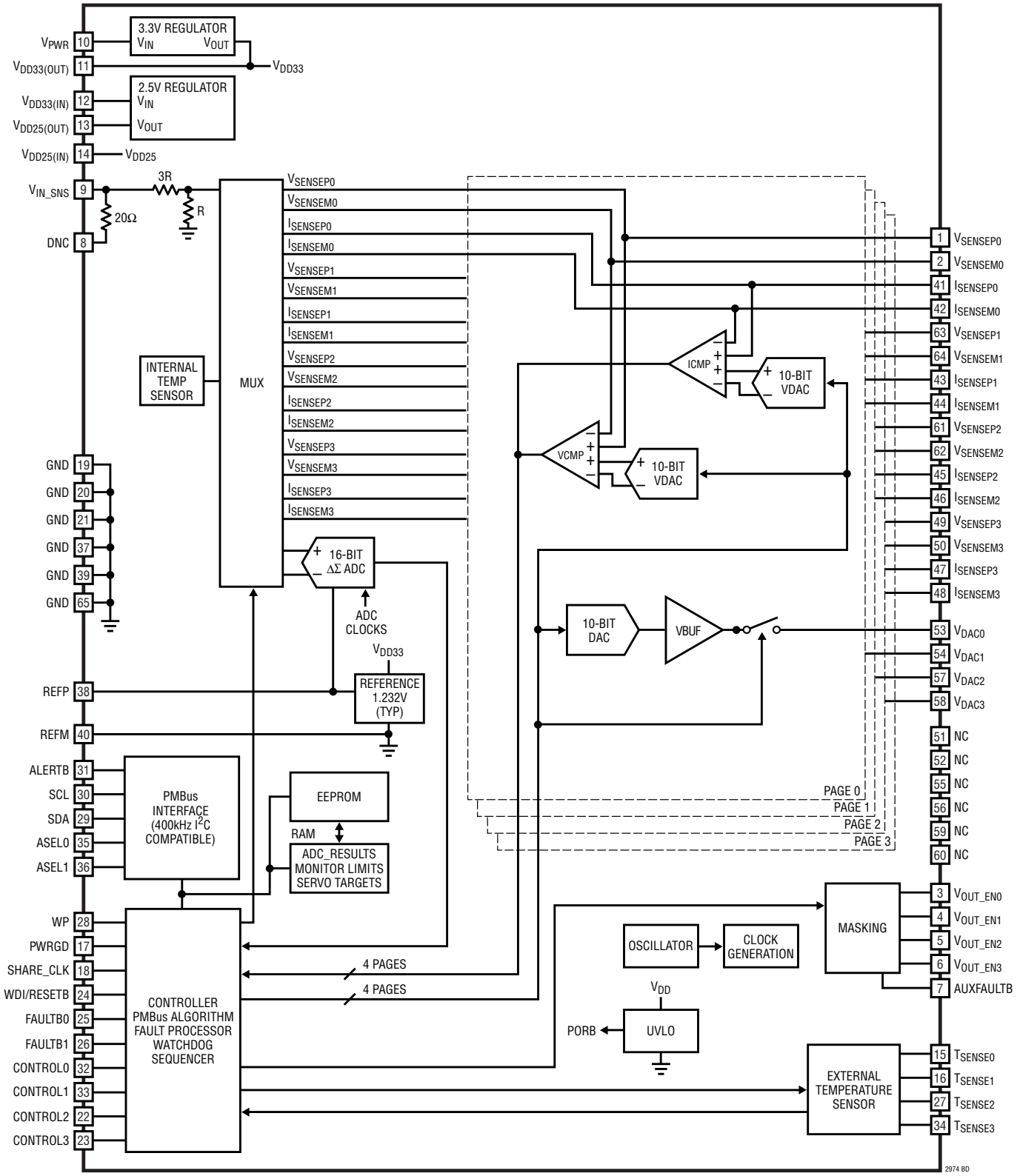
PIN NAME	PIN NUMBER	PIN TYPE	DESCRIPTION
$V_{SENSEP0}$	1*	In	DC/DC Converter Differential (+) Output Voltage-0 Sensing Pin
$V_{SENSEM0}$	2*	In	DC/DC Converter Differential (–) Output Voltage-0 Sensing Pin
V_{OUT_EN0}	3	Out	DC/DC Converter Enable-0 Pin. Output High Voltage Optionally Pulled-Up to 12V by 5µA
V_{OUT_EN1}	4	Out	DC/DC Converter Enable-1 Pin. Output High Voltage Optionally Pulled-Up to 12V by 5µA
V_{OUT_EN2}	5	Out	DC/DC Converter Enable-2 Pin. Output High Voltage Optionally Pulled-Up to 12V by 5µA
V_{OUT_EN3}	6	Out	DC/DC Converter Enable-3 Pin. Output High Voltage Optionally Pulled-Up to 12V by 5µA
AUXFAULTB	7	Out	Auxillary Fault Output Pin. Output High Voltage Optionally Pulled-Up to 12V by 5µA. Can Be Configured to Pull Low When OV/OC/UC Detected
DNC	8	Do Not Connect	Do Not Connect to this Pin
V_{IN_SNS}	9	In	V_{IN} SENSE Input. This Voltage is Compared Against the V_{IN} On and Off Voltage Thresholds In Order to Determine When to Enable and Disable, Respectively, the Downstream DC/DC Converters
V_{PWR}	10	In	V_{PWR} Serves as the Unregulated Power Supply Input to the Chip (4.5 to 15V). If a 4.5V to 15V Supply Voltage Is Unavailable, Short V_{PWR} to V_{DD33} and Power the Chip Directly from a 3.3V Supply. Bypass to GND with 0.1µF Capacitor.
V_{DD33}	11	In/Out	If Shorted to V_{PWR}, It Serves as 3.13 to 3.47V Supply Input Pin. Otherwise It Is a 3.3V Internally Regulated Voltage Output (Use 0.1µF Decoupling Capacitor to GND). If Using the Internal Regulator to Provide V_{DD33}, Do Not Connect to V_{DD33} Pins of Any Other Devices
V_{DD33}	12	In	Input for Internal 2.5V Sub-Regulator. Short this Pin to Pin 11. If Using the Internal Regulator to Provide V_{DD33}, Do Not Connect to V_{DD33} Pins of Any Other Devices
V_{DD25}	13	In/Out	2.5V Internally Regulated Voltage Output. Bypass to GND with a 0.1µF Capacitor. Do Not Connect to V_{DD25} Pins of Any Other Devices
V_{DD25}	14	In	2.5V Supply Voltage Input. Short this Pin to Pin 13. Do Not Connect to V_{DD25} Pins of Any Other Devices
T_{SENSE0}	15*	In/Out	External Temperature Current Output and Voltage Input for Channel 0. Maximum allowed capacitance is 1µF
T_{SENSE1}	16*	In/Out	External Temperature Current Output and Voltage Input for Channel 1. Maximum allowed capacitance is 1µF
PWRGD	17	Out	Power-Good Open Drain Output. Indicates When Selected Outputs Are Power Good. Can be Used as System Power-on Reset
SHARE_CLK	18	In/Out	Bidirectional Clock Sharing Pin. Connect a 5.49kΩ Pull-Up Resistor to V_{DD33}. Connect to All Other SHARE_CLK Pins in the System
GND	19	Ground	Chip Ground. Must Be Soldered to PCB
GND	20	Ground	Chip Ground. Must Be Soldered to PCB
GND	21	Ground	Chip Ground. Must Be Soldered to PCB
CONTROL2	22	In	Control Pin 2 Input
CONTROL3	23	In	Control Pin 3 Input
WDI/RESETB	24	In	Watchdog Timer Interrupt and Chip Reset Input. Connect a 10kΩ Pull-Up Resistor to V_{DD33}. Rising Edge Resets Watchdog Counter. Holding this Pin Low for More than t_{RESETB} Resets the Chip
FAULTB0	25	In/Out	Open-Drain Output and Digital Input. Active Low Bidirectional Fault Indicator-0. Connect a 10kΩ Pull-Up Resistor to V_{DD33}
FAULTB1	26	In/Out	Open-Drain Output and Digital Input. Active Low Bidirectional Fault Indicator-1. Connect a 10kΩ Pull-Up Resistor to V_{DD33}
T_{SENSE2}	27*	In/Out	External Temperature Current Output and Voltage Input for Channel 2. Maximum allowed capacitance is 1µF
WP	28	In	Digital Input. Write-Protect Input Pin, Active High
SDA	29	In/Out	PMBus Bidirectional Serial Data Pin
SCL	30	In	PMBus Serial Clock Input Pin (400kHz Maximum)

PIN FUNCTIONS

PIN NAME	PIN NUMBER	PIN TYPE	DESCRIPTION
ALERTB	31	Out	Open-Drain Output. Generates an Interrupt Request in a Fault/Warning Situation
CONTROL0	32	In	Control Pin 0 Input
CONTROL1	33	In	Control Pin 1 Input
T_{SENSE3}	34*	In/Out	External Temperature Current Output and Voltage Input for Channel 3. Maximum allowed capacitance is 1µF
ASEL0	35	In	Ternary Address Select Pin 0 Input. Connect to V_{DD33}, GND or Float to Encode 1 of 3 Logic States
ASEL1	36	In	Ternary Address Select Pin 1 Input. Connect to V_{DD33}, GND or Float to Encode 1 of 3 Logic States
GND	37	Ground	Chip Ground. Must Be Soldered to PCB
REFP	38	Out	Reference Voltage Output. Needs 0.1µF Decoupling Capacitor to REFM
GND	39	Ground	Chip Ground. Must Be Soldered to PCB
REFM	40	Out	Reference Return Pin. Needs 0.1µF Decoupling Capacitor to REFP
$I_{SENSEP0}$	41*	In	DC/DC Converter Differential (+) Output Current-0 Sensing Pin
$I_{SENSEM0}$	42*	In	DC/DC Converter Differential (–) Output Current-0 Sensing Pin
$I_{SENSEP1}$	43*	In	DC/DC Converter Differential (+) Output Current-1 Sensing Pin
$I_{SENSEM1}$	44*	In	DC/DC Converter Differential (–) Output Current-1 Sensing Pin
$I_{SENSEP2}$	45*	In	DC/DC Converter Differential (+) Output Current-2 Sensing Pin
$I_{SENSEM2}$	46*	In	DC/DC Converter Differential (–) Output Current-2 Sensing Pin
$I_{SENSEP3}$	47*	In	DC/DC Converter Differential (+) Output Current-3 Sensing Pin
$I_{SENSEM3}$	48*	In	DC/DC Converter Differential (–) Output Current-3 Sensing Pin
$V_{SENSEP3}$	49*	In	DC/DC Converter Differential (+) Output Voltage-3 Sensing Pin
$V_{SENSEM3}$	50*	In	DC/DC Converter Differential (–) Output Voltage-3 Sensing Pin
NC	51	No Connect	No Connect
NC	52	No Connect	No Connect
V_{DAC0}	53	Out	DAC0 Output
V_{DAC1}	54	Out	DAC1 Output
NC	55	No Connect	No Connect
NC	56	No Connect	No Connect
V_{DAC2}	57	Out	DAC2 Output
V_{DAC3}	58	Out	DAC3 Output
NC	59	No Connect	No Connect
NC	60	No Connect	No Connect
$V_{SENSEP2}$	61*	In	DC/DC Converter Differential (+) Output Voltage-2 Sensing Pin
$V_{SENSEM2}$	62*	In	DC/DC Converter Differential (–) Output Voltage-2 Sensing Pin
$V_{SENSEP1}$	63*	In	DC/DC Converter Differential (+) Output Voltage-1 Sensing Pin
$V_{SENSEM1}$	64*	In	DC/DC Converter Differential (–) Output Voltage-1 Sensing Pin
GND	65	Ground	Exposed Pad. Must Be Soldered to PCB

*Any unused $V_{SENSEPn}$/$I_{SENSEPn}$, $V_{SENSEMn}$/$I_{SENSEMn}$ or T_{SENSEn} pins should be tied to GND. Refer to Unused ADC Sense Inputs in the Applications Information section.

BLOCK DIAGRAM



See Figure 31 for a Typical Application with a Simplified Block Diagram

OPERATION

LTC2974 OPERATION OVERVIEW

The LTC2974 is a PMBus programmable power supply controller, monitor, sequencer and voltage and current supervisor that can perform the following operations:

- Accept PMBus compatible programming commands.
- Provide DC/DC converter input voltage, output voltage, output current, output temperature, and internal junction temperature readback through the PMBus interface.
- Control the output of DC/DC converters that set the output voltage with a trim pin or DC/DC converters that set the output voltage using an external resistor feedback network.
- Sequence the startup of DC/DC converters via PMBus programming and the CONTROL input pins. The LTC 2974 supports time-based sequencing and tracking sequencing. Cascade sequence on with time based sequence off is also supported.
- Trim the DC/DC converter output voltage (typically in 0.02% steps), in closed-loop servo operating mode, autonomously or through PMBus programming.
- Margin the DC/DC converter output voltage to PMBus programmed limits.
- Trim or margin the DC/DC converter output voltage with direct access to the margin DAC.
- Supervise the DC/DC converter input voltage, output voltage, load current and the inductor temperatures for overvalue/undervalue conditions with respect to PMBus programmed limits and generate appropriate faults and warnings.
- Accurately handle inductor self-heating transients using a proprietary algorithm. These self-heating effects are combined with external temperature sensor readings to improve accuracy of current supervisors and ADC current measurement.
- Respond to a fault condition by continuing operation indefinitely, latching-off after a programmable deglitch period, latching-off immediately or sequencing off after TOFF_DELAY. Use retry mode to automatically recover from a latched-off condition. With retry enabled, MFR_RETRY_COUNT programs the number of retries (0 to 6 or infinite) for all pages.
- Optionally stop trimming the DC/DC converter output voltage after it reaches the initial margin or nominal target. Optionally allow servo to resume if target drifts outside of V_{OUT} warning limits.
- Store command register contents to EEPROM with CRC and ECC through PMBus programming.
- Restore EEPROM contents through PMBus programming or when V_{DD33} is applied on power-up.
- Report the DC/DC converter output voltage status through the power good output.
- Generate interrupt requests by asserting the ALERTB pin in response to supported PMBus faults and warnings.
- Coordinate system wide fault responses for all DC/DC converters connected to the LTC2974 FAULTB0 and FAULTB1 pins.
- Synchronize sequencing delays or shutdown for multiple devices using the SHARE_CLK pin.
- Software and hardware write protect the command registers.
- Disable the input voltage to the supervised DC/DC converters in response to output OV, UV, OC and UC faults.
- Log telemetry and status data to EEPROM in response to a faulted-off condition.
- Supervise an external microcontroller's activity for a stalled condition with a programmable watchdog timer and reset it if necessary.
- Prevent a DC/DC converter from re-entering the on state after a power cycle until a programmable interval (MFR_RESTART_DELAY) has elapsed and its output has decayed below a programmable threshold voltage (MFR_VOUT_DISCHARGE_THRESHOLD).
- Record minimum and maximum observed values of input voltage, output voltages, output currents and output temperatures.
- Access user EEPROM data directly, without altering RAM space (Mfr_ee_unlock, Mfr_ee_erase, and Mfr_ee_data). Facilitates in-house bulk programming.
- Accommodate multiple hosts with Command Plus

OPERATION

EEPROM

The LTC2974 contains internal EEPROM (Non-Volatile Memory) with error-correcting code (ECC) to store configuration settings and fault log information. EEPROM endurance, retention and mass write operation time are specified over the operating temperature range. See Electrical Characteristics and Absolute Maximum Ratings sections.

Non destructive operation above T_J = 105°C is possible although the Electrical Characteristics are not guaranteed and the EEPROM will be degraded.

Operating the EEPROM above 105°C may result in a degradation of retention characteristics. The fault logging function, which is useful in debugging system problems that may occur at high temperatures, only writes to fault log EEPROM locations. If occasional writes to these registers occur above 105°C, a slight degradation in the data retention characteristics of the fault log may occur.

It is recommended that the EEPROM not be written using STORE_USER_ALL or bulk programming when T_J > 85°C.

The degradation in EEPROM retention for temperatures >105°C can be approximated by calculating the dimensionless acceleration factor using the following equation.

$$AF = e^{\left[\left(\frac{Ea}{k}\right)\bullet\left(\frac{1}{T_{USE}+273}-\frac{1}{T_{STRESS}+273}\right)\right]}$$

Where:

AF = acceleration factor

Ea = activation energy = 1.4eV

k = 8.617 • 10^{-5}eV/°K

T_{USE} = 105°C specified junction temperature

T_{STRESS} = actual junction temperature °C

Example: Calculate the effect on retention when operating at a junction temperature of 125°C for 10 hours.

T_{STRESS} = 125°C

T_{USE} = 105°C

AF = 8.65

Equivalent operating time at 105°C = 86.5 hours.

So the overall rentention of the EEPROM was degraded by an additional 76.5 hours as a result of operation at a junction temperature of 125°C for 10 hours. Note that the effect of this overstress is negligible when compared to the overall EEPROM rentention rating of 87,600 hours at a maximum junction temperature of 105°C.

AUXFAULTB

The AUXFAULTB pin can be configured to indicate when some fault conditions have been detected. See Figure 1 for a conceptual view of this multiplexing.

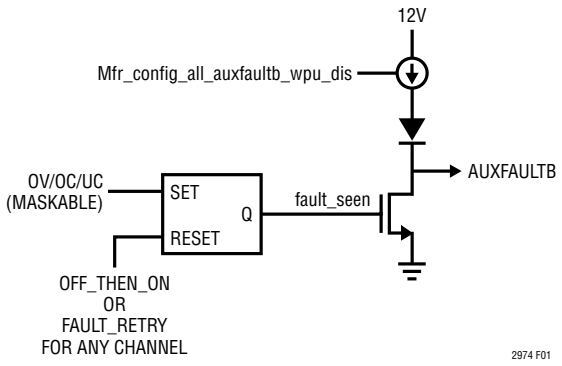


Figure 1. AUXFAULTB MUX

The MFR_CONFIG2_LTC2974 and MFR_CONFIG3_LTC2974 commands can be used on a per channel basis to select which, if any, fault conditions will cause the AUXFAULTB pin to be driven low. The only fault types which can be propagated to the AUXFAULTB pin are overvoltage faults and overcurrent/undercurrent faults.

Mfr_config_all_auxfaultb_wpu selects whether the AUXFAULTB pin is in the hi-Z state, or weakly pulled-up to approximately 12V, using a 5µA current. As shown in Figure 1, the pulldown to GND overrides if any enabled faults are detected.

OPERATION

RESETB

Holding the WDI/RESETB pin low for more than t_{RESETB} will cause the LTC2974 to enter the power-on reset state. While in the power-on reset state, the device will not communicate on the I^2C bus. Following the subsequent rising-edge of the WDI/RESETB pin, the LTC2974 will execute its power-on sequence per the user configuration stored in EEPROM. Connect WDI/RESETB to V_{DD33} with a 10k resistor. WDI/RESETB includes an internal 256µs deglitch filter so additional filter capacitance on this pin is not recommended.

PMBus SERIAL DIGITAL INTERFACE

The LTC2974 communicates with a host (master) using the standard PMBus serial bus interface. The PMBus Timing Diagram shows the timing relationship of the signals on the bus. The two bus lines, SDA and SCL, must be high when the bus is not in use. External pull-up resistors or current sources are required on these lines.

The LTC2974 is a slave device. The master can communicate with the LTC2974 using the following formats:

- Master transmitter, slave receiver
- Master receiver, slave transmitter

The following SMBus commands are supported:

- Write Byte, Write Word, Send Byte
- Read Byte, Read Word, Block Read
- Alert Response Address

Figures 1 to 12 illustrate the aforementioned SMBus protocols. All transactions support PEC (packet error check) and GCP (group command protocol). The Block Read supports 255 bytes of returned data. For this reason, the SMBus timeout may be extended using the Mfr_config_all_longer_pmbus_timeout setting.

PMBus

PMBus is an industry standard that defines a means of communication with power conversion devices. It is comprised of an industry standard SMBus serial interface and the PMBus command language.

The PMBus two wire interface is an incremental extension of the SMBus. SMBus is built upon I^2C with some minor differences in timing, DC parameters and protocol. The SMBus protocols are more robust than simple I^2C byte commands because they provide timeouts to prevent bus hangs and optional Packet Error Checking (PEC) to ensure data integrity. In general, a master device that can be configured for I^2C communication can be used for PMBus communication with little or no change to hardware or firmware.

For a description of the minor extensions and exceptions PMBus makes to SMBus, refer to PMBus Specification Part 1 Revision 1.1: Section 5: Transport. This can be found at:

www.pmbus.org

For a description of the differences between SMBus and I^2C, refer to System Management Bus (SMBus) Specification Version 2.0: Appendix B – Differences between SMBus and I^2C. This can be found at:

www.smbus.org

When using an I^2C controller to communicate with a PMBus part it is important that the controller be able to write a byte of data without generating a stop. This will allow the controller to properly form the repeated start of a PMBus read command by concatenating a start command byte write with an I^2C read.

Device Address

The I^2C/SMBus address of the LTC2974 equals the base address + N where N is a number from 0 to 8. N can be configured by setting the ASEL0 and ASEL1 pins to V_{DD33}, GND or FLOAT. See Table 1. Using one base address and the nine values of N, nine LTC2974s can be connected together to control thirty six outputs. The base address is stored in the MFR_I2C_BASE_ADDRESS register. The base address can be written to any value, but generally should not be changed unless the desired range of addresses overlap existing addresses. Watch that the address range does not overlap with other I^2C/SMBus device or global addresses, including I^2C/SMBus multiplexers and bus buffers. This will bring you great happiness.

OPERATION

The LTC2974 always responds to its global address and the SMBus Alert Response address regardless of the state of its ASEL pins and the MFR_I2C_BASE_ADDRESS register.

Processing Commands

The LTC2974 uses a dedicated processing block to ensure quick response to all of its commands. There are a few exceptions where the part will NACK a subsequent command because it is still processing the previous command. These are summarized in the following tables. MFR_COMMON is a special command that may always be read even when the part is busy. This provides an alternate method for a host to determine if the LTC2974 is busy.

EEPROM Related Commands

COMMAND	TYPICAL DELAY*	COMMENT
STORE_USER_ALL	t_{MASS_WRITE}	See Electrical Characterization table. The LTC2974 will not accept any commands while it is transferring register contents to the EEPROM. The command byte will be NACKed. MFR_COMMON may always be read.
RESTORE_USER_ALL	30ms	The LTC2974 will not accept any commands while it is transferring EEPROM data to command registers. The command byte will be NACKed. MFR_COMMON may always be read.
MFR_FAULT_LOG_CLEAR	175ms	The LTC2974 will not accept any commands while it is initializing the fault log EEPROM space. The command byte will be NACKed. MFR_COMMON may always be read.
MFR_FAULT_LOG_STORE	20ms	The LTC2974 will not accept any commands while it is transferring fault log RAM buffer to EEPROM space. The command byte will be NACKed. MFR_COMMON may always be read.
Internal Fault log	20ms	An internal fault log event is a one time event that uploads the contents of the fault log to EEPROM in response to a fault. Internal fault logging may be disabled. Commands received during this EEPROM write are NACKed. MFR_COMMON may always be read.
MFR_FAULT_LOG_RESTORE	2ms	The LTC2974 will not accept any commands while it is transferring EEPROM data to the fault log RAM buffer. The command byte will be NACKed. MFR_COMMON may always be read.

*The typical delay is measured from the command's stop to the next command's start.

Other Commands

COMMAND	DELAY*	COMMENT
MFR_CONFIG	<50µs	The LTC2974 will not accept any commands while it is completing this command. The command byte will be NACKed. MFR_COMMON may always be read.
IOUT_CAL_GAIN	<500µs	The LTC2974 will not accept any commands while it is completing this command. The command byte will be NACKed. MFR_COMMON may always be read.

*The typical delay is measured from the command's stop to the next command's start.

Other PMBus Timing Notes

COMMAND	COMMENT
CLEAR_FAULTS	The LTC2974 will accept commands while it is completing this command but the affected status flags will not be cleared for up to 500µs.

OPERATION

Table 1. LTC2974 Address Look-Up Table with MFR_I2C_BASE_ADDRESS Set to 7bit 0x5C

ADDRESS PINS		DESCRIPTION	HEX DEVICE ADDRESS		BINARY DEVICE ADDRESS							
ASEL1	ASEL0		7-Bit	8-Bit	6	5	4	3	2	1	0	R/W
X	X	Alert Response	0C	19	0	0	0	1	1	0	0	1
X	X	Global	5B	B6	1	0	1	1	0	1	1	0
L	L	N = 0	5C*	B8	1	0	1	1	1	0	0	0
L	NC	N = 1	5D	BA	1	0	1	1	1	0	1	0
L	H	N = 2	5E	BC	1	0	1	1	1	1	0	0
NC	L	N = 3	5F	BE	1	0	1	1	1	1	1	0
NC	NC	N = 4	60	C0	1	1	0	0	0	0	0	0
NC	H	N = 5	61	C2	1	1	0	0	0	0	1	0
H	L	N = 6	62	C4	1	1	0	0	0	1	0	0
H	NC	N = 7	63	C6	1	1	0	0	0	1	1	0
H	H	N = 8	64	C8	1	1	0	0	1	0	0	0

H = Tie to V_{DD33}, NC = No Connect = Open or Float, L = Tie to GND, X = Don't Care
*MFR_I2C_BASE_ADDRESS = 7bit 0x5C (Factory Default)

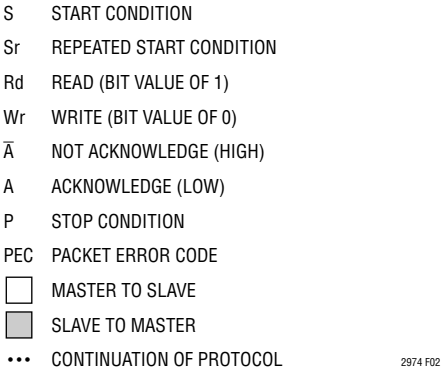


Figure 2. PMBus Packet Protocol Diagram Element Key

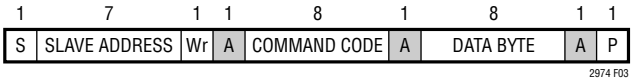


Figure 3. Write Byte Protocol

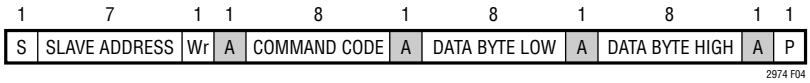


Figure 4. Write Word Protocol

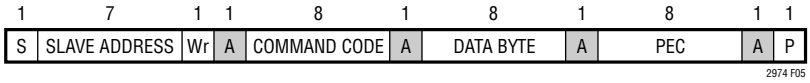


Figure 5. Write Byte Protocol with PEC

OPERATION

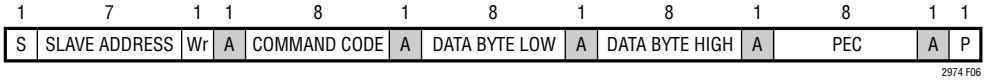


Figure 6. Write Word Protocol with PEC

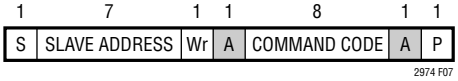


Figure 7. Send Byte Protocol

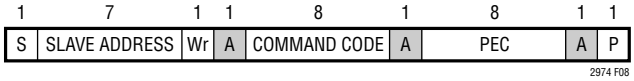


Figure 8. Send Byte Protocol with PEC

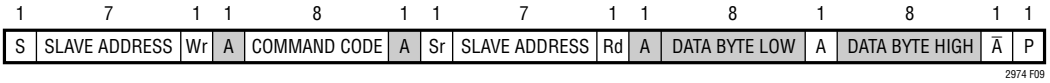


Figure 9. Read Word Protocol

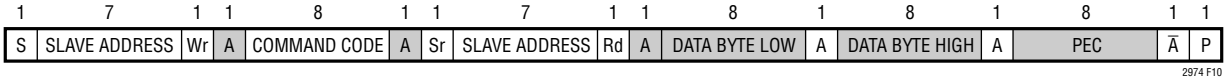


Figure 10. Read Word Protocol with PEC

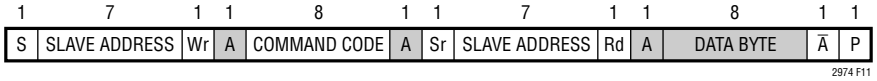


Figure 11. Read Byte Protocol

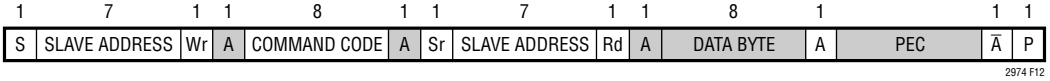


Figure 12. Read Byte Protocol with PEC

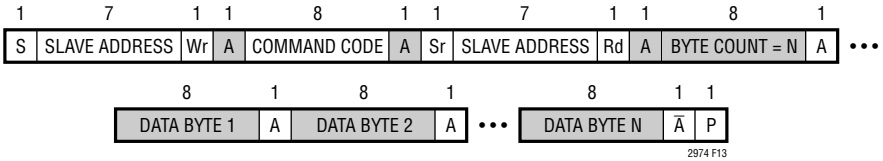


Figure 13. Block Read

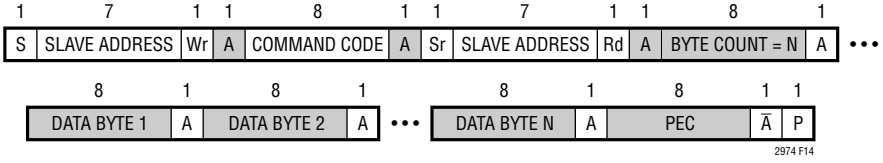


Figure 14. Block Read with PEC

PMBUS COMMAND SUMMARY

Summary Table

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	EEPROM	DEFAULT VALUE: FLOAT HEX	REF PAGE
PAGE	0x00	Channel or page currently selected for any command that supports paging.	R/W Byte	N	Reg			0x00	29
OPERATION	0x01	Operating mode control. On/Off, Margin High and Margin Low.	R/W Byte	Y	Reg		Y	0x00	34
ON_OFF_CONFIG	0x02	CONTROL pin and PMBus on/off command setting.	R/W Byte	Y	Reg		Y	0x1E	34
CLEAR_FAULTS	0x03	Clear any fault bits that have been set.	Send Byte	Y				NA	65
WRITE_PROTECT	0x10	Level of protection provided by the device against accidental changes.	R/W Byte	N	Reg		Y	0x00	29
STORE_USER_ALL	0x15	Store entire operating memory to EEPROM.	Send Byte	N				NA	44
RESTORE_USER_ALL	0x16	Restore entire operating memory from EEPROM.	Send Byte	N				NA	44
CAPABILITY	0x19	Summary of PMBus optional communication protocols supported by this device.	R Byte	N	Reg			0xB0	83
VOUT_MODE	0x20	Output voltage data format and mantissa exponent (2^{-13}).	R Byte	Y	Reg			0x13	48
VOUT_COMMAND	0x21	Servo target. Nominal DC/DC converter output voltage setpoint.	R/W Word	Y	L16	V	Y	1.0 0x2000	48
VOUT_MAX	0x24	Upper limit on the output voltage the unit can command regardless of any other commands.	R/W Word	Y	L16	V	Y	4.0 0x8000	48
VOUT_MARGIN_HIGH	0x25	Margin high DC/DC converter output voltage setting.	R/W Word	Y	L16	V	Y	1.05 0x219A	48
VOUT_MARGIN_LOW	0x26	Margin low DC/DC converter output voltage setting.	R/W Word	Y	L16	V	Y	0.95 0x1E66	48
VIN_ON	0x35	Input voltage (V_{IN_SNS}) above which power conversion can be enabled.	R/W Word	N	L11	V	Y	10.0 0xD280	47
VIN_OFF	0x36	Input voltage (V_{IN_SNS}) below which power conversion is disabled. All $V_{OUT\_EN}n$ pins go off immediately or sequence off after TOFF_DELAY (See Mfr_track_en_chann).	R/W Word	N	L11	V	Y	9.0 0xD240	47
IOUT_CAL_GAIN	0x38	The nominal resistance of the current sense element in mΩ.	R/W Word	Y	L11	mΩ	Y	1.0 0xBA00	50
VOUT_OV_FAULT_LIMIT	0x40	Output overvoltage fault limit.	R/W Word	Y	L16	V	Y	1.1 0x2333	48
VOUT_OV_FAULT_RESPONSE	0x41	Action to be taken by the device when an output overvoltage fault is detected.	R/W Byte	Y	Reg		Y	0x80	58
VOUT_OV_WARN_LIMIT	0x42	Output overvoltage warning limit.	R/W Word	Y	L16	V	Y	1.075 0x2266	48
VOUT_UV_WARN_LIMIT	0x43	Output undervoltage warning limit.	R/W Word	Y	L16	V	Y	0.925 0x1D9A	48
VOUT_UV_FAULT_LIMIT	0x44	Output undervoltage fault limit. Used for Ton_max_fault and power good de-assertion.	R/W Word	Y	L16	V	Y	0.9 0x1CCD	48

Note: The data format abbreviations are detailed at the end of this table

PMBUS COMMAND SUMMARY

Summary Table

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	EEPROM	DEFAULT VALUE: FLOAT HEX	REF PAGE
VOUT_UV_FAULT_RESPONSE	0x45	Action to be taken by the device when an output undervoltage fault is detected.	R/W Byte	Y	Reg		Y	0x7F	58
IOUT_OC_FAULT_LIMIT	0x46	Output overcurrent fault limit.	R/W Word	Y	L11	A	Y	10.0 0xD280	50
IOUT_OC_FAULT_RESPONSE	0x47	Action to be taken by the device when an output overcurrent fault is detected.	R/W Byte	Y	Reg		Y	0x00	58
IOUT_OC_WARN_LIMIT	0x4A	Output overcurrent warning limit.	R/W Word	Y	L11	A	Y	5.0 0xCA80	50
IOUT_UC_FAULT_LIMIT	0x4B	Output undercurrent fault limit. Used to detect a reverse current and must be a negative value.	R/W Word	Y	L11	A	Y	-1.0 0xB400	50
IOUT_UC_FAULT_RESPONSE	0x4C	Action to be taken by the device when an output undercurrent fault is detected.	R/W Byte	Y	Reg		Y	0x00	58
OT_FAULT_LIMIT	0x4F	Overtemperature fault limit for the external temperature sensor.	R/W Word	Y	L11	°C	Y	65.0 0xEA08	52
OT_FAULT_RESPONSE	0x50	Action to be taken by the device when an overtemperature fault is detected on the external temperature sensor.	R/W Byte	Y	Reg		Y	0xB8	58
OT_WARN_LIMIT	0x51	Overtemperature warning limit for the external temperature sensor	R/W Word	Y	L11	°C	Y	60.0 0xE3C0	52
UT_WARN_LIMIT	0x52	Undertemperature warning limit for the external temperature sensor.	R/W Word	Y	L11	°C	Y	0 0x8000	52
UT_FAULT_LIMIT	0x53	Undertemperature fault limit for the external temperature sensor.	R/W Word	Y	L11	°C	Y	–5.0 0xCD80	52
UT_FAULT_RESPONSE	0x54	Action to be taken by the device when an undertemperature fault is detected on the external temperature sensor.	R/W Byte	Y	Reg		Y	0xB8	58
VIN_OV_FAULT_LIMIT	0x55	Input overvoltage fault limit measured at V_{IN_SNS} pin.	R/W Word	N	L11	V	Y	15.0 0xD3C0	47
VIN_OV_FAULT_RESPONSE	0x56	Action to be taken by the device when an input overvoltage fault is detected.	R/W Byte	N	Reg		Y	0x80	58
VIN_OV_WARN_LIMIT	0x57	Input overvoltage warning limit measured at V_{IN_SNS} pin.	R/W Word	N	L11	V	Y	14.0 0xD380	47
VIN_UV_WARN_LIMIT	0x58	Input undervoltage warning limit measured at V_{IN_SNS} pin.	R/W Word	N	L11	V	Y	0 0x8000	47
VIN_UV_FAULT_LIMIT	0x59	Input undervoltage fault limit measured at V_{IN_SNS} pin.	R/W Word	N	L11	V	Y	0 0x8000	47
VIN_UV_FAULT_RESPONSE	0x5A	Action to be taken by the device when an input undervoltage fault is detected.	R/W Byte	N	Reg		Y	0x00	58
POWER_GOOD_ON	0x5E	Output voltage at or above which a power good should be asserted.	R/W Word	Y	L16	V	Y	0.96 0x1EB8	48
POWER_GOOD_OFF	0x5F	Output voltage at or below which a power good should be de-asserted when Mfr_config_all_pwrgd_off_uses_uv is clear.	R/W Word	Y	L16	V	Y	0.94 0x1E14	48

PMBUS COMMAND SUMMARY

Summary Table

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	EEPROM	DEFAULT VALUE: FLOAT HEX	REF PAGE
TON_DELAY	0x60	Time from CONTROL pin and/or OPERATION command = ON to $V_{OUT\_EN}n$ pin = ON.	R/W Word	Y	L11	ms	Y	1.0 0xBA00	55
TON_RISE	0x61	Time from when the $V_{OUT\_EN}n$ pin goes high until the LTC2974 optionally soft-connects its DAC and begins to servo the output voltage to the desired value.	R/W Word	Y	L11	ms	Y	10.0 0xD280	55
TON_MAX_FAULT_LIMIT	0x62	Maximum time from $V_{OUT\_EN}n$ = ON assertion that an UV condition will be tolerated before a TON_MAX_FAULT condition results.	R/W Word	Y	L11	ms	Y	15.0 0xD3C0	55
TON_MAX_FAULT_RESPONSE	0x63	Action to be taken by the device when a TON_MAX_FAULT event is detected.	R/W Byte	Y	Reg		Y	0xB8	58
TOFF_DELAY	0x64	Time from CONTROL pin and/or OPERATION command = OFF to $V_{OUT\_EN}n$ pin = OFF.	R/W Word	Y	L11	ms	Y	1.0 0xBA00	55
STATUS_BYTE	0x78	One byte summary of the unit's fault condition.	R Byte	Y	Reg			NA	65
STATUS_WORD	0x79	Two byte summary of the unit's fault condition.	R Word	Y	Reg			NA	65
STATUS_VOUT	0x7A	Output voltage fault and warning status.	R Byte	Y	Reg			NA	65
STATUS_IOUT	0x7B	Output current fault and warning status.	R Byte	Y	Reg			NA	65
STATUS_INPUT	0x7C	Input supply fault and warning status.	R Byte	N	Reg			NA	65
STATUS_TEMPERATURE	0x7D	External temperature fault and warning status for READ_TEMPERATURE_1.	R Byte	Y	Reg			NA	65
STATUS_CML	0x7E	Communication and memory fault and warning status.	R Byte	N	Reg			NA	65
STATUS_MFR_SPECIFIC	0x80	Manufacturer specific fault and state information.	R Byte	Y	Reg			NA	65
READ_VIN	0x88	Input supply voltage.	R Word	N	L11	V		NA	70
READ_VOUT	0x8B	DC/DC converter output voltage.	R Word	Y	L16	V		NA	70
READ_IOUT	0x8C	DC/DC converter output current.	R Word	Y	L11	A		NA	70
READ_TEMPERATURE_1	0x8D	External diode junction temperature. This is the value used for all temperature related processing, including IOUT_CAL_GAIN.	R Word	Y	L11	°C		NA	70
READ_TEMPERATURE_2	0x8E	Internal junction temperature.	R Word	N	L11	°C		NA	70
READ_POUT	0x96	DC/DC converter output power.	R Word	Y	L11	W		NA	70
PMBUS_REVISION	0x98	PMBus revision supported by this device. Current revision is 1.1.	R Byte	N	Reg			0x11	83
USER_DATA_00	0xB0	Manufacturer reserved for LTpowerPlay.	R/W Word	N	Reg		Y	NA	84
USER_DATA_01	0xB1	Manufacturer reserved for LTpowerPlay.	R/W Word	Y	Reg		Y	NA	84
USER_DATA_02	0xB2	OEM Reserved.	R/W Word	N	Reg		Y	NA	84

PMBUS COMMAND SUMMARY

Summary Table

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	EEPROM	DEFAULT VALUE: FLOAT HEX	REF PAGE
USER_DATA_03	0xB3	Scratchpad location.	R/W Word	Y	Reg		Y	0x0000	84
USER_DATA_04	0xB4	Scratchpad location.	R/W Word	N	Reg		Y	0x0000	84
MFR_LTC_RESERVED_1	0xB5	Manufacturer reserved.	R/W Word	Y	Reg		Y	NA	84
MFR_INFO	0xB6	Manufacturer specific information.	R Word	N	Reg			NA	83
MFR_T_SELF_HEAT	0xB8	Calculated temperature rise due to self-heating of output current sense device above value measured by external temperature sensor.	R Word	Y	L11	°C		NA	52
MFR_IOUT_CAL_GAIN_TAU_INV	0xB9	Inverse of time constant for Mfr_t_self_heat changes scaled by 4 • t_{CONV_SENSE}.	R/W Word	Y	L11		Y	0.0 0x8000	52
MFR_IOUT_CAL_GAIN_THETA	0xBA	Thermal resistance from inductor core to point measured by external temperature sensor.	R/W Word	Y	L11	°C/W	Y	0.0 0x8000	52
MFR_READ_IOUT	0xBB	Alternate data format for READ_IOUT. One LSB = 2.5mA.	R Word	Y	CF	2.5mA		NA	70
MFR_LTC_RESERVED_2	0xBC	Manufacturer reserved.	R/W Word	Y	Reg			NA	84
MFR_EE_UNLOCK	0xBD	Unlock user EEPROM for access by MFR_EE_ERASE and MFR_EE_DATA commands.	R/W Byte	N	Reg			NA	44
MFR_EE_ERASE	0xBE	Initialize user EEPROM for bulk programming by MFR_EE_DATA.	R/W Byte	N	Reg			NA	44
MFR_EE_DATA	0xBF	Data transferred to and from EEPROM using sequential PMBus word reads or writes. Supports bulk programming.	R/W Word	N	Reg			NA	44
MFR_COMMAND_PLUS	0xC8	Alternate access to block read and other data. Commands for all additional hosts.	R/W Word	N	Reg				29
MFR_DATA_PLUS0	0xC9	Alternate access to block read and other data. Data for additional host 0.	R/W Word	N	Reg				29
MFR_DATA_PLUS1	0xCA	Alternate access to block read and other data. Data for additional host 1.	R/W Word	N	Reg				29
MFR_CONFIG_LTC2974	0xD0	Configuration bits that are channel specific.	R/W Word	Y	Reg		Y	0x0080	34
MFR_CONFIG_ALL_LTC2974	0xD1	Configuration bits that are common to all pages.	R/W Word	N	Reg		Y	0x0F7B	34
MFR_FAULTB0_PROPAGATE	0xD2	Configuration that determines if a channel's faulted off state is propagated to the FAULTB0 pin.	R/W Byte	Y	Reg		Y	0x00	63
MFR_FAULTB1_PROPAGATE	0xD3	Configuration that determines if a channel's faulted off state is propagated to the FAULTB1 pin.	R/W Byte	Y	Reg		Y	0x00	63
MFR_PWRGD_EN	0xD4	Configuration that maps WDI/RESETB status and individual channel power good to the PWRGD pin.	R/W Word	N	Reg		Y	0x0000	56
MFR_FAULTB0_RESPONSE	0xD5	Action to be taken by the device when the FAULTB0 pin is asserted low.	R/W Byte	N	Reg		Y	0x00	63
MFR_FAULTB1_RESPONSE	0xD6	Action to be taken by the device when the FAULTB1 pin is asserted low.	R/W Byte	N	Reg		Y	0x00	63

PMBUS COMMAND SUMMARY

Summary Table

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	EEPROM	DEFAULT VALUE: FLOAT HEX	REF PAGE
MFR_IOUT_PEAK	0xD7	Maximum measured value of READ_IOUT.	R Word	Y	L11	A		NA	70
MFR_IOUT_MIN	0xD8	Minimum measured value of READ_IOUT.	R Word	Y	L11	A		NA	70
MFR_CONFIG2_LTC2974	0xD9	Configuration bits that are channel specific	R/W Byte	N	Reg		Y	0x00	34
MFR_CONFIG3_LTC2974	0xDA	Configuration bits that are channel specific	R/W Byte	N	Reg		Y	0x00	34
MFR_RETRY_DELAY	0xDB	Retry interval during FAULT retry mode.	R/W Word	N	L11	ms	Y	200 0xF320	58
MFR_RESTART_DELAY	0xDC	Delay from actual CONTROL active edge to virtual CONTROL active edge.	R/W Word	N	L11	ms	Y	400 0xFB20	55
MFR_VOUT_PEAK	0xDD	Maximum measured value of READ_VOUT.	R Word	Y	L16	V		NA	70
MFR_VIN_PEAK	0xDE	Maximum measured value of READ_VIN.	R Word	N	L11	V		NA	70
MFR_TEMPERATURE_1_PEAK	0xDF	Maximum measured value of READ_TEMPERATURE_1.	R Word	Y	L11	°C		NA	70
MFR_DAC	0xE0	The code of the 10-bit DAC.	R/W Word	Y	Reg			NA	48
MFR_POWERGOOD_ ASSERTION_DELAY	0xE1	Power-good output assertion delay.	R/W Word	N	L11	ms	Y	100 0xEB20	56
MFR_WATCHDOG_T_FIRST	0xE2	First watchdog timer interval.	R/W Word	N	L11	ms	Y	0 0x8000	56
MFR_WATCHDOG_T	0xE3	Watchdog timer interval.	R/W Word	N	L11	ms	Y	0 0x8000	56
MFR_PAGE_FF_MASK	0xE4	Configuration defining which channels respond to global page commands (PAGE=0xFF).	R/W Byte	N	Reg		Y	0x0F	29
MFR_PADS	0xE5	Current state of selected digital I/O pads.	R/W Word	N	Reg			NA	65
MFR_I2C_BASE_ADDRESS	0xE6	Base value of the I^2C/SMBus address byte.	R/W Byte	N	Reg		Y	0x5C	29
MFR_SPECIAL_ID	0xE7	Manufacturer code for identifying the LTC2974.	R Word	N	Reg		Y	0x0215	83
MFR_SPECIAL_LOT	0xE8	Customer dependent codes that identify the factory programmed user configuration stored in EEPROM. Contact factory for default value.	R Byte	Y	Reg		Y	NA	83
MFR_VOUT_DISCHARGE_ THRESHOLD	0xE9	Coefficient used to multiply VOUT_ COMMAND in order to determine V_{OUT} off threshold voltage.	R/W Word	Y	L11		Y	2.0 0xC200	48
MFR_FAULT_LOG_STORE	0xEA	Command a transfer of the fault log from RAM to EEPROM.	Send Byte	N				NA	74
MFR_FAULT_LOG_RESTORE	0xEB	Command a transfer of the fault log previously stored in EEPROM back to RAM.	Send Byte	N				NA	74
MFR_FAULT_LOG_CLEAR	0xEC	Initialize the EEPROM block reserved for fault logging and clear any previous fault logging locks.	Send Byte	N				NA	74
MFR_FAULT_LOG_STATUS	0xED	Fault logging status.	R Byte	N	Reg		Y	NA	74

PMBUS COMMAND SUMMARY

Summary Table

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	EEPROM	DEFAULT VALUE: FLOAT HEX	REF PAGE
MFR_FAULT_LOG	0xEE	Fault log data bytes. This sequentially retrieved data is used to assemble a complete fault log.	R Block	N	Reg		Y	NA	74
MFR_COMMON	0xEF	Manufacturer status bits that are common across multiple LTC chips.	R Byte	N	Reg			NA	65
MFR_IOUT_CAL_GAIN_TC	0xF6	Temperature coefficient applied to IOUT_CAL_GAIN.	R/W Word	Y	CF	ppm	Y	0x0000	50
MFR_RETRY_COUNT	0xF7	Retry count for all faulted off conditions that enable retry.	R/W Byte	N	Reg		Y	0x07	58
MFR_TEMP_1_GAIN	0xF8	Inverse of external diode temperature non ideality factor. One LSB = 2^{-14}.	R/W Word	Y	CF		Y	1 0x4000	52
MFR_TEMP_1_OFFSET	0xF9	Offset value for the external temperature.	R/W Word	Y	L11	°C	Y	0 0x8000	52
MFR_IOUT_SENSE_VOLTAGE	0xFA	Absolute value of the voltage between $I_{SENSEP}n$ and $I_{SENSEM}n$. One LSB = 3.05µV.	R Word	Y	CF	3.05µV		NA	70
MFR_VOUT_MIN	0xFB	Minimum measured value of READ_VOUT.	R Word	Y	L16	V		NA	70
MFR_VIN_MIN	0xFC	Minimum measured value of READ_VIN.	R Word	N	L11	V		NA	70
MFR_TEMPERATURE_1_MIN	0xFD	Minimum measured value of READ_TEMPERATURE_1.	R Word	Y	L11	°C		NA	70

Data Formats

L11	Linear_5s_11s	PMBus data field b[15:0] Value = $Y \cdot 2^N$ where N = b[15:11] is a 5-bit two's complement integer and Y = b[10:0] is an 11-bit two's complement integer Example: READ_VIN = 10V For b[15:0] = 0xD280 = 1101_0010_1000_0000b Value = $640 \cdot 2^{-6} = 10$ See PMBus Spec Part II: Paragraph 7.3
L16	Linear_16u	PMBus data field b[15:0] Value = $Y \cdot 2^N$ where Y = b[15:0] is an unsigned integer and N = Vout_mode_parameter is a 5-bit two's complement exponent that is hardwired to –13 decimal. Example: VOUT_COMMAND = 4.75V For b[15:0] = 0x9800 = 1001_1000_0000_0000b Value = $38912 \cdot 2^{-13} = 4.75$ See PMBus Spec Part II: Paragraph 8.4.1
Reg	Register	PMBus data field b[15:0] or b[7:0]. Bit field meaning is defined in detailed PMBus Command Register Description.
CF	Custom Format	PMBus data field b[15:0] Value is defined in detailed PMBus Command Register Description. This is often an unsigned or two's complement integer scaled by an MFR specific constant.

PMBUS COMMAND DESCRIPTION

ADDRESSING AND WRITE PROTECT

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	EEPROM	DEFAULT VALUE	REF PAGE
PAGE	0x00	Channel or page currently selected for any command that supports paging.	R/W Byte	N	Reg			0x00	29
WRITE_PROTECT	0x10	Level of protection provided by the device against accidental changes.	R/W Byte	N	Reg		Y	0x00	30
MFR_I2C_BASE_ADDRESS	0xE6	Base value of the I^2C/SMBus address byte.	R/W Byte	N	Reg		Y	0x5C	31
MFR_PAGE_FF_MASK	0xE4	Configuration defining which channels respond to global page commands (PAGE=0xFF).	R/W Byte	N	Reg		Y	0x0F	30
MFR_COMMAND_PLUS	0xC8	Alternate access to block read and other data. Commands for all additional hosts.	R/W Word	N	Reg				31
MFR_DATA_PLUS0	0xC9	Alternate access to block read and other data. Data for additional host 0.	R/W Word	N	Reg				31
MFR_DATA_PLUS1	0xCA	Alternate access to block read and other data. Data for additional host 1.	R/W Word	N	Reg				31

PAGE

The LTC2974 has four pages that correspond to the four DC/DC converter channels that can be managed. Each DC/DC converter channel can be uniquely programmed by first setting the appropriate page.

Setting PAGE = 0xFF allows a simultaneous write to all pages for PMBus commands that support global page programming. The only commands that support PAGE = 0xFF are CLEAR_FAULTS, OPERATION and ON_OFF_CONFIG. See MFR_PAGE_FF_MASK for additional options. Reading any paged PMBus register with PAGE = 0xFF returns unpredictable data and will trigger a CML fault. Writes to commands that do not support PAGE = 0xFF with PAGE = 0xFF will be ignored and generate a CML fault.

PAGE Data Contents

BIT(S)	SYMBOL	OPERATION
b[7:0]	Page	Page operation. 0x00: All PMBus commands address channel/page 0. 0x01: All PMBus commands address channel/page 1. 0x02: All PMBus commands address channel/page 2. 0x03: All PMBus commands address channel/page 3. 0xXX: All non specified values reserved. 0xFF: A single PMBus write/send to commands that support this mode will simultaneously address all channel/pages with MFR_PAGE_FF_MASK enabled.

PMBUS COMMAND DESCRIPTION

WRITE_PROTECT

The WRITE_PROTECT command provides protection against accidental programming of the LTC2974 command registers. All supported commands may have their parameters read, regardless of the WRITE_PROTECT setting, and the EEPROM contents can also be read regardless of the WRITE_PROTECT settings.

There are two levels of protection:

- Level 1: Nothing can be changed except the level of write protection itself. Values can be read from all pages. This setting can be stored to EEPROM.
- Level 2: Nothing can be changed except for the level of protection, channel on/off state, and clearing of faults. Values can be read from all pages. This setting can be stored to EEPROM.

WRITE_PROTECT Data Contents

BIT(S)	SYMBOL	OPERATION
b[7:0]	Write_protect[7:0]	1000_0000b: Level 1 Protection - Disable all writes except to the WRITE_PROTECT, PAGE, MFR_EE_UNLOCK, and STORE_USER_ALL commands. 0100_0000b: Level 2 Protection – Disable all writes except to the WRITE_PROTECT, PAGE, MFR_EE_UNLOCK, STORE_USER_ALL, OPERATION, MFR_PAGE_FF_MASK and CLEAR_FAULTS commands. 0000_0000b: Enable writes to all commands. xxxx_xxxxb: All other values reserved.

Write Protect Pin

The WP pin allows the user to write-protect the LTC2974's configuration registers. The WP pin is active high, and when asserted it provides Level 2 protection: all writes are disabled except to the WRITE_PROTECT, PAGE, MFR_EE_UNLOCK, STORE_USER_ALL, OPERATION, MFR_PAGE_FF_MASK and CLEAR_FAULTS commands. The most restrictive setting between the WP pin and WRITE_PROTECT command will override.

WP PIN STATE	WRITE_PROTECT COMMAND VALUE	WRITE PROTECT LEVEL
Low	0x00	No write protection
	0x40	Level 2
	0x80	Level 1
High	0x00	Level 2
	0x40	Level 2
	0x80	Level 1

MFR_PAGE_FF_MASK

The MFR_PAGE_FF_MASK command is used to select which channels respond when the global page command (PAGE=0xFF) is in use.

MFR_PAGE_FF_MASK Data Contents

BIT(S)	SYMBOL	OPERATION
b[7:4]	Reserved	Always returns 0000b
b[3]	Mfr_page_ff_mask_chan3	Channel 3 masking of global page command (PAGE=0xFF) accesses 0 = ignore global page command accesses 1 = fully respond to global page command accesses

PMBUS COMMAND DESCRIPTION

MFR_PAGE_FF_MASK Data Contents

BIT(S)	SYMBOL	OPERATION
b[2]	Mfr_page_ff_mask_chan2	Channel 2 masking of global page command (PAGE=0xFF) accesses 0 = ignore global page command accesses 1 = fully respond to global page command accesses
b[1]	Mfr_page_ff_mask_chan1	Channel 1 masking of global page command (PAGE=0xFF) accesses 0 = ignore global page command accesses 1 = fully respond to global page command accesses
b[0]	Mfr_page_ff_mask_chan0	Channel 0 masking of global page command (PAGE=0xFF) accesses 0 = ignore global page command accesses 1 = fully respond to global page command accesses

MFR_I2C_BASE_ADDRESS

The MFR_I2C_BASE_ADDRESS command determines the base value for the I^2C/SMBus address byte. Offsets of 0 to 8 are added to this base address to generate the device I^2C/SMBus address. The part responds to the device address. For example, with the factory default MFR_I2C_BASE_ADDRESS of 0x5C, with both ASEL1 and ASEL0 High (Offset N=2), the device address would be 0x5C+2 = 0x5E.

MFR_I2C_BASE_ADDRESS Data Contents

BIT(S)	SYMBOL	OPERATION
b[7]	Reserved	Read only, always returns 0.
b[6:0]	i2c_base_address	This 7-bit value determines the base value of the 7-bit I^2C/SMBus address. See Operation Section: Device Address.

MFR_COMMAND_PLUS

MFR_DATA_PLUS0 and MFR_DATA_PLUS1

MFR_STATUS_PLUS0, and MFR_STATUS_PLUS1

Similar to the PAGE register, these registers allow the user to indirectly address memory. These registers are useful to advanced users for reading or writing memory as described below.

Command Plus operations use a sequence of word commands to support the following:

- An alternate method for reading block data using sequential standard word reads.
- A peek operation that allows up to two additional hosts to read an internal register using PMBus word protocol where each host has a unique page.
- A poke operation that allows up to two additional hosts to write an internal register using PMBus word protocol where each host has a unique page.
- Peek, Poke and Command Plus block reads do not interfere with normal PMBus accesses or page values set by PAGE. This enables multi master support for up to 3 hosts.

PMBUS COMMAND DESCRIPTION

MFR_COMMAND_PLUS Data Contents

BIT(S)	SYMBOL	OPERATION
b[15]	Mfr_command_plus_reserved	Reserved. Always returns 0.
b[14]	Mfr_command_plus_id	Command plus host ID. 0: Mfr_command_plus pointer and page are cached and used for all Mfr_data_plus0 accesses. 1: Mfr_command_plus pointer and page are cached and used for all Mfr_data_plus1 accesses.
b[13:9]	Mfr_command_plus_page	Page to be used when peeking or poking via Mfr_data_plus0 or Mfr_data_plus1. Allowed values are 0 through 3. This page value is cached separately for Mfr_data_plus0 and Mfr_data_plus1 based on the value of Mfr_command_plus_id when this register is written.
b[8:0]	Mfr_command_plus_pointer	Internal memory location accessed by Mfr_data_plus0 or Mfr_data_plus1. Mfr_data_plus0 and Mfr_data_plus1 pointers are cached separately. Legal values are listed in the CMD Code column of the PMBus COMMAND SUMMARY table. All other values are reserved, except for the special poke enable/disable values listed in the Enabling and Disabling Poke Operations section, and the command values listed below for Mfr_status_plus0 and Mfr_status_plus1.

MFR_DATA_PLUS0 and MFR_DATA_PLUS1 Data Contents

BIT(S)	SYMBOL	OPERATION
b[15:0]	Mfr_data_plus0 Mfr_data_plus1	A read from this register returns data referenced by the last matching Mfr_command_plus write. More specifically, writes to Mfr_command_plus by host 0 update Mfr_data_plus0, and writes to Mfr_command_plus by host1 update Mfr_data_plus1. Multiple sequential reads while pointer = Mfr_fault_Log return the complete contents of the block read buffer. Block reads beyond the end of buffer return zeros. A write to this register will transfer the data to the location referenced by the last matching Mfr_command_plus_pointer when the Poke operation protocol described in the Poke Operation Using Mfr_data_plus0 section is followed.

MFR_STATUS_PLUS0 and MFR_STATUS_PLUS1 Data Contents

BIT(S)	SYMBOL	OPERATION
b[7:2]	Reserved	
b[1]	Mfr_status_plus_poke_failed0 Mfr_status_plus_poke_failed1	Status of most recent poke for matching host. 0: Last poke operation did not fail. 1: Last poke operation failed because pokes were not enabled, as described in Enabling and Disabling Poke Operations below, or an illegal Mfr_command_plus_page value was used.
b[0]	Mfr_status_plus_block_peek_failed0 Mfr_status_plus_block_peek_failed1	Status of most recent block peek for matching host. 0: Last block peek was not aborted. 1: Last block peek was aborted due to an intervening fault log EEPROM write, MFR_FAULT_LOG_STORE command, or standard PMBus block read of MFR_FAULT_LOG. The intervening operation is always completed cleanly.

MFR_STATUS_PLUS0 is at command location 0x2C, and MFR_STATUS_PLUS1 is at command location 0x2D. These correspond to reserved PMBus command locations. These two status registers can only be read via Command Plus peeks.

Reading Fault Log Using Command Plus and Mfr_data_plus0

Write Mfr_command_plus_pointer = 0xEE with Mfr_command_plus_page = 0 and Mfr_command_plus_id = 0.

Read data from Mfr_data_plus0; each read returns the next data word of the MFR_FAULT_LOG command:

- The first word read is Byte_count[15:0] = 0x00FF.
- The next set of words read is the Preamble with 2 bytes packed into a word. Refer to the Fault Log section for details.
- The next set of words read is the Cyclical Loop Data with 2 bytes per word. Refer to the Fault Log section for details.

PMBUS COMMAND DESCRIPTION

- Extra reads return zero.
- Interleaved PMBus word and byte commands do not interfere with an ongoing Command Plus block read.
- Interleaved PMBus block reads of MFR_FAULT_LOG will interrupt this command.

Check status to be sure the data just read was all valid:

- Write Mfr_command_plus_pointer = 0x2C with Mfr_command_plus_page = 0 and Mfr_command_plus_id = 0.
- Read data from Mfr_data_plus0 and confirm that Mfr_status_plus_block_peek_failed0 = 0.

Peek Operation Using Mfr_data_plus0

Internal words and bytes may be read using Command Plus:

Write Mfr_command_plus_pointer = CMD_CODE with Mfr_command_plus_page = page and Mfr_command_plus_id = 0.

The CMD_CODE's are listed in the PMBus COMMAND SUMMARY table.

Read data from Mfr_data_plus0. Data is always read using a word read. Byte data is returned with upper byte set to 0.

Enabling and Disabling Poke Operations

Poke operations to Mfr_data_plus0 are enabled by writing Mfr_command_plus = 0x0BF6.

Poke operations to Mfr_data_plus0 are disabled by writing Mfr_command_plus = 0x01F6.

Poke operations to Mfr_data_plus1 are enabled by writing Mfr_command_plus = 0x4BF6.

Poke operations to Mfr_data_plus1 are disabled by writing Mfr_command_plus = 0x41F6.

Poke Operation Using Mfr_data_plus0

Internal words and bytes may be written using Command Plus:

Enable Poke access for Mfr_data_plus0. This need only be done once after a power-up or WDI reset.

Write Mfr_command_plus_pointer = CMD_CODE with Mfr_command_plus_page = page and Mfr_command_plus_id = 0.

The CMD_CODEs are listed in the PMBus COMMAND SUMMARY table.

Write the new data value to MFR_DATA_PLUS0

Optionally check status to be sure data was written as desired:

- Write Mfr_command_plus_pointer = 0x2C with Mfr_command_plus_page = 0 and Mfr_command_plus_id = 0.
- Read data from Mfr_data_plus0 and confirm that Mfr_status_plus_poke_failed0 = 0.

Command Plus Operations Using Mfr_data_plus1

All the previous operations may be accessed via Mfr_data_plus1 by substituting Mfr_command_plus_id value with a 1. Poke operations must be enabled for Mfr_data_plus1.

PMBUS COMMAND DESCRIPTION

ON/OFF CONTROL, MARGINING AND CONFIGURATION

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	EEPROM	DEFAULT VALUE	REF PAGE
OPERATION	0x01	Operating mode control. On/Off, Margin High and Margin Low.	R/W Byte	Y	Reg		Y	0x00	34
ON_OFF_CONFIG	0x02	CONTROL pin and PMBus on/off command setting.	R/W Byte	Y	Reg		Y	0x1E	35
MFR_CONFIG_LTC2974	0xD0	Configuration bits that are channel specific.	R/W Word	Y	Reg		Y	0x0080	36
MFR_CONFIG2_LTC2974	0xD9	Configuration bits that are channel specific	R/W Byte	N	Reg		Y	0x00	39
MFR_CONFIG3_LTC2974	0xDA	Configuration bits that are channel specific	R/W Byte	N	Reg		Y	0x00	39
MFR_CONFIG_ALL_LTC2974	0xD1	Configuration bits that are common to all pages.	R/W Word	N	Reg		Y	0x0F7B	43

OPERATION

The OPERATION command is used to turn the unit on and off in conjunction with the CONTROL pin and ON_OFF_CONFIG. This command register responds to the global page command (PAGE=0xFF). The contents and functions of the data byte are shown in the following tables. A minimum t_{OFF_MIN} wait time must be observed between any OPERATION commands used to turn the unit off and then back on.

OPERATION Data Contents (On_off_config_use_pmbus=1)

SYMBOL	Action	Operation_control[1:0]	Operation_margin[1:0]	Operation_fault[1:0]	Reserved (read only)
BITS		b[7:6]	b[5:4]	b[3:2]	b[1:0]
FUNCTION	Turn off immediately	00	XX	XX	00
	Sequence on	10	00	XX	00
	Margin low (ignore faults and warnings)	10	01	01	00
	Margin low	10	01	10	00
	Margin high (ignore faults and warnings	10	10	01	00
	Margin high	10	10	10	00
	Sequence off with margin to nominal	01	00	XX	00
	Sequence off with margin low (ignore faults and warnings)	01	01	01	00
	Sequence off with margin low	01	01	10	00
	Sequence off with margin high (ignore faults and warnings)	01	10	01	00
	Sequence off with margin high	01	10	10	00
	Reserved	All remaining combinations			

PMBUS COMMAND DESCRIPTION

OPERATION Data Contents (On_off_config_use_pmbus=0)
On or Off

SYMBOL	Action	Operation_control[1:0]	Operation_margin[1:0]	Operation_fault[1:0]	Reserved (read only)
BITS		b[7:6]	b[5:4]	b[3:2]	b[1:0]
FUNCTION	Output at nominal	00, 01 or 10	00	XX	00
	Margin low (ignore faults and warnings)	00, 01 or 10	01	01	00
	Margin low	00, 01 or 10	01	10	00
	Margin high (ignore faults and warnings	00, 01 or 10	10	01	00
	Margin high	00, 01 or 10	10	10	00
	Reserved	All remaining combinations			

ON_OFF_CONFIG

The ON_OFF_CONFIG command configures the combination of CONTROL pin input and PMBus commands needed to turn the LTC2974 on/off, including the power-on behavior, as shown in the following table. This command register responds to the global page command (PAGE=0xFF). After the part has initialized, an additional comparator monitors VIN_SNS. The VIN_ON threshold must be exceeded before the output power sequencing can begin. After V_{IN} is initially applied, the part will typically require t_{INIT} time to initialize and begin the TON_DELAY timer. The readback of voltages and currents may require an additional wait for tUPDATE_ADC. A minimum t_{OFF_MIN} wait time must be observed for any CONTROL pin toggle used to turn the unit off and then back on.

ON_OFF_CONFIG Data Contents

BIT(S)	SYMBOL	OPERATION
b[7:5]	Reserved	Don't care. Always returns 0.
b[4]	On_off_config_controlled_on	Control default autonomous power up operation. 0: Unit powers up regardless of the CONTROL pin or OPERATION value. Unit always powers up with sequencing. To turn unit on without sequencing, set TON_DELAY = 0. 1: Unit does not power up unless commanded by the CONTROL pin and/or the OPERATION command on the serial bus. If On_off_config[3:2] = 00, the unit never powers up.
b[3]	On_off_config_use_pmbus	Controls how the unit responds to commands received via the serial bus. 0: Unit ignores the Operation_control[1:0]. 1: Unit responds to Operation_control[1:0]. Depending on On_off_config_use_control, the unit may also require the CONTROL pin to be asserted for the unit to start.
b[2]	On_off_config_use_control	Controls how unit responds to the CONTROL pin. 0: Unit ignores the CONTROL pin. 1: Unit requires the CONTROL pin to be asserted to start the unit. Depending on On_off_config_use_pmbus the OPERATION command may also be required to instruct the device to start.
b[1]	Reserved	Not supported. Always returns 1.
b[0]	On_off_config_control_fast_off	CONTROL pin turn off action when commanding the unit to turn off 0: Use the programmed TOFF_DELAY. 1: Turn off the output and stop transferring energy as quickly as possible. The device does not sink current in order to decrease the output voltage fall time.

PMBUS COMMAND DESCRIPTION

MFR_CONFIG_LTC2974

This command is used to configure various manufacturer specific operating parameters for each channel.

MFR_CONFIG_LTC2974 Data Contents

BIT(S)	SYMBOL	OPERATION
b[15]	Reserved	Don't care. Always returns 0.
b[14]	Mfr_config_cascade_on	Configures channel's control pin for cascade sequence ON. There is no provision for cascade sequence OFF. See description for time based sequence OFF options.
b[13:12]	Mfr_config_controln_sel	Selects the active control pin input (CONTROL0 , CONTROL1, CONTROL2 or CONTROL3) for this channel. 00: Select CONTROL0 pin. 01: Select CONTROL1 pin. 10: Select CONTROL2 pin. 11: Select CONTROL3 pin.
b[11]	Mfr_config_fast_servo_off	Disables fast servo when margining or trimming output voltages: 0: fast-servo enabled. 1: fast-servo disabled.
b[10]	Mfr_config_supervisor_resolution	Selects voltage supervisor resolution: 0: high resolution = 4mV / LSB, range for $V_{VSENSEP n} – V_{VSENSEM n}$ is 0 to 3.8V 1: low resolution = 8mV / LSB, range for $V_{VSENSEP n} – V_{VSENSEM n}$ is 0 to 6.0V
b[9:8]	Reserved	Always returns 0.
b[7]	Mfr_config_servo_continuous	Select whether the UNIT should continuously servo VOUT after it has reached a new margin or nominal target. Only applies when Mfr_ config _dac_mode = 00b. 0: Do not continuously servo VOUT after reaching initial target. 1: Continuously servo VOUT to target.
b[6]	Mfr_config_servo_on_warn	Control re-servo on warning feature. Only applies when Mfr_config_dac_mode = 00b and Mfr_config_ servo_continuous = 0. 0: Do not allow the unit to re-servo when a VOUT warning threshold is met or exceeded. 1: Allow the unit to re-servo VOUT to nominal target if VOUT ≥ V(Vout_ov_warn_limit) or VOUT ≤ V(Vout_uv_warn_limit).
b[5:4]	Mfr_config_dac_mode	Determines how DAC is used when channel is in the ON state and TON_RISE has elapsed. 00: Soft-connect (if needed) and servo to target. 01: DAC not connected. 10: DAC connected immediately using value from MFR_DAC command. If this is the configuration after a reset or RESTORE_USER_ALL, MFR_DAC will be undefined and must be written to desired value. 11: DAC is soft-connected. After soft-connect is complete MFR_DAC may be written.
b[3]	Mfr_config_vo_en_wpu_en	V_{OUT_EN} pin charge-pumped, current-limited pull-up enable. 0: Disable weak pull-up. V_{OUT_EN} pin driver is three-stated when channel is on. 1: Use weak current-limited pull-up on V_{OUT_EN} pin when the channel is on.
b[2]	Mfr_config_vo_en_wpd_en	V_{OUT_EN} pin current-limited pull-down enable. 0: Use a fast N-channel device to pull down V_{OUT_EN} pin when the channel is off for any reason. 1: Use weak current-limited pull-down to discharge V_{OUT_EN} pin when channel is off due to soft stop by the CONTROL pin and/or OPERATION command. If the channel is off due to a fault, use the fast pull-down on the V_{OUT_EN} pin.

PMBUS COMMAND DESCRIPTION

MFR_CONFIG_LTC2974 Data Contents

BIT(S)	SYMBOL	OPERATION
b[1]	Mfr_config_dac_gain	DAC buffer gain. 0: Select DAC buffer gain dac_gain_0 (1.38V full-scale) 1: Select DAC buffer gain dac_gain_1 (2.65V full-scale)
b[0]	Mfr_config_ dac_pol	DAC output polarity. 0: Encodes negative (inverting) DC/DC converter trim input. 1: Encodes positive (non-inverting) DC/DC converter trim input.

Cascade Sequence ON with Time-Based Sequence OFF

Cascade sequence ON allows a master power supply to sequence on a series of slave supplies by connecting each power supply's power good output to the control pin of the next power supply in the chain. Please note that the power good signal is that of the power supply and not derived from the LTC2974's internal power good processing. Power good based cascade sequence OFF is not supported, OFF sequencing must be managed using immediate or time based sequence OFF. See also "Tracking Based Sequencing".

Cascade sequence ON is illustrated in Figure 15. For each slave channel Mfr_config_cascade_on is asserted high and the associated control input is connected to the power good output of the previous power supply. In this configuration each slave channel's startup is delayed until the previous supply has powered up.

Cascade sequence OFF is not directly supported. Options for reversing the sequence when turning the supplies off include:

- Using the OPERATION command to turn off all the channels with an appropriate off delay.
- Using the FAULT pin to bring all the channels down immediately or in sequence with an appropriate off delay.

When asserted, Mfr_config_cascade_on enables a slave channel to honor fault retries even when its control pin is low. Additionally, if the system has faulted off after zero or a finite number of retries, an OPERATION command may

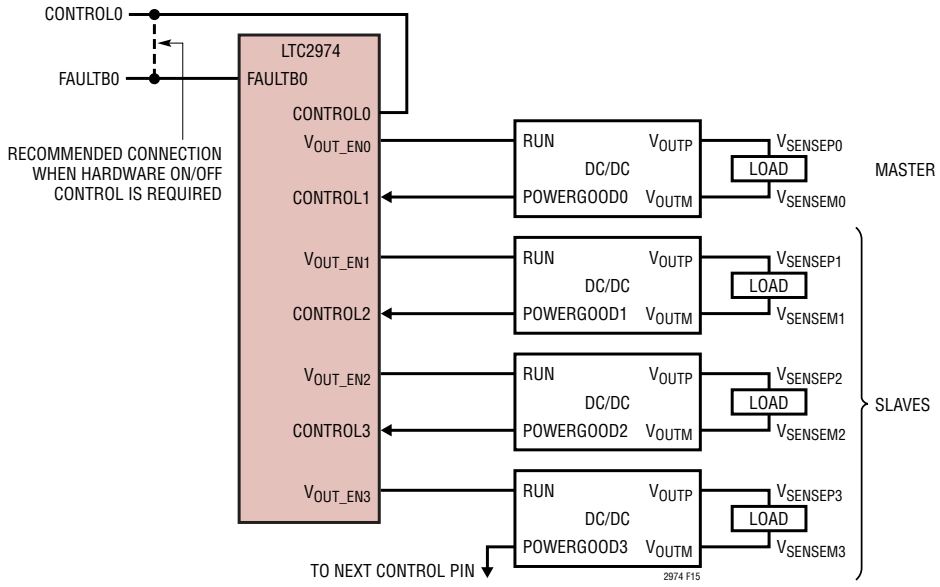


Figure 15. LTC2974 Configured to Cascade Sequence ON and Time-Base Sequence OFF

PMBUS COMMAND DESCRIPTION

be used to turn all cascade channels off then on to clear the faulted off state when the slave's control pin is low. For this reason we refer to the control pin as being redefined as a sequence pin.

The waveform of Figure 16 illustrates cascade sequence ON and time based sequence OFF using the configuration illustrated in Figure 15. In this example the FAULTB0 pin is used as a broadcast off signal. Turning the system off with the FAULTB0 requires all slave channels to be configured with Mfr_faultb0_response_chan*n* asserted high. After the system is turned off, the LTC2974 will assert ALERTB with all slave channels indicating a Status_mfr_fault0_in event.

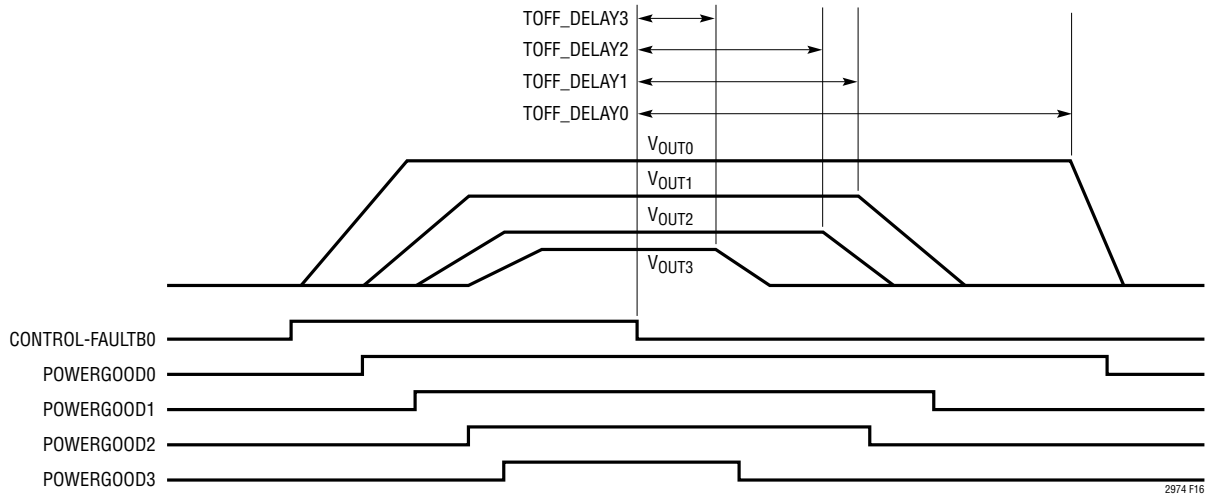


Figure 16. Cascade Sequence ON with Time Based Sequence Down on FAULT0

PMBUS COMMAND DESCRIPTION

MFR_CONFIG2_LTC2974

This command register determines whether V_{OUT} overvoltage or overcurrent faults from a given channel cause the AUXFAULTB pin to be pulled low.

MFR_CONFIG2_LTC2974 Data Contents

BIT(S)	SYMBOL	OPERATION
b[7]	Mfr_auxfaultb_oc_fault_response_chan3	Response to channel 3 IOUT_OC_FAULT. 1 = Pull AUXFAULTB low via fast pull-down. 0 = Do not pull AUXFAULTB low.
b[6]	Mfr_auxfaultb_oc_fault_response_chan2	Response to channel 2 IOUT_OC_FAULT. 1 = Pull AUXFAULTB low via fast pull-down. 0 = Do not pull AUXFAULTB low.
b[5]	Mfr_auxfaultb_oc_fault_response_chan1	Response to channel 1 IOUT_OC_FAULT. 1 = Pull AUXFAULTB low via fast pull-down. 0 = Do not pull AUXFAULTB low.
b[4]	Mfr_auxfaultb_oc_fault_response_chan0	Response to channel 0 IOUT_OC_FAULT. 1 = Pull AUXFAULTB low via fast pull-down. 0 = Do not pull AUXFAULTB low.
b[3]	Mfr_auxfaultb_ov_fault_response_chan3	Response to channel 3 VOUT_OV_FAULT. 1 = Pull AUXFAULTB low via fast pull-down. 0 = Do not pull AUXFAULTB low.
b[2]	Mfr_auxfaultb_ov_fault_response_chan2	Response to channel 2 VOUT_OV_FAULT. 1 = Pull AUXFAULTB low via fast pull-down. 0 = Do not pull AUXFAULTB low.
b[1]	Mfr_auxfaultb_ov_fault_response_chan1	Response to channel 1 VOUT_OV_FAULT. 1 = Pull AUXFAULTB low via fast pull-down. 0 = Do not pull AUXFAULTB low.
b[0]	Mfr_auxfaultb_ov_fault_response_chan0	Response to channel 0 VOUT_OV_FAULT. 1 = Pull AUXFAULTB low via fast pull-down. 0 = Do not pull AUXFAULTB low.

MFR_CONFIG3_LTC2974

This command register determines whether V_{OUT} undercurrent faults from a given channel cause the AUXFAULTB pin to be pulled low. This command also allows tracking to be enabled on any channel.

MFR_CONFIG3_LTC2974 Data Contents

BIT(S)	SYMBOL	OPERATION
b[7]	Mfr_auxfaultb_uc_fault_response_chan3	Response to channel 3 IOUT_UC_FAULT. 1 = Pull AUXFAULTB low via fast pull-down. 0 = Do not pull AUXFAULTB low.
b[6]	Mfr_auxfaultb_uc_fault_response_chan2	Response to channel 2 IOUT_UC_FAULT. 1 = Pull AUXFAULTB low via fast pull-down. 0 = Do not pull AUXFAULTB low.

PMBUS COMMAND DESCRIPTION

b[5]	Mfr_auxfaultb_uc_fault_response_chan1	Response to channel 1 IOUT_UC_FAULT. 1 = Pull AUXFAULTB low via fast pull-down. 0 = Do not pull AUXFAULTB low.
b[4]	Mfr_auxfaultb_uc_fault_response_chan0	Response to channel 0 IOUT_UC_FAULT. 1 = Pull AUXFAULTB low via fast pull-down. 0 = Do not pull AUXFAULTB low.
b[3]	Mfr_track_en_chan3	Select if channel 3 is a slave in a tracked power supply system. 0: Channel is not a slave in a tracked power supply system. 1: Channel is a slave in a tracked power supply system.
b[2]	Mfr_track_en_chan2	Select if channel 2 is a slave in a tracked power supply system. 0: Channel is not a slave in a tracked power supply system. 1: Channel is a slave in a tracked power supply system.
b[1]	Mfr_track_en_chan1	Select if channel 1 is a slave in a tracked power supply system. 0: Channel is not a slave in a tracked power supply system. 1: Channel is a slave in a tracked power supply system.
b[0]	Mfr_track_en_chan0	Select if channel 0 is a slave in a tracked power supply system. 0: Channel is not a slave in a tracked power supply system. 1: Channel is a slave in a tracked power supply system.

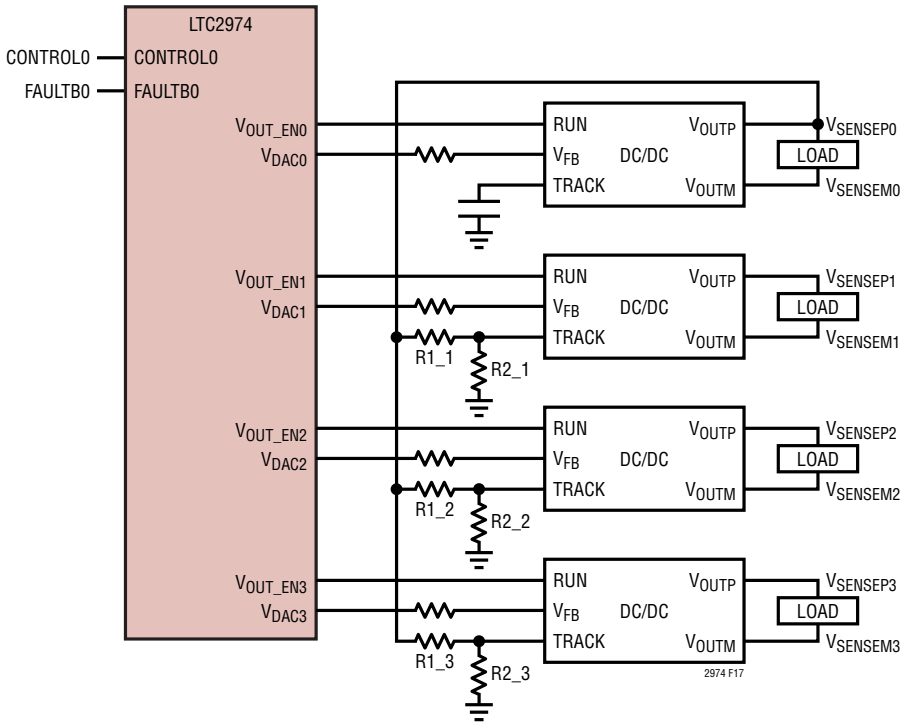


Figure 17. LTC2974 Configured to Control, Supervise and Monitor Power Supplies Equipped with Tracking Pin

PMBUS COMMAND DESCRIPTION

Tracking Supplies On and Off

The LTC2974 supports tracking power supplies that are equipped with a tracking pin and configured for tracking. A tracking power supply uses a secondary feedback terminal (TRACK) to allow its output voltage to be scaled to an external master voltage. Typically the external voltage is generated by the supply with the highest voltage in the system, which is fed to the slave track pins (see Figure 17). Supplies that track a master supply must be enabled before the master supply comes up and disabled after the master supply comes down. Enabling the slave supplies when the master is down requires supervisors monitoring the slaves to disable UV detection. Slave UC detection must also be

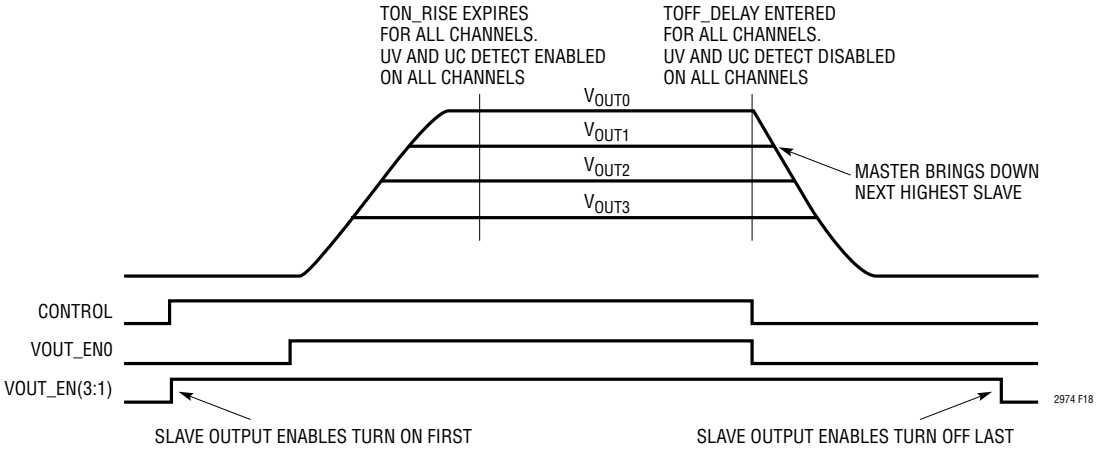


Figure 18. Control Pin Tracking All Supplies Up And Down

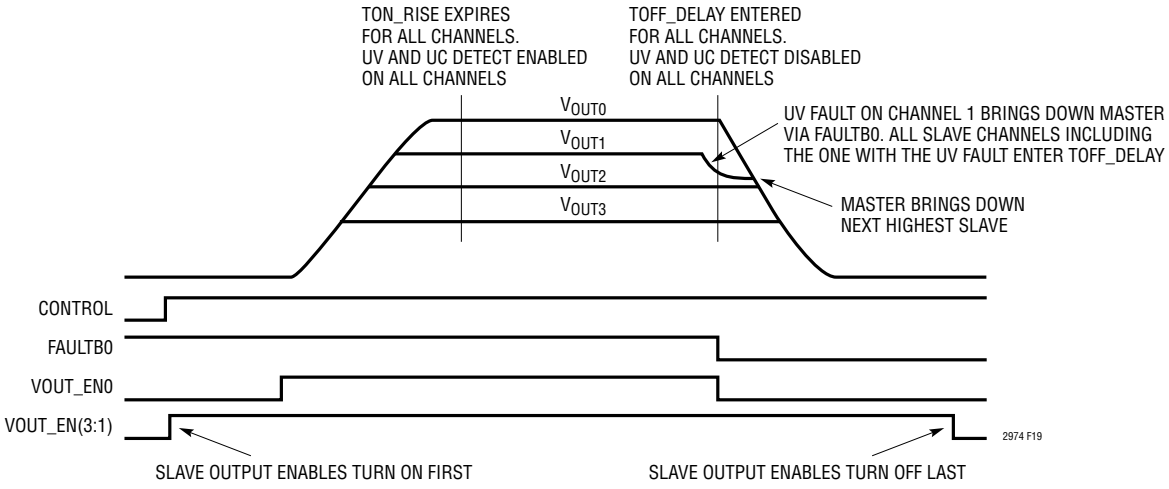


Figure 19. Fault on Channel 1 Tracking All Supplies Down

PMBUS COMMAND DESCRIPTION

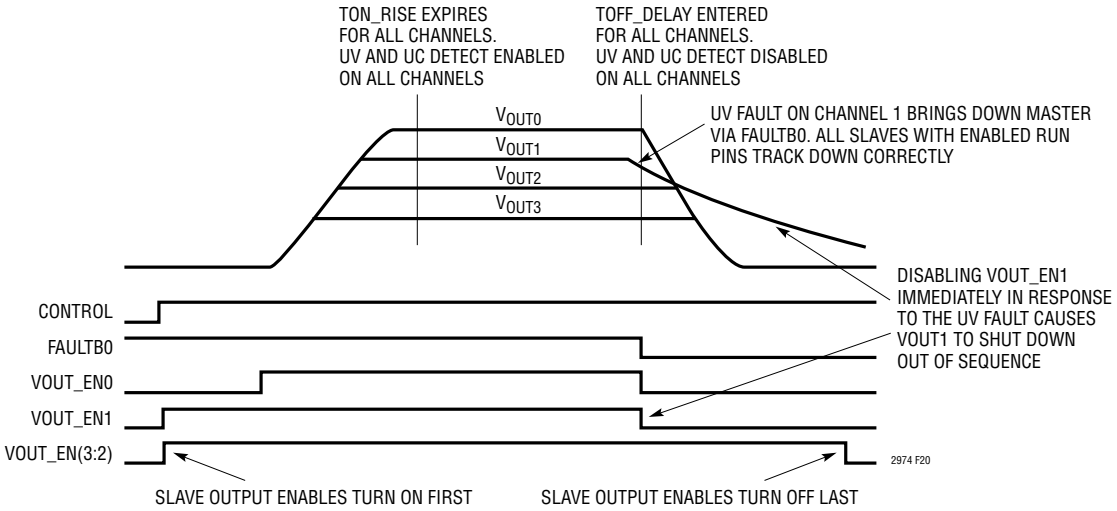


Figure 20. Improperly Configured Fault Response on Faulting Channel Disrupts Tracking

disabled when the slaves are tracking the master down to prevent false UC events. All channels configured for tracking must track off together in response to a fault on any channel or any other condition that can bring one or more of the channels down. Prematurely disabling a slave channel via its RUN pin may cause that channel to shut down out of sequence (see Figure 20)

An important feature of the LTC2974 is the ability to control, monitor and supervise DC/DC converters that are configured to track a master supply on and off.

The LTC2974 supports the following tracking features:

- Track channels on and off without issuing false UV/UC events when the slave channels are tracking up or down.
- Track channels down in response to a fault from a slave or master.
- Track channels down when VIN_SNS drops below VIN_OFF, share clock is held low or Restore_user_all is issued.
- Ability to reconfigure selected channels that are part of a tracking group to sequence up after the group has tracked up or sequence down before the group has tracked down.

Tracking Implementation

The LTC2974 supports tracking through the coordinated programing of Ton_delay, Ton_rise,Toff_delay and Mfr_track_en_chan*n*. The master channel must be configured to turn on after all the slave channels have turned on and to turn off before all the slave channels turn off. Slaves that are enabled before the master will remain off until the tracking pin allows them to turn on. Slaves will be turned off via the tracking pin even though their run pin is still asserted. Ton_rise must be extended on the slaves so that it ends relative to the rise of the TRACK pin and not the rise of the V_{OUT_EN} pin.

When Mfr_track_en_chan*n* is enabled the channel is reconfigured to:

- Sequence down on fault, VIN_OFF, SHARE_CLK low or RESTORE_USER_ALL.
- Ignore UV and UC during TOFF_DELAY. Note that ignoring UV and UC during TON_RISE and TON_MAX_FAULT always happens regardless of how this bit is set.

PMBUS COMMAND DESCRIPTION

The following example illustrates configuring an LTC2974 with one master channel and three slaves.

Master channel 0

TON_DELAY = Ton_delay_master

TON_RISE = Ton_rise_master

TOFF_DELAY = Toff_delay_master

Mfr_track_en_chan0 = 0

Slave channel *n*

TON_DELAY = Ton_delay_slave

TON_RISE = Ton_delay_master + Ton_rise_slave

TOFF_DELAY = Toff_delay_master + Toff_delay_slave

Mfr_track_en_chan0 = 1

Where:

Ton_delay_master – Ton_delay_slave > RUN to TRACK setup time

Toff_delay_slave > time for master supply to fall.

The system response to a control pin toggle is illustrated in Figure 18.

The system response to a UV fault on a slave channel is illustrated in Figure 19.

MFR_CONFIG_ALL_LTC2974

This command is used to configure parameters that are common to all channels on the IC. They may be set or reviewed from any PAGE setting.

MFR_CONFIG_ALL_LTC2974 Data Contents

BIT(S)	SYMBOL	OPERATION
b[15:12]	Reserved	Don't care. Always returns 0.
b[11]	Mfr_config_all_pwrgd_off_uses_uv	Selects PWRGD de-assertion source for all channels. 0: PWRGD is de-asserted based on V_{OUT} being below or equal to POWER_GOOD_OFF. This option uses the ADC. Response time is approximately 100ms to 200ms. 1: PWRGD is de-asserted based on V_{OUT} being below or equal to VOUT_UV_LIMIT. This option uses the high speed supervisor. Response time is approximately 12µs.
b[10]	Reserved	Don't care.
b[9]	Mfr_config_all_control3_pol	Selects active polarity of CONTROL3 pin 0: Active low (pull pin low to start unit). 1: Active high (pull pin high to start unit).
b[8]	Mfr_config_all_control2_pol	Selects active polarity of CONTROL2 pin 0: Active low (pull pin low to start unit). 1: Active high (pull pin high to start unit).

PMBUS COMMAND DESCRIPTION

MFR_CONFIG_ALL_LTC2974 Data Contents

BIT(S)	SYMBOL	OPERATION
b[7]	Mfr_config_all_fault_log_enable	Enable fault logging to EEPROM in response to Fault. 0: Fault logging to EEPROM is disabled. 1: Fault logging to EEPROM is enabled.
b[6]	Mfr_config_all_vin_on_clr_faults_en	Allow V_{IN} rising above VIN_ON to clear all latched faults. 0: VIN_ON clear faults feature is disabled. 1: VIN_ON clear faults feature is enabled.
b[5]	Mfr_config_all_control1_pol	Selects active polarity of CONTROL1 pin 0: Active low (pull pin low to start unit). 1: Active high (pull pin high to start unit).
b[4]	Mfr_config_all_control0_pol	Selects active polarity of CONTROL0 pin 0: Active low (pull pin low to start unit). 1: Active high (pull pin high to start unit).
b[3]	Mfr_config_all_vin_share_enable	Allow this unit to hold SHARE_CLK pin low when V_{IN} has not risen above VIN_ON or has fallen below VIN_OFF. When enabled this unit will also turn all channels off in response to Share-clock being held low. 0: SHARE_CLK inhibit is disabled. 1: SHARE_CLK inhibit is enabled.
b[2]	Mfr_config_all_pec_en	PMBus packet error checking enable. 0: PEC is accepted but not required. 1: PEC is enabled.
b[1]	Mfr_config_all_longer_pmbus_timeout	Increase PMBus timeout interval by a factor of 8. Recommended for fault logging. 0: PMBus timeout is not multiplied by a factor of 8. 1: PMBus timeout is multiplied by a factor of 8.
b[0]	Mfr_config_all_auxfaultb_wpu_dis	AUXFAULTB charge-pumped, current-limited pull-up disable. 0: Use weak current-limited pull-up on AUXFAULTB after power-up, as long as no faults have forced AUXFAULTB off. 1: Disable weak pull-up. AUXFAULTB driver is tri-stated after power-up as long as no faults have forced AUXFAULTB off.

PROGRAMMING USER EEPROM SPACE

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	EEPROM	DEFAULT VALUE	REF PAGE
STORE_USER_ALL	0x15	Store entire operating memory to EEPROM.	Send Byte	N				NA	45
RESTORE_USER_ALL	0x16	Restore entire operating memory from EEPROM.	Send Byte	N				NA	45
MFR_EE_UNLOCK	0xBD	Unlock user EEPROM for access by MFR_EE_ERASE and MFR_EE_DATA commands.	R/W Byte	N	Reg			NA	45
MFR_EE_ERASE	0xBE	Initialize user EEPROM for bulk programming by MFR_EE_DATA.	R/W Byte	N	Reg			NA	46
MFR_EE_DATA	0xBF	Data transferred to and from EEPROM using sequential PMBus word reads or writes. Supports bulk programming.	R/W Word	N	Reg			NA	46

PMBUS COMMAND DESCRIPTION

STORE_USER_ALL and RESTORE_USER_ALL

STORE_USER_ALL, RESTORE_USER_ALL commands provide access to User EEPROM space. Once a command is stored in User EEPROM, it will be restored with explicit restore command or when the part emerges from power-on reset after power is applied. While either of these commands is being processed, the part will indicate it is busy, see Response When Part Is Busy on page 47.

STORE_USER_ALL. Issuing this command will store all operating memory commands with a corresponding EEPROM memory location.

RESTORE_USER_ALL. Issuing this command will restore all commands from EEPROM Memory. It is recommended that this command not be executed while a unit is enabled since all monitoring is suspended while the EEPROM is transferred to operating memory, and intermediate values from EEPROM may not be compatible with the values initially stored in operating memory.

Bulk Programming the User EEPROM Space

The MFR_EE_UNLOCK, MFR_EE_ERASE and MFR_EE_DATA commands provide a method for 3rd party EEPROM programming houses and end users to easily program the LTC2974 independent of any order dependencies or delays between PMBus commands. All data transfers are directly to and from the EEPROM and do not affect the volatile RAM space currently configuring the device.

The first step is to program a master reference part with the desired configuration. MFR_EE_UNLOCK and MFR_EE_DATA are then used to read back all the data in User EEPROM space as sequential words. This information is stored to the master programming HEX file. Subsequent parts may be cloned to match the master part using MFR_EE_UNLOCK, MFR_EE_ERASE and MFR_EE_DATA to transfer data from the master HEX file. These commands operate directly on the EEPROM independent of the part configurations stored in RAM space. During EEPROM access the part will indicate that it is busy as described below.

In order to support simple programming fixtures the bulk programming features only uses PMBus word and byte commands. The MFR_UNLOCK configures the appropriate access mode and resets an internal address pointer allowing a series of word commands to behave as a block read or write with the address pointer being incremented after each operation. PEC use is optional and is configured by the MFR_EE_UNLOCK operation.

MFR_EE_UNLOCK

The MFR_EE_UNLOCK command prevents accidental EEPROM access in normal operation and configures the required EEPROM bulk programming mode for bulk initialization, sequential writes, or reads. MFR_EE_UNLOCK augments the protection provided by write protect. Upon unlocking the part for the required operation, an internal address pointer is reset allowing a series of MFR_EE_DATA reads or writes to sequentially transfer data, similar to a block read or block write. The MFR_EE_UNLOCK command can clear or set PEC mode based on the desired level of error protection. An MFR_EE_UNLOCK sequence consists of writing two or three unlock codes as described below. The following table documents the allowed sequences. Writing a non-supported sequence locks the part. Reading MFR_EE_UNLOCK returns the last byte written or zero if the part is locked.

PMBUS COMMAND DESCRIPTION

MFR_EE_UNLOCK Data Contents

BIT(S)	SYMBOL	OPERATION
b[7:0]	Mfr_ee_unlock[7:0]	To unlock user EEPROM space for Mfr_ee_erase and Mfr_ee_data read or write operations with PEC allowed: Write 0x2b followed by 0xd4. To unlock user EEPROM space for Mfr_ee_erase and Mfr_ee_data read or write operations with PEC required: Write 0x2b followed by 0xd5. To unlock user and manufacturer EEPROM space for Mfr_ee_data read only operations with PEC allowed: Write 0x2b, followed by 0x91 followed by 0xe4. To unlock user and manufacturer EEPROM space for Mfr_ee_data read only operations with PEC required: Write 0x2b, followed by 0x91 followed by 0xe5.

MFR_EE_ERASE

The MFR_EE_ERASE command is used to erase the entire contents of the user EEPROM space and configures this space to accept new program data. Writing values other than 0x2B will lock the part. Reads return the last value written.

MFR_EE_ERASE Data contents

BIT(S)	SYMBOL	OPERATION
b[7:0]	Mfr_ee_erase[7:0]	To erase the user EEPROM space and configure to accept new data: 1) Use the appropriate Mfr_ee_unlock sequence to configure for Mfr_ee_erase commands with or without PEC. 2) Write 0x2B to Mfr_ee_erase. The part will indicate it is busy erasing the EEPROM by the mechanism detailed below.

MFR_EE_DATA

The MFR_EE_DATA command allows the user to transfer data directly to or from the EEPROM without affecting RAM space.

To read the user EEPROM space issue the appropriate Mfr_ee_unlock command and perform Mfr_ee_data reads until the EEPROM has been completely read. Extra reads will lock the part and return zero. The first read returns the 16-bit EEPROM packing revision ID that is stored in ROM. The second read returns the number of 16-bit words available; this is the number of reads or writes to access all memory locations. Subsequent reads return EEPROM data starting with lowest address.

To write to the user EEPROM space issue the appropriate Mfr_ee_unlock and Mfr_ee_erase commands followed by successive Mfr_ee_data word writes until the EEPROM is full. Extra writes will lock the part. The first write is to the lowest address.

Mfr_ee_data reads and writes must not be mixed.

PMBUS COMMAND DESCRIPTION

MFR_EE_DATA Data Contents

BIT(S)	SYMBOL	OPERATION
b[15:0]	Mfr_ee_data[15:0]	To read user space 1) Use the appropriate Mfr_ee_unlock sequence to configure for Mfr_ee_data commands with or without PEC. 2) Read Mfr_ee_data[0] = PackingId (MFR Specific ID). 3) Read Mfr_ee_data[1] = NumberOfUserWords (total number of 16-bit word available). 4) Read Mfr_ee_data[2] through Mfr_ee_data[NumberOfWord+1] (User EEPROM data contents) To write user space 1) Initialize the user memory using the sequence described for the MFR_EE_ERASE command. 2) Use the appropriate Mfr_ee_unlock sequence to configure for Mfr_ee_data commands with or without PEC. 3) Write Mfr_ee_data[0] through Mfr_ee_data[NumberOfWord-1] (User EEPROM data content to be wriiten) The part will indicate it is busy erasing the EEPROM by the mechanism detailed below.

Response When Part Is Busy

The part will indicate it is busy accessing the EEPROM by the following mechanism:

1) Clearing Mfr_common_busyb of the MFR_COMMON register. This byte can always be read and will never NACK a byte read request even if the part is busy.

2) NACKing commands other than MFR_COMMON.

MFR_EE Erase and Write Programming Time

The program time per word is typically 0.17ms and will require spacing the I^2C/SMBus writes at greater than 0.17ms to guarantee the write has completed. The Mfr_ee_erase command takes approximately 400ms. We recommend using MFR_COMMON for handshaking.

INPUT VOLTAGE COMMANDS AND LIMITS

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	EEPROM	DEFAULT VALUE	REF PAGE
VIN_ON	0x35	Input voltage (V_{IN_SNS}) above which power conversion can be enabled.	R/W Word	N	L11	V	Y	10.0 0xD280	47
VIN_OFF	0x36	Input voltage (V_{IN_SNS}) below which power conversion is disabled. All $V_{OUT\_EN}n$ pins go off immediately or sequence off after TOFF_DELAY (See Mfr_track_en_chann).	R/W Word	N	L11	V	Y	9.0 0xD240	47
VIN_OV_FAULT_LIMIT	0x55	Input overvoltage fault limit measured at V_{IN_SNS} pin.	R/W Word	N	L11	V	Y	15.0 0xD3C0	47
VIN_OV_WARN_LIMIT	0x57	Input overvoltage warning limit measured at V_{IN_SNS} pin.	R/W Word	N	L11	V	Y	14.0 0xD380	47
VIN_UV_WARN_LIMIT	0x58	Input undervoltage warning limit measured at V_{IN_SNS} pin.	R/W Word	N	L11	V	Y	0 0x8000	47
VIN_UV_FAULT_LIMIT	0x59	Input undervoltage fault limit measured at V_{IN_SNS} pin.	R/W Word	N	L11	V	Y	0 0x8000	47

VIN_ON, VIN_OFF, VIN_OV_FAULT_LIMIT, VIN_OV_WARN_LIMIT, VIN_UV_WARN_LIMIT and VIN_UV_FAULT_LIMIT

These commands provide voltage supervising limits for the input voltage V_{IN_SNS}.

PMBUS COMMAND DESCRIPTION

OUTPUT VOLTAGE COMMANDS AND LIMITS

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	EEPROM	DEFAULT VALUE	REF PAGE
VOUT_MODE	0x20	Output voltage data format and mantissa exponent (2^{-13}).	R Byte	Y	Reg			0x13	48
VOUT_COMMAND	0x21	Servo target. Nominal DC/DC converter output voltage setpoint.	R/W Word	Y	L16	V	Y	1.0 0x2000	49
VOUT_MAX	0x24	Upper limit on the output voltage the unit can command regardless of any other commands.	R/W Word	Y	L16	V	Y	4.0 0x8000	49
VOUT_MARGIN_HIGH	0x25	Margin high DC/DC converter output voltage setting.	R/W Word	Y	L16	V	Y	1.05 0x219A	49
VOUT_MARGIN_LOW	0x26	Margin low DC/DC converter output voltage setting.	R/W Word	Y	L16	V	Y	0.95 0x1E66	49
VOUT_OV_FAULT_LIMIT	0x40	Output overvoltage fault limit.	R/W Word	Y	L16	V	Y	1.1 0x2333	49
VOUT_OV_WARN_LIMIT	0x42	Output overvoltage warning limit.	R/W Word	Y	L16	V	Y	1.075 0x2266	49
VOUT_UV_WARN_LIMIT	0x43	Output undervoltage warning limit.	R/W Word	Y	L16	V	Y	0.925 0x1D9A	49
VOUT_UV_FAULT_LIMIT	0x44	Output undervoltage fault limit. Used for Ton_max_fault and power good de-assertion.	R/W Word	Y	L16	V	Y	0.9 0x1CCD	49
POWER_GOOD_ON	0x5E	Output voltage at or above which a power good should be asserted.	R/W Word	Y	L16	V	Y	0.96 0x1EB8	49
POWER_GOOD_OFF	0x5F	Output voltage at or below which a power good should be de-asserted when Mfr_config_all_pwrgd_off_uses_uv is clear.	R/W Word	Y	L16	V	Y	0.94 0x1E14	49
MFR_VOUT_DISCHARGE_THRESHOLD	0xE9	Coefficient used to multiply VOUT_COMMAND in order to determine V_{OUT} off threshold voltage.	R/W Word	Y	L11		Y	2.0 0xC200	49
MFR_DAC	0xE0	The code of the 10-bit DAC.	R/W Word	Y	Reg			0x0000	49

VOUT_MODE

This command is read only and specifies the mode and exponent for all commands with a L16 data format. See Data Formats on page 28.

VOUT_MODE Data Contents

BIT(S)	SYMBOL	OPERATION
b[7:5]	Vout_mode_type	Reports linear mode. Hard-wired to 000b.
b[4:0]	Vout_mode_parameter	Linear mode exponent. 5-bit two's complement integer. Hardwired to 0x13 (–13 decimal).

PMBUS COMMAND DESCRIPTION

VOUT_COMMAND, VOUT_MAX, VOUT_MARGIN_HIGH, VOUT_MARGIN_LOW, VOUT_OV_FAULT_LIMIT, VOUT_OV_WARN_LIMIT, VOUT_UV_WARN_LIMIT, VOUT_UV_FAULT_LIMIT, POWER_GOOD_ON and POWER_GOOD_OFF

These commands provide various servo, margining and supervising limits for a channel's output voltage.

MFR_VOUT_DISCHARGE_THRESHOLD

This register contains the coefficient that multiplies VOUT_COMMAND in order to determine the OFF threshold voltage for the associated output. If the output voltage has not decayed below MFR_VOUT_DISCHARGE_THRESHOLD • VOUT_COMMAND prior to the channel being commanded to enter/re-enter the ON state, the Status_mfr_discharge bit in the STATUS_MFR_SPECIFIC register will be set and the ALERTB pin will be asserted low. In addition, the channel will not enter the ON state until the output has decayed below its off-threshold voltage. Setting this to a value greater than 1.0 effectively disables DISCHARGE_THRESHOLD checking, allowing the channel to turn back on even if it has not decayed at all.

Other channels can be held-off if a particular output has failed to discharge by using the bidirectional FAULTB*n* pins (refer to the MFR_FAULTB*n*_RESPONSE and MFR_FAULTB*n*_PROPOGATE registers).

MFR_DAC

This command register allows the user to directly program the 10-bit DAC. Manual DAC writes require the channel to be in the ON state,TON_RISE to have expired and MFR_CONFIG_LTC2974 b[5:4] = 10b or 11b. Writing MFR_CONFIG_LTC2974 b[5:4] = 10b commands the DAC to hard connect with the value in Mfr_dac_direct_val. Writing b[5:4] = 11b commands the DAC to soft-connect. Once the DAC has soft-connected, Mfr_dac_direct_val returns the value that allowed the DAC to be connected without perturbing the power supply. MFR_DAC writes are ignored when MFR_CONFIG_LTC2974 b[5:4] = 00b or 01b.

MFR_DAC Data Contents

BIT(S)	SYMBOL	OPERATION
b[15:10]	Reserved	Read only, always returns 0.
b[9:0]	Mfr_dac_direct_val	DAC code value.

PMBUS COMMAND DESCRIPTION

OUTPUT CURRENT COMMANDS AND LIMITS

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	EEPROM	DEFAULT VALUE	REF PAGE
IOUT_CAL_GAIN	0x38	The nominal resistance of the current sense element in mΩ.	R/W Word	Y	L11	mΩ	Y	1.0 0xBA00	50
IOUT_OC_FAULT_LIMIT	0x46	Output overcurrent fault limit.	R/W Word	Y	L11	A	Y	10.0 0xD280	51
IOUT_OC_WARN_LIMIT	0x4A	Output overcurrent warning limit.	R/W Word	Y	L11	A	Y	5.0 0xCA80	51
IOUT_UC_FAULT_LIMIT	0x4B	Output undercurrent fault limit. Used to detect a reverse current and must be a negative value.	R/W Word	Y	L11	A	Y	-1.0 0xB400	51
MFR_IOUT_CAL_GAIN_TC	0xF6	Temperature coefficient applied to IOUT_CAL_GAIN.	R/W Word	Y	CF	ppm	Y	0x0000	51

IOUT_CAL_GAIN

The IOUT_CAL_GAIN command is used to set the ratio of the voltage at the current sense pins to the sensed current. For devices using a fixed current sense resistor, it is the same value as the resistance of the resistor (units are expressed in mΩ). IOUT_CAL_GAIN is internally limited to values between 0.01mΩ to 1,000mΩ. The register readback value always returns what was last written and does not reflect internal limiting.

Calculations using IOUT_CAL_GAIN are:

$$V_{IOUT\_OC\_FAULT\_LIMIT} = IOUT\_OC\_FAULT\_LIMIT \bullet IOUT\_CAL\_GAIN \bullet T_{CORRECTION}$$

$$V_{IOUT\_UC\_FAULT\_LIMIT} = IOUT\_UC\_FAULT\_LIMIT \bullet IOUT\_CAL\_GAIN \bullet T_{CORRECTION}$$

Where:

$$T_{CORRECTION} = (1 + MFR\_IOUT\_CAL\_GAIN\_TC \bullet 1E\text{-}6 \bullet (READ\_TEMPERATURE\_1 + MFR\_T\_SELF\_HEAT - 25.0))$$

$$READ\_IOUT = \frac{V_{IOUT\_SNSPn} - V_{IOUT\_SNSMn}}{(IOUT\_CAL\_GAIN) \bullet T_{CORRECTION}}$$

Note:

$T_{CORRECTION}$ is limited by hardware to a value between 0.25 and 4.0.

READ_TEMPERATURE_2 is substituted for READ_TEMPERATURE_1 if the associated T_{SENSE} network fails to detect a valid temperature. See READ_TEMPERATURE_1 for more information.

PMBUS COMMAND DESCRIPTION

IOUT_OC_FAULT_LIMIT, IOUT_OC_WARN_LIMIT and IOUT_UC_FAULT_LIMIT

I_{OUT} supervisor fault and warning limits.

IOUT_OC_FAULT_LIMIT is internally limited to values greater or equal to zero. The register readback value always returns what was last written and does not reflect internal limiting.

IOUT_UC_FAULT_LIMIT is internally limited to values less than zero. The register readback value always returns what was last written and does not reflect internal limiting.

MFR_IOUT_CAL_GAIN_TC

The MFR_IOUT_CAL_GAIN_TC is a paged command that sets the temperature coefficient of the IOUT_CAL_GAIN register value in ppm/°C. This command uses the temperature measured by the external temperature diode for the associated page.

Refer to IOUT_CAL_GAIN for details on proper usage.

MFR_IOUT_CAL_GAIN_TC Data Contents

BIT(S)	SYMBOL	OPERATION
b[15:0]	Mfr_iout_cal_gain_tc	16-bit twos complement integer representing the temperature coefficient. Value = Y where Y = b[15:0] is a twos complement. Example: Mfr_iout_cal_gain_tc = 3900ppm For b[15:0] = 0x0F3C Value = 3900

PMBUS COMMAND DESCRIPTION

EXTERNAL TEMPERATURE COMMANDS AND LIMITS

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	EEPROM	DEFAULT VALUE	REF PAGE
OT_FAULT_LIMIT	0x4F	Overtemperature fault limit for the external temperature sensor.	R/W Word	Y	L11	°C	Y	65.0 0xEA08	52
OT_WARN_LIMIT	0x51	Overtemperature warning limit for the external temperature sensor	R/W Word	Y	L11	°C	Y	60.0 0xE3C0	52
UT_WARN_LIMIT	0x52	Undertemperature warning limit for the external temperature sensor.	R/W Word	Y	L11	°C	Y	0 0x8000	52
UT_FAULT_LIMIT	0x53	Undertemperature fault limit for the external temperature sensor.	R/W Word	Y	L11	°C	Y	–5.0 0xCD80	52
MFR_TEMP_1_GAIN	0xF8	Inverse of external diode temperature non ideality factor. One LSB = 2^{-14}.	R/W Word	Y	CF		Y	1 0x4000	52
MFR_TEMP_1_OFFSET	0xF9	Offset value for the external temperature.	R/W Word	Y	L11	°C	Y	0 0x8000	52
MFR_T_SELF_HEAT	0xB8	Calculated temperature rise due to self-heating of output current sense device above value measured by external temperature sensor.	R Word	Y	L11	°C		NA	53
MFR_IOUT_CAL_GAIN_TAU_INV	0xB9	Inverse of time constant for Mfr_t_self_heat changes scaled by 4 • tCONV_SENSE.	R/W Word	Y	L11		Y	0.0 0x8000	53
MFR_IOUT_CAL_GAIN_THETA	0xBA	Thermal resistance from inductor core to point measured by external temperature sensor.	R/W Word	Y	L11	°C/W	Y	0.0 0x8000	53

OT_FAULT_LIMIT, OT_WARN_LIMIT, UT_WARN_LIMIT and UT_FAULT_LIMIT

These commands provide supervising limits for temperature as measured by the external diode.

MFR_TEMP_1_GAIN and MFR_TEMP_1_OFFSET

The MFR_TEMP_1_GAIN command specifies the inverse of the temperature sensor ideality factor. The MFR_TEMP_1_OFFSET allows an offset to be applied to the measured temperature.

Calculations using these paged commands are:

READ_TEMPERATURE_1 = T_{EXT} • MFR_TEMP_1_GAIN – 273.15 + MFR_TEMP_1_OFFSET

Where:

T_{EXT} = Measured external temperature in degrees Kelvin.

READ_TEMPERATURE_2 is substituted for READ_TEMPERATURE_1 if the associated T_{SENSE} network fails to detect a valid temperature. Under these conditions MFR_TEMP1_GAIN and MFR_TEMP1_OFFSET will have no effect. See READ_TEMPERATURE_1 for more information.

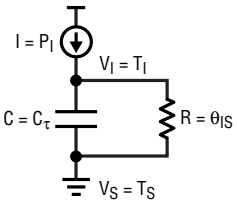
MFR_TEMP_1_GAIN Data Contents

BIT(S)	SYMBOL	OPERATION
b[15:0]	Mfr_temp_1_gain[15:0]	16-bit integer representing inverse of temperature non-ideality factor. Value = Y • 2^{14} where Y = b[15:0] is an unsigned integer. Example: MFR_TEMP_1_GAIN = 1.0 For b[15:0] = 0x4000 Value = 16384 • 2^{-14} = 1.0

PMBUS COMMAND DESCRIPTION

MFR_T_SELF_HEAT, MFR_IOUT_CAL_GAIN_TAU_INV and MFR_IOUT_CAL_GAIN_THETA

The LTC2974 uses an innovative (patent pending) algorithm to dynamically model the temperature rise from the external temperature sensor to the inductor core. This temperature rise is called MFR_T_SELF_HEAT and is used to calculate the final temperature correction required by IOUT_CAL_GAIN. The temperature rise is a function of the power dissipated in the inductor DCR, the thermal resistance from the inductor core to the remote temperature sensor and the thermal time constant of the inductor to board system. The algorithm simplifies the placement requirements for the external temperature sensor and compensates for the significant steady state and transient temperature error from the inductor core to the primary inductor heat sink.



P_I = CURRENT REPRESENTING THE POWER DISSIPATED BY THE INDUCTOR (V_{DCR} • READ_IOUT WHERE $V_{DCR} = (V_{ISENSEP} – V_{ISENSM})$)

C_τ = CAPACITANCE REPRESENTING THERMAL HEAT CAPACITY OF THE INDUCTOR (INCLUDED IN MFR_IOUT_CAL_GAIN_TAU_INV)

T_I = VOLTAGE REPRESENTING THE TEMPERATURE OF THE INDUCTOR

θ_{IS} = RESISTANCE REPRESENTING THE THERMAL RESISTANCE FROM THE DCR TO THE REMOTE TEMPERATURE SENSOR (MFR_IOUT_CAL_GAIN_THETA)

T_S = VOLTAGE REPRESENTING THE TEMPERATURE AT THE REMOTE TEMPERATURE SENSOR

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Figure 21. Electronic Analogy for Inductor Temperature Model

The best way to understand the self-heating effect inside the inductor is to model the system using the circuit analogy of Figure 21. The 1st order differential equation for the above model may be approximated by the following difference equation:

$$P_I – T_I/\theta_{IS} = C_\tau\ \Delta T_I/\Delta t \text{ (Eq1) (when } T_S = 0)$$

from which:

$$\Delta T_I = \Delta t\ (P_I\ \theta_{IS} – T_I)/(\theta_{IS}\ C_\tau) \text{ (Eq2) or}$$

$$\Delta T_I = (P_I\ \theta_{IS} – T_I) \bullet \tau_{INV} \text{ (Eq3)}$$

where

$$\tau_{INV} = \Delta t/(\theta_{IS}\ C_\tau) \text{ (Eq4)}$$

and Δt is the sample period of the external temperature ADC.

The LTC2974 implements the self-heating algorithm using Eq3 and Eq4 where:

ΔT_I = ΔMFR_T_SELF_HEAT

P_I = READ_IOUT • ($V_{ISENSEP} – V_{ISENSEM}$)

T_S = READ_TEMPERATURE_1

T_I = MFR_T_SELF_HEAT + T_S

$\Delta t = 4 \bullet t_{CONV\_SENSE}$. (One complete external temperature loop period)

τ_{INV} = MFR_IOUT_CAL_GAIN_TAU_INV

θ_{IS} = MFR_IOUT_CAL_GAIN_THETA

PMBUS COMMAND DESCRIPTION

Initially self heat is set to zero. After each temperature measurement self heat is updated to be the previous value of self heat incremented or decremented by ΔMFR_T_SELF_HEAT.

The actual value of C_τ is not required. The important quantity is the thermal time constant $\tau_{INV} = (\theta_{IS}\ C_\tau)$. For example, if an inductor has a thermal time constant τ_{INV} = 5 seconds then:

MFR_IOUT_CAL_GAIN_TAU_INV = $(4 \bullet t_{CONV\_SENSE})/5 = 4 \bullet 66ms/5s = 0.0528$

Refer to the application section for more information on calibrating θ_{IS} and τ_{INV}.

READ_TEMPERATURE_2 is substituted for READ_TEMPERATURE_1 if the associated T_{SENSE} network fails to detect a valid temperature. Under these conditions T_S = READ_TEMPERATURE_2 and the self-heating correction is applied using the internal die temperature. See READ_TEMPERATURE_1 for more information.

MFR_T_SELF_HEAT Data Content

Bit(s)	Symbol	Operation
b[15:0]	Mfr_t_self_heat	Values are limited to the range 0°C to 50°C.

MFR_IOUT_CAL_GAIN_THETA Data Content

Bit(s)	Symbol	Operation
b[15:0]	Mfr_iout_cal_gain_theta	Values ≤ 0 set MFR_T_SELF_HEAT to zero.

MFR_IOUT_CAL_GAIN_TAU_INV Data Content

Bit(s)	Symbol	Operation
b[15:0]	Mfr_iout_cal_gain_tau_inv	Values ≤ 0 set MFR_T_SELF_HEAT to zero. Values ≥ 1 set MFR_T_SELF_HEAT to MFR_IOUT_CAL_GAIN_THETA • READ_IOUT • ($V_{ISENSEP} – V_{ISENSEM}$).

PMBUS COMMAND DESCRIPTION

SEQUENCING TIMING LIMITS AND CLOCK SHARING

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	EEPROM	DEFAULT VALUE	REF PAGE
TON_DELAY	0x60	Time from CONTROL pin and/or OPERATION command = ON to $V_{OUT\_EN}n$ pin = ON.	R/W Word	Y	L11	ms	Y	1.0 0xBA00	55
TON_RISE	0x61	Time from when the $V_{OUT\_EN}n$ pin goes high until the LTC2974 optionally soft-connects its DAC and begins to servo the output voltage to the desired value.	R/W Word	Y	L11	ms	Y	10.0 0xD280	55
TON_MAX_FAULT_LIMIT	0x62	Maximum time from $V_{OUT\_EN}n$ = ON assertion that an UV condition will be tolerated before a TON_MAX_FAULT condition results.	R/W Word	Y	L11	ms	Y	15.0 0xD3C0	55
TOFF_DELAY	0x64	Time from CONTROL pin and/or OPERATION command = OFF to $V_{OUT\_EN}n$ pin = OFF.	R/W Word	Y	L11	ms	Y	1.0 0xBA00	55
MFR_RESTART_DELAY	0xDC	Delay from actual CONTROL active edge to virtual CONTROL active edge.	R/W Word	N	L11	ms	Y	400 0xFB20	55

TON_DELAY, TON_RISE, TON_MAX_FAULT_LIMIT and TOFF_DELAY

These commands share the same format and provide sequencing and timer fault and warning delays in ms.

TON_DELAY sets the amount of time in milliseconds that a channel waits following the start of an ON sequence before its V_{OUT_EN} pin enables a DC/DC converter. This delay is counted using SHARE_CLK only.

TON_RISE sets the amount of time in ms that elapses after the power supply has been enabled until the LTC2974's DAC soft-connects and servos the output voltage to the desired level if Mfr_dac_mode = 00b. This delay is counted using SHARE_CLK only.

TON_MAX_FAULT_LIMIT is the maximum amount of time that the power supply being controlled by the LTC2974 can attempt to power up the output without reaching the VOUT_UV_FAULT_LIMIT. If it does not, then a TON_MAX_FAULT is declared. If the output reaches VOUT_UV_FAULT_LIMIT prior to TON_MAX_FAULT_LIMIT, the LTC2974 unmasks the VOUT_UV_FAULT_LIMIT threshold. (Note that a value of zero means there is no limit to how long the power supply can attempt to bring up its output voltage.) This delay is counted using SHARE_CLK only.

TOFF_DELAY is the amount of time that elapses after the CONTROL pin and/or OPERATION command is de-asserted until the channel is disabled (soft-off). This delay is counted using SHARE_CLK if available, otherwise the internal oscillator is used.

All of the above TON and TOFF delays are internally limited to 655ms, and rounded to the nearest 10µs. The read value of these commands always returns what was last written and does not reflect internal limiting.

MFR_RESTART_DELAY

This command essentially sets the off time of a CONTROL pin initiated restart. If the CONTROL pin is toggled off for at least 10µs then on, all dependent channels are disabled, held off for a time = Mfr_restart_delay, then sequenced back on. CONTROL pin transitions whose OFF time exceeds Mfr_restart_delay are not affected by this command. A value of all zeros disables this feature. This delay is counted using SHARE_CLK only.

This delay is internally limited to 13.1 seconds, and rounded to the nearest 200µs. The read value of this command always returns what was last written and does not reflect internal limiting.

PMBUS COMMAND DESCRIPTION

Clock Sharing

Multiple LTC PMBus devices can synchronize their clocks in an application by connecting together the open-drain SHARE_CLK input/outputs to a pull-up resistor as a wired OR. In this case the fastest clock will take over and synchronize all other chips to its falling edge.

SHARE_CLK can optionally be used to synchronize ON/OFF dependency on V_{IN} across multiple chips by setting the Mfr_config_all_vin_share_enable bit of the MFR_CONFIG_ALL register. When configured this way the chip will hold SHARE_CLK low when the unit is off for insufficient input voltage, and upon detecting that SHARE_CLK is held low the chip will disable all channels after a brief deglitch period. When the SHARE_CLK pin is allowed to rise, the chip will respond by beginning a start sequence. In this case the slowest VIN_ON detection will take over and synchronize other chips to its start sequence.

WATCHDOG TIMER AND POWER GOOD

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	EEPROM	DEFAULT VALUE	REF PAGE
MFR_PWRGD_EN	0xD4	Configuration that maps WDI/RESETB status and individual channel power good to the PWRGD pin.	R/W Word	N	Reg		Y	0x0000	56
MFR_POWERGOOD_ASSERTION_DELAY	0xE1	Power-good output assertion delay.	R/W Word	N	L11	ms	Y	100 0xEB20	57
MFR_WATCHDOG_T_FIRST	0xE2	First watchdog timer interval.	R/W Word	N	L11	ms	Y	0 0x8000	57
MFR_WATCHDOG_T	0xE3	Watchdog timer interval.	R/W Word	N	L11	ms	Y	0 0x8000	57

MFR_PWRGD_EN

This command register controls the mapping of the watchdog and channel power good status to the PWRGD pin.

MFR_PWRGD_EN Data Contents

BIT(S)	SYMBOL	OPERATION
b[15:9]	Reserved	Read only, always returns 0s.
b[8]	Mfr_pwrgd_en_wdog	Watchdog. 1 = Watchdog timer not-expired status is ANDed with PWRGD status for any similarly enabled channels to determine when the PWRGD pin gets asserted. 0 = Watchdog timer does not affect the PWRGD pin.
b[7:4]	Reserved	Always returns 0000b.
b[3]	Mfr_pwrgd_en_chan3	Channel 3. 1 = PWRGD status for this channel is ANDed with PWRGD status for any similarly enabled channels to determine when the PWRGD pin gets asserted. 0 = PWRGD status for this channel does not affect the PWRGD pin.
b[2]	Mfr_pwrgd_en_chan2	Channel 2. 1 = PWRGD status for this channel is ANDed with PWRGD status for any similarly enabled channels to determine when the PWRGD pin gets asserted. 0 = PWRGD status for this channel does not affect the PWRGD pin.

PMBUS COMMAND DESCRIPTION

b[1]	Mfr_pwrgd_en_chan1	Channel 1. 1 = PWRGD status for this channel is ANDed with PWRGD status for any similarly enabled channels to determine when the PWRGD pin gets asserted. 0 = PWRGD status for this channel does not affect the PWRGD pin.
b[0]	Mfr_pwrgd_en_chan0	Channel 0. 1 = PWRGD status for this channel is ANDed with PWRGD status for any similarly enabled channels to determine when the PWRGD pin gets asserted. 0 = PWRGD status for this channel does not affect the PWRGD pin.

MFR_POWERGOOD_ASSERTION_DELAY

This command register allows the user to program the delay from when the internal power-good signal becomes valid until the power-good output is asserted. This delay is counted using SHARE_CLK if available, otherwise the internal oscillator is used. This delay is internally limited to 13.1 seconds, and rounded to the nearest 200µs. The read value of this command always returns what was last written and does not reflect internal limiting.

The power good de-assertion delay and threshold source is controlled by Mfr_config_all_pwrgd_off_uses_uv. Systems that require a fast power good de-assertion should set Mfr_config_all_pwrgd_off_uses_uv=1. This uses the VOUT_UV_FAULT_LIMIT and the high speed comparator to de-assert the PWRGD pin. Systems that require a separate power good off threshold should set Mfr_config_all_pwrgd_off_uses_uv=0. This uses the slower ADC polling loop and POWER_GOOD_OFF to de-assert the PWRGD pin.

Watchdog Operation

A non-zero write to the MFR_WATCHDOG_T register will reset the watchdog timer. Low-to-high transitions on the WDI/RESETB pin also reset the watchdog timer. If the timer expires, ALERTB is asserted and the PWRGD output is optionally de-asserted and then reasserted after MFR_PWRGD_ASSERTION_DELAY ms. Writing 0 to either the MFR_WATCH_DOG_T or MFR_WATCHDOG_T_FIRST registers will disable the timer.

MFR_WATCHDOG_T_FIRST and MFR_WATCHDOG_T

The MFR_WATCHDOG_T_FIRST register allows the user to program the duration of the first watchdog timer interval following assertion of the PWRGD pin, assuming the PWRGD pin reflects the status of the watchdog timer. If assertion of PWRGD is not conditioned by the watchdog timer's status, then MFR_WATCHDOG_T_FIRST applies to the first timing interval after the timer is enabled. Writing a value of 0ms to the MFR_WATCHDOG_T_FIRST register disables the watchdog timer. This delay is internally limited to 65 seconds and rounded to the nearest 1ms.

The MFR_WATCHDOG_T register allows the user to program watchdog timer intervals subsequent to the MFR_WATCHDOG_T_FIRST timing interval. Writing a value of 0ms to the MFR_WATCHDOG_T register disables the watchdog timer. This delay is internally limited to 655ms and rounded to the nearest 10µs.

Both timers operate on an internal clock independent of SHARE_CLK. The read value of both commands always returns what was last written and does not reflect internal limiting.

PMBUS COMMAND DESCRIPTION

FAULT RESPONSES

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	EEPROM	DEFAULT VALUE	REF PAGE
VOUT_OV_FAULT_RESPONSE	0x41	Action to be taken by the device when an output overvoltage fault is detected.	R/W Byte	Y	Reg		Y	0x80	59
VOUT_UV_FAULT_RESPONSE	0x45	Action to be taken by the device when an output undervoltage fault is detected.	R/W Byte	Y	Reg		Y	0x7F	59
IOUT_OC_FAULT_RESPONSE	0x47	Action to be taken by the device when an output overcurrent fault is detected.	R/W Byte	Y	Reg		Y	0x00	60
IOUT_UC_FAULT_RESPONSE	0x4C	Action to be taken by the device when an output undercurrent fault is detected.	R/W Byte	Y	Reg		Y	0x00	60
OT_FAULT_RESPONSE	0x50	Action to be taken by the device when an overtemperature fault is detected on the external temperature sensor.	R/W Byte	Y	Reg		Y	0xB8	61
UT_FAULT_RESPONSE	0x54	Action to be taken by the device when an undertemperature fault is detected on the external temperature sensor.	R/W Byte	Y	Reg		Y	0xB8	61
VIN_OV_FAULT_RESPONSE	0x56	Action to be taken by the device when an input overvoltage fault is detected.	R/W Byte	N	Reg		Y	0x80	61
VIN_UV_FAULT_RESPONSE	0x5A	Action to be taken by the device when an input undervoltage fault is detected.	R/W Byte	N	Reg		Y	0x00	61
TON_MAX_FAULT_RESPONSE	0x63	Action to be taken by the device when a TON_MAX_FAULT event is detected.	R/W Byte	Y	Reg		Y	0xB8	62
MFR_RETRY_DELAY	0xDB	Retry interval during FAULT retry mode.	R/W Word	N	L11	ms	Y	200 0xF320	62
MFR_RETRY_COUNT	0xF7	Retry count for all faulted off conditions that enable retry.	R/W Byte	N	Reg		Y	0x07	62

Clearing Latched Faults

Latched faults are reset by toggling the CONTROL pin, using the OPERATION command, or removing and reapplying the bias voltage to the V_{IN_SNS} pin. All fault and warning conditions result in the ALERTB pin being asserted low and the corresponding bits being set in the status registers. The CLEAR_FAULTS command resets the contents of the status registers and de-asserts the ALERTB output. The CLEAR_FAULTS does not clear a faulted off state nor allow a channel to turn back on.

PMBUS COMMAND DESCRIPTION

VOUT_OV_FAULT_RESPONSE and VOUT_UV_FAULT_RESPONSE

The fault response documented here is for voltages that are measured by the high speed supervisor. These voltages are measured over a short period of time and may require a deglitch period. Note that in addition to the response described by these commands, the LTC2974 will also:

- Set the appropriate bit(s) in the STATUS_BYTE.
- Set the appropriate bit(s) in the STATUS_WORD.
- Set the appropriate bit in the corresponding STATUS_VOUT register, and
- Notify the host by pulling the ALERTB pin low.

VOUT_OV_FAULT_RESPONSE and VOUT_UV_FAULT_RESPONSE Data Contents

BIT(S)	SYMBOL	OPERATION
b[7:6]	Vout_ov_fault_response_action, Vout_uv_fault_response_action	Response action: 00b: The unit continues operation without interruption. 01b: The unit continues operating for the delay time specified by bits[2:0] in increments of t_{S_VS}. See Electrical Characteristics Table. If the fault is still present at the end of the delay time, the unit shuts down immediately or sequences off after TOFF_DELAY (See Mfr_track_en_chann). After shutting down, the device responds according to the retry settings in bits [5:3]. 10b-11b: The unit shuts down immediately or sequences off after TOFF_DELAY (See Mfr_track_en_chann). After shutting down, the device responds according to the retry settings in bits [5:3].
b[5:3]	Vout_ov_fault_response_retry, Vout_uv_fault_response_retry	Response retry behavior: 000b: A zero value for the retry setting means that the unit does not attempt to restart. The output remains disabled until the fault is cleared. 001b-111b: The PMBus device attempts to restart the number of times specified by the global Mfr_retry_count[2:0] until it is commanded OFF (by the CONTROL pin or OPERATION command or both), bias power is removed, or another fault condition causes the unit to shut down. Changing the value might not take effect until the next off-then-on sequence on that channel.
b[2:0]	Vout_ov_fault_response_delay, Vout_uv_fault_response_delay	This sample count determines the amount of time a unit is to ignore a fault after it is first detected. Use this delay to deglitch fast faults. 000b: There is no additional deglitch delay applied to fault detection. 001b-111b: The fault is deglitched for deglitch period of b[2:0] samples at a sampling period of tS_VS (12.2µs typical).

PMBUS COMMAND DESCRIPTION

IOUT_OC_FAULT_RESPONSE and IOUT_UC_FAULT_RESPONSE

The fault response documented here is for currents that are measured by the high speed supervisor. These currents are measured over a short period of time and may require a deglitch period. Note that in addition to the response described by these commands, the LTC2974 will also:

- Set the appropriate bit in the STATUS_BYTE.
- Set the appropriate bit in the STATUS_WORD.
- Set the appropriate bit in the corresponding STATUS_IOUT register, and
- Notify the host by pulling the ALERTB pin low.

IOUT_OC_FAULT_RESONSE and IOUT_UC_FAULT_RESPONSE Data Contents

<table>
<tr><th>BIT(S)</th><th>SYMBOL</th><th>OPERATION</th></tr>
<tr><td>b[7:6]</td><td>Iout_oc_fault_response_action,
Iout_uc_fault_response_action</td><td>Response action:
00b and 01b: The unit continues operation without interruption. Note that the current will not be limited to the value of Iout_oc_fault_limit or Iout_uc_fault_limit.
10b: The unit continues operating for the delay time specified by bits [2:0]. If the fault is still present at the end of the delay time, the unit shuts down immediately or sequences off after TOFF_DELAY (See Mfr_track_en_chann). After shutting down, the device responds according to the retry settings in bits [5:3]. Note that the current will not be limited to the value of Iout_oc_fault_limit or Iout_uc_fault_limit.
11b: The unit shuts down immediately or sequences off after TOFF_DELAY (See Mfr_track_en_chann). After shutting down, the device responds according to the retry settings in bits [5:3].</td></tr>
<tr><td>b[5:3]</td><td>Iout_oc_fault_response_retry,
Iout_uc_fault_response_retry</td><td>Response retry behavior:
000b: A zero value for the retry setting means that the unit does not attempt to restart. The output remains disabled until the fault is cleared.
001-111b: The PMBus device attempts to restart the number of times specified by the global Mfr_retry_count[2:0] until it is commanded off (by the control pin or operation command or both), bias power is removed, or another fault condition causes the unit to shut down.
Changing the value might not take effect until the next off-then-on sequence on that channel.</td></tr>
<tr><td>b[2:0]</td><td>Iout_oc_fault_response_delay,
Iout_uc_fault_response_delay</td><td>This sample count determines the amount of time a unit is to ignore a fault after it is first detected. Use this delay to deglitch fast faults.
000b: There is no additional deglitch delay applied to fault detection.
001b-111b: The fault is deglitched for the interval selected by b[2:0] as follows.
<table>
<tr><th>b[2:0]</th><th>Deglitch interval</th></tr>
<tr><td>001b</td><td>100µs</td></tr>
<tr><td>010b</td><td>1ms</td></tr>
<tr><td>011b</td><td>5ms</td></tr>
<tr><td>100b</td><td>10ms</td></tr>
<tr><td>101b</td><td>20ms</td></tr>
<tr><td>110b</td><td>50ms</td></tr>
<tr><td>111b</td><td>100ms</td></tr>
</table>
</td></tr>
</table>

PMBUS COMMAND DESCRIPTION

OT_FAULT_RESPONSE, UT_FAULT_RESPONSE, VIN_OV_FAULT_RESPONSE and VIN_UV_FAULT_RESPONSE

The fault response documented here is for values that are measured by the ADC. Note that in addition to the response described by these commands, the LTC2974 will also:

- Set the appropriate bit(s) in the STATUS_BYTE.
- Set the appropriate bit(s) in the STATUS_WORD.
- Set the appropriate bit in the corresponding STATUS_VIN or STATUS_TEMPERATURE register, and
- Notify the host by pulling the ALERTB pin low.

OT_FAULT_RESPONSE, UT_FAULT_RESPONSE, VIN_OV_FAULT_RESPONSE, VIN_UV_FAULT_RESPONSE Data Contents

BIT(S)	SYMBOL	OPERATION
b[7:6]	Ot_fault_response_action, Ut_fault_response_action, Vin_ov_fault_response_action, Vin_uv_fault_response_action	Response action: 00b: The unit continues operation without interruption. 01b-11b: The unit shuts down immediately or sequences off after TOFF_DELAY (See Mfr_track_en_chann). After shutting down, the device responds according to the retry settings in bits [5:3].
b[5:3]	Ot_fault_response_retry, Ut_fault_response_retry, Vin_ov_fault_response_retry, Vin_uv_fault_response_retry	Response retry behavior: 000b: A zero value for the retry setting means that the unit does not attempt to restart. The output remains disabled until the fault is cleared. 001b-111b: The PMBus device attempts to restart the number of times specified by the global Mfr_retry_count[2:0] until it is commanded OFF (by the CONTROL pin or OPERATION command or both), bias power is removed, or another fault condition causes the unit to shut down. Changing the value might not take effect until the next off-then-on sequence on that channel.
b[2:0]	Ot_fault_response_delay, Ut_fault_response_delay, Vin_ov_fault_response_delay, Vin_uv_fault_response_delay	Hard coded to 000b: There is no additional deglitch delay applied to fault detection.

PMBUS COMMAND DESCRIPTION

TON_MAX_FAULT_RESPONSE

This command defines the LTC2974 response to a TON_MAX_FAULT. It may be used to protect against a short-circuited output at startup. After startup use VOUT_UV_FAULT_RESPONSE to protect against a short-circuited output.

The device also:

- Sets the HIGH_BYTE bit in the STATUS_BYTE,
- Sets the VOUT bit in the STATUS_WORD,
- Sets the TON_MAX_FAULT bit in the STATUS_VOUT register, and
- Notifies the host by asserting ALERTB.

TON_MAX_FAULT_RESPONSE Data Contents

BIT(S)	SYMBOL	OPERATION
b[7:6]	Ton_max_fault_response_action	Response action: 00b: The unit continues operation without interruption. 01b-11b: The unit shuts down immediately or sequences off after TOFF_DELAY (See Mfr_track_en_chann). After shutting down, the device responds according to the retry settings in bits [5:3].
b[5:3]	Ton_max_fault_response_retry	Response retry behavior: 000b: A zero value for the retry setting means that the unit does not attempt to restart. The output remains disabled until the fault is cleared. 001b-111b: The PMBus device attempts to restart the number of times specified by the global Mfr_retry_count[2:0] until it is commanded OFF (by the CONTROL pin or OPERATION command or both), bias power is removed, or another fault condition causes the unit to shut down. Changing the value might not take effect until the next off-then-on sequence on that channel.
b[2:0]	Ton_max_fault_response_delay	Hard coded to 000b: There is no additional deglitch delay applied to fault detection.

MFR_RETRY_DELAY

This command determines the retry interval when the LTC2974 is in retry mode in response to a fault condition. This delay is counted using SHARE_CLK only. This delay is internally limited to 13.1 seconds, and rounded to the nearest 200µs. The read value of this command always returns what was last written and does not reflect internal limiting.

MFR_RETRY_COUNT

The MFR_RETRY_COUNT is a global command that sets the number of retries attempted when any channel faults off with its fault response retry field set to a non zero value.

In the event of multiple or recurring retry faults on the same channel the total number of retries equals MFR_RETRY_COUNT. If a channel has not been faulted off for 6 seconds, its retry counter is cleared. Toggling a channel's CONTROL pin off then on or issuing OPERATION off then on commands will synchronously clear the retry count.

MFR_RETRY_COUNT Data Contents

BIT(S)	SYMBOL	OPERATION
b[7:3]	Reserved	Always returns zero.
b[2:0]	Mfr_retry_count [2:0]	0: No retries: 1-6: Number of retries. 7: Infinite retries. Changing the value might not take effect until the next off-then-on sequence on that channel.

PMBUS COMMAND DESCRIPTION

SHARED EXTERNAL FAULTS

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	EEPROM	DEFAULT VALUE	REF PAGE
MFR_FAULTB0_PROPAGATE	0xD2	Configuration that determines if a channel's faulted off state is propagated to the FAULTB0 pin.	R/W Byte	Y	Reg		Y	0x00	63
MFR_FAULTB1_PROPAGATE	0xD3	Configuration that determines if a channel's faulted off state is propagated to the FAULTB1 pin.	R/W Byte	Y	Reg		Y	0x00	63
MFR_FAULTB0_RESPONSE	0xD5	Action to be taken by the device when the FAULTB0 pin is asserted low.	R/W Byte	N	Reg		Y	0x00	64
MFR_FAULTB1_RESPONSE	0xD6	Action to be taken by the device when the FAULTB1 pin is asserted low.	R/W Byte	N	Reg		Y	0x00	64

MFR_FAULTB0_PROPAGATE and MFR_FAULTB1_PROPAGATE

These manufacturer specific commands enable channels that have faulted off to propagate that state to the appropriate fault pin. MFR_FAULTB0_PROPAGATE allows any channel's faulted off state to propagate to the FAULTB0 pin. MFR_FAULTB1_PROPAGATE allows any channel's faulted off state to propagate to the FAULTB1 pin.

Note that pulling a fault pin low will have no effect for channels that have MFR_FAULTBn_RESPONSE set to 0. The channel continues operation without interruption. This fault response is called Ignore (0x0) in LTpowerPlay.

MFR_FAULTB0_PROPAGATE Data Contents

BIT(S)	SYMBOL	OPERATION
b[7:1]	Reserved	Don't care. Always returns 0.
b[0]	Mfr_faultb0_propagate	Enable fault propagation. 0: Channel's faulted off state does not assert FAULTB0 low. 1 :Channel's faulted off state asserts FAULTB0 low.

MFR_FAULTB1_PROPAGATE Data Contents

BIT(S)	SYMBOL	OPERATION
b[7:1]	Reserved	Don't care. Always returns 0.
b[0]	Mfr_faultb1_propagate	Enable fault propagation. 0: Channel's faulted off state does not assert FAULTB1 low. 1: Channel's faulted off state asserts FAULTB1 low.

PMBUS COMMAND DESCRIPTION

MFR_FAULTB0_RESPONSE and MFR_FAULTB1_RESPONSE

These manufacturer specific commands share the same format and specify the response to assertions of the FAULTB pins. MFR_FAULTB0_RESPONSE determines which channels shut off when the FAULTB0 pin is asserted low and MFR_FAULTB1_RESPONSE determines which channels shut off when the FAULTB1 pin is asserted low.When a channel shuts off in response to a FAULTB*n* pin, the ALERTB pin is asserted low and the appropriate bit is set in the STATUS_MFR_SPECIFIC register. For a graphical explanation, see the switches on the left hand side of Figure 28: Channel Fault Management Block Diagram.

Faults will not propagate for channels that have MFR_FAULTB*n*_RESPONSE set to 0: The channel continues operation without interruption. Note that this fault response is called No Action in LTpowerPlay.

MFR_FAULTB0_RESPONSE and MFR_FAULTB1_RESPONSE Data Contents

BIT(S)	SYMBOL	OPERATION
b[7:4]	Reserved	Read only, always returns 0000b.
b[3]	Mfr_faultb0_response_chan3, Mfr_faultb1_response_chan3	Channel 3 response. 0: The channel continues operation without interruption 1: The channel shuts down if the corresponding FAULTB pin is still asserted after 10µs. When the FAULTB pin subsequently de-asserts, the channel turns back on, honoring TON_DELAY and TON_RISE settings.
b[2]	Mfr_faultb0_response_chan2, Mfr_faultb1_response_chan2	Channel 2 response. 0: The channel continues operation without interruption 1: The channel shuts down if the corresponding FAULTB pin is still asserted after 10µs. When the FAULTB pin subsequently de-asserts, the channel turns back on, honoring TON_DELAY and TON_RISE settings.
b[1]	Mfr_faultb0_response_chan1, Mfr_faultb1_response_chan1	Channel 1 response. 0: The channel continues operation without interruption 1: The channel shuts down if the corresponding FAULTB pin is still asserted after 10µs. When the FAULTB pin subsequently de-asserts, the channel turns back on, honoring TON_DELAY and TON_RISE settings.
b[0]	Mfr_faultb0_response_chan0, Mfr_faultb1_response_chan0	Channel 0 response. 0: The channel continues operation without interruption 1: The channel shuts down if the corresponding FAULTB pin is still asserted after 10µs. When the FAULTB pin subsequently de-asserts, the channel turns back on, honoring TON_DELAY and TON_RISE settings.

PMBUS COMMAND DESCRIPTION

FAULT WARNING AND STATUS

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	EEPROM	DEFAULT VALUE	REF PAGE
CLEAR_FAULTS	0x03	Clear any fault bits that have been set.	Send Byte	Y				NA	65
STATUS_BYTE	0x78	One byte summary of the unit's fault condition.	R Byte	Y	Reg			NA	65
STATUS_WORD	0x79	Two byte summary of the unit's fault condition.	R Word	Y	Reg			NA	66
STATUS_VOUT	0x7A	Output voltage fault and warning status.	R Byte	Y	Reg			NA	66
STATUS_IOUT	0x7B	Output current fault and warning status.	R Byte	Y	Reg			NA	67
STATUS_INPUT	0x7C	Input supply fault and warning status.	R Byte	N	Reg			NA	67
STATUS_TEMPERATURE	0x7D	External temperature fault and warning status for READ_TEMPERATURE_1.	R Byte	Y	Reg			NA	67
STATUS_CML	0x7E	Communication and memory fault and warning status.	R Byte	N	Reg			NA	68
STATUS_MFR_SPECIFIC	0x80	Manufacturer specific fault and state information.	R Byte	Y	Reg			NA	68
MFR_PADS	0xE5	Current state of selected digital I/O pads.	R/W Word	N	Reg			NA	69
MFR_COMMON	0xEF	Manufacturer status bits that are common across multiple LTC chips.	R Byte	N	Reg			NA	69

CLEAR_FAULTS

The CLEAR_FAULTS command is used to clear status bits that have been set. This command clears all fault and warning bits in all unpaged status registers, and paged status registers selected by the current PAGE setting. At the same time, the device negates (clears, releases) its contribution to ALERTB.

The CLEAR_FAULTS command does not cause a unit that has latched off for a fault condition to restart. See Clearing Latched Faults for more information.

If the fault is present after the fault is cleared, the fault status bit shall be set again and the host notified by the usual means.

Note: this command responds to the global page command. (PAGE=0xFF)

STATUS_BYTE

The STATUS_BYTE command returns the summary of the most critical faults or warnings which have occurred, as shown in the following table. STATUS_BYTE is a subset of STATUS_WORD and duplicates the same information.

STATUS_BYTE Data Contents

BIT(S)	SYMBOL	OPERATION
b[7]	Status_byte_busy	Same as Status_word_busy.
b[6]	Status_byte_off	Same as Status_word_off.
b[5]	Status_byte_vout_ov	Same as Status_word_vout_ov.
b[4]	Status_byte_iout_oc	Same as Status_word_iout_oc.
b[3]	Status_byte_vin_uv	Same as Status_word_vin_uv.
b[2]	Status_byte_temp	Same as Status_word_temp.
b[1]	Status_byte_cml	Same as Status_word_cml.
b[0]	Status_byte_high_byte	Same as Status_word_high_byte.

PMBUS COMMAND DESCRIPTION

STATUS_WORD

The STATUS_WORD command returns two bytes of information with a summary of the unit's fault condition. Based on the information in these bytes, the host can get more information by reading the appropriate detailed status register.

The low byte of the STATUS_WORD is the same register as the STATUS_BYTE command.

STATUS_WORD Data Contents

BIT(S)	SYMBOL	OPERATION
b[15]	Status_word_vout	An output voltage fault or warning has occurred. See STATUS_VOUT.
b[14]	Status_word_iout	An output current fault or warning has occurred. See STATUS_IOUT.
b[13]	Status_word_input	An input voltage fault or warning has occurred. See STATUS_INPUT.
b[12]	Status_word_mfr	A manufacturer specific fault has occurred. See STATUS_MFR._SPECIFIC.
b[11]	Status_word_power_not_good	The PWRGD pin, if enabled, is negated. Power is not good.
b[10]	Status_word_fans	Not supported. Always returns 0.
b[9]	Status_word_other	Not supported. Always returns 0.
b[8]	Status_word_unknown	Not supported. Always returns 0.
b[7]	Status_word_busy	Device busy when PMBus command received. See OPERATION: Processing Commands.
b[6]	Status_word_off	This bit is asserted if the unit is not providing power to the output, regardless of the reason, including simply not being enabled. The off-bit is clear if unit is allowed to provide power to the output.
b[5]	Status_word_vout_ov	An output overvoltage fault has occurred.
b[4]	Status_word_iout_oc	An output overcurrent fault has occurred.
b[3]	Status_word_vin_uv	A V_{IN} undervoltage fault has occurred.
b[2]	Status_word_temp	A temperature fault or warning has occurred. See STATUS_TEMPERATURE.
b[1]	Status_word_cml	A communication, memory or logic fault has occurred. See STATUS_CML.
b[0]	Status_word_high_byte	A fault/warning not listed in b[7:1] has occurred or Status_word_power_not_good = 1.

STATUS_VOUT

The STATUS_VOUT command returns the summary of the output voltage faults or warnings which have occurred, as shown in the following table:

STATUS_VOUT Data Contents

BIT(S)	SYMBOL	OPERATION
b[7]	Status_vout_ov_fault	Overvoltage fault.
b[6]	Status_vout_ov_warn	Overvoltage warning.
b[5]	Status_vout_uv_warn	Undervoltage warning
b[4]	Status_vout_uv_fault	Undervoltage fault.
b[3]	Status_vout_max_warn	VOUT_MAX warning. An attempt has been made to set the output voltage to a value higher than allowed by the VOUT_MAX command.
b[2]	Status_vout_ton_max_fault	TON_MAX_FAULT sequencing fault.
b[1]	Status_vout_toff_max_warn	Not supported. Always returns 0.
b[0]	Status_vout_tracking_error	Not supported. Always returns 0.

PMBUS COMMAND DESCRIPTION

STATUS_IOUT

The STATUS_IOUT command returns the summary of the output current faults or warnings which have occurred, as shown in the following table:

STATUS_IOUT Data Contents

BIT(S)	SYMBOL	OPERATION
b[7]	Status_iout_oc_fault	Overcurrent fault.
b[6]	Status_iout_oc_uv_fault	Not Supported. Always returns 0.
b[5]	Status_iout_oc_warn	Overcurrent warning
b[4]	Status_iout_uc_fault	Undercurrent fault.
b[3]	Status_iout_curr_share_fault	Not Supported. Always returns 0.
b[2]	Status_pout_power_limiting	Not Supported. Always returns 0.
b[1]	Status_pout_overpower_fault	Not Supported. Always returns 0.
b[0]	Status_pout_overpower_warn	Not Supported. Always returns 0.

STATUS_INPUT

The STATUS_INPUT command returns the summary of the V_{IN} faults or warnings which have occurred, as shown in the following table:

STATUS_INPUT Data Contents

BIT(S)	SYMBOL	OPERATION
b[7]	Status_input_ov_fault	V_{IN} overvoltage fault
b[6]	Status_input_ov_warn	V_{IN} overvoltage warning
b[5]	Status_input_uv_warn	V_{IN} undervoltage warning
b[4]	Status_input_uv_fault	V_{IN} undervoltage fault
b[3]	Status_input_off	Unit is off for insufficient input voltage.
b[2]	IIN overcurrent fault	Not supported. Always returns 0.
b[1]	IIN overcurrent warn	Not supported. Always returns 0.
b[0]	PIN overpower warn	Not supported. Always returns 0.

STATUS_TEMPERATURE

The STATUS_TEMPERATURE command returns the summary of the temperature faults or warnings which have occurred, as shown in the following table. Note that this information is paged and refers to the temperature of the associated external diode.

STATUS_TEMPERATURE Data Contents

BIT(S)	SYMBOL	OPERATION
b[7]	Status_temperature_ot_fault	Overtemperature fault.
b[6]	Status_temperature_ot_warn	Overtemperature warning.
b[5]	Status_temperature_ut_warn	Undertemperature warning.
b[4]	Status_temperature_ut_fault	Undertemperature fault.
b[3]	Reserved	Reserved. Always returns 0.
b[2]	Reserved	Reserved. Always returns 0.
b[1]	Reserved	Reserved. Always returns 0.
b[0]	Reserved	Reserved. Always returns 0.

PMBUS COMMAND DESCRIPTION

STATUS_CML

The STATUS_CML command returns the summary of the communication, memory and logic faults or warnings which have occurred, as shown in the following table:

STATUS_CML Data Contents

BIT(S)	SYMBOL	OPERATION
b[7]	Status_cml_cmd_fault	1 = An illegal or unsupported command fault has occurred. 0 = No fault has occurred.
b[6]	Status_cml_data_fault	1 = Illegal or unsupported data received. 0 = No fault has occurred.
b[5]	Status_cml_pec_fault	1 = A packet error check fault has occurred. Note: PEC checking is always active in the LTC2974. Any extra byte received before a STOP will set Status_cml_pec_fault unless the extra byte is a matching PEC byte. 0 = No fault has occurred.
b[4]	Status_cml_memory_fault	1 = A fault has occurred in the EEPROM. 0 = No fault has occurred.
b[3]	Status_cml_processor_fault	Not supported, always returns 0.
b[2]	Reserved	Reserved, always returns 0.
b[1]	Status_cml_pmbus_fault	1 = A communication fault other than ones listed in this table has occurred. This is a catch all category for illegally formed I^2C/SMBus commands (Example: An address byte with read =1 received immediately after a START). 0 = No fault has occurred.
b[0]	Status_cml_unknown_fault	Not supported, always returns 0.

STATUS_MFR_SPECIFIC

The STATUS_MFR_SPECIFIC command returns manufacturer specific status flags. Bits marked CHANNEL = All are not paged. Bits marked STICKY = Yes stay set until a CLEAR_FAULTS is issued or the channel is commanded on by the user. Bits marked ALERT = Yes pull ALERTB low when the bit is set. Bits marked OFF = Yes indicate that the event can be configured elsewhere to turn the channel off.

STATUS_MFR_SPECIFIC Data Contents

BIT(S)	SYMBOL	OPERATION	CHANNEL	STICKY	ALERT	OFF
b[7]	Status_mfr_discharge	1 = A V_{OUT} discharge fault occurred while attempting to enter the ON state. 0 = No V_{OUT} discharge fault has occurred.	Current Page	Yes	Yes	Yes
b[6]	Status_mfr_fault1_in	This channel attempted to turn on while the FAULTB1 pin was asserted low, or this channel has shut down at least once in response to a FAULTB1 pin asserting low since the last CONTROL pin toggle, OPERATION command ON/OFF cycle or CLEAR_FAULTS command. If Mfr_track_en_chann is set, Status_mfr_fault1_in may also be set for the channel causing the fault.	Current Page	Yes	Yes	Yes
b[5]	Status_mfr_fault0_in	This channel attempted to turn on while the FAULTB0 pin was asserted low, or this channel has shut down at least once in response to a FAULTB0 pin asserting low since the last CONTROL pin toggle, OPERATION command ON/OFF cycle or CLEAR_FAULTS command. If Mfr_track_en_chann is set, Status_mfr_fault0_in may also be set for the channel causing the fault.	Current Page	Yes	Yes	Yes
b[4]	Status_mfr_servo_target_reached	Servo target has been reached.	Current Page	No	No	No
b[3]	Status_mfr_dac_connected	DAC is connected and driving V_{DAC} pin.	Current Page	No	No	No

PMBUS COMMAND DESCRIPTION

b[2]	Status_mfr_dac_saturated	A previous servo operation terminated with maximum or minimum DAC value.	Current Page	Yes	No	No
b[1]	Status_mfr_auxfaultb_faulted_off	AUXFAULTB has been de-asserted due to a V_{OUT} or I_{OUT} fault.	All	No	No	No
b[0]	Status_mfr_watchdog_fault	1 = A watchdog fault has occurred. 0 = No watchdog fault has occurred.	All	Yes	Yes	No

MFR_PADS

The MFR_PADS command provides read-only access of digital pads (pins). The input values are before any deglitching logic.

MFR_PADS Data Contents

BIT(S)	SYMBOL	OPERATION
b[15]	Mfr_pads_pwrgd_drive	0 = PWRGD pad is being driven low by this chip. 1 = PWRGD pad is not being driven low by this chip.
b[14]	Mfr_pads_alertb_drive	0 = ALERTB pad is being driven low by this chip. 1 = ALERTB pad is not being driven low by this chip.
b[13:12]	Mfr_pads_faultb_drive[1:0]	bit[1] used for FAULTB0 pad, bit[0] used for FAULTB1 pad as follows: 0 = FAULTB pad is being driven low by this chip. 1 = FAULTB pad is not being driven low by this chip.
b[11:10]	Reserved[1:0]	Always returns 00b.
b[9:8]	Mfr_pads_asel1[1:0]	11: Logic high detected on ASEL1 input pad. 10: ASEL1 input pad is floating. 01: Reserved. 00: Logic low detected on ASEL1 input pad.
b[7:6]	Mfr_pads_asel0[1:0]	11: Logic high detected on ASEL0 input pad. 10: ASEL0 input pad is floating. 01: Reserved. 00: Logic low detected on ASEL0 input pad.
b[5]	Mfr_pads_control1	1: Logic high detected on CONTROL1 pad. 0: Logic low detected on CONTROL1 pad.
b[4]	Mfr_pads_control0	1: Logic high detected on CONTROL0 pad. 0: Logic low detected on CONTROL0 pad.
b[3:2]	Mfr_pads_faultb[1:0]	bit[1] used for FAULTB0 pad, bit[0] used for FAULTB1 pad as follows: 1: Logic high detected on FAULTB pad. 0: Logic low detected on FAULTB pad.
b[1]	Mfr_pads_control2	1: Logic high detected on CONTROL2 pad. 0: Logic low detected on CONTROL2 pad.
b[0]	Mfr_pads_control3	1: Logic high detected on CONTROL3 pad. 0: Logic low detected on CONTROL3 pad.

MFR_COMMON

This command returns status information for the alert, device busy, share-clock pin (SHARE_CLK) and the write-protect pin (WP).

PMBUS COMMAND DESCRIPTION

This is the only command that may still be read when the LTC2974 is busy processing an EEPROM or other command. It may be polled by the host to determine when the LTC2974 is available to process a PMBus command. A busy device will always acknowledge its address but will NACK the command byte and set Status_byte_busy and Status_word_busy when it receives a command that it cannot immediately process. ALERTB will not be asserted low in this case.

MFR_COMMON Data Contents

BIT(S)	SYMBOL	OPERATION
b[7]	Mfr_common_alertb	Returns alert status. 1: ALERTB is de-asserted high. 0: ALERTB is asserted low.
b[6]	Mfr_common_busyb	Returns device busy status. 1: The device is available to process PMBus commands. 0: The device is busy and will NACK PMBus commands.
b[5:2]	Reserved	Read only, always returns 1s.
b[1]	Mfr_common_share_clk	Returns the status of the share-clock pin. 1: Share-clock pin is being held low. 0: Share-clock pin is active.
b[0]	Mfr_common_write_protect	Returns the status of the write-protect pin. 1: Write-protect pin is high. 0: Write-protect pin is low.

TELEMETRY

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	EEPROM	DEFAULT VALUE	REF PAGE
READ_VIN	0x88	Input supply voltage.	R Word	N	L11	V		NA	71
READ_VOUT	0x8B	DC/DC converter output voltage.	R Word	Y	L16	V		NA	71
READ_IOUT	0x8C	DC/DC converter output current.	R Word	Y	L11	A		NA	71
READ_TEMPERATURE_1	0x8D	External diode junction temperature. This is the value used for all temperature related processing, including IOUT_CAL_GAIN.	R Word	Y	L11	°C		NA	71
READ_TEMPERATURE_2	0x8E	Internal junction temperature.	R Word	N	L11	°C		NA	71
READ_POUT	0x96	DC/DC converter output power.	R Word	Y	L11	W		NA	71
MFR_READ_IOUT	0xBB	Alternate data format for READ_IOUT. One LSB = 2.5mA.	R Word	Y	CF	2.5mA		NA	71
MFR_IOUT_SENSE_VOLTAGE	0xFA	Absolute value of the voltage between $I_{SENSEP}n$ and $I_{SENSEM}n$. One LSB = 3.05µV.	R Word	Y	CF	3.05µV		NA	72
MFR_VIN_PEAK	0xDE	Maximum measured value of READ_VIN.	R Word	N	L11	V		NA	73
MFR_VOUT_PEAK	0xDD	Maximum measured value of READ_VOUT.	R Word	Y	L16	V		NA	73
MFR_IOUT_PEAK	0xD7	Maximum measured value of READ_IOUT.	R Word	Y	L11	A		NA	73
MFR_TEMPERATURE_1_PEAK	0xDF	Maximum measured value of READ_TEMPERATURE_1.	R Word	Y	L11	°C		NA	73
MFR_VIN_MIN	0xFC	Minimum measured value of READ_VIN.	R Word	N	L11	V		NA	73
MFR_VOUT_MIN	0xFB	Minimum measured value of READ_VOUT.	R Word	Y	L16	V		NA	73
MFR_IOUT_MIN	0xD8	Minimum measured value of READ_IOUT.	R Word	Y	L11	A		NA	73
MFR_TEMPERATURE_1_MIN	0xFD	Minimum measured value of READ_TEMPERATURE_1.	R Word	Y	L11	°C		NA	73

PMBUS COMMAND DESCRIPTION

READ_VIN

This command returns the most recent ADC measured value of the input voltage at the V_{IN_SNS} pin.

READ_VOUT

This command returns the most recent ADC measured value of the channel's output voltage.

READ_IOUT

This command returns the most recent ADC measured value of the channel's output current.

READ_TEMPERATURE_1

This command returns the most recent measured value of the external diode temperature in °C. This value is used for all temperature related operations and calculations. This command is paged. READ_TEMPERATURE_2 is substituted for READ_TEMPERATURE_1 if the associated T_{SENSE} network fails to detect a valid temperature.

The T_{SENSE} network will fail to detect a valid temperature under the following conditions:

The T_{SENSE} pin is shorted to a constant voltage.

The sense diode has an ideality factor greater than N_TS max.

READ_TEMPERATURE_2

This command returns the most recent ADC measured value of junction temperature in °C as determined by the LTC2974's internal temperature sensor. This register is for information purposes and does not generate any faults, warnings, or affect any other registers or internal calculations unless it is used as READ_TEMPERATURE_1. This command is not paged.

READ_TEMPERATURE_2 is substituted for READ_TEMPERATURE_1 if a channel's T_{SENSE} network fails to detect a valid temperature.

READ_POUT

This command returns the most recent ADC measured value of the channel's output power in watts.

MFR_READ_IOUT

This command returns the most recent ADC measured value of the channel's output current, using a custom format that provides better numeric representation granularity than the READ_IOUT command for currents whose absolute value is between 2A and 82A.

PMBUS COMMAND DESCRIPTION

MFR_READ_IOUT Data Contents

BIT(S)	SYMBOL	OPERATION
b[15:0]	Mfr_read_iout[15:0]	Channel output current expressed in custom format for improved resolution at high currents. Value = Y • 2.5 where Y = b[15:0] is a signed two's-complement number. Example: MFR_READ_IOUT = 5mA For b[15:0] = 0x0002 Value = 2 • 2.5 = 5mA

The granularity of the returned value is always 2.5mA, and the return value is limited to ±81.92A. The READ_IOUT command provides the best resolution for currents less than 2A and must be used for currents larger than 82A. Note that the accuracy of the returned value is always limited by the ADC Characteristics listed in the Electrical Characteristics section.

Table 2. Comparison of Granularity Due to Numeric Format

CURRENT RANGE	READ_IOUT GRANULARITY	MFR_READ_IOUT GRANULARITY
31.25mA ≤ I_{OUT} < 62.5mA	61µA	2.5mA
62.5mA ≤ I_{OUT} < 125mA	122µA	2.5mA
125mA ≤ I_{OUT} < 250mA	244µA	2.5mA
250mA ≤ I_{OUT} < 500mA	488µA	2.5mA
0.5A ≤ I_{OUT} < 1A	977µA	2.5mA
1A ≤ I_{OUT} < 2A	1.95mA	2.5mA
2A ≤ I_{OUT} < 4A	3.9mA	2.5mA
4A ≤ I_{OUT} < 8A	7.8mA	2.5mA
8A ≤ I_{OUT} < 16A	15.6mA	2.5mA
16A ≤ I_{OUT} < 32A	31.3mA	2.5mA
32A ≤ I_{OUT} < 64A	62.5mA	2.5mA
64A ≤ I_{OUT} < 82A	125mA	2.5mA
82A ≤ I_{OUT} < 128A	125mA	Saturated
128A ≤ I_{OUT} < 256A	250mA	Saturated

MFR_IOUT_SENSE_VOLTAGE

This command returns the absolute value of the voltage measured between $I_{SENSEP}n$ and $I_{SENSEM}n$ during the last READ_IOUT ADC conversion without any temperature correction.

MFR_IOUT_SENSE_VOLTAGE Data Contents

BIT(S)	SYMBOL	OPERATION
b[15:0]	Mfr_iout_sense_voltage	Absolute value of raw voltage conversion measured between $I_{SENSEPn}$ and $I_{SENSEMn}$. Value = Y • 0.025 • 2^{-13} where Y = b[15:0] is an unsigned integer. Example: MFR_IOUT_SENSE_VOLTAGE = 1.544mV For b[15:0] = 0x1FA=506 Value = 506 • 0.025 • 2^{-13} = 1.544mV

PMBUS COMMAND DESCRIPTION

MFR_VIN_PEAK

This command returns the maximum ADC measured value of the input voltage. This register is reset to 0x7C00 (-2^{25}) when the LTC2974 emerges from power-on reset, when a CLEAR_FAULTS command to any page is executed, or a channel goes through an off-to-on transition.

MFR_VOUT_PEAK

This command returns the maximum ADC measured value of the channel's output voltage. This register is reset to 0xF800 (0.0) when the LTC2974 emerges from power-on reset, when a CLEAR_FAULTS command to the page is executed, or the channel goes through an off-to-on transition.

MFR_IOUT_PEAK

This commands returns the maximum ADC measured value of the channel's output current. This register is reset to 0x7C00 (-2^{25}) when the LTC2974 emerges from power-on reset, when a CLEAR_FAULTS command to the page is executed, or the channel goes through an off-to-on transition.

MFR_TEMPERATURE_1_PEAK

This command returns the maximum measured value of the external diode temperature in °C. This register is reset to 0x7C00 (-2^{25}) when the LTC2974 emerges from power-on reset, when a CLEAR_FAULTS command to the page is executed, or the channel goes through an off-to-on transition.

MFR_VIN_MIN

This command returns the minimum ADC measured value of the input voltage. This register is reset to 0x7BFF (approximately 2^{25}) when the LTC2974 emerges from power-on reset, when a CLEAR_FAULTS command to any page is executed, or a channel goes through an off-to-on transition.

MFR_VOUT_MIN

This command returns the minimum ADC measured value of the channel's output voltage. This register is reset to 0xFFFF (7.9999) when the LTC2974 emerges from power-on reset, when a CLEAR_FAULTS command to the page is executed, or the channel goes through an off-to-on transition. Updates are disabled when Margin Low (Ignore Faults and Warnings) is enabled.

MFR_IOUT_MIN

This command returns the minimum ADC measured values of the channel's output current. This register is reset to 0x7BFF (approximately 2^{25}) when the LTC2974 emerges from power-on reset, when a CLEAR_FAULTS command to the page is executed, or the channel goes through an off-to-on transition.

MFR_TEMPERATURE_1_MIN

This command returns the minimum measured value of the external diode temperature in °C. This register is reset to 0x7BFF (approximately 2^{25}) when the LTC2974 emerges from power-on reset, when a CLEAR_FAULTS command to the page is executed, or the channel goes through an off-to-on transition.

PMBUS COMMAND DESCRIPTION

FAULT LOGGING

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	EEPROM	DEFAULT VALUE	REF PAGE
MFR_FAULT_LOG_STORE	0xEA	Command a transfer of the fault log from RAM to EEPROM.	Send Byte	N				NA	74
MFR_FAULT_LOG_RESTORE	0xEB	Command a transfer of the fault log previously stored in EEPROM back to RAM.	Send Byte	N				NA	74
MFR_FAULT_LOG_CLEAR	0xEC	Initialize the EEPROM block reserved for fault logging and clear any previous fault logging locks.	Send Byte	N				NA	75
MFR_FAULT_LOG_STATUS	0xED	Fault logging status.	R Byte	N	Reg		Y	NA	75
MFR_FAULT_LOG	0xEE	Fault log data bytes. This sequentially retrieved data is used to assemble a complete fault log.	R Block	N	Reg		Y	NA	75

Fault Log Operation

A conceptual diagram of the fault log is shown in Figure 22. The fault log provides black box capability for the LTC2974. During normal operation the contents of the status registers, the output voltage/current/temperature readings, the input voltage readings, as well as peak and min values of these quantities, are stored in a continuously updated buffer in RAM. You can think of the operation as being similar to a strip chart recorder. When a fault occurs, the contents are written into EEPROM for non volatile storage. The EEPROM fault log is then locked. The part can be powered down with the fault log available for reading at a later time.

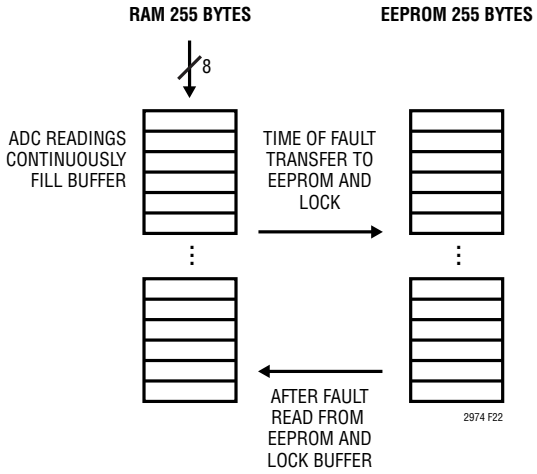

Figure 22. Fault Logging

MFR_FAULT_LOG_STORE

This command allows the user to transfer data from the RAM buffer to EEPROM.

MFR_FAULT_LOG_RESTORE

This command allows the user to transfer a copy of the fault-log data from the EEPROM to the RAM buffer. After a restore the RAM buffer is locked until a successful MFR_FAULT_LOG read.

PMBUS COMMAND DESCRIPTION

MFR_FAULT_LOG_CLEAR

This command initializes the EEPROM block reserved for fault logging. Any previous fault log stored in EEPROM will be erased by this operation and logging of the fault log RAM to EEPROM will be enabled. Make sure that Mfr_fault_log_status_ram = 0 before issuing the MFR_FAULT_LOG_CLEAR command.

MFR_FAULT_LOG_STATUS

This register is used to manage fault log events. The Mfr_fault_log_status_eeprom bit is set after a MFR_FAULT_LOG_STORE command or a faulted-off event triggers a transfer of the fault log from RAM to EEPROM. This bit is cleared by a MFR_FAULT_LOG_CLEAR command.

Mfr_fault_log_status_ram is set after a MFR_FAULT_ LOG_RESTORE to indicate that the data in the RAM has been restored from EEPROM and not yet read using a MFR_FAULT_LOG command. This bit is cleared only by a successful execution of an MFR_FAULT_LOG command.

MFR_FAULT_LOG_STATUS Data Contents

BIT(S)	SYMBOL	OPERATION
b[7:2]	Reserved	Read only, always returns 0s.
b[1]	Mfr_fault_log_status_ram	Fault log RAM status: 0: The fault log RAM allows updates. 1: The fault log RAM is locked until the next MFR_FAULT_LOG read.
b[0]	Mfr_fault_log_status_eeprom	Fault log EEPROM status: 0: The transfer of the fault log RAM to the EEPROM is enabled. 1: The transfer of the fault log RAM to the EEPROM is inhibited.

MFR_FAULT_LOG

Read only. This 2040-bit (255 byte) data block contains a copy of the RAM buffer fault log. The RAM buffer is continuously updated after each ADC conversion as long as Mfr_fault_log_status_ram is clear.

With Mfr_config_all_fault_log_enable = 1 and Mfr_fault_log_status_eeprom = 0, the RAM buffer is transferred to EEPROM whenever an LTC2974 fault causes a channel to latch off or a MFR_FAULT_LOG_STORE command is received. This transfer is delayed until the ADC has updated its READ values for all channels when Mfr_config_all_fast_fault_log is clear, otherwise it happens within 24ms. This optional delay can be used to ensure that the slower ADC monitored values are all updated for the case where a fast supervisor detected fault initiates the transfer to EEPROM.

Mfr_fault_log_status_eeprom is set high after the RAM buffer is transferred to EEPROM and not cleared until a MFR_FAULT_LOG_CLEAR is received, even if the LTC2974 is reset or powered down. Fault log EEPROM transfers are not initiated as a result of Status_mfr_discharge events.

During a MFR_FAULT_LOG read, data is returned one byte at a time as defined in Table 3. The fault log data is partitioned into two sections. The first section is referred to as the preamble and contains the Position_last pointer, time information and peak and min values. The second section contains a chronological record of telemetry and requires Position_last for proper interpretation. The fault log stores approximately 300ms of telemetry. To prevent timeouts during block reads, it is recommended that Mfr_config_all_longer_pmbus_timeout be set to 1.

PMBUS COMMAND DESCRIPTION

Table 3. Data Block Contents

DATA	BYTE*	DESCRIPTION
Position_last[7:0]	0	Position of fault log pointer when fault occurred.
SharedTime[7:0]	1	41-bit share-clock counter value when fault occurred. Counter LSB is in 200µs increments.
SharedTime[15:8]	2	
SharedTime[23:16]	3	
SharedTime[31:24]	4	
SharedTime[39:32]	5	
SharedTime[40]	6	
Mfr_vout_peak0[7:0]	7	
Mfr_vout_peak0[15:8]	8	
Mfr_vout_min0[7:0]	9	
Mfr_vout_min0[15:8]	10	
Mfr_temperature_peak0[7:0]	11	
Mfr_temperature_peak0[15:8]	12	
Mfr_temperature_min0[7:0]	13	
Mfr_temperature_min0[15:8]	14	
Mfr_iout_peak0[7:0]	15	
Mfr_iout_peak0[15:8]	16	
Mfr_iout_min0[7:0]	17	
Mfr_iout_min0[15:8]	18	
Mfr_vin_peak[7:0]	19	
Mfr_vin_peak[15:8]	20	
Mfr_vin_min[7:0]	21	
Mfr_vin_min[15:8]	22	
Mfr_vout_peak1[7:0]	23	
Mfr_vout_peak1[15:8]	24	
Mfr_vout_min1[7:0]	25	
Mfr_vout_min1[15:8]	26	
Mfr_temperature_peak1[7:0]	27	
Mfr_temperature_peak1[15:8]	28	
Mfr_temperature_min1[7:0]	29	
Mfr_temperature_min1[15:8]	30	
Mfr_iout_peak1[7:0]	31	
Mfr_iout_peak1[15:8]	32	
Mfr_iout_min1[7:0]	33	
Mfr_iout_min1[15:8]	34	
Mfr_vout_peak2[7:0]	35	
Mfr_vout_peak2[15:8]	36	
Mfr_vout_min2[7:0]	37	
Mfr_vout_min2[15:8]	38	

Table 3. Data Block Contents

DATA	BYTE*	DESCRIPTION
Mfr_temperature_peak2[7:0]	39	
Mfr_temperature_peak2[15:8]	40	
Mfr_temperature_min2[7:0]	41	
Mfr_temperature_min2[15:8]	42	
Mfr_iout_peak2[7:0]	43	
Mfr_iout_peak2[15:8]	44	
Mfr_iout_min2[7:0]	45	
Mfr_iout_min2[15:8]	46	
Mfr_vout_peak3[7:0]	47	
Mfr_vout_peak3[15:8]	48	
Mfr_vout_min3[7:0]	49	
Mfr_vout_min3[15:8]	50	
Mfr_temperature_peak3[7:0]	51	
Mfr_temperature_peak3[15:8]	52	
Mfr_temperature_min3[7:0]	53	
Mfr_temperature_min3[15:8]	54	
Mfr_iout_peak3[7:0]	55	
Mfr_iout_peak3[15:8]	56	
Mfr_iout_min3[7:0]	57	
Mfr_iout_min3[15:8]	58	
Status_vout0[7:0]	59	
Status_iout0[7:0]	60	
Status_mfr_specific0[7:0]	61	
Status_vout1[7:0]	62	
Status_iout1[7:0]	63	
Status_mfr_specific1[7:0]	64	
Status_vout2[7:0]	65	
Status_iout2[7:0]	66	
Status_mfr_specific2[7:0]	67	
Status_vout3[7:0]	68	
Status_iout3[7:0]	69	
Status_mfr_specific3[7:0]	70	
		71 bytes for preamble
Fault_log [Position_last]	71	
Fault_log [Position_last-1]	72	
.		
.		
.		
Fault_log [Position_last-170]	237	
Reserved	238-254	

PMBUS COMMAND DESCRIPTION

Table 3. Data Block Contents

DATA	BYTE*	DESCRIPTION
		Number of loops: (238 – 71)/54 = 3.1

*Note that PMBus data byte numbers start at 1 rather than 0.
See Figure 13 Block Read.

The data returned between bytes 71 and 237 of the previous table is interpreted using Position_last and the following table. The key to identifying the data located in byte 71 is to locate the DATA corresponding to POSITION = Position_last in the next table. Subsequent bytes are identified by decrementing the value of POSITION. For example: If Position_last = 8 then the first data returned in a block read is Status_temperature of page 0 followed by Read_temperature_1[15:8] of page 0 followed by Read_temperature_1[7:0] of page 0 and so on. See Table 4.

Table 4. Interpreting Cyclical Loop Data

POSITION	DATA
0	Read_temperature_2[7:0]
1	Read_temperature_2[15:8]
2	Read_vout0[7:0]
3	Read_vout0[15:8]
4	Status_vout0[7:0]
5	Status_mfr_specific0[7:0]
6	Read_temperature_1_0[7:0]
7	Read_temperature_1_0[15:8]
8	Status_temperature0[7:0]
9	Status_iout0[7:0]
10	Read_iout0[7:0]
11	Read_iout0[15:8]
12	Read_pout0[7:0]
13	Read_pout0[15:8]
14	Read_vin[7:0]
15	Read_vin[15:8]
16	Status_input[7:0]
17	0x0
18	Read_vout1[7:0]
19	Read_vout1[15:8]
20	Status_vout1[7:0]
21	Status_mfr_specific1[7:0]
22	Read_temperature_1_1[7:0]
23	Read_temperature_1_1[15:8]
24	Status_temperature1[7:0]
25	Status_iout1[7:0]
26	Read_iout1[7:0]
27	Read_iout1[15:8]
28	Read_pout1[7:0]
29	Read_pout1[15:8]
30	Read_vout2[7:0]
31	Read_vout2[15:8]
32	Status_vout2[7:0]
33	Status_mfr_specific2[7:0]
34	Read_temperature_1_2[7:0]
35	Read_temperature_1_2[15:8]
36	Status_temperature2[7:0]
37	Status_iout2[7:0]
38	Read_iout2[7:0]
39	Read_iout2[15:8]
40	Read_pout2[7:0]
41	Read_pout2[15:8]
42	Read_vout3[7:0]
43	Read_vout3[15:8]
44	Status_vout3[7:0]
45	Status_mfr_specific3[7:0]
46	Read_temperature_1_3[7:0]
47	Read_temperature_1_3[15:8]
48	Status_temperature3[7:0]
49	Status_iout3[7:0]
50	Read_iout3[7:0]
51	Read_iout3[15:8]
52	Read_pout3[7:0]
53	Read_pout3[15:8]
	Total Bytes = 54

PMBUS COMMAND DESCRIPTION

MFR_FAULT_LOG Read Example

The following table fully decodes a sample fault log read with Position_last = 13 to help clarify the cyclical nature of the operation.

Data Block Contents

PREAMBLE INFORMATION

BYTE NUMBER DECIMAL	BYTE NUMBER HEX		DATA	DESCRIPTION
0	00		Position_last[7:0] = 13	Position of fault-log pointer when fault occurred.
1	01		SharedTime[7:0]	41-bit share-clock counter value when fault occurred. Counter LSB is in 200µs increments.
2	02		SharedTime[15:8]	
3	03		SharedTime[23:16]	
4	04		SharedTime[31:24]	
5	05		SharedTime[39:32]	
6	06		SharedTime[40]	
7	07		Mfr_vout_peak0[7:0]	
8	08		Mfr_vout_peak0[15:8]	
9	09		Mfr_vout_min0[7:0]	
10	0A		Mfr_vout_min0[15:8]	
11	0B		Mfr_temperature_ peak0[7:0]	
12	0C		Mfr_temperature_ peak0[15:8]	
13	0D		Mfr_temperature_ min0[7:0]	
14	0E		Mfr_temperature_ min0[15:8]	
15	0F		Mfr_iout_peak0[7:0]	
16	10		Mfr_iout_peak0[15:8]	
17	11		Mfr_iout_min0[7:0]	
18	12		Mfr_iout_min0[15:8]	
19	13		Mfr_vin_peak_[7:0]	
20	14		Mfr_vin_peak_[15:8]	
21	15		Mfr_vin_min_[7:0]	
22	16		Mfr_vin_min_[15:8]	
23	17		Mfr_vout_peak1[7:0]	
24	18		Mfr_vout_peak1[15:8]	
25	19		Mfr_vout_min1[7:0]	
26	1A		Mfr_vout_min1[15:8]	
27	1B		Mfr_temperature_ peak1[7:0]	

PREAMBLE INFORMATION (CONT.)

BYTE NUMBER DECIMAL	BYTE NUMBER HEX		DATA	DESCRIPTION
28	1C		Mfr_temperature_ peak1[15:8]	
29	1D		Mfr_temperature_ min1[7:0]	
30	1E		Mfr_temperature_ min1[15:8]	
31	1F		Mfr_iout_peak1[7:0]	
32	20		Mfr_iout_peak1[15:8]	
33	21		Mfr_iout_min1[7:0]	
34	22		Mfr_iout_min1[15:8]	
35	23		Mfr_vout_peak2[7:0]	
36	24		Mfr_vout_peak2[15:8]	
37	25		Mfr_vout_min2[7:0]	
38	26		Mfr_vout_min2[15:8]	
39	27		Mfr_temperature_ peak2[7:0]	
40	28		Mfr_temperature_ peak2[15:8]	
41	29		Mfr_temperature_ min2[7:0]	
42	2A		Mfr_temperature_ min2[15:8]	
43	2B		Mfr_iout_peak2[7:0]	
44	2C		Mfr_iout_peak2[15:8]	
45	2D		Mfr_iout_min2[7:0]	
46	2E		Mfr_iout_min2[15:8]	
47	2F		Mfr_vout_peak3[7:0]	
48	30		Mfr_vout_peak3[15:8]	
49	31		Mfr_vout_min3[7:0]	
50	32		Mfr_vout_min3[15:8]	
51	33		Mfr_temperature_ peak3[7:0]	
52	34		Mfr_temperature_ peak3[15:8]	
53	35		Mfr_temperature_ min3[7:0]	
54	36		Mfr_temperature_ min3[15:8]	
55	37		Mfr_iout_peak3[7:0]	
56	38		Mfr_iout_peak3[15:8]	
57	39		Mfr_iout_min3[7:0]	
58	3A		Mfr_iout_min3[15:8]	
59	3B		Status_vout0[7:0]	

PMBUS COMMAND DESCRIPTION

PREAMBLE INFORMATION (CONT.)

BYTE NUMBER DECIMAL	BYTE NUMBER HEX		DATA	DESCRIPTION
60	3C		Status_iout0[7:0]	
61	3D		Status_ temperature0[7:0]	
62	3E		Status_vout1[7:0]	
63	3F		Status_iout1[7:0]	
64	40		Status_ temperature1[7:0]	
65	41		Status_vout2[7:0]	
66	42		Status_iout2[7:0]	
67	43		Status_ temperature2[7:0]	
68	44		Status_vout3[7:0]	
69	45		Status_iout3[7:0]	
70	46		Status_ temperature3[7:0]	End of Preamble

CYCLICAL MUX LOOP DATA PARTIAL LOOP

BYTE NUMBER DECIMAL	BYTE NUMBER HEX	LOOP BYTE NUMBER DECIMAL	MUX LOOP 0	54 BYTES PER LOOP
71	47	13	Read_pout0[15:8]	Position_last
72	48	12	Read_pout0[7:0]	
73	49	11	Read_iout0[15:8]	
74	4A	10	Read_iout0[7:0]	
75	4B	9	Status_iout0[7:0]	
76	4C	8	Status_ temperature0[7:0]	
77	4D	7	Read_ temperature_1_0[15:8]	
78	4E	6	Read_ temperature_1_0[7:0]	
79	4F	5	Status_mfr_ specific0[7:0]	
80	50	4	Status_vout0[7:0]	
81	51	3	Read_vout0[15:8]	
82	52	2	Read_vout0[7:0]	
83	53	1	Read_ temperature_2[15:8]	
84	54	0	Read_ temperature_2[7:0]	

CYCLICAL MUX LOOP DATA FULL LOOP

BYTE NUMBER DECIMAL	BYTE NUMBER HEX	LOOP BYTE NUMBER DECIMAL	MUX LOOP 1	54 BYTES PER LOOP
85	55	53	Read_pout3[15:8]	
86	56	52	Read_pout3[7:0]	
87	57	51	Read_iout3[15:8]	
88	58	50	Read_iout3[7:0]	
89	59	49	Status_iout3[7:0]	
90	5A	48	Status_ temperature3[7:0]	
91	5B	47	Read_ temperature_1_3[15:8]	
92	5C	46	Read_ temperature_1_3[7:0]	
93	5D	45	Status_mfr_ specific3[7:0]	
94	5E	44	Status_vout3[7:0]	
95	5F	43	Read_vout3[15:8]	
96	60	42	Read_vout3[7:0]	
97	61	41	Read_pout2[15:8]	
98	62	40	Read_pout2[7:0]	
99	63	39	Read_iout2[15:8]	
100	64	38	Read_iout2[7:0]	
101	65	37	Status_iout2[7:0]	
102	66	36	Status_ temperature2[7:0]	
103	67	35	Read_ temperature_1_2[15:8]	
104	78	34	Read_ temperature_1_2[7:0]	
105	69	33	Status_mfr_ specific2[7:0]	
106	6A	32	Status_vout2[7:0]	
107	6B	31	Read_vout2[15:8]	
108	6C	30	Read_vout2[7:0]	
109	6D	29	Read_pout1[15:8]	
110	6E	28	Read_pout1[7:0]	
111	6F	27	Read_iout1[15:8]	
112	70	26	Read_iout1[7:0]	
113	71	25	Status_iout1[7:0]	
114	72	24	Status_ temperature2[7:0]	
115	73	23	Read_ temperature_1_1[15:8]	

PMBUS COMMAND DESCRIPTION

CYCLICAL MUX LOOP DATA FULL LOOP (CONT.)

BYTE NUMBER DECIMAL	BYTE NUMBER HEX	LOOP BYTE NUMBER DECIMAL	MUX LOOP 1	54 BYTES PER LOOP
116	74	22	Read_ temperature_1_1[7:0]	
117	75	21	Status_mfr_ specific1[7:0]	
118	76	20	Status_vout1[7:0]	
119	77	19	Read_vout1[15:8]	
120	78	18	Read_vout1[7:0]	
121	79	17	0x0	
122	7A	16	Status_input[7:0]	
123	7B	15	Read_vin[15:8]	
124	7C	14	Read_vin[7:0]	
125	7D	13	Read_pout0[15:8]	
126	7E	12	Read_pout0[7:0]	
127	7F	11	Read_iout0[15:8]	
128	80	10	Read_iout0[7:0]	
129	81	9	Status_iout0[7:0]	
130	82	8	Status_ temperature0[7:0]	
131	83	7	Read_ temperature_1_0[15:8]	
132	84	6	Read_ temperature_1_0[7:0]	
133	85	5	Status_mfr_ specific0[7:0]	
134	86	4	Status_vout0[7:0]	
135	87	3	Read_vout0[15:8]	
136	88	2	Read_vout0[7:0]	
137	89	1	Read_ temperature_2[15:8]	
138	8A	0	Read_ temperature_2[7:0]	

CYCLICAL MUX LOOP DATA FULL LOOP

BYTE NUMBER DECIMAL	BYTE NUMBER HEX	LOOP BYTE NUMBER DECIMAL	MUX LOOP 2	54 BYTES PER LOOP
139	8B	53	Read_pout3[15:8]	
140	8C	52	Read_pout3[7:0]	
141	8D	51	Read_iout3[15:8]	
142	8E	50	Read_iout3[7:0]	
143	8F	49	Status_iout3[7:0]	

CYCLICAL MUX LOOP DATA FULL LOOP (CONT.)

BYTE NUMBER DECIMAL	BYTE NUMBER HEX	LOOP BYTE NUMBER DECIMAL	MUX LOOP 2	54 BYTES PER LOOP
144	90	48	Status_ temperature3[7:0]	
145	91	47	Read_ temperature_1_3[15:8]	
146	92	46	Read_ temperature_1_3[7:0]	
147	93	45	Status_mfr_ specific3[7:0]	
148	94	44	Status_vout3[7:0]	
149	95	43	Read_vout3[15:8]	
150	96	42	Read_vout3[7:0]	
151	97	41	Read_pout2[15:8]	
152	98	40	Read_pout2[7:0]	
153	99	39	Read_iout2[15:8]	
154	9A	38	Read_iout2[7:0]	
155	9B	37	Status_iout2[7:0]	
156	9C	36	Status_ temperature2[7:0]	
157	9D	35	Read_ temperature_1_2[15:8]	
158	9E	34	Read_ temperature_1_2[7:0]	
159	9F	33	Status_mfr_ specific2[7:0]	
160	A0	32	Status_vout2[7:0]	
161	A1	31	Read_vout2[15:8]	
162	A2	30	Read_vout2[7:0]	
163	A3	29	Read_pout1[15:8]	
164	A4	28	Read_pout1[7:0]	
165	A5	27	Read_iout1[15:8]	
166	A6	26	Read_iout1[7:0]	
167	A7	25	Status_iout1[7:0]	
168	A8	24	Status_ temperature2[7:0]	
169	A9	23	Read_ temperature_1_1[15:8]	
170	AA	22	Read_ temperature_1_1[7:0]	
171	AB	21	Status_mfr_ specific1[7:0]	
172	AC	20	Status_vout1[7:0]	
173	AD	19	Read_vout1[15:8]	

PMBUS COMMAND DESCRIPTION

CYCLICAL MUX LOOP DATA FULL LOOP (CONT.)

BYTE NUMBER DECIMAL	BYTE NUMBER HEX	LOOP BYTE NUMBER DECIMAL	MUX LOOP 2	54 BYTES PER LOOP
174	AE	18	Read_vout1[7:0]	
175	AF	17	0x0	
176	B0	16	Status_input[7:0]	
177	B1	15	Read_vin[15:8]	
178	B2	14	Read_vin[7:0]	
179	B3	13	Read_pout0[15:8]	
180	B4	12	Read_pout0[7:0]	
181	B5	11	Read_iout0[15:8]	
182	B6	10	Read_iout0[7:0]	
183	B7	9	Status_iout0[7:0]	
184	B8	8	Status_ temperature0[7:0]	
185	B9	7	Read_ temperature_1_0[15:8]	
186	BA	6	Read_ temperature_1_0[7:0]	
187	BB	5	Status_mfr_ specific0[7:0]	
188	BC	4	Status_vout0[7:0]	
189	BD	3	Read_vout0[15:8]	
190	BE	2	Read_vout0[7:0]	
191	BF	1	Read_ temperature_2[15:8]	
192	C0	0	Read_ temperature_2[7:0]	

CYCLICAL MUX LOOP DATA PARTIAL LOOP

BYTE NUMBER DECIMAL	BYTE NUMBER HEX	LOOP BYTE NUMBER DECIMAL	MUX LOOP 3	54 BYTES PER LOOP
193	C1	53	Read_pout3[15:8]	
194	C2	52	Read_pout3[7:0]	
195	C3	51	Read_iout3[15:8]	
196	C4	50	Read_iout3[7:0]	
197	C5	49	Status_iout3[7:0]	
198	C6	48	Status_ temperature_3[7:0]	
199	C7	47	Read_ temperature_1_3[15:8]	
200	C8	46	Read_ temperature_1_3[7:0]	

CYCLICAL MUX LOOP DATA PARTIAL LOOP (CONT.)

BYTE NUMBER DECIMAL	BYTE NUMBER HEX	LOOP BYTE NUMBER DECIMAL	MUX LOOP 3	54 BYTES PER LOOP
201	C9	45	Status_mfr_ specific3[7:0]	
202	CA	44	Status_vout3[7:0]	
203	CB	43	Read_vout3[15:8]	
204	CC	42	Read_vout3[7:0]	
205	CD	41	Read_pout2[15:8]	
206	CE	40	Read_pout2[7:0]	
207	CF	39	Read_iout2[15:8]	
208	D0	38	Read_iout2[7:0]	
209	D1	37	Status_iout2[7:0]	
210	D2	36	Status_ temperature2[7:0]	
211	D3	35	Read_ temperature_1_2[15:8]	
212	D4	34	Read_ temperature_1_2[7:0]	
213	D5	33	Status_mfr_ specific2[7:0]	
214	D6	32	Status_vout2[7:0]	
215	D7	31	Read_vout2[15:8]	
216	D8	30	Read_vout2[7:0]	
217	D9	29	Read_pout1[15:8]	
218	DA	28	Read_pout1[7:0]	
219	DB	27	Read_iout1[15:8]	
220	DC	26	Read_iout1[7:0]	
221	DD	25	Status_iout1[7:0]	
222	DE	24	Status_ temperature2[7:0]	
223	DF	23	Read_ temperature_1_1[15:8]	
224	E0	22	Read_ temperature_1_1[7:0]	
225	E1	21	Status_mfr_ specific1[7:0]	
226	E2	20	Status_vout1[7:0]	
227	E3	19	Read_vout1[15:8]	
228	E4	18	Read_vout1[7:0]	
229	E5	17	0x0	
230	E6	16	Status_input[7:0]	
231	E7	15	Read_vin[15:8]	
232	E8	14	Read_vin[7:0]	

PMBUS COMMAND DESCRIPTION

CYCLICAL MUX LOOP DATA PARTIAL LOOP (CONT.)

BYTE NUMBER DECIMAL	BYTE NUMBER HEX	LOOP BYTE NUMBER DECIMAL	MUX LOOP 3	54 BYTES PER LOOP
233	E9	13	Read_pout0[15:8]	
234	EA	12	Read_pout0[7:0]	
235	EB	11	Read_iout0[15:8]	
236	EC	10	Read_iout0[7:0]	
237	ED	9	Status_iout0[7:0]	Last valid fault log byte
238	EE		0x00	Bytes EE - FE return 0x00
239	EF		0x00	
240	F0		0x00	
241	F1		0x00	
242	F2		0x00	
243	F3		0x00	
244	F4		0x00	
245	F5		0x00	
246	F6		0x00	
247	F7		0x00	
248	F8		0x00	
249	F9		0x00	
250	FA		0x00	
251	FB		0x00	
252	FC		0x00	
253	FD		0x00	
254	FE		0x00	This is PMBUS byte 255. It must be read to clear Mfr_fault_log_ status_ram.

PMBUS COMMAND DESCRIPTION

IDENTIFICATION/INFORMATION

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	EEPROM	DEFAULT VALUE	REF PAGE
CAPABILITY	0x19	Summary of PMBus optional communication protocols supported by this device.	R Byte	N	Reg			0xB0	83
PMBUS_REVISION	0x98	PMBus revision supported by this device. Current revision is 1.1.	R Byte	N	Reg			0x11	83
MFR_SPECIAL_ID	0xE7	Manufacturer code for identifying the LTC2974.	R Word	N	Reg		Y	0x0215	83
MFR_SPECIAL_LOT	0xE8	Customer dependent codes that identify the factory programmed user configuration stored in EEPROM. Contact factory for default value.	R Byte	Y	Reg		Y	NA	83
MFR_INFO	0xB6	Manufacturer specific information.	R Word	N	Reg			NA	84

CAPABILITY

The CAPABILITY command provides a way for a host system to determine some key capabilities of the LTC2974.

CAPABILITY Data Contents

BIT(S)	SYMBOL	OPERATION
b[7]	Capability_pec	Hard coded to 1 indicating Packet Error Checking is supported. Reading the Mfr_config_all_pec_en bit will indicate whether PEC is currently required.
b[6:5]	Capability_scl_max	Hard coded to 01b indicating the maximum supported bus speed is 400kHz.
b[4]	Capability_smb_alert	Hard coded to 1 indicating this device does have an ALERTB pin and does support the SMBus Alert Response Protocol.
b[3:0]	Reserved	Always returns 0.

PMBUS_REVISION

PMBUS_REVISION Data Contents

BIT(S)	SYMBOL	OPERATION
b[7:0]	PMBus_rev	Reports the PMBus standard revision compliance. This is hard-coded to 0x11 for revision 1.1.

MFR_SPECIAL_ID

This register contains the manufacturer ID for the LTC2974. Always returns 0x0215.

MFR_SPECIAL_LOT

These paged registers contain information that identifies the user configuration that was programmed at the factory. Contact the factory to request a custom factory programmed user configuration and special lot number.

PMBUS COMMAND DESCRIPTION

MFR_INFO

The MFR_INFO register contains manufacturer specific information and is updated after a power-on reset, a RESTORE_USER_ALL command, or an EEPROM bulk read operation.

MFR_INFO Data Contents

BIT(S)	SYMBOL	OPERATION
b[15:6]	Reserved	Reserved.
b[5]	Mfr_info_ecc_user	EEPROM ECC status. 0: Corrections made in the EEPROM user space. 1: No corrections made in the EEPROM user space.
b[4:0]	Reserved	Reserved.

USER SCRATCHPAD

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	EEPROM	DEFAULT VALUE	REF PAGE
USER_DATA_00	0xB0	Manufacturer reserved for LTpowerPlay.	R/W Word	N	Reg		Y	NA	84
USER_DATA_01	0xB1	Manufacturer reserved for LTpowerPlay.	R/W Word	Y	Reg		Y	NA	84
USER_DATA_02	0xB2	OEM Reserved.	R/W Word	N	Reg		Y	NA	84
USER_DATA_03	0xB3	Scratchpad location.	R/W Word	Y	Reg		Y	0x0000	84
USER_DATA_04	0xB4	Scratchpad location.	R/W Word	N	Reg		Y	0x0000	84
MFR_LTC_RESERVED_1	0xB5	Manufacturer reserved.	R/W Word	Y	Reg		Y	NA	84
MFR_LTC_RESERVED_2	0xBC	Manufacturer reserved.	R/W Word	Y	Reg			NA	84

USER_DATA_00, USER_DATA_01, USER_DATA_02, USER_DATA_03, USER_DATA_04, MFR_LTC_RESERVED_1 and MFR_LTC_RESERVED_2

These registers are provided as user scratchpad and additional manufacturer reserved locations.

USER_DATA_03 and USER_DATA_04 are available for user scratch pad use. These 10 bytes (1 unpaged word plus 4 paged words) might be used for traceability or revision information such as serial number, board model number, assembly location, or assembly date.

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OVERVIEW

The LTC2974 is a power management IC that is capable of sequencing, margining, trimming, supervising output voltage for OV/UV conditions, supervising output current for OC/UC conditions, fault management, and voltage/current/temperature readback for four DC/DC converter channels. Input voltage and LTC2974 junction temperature readback are also available. Linear Technology Power System Managers can coordinate operation among multiple devices using common SHARE_CLK, FAULTB, and CONTROL pins. The LTC2974 utilizes a PMBus compliant interface and command set.

POWERING THE LTC2974

The LTC2974 can be powered two ways. The first method requires that a voltage between 4.5V and 15V be applied to the V_{PWR} pin. See Figure 23. An internal linear regulator converts V_{PWR} down to 3.3V which drives all of the internal circuitry of the LTC2974.

Alternatively, power from an external 3.3V supply may be applied directly to the V_{DD33} pins 11 and 12 using a voltage between 3.13V and 3.47V. See Figure 24. Tie V_{PWR} to the V_{DD33} pins. All functionality is available when using this alternate power method. The higher voltages needed for the V_{OUT_EN} pins and bias for the V_{SENSE} pins are charge pumped from V_{DD33}.

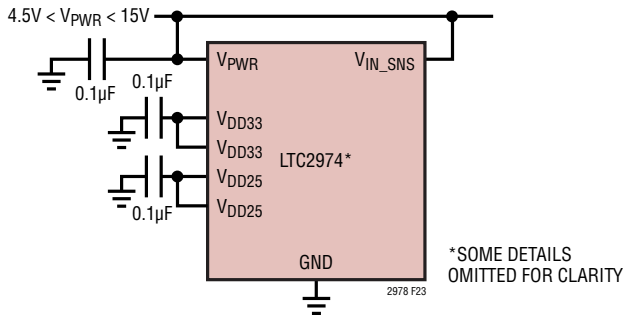

Figure 23. Powering LTC2974 Directly from an Intermediate Bus

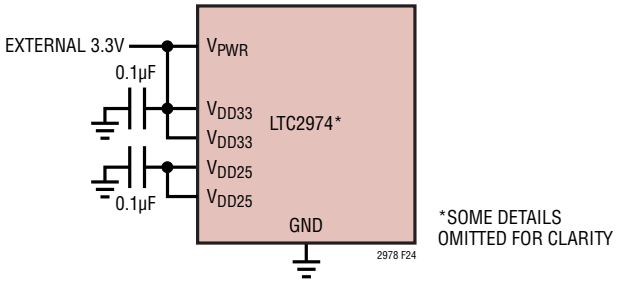

Figure 24. Powering LTC2974 from External 3.3V Supply

SETTING COMMAND REGISTER VALUES

The command register settings described herein are intended as a reference and for the purpose of understanding the registers in a software development environment. In actual practice, the LTC2974 can be completely configured for stand-alone operation with the LTC USB to I^2C/SMBus/PMBus controller (DC1613) and software GUI using intuitive menu driven objects.

SEQUENCE, SERVO, MARGIN AND RESTART OPERATIONS

Command Units On or Off

Three control parameters determine how a particular channel is turned on and off: The CONTROL pins, the OPERATION command and the value of the input voltage measured at the V_{IN_SNS} pin (V_{IN}). In all cases, VIN must exceed VIN_ON in order to enable the device to respond to the CONTROL pins or OPERATION commands. When V_{IN} drops below VIN_OFF an immediate OFF or sequence off after TOFF_DELAY of all channels will result (See Mfr_track_en_chann). Refer to the OPERATION section in the data sheet for a detailed description of the ON_OFF_CONFIG command.

Some examples of typical ON/OFF configurations are:

1. A DC/DC converter may be configured to turn on any time V_{IN} exceeds VIN_ON.
2. A DC/DC converter may be configured to turn on only when it receives an OPERATION command.
3. A DC/DC converter may be configured to turn on only via the CONTROL pin.
4. A DC/DC converter may be configured to turn on only when it receives an OPERATION command and the CONTROL pin is asserted.

On Sequencing

The TON_DELAY command sets the amount of time that

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a channel will wait following the start of an ON sequence before its V_{OUT_EN} pin will enable a DC/DC converter. Once the DC/DC converter has been enabled, the TON_RISE value determines the time at which the device soft-connects the DAC and servos the DC/DC converter output to the VOUT_COMMAND value. The TON_MAX_FAULT_LIMIT value determines the time at which the device checks for an undervoltage condition. If a TON_MAX_FAULT occurs, the channel can be configured to disable the DC/DC converter and propagate the fault to other channels using the bidirectional FAULTB pins. Figure 25 shows a typical on-sequence using the CONTROL pin. Note that overvolt-age faults are checked against the VOUT_OV_FAULT_LIMIT value at all times the device is powered up and not in a reset state nor margining while ignoring OVs.

On State Operation

Once a channel has reached the ON state, the OPERATION command can be used to command the DC/DC converter's output to margin high, margin low, or return to a nominal output voltage indicated by VOUT_COMMAND. The user also has the option of configuring a channel to continuously trim the output of the DC/DC converter to the VOUT_COMMAND voltage, or the channel's $V_{DAC}n$ output can be placed in a high impedance state thus allowing the DC/DC converter output voltage to go to its nominal value, $V_{DC}n_{(NOM)}$. Refer to the MFR_CONFIG_LTC2974 command for details on how to configure the output voltage servo.

Servo Modes

The ADC, DAC and internal processor comprise a digital servo loop that can be configured to operate in several useful modes. The servo target refers to the desired output voltage.

Continuous/non-continuous trim mode: MFR_CONFIG_LTC2974 b[7]. In continuous trim mode, the servo will update the DAC in a closed loop fashion each time it takes a V_{OUT} reading. The update rate is determined by the time it takes to step through the ADC MUX which is no more than t_{UPDATE_ADC}. See Electrical Characteristics table Note 6. In non-continuous trim mode, the servo will drive the DAC until the ADC measures the output voltage desired and then stop updating the DAC.

Non-continuous servo on warn mode: MFR_CONFIG_LTC2974 b[7] = 0, b[6] = 1. When in non-continuous mode, the LTC2974 will re-trim (re-servo) the output if the output drifts beyond the OV or UV warn limits.

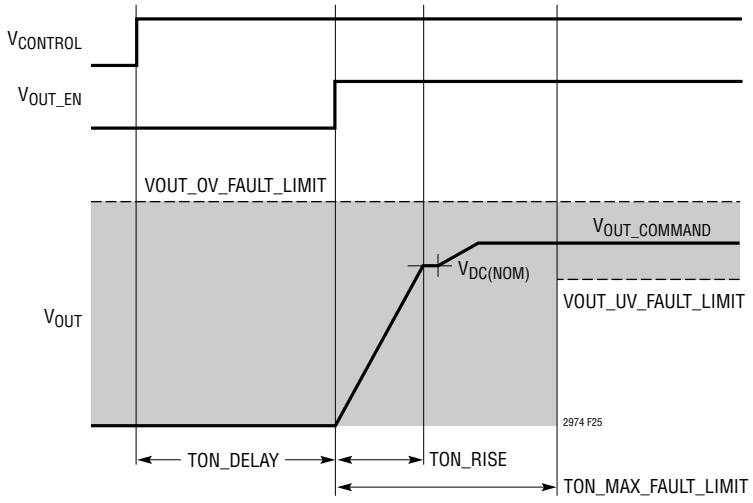

Figure 25. Typical ON Sequence Using Control Pin

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DAC Modes

The DACs that drive the V_{DACn} pins can operate in several useful modes. See MFR_CONFIG_LTC2974.

- Soft-connect. Using the LTC patented soft-connect feature, the DAC output is driven to within 1 LSB of the voltage at the DC/DC's feedback node before connecting, to avoid introducing transients on the output. This mode is used when servoing the output voltage. During startup, the LTC2974 waits until TON_RISE has expired before connecting the DAC. This is the most common operating mode.
- Disconnected. DAC output is high Z.
- DAC manual with soft-connect. Non servo mode. The DAC soft-connects to the feedback node. Soft-connect drives the DAC code to match the voltage at the feedback node. After connection, the DAC is moved by writing DAC codes to the MFR_DAC register.
- DAC manual with hard connect. Non servo mode. The DAC hard connects to the feedback node using the current value in MFR_DAC. After connection, the DAC is moved by writing DAC codes to the MFR_DAC register.

Margining

The LTC2974 margins and trims the output of a DC/DC converter by forcing a voltage across an external resistor connected between the DAC output and the feedback node or the trim pin. Preset limits for margining are stored in the VOUT_MARGIN_HIGH/LOW registers. Margining is actuated by writing the appropriate bits to the OPERATION register.

Margining requires the DAC to be connected. Margin requests that occur when the DAC is disconnected will be ignored.

Off Sequencing

An off sequence is initiated using the CONTROL pin or the OPERATION command. The TOFF_DELAY value determines the amount of time that elapses from the beginning of the off sequence until each channel's V_{OUT_EN} pin is pulled low, thus disabling its DC/DC converter.

V_{OUT} Off Threshold Voltage

The MFR_VOUT_DISCHARGE_THRESHOLD command register allows the user to specify the OFF threshold that the output voltage must decay below before the channel can enter/re-enter the ON state. The OFF threshold voltage is specified by multiplying MFR_VOUT_DISCHARGE_THRESHOLD and VOUT_COMMAND. In the event that an output voltage has not decayed below its OFF threshold before attempting to enter the ON state, the channel will continue to be held off, the appropriate bit is set in the STATUS_MFR_SPECIFIC register, and the ALERTB pin will be asserted low. When the output voltage has decayed below its OFF threshold, the channel can enter the ON state.

Automatic Restart via MFR_RESTART_DELAY Command and CONTROL pin

An automatic restart sequence can be initiated by driving the CONTROL pin to the off state for >10µs and then releasing it. The automatic restart disables all V_{OUT_EN} pins that are mapped to a particular CONTROL pin for a time period = MFR_RESTART_DELAY and then starts all DC/DC Converters according to their respective TON_DELAYs. (see Figure 26). V_{OUT_EN} pins are mapped to one of the CONTROL pins by the MFR_CONFIG_LTC2974 command. This feature allows a host that is about to reset to restart the power in a controlled manner after it has recovered.

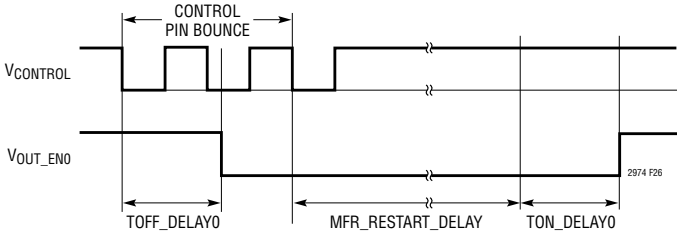

Figure 26. Off Sequence with Automatic Restart

FAULT MANAGEMENT

Output Overvoltage, Undervoltage, Overcurrent, and Undercurrent Faults

The high-speed voltage supervisor OV and UV fault thresholds are configured using the VOUT_OV_FAULT_LIMIT and VOUT_UV_FAULT_LIMIT commands, respectively. The VOUT_OV_FAULT_RESPONSE and VOUT_UV_FAULT_RESPONSE registers determine the responses to

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OV/UV faults. In addition, the high-speed current supervisor OC and UC fault thresholds are configured using the IOUT_OC_FAULT_LIMIT and IOUT_UC_FAULT_LIMIT commands, respectively. The IOUT_OC_FAULT_RESPONSE and IOUT_UC_FAULT_RESPONSE commands determine the responses to OC/UC faults. Fault responses can range from disabling the DC/DC converter immediately, waiting to see if the fault condition persists for some interval before disabling the DC/DC converter, or allowing the DC/DC converter to continue operating in spite of the fault. If a DC/DC converter is disabled, the LTC2974 can be configured to retry one to six times, retry continuously without limitation, or latch-off. The retry interval is specified using the MFR_RETRY_DELAY command. Latched faults are reset by toggling the CONTROL pin, using the OPERATION command, or removing and reapplying the bias voltage to the V_{IN_SNS} pin. All fault and warning conditions result in the ALERTB pin being asserted low and the corresponding bits being set in the status registers. The CLEAR_FAULTS command resets the contents of the status registers and de-asserts the ALERTB output.

Output Overvoltage, Undervoltage, and Overcurrent Warnings

OV, UV, and OC warning thresholds are processed by the LTC2974's ADC. These thresholds are set by the VOUT_OV_WARN_LIMIT, VOUT_UV_WARN_LIMIT, and IOUT_OC_WARN_LIMIT registers, respectively. Note that there is no I_{OUT} UC warning threshold. If a warning occurs, the corresponding bits are set in the status registers and the ALERTB output is asserted low. Note that a warning will never cause a V_{OUT_EN} output pin to disable a DC/DC converter.

Configuring the AUXFAULTB Output

The AUXFAULTB output may be used to indicate an output OV, OC, or UC fault. Use the MFR_CONFIG2_LTC2974 and MFR_CONFIG3_LTC2974 registers to configure the AUXFAULTB pin to assert low in response to VOUT_OV, IOUT_OC or IOUT_UC fault conditions. The AUXFAULTB output will stop pulling low when the LTC2974 is commanded to re-enter the ON state following a faulted-off condition.

A charge-pumped 5µA pull-up to 12V is also available on the AUXFAULTB output. Refer to the MFR_CONFIG_ALL_LTC2974 register description in the PMBUS COMMAND DESCRIPTION section for more information.

Figure 27 shows an application circuit where the AUXFAULTB output is used to trigger an SCR crowbar on the intermediate bus in order to protect the DC/DC converter's load from a catastrophic fault such as a stuck top gate. The stuck top gate causes an OV fault, which in turn causes the LTC2974 to pull AUXFAULTB low, thus deasserting the ON input to the LTC4210 hot-swap controller, which opens the switch Q1 that supplies the DC/DC converter input. In

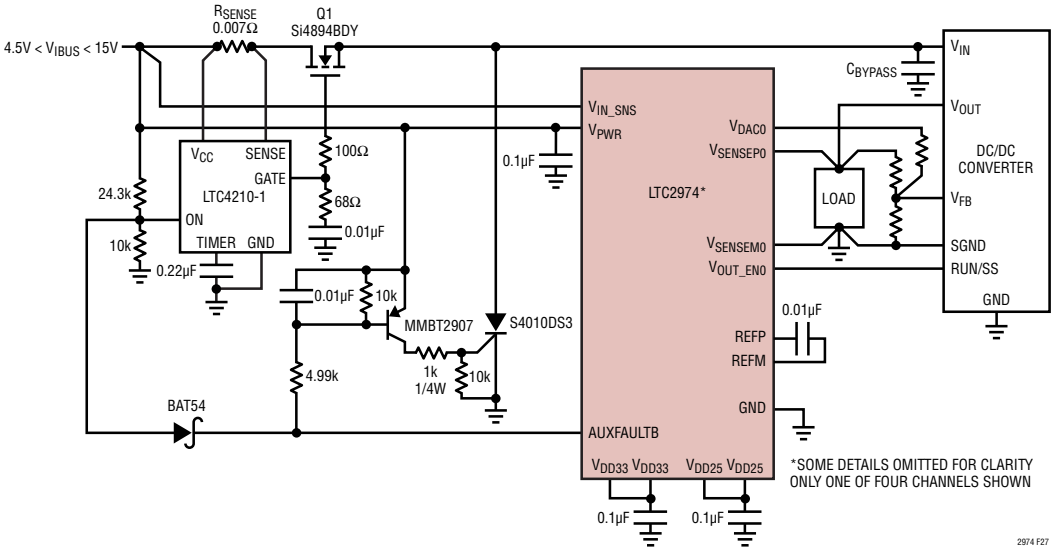

Figure 27. Application Circuit with Crowbar Protection on Intermediate Bus

APPLICATIONS INFORMATION

addition, when AUXFAULTB goes low it forces the S4010DS3 SCR device into the on-state via the 2N2907 PNP, thus quickly dropping the voltage on the V_{IN} input to the DC/DC converter, preventing the stuck top gate from damaging components supplied by this converter. Note that the V_{PWR} input to the LTC2974 bypasses switch Q1, keeping the LTC2974 fully powered throughout the above sequence.

Multi-Channel Fault Management

Multi-channel fault management is handled using the bidirectional FAULTB pins. Figure 28 illustrates the connections between channels and the FAULTB pins.

- The MFR_FAULTB*n*_PROPAGATE register acts like a programmable switch that allows faulted_off conditions from a particular channel (PAGE) to propagate to either FAULTB output. The MFR_FAULTB*n*_RESPONSE register controls similar switches on the inputs to each channel that allow any channel to shut down in response to any combination of the FAULTB pins. Channels responding to a FAULTB pin pulling low will attempt a new start sequence when the FAULTB pin in question is released by the faulted channel.
- A FAULTB pin can also be asserted low by an external driver in order to initiate an immediate off-sequence after a 10µs deglitch delay.

INTERCONNECT BETWEEN MULTIPLE LTC2974'S

Figure 29 shows how to interconnect the pins in a typical multi-LTC2974 array.

- All V_{IN_SNS} lines should be tied together in a star type connection at the point where V_{IN} is to be sensed. This will minimize timing errors for the case where the ON_OFF_CONFIG is configured to start the LTC2974 based on V_{IN} and ignore the CONTROL line and the OPERATION command. In multi-part applications that are sensitive to timing differences, it is recommended that the Vin_share_enable bit of the MFR_CONFIG_ALL_LTC2974 register be set high in order to allow SHARE_CLK to synchronize on/off sequencing in response to the VIN_ON and VIN_OFF thresholds.
- Connecting all AUXFAULTB lines together will allow selected faults on any DC/DC converter's output in the array to shut off a common input switch.
- ALERTB is typically one line in an array of PMBus converters. The LTC2974 allows a rich combination of faults and warnings to be propagated to the ALERTB pin.
- WDI/RESETB can be used to put the LTC2974 in the power-on reset state. Pull WDI/RESETB low for at least t_{RESETB} to enter this state.
- The FAULTB lines can be connected together to create fault dependencies. Figure 29 shows a configuration where a fault on any FAULTB will pull all others low. This is useful for arrays where it is desired to abort a startup sequence in the event any channel does not come up (see Figure 30).
- PWRGD reflects the status of the outputs that are mapped to it by the MFR_PWRGD_EN command. Figure 29 shows all the PWRGD pins connected together, but any combination may be used.

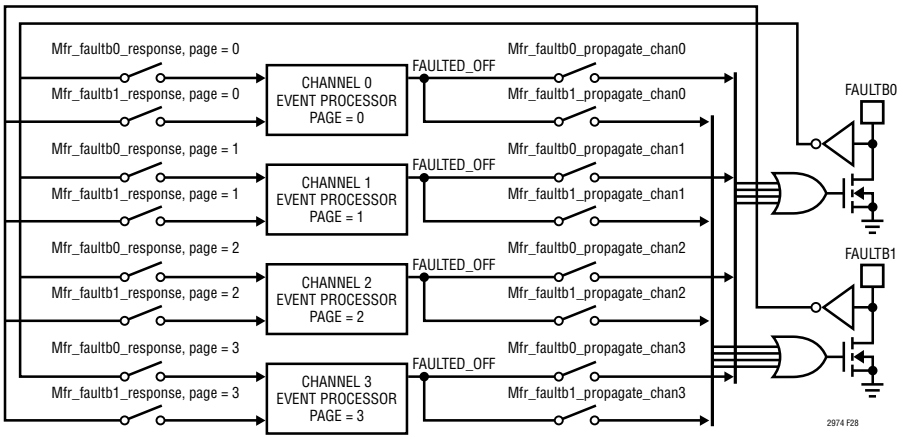

Figure 28. Channel Fault Management Block Diagram

APPLICATIONS INFORMATION

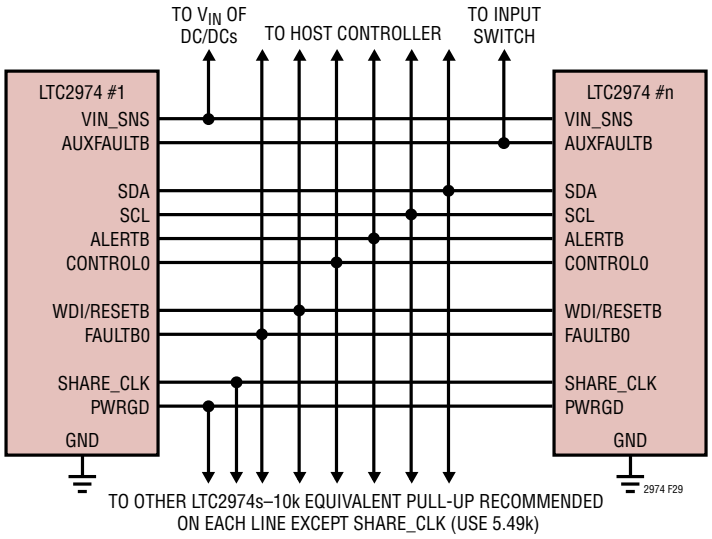

Figure 29. Typical Connections between Multiple LTC2974s

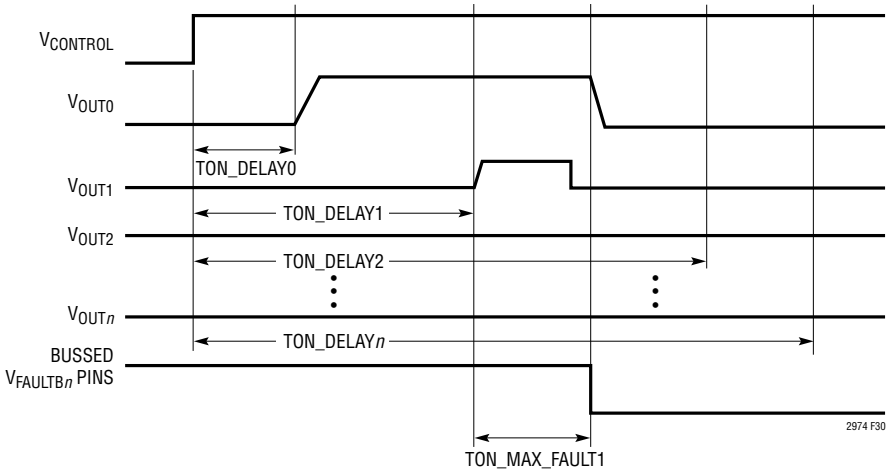

Figure 30. Aborted On-Sequence Due to Channel 1 Short

APPLICATION CIRCUITS

Trimming and Margining DC/DC Converters with External Feedback Resistors

Figure 31 shows a typical application circuit for trimming/margining a power supply with an external feedback network. The $V_{SENSEP0}$ and $V_{SENSEM0}$ differential inputs sense the load voltage directly, and a correction voltage is developed on the V_{DAC0} pin by the closed-loop servo algorithm. The V_{DAC0} output is connected to the DC/DC converter's feedback node through resistor R30. For this configuration, set Mfr_config_dac_pol to 0.

Four-Step Resistor Selection Procedure for DC/DC Converters with External Feedback Resistors

The following four-step procedure should be used to calculate the resistor values required for the application circuit shown in Figure 31.

1. Assume values for feedback resistor R20 and the nominal DC/DC converter output voltage $V_{DC(NOM)}$, and solve for R10.

   $V_{DC(NOM)}$ is the output voltage of the DC/DC converter when the LTC2974's V_{DAC0} pin is in a high impedance

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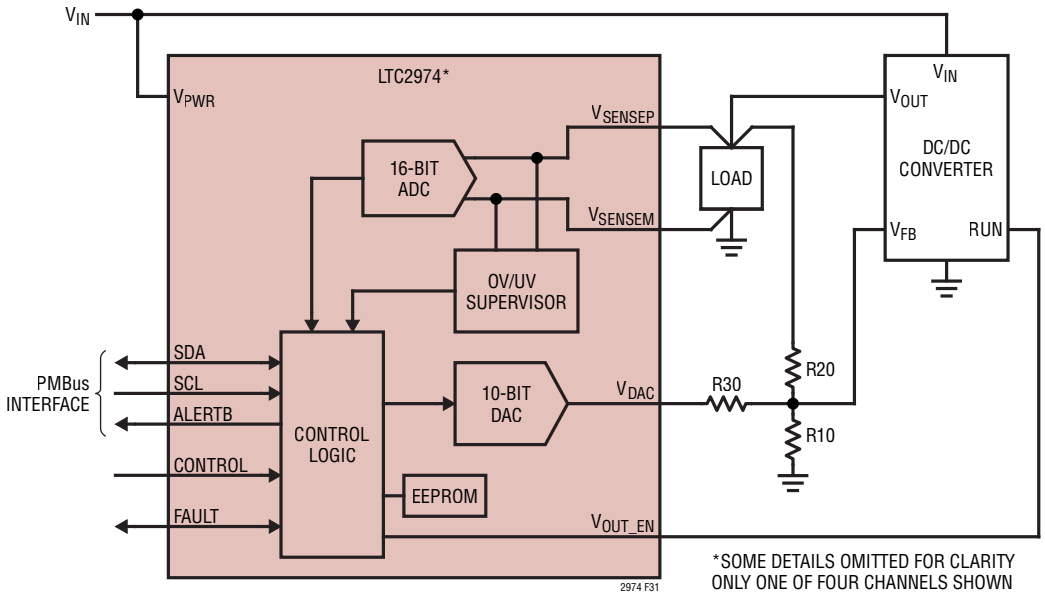

Figure 31. Application Circuit for DC/DC Converters with External Feedback Resistors

state. R10 is a function of R20, $V_{DC(NOM)}$, the voltage at the feedback node (V_{FB}) when the loop is in regulation, and the feedback node's input current (I_{FB}).

$$R10 = \frac{R20 \bullet V_{FB}}{V_{DC(NOM)} - I_{FB} \bullet R20 - V_{FB}} \quad (1)$$

2. Solve for the value of R30 that yields the maximum required DC/DC converter output voltage $V_{DC(MAX)}$.

   When V_{DAC0} is at 0V, the output of the DC/DC converter is at its maximum voltage.

$$R30 \le \frac{R20 \bullet V_{FB}}{V_{DC(MAX)} - V_{DC(NOM)}} \quad (2)$$

3. Solve for the minimum value of V_{DAC0} that is needed to yield the minimum required DC/DC converter output voltage $V_{DC(MIN)}$.

   The DAC has two full-scale settings, 1.38V and 2.65V. In order to select the appropriate full-scale setting, calculate the minimum required V_{FS_VDAC} output voltage:

$$V_{FS\_VDAC} > \left(V_{DC(NOM)} - V_{DC(MIN)}\right) \bullet \frac{R30}{R20} + V_{FB} \quad (3)$$

4. Re-calculate the minimum, nominal, and maximum DC/DC converter output voltages and the resulting margining resolution.

$$V_{DC(NOM)} = V_{FB} \bullet \left(1 + \frac{R20}{R10}\right) + I_{FB} \bullet R20 \quad (4)$$

$$V_{DC(MIN)} = V_{DC(NOM)} - \frac{R20}{R30} \bullet \left(V_{FS\_VDAC} - V_{FB}\right) \quad (5)$$

$$V_{DC(MAX)} = V_{DC(NOM)} + \frac{R20}{R30} \bullet V_{FB} \quad (6)$$

$$V_{RES} = \frac{\frac{R20}{R30} \bullet V_{FS\_VDAC}}{1023} \text{ V/DAC LSB} \quad (7)$$

Trimming and Margining DC/DC Converters with a TRIM Pin

Figure 32 illustrates a typical application circuit for trimming/margining the output voltage of a DC/DC converter with a TRIM Pin. The LTC2974's V_{DAC0} pin connects to the TRIM pin through resistor R30. For this configuration, set the DAC polarity bit Mfr_config_dac_pol in MFR_CONFIG_LTC2974 to 1.

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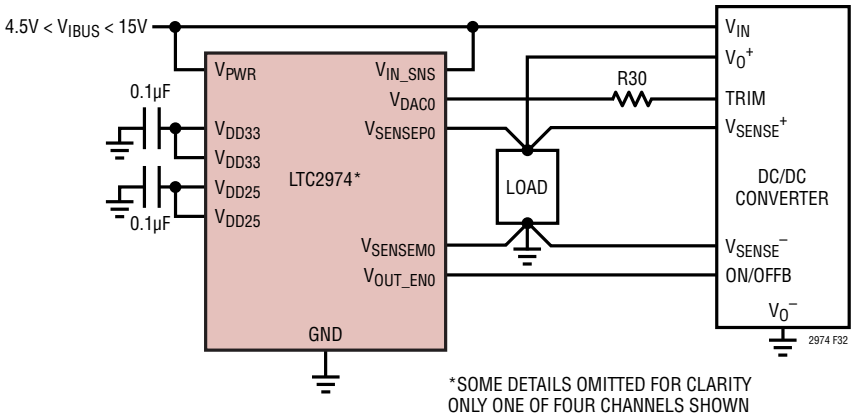

Figure 32. Application Circuit for DC/DC Converters with Trim Pin

DC/DC converters with a TRIM pin may be margined high or low by connecting an external resistor between the TRIM pin and either the V_{SENSEP} or V_{SENSEM} pin. The relationships between these resistors and the Δ% change in the output voltage of the DC/DC converter are typically expressed as:

$$R_{TRIM\_DOWN} = \frac{R_{TRIM} \bullet 50}{\Delta_{DOWN}\%} - R_{TRIM} \quad (8)$$

$$R_{TRIM\_UP} =$$

$$R_{TRIM} \bullet \left[\frac{V_{DC} \bullet (100 + \Delta_{UP}\%)}{2 \bullet V_{REF} \bullet \Delta_{UP}\%} - \left(\frac{50}{\Delta_{UP}\%} \right) - 1 \right] \quad (9)$$

where R_{TRIM} is the resistance looking into the TRIM pin, V_{REF} is the TRIM pin's open-circuit output voltage and V_{DC} is the DC/DC converter's nominal output voltage. Δ_{UP}% and Δ_{DOWN}% denote the percentage change in the converter's output voltage when margining up or down, respectively.

Two-Step Resistor and DAC Full-Scale Voltage Selection Procedure for DC/DC Converters with a TRIM Pin

The following two-step procedure should be used to calculate the resistor value for R30 and the required full-scale DAC voltage (refer to Figure 32).

1. Solve for R30:

$$R30 \le R_{TRIM} \bullet \left(\frac{50 - \Delta_{DOWN}\%}{\Delta_{DOWN}\%} \right) \quad (10)$$

2. Calculate the maximum required output voltage for V_{DAC0}:

$$V_{DAC0} \ge \left(1 + \frac{\Delta_{UP}\%}{\Delta_{DOWN}\%} \right) \bullet V_{REF} \quad (11)$$

Note: Not all DC/DC converters follow these trim equations, especially newer bricks. Consult LTC Field Application Engineering.

APPLICATIONS INFORMATION

Measuring Current with a Sense Resistor

A circuit for measuring current with a sense resistor is shown in Figure 33. The balanced filter rejects both common mode and differential mode noise from the output of the DC/DC converter. The filter is placed directly across the sense resistor in series with the DC/DC converter's inductor. Note that the current sense inputs must be limited to less than 6V with respect to ground. Select R_{CM} and C_{CM} such that the filter's corner frequency is < 1/10 the DC/DC converter's switching frequency. This will result in a current sense waveform that offers a good compromise between the voltage ripple and the delay through the filter. A value 1kΩ for R_{CM} is suggested in order to minimize gain errors due to the current sense inputs' internal resistance.

Measuring Current with Inductor DCR

Figure 34 shows the circuit for applications that require DCR current sense. A second order R-C filter is required in these applications in order to minimize the ripple voltage seen at the current sense inputs. A value of 1kΩ is suggested for R_{CM1} and R_{CM2} in order to minimize gain errors due the current sense inputs' internal resistance. C_{CM1} should be selected to provide cancellation of the zero created by the DCR and inductance, i.e. $C_{CM1} = L/(DCR \bullet R_{CM1})$. C_{CM2} should be selected to provide a second stage corner frequency at < 1/10 of the DC/DC converter's switching frequency. In addition, C_{CM2} needs to be much smaller than C_{CM1} in order to prevent significant loading of the filter's first stage.

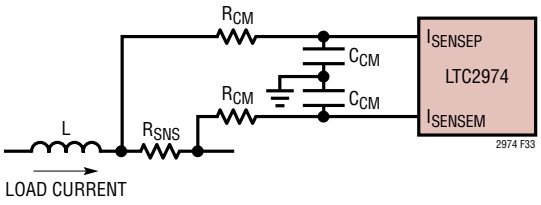

Figure 33. Sense Resistor Current Sensing Circuits

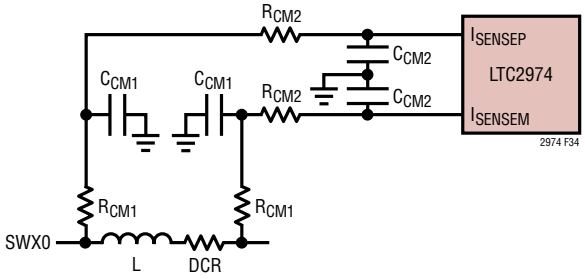

Figure 34. DCR Current Sensing Circuits

Single Phase Design Example

As a design example for a DCR current sense application, assume L = 2.2µH, DCR = 10mΩ, and F_{SW} = 500kHz.

Let R_{CM1} = 1kΩ and solve for C_{CM1}:

$$C_{CM1} \geq \frac{2.2\mu H}{10m\Omega \bullet 1k\Omega} = 220nF$$

Let R_{CM2} = 1kΩ. In order to get a second pole at $F_{SW}/10$ = 50kHz:

$$C_{CM2} \cong \frac{1}{2\pi \bullet 50kHz \bullet 1k\Omega} = 3.18nF$$

Let C_{CM2} = 3.3nF. Note that since C_{CM2} is much less than C_{CM1} the loading effects of the second stage filter on the matched first stage are not significant. Consequently, the delay time constant through the filter for the current sense waveform will be approximately 3µs.

Measuring Multiphase Currents

For current sense applications with more than one phase, R-C averaging may be employed. Figure 35 shows an example of this approach for a 3-phase system with DCR current sensing. The current sense waveforms are averaged together prior to being applied to the second stage of the filter consisting of R_{CM2} and C_{CM2}. Because the R_{CM1} resistors for the three phases are in parallel, the value of R_{CM1} must be multiplied by the number of phases. Also note that since the DCRs are effectively in parallel, the value for IOUT_CAL_GAIN will be equal to the inductor's DCR divided by the number of phases. Care should be taken in the layout of the multiphase inductors to keep the PCB trace resistance from the DC side of each inductor to the summing node balanced in order to provide the most accurate results.

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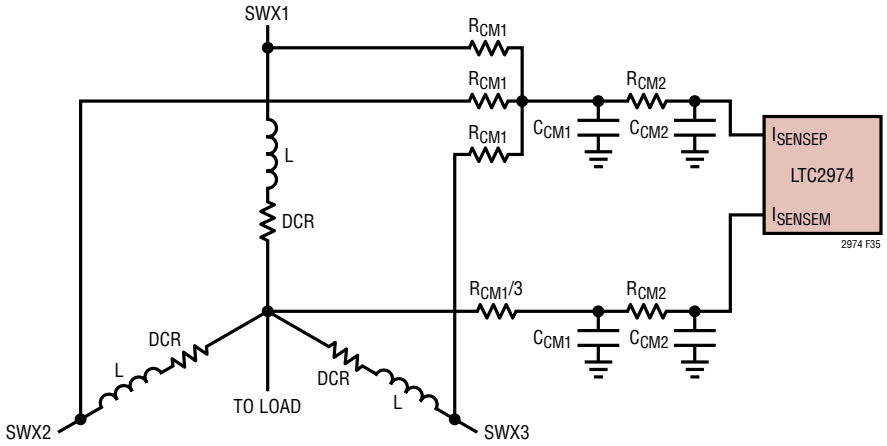

Figure 35. Multiphase DCR Current Sensing Circuits

Multiphase Design Example

Using the same values for inductance and DCR from the previous design example, the value for R_{CM1} will be 3kΩ for a three phase DC/DC converter if C_{CM1} is left at 220nF. Similarly, the value for IOUT_CAL_GAIN will be DCR/3 = 3.33mΩ.

Anti-aliasing Filter Considerations

Noisy environments require an anti-aliasing filter on the input to the LTC2974's ADC. The R-C circuit shown in Figure 36 is adequate for most situations. Keep R40 = R50 ≤ 200Ω to minimize ADC gain errors, and select a value for capacitors C10 and C20 that does not add too much additional response time to the OV/UV supervisor, e.g. τ = 10µs (R = 100Ω, C = 0.10µF).

Sensing Negative Voltages

Figure 37 shows the LTC2974 sensing a negative power supply (V_{EE}). The R1/R2 resistor divider translates the negative supply voltage to the LTC2974's $V_{SENSEM1}$ input while the $V_{SENSEP1}$ input is tied to the REFP pin which has a typical output voltage of 1.23V. Read_vout is determined from the following equation:

$$V_{EE} = V_{REFP} - (READ\_VOUT) \bullet \left(\frac{R2}{R1} + 1\right) - 1\mu A \bullet R2 \quad (14)$$

Where READ_VOUT returns $V_{SENSEP} - V_{SENSEM}$

The voltage divider should be configured in order to present about 0.5V to the voltage sense inputs when the negative supply reaches its POWER_GOOD_ON threshold so that

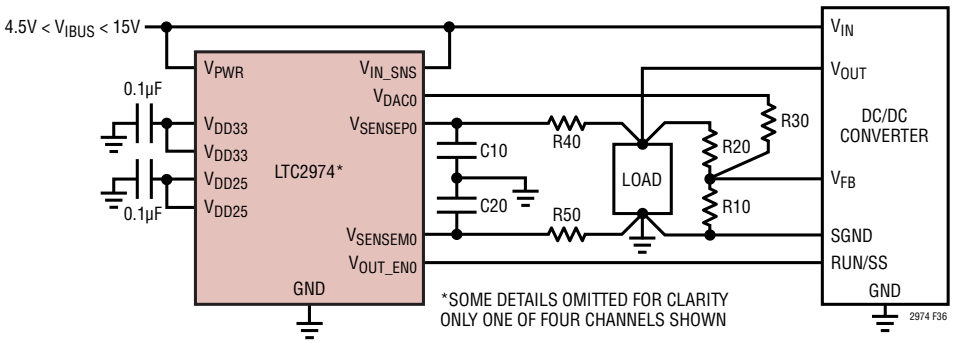

Figure 36. Anti-Aliasing Filter on V_{SENSE} Lines

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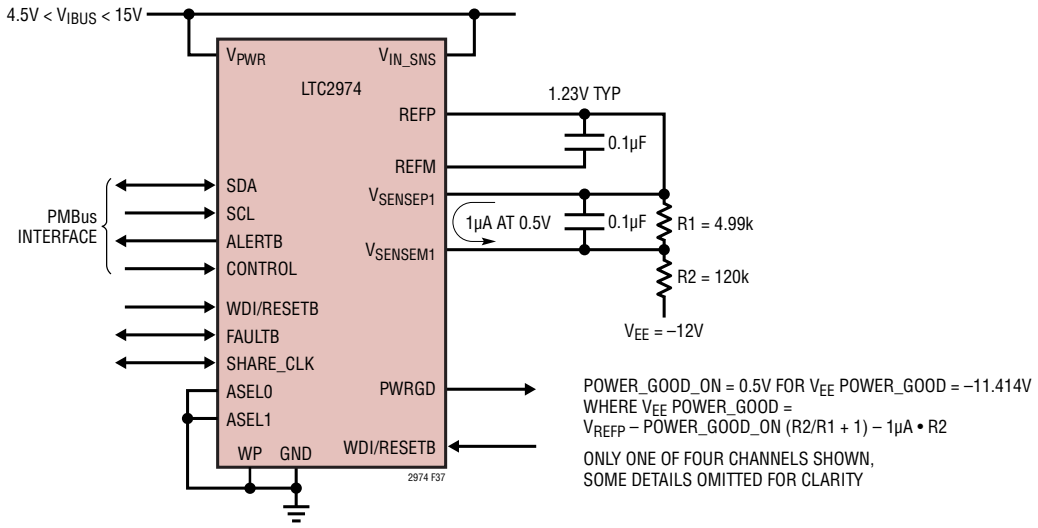

Figure 37. Sensing Negative Voltages

the current flowing out of the $V_{SENSEMn}$ pin is minimized to ~1µA. The relationship between the POWER_GOOD_ON register value and the corresponding negative supply value can be determined using Equation 14.

Connecting the DC1613 USB to I²C/SMBus/PMBus Controller to the LTC2974 in System

The DC1613 USB to I²C/SMBus/PMBus Controller can be interfaced to the LTC2974s on the user's board for programming, telemetry and system debug. The controller, when used in conjunction with LTpowerPlay software, provides a powerful way to debug an entire power system. Failures are quickly diagnosed using telemetry, fault status registers and the fault log. The final configuration can be quickly developed and stored to the LTC2974's EEPROM.

Figure 38 and Figure 39 illustrate application schematics for powering, programming and communicating with one or more LTC2974's via the DC1613 I²C/SMBus/PMBus controller regardless of whether or not system power is present.

Figure 38 shows the recommended schematic to use when the LTC2974 is powered by the system intermediate bus through its V_{PWR} pin.

Figure 39 shows the recommended schematic to use when the LTC2974 is powered by the system 3.3V through its V_{DD33} and V_{PWR} pins. The LTC4412 ideal OR'ing circuit allows either the controller or system to power the LTC2974.

Because of the controller's limited current sourcing capability, only the LTC2974s, their associated pull up resistors and the I²C/SMBus pull-up resistors should be powered from the ORed 3.3V supply. In addition, any device sharing I²C/SMBus bus connections with the LTC2974 should not have body diodes between the SDA/SCL pins and its V_{DD} node because this will interfere with bus communication in the absence of system power.

The DC1613 controller's I²C/SMBus connections are opto-isolated from the PC's USB port. The 3.3V supply from the controller and the LTC2974's V_{DD33} pin can be paralleled because the LTC LDOs that generate these voltages can be backdriven and draw <10µA. The controller's 3.3V current limit is 100mA.

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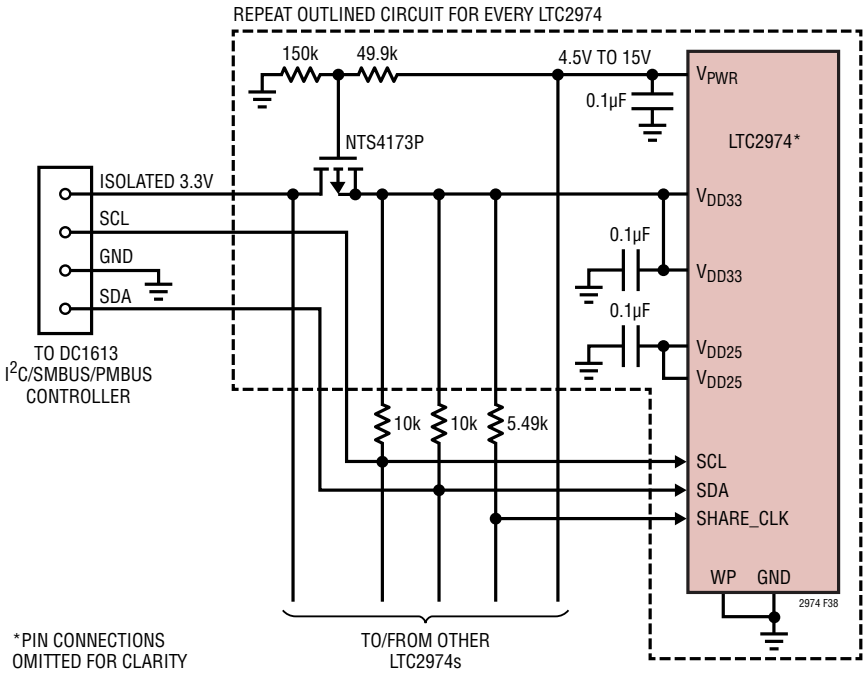
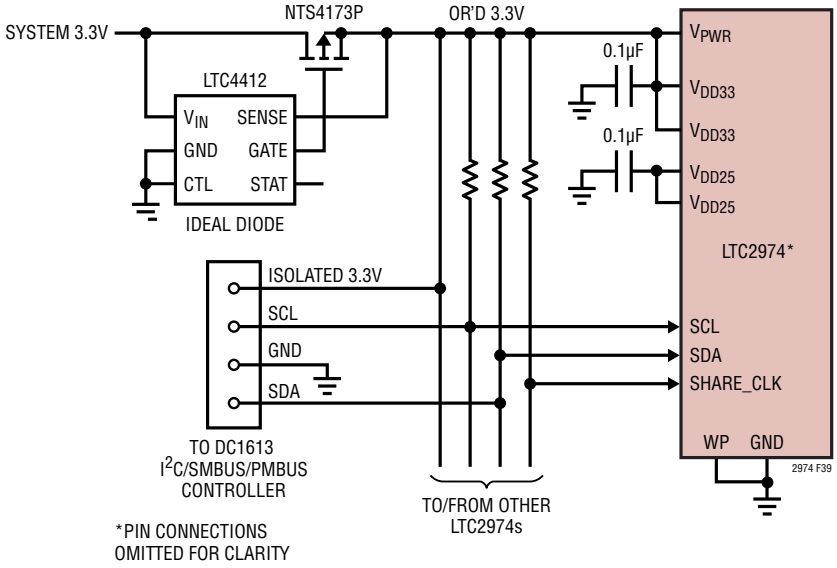


Figure 38. DC1613 Controller Connections When V_{PWR} Is Used



NOTE: DC1613 CONTROLLER I2C CONNECTIONS ARE OPTO-ISOLATED
ISOLATED 3.3V FROM LTC CONTROLLER CAN BE BACK DRIVEN AND WILL ONLY DRAW <10µA
ISOLATED 3.3V CURRENT LIMIT IS 100mA

Figure 39. DC1613 Controller Connections When LTC2974 Is Powered Directly from 3.3V

APPLICATIONS INFORMATION

ACCURATE DCR TEMPERATURE COMPENSATION

Using the DC resistance of the inductor as a current shunt element has several advantages – no additional power loss, lower circuit complexity and cost. However, the strong temperature dependence of the inductor resistance and the difficulty in measuring the exact inductor core temperature introduce errors in the current measurement. For copper, a change of inductor temperature of only 1°C corresponds to approximately 0.39% current gain change. Figure 40 shows a sample layout using the integrated DC/DC converter LTC3601 (right) and its corresponding thermal image (left). The converter is providing 1.8V, 1.5A to the output load.

Heat dissipation in the inductor under high load conditions creates transient and steady state thermal gradients between the inductor and the temperature sensor, and the sensed temperature does not accurately represent the inductor core temperature. This temperature gradient is clearly visible in the thermal image of Figure 40. In addition, transient heating/cooling effects have to be accounted for in order to reduce the transient errors introduced when load current changes are faster than heat transfer time constants of the inductor. Both of these problems are addressed by introducing two additional parameters: the thermal resistance θ_{IS} from the inductor core to the on-board temperature sensor, and the inductor thermal time constant τ. The thermal resistance θ_{IS} [°C/W], is used to calculate the steady state difference between the sensed temperature T_S and the internal inductor temperature T_I for a given power dissipated in the inductor P_I:

$$T_I - T_S = \theta_{IS}\, P_I = \theta_{IS}\, V_{DCR}\, I_{OUT} \qquad (1.1)$$

The additional temperature rise is used for a more accurate estimate of the inductor DC resistance R_I:

$$R_I = R0\,(1 + \alpha\,[T_S - T_{REF} + \theta_{IS}\, V_{DCR}\, I_{OUT}]) \qquad (1.2)$$

In the equations above, V_{DCR} is the inductor DC voltage drop, I_{OUT} is the RMS value of the output current, R0 is the inductor DC resistance at the reference temperature T_{REF} and α is the temperature coefficient of the resistance. Since most inductors are made of copper, we can expect a temperature coefficient close to α_{CU} = 3900ppm/°C. For a given α, the remaining parameters θ_{IS} and R0 can be calibrated at a single temperature using only two load currents:

$$R0 = \frac{(R2-R1)(P2+P1)-(R2+R1)(P2-P1)}{\alpha(T2-T1)(P2+P1)-(P2-P1)\left(2+\alpha\left[T1+T2-2T_{REF}\right]\right)} \qquad (1.3)$$

$$\theta_{IS} = \frac{1}{\alpha R0}\,\frac{\alpha(R1+R2)(T2-T1)-(R2-R1)\left(2+\alpha\left[T1+T2-2T_{REF}\right]\right)}{\alpha(T2-T1)(P2+P1)-(P2-P1)\left(2+\alpha\left[T1+T2-2T_{REF}\right]\right)} \qquad (1.4)$$

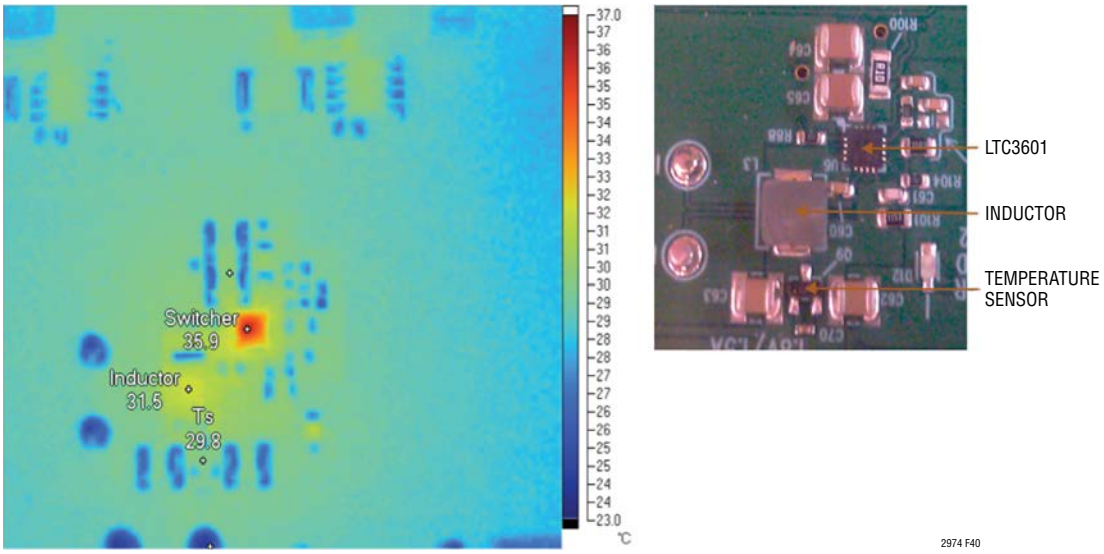


Figure 40. Thermal Image of a DC/DC Converter Showing the Difference Between the Actual Inductor Temperature and the Temperature Sensing Point

APPLICATIONS INFORMATION

The inductor resistance, $R_K = V_{DCR(K)}/I_{OUT(K)}$, power dissipation $P_K = V_{DCR(K)}\ I_{OUT(K)}$ and the sensed temperature T_K, (K = 1, 2) are recorded for each load current. To increase the accuracy in calculating θ_{IS}, the two load currents should be chosen around I1 = 10% and I2 = 90% of the current range of the system.

The inductor thermal time constant τ models the first order thermal response of the inductor and allows accurate DCR compensation during load transients. During a transition from low to high load current, the inductor resistance increases due to the self-heating. If we apply a single load step from the low current I1 to the higher current I2, the voltage across the inductor will change instantaneously from I1R1 to I2R1 and then slowly approach I2R2. Here R1 is the steady state resistance at the given temperature and load current I1, and R2 is the slightly higher DC resistance at I2, due to the inductor self-heating. Note that the electrical time constant τ_{EL} = L/R is several orders of magnitude shorter than the thermal one, and "instantaneous" is relative to the thermal time constant. The two settled regions give us the data sets (I1, T1, R1, P1) and (I2, T2, R2, P2) and the two-point calibration technique (1.3-1.4) is used to extract the steady-state parameters θ_{IS} and R0 (given a previously characterized average α). The relative current error calculated using the steady-state expression (1.2) will peak immediately after the load step, and then decay to zero with the inductor thermal time constant τ.

$$\frac{\Delta I}{I}(t) = \alpha\ \theta_{IS}\left(V2 \bullet I2 - V1 \bullet I1\right)e^{-t/\tau} \qquad (1.5)$$

The time constant τ is calculated from the slope of the best-fit line y = ln(ΔI/I) = a1 + a2t:

$$\tau = -\frac{1}{a2} \qquad (1.6)$$

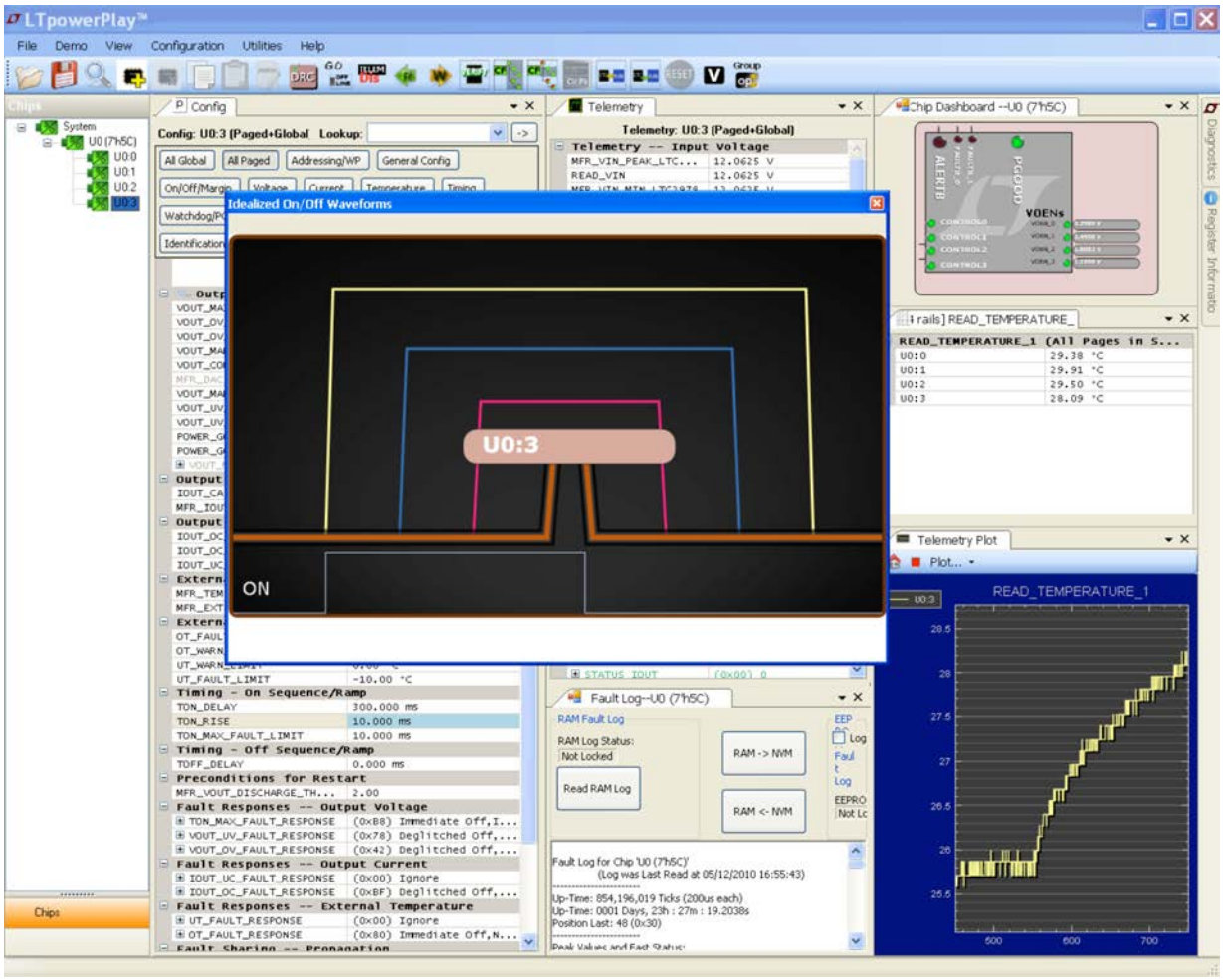
In summary, a single load current step is all that is needed to calibrate the DCR current measurement. The stable portions of the response give us the thermal resistance θ_{IS} and nominal DC resistance R0, and the settling characteristic is used to measure the inductor thermal time constant τ.

To get the best performance, the temperature sensor has to be as close as possible to the inductor and away from other significant heat sources. For example in Figure 40, the bipolar sense transistor is close to the inductor and away from the switcher. Connect the collector of the PNP to the base. Route the base and emitter separately to the LTC2974. Connect the base and collector to signal ground close to the LTC2974.

LTpowerPlay: AN INTERACTIVE GUI FOR POWER MANAGERS

LTpowerPlay is a powerful Windows based development environment that supports Linear Technology Power System Manager ICs with EEPROM, including the LTC2974 4-channel PMBus Power System Manager. The software supports a variety of different tasks. You can use LTpowerPlay to evaluate Linear Technology ICs by connecting to a demo board system. LTpowerPlay can also be used in an offline mode (with no hardware present) in order to build a multi-chip configuration file that can be saved and re-loaded at a later time. LTpowerPlay provides unprecedented diagnostic and debug features. It becomes a valuable diagnostic tool during board bring-up to program the power management scheme in a system. LTpowerPlay utilizes Linear Technology's DC1613 USB-to-I^2C/SMBus/PMBus Controller to communicate with one of many potential targets, including the DC1809/DC1810 demo board set, the DC1508 socketed programming board, or a customer target system. The software also provides an automatic update feature to keep the software current with the latest set of device drivers and documentation. A great deal of context sensitive help is available within LTpowerPlay along with several tutorial demos. Complete information is available.

APPLICATIONS INFORMATION



PCB ASSEMBLY AND LAYOUT SUGGESTIONS

Bypass Capacitor Placement

The LTC2974 requires 0.1µF bypass capacitors between the V_{DD33} pins and GND, the V_{DD25} pin and GND, and the REFP pin and REFM pin. If the chip is being powered from the V_{PWR} input, then that pin should also be bypassed to GND by a 0.1µF capacitor. In order to be effective, these capacitors should be made of a high quality ceramic dielectric such as X5R or X7R and be placed as close to the chip as possible.

Exposed Pad Stencil Design

The LTC2974's package is thermally and electrically efficient. This is enabled by the exposed die attach pad on the under side of the package which must be soldered

APPLICATIONS INFORMATION

down to the PCB or mother board substrate. It is a good practice to minimize the presence of voids within the exposed pad inter-connection. Total elimination of voids is difficult, but the design of the exposed pad stencil is key. Figure 41 shows a suggested screen print pattern. The proposed stencil design enables out-gassing of the solder paste during reflow as well as regulating the finished solder thickness. See IPC7525A

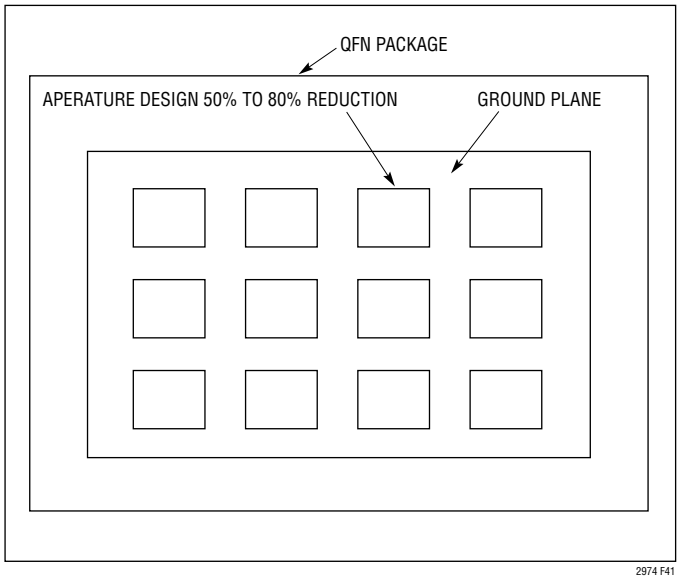


Figure 41. Suggested Screen Pattern for Die Attach Pad

PCB Board Layout

Mechanical stress on a PC board and soldering-induced stress can cause the LTC2974's reference voltage and the voltage drift to shift. A simple way to reduce the stress-related shifts is to mount the IC near the short edge of the PC board, or in a corner. The board acts as a stress boundary, or a region where the flexure of the board is minimal.

Unused ADC Sense Inputs

Connect all unused ADC sense inputs ($V_{SENSEP}n$, $V_{SENSEM}n$, $T_{SENSE}n$, $I_{SENSEP}n$ or $I_{SENSEM}n$) to GND. In a system where the inputs are connected to removable cards and may be left floating in certain situations, connect the inputs to GND using 100k resistors. Place the 100k resistors before any filter components, as shown in Figure 42, to prevent loading of the filter.

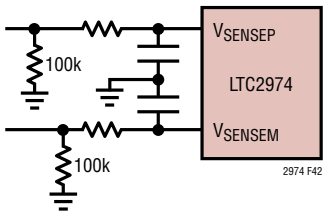


Figure 42. Connecting Unused Inputs to GND

APPLICATIONS INFORMATION

DESIGN CHECKLIST

I²C

- The LTC2974 must be configured for a unique address.
- The address select pins (ASEL*n*) are tri-level; Check Table 1.
- Check addresses for collision with other devices on the bus and any global addresses.

Output Enables

- Use appropriate pull-up resistors on all $V_{OUT\_EN}n$ pins.
- Verify that the absolute maximum ratings of the $V_{OUT\_EN}n$ pins are not exceeded.

V_{IN} Sense

- No external resistive divider is required to sense V_{IN}; V_{IN_SNS} already has an internal calibrated divider.

External Temperature Sense

- Verify the PNP sense transistor is close to the inductor and away from other significant heat sources.
- Verify the PNP sense transistor emitter routes to the LTC2974, and the base and collector connect to signal ground near the LTC2974.

Logic Signals

- Verify the absolute maximum ratings of the digital pins (SCL, SDA, ALERTB, FAULTB*n*, CONTROL*n*, SHARE_CLK, WDI, ASEL*n*, PWRGD) are not exceeded.
- Connect all SHARE_CLK pins in the system together and pull up to 3.3V with a 5.49k resistor.
- Do not leave CONTROL*n* pins floating. Pull up to 3.3V with a 10k resistor.
- Tie WDI/RESETB to V_{DD33} with a 10k resistor. Do not connect a capacitor to the WDI/RESETB pin.
- Tie WP to either V_{DD33} or GND. Do not leave floating.

Unused Inputs

- Connect all unused $V_{SENSEP}n$, $V_{SENSEM}n$, $I_{SENSEP}n$, $I_{SENSEM}n$, and $T_{SENSE}n$ pins to GND. Do not float unused inputs. Refer to Unused ADC Sense Inputs in the Applications Information section.

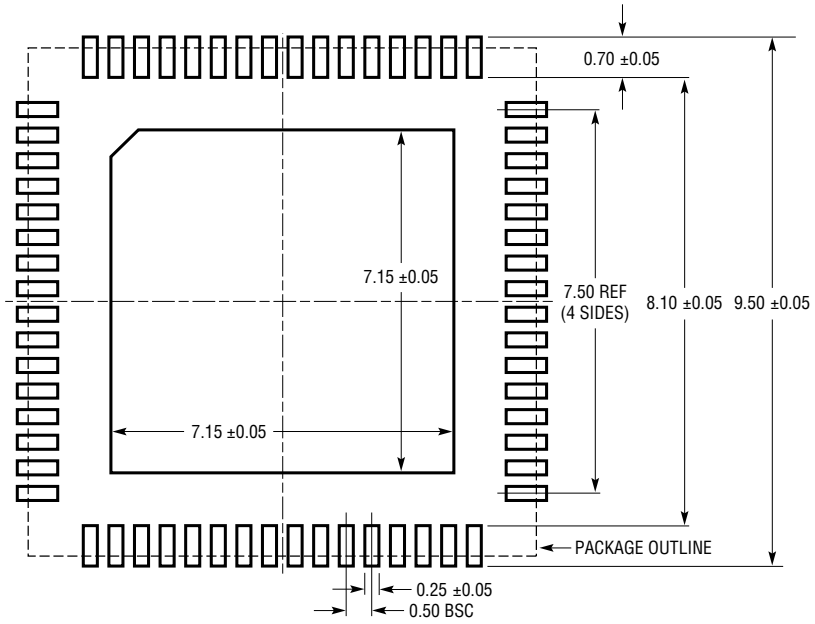
DAC Outputs

- Select appropriate resistor for desired margin range. Refer to the resistor selection tool in LTpowerPlay for assistance.

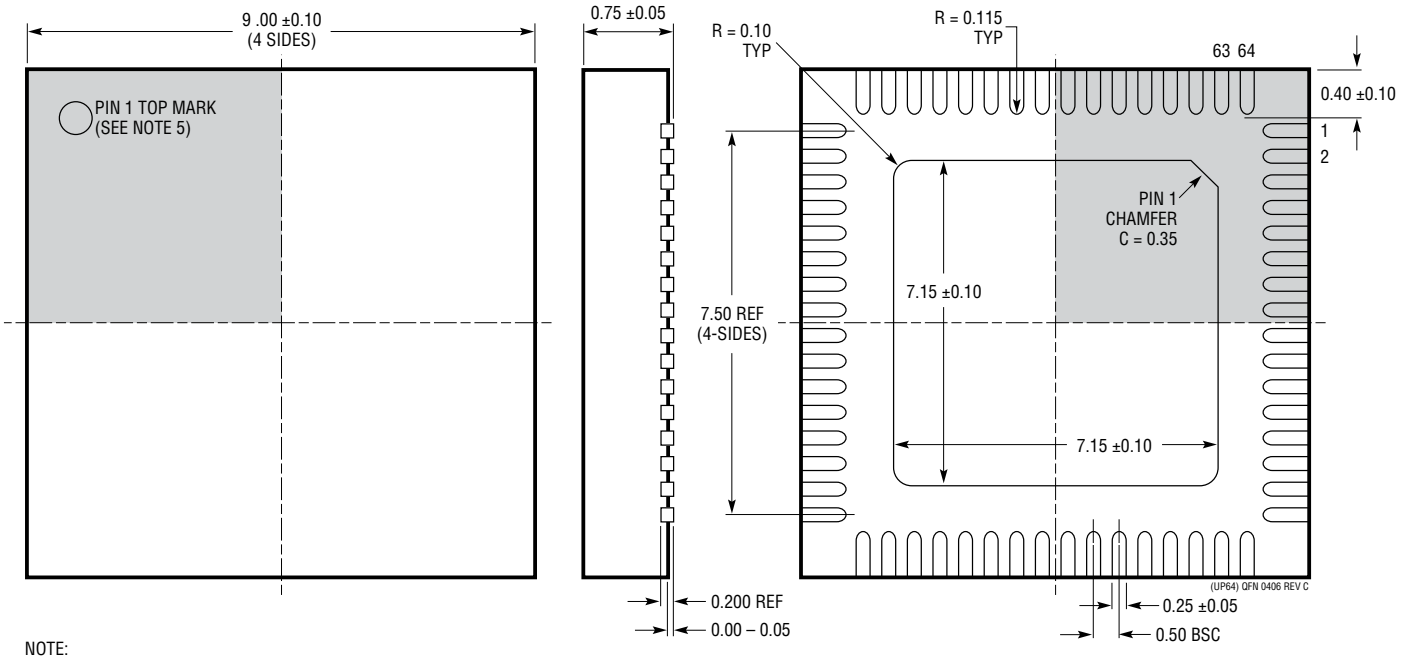
For a more complete list of design considerations and a schematic checklist, see the Design Checklist on the LTC2974 product page.

PACKAGE DESCRIPTION

UP Package
64-Lead Plastic QFN (9mm × 9mm)
(Reference LTC DWG # 05-08-1705 Rev C)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



BOTTOM VIEW—EXPOSED PAD

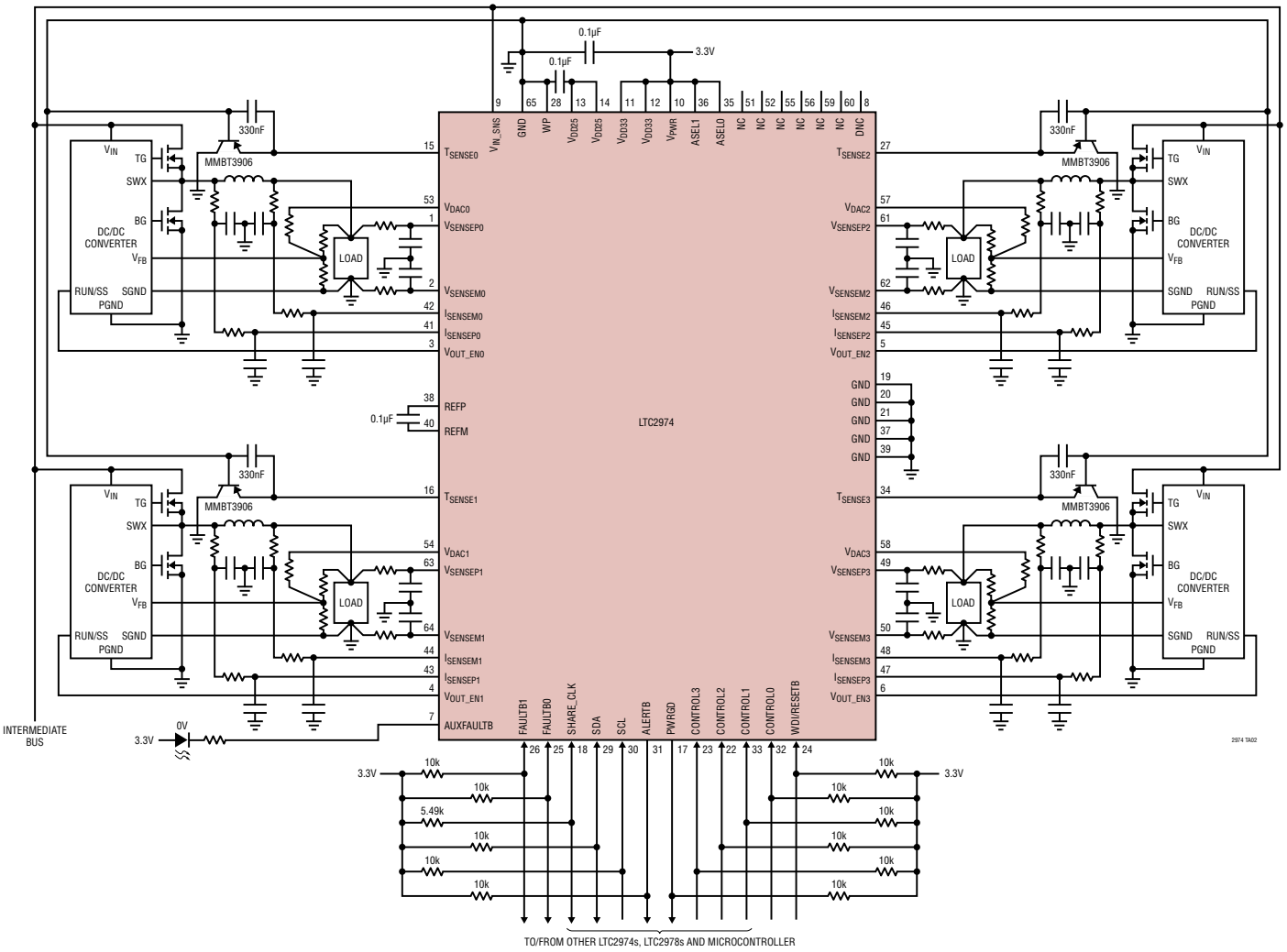
NOTE:
1. DRAWING CONFORMS TO JEDEC PACKAGE OUTLINE MO-220 VARIATION WNJR-5
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE
   MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE, IF PRESENT
4. EXPOSED PAD SHALL BE SOLDER PLATED
5. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE
6. DRAWING NOT TO SCALE

Rev. E

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	5/13	Title, Features and Description revised.	1
		Added specifications: t_{INIT}, t_{UPDATE_ADC}, t_{OFF_MIN}.	5, 9
		Changed V_{FS_VDAC} minimums to 1.3 and 2.5 from 1.32 and 2.53.	6
		Curve G08: Corrected Y-axis units from mA to µA.	10
		Block Diagram revised.	15
		RESETB section: Clarified I^2C disabled, 10k resistor and capacitance.	18
		Typical Delay numbers in EEPROM Related Commands table updated.	19
		TON_RISE Description: Changed "output starts to rise" to "$V_{OUT\_EN}n$ pin goes high."	24, 51
		Changed data format for MFR_DAC and MFR_I2C_BASE_ADDRESS to Reg from U16. Changed default value for MFR_SPECIAL_ID to 0x0213 from 0x0212.	26, 44
		Removed U16 row from Data Formats table.	27
		Operation, ON_OFF_CONFIG sections: Added sentence on waiting a t_{OFF_MIN}.	30, 31
		b[5:4] Operation: Added warning about undefined MFR_DAC.	32
		b[3] to b[0] Operation: Clarified that setting these bits disables UV and UC.	36
		Changed Format for MFR_RETRY_COUNT to Reg from U16.	54
		STATUS_VOUT b[3] Operation: Clarified behavior after bit is cleared.	62
		STATUS_MFR_SPECIFIC section: Added STICKY, ALERT, OFF columns; removed FAULT column. Added column definitions above table.	64
		STATUS_MFR_SPECIFIC b[6] and b[5]: Clarified behavior if MFR_TRACK_EN_CHANn is set.	64
		MFR_VOUT_MIN: Clarified when updates are disabled.	69
		MFR_FAULT_LOG_CLEAR: Clarified conditions before issuing this command.	71
		MFR_SPECIAL_ID: Changed value from 0x0210 to 0x0213.	78, 79
		Added section: Unused ADC Sense Inputs.	94
B	8/13	Updated V_{OS_CMP} Offset Voltage specification.	7
		$V_{VOUT\_EN}n$ Output High Voltage specification changed from 11.6V minimum to 10V.	7
C	10/13	$V_{AUXFAULTB}$ Output High Voltage specification: Changed minimum from 12V to 10V.	7
D	9/19	Updated Typical Application; added EEPROM ECC information.	1, 17
		Raised LTC2974I Operating Junction Temperature Range to 105°C and Storage Temperature Range to 150°C.	4
		Updated specifications: TUE_ADC_CURR_SNS, Sense Input Current Characteristics, t_{S_VDAC}, EEPROM Retention; removed I_{OS_CS}; added V_{VOUT_VALID}.	5 to 7
		Added Notes 3, 11; Updated Note 5; Updated Note numbers.	9
		Added graphs: Voltage and Current Input Currents vs Voltage (G08, G09, G26, G27), Closed-Loop Servo Error (G28), $V_{OUT\_EN[3:0]}$ Output Voltage vs V_{DD33} (G29).	10 to 13
		Updated V_{DD33}, V_{DD25}, SHARE_CLK pin functions.	14
		Updated EEPROM and AUXFAULTB sections.	18
		Updated Table 1, Figure 2, Figures 9 to 14.	21, 22
		Updated: default values for ON_OFF_CONFIG, IOUT_UC_FAULT_LIMIT, MFR_SPECIAL_ID, MFR_RETRY_COUNT; added MFR_INFO, MFR_COMMAND_PLUS, MFR_DATA_PLUS*n*.	23 to 28
		Updated Write Protect Pin section.	30
		Added MFR_COMMAND_PLUS and related sections.	31 to 33
		Updated: MFR_CONFIG_ALL_LTC2974 b[10] to reserved status and b[1]; MFR_EE_DATA bits and symbol.	43, 44, 47
		Updated: STATUS_WORD b[0], STATUS_VOUT b[3].	66
		Updated descriptions: MFR_READ_IOUT, all MFR commands on page 73.	72, 73
		Updated section on Configuring the AUXFAULTB Output and Figure 27.	88
		Added sections: Unused ADC Sense Inputs, Design Checklist.	101, 102
E	3/20	Updated default value for MFR_DAC	27

TYPICAL APPLICATION



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC2970	Dual I²C Power Supply Monitor and Margining Controller	5V to 15V, 0.5% TUE 14-Bit ADC, 8-Bit DAC, Temperature Sensor
LTC2975	4-Channel PMBus Power System Manager	0.25% TUE 16-Bit ADC, Voltage/Current/Temperature Monitoring and Supervision, Input Current and Power, Input Energy Accumulator
LTC2977	8-Channel PMBus Power System Manager	0.25% TUE 16-Bit ADC, Voltage/Temperature Monitoring and Supervision
LTC2980	16-Channel PMBus Power System Manager	Dual LTC2977
LTM2987	16-Channel µModule® PMBus Power System Manager	Dual LTC2977 with Integrated Passive Components
LTC3880	Dual Output PolyPhase Step-Down DC/DC Controller	0.5% TUE 16-Bit ADC, Voltage/Current/Temperature Monitoring and Supervision
LTC3883	Single Output PolyPhase Step-Down DC/DC Controller	0.5% TUE 16-Bit ADC, Voltage/Current/Temperature Monitoring and Supervision