30A Power/Energy Monitor with Integrated Sense Resistor

FEATURES

- **Measures Current, Voltage, Power, Charge, Energy**
- **±30A Current Range with Low 9mA Offset**
- **Integrated 300µΩ Sense Resistor**
- **0V to 15V Input Range Independent of Supply Voltage**
- **Instantaneous Multiplication of Voltage and Current**
- 0.5% Voltage Accuracy
- 1% Current and Charge Accuracy
- 1.2% Power and Energy Accuracy
- Alerts When Thresholds Exceeded
- Stores Maximum and Minimum Values
- Shutdown Mode with I_Q < 10µA
- I^2C/SPI Compatible Interface
- Available in 32-Lead 4mm × 6mm QFN Package

APPLICATIONS

- Servers
- Telecom Infrastructure
- Industrial
- Electric Vehicles
- Photovoltaics

DESCRIPTION

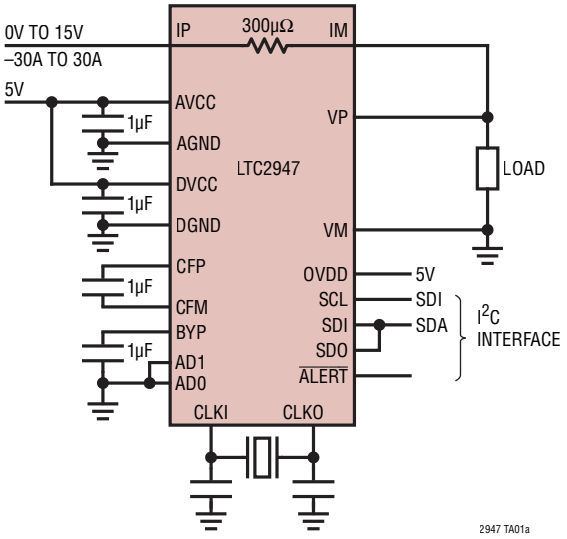
The LTC®2947 is a high precision power and energy monitor with an internal sense resistor supporting up to ±30A. Three internal No Latency ΔΣ™ ADCs ensure accurate measurement of voltage and current, while high-bandwidth analog multiplication of voltage and current provides accurate power measurement in a wide range of applications. Internal or external clocking options enable precise charge and energy measurements.

An internal 300µΩ, temperature-compensated sense resistor minimizes efficiency loss and external components, simplifying energy measurement applications while enabling high accuracy current measurement over the full temperature range.

All measured quantities are stored in internal registers accessible via the selectable I^2C/SPI interface. The LTC2947 features programmable high and low thresholds for all measured quantities to reduce digital traffic with the host.

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TYPICAL APPLICATION



Energy Measurement Total Unadjusted Error vs Current, VP – VM = 12V

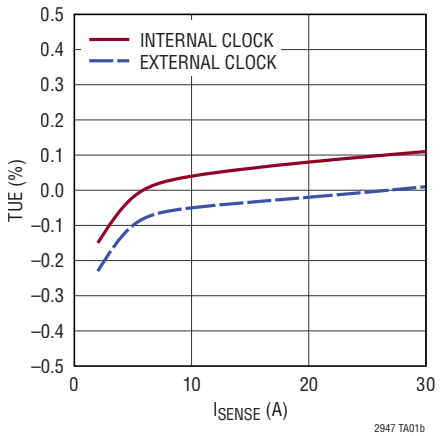


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ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

Supply Pins:
- AVCC to AGND Voltage ..... –0.3V to 20V
- DVCC to DGND Voltage..... –0.3V to 20V
- DGND to AGND Voltage ..... –0.1V to 0.1V

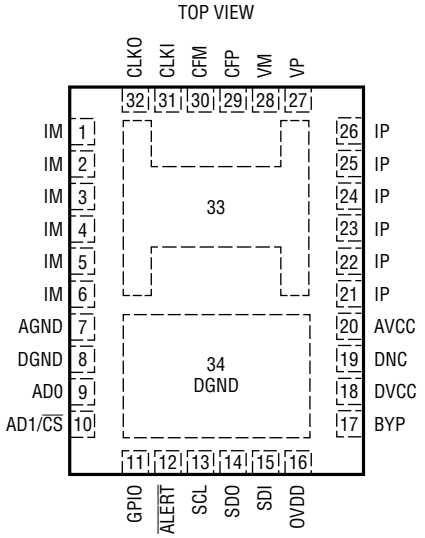
Digital Input/Output Pins:
- OVDD to DGND Voltage ..... –0.3V to 5.5V
- SCL, SDI, SDO, GPIO, $\overline{\text{ALERT}}$, AD1, AD0 to DGND Voltage .....–0.3V to V_{OVDD}
- CLKI to DGND Voltage ..... –0.3V to 5.5V

Analog Pins
- VP, VM to AGND Voltage..... –0.3V to 20V
- VP to VM Voltage..... –0.3V to 20V
- IP, IM Total Current (for 1ms)..... –50A to 50A
- IP, IM Total Current (Note 6) ..... –36A to 36A
- IP, IM Current Per Pin (for 1ms)..... –8.3A to 8.3A
- IP, IM Current Per Pin (Note 6) ..... –6A to 6A
- CFP, CFM, BYP, CLKO ..... (Note 3)

Operating Ambient Temperature Range
- LTC2947I ..... –40° to 85°C

Storage Temperature Range ..... –65° to 150°C

PIN CONFIGURATION



UFE PACKAGE
VARIATION: UFE32MA
32-LEAD PLASTIC QFN (4mm × 6mm)

T_{JMAX} = 125°C, θ_{JA} = 50°C/W
EXPOSED PAD (PIN 33); DO NOT CONNECT
EXPOSED PAD (PIN 34) IS DGND, MAY BE CONNECTED TO DGND OR LEFT FLOATING

ORDER INFORMATION

TUBE	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC2947IUFE#PBF	LTC2947IUFE#TRPBF	2947	32-Lead (4mm × 6mm) Plastic QFN	–40°C to 85°C

Contact the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Power Supply							
V_{AVCC}, V_{DVCC}	Supply Voltage		●	4.75		15	V
V_{OVDD}	Supply Voltage of Digital Interface		●	1.8		5.5	V
V_{UVLO}	V_{AVCC}, V_{DVCC} Undervoltage Lockout Threshold	V_{AVCC}, V_{DVCC} Falling	●			4.75	V
I_{AVCC}	Supply Current Analog Section	Continuous Mode Idle Mode Shutdown Mode Shutdown Mode	● ● ●		3 0.2 0.3 0.3	3.5 0.3 0.5 1	mA mA µA µA
I_{DVCC}	Supply Current Digital Section	Continuous Mode Idle Mode Shutdown Mode Shutdown Mode	● ● ●		6 6 7 7	8 8 9.5 90	mA mA µA µA
	Delay of $V_{AVCC,DVCC}$ to V_{OVDD} at Power-Up	V_{OVDD}, V_{AVCC}, $V_{DVCC} \geq 0.9 \bullet V_{OVDDfinal}$ (Note 8)	●	0			ns
Current Sense (IP, IM) ADC							
	Resolution (No Missing Codes)	(Note 5)	●	15			Bit
I_{SENSE}	Input Current Through IP and IM	(Note 6)	●			±30	A
R_{SENSE}	Internal Sense Resistor	(Note 7)	●	140	300	450	µΩ
	Sense Resistor Voltage	Current through IP and IM = 30A			9		mV
	Common Mode Input Voltage Range		●	–0.1		15.5	V
LSB_I	Current Sense Quantization Step				3		mA
	Current Gain Error		 ●			±0.75 ±1	% of reading % of reading
I_{OS}	Current Offset		 ●			±3 ±5	LSB LSB
INL_I	Current Integral Nonlinearity	(Note 6)	●			±0.3	%
TUE_I	Total Unadjusted Error	$\|I\| \geq 6A$ (Note 6)	 ●			±1 ±1.5	% of reading % of reading
	Input DC Common Mode Rejection		●	120			dB
	RMS Noise	(Note 5)			320		nV
	Sampling Rate				10.5		MHz
Voltage Sense (VP, VM) ADC							
	Resolution (No Missing Codes)	(Note 5)	●	14			bit
	Common Mode Voltage		●	0		15.5	V
V_D	Input Differential Voltage Range	$V_{VP} – V_{VM}$	●	–0.3		15.5	V
	V_D Quantization Step				2		mV
	Voltage Gain Error		●			±0.4	% of reading
	Voltage Offset		●			±2	LSB
INL_V	Voltage Integral Nonlinearity		●			±2	LSB
TUE_V	Voltage Total Unadjusted Error	$V_D \geq 4.0V$	●			±0.5	% of reading
	Input DC Voltage Common Mode Rejection		●	70			dB
	Sampling Rate				5.25		MHz

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Power Measurement							
	Resolution (No Missing Codes)	(Note 5)	●	18			bit
	Full-Scale Power				450		W
	Power Quantization Step				50		mW
	Power Gain Error		 ●			±0.8 ±1	% of reading % of reading
	Power Offset		 ●			±4 ±6	LSB LSB
INL_P	Power Integral Nonlinearity	|I| ≥ 6A, V_D ≥ 12V (Note 6)	 ●			±0.3 ±0.5	% of reading % of reading
TUE_P	Power Total Unadjusted Error	|I| ≥ 6A, V_D ≥ 12V (Note 6)	 ●			±1.2 ±1.5	% of reading % of reading
	Sampling Rate				5.25		MHz
Timing							
TUE_{TB}	Time Base Total Unadjusted Error	Internal Clock	 ●			±0.5 ±1	% of reading % of reading
		Ideal External Clock or Ideal 4MHz Crystal (Note 5)	●			±340	ppm
t_{UPDATE}	Update Time of Result Registers		●	95	100	105	ms
Energy Measurement							
TUE_E	Energy Total Unadjusted Error	|I| ≥ 6A, V_D ≥ 12V, Ideal External Clock (Note 6)	 ●			±1.2 ±1.5	% of reading % of reading
		|I| ≥ 6A, V_D ≥ 12V, Internal Clock (Note 6)	 ●			±1.5 ±2.5	% of reading % of reading
Charge Measurement							
TUE_C	Charge Total Unadjusted Error	|I| ≥ 6A, Ideal External Clock (Note 6)	 ●			±1 ±1.5	% of reading % of reading
		|I| ≥ 6A, Internal Clock (Note 6)	 ●			±1.5 ±2.5	% of reading % of reading
Temperature Measurement ADC							
	Resolution (No Missing Codes)	(Note 5)	●	13			bit
	Temperature Quantization Step				0.204		°C
	Temperature Error	(Note 5)			±5		K
Digital Inputs and Digital Outputs SCL, SDI, GPIO, $\overline{\text{ALERT}}$, SDO, $\overline{\text{CS}}$, CLKI, ADO							
V_{ITH}	Logic Input Threshold	SCL, SDI, GPIO, $\overline{\text{CS}}$, ADO	●	0.3 • V_{OVDD}		0.7 • V_{OVDD}	V
I_{IN}	Input Current SCL, SDI, GPIO		●			±1	µA
C_{IN}	Input Capacitance	(Note 5)	●			10	pF
V_{OL}	Low Level Output Voltage SDO, GPIO, $\overline{\text{ALERT}}$	V_{OVDD} ≥ 3.3V, I_{PIN} = 3mA 1.8V ≤ V_{OVDD} < 3.3V, I_{PIN} = 1mA	● ●			0.4 0.4	V V
V_{OH}	High Level Output Voltage (SDO)	I_{SDAO} = –0.5mA	●	V_{OVDD} – 0.5			V
	CLKI Input Threshold		●	0.4	0.7	2	V
	External Clock Frequency on Pin CLKI		●	0.2		25	MHz

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
AD1, AD0							
	Resistance Allowed on AD1 and AD0 When They Are Tied to OVDD or DGND to Set a Valid L or H Level	See Table 3	●			500	Ω
	Resistance to DGND to Set a Valid R Level		●	20	100	500	kΩ
	External Capacitive Load Allowed on AD1 and AD0 to Set a Valid R Level		●			100	pF
I²C Bus Timing							
$f_{SCL(MAX)}$	Maximum SCL Clock Frequency		●	400	900		kHz
$t_{BUF(MIN)}$	Bus Free Time Between STOP/START		●			1.3	µs
$t_{SU,STA(MIN)}$	Minimum Repeated START Setup Time		●			600	ns
$t_{HD,STA(MIN)}$	Minimum Hold Time (Repeated) START Condition		●			600	ns
$t_{SU,STO(MIN)}$	Minimum Set-Up Time for STOP Condition		●			600	ns
$t_{SU,DAT(MIN)}$	Minimum Data Set-Up Time Input		●			100	ns
$t_{HD,DAT(MIN)}$	Minimum Data Hold Time Input		●			0	ns
$t_{HD,DATO}$	Data Hold Time Output		●	300		900	ns
t_{RST}	Stuck Bus Reset Time	SCL or SDI Held Low	●	25	50		ms
t_{OF}	Data Output Fall Time	(Notes 4, 5)	●	20 + 0.1 • C_B			ns
SPI Bus Timing							
$t_{SPIDS(MIN)}$	Minimum SDI to SCL Data Setup		●			100	ns
$t_{SPIBUF(MIN)}$	Minimum SPI Bus Free Time Between Two $\overline{CS}$ Active States		●			4	µs
$t_{SPIDH(MIN)}$	Minimum SDI to SCL Data Hold		●			100	ns
$t_{SPICH(MIN)}$	Minimum SCL high state duration		●			500	ns
$t_{SPICL(MIN)}$	Minimum SCL low state duration		●			500	ns
$t_{SPIA1S(MIN)}$	Minimum $\overline{CS}$ to First SCL Setup Time		●			50	ns
$t_{SPIA1H(MIN)}$	Minimum $\overline{CS}$ to Last SCL Hold Time		●			50	ns
t_{HDSDO}	SDO to SCL High to Low Output Hold Time		●	50		350	ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Positive currents flow into pins; negative currents flow out of pins. Minimum and maximum values refer to absolute values.

Note 3: Do not apply a voltage or current source to these pins. They must be connected to capacitive loads only. Pin CLKO may also be connected to a crystal as desired. Otherwise permanent damage may occur.

Note 4: C_B = capacitance of one bus line in pF (10pF ≤ C_B ≤ 400pF).

Note 5: Guaranteed by design and characterization, not subject to test.

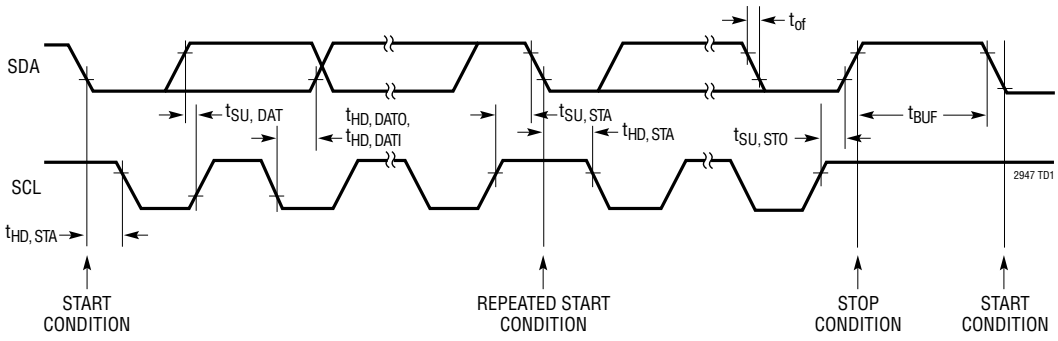
Note 6: Guaranteed by design and test correlation.

Note 7: R_{SENSE} value is internally compensated for the actual value of the sense resistor.

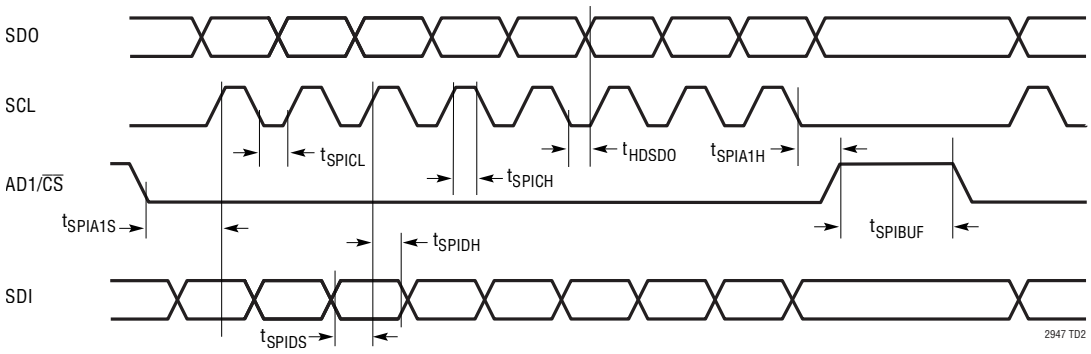
Note 8: $V_{OVDDfinal}$ is the supply voltage value at OVDD at the end of its settling at power-up.

TIMING DIAGRAMS

Definition of Timing on I²C Bus

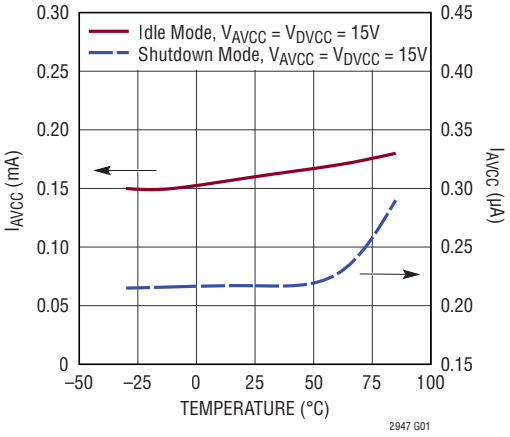


Definition of SPI Timing

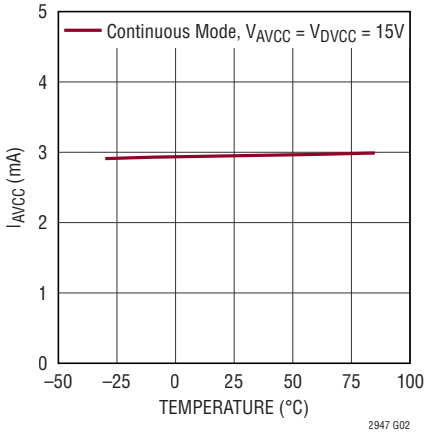


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

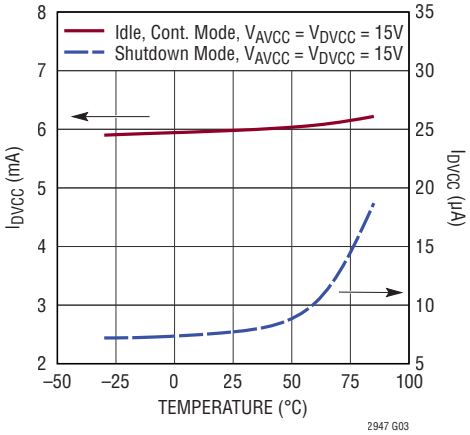
AVCC Supply Current vs Temperature



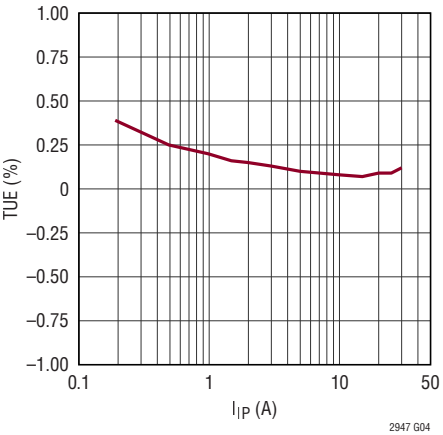
AVCC Supply Current Continuous Mode vs Temperature



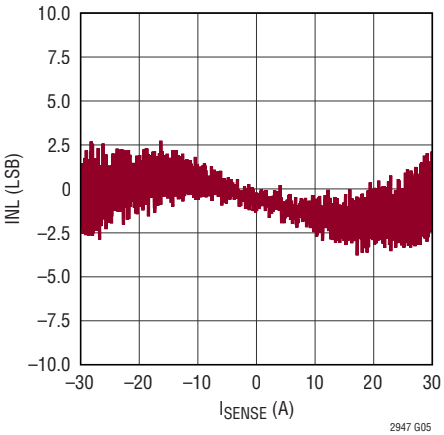
DVCC Supply Current vs Temperature



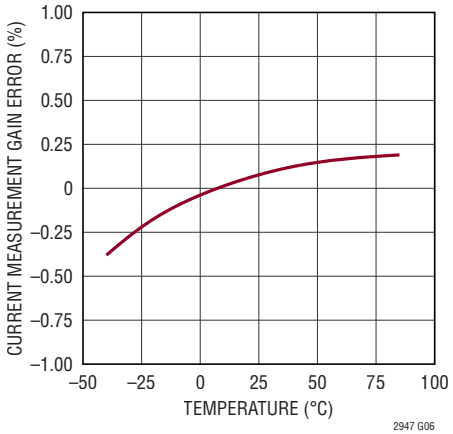
Current Measurement Total Unadjusted Error



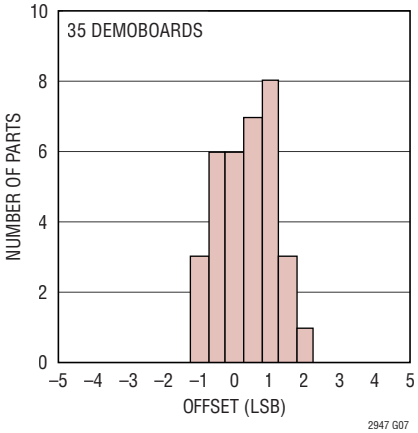
Current Measurement Integral Nonlinearity



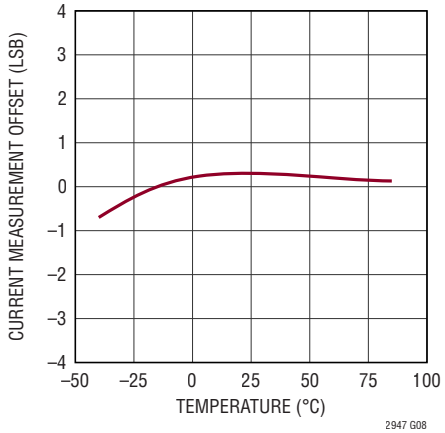
Current Measurement Gain Error vs Temperature



Current Measurement Offset Distribution

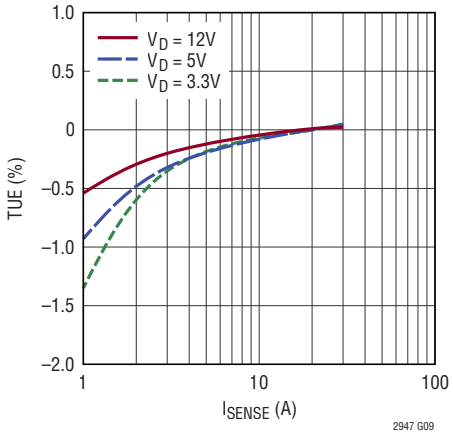


Current Measurement Offset vs Temperature

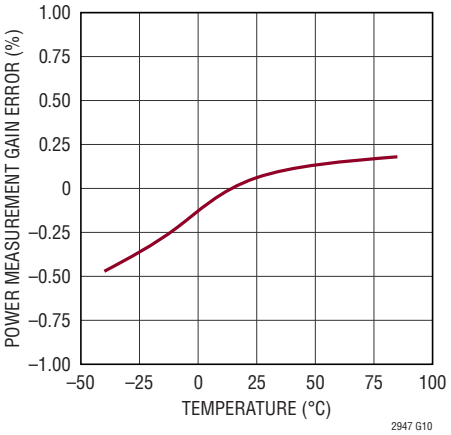


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

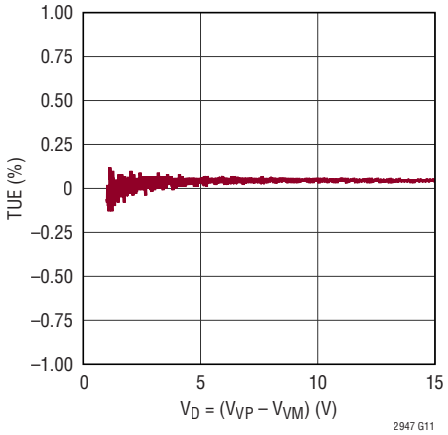
Power Measurement Total Unadjusted Error



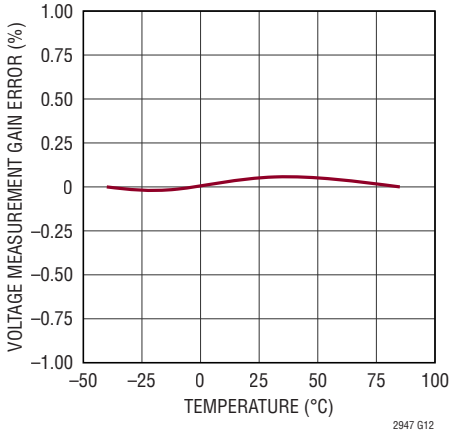
Power Measurement Gain Error vs Temperature



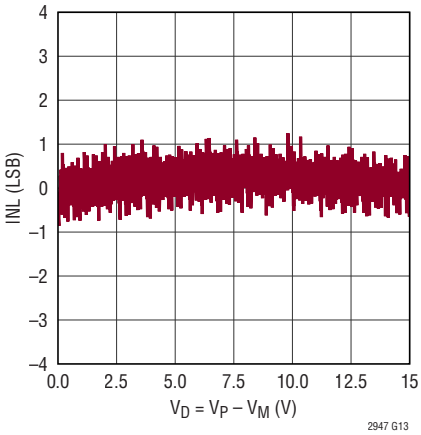
Voltage Measurement ADC Total Unadjusted Error



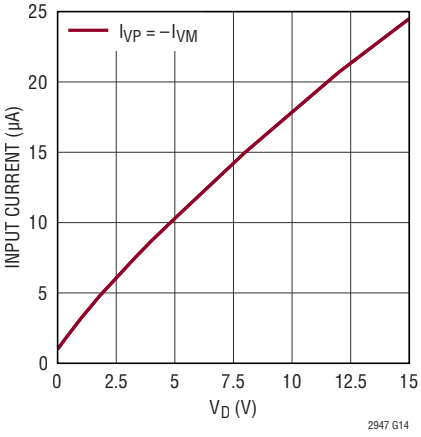
Voltage Measurement Gain Error vs Temperature



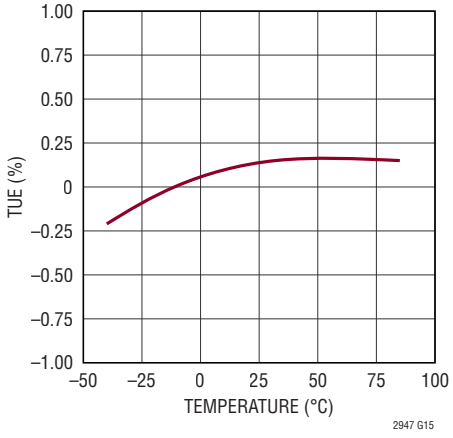
Voltage Measurement Integral Nonlinearity



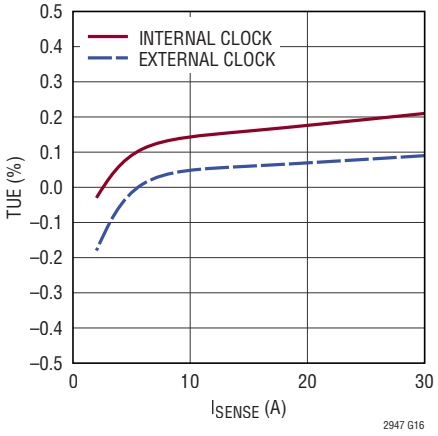
VP, VM Input Current vs VP, VM Sense Voltage



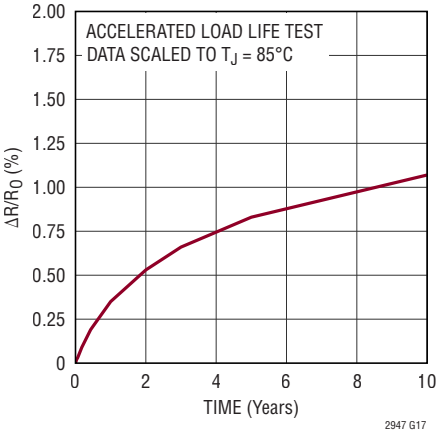
Time Base Total Unadjusted Error vs Temperature



Charge Measurement Total Unadjusted Error vs Current



Sense Resistor Stability



PIN FUNCTIONS

IM (Pins 1, 2, 3, 4, 5, 6): Negative Current Input. Connects to internal current sense resistor. All six pins must be tied together.

AGND (Pin 7): Analog Ground. See Layout Considerations in the Applications Information section.

DGND (Pin 8): Digital Ground. See Layout Considerations in the Applications Information section.

AD0 (Pin 9): Address Input 0. To select SPI mode, tie AD0 to OVDD. For I²C mode, tie AD0 to ground, either directly (L) or through a 100kΩ resistor (R), to select one of six I²C addresses. See Table 3 in the Applications Information section for details.

AD1/$\overline{CS}$ (Pin 10): Address Input 1 / Chip Select. In SPI mode, this is the Chip Select input, active low. In I²C mode, tie to OVDD (H), DGND (L), or through a 100kΩ resistor to ground (R) to select one of six I²C addresses. See Table 3 in the Applications Information section for details.

GPIO (Pin 11): General Purpose I/O (Open Drain). Connect through a pull-up resistor to OVDD. Tie to ground if unused.

$\overline{ALERT}$ (Pin 12): Alert Output. $\overline{ALERT}$ behaves as an open-drain logic output that pulls to ground if an unmasked Threshold register is exceeded or an unmasked error condition is detected. When the interface is operating in I²C mode, the $\overline{ALERT}$ pin follows the SMBus ARA (Alert Response) protocol. See the I²C Mode section for more information. Tie $\overline{ALERT}$ to ground if unused.

SCL (Pin 13): Serial Clock. Serial clock input in both I²C and SPI Modes.

SDO (Pin 14): Serial Data Output. Data output in both I²C and SPI modes. In I²C mode, this pin may be tied to SDI to act as a standard bidirectional SDA pin, or kept separate to ease opto-isolation.

SDI (Pin 15): Serial Data Input. Data input in both I²C and SPI modes. In I²C mode, this pin may be tied to SDO to act as a standard bidirectional SDA pin, or kept separate to ease opto-isolation.

OVDD (Pin 16): Digital Interface Supply. Connect a 1µF bypass capacitor from OVDD to DGND. The voltage at OVDD must reach 90% of its final value at the same time or before the voltage at AVCC/DVCC reaches this voltage level.

BYP (Pin 17): Internal 2.5V Voltage Supply for Powering Internal Circuitry. Do not load. Connect a 1µF bypass capacitor to DGND.

DVCC (Pin 18): Digital Power Supply. Connect a 1µF bypass capacitor from DVCC to DGND. AVCC and DVCC should be connected together.

DNC (Pin 19): Do Not Connect.

AVCC (Pin 20): Analog Power Supply. Connect a 1µF bypass capacitor from AVCC to AGND. AVCC and DVCC should be connected together.

IP (Pins 21, 22, 23, 24, 25, 26): Positive Current Input. Connects to internal current sense resistor. All six pins must be tied together.

VP (Pin 27): Positive Voltage Sense Input. Connect to the positive terminal of the voltage to be measured. A 22Ω series resistor and a 2.2µF bypass capacitor to VM is recommended.

VM (Pin 28): Negative Voltage Sense Input. Connect to the negative terminal of the voltage to be measured. A 22Ω series resistor and a 2.2µF bypass capacitor to VP is recommended.

CFP (Pin 29): Positive Filter Pin. Connect a 1µF bypass capacitor between CFP and CFM and a 0.1µF common mode capacitor from CFP to AGND.

CFM (Pin 30): Negative Filter Pin. Connect a 1µF bypass capacitor between CFP and CFM and a 0.1µF common mode capacitor from CFM to AGND.

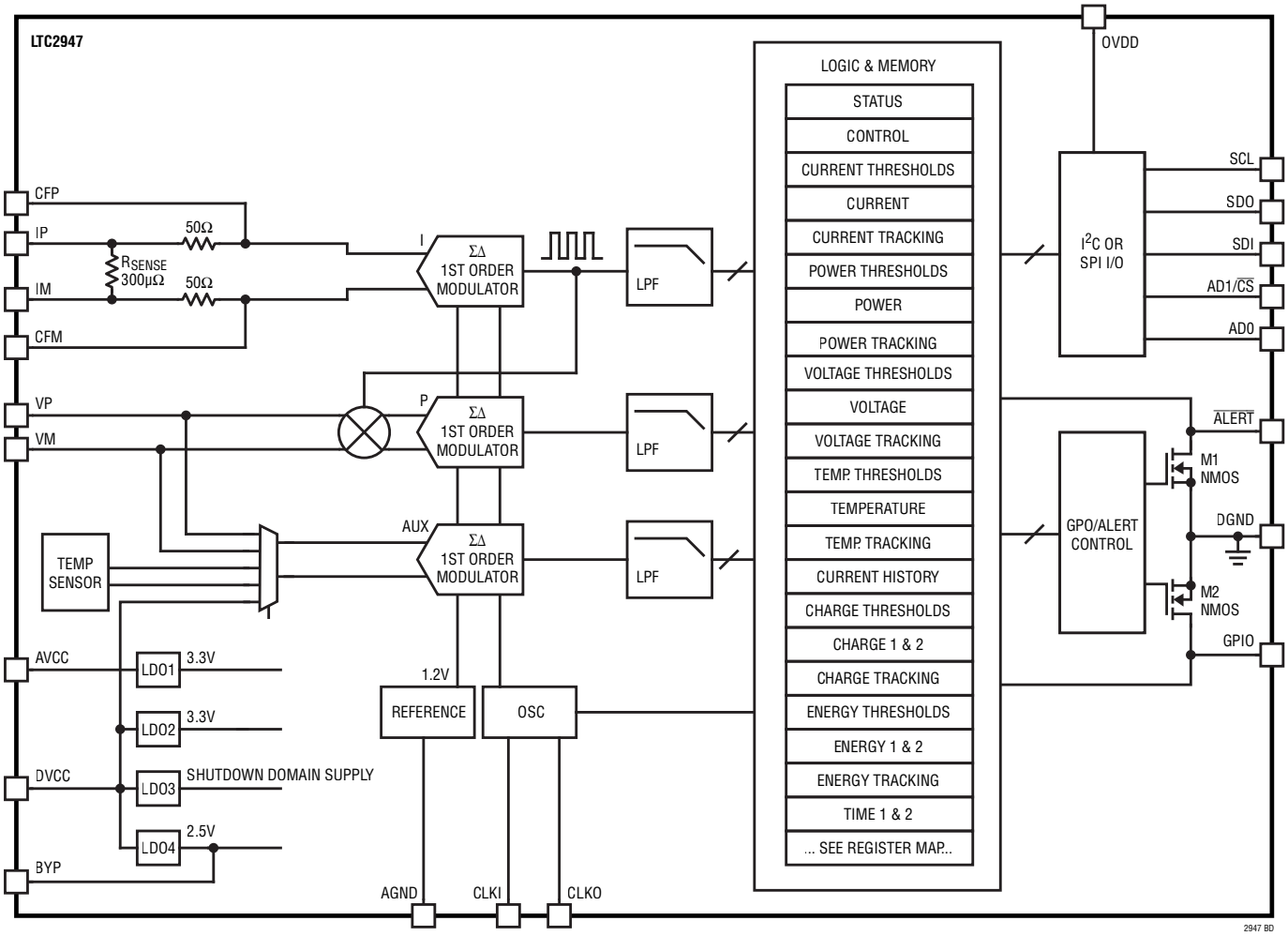
CLKI (Pin 31): Clock Input. Connect to ground if the internal clock is used. For improved accuracy, connect a crystal between CLKI and CLKO and matching capacitors to ground, or drive CLKI with an external clock. See the Timebase Control section for more information.

CLKO (Pin 32): Clock Output. Connect a crystal between CLKO and CLKI if used; leave floating otherwise.

EXPOSED PAD 1 (Pin 33): Internal current sense resistor. Do not connect to any metal or other conducting material. See the Layout Considerations section for more information.

DGND (Pin 34): Exposed Pad. Connect to DGND or leave floating.

BLOCK DIAGRAM



OPERATION

OVERVIEW

The LTC2947 is a high precision power and energy meter with integrated sense resistor for currents up to ±30A and voltages as high as 15V. It measures a total of seven parameters: current, voltage, power, charge (coulombs), energy, and run time, as well as its own chip temperature.

It includes three No Latency ΔΣ analog-to-digital converters to simultaneously measure current, voltage, and power. It also measures die temperature and derives the accumulated quantities charge, energy, and time using an external clock or an on-board oscillator. It stores these values in internal registers that can be read out via the serial interface, configurable as either I^2C or SPI.

The LTC2947 keeps track of the minimum and maximum measured values for each of the measured quantities. Thresholds can be set for each parameter, and the LTC2947 will set the corresponding bit in the Alert register and optionally alert the host by pulling low on the $\overline{\text{ALERT}}$ pin when a threshold is exceeded.

A GPIO pin is included that can be used for four different purposes. It can be configured as a general-purpose-logic input or output, as an output to automatically control a fan based on the LTC2947's internal silicon temperature measurement or as an input to enable and disable accumulation of charge, energy, and time.

MODES OF OPERATION

Power Up

When all power supply voltages have risen above their UVLO thresholds, the LTC2947 boots up, sets all registers to their default state, and enters IDLE mode, where it waits for further instructions from the host. The LTC2947 requires about 100ms to boot up and enter the IDLE mode.

IDLE

In IDLE mode, all internal circuitry is active but no measurements are being made. From IDLE, the LTC2947 can be instructed to go into single shot, continuous, or shutdown modes via the Operation Control control register.

Single Shot (SSHOT):

When the SSHOT bit in the Operation Control register is set, the LTC2947 takes four measurements (current, voltage, power, and temperature), and updates the corresponding registers and the Minimum/Maximum and Threshold registers. No time measurements are made and the Charge and Energy registers are not updated. It then clears the SSHOT bit in the Operation Control register, sets the UPDATE bit in Status register and returns to the IDLE mode. One single shot measurement cycle takes 100ms. The host can poll the UPDATE bit in the Status register to detect the completion of the measurement cycle.

Continuous Measurement Mode (CONT)

When the CONT bit in the Operation Control register is set, the LTC2947 repeatedly measures current, voltage, power, and temperature, recalculates energy, charge, time and updates the Minimum/Maximum Tracking and Threshold registers. Each measurement cycle takes about 100ms. The current and power ADCs run continuously in this mode, ensuring that no charge or energy is missed. The LTC2947 remains in continuous mode until bit CONT of the Operation Control register is reset by the user. If the SSHOT bit is set while in continuous mode, the LTC2947 completes the current measurement cycle and then enters single shot mode, clearing the CONT bit in the Operation Control register.

Shutdown (SHDN):

When the SHDN bit in the Operation Control register is set, the LTC2947 goes into shutdown mode, and supply current reduces to about 10μA. If the device is in the middle of a measurement cycle, in either single shot or continuous mode, it completes the cycle before entering shutdown and clearing the SSHOT or CONT bits. Shutdown clears the voltage, current, and temperature results, but preserves the values of the accumulated quantities charge and energy and all threshold and tracking values.

While in shutdown mode, the LTC2947 continues to monitor the serial interface. In SPI mode, the LTC2947 transitions from shutdown to IDLE when $\overline{\text{CS}}$ goes low. In I^2C mode,

OPERATION

the LTC2947 transitions to IDLE after acknowledging the correct slave address. The LTC2947 requires about 100ms to wake up from shutdown. During this time, it ignores register writes and responds to register reads with 0x01. Once awake, the LTC2947 goes into IDLE mode and waits for further instructions. The host can poll the Operation Control register and watch for a 0x00 response to determine that the LTC2947 is awake and in IDLE mode.

In shutdown mode, the internal analog and digital supplies are switched off. This causes the UVLOA and UVLOD bits to be set when the LTC2947 resumes from shutdown. The UVLOSTBY bit and the PORA bit are only set if the supply voltage at AVCC/DVCC drops below V_{UVLO} and a power-on reset has occurred.

The state diagram (Figure 1) summarizes the different modes of operation of LTC2947. Transitions and control bit settings initiated by the user are marked in black while transitions and control bit settings caused by the device are marked in blue.

Switching between operating modes can require up to 100ms if a measurement cycle is in progress.

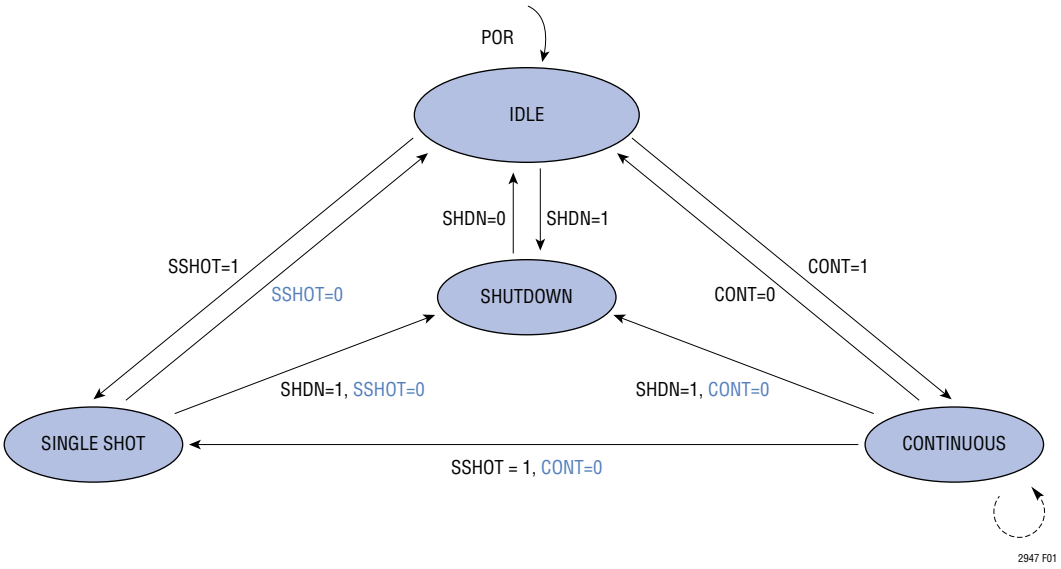


Figure 1. Modes of Operation

OPERATION

CURRENT, VOLTAGE AND TEMPERATURE MEASUREMENT

The LTC2947 measures each input with an ADC specifically tailored for the task. Current through the internal sense resistor is measured with a ΔΣ ADC that has a measurement range of ±30A and a resolution of 3mA. The common mode voltage can range from 100mV below GND up to 15.5V, regardless of the supply voltage at AVCC. This ADC uses a first-order architecture and continuous offset calibration to ensure that all input samples are averaged with equal weight and none are missed—the current ADC is never "blind." A 10MHz sampling rate maintains averaging accuracy for all current waveforms including harmonics up to 2.5MHz. A new average value is reported every 100ms.

A second ADC sequentially measures both temperature and differential voltage between the VP and VM pins while the current measurement is being made. The temperature measurement is both reported to the host and used internally by the LTC2947 to compensate for the temperature drift of the internal current sense resistor, resulting in very stable current measurements. The voltage measurement has a 2mV resolution and temperature has a 0.204°C resolution. The differential voltage measurement range (VP-VM) ranges from –0.3V to 15.5V, independent of supply voltage.

Note that the temperature measurement is made with a sensor on the die, which can vary significantly from ambient temperature if the current in the internal sense resistor is high. A high supply voltage at AVCC/DVCC increases the internal power and will also increase the internal temperature.

POWER MEASUREMENT

The LTC2947 measures power with a third ADC that multiplies voltage (VP-VM) and current at the full 5MHz sampling frequency, prior to any averaging due to the analog-to-digital conversion. This maintains accuracy even if current and voltage change in phase during the 100ms conversion time, which can happen if the power is drawn from a source with significant impedance, such as a battery. Figure 2 shows an example of a 12V supply dropping to 11V due to internal series resistance when 9A current pulses are drawn by a load. In this example, the multiplication of average current with average voltage would lead to a 6% error in the calculated power as the voltage is significantly lower than the average voltage at the moments where the current is drawn. The scheme used by the LTC2947 avoids this error, maintaining specified accuracy with signals up to 50kHz.

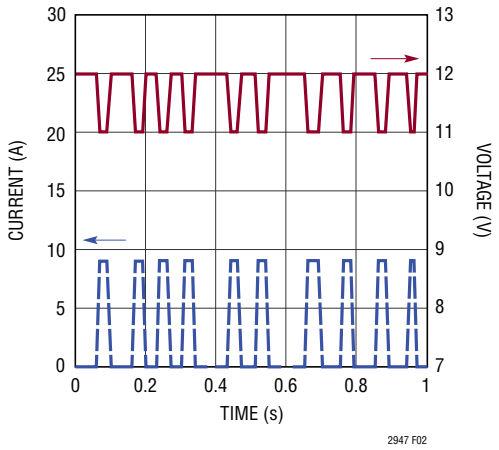


Figure 2. Power Measurement of Transient Signals

CHARGE, ENERGY MEASUREMENT AND ACCUMULATED TIME

The LTC2947 integrates the current and power measurements over time to calculate charge and energy flowing to or from the load. It also keeps track of total accumulated time used for the integration. The integration time base can be provided by the internal clock, an external clock attached to CLKI, or an external crystal connected to CLKI and CLKO. If an external clock is used, the LTC2947 presents time, charge and energy as a mathematical relationship to the external clock period.

For each of the quantities charge, energy, and time, the LTC2947 provides two sets of registers. Each register set can be separately configured to accumulate either based on the sign of the measured current, or by the level of the GPIO pin, or by the Control register settings. This allows the first set of accumulation registers to be configured to always integrate while the second set only integrates if current is positive (to account for battery charging efficiency, for example). A minimum current threshold can also be set below which integration is stopped.

APPLICATIONS INFORMATION

TIMEBASE: INTERNAL/EXTERNAL CLOCK/CRYSTAL

Accurately measuring charge and energy by integrating current and power requires a precise timing. The LTC2947 uses either a trimmed internal oscillator or an external clock as the time base for determining the integration period. It can use either an external square wave clock in a frequency range between 200kHz and 25MHz or a 4MHz crystal as an external clock input. If an external square wave is used, it should be connected to the CLKI pin and the CLKO pin should be left floating. Figure 3 shows the recommended circuit if a crystal is used to generate the reference clock.

When the internal clock is used, tie CLKI to DGND and leave CLKO floating.

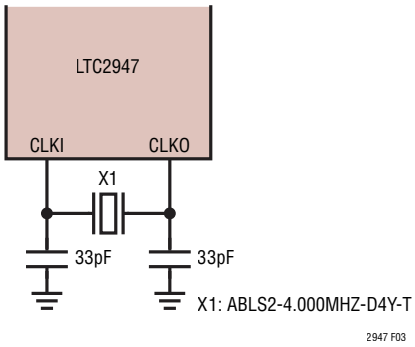


Figure 3. Reference Clock with a Crystal

Timebase Control

The LTC2947 uses the internal oscillator by default. If an external clock or a crystal is used, the PRE and DIV parameters in the Timebase Control register need to be set appropriately. The LTC2947 then compares its internal clock to the external frequency and represents time, charge, and energy as multiples of the external clock period. To accommodate the large range of allowed external frequencies, an internal pre-scaler must be configured via the Timebase Control register (0xE9).

The prescaler consists of 2 stages, with the first dividing the external frequency f_{REF} by a factor 2^{PRE}, and the second by a factor DIV. PRE is set between 0 and 5 with bits [2:0] of the Timebase Control register (0xE9). PRE should be set to the lowest value that gives less than 1MHz when dividing the external frequency by 2^{PRE} as shown in Table 1:

Table 1. Parameter PRE with External Clock

f_{REF}	PRE	2^{PRE}	PRE[2:0]
0.1MHz ≤ f_{REF} ≤ 1MHz	0	1	000
1MHz < f_{REF} ≤ 2MHz	1	2	001
2MHz < f_{REF} ≤ 4MHz	2	4	010
4MHz < f_{REF} ≤ 8MHz	3	8	011
8MHz < f_{REF} ≤ 16MHz	4	16	100
16MHz < f_{REF} ≤ 25MHz	5	32	101
Internal	7	–	111

The second stage of the prescaler then divides the result by a factor DIV. DIV is set between 0 and 31 by bits [7:3] of the Timebase Control register. DIV should be set to the next lower integer value of the ratio between the output of the first stage of the prescaler ($f_{REF_1} = f_{REF}/2^{PRE}$) and 32768Hz or, in other terms:

$$DIV = floor\left(\frac{f_{REF}}{2^{PRE} \bullet 32768Hz}\right)$$

If a 4MHz crystal is used, the values are: PRE=2, DIV=30.

The QuikEval™ software for the LTC2947 contains an easy-to-use calculator for these parameters.

Table 2 gives a few examples for common frequencies:

Table 2. Timebase Settings For Common Frequencies

f_{REF} (MHz)	PRE	2^{PRE}	f_{REF_1} (MHz)	DIV	TIMEBASE CONTROL [7:0]
1MHz	0	1	1	30	1111 0000
1.5MHz	1	2	0.75	22	1011 0001
4MHz	2	4	1	30	1111 0010
10MHz	4	16	0.625	19	1001 1100
20MHz	5	32	0.625	19	1001 1101
25MHz	5	32	0.781	23	1011 1101
Internal	7	–	–	X	XXXX X111

CONFIGURING THE GPIO PIN

The LTC2947 has one GPIO pin that can be configured to be a general purpose input or a general purpose open drain output by means of the bit GPOEN in the GPIO Status and Control register (0x67)[0].

APPLICATIONS INFORMATION

When the GPIO pin is configured as an input by setting 0x67[0]=0, the status of the GPIO pin is reported by the GPI bit of the GPIO Status and Control register at (0x67)[4]. The state of the general purpose input pin can be used to control the accumulation of charge, energy and time by means of the Accumulator Control GPIO register (0xE3). This accumulation function can be enabled separately for each of the two sets of accumulation registers. Setting bits (0xE3)[1:0] to [01] enables accumulation of Charge1, Energy1 and Time1 when GPIO is 1, while setting bits (0xE3)[1:0] to [10] enables accumulation of Charge1, Energy1 and Time1 when GPIO is 0. Setting bits (0xE3)[1:0] to [00] disables the accumulation control of the first set of accumulation registers by the GPIO level. Similarly, accumulation of Charge2, Energy2 and Time2 can be controlled by bits (0xE3)[3:2] of the accumulation control GPIO Register.

When the GPIO pin is configured as an open drain output by setting (0x67)[0]=[1], it can be pulled low by writing bit GPO in the GPIO Status and Control register (0x67)[5] to 0 or released high by writing bit GPO to 1. As an open drain output, the GPIO pin can also be configured to control a fan as a function of measured temperature by setting bit FANEN (0x67)[6] to 1. Then, the GPIO pin becomes active as soon as a temperature measurement result is above the threshold TFANH written at (page1.0x9C) and (page1.0x9D), and is deactivated if the temperature falls below the threshold TFANL written at (page1.0x9E) and (page1.0x9F). The polarity of the GPIO pin can be configured by setting bit FANPOL at (0x67)[7] to 0 or 1, respectively. The GPIO output level is maintained in shutdown. Since the internal sampling rate of the GPIO state is 100ms the reaction on any change of that state as input or output may be in this time range.

INTERNAL SENSE RESISTOR

The LTC2947 uses proprietary techniques to compensate for the internal sense resistor's temperature coefficient. A factory trim of both absolute value and tempco compensation, together with an ultralow offset ADC, contribute to the LTC2947's superior accuracy when current measurement is involved (i.e. current, power, charge, energy).

Like all sense resistors, the integrated sense resistor in the LTC2947 will exhibit minor long-term resistance shifts. See the Typical Performance Characteristics section for expected resistor drift performance under worst-case conditions. Drift will be much less at lower temperatures and/or currents.

CURRENT AND VOLTAGE INPUT FILTERING

To ensure the full electrical performance of the ADCs for current, power and voltage, apply the input filtering circuitry as shown in Figure 4 to pins CFP, CFM, VP and VM. These components provide optimum input filtering for noise reduction. Equal time constants at the current and voltage inputs minimize errors in power measurement of transient signals due to different delays in each path.

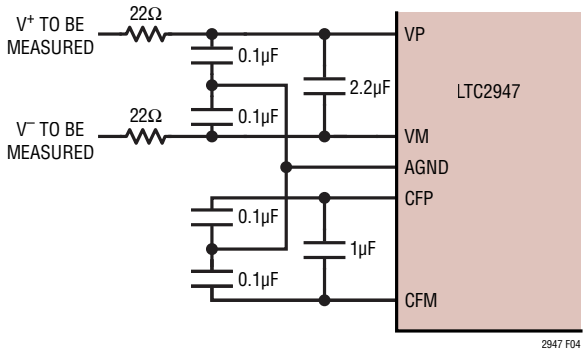


Figure 4. Input Filtering

APPLICATIONS INFORMATION

LAYOUT CONSIDERATIONS

Lowering the electrical resistance of the PCB traces to the IP and IM pins minimizes heating of the area near the LTC2947 and the temperature increase of the LTC2947 itself. Methods to lower the electrical resistance of the PCB traces include increasing the width of these traces and the number of PCB layers and including a sufficient number of vias as shown in Figure 5.

When connecting to the IP and IM pins, it is recommended to use PCB traces with a 70µm minimum thickness or greater. The current reading value is slightly dependent on the thickness of IP and IM PCB traces below 70µm. If thinner traces are used, Figure 6 shows the correction factor with which the Current LSB is to be multiplied to increase the accuracy. Since the Current reading is involved also in Power, Charge and Energy reading, the correction factor is to be taken into account in these quantities, too.

The exposed pad between IP and IM must not have contact or be soldered to any electrically conducting PCB pad or track.

The input filter common-mode capacitors and pins CFP and CFM should be star-connected directly to the AGND pin. Any unrelated ground currents in this connection will cause measurement errors. This can be achieved by combining

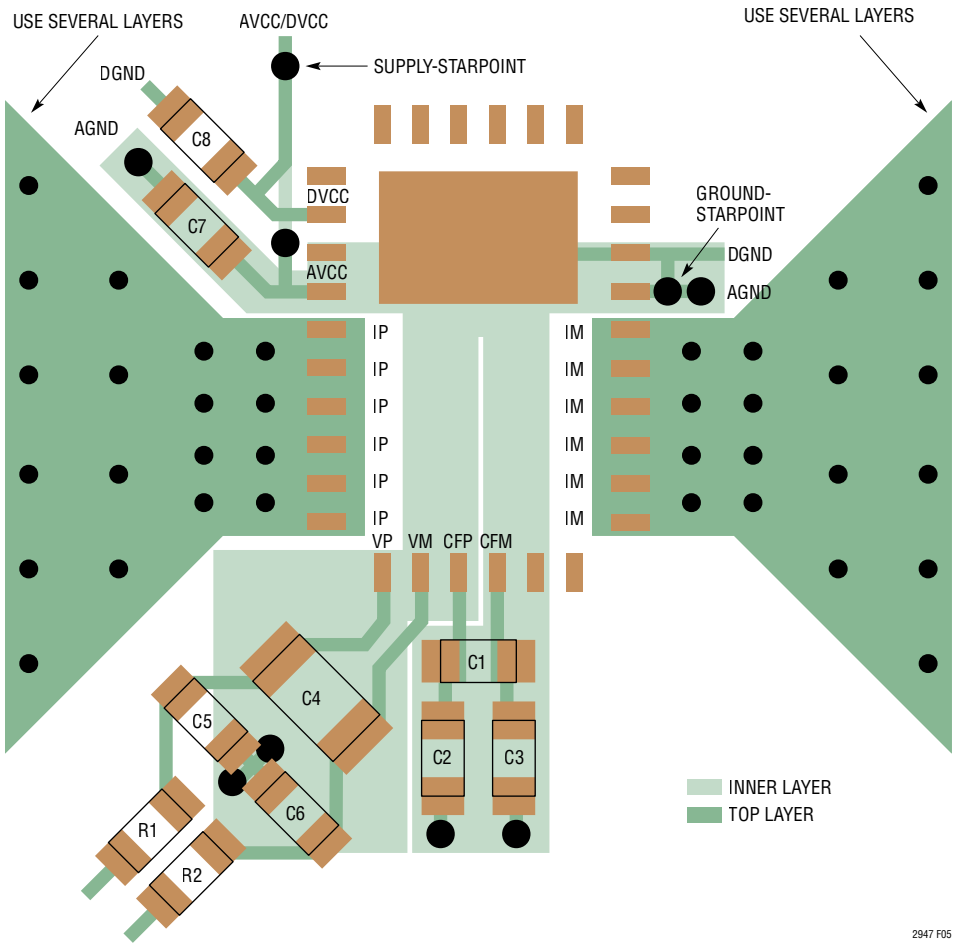


Figure 5. Recommended Layout of Current Tracks, Voltage Input and Ground

APPLICATIONS INFORMATION

the ground tracks of the capacitors at CFP, CFM including the AGND pin to a separate small plane and connecting this plane at one point to the ground of the PCB. Figure 5 sketches this star connection concept; the interference to the ADC inputs is minimized. In the same way, a small separate plane can collect the ground connections of the capacitors attached to DVCC, OVDD, including the DGND pin, and be connected to the same ground-starpoint as the AGND plane to the ground of the PCB.

The supplies of AVCC and DVCC pins should also be star-routed. The decoupling caps should be placed closer to these pins than the supply-starpoint.

The crystal oscillator's clock amplitude is sensitive to parasitics such as stray capacitance on the CLKOUT pin and coupling between the CLKIN and CLKOUT pins. It is recommended that the CLKIN and CLKOUT traces from the LTC2947 to the crystal oscillator network be as short as practical, with the load capacitors placed next to the crystal. To minimize stray capacitances, avoid large ground planes and digital signals near the crystal network.

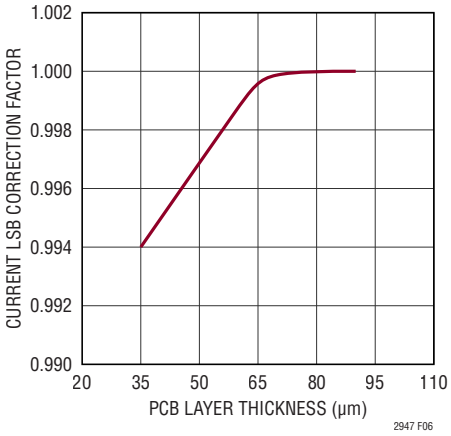


Figure 6. Current LSB Correction Factor vs PCB Thickness

DIGITAL INTERFACE

SELECTING SPI OR I²C SERIAL INTERFACE

The serial interface of the LTC2947 can operate in either SPI or I²C mode. To select SPI mode, tie AD0 to OVDD. To select I²C mode, connect AD0 according to Table 3. The LTC2947 selects SPI or I²C mode by reading pin AD0 when DVCC is powered up. To ensure proper mode detection, OVDD should be powered up before DVCC.

SPI MODE

Physical Layer

In SPI mode, the LTC2947 acts as a SPI slave, with the AD1 pin acting as $\overline{CS}$ (chip select, active low). Logic input thresholds and output swings are set by the voltage at the OVDD pin, which should be connected to the same supply as the SPI master device. A 1µF bypass capacitor is recommended from OVDD to DGND. The SDI pin is often referred to as MOSI, the SDO pin as MISO. The LTC2947 samples data at SDI on the rising edge of SCL and changes data at SDO on the falling edge of SCL (often referred to as CPHA=0, CPOL=0).

Data Layer

All data sent to the LTC2947 is transmitted in 8-bit bytes, MSB first. The LTC2947 returns data in this same format. Multiple bytes can be sent in a single transaction. Figure 8 and Figure 9 show typical write and read transactions.

Write Protocol

The master writes to the LTC2947 by sending 0x00 as the first byte in a transaction followed by the address of the first register to be written. The next transmitted byte will be written to this address. The LTC2947 increments its address pointer after each byte is received, so multiple bytes can be written as part of a single transaction. Incomplete bytes are discarded.

Read Protocol

The master reads from the LTC2947 by sending 0x01 as the first byte in a transaction followed by the address of the first register to be read. The LTC2947 sends data bytes starting from that address, incrementing the address pointer after each byte sent. Any number of bytes can be read; if the address pointer reaches address 0xFF, it will roll over to address 0x00. Any data on the SDI line after the register address is ignored by the LTC2947.

SPI Alert Handling

The LTC2947 can be configured to generate alerts via the $\overline{ALERT}$ pin when a variety of events occur. To enable alerts, set bit ALERTBEN in the Alert Master Control Enable register (0xE8)[0] (this is the default setting). Select which events trigger alerts by clearing bits in the Mask registers (addresses 0x88 to 0x8F).

If an alert is enabled, the corresponding event causes the $\overline{ALERT}$ pin to pull low. To release the $\overline{ALERT}$ pin in SPI mode, the master must read the Status, Threshold and Overflow Alert registers (0x80 to 0x87).

DIGITAL INTERFACE

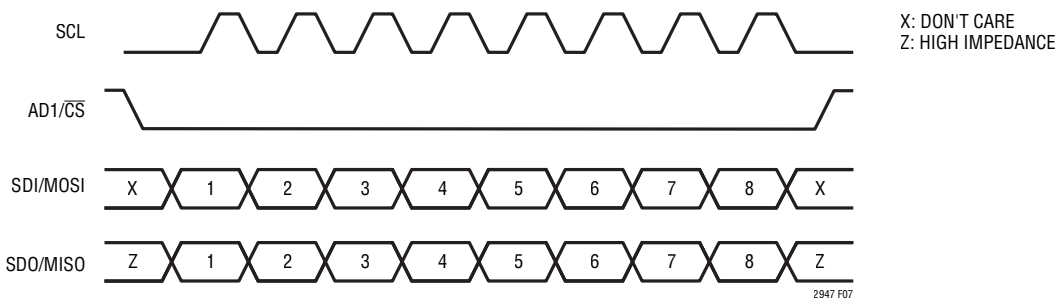


Figure 7. General Data Transfer Over SPI

DIGITAL INTERFACE

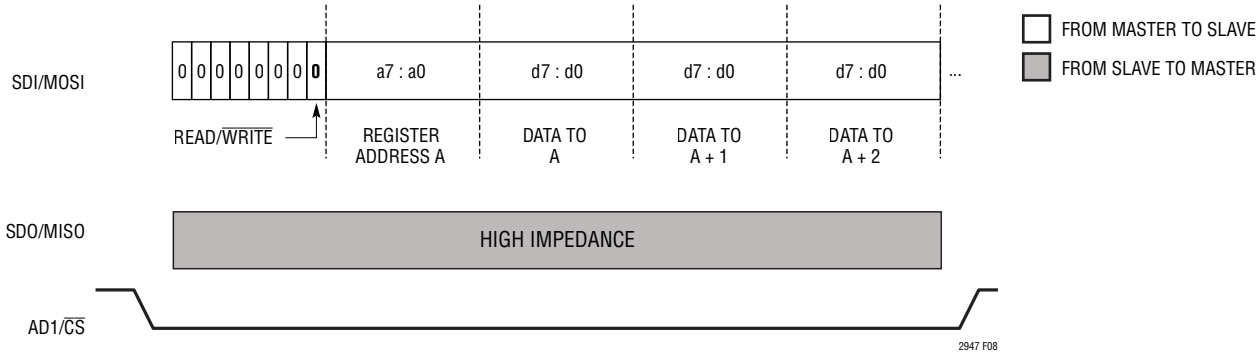


Figure 8. SPI Write Protocol

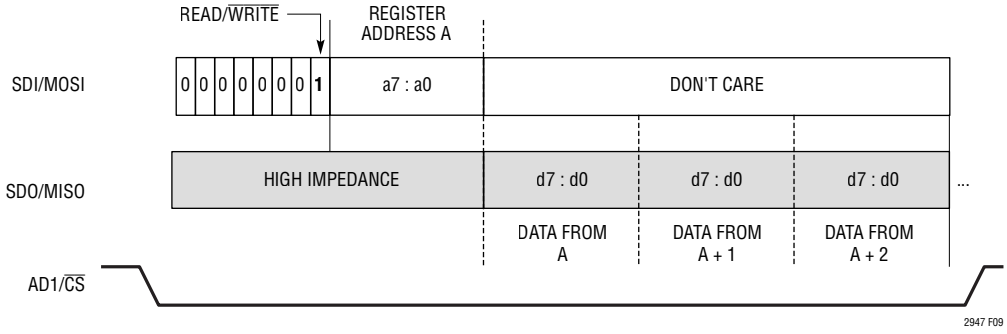


Figure 9. SPI Read Protocol

DIGITAL INTERFACE

I²C MODE

I²C Device Addressing

If AD0 is not tied high at power up, the LTC2947 operates in I²C mode. The I²C address can be configured by connecting AD1 and AD0 as shown in Table 3. The levels are: L: low, tie to DGND, H: high, tie to OVDD, R: resistor, connect to DGND with a 100kΩ resistor. The LTC2947 will check AD0 and AD1 at the beginning of each I²C transaction and respond to the corresponding I²C address.

START and STOP Conditions

When the I²C bus is idle, both SCL and SDA are in the HIGH state. The master signals the beginning of a transmission with a START condition by transitioning SDA from high to low while SCL stays high. When the master has finished communicating with the slave, it issues a STOP condition by transitioning SDA from LOW to high while SCL stays high. The bus is then free for another transmission.

Stuck-Bus Reset

The LTC2947 I²C interface includes a stuck-bus timer to prevent it from holding the bus lines low indefinitely if the SCL signal is interrupted during a transfer. The timer starts when either SCL or SDI is low, and resets when both SCL and SDI are high. If either SCL or SDI stay low for more than 50ms, the stuck-bus timer will reset the internal I²C interface to release the bus. Normal communication will resume at the next START command.

Acknowledge

An acknowledge signal is used for handshaking between the master and the slave. When receiving data, the LTC2947 will pull the SDA line low every ninth clock cycle to acknowledge each data byte. If the slave fails to acknowledge by leaving SDA high, the master should abort the transmission by generating a STOP condition. Similarly, when the master is receiving data from the slave, it must generate acknowledge pulses by pulling down the SDA line every 9th clock. After the last byte has been received by the master, it may leave the SDA line high (not acknowledge) and issue a STOP condition to terminate the transmission.

Write Protocol

The master begins a write operation with a START condition followed by the 7-bit slave address with the R/$\overline{W}$ bit set to zero. If the slave address matches the address programmed at its AD0/AD1 pins, the LTC2947 acknowledges the address byte. The master then sends a register address byte that indicates which internal register the master wishes to write. The LTC2947 acknowledges again and latches the register address into its internal register address pointer. The master then sends the data byte(s) and the LTC2947 acknowledges and writes the data into the selected internal register. The register address pointer will automatically increment by one as each byte is acknowledged. The write operation terminates and the register address pointer resets to 00h when the master sends a STOP condition.

Table 3. I²C Addresses

AD0	AD1	8-BIT ADDRESS BYTE READ	8-BIT ADDRESS BYTE WRITE	7-BIT DEVICE ADDRESS	BINARY DEVICE ADDRESS							
				a6:a0	a6	a5	a4	a3	a2	a1	a0	R/$\overline{W}$
L	L	0xB8	0xB9	0x5C	1	0	1	1	1	0	0	1/0
L	H	0xBA	0xBB	0x5D	1	0	1	1	1	0	1	1/0
L	R	0xBC	0xBD	0x5E	1	0	1	1	1	1	0	1/0
R	L	0xC8	0xC9	0x64	1	1	0	0	1	0	0	1/0
R	H	0xCA	0xCB	0x65	1	1	0	0	1	0	1	1/0
R	R	0xCC	0xCD	0x66	1	1	0	0	1	1	0	1/0

Note 10: L: tie to DGND, H: tie to OVDD, R: resistor, connect to DGND with a 100kΩ resistor.

DIGITAL INTERFACE

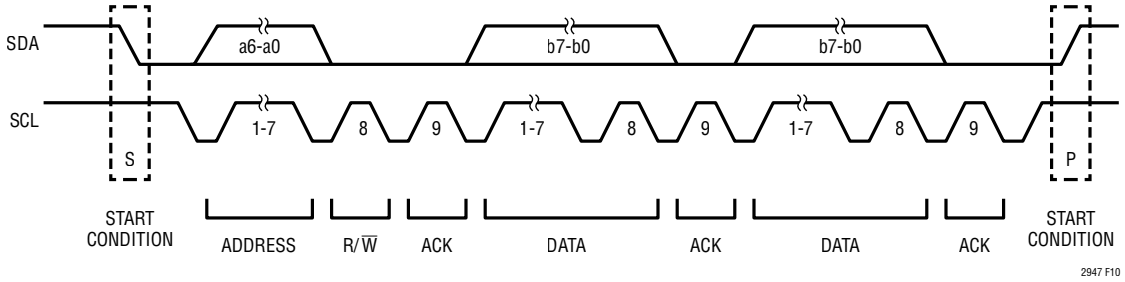


Figure 10. General Data Transfer Over I²C

S	ADDRESS	W	A	REGISTER	A	DATA	A	P
	a6:a0	0	0	b7:b0	0	b7:b0	0	

2947 F11

Figure 11. I²C Write Byte Protocol

S	ADDRESS	W	A	REGISTER	A	DATA	A	DATA	A	…	DATA	A	P
	a6:a0	0	0	b7:b0	0	b7:b0	0	b7:b0	0	...	b7:b0	0	

2947 F12

Figure 12. I²C Write Multiple Bytes Protocol

S	ADDRESS	W	A	REGISTER	A	S	ADDRESS	R	A	DATA	Ā	P
	a6:a0	0	0	b7:b0	0		a6:a0	1	0	b7:b0	1	

2947 F13

Figure 13. I²C Read Byte Protocol

S	ADDRESS	W	A	REGISTER	A	S	ADDRESS	R	A	DATA	A	DATA	A	…	DATA	Ā	P
	a6:a0	0	0	b7:b0	0		a6:a0	1	0	b7:b0	0	b7:b0	0	...	b7:b0	1	

2947 F14

Figure 14. I²C Read Multiple Bytes Protocol

FROM MASTER TO SLAVE

FROM SLAVE TO MASTER

A: ACKNOWLEDGE (LOW)
Ā: NOT-ACKNOWLEDGE (HIGH)

R: READ BIT (HIGH)
W: WRITE BIT (LOW)

S: START CONDITION
P: STOP CONDITION

DIGITAL INTERFACE

Read Protocol

The master begins a read operation with a START condition followed by the 7-bit slave address with the R/$\overline{W}$ bit set to zero. If the slave address matches the address programmed at its AD0/AD1 pins, the LTC2947 acknowledges and the master sends a register address byte that indicates which internal register the master wishes to read. The LTC2947 acknowledges again and latches the register address byte into its internal register address pointer. The master then sends a repeated START condition followed by the same 7-bit address with the R/$\overline{W}$ bit now set to 1. The LTC2947 acknowledges one more time and then sends the contents of the requested register. If the master acknowledges, the LTC2947 will increment the register address pointer and send the contents of the next register, and send out data bytes. The read operation terminates and the register address pointer resets to 00h when the master sends a STOP condition.

SMBus Alert Response Protocol

The LTC2947 uses the SMBus alert response protocol (ARA) to manage alerts in I^{2}C mode. To enable alerts, set the ALERTBEN bit in the Alert Master Control Enable register (0xE8)[0]—this is the default setting. Select which events trigger alerts by clearing bits in the Alert Mask registers (addresses 0x88 to 0x8F).

S	ALERT RESPONSE ADDRESS	R	A	DEVICE ADDRESS	$\overline{W}$	$\overline{A}$	P
	0001100	1	0	a6:a0	0	1	

2947 F15

Figure 15. Serial Bus I^{2}C Alert Response Protocol

If two or more devices on the same bus are generating alerts when the ARA is broadcasted, standard I^{2}C arbitration causes the device with the highest priority (lowest address) to reply first and the device with the lowest priority (highest address) to reply last. The bus master will repeat the alert response protocol until the $\overline{ALERT}$ line is released. Once the device causing the alert is identified, the master may read the Status, Threshold and Overflow Alert registers (0x80 to 0x87) to determine what caused the fault. In SPI mode, reading the Status or Alert registers will release the $\overline{ALERT}$ pin. In I^{2}C mode, the $\overline{ALERT}$ pin is released using the SMBus ARA protocol; reading the Status or Alert registers will not release $\overline{ALERT}$.

REGISTER MAP

The LTC2947 is configured and communicates with the host system through its internal registers, addressed via the serial interface. There are a total of 496 register addresses arranged as two 256-byte pages in the LTC2947 register map, not all of which are used (Figure 16).

In order to facilitate the embedding of the LTC2947 into a system, C/C++ code examples targeting the Linduino, Analog Devices' Arduino compatible development platform, are available at the LTC2947's Linduino Sketch Webpage.

The headers provide register address definitions, register bit mask definitions, LSB values for RAW quantities, PRE/DIV calculation from external oscillator frequencies, and LSB values for accumulated quantities depending on user defined PRE/DIV values.

OFFSET																
	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
BASE	**PAGE 0**															
0x00	C1[47:0]						E1[47:0]						TB1[31:0]			
0x10	C2[47:0]						E2[47:0]						TB2[31:0]			
0x20																
0x30																
0x40	IMAX[15:0]		IMIN[15:0]		PMAX[15:0]		PMIN[15:0]									
0x50	VMAX[15:0]		VMIN[15:0]		TEMPMAX[15:0]		TEMPMIN[15:0]		VDVCCMAX[15:0]		VDVCCMIN[15:0]					
0x60								GPIOSTATCTL								
0x70																
0x80	STATUS	STATVT	STATIP	STATC	STATE	STATCEOF	STATTB	STATVDVCC	STATUSM	STATVTM	STATIPM	STATCM	STATEM	STATCEOFM	STATTBM	STATVDVCCM
0x90	I[23:0]			P[23:0]												
0xA0	V[15:0]		TEMP[15:0]		VDVCC[15:0]											
0xB0	IH1[23:0]			IH2[23:0]			IH3[23:0]			IH4[23:0]			IH5[23:0]			
0xC0																
0xD0																
0xE0		ACCICTL		ACCGPCTL	ACCIDB				ALERTBCTL	TBCTL						
0xF0	OPCTL															PGCTL
	PAGE 1															
0x00	C1TH[47:0]						C1TL[47:0]						TB1TH[31:0]			
0x10	E1H[47:0]						E1TL[47:0]									
0x20	C2TH[47:0]						C2TL[47:0]						TB2TH[31:0]			
0x30	E2TH[47:0]						E2TL[47:0]									
0x40																
0x50																
0x60																
0x70																
0x80	ITH[15:0]		ITL[15:0]		PTH[15:0]		PTL[15:0]									
0x90	VTH[15:0]		VTL[15:0]		TEMPTH[15:0]		TEMPTL[15:0]		VDVCCTH[15:0]		VDVCCTL[15:0]		TEMPFANH[15:0]		TEMPFANL[15:0]	
0xA0																
0xB0																
0xC0																
0xD0																
0xE0																
0xF0	OPCTL															PGCTL
	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
OFFSET																

Figure 16. Register Map

REGISTER DESCRIPTION

REGISTER NAMING CONVENTIONS

RW Read-Write
RO Read Only
COR Clear on Read
DEF Default Value
SI Signed Integer
UI Unsigned Integer

PAGING MECHANISM

The memory map of the LTC2947 is organized into two pages, PAGE0 and PAGE1. PAGE0 contains all quantity, control and status registers while PAGE1 contains all threshold registers. Each page has a register address space ranging from 0x00 to 0xEF, with each register consisting of one 8-bit byte of data. Multiple-byte data is stored with most significant byte at the lowest address (little-endian). For instance, the MSB C1[47:40] of the quantity C1 is stored at address 0x00 in PAGE0.

Some addresses in the register map are not used and are reserved. Bits in non-reserved registers that are not explicitly described are also reserved. Writing to unused reserved registers or reserved bits in non-reserved registers may result in unwanted behavior of the LTC2947; writing 0 to reserved bits in non-reserved registers is allowed. Reading of unused registers is generally harmless but will return random data.

Addresses in the range 0xF0 to 0xFF are used to control page access and are common to both pages. These registers (OPCTL (0xF0) and PGCTL (0XFF)) must be written with single byte transactions. Do not write as part of a multiple-byte write.

PAGE CONTROL

The Page Control register (0xFF) selects the active memory page.

Table 4. Page Control PGCTL (0xFF)

BIT	SYMBOL	TYPE	COR	DEFAULT	OPERATION
0	PAGE	RW	N	0	Memory Map Page Select. 0: PAGE0 of the memory map is selected. 1: PAGE1 of the memory map is selected.

OPERATION CONTROL

The Operation Control register OPCTL (0xF0) sets the operating mode of the LTC2947, clears its accumulation and tracking registers and resets the part. There are two operating modes, single-shot and continuous, and a shutdown mode.

Table 5. Operation Control OPCTL (0xF0)

BIT	SYMBOL	TYPE	COR	DEFAULT	OPERATION
0	SHDN	RW	N	0	0: Normal operation 1: Shutdown. The LTC2947 will exit shutdown in SPI mode if the pin AD1/$\overline{CS}$ is pulled low and in I^2C mode if it receives the correct I^2C address (programmed at the ADx pins).

REGISTER DESCRIPTION

Table 5. Operation Control OPCTL (0xF0) (continued)

BIT	SYMBOL	TYPE	COR	DEFAULT	OPERATION
1	CLR	RW	N	0	1: Clear. The accumulation and tracking (max/min) registers are cleared: C1, E1, TB1, C2, E2, TB2, IMAX, IMIN, PMAX, PMIN, VMAX, VMIN, TEMPMAX, TEMPMIN, VDVCCMAX, VDVCCMIN. (Note 11)
2	SSHOT	RW	N	0	1: Single Shot Measurement. A single set of measurements of current, voltage, power, temperature and V_{DVCC} are performed and the result registers updated. If CONT is set, it is cleared after completion of any conversion cycle in progress and the single shot measurement is executed. SSHOT is cleared after the single measurement cycle is complete.
3	CONT	RW	N	0	0: Continuous measurement is disabled 1: Continuous measurement is enabled. Measurement cycles run continuously. Charge and energy measurements are only active in continuous mode.
7	RST	RW	N	0	Global Reset. When set, the 2947 is reset and all registers are set to their default values.

Note 11: Continuous mode must be disabled to ensure proper behavior of the CLR function. To execute a CLR when continuous mode is active, clear the CONT bit, wait 100ms and then poll the UPDATE bit in the Status register(0x80)[4] to ensure that all measurement cycles have completed. Once bit UPDATE is set to 1 by the LTC2947, the master can set bit CLR and CONT can then be re-enabled.

REGISTER MAP PAGE0

Table 6. PAGE0 Registry Summary

ADDRESS	NAME	TYPE	COR	DEFAULT	PARAMETER	TABLE	PAGE
Accumulated Results							
0x00	C1[47:0]	RW	N	0x00	Charge1	7,8	28
0x06	E1[47:0]	RW	N	0x00	Energy1	7,8	28
0x0C	TB1[31:0]	RW	N	0x00	Time1	7,8	28
0x10	C2[47:0]	RW	N	0x00	Charge2	7,8	28
0x16	E2[47:0]	RW	N	0x00	Energy2	7,8	28
0x1C	TB2TH[31:0]	RW	N	0x00	Time2	7,8	28
Tracking							
0x40	IMAX[15:0]	RW	N	0x8000	Maximum Current	10	30
0x42	IMIN[15:0]	RW	N	0x7FFF	Minimum Current	10	30
0x44	PMAX[15:0]	RW	N	0x8000	Maximum Power	10	30
0x46	PMIN[15:0]	RW	N	0x7FFF	Minimum Power	10	30
0x50	VMAX[15:0]	RW	N	0x8000	Maximum Voltage V_D	10	30
0x52	VMIN[15:0]	RW	N	0x7FFF	Minimum Voltage V_D	10	30
0x54	TEMPMAX[15:0]	RW	N	0x8000	Maximum Temperature	10	30
0x56	TEMPMIN[15:0]	RW	N	0x7FFF	Minimum Temperature	10	30
0x58	VDVCCMAX[15:0]	RW	N	0x8000	Maximum Voltage at DVCC	10	30
0x5A	VDVCCMIN[15:0]	RW	N	0x7FFF	Minimum Voltage at DVCC	10	30
GPIO							
0x67	GPIOSTATCTL	RW	N	0x00	GPIO Status and Control	11	30
Status							
0x80	STATUS	RO	Y	0x0F	Status	17	32

REGISTER DESCRIPTION

Table 6. PAGE0 Registry Summary (continued)

Threshold And Overflow Alerts							
0x81	STATVT	RO	Y	0x00	Voltage, Temperature Threshold Alerts	18	33
0x82	STATIP	RO	Y	0x00	Current, Power Threshold Alerts	19	33
0x83	STATC	RO	Y	0x00	Charge Threshold Alerts	20	33
0x84	STATE	RO	Y	0x00	Energy Threshold Alerts	21	34
0x85	STATCEOF	RO	Y	0x00	Charge, Energy Overflow Alerts	22	34
0x86	STATTB	RO	Y	0x00	Timebase Alerts	23	34
0x87	STATVDVCC	RO	Y	0x00	V_{DVCC} Threshold Alerts	24	34
Mask							
0x88	STATUSM	RW	N	0x79	Status Mask	25	34
0x89	STATVTM	RW	N	0x3F	Voltage, Temperature Threshold Alert Mask	26	35
0x8A	STATIPM	RW	N	0xF	Current, Power Threshold Alert Mask	27	35
0x8B	STATCM	RW	N	0x3F	Charge Threshold Alerts Mask	28	36
0x8C	STATEM	RW	N	0x3F	Energy Threshold Alerts Mask	29	36
0x8D	STATCEOF	RW	N	0x33	Charge, Energy Overflow Alerts Mask	30	36
0x8E	STATTBM	RW	N	0x33	Timebase Alerts Mask	31	37
0x8F	STATVDVCCM	RW	N	0x03	VDVCC Threshold Alerts Mask	31	37
Non Accumulated Results							
0x90	I[23:0]	RO	N	0x00	Current	9	29
0x93	P[23:0]	RO	N	0x00	Power	9	29
0xA0	V[15:0]	RO	N	0x00	Voltage	9	29
0xA2	TEMP[15:0]	RO	N	0x00	Temperature	9	29
0xA4	VDVCC[15:0]	RO	N	0x00	Voltage at DVCC	9	29
0xB0	IH1[23:0]	RO	N	0x00	Current History 1	9	29
0xB3	IH2[23:0]	RO	N	0x00	Current History 2	9	29
0xB6	IH3[23:0]	RO	N	0x00	Current History 3	9	29
0xB9	IH4[23:0]	RO	N	0x00	Current History 4	9	29
0xBC	IH5[23:0]	RO	N	0x00	Current History 5	9	29
Control							
0xE1	ACCICTL	RW	N	0x00	Accumulator Control Current Polarity	12	31
0xE3	ACCGPCTL	RW	N	0x00	Accumulator Control GPIO	13	31
0xE4	ACCIDB	RW	N	0x00	Accumulation Deadband	14	31
0xE8	ALERTBCTL	RW	N	0x01	Alert Master Control Enable	15	31
0xE9	TBCTL	RW	N	0x07	Timebase Control	16	32
0xF0	OPCTL	RW	N	0x00	Operation Control	5	25
0xFF	PGCTL	RW	N	0x00	Page Control	4	25

REGISTER DESCRIPTION

Accumulated Result Registers

The registers in Tables 7 and 8 contain two sets of the accumulated quantities charge, energy and time. The time registers are unsigned integer values while the charge and energy registers are two's complement signed integer values. The value of each accumulated quantity can be determined by multiplying the respective register value with the corresponding LSB value from Tables 7 or 8. If the internal clock or a 4MHz crystal is used as a reference clock, use the LSB values in Table 7. If an external reference clock is used, calculate the LSB values according to Table 8. The values of PRE(0xE9)[2:0] and DIV(0xE9)[7:3] should be set according to the Timebase Control section.

Table 7. Accumulated Results Register Parameters for Use with Crystal or Internal Clock

ADDRESS	NAME	TYPE	COR	DEFAULT	PARAMETER	LSB (CRYSTAL = 4MHz OR INTERNAL CLOCK)	PRE (CRYSTAL = 4MHz)	DIV (CRYSTAL = 4MHz)	UNIT	SI/UI
0x00	C1[47:0]	RW	N	0x00	Charge1=C1•LSB_{C1}	LSB_{C1} = 1.193E-06	2	30	A•s	SI
0x06	E1[47:0]	RW	N	0x00	Energy1=E1•LSB_{E1}	LSB_{E1} = 19.89E-06	2	30	W•s	SI
0x0C	TB1[31:0]	RW	N	0x00	Time1=TB1•LSB_{TB1}	LSB_{TB1} = 397.8E-06	2	30	s	UI
0x10	C2[47:0]	RW	N	0x00	Charge2=C2•LSB_{C2}	LSB_{C2} = 1.193E-06	2	30	A•s	SI
0x16	E2[47:0]	RW	N	0x00	Energy2=E2•LSB_{E2}	LSB_{E2} = 19.89E-0	2	30	W•s	SI
0x1C	TB2[31:0]	RW	N	0x00	Time2=TB2•LSB_{TB2}	LSB_{TB2} = 397.8E-06	2	30	s	UI

When the internal clock is used, PRE and DIV should be set to their default values which is done by writing 0x07 to register (0xE9) (see Table 16).

Table 8. Accumulated Results Register Parameters for Use with External Clock

ADDRESS	NAME	TYPE	COR	DEFAULT	PARAMETER	LSB	PRE, DIV	UNIT	SI/UI
0x00	C1[47:0]	RW	N	0x00	Charge1=C1•LSB_{C1}	$LSB_{C1} = 0.0385 \cdot 1/f_{EXT} \cdot 2^{PRE} \cdot (DIV+1)$	Note 12	A•s	SI
0x06	E1[47:0]	RW	N	0x00	Energy1=E1•LSB_{E1}	$LSB_{E1} = 0.6416 \cdot 1/f_{EXT} \cdot 2^{PRE} \cdot (DIV+1)$	Note 12	W• s	SI
0x0C	TB1[31:0]	RW	N	0x00	Time1=TB1•LSB_{TB1}	$LSB_{TB1} = 12.83 \cdot 1/f_{EXT} \cdot 2^{PRE} \cdot (DIV+1)$	Note 12	s	UI
0x10	C2[47:0]	RW	N	0x00	Charge2=C2•LSB_{C2}	$LSB_{C2} = 0.0385 \cdot 1/f_{EXT} \cdot 2^{PRE} \cdot (DIV+1)$	Note 12	A•s	SI
0x16	E2[47:0]	RW	N	0x00	Energy2=E2•LSB_{E2}	$LSB_{E2} = 0.6416 \cdot 1/f_{EXT} \cdot 2^{PRE} \cdot (DIV+1)$	Note 12	W•s	SI
0x1C	TB2[31:0]	RW	N	0x00	Time2=TB2•LSB_{TB2}	$LSB_{TB2} = 12.83 \cdot 1/f_{EXT} \cdot 2^{PRE} \cdot (DIV+1)$	Note 12	s	UI

Note 12: Values of PRE and DIV should be calculated according to Timebase Control section.

For instance, an external clock frequency of 10MHz would require values PRE to be set to 4 and DIV to be set to 19. With f_{EXT}=10MHz, LSB_{C1} is calculated as 1.23418E-06A•s. To get the Charge1 value, the register content of C1 is multiplied with LSB_{C1}. In this case, a C1 register value of 0x7B A2 92 results in a Charge1 value of 10.0A•s. For a C1 register value of 0xFF FF FF 84 5D 6E, the resulting Charge1 is –10.0A•s.

LSB values may be calculated easily using the QuikEval software for the LTC2947.

The registers for charge, energy and time can be preset to a non-zero initial value. All bytes of the respective quantity should be written in the same multi-byte transaction. For instance, to set a start value of 10.0W•s (assuming an external reference clock of 10MHz) for Energy1, all 6 bytes 0x00 00 00 07 6B 08 should be written to registers E1(0x06-0x0B) as one transaction.

REGISTER DESCRIPTION

Non-Accumulated Result Registers

Registers in Table 9 contain measured values of current, power, voltage, temperature, and V_{DVCC}. All quantities are represented as two's complement signed integer values.

Current is the current I flowing through pins IP and IM. Voltage is the differential voltage V_D across pins VP and VM. Power is the instantaneous multiplication of voltage V_D and current I. Temperature is the temperature of the on-silicon temperature sensor. V_{DVCC} is the voltage across pins DVCC and DGND. The Current History registers store the 5 current readings prior to the most recent reading; Current History 1 is the most recent previous current result, Current History 2 is the current result prior to Current History 1, and so on.

All measured values are scaled with the LSB values from Table 9. To calculate the physical value of the measured parameter except for temperature, multiply the register value by the appropriate LSB value. To calculate temperature, multiply the TEMP register value by 0.204°C and add 5.5°C.

Table 9. Non-Accumulated Results Registers

ADDRESS	NAME	TYPE	COR	DEFAULT	PARAMETER	LSB	UNIT	SI/UI
0x90	I[23:0]	RO	N	0x00	Current	3	mA	SI
0x93	P[23:0]	RO	N	0x00	Power	50	mW	SI
0xA0	V[15:0]	RO	N	0x00	Voltage	2	mV	SI
0xA2	TEMP[15:0]	RO	N	0x00	Temperature = TEMP • 0.204 + 5.5	–	°C	SI
0xA4	VDVCC[15:0]	RO	N	0x00	Voltage at DVCC	145	mV	SI
0xB0	IH1[23:0]	RO	N	0x00	Current History 1 (prev. result) = I • LSB_I	3	mA	SI
0xB3	IH2[23:0]	RO	N	0x00	Current History 2 (prev. result – 1) = I • LSB_I	3	mA	SI
0xB6	IH3[23:0]	RO	N	0x00	Current History 3 (prev. result – 2) = I • LSB_I	3	mA	SI
0xB9	IH4[23:0]	RO	N	0x00	Current History 4 (prev. result – 3) = I • LSB_I	3	mA	SI
0xBC	IH5[23:0]	RO	N	0x00	Current History 5 (prev. result – 4) = I • LSB_I	3	mA	SI

For example: Table 9 gives LSB_I = 3mA. For an I register value I(0x90-0x92) of 0x00 0B B8, the resulting current is 9.0A. For a register value of 0xFF F4 48, the resulting current is –9.0A.

For a TEMP register value TEMP(0xA2-0xA3) of 0x00 78, the resulting temperature is 30°C. For a register value of 0xFF 52, the resulting temperature is –30°C.

Additional power resolution can be obtained by reading the results of registers V(0xA0-0xA1) and I(0x90-0x92) in one multi-byte transaction and multiplying them externally in the host. In this case the LSB of the resulting power value is 6µW instead of 50mW. The bandwidth in this mode is significantly reduced.

Tracking Registers

The Tracking registers keep track of the maximum and minimum values of all conversions since the last reset. Value scaling is done in the same manner as the Non Accumulated Results register values, using LSB values from Table 10. Negative values are treated as smaller (more minimum) than positive values as the minimum registers are updated.

For example: A register value PMAX(0x44-0x45) of 0x01 F4 indicates a measured maximum power of 500 • 0.2W = 100W. A register value PMIN(0x46-0x47) 0xFA 24 indicates a measured minimum power of –1500 • 0.2W = –300W. The calculation of the other tracked parameter values is done the same way with the corresponding LSB values.

REGISTER DESCRIPTION

Table 10. Tracking Registers

ADDRESS	NAME	TYPE	COR	DEFAULT	PARAMETER	LSB	UNIT	SI/UI
0x40	IMAX[15:0]	RW	N	0x8000	Maximum Current	12	mA	SI
0x42	IMIN[15:0]	RW	N	0x7FFF	Minimum Current	12	mA	SI
0x44	PMAX[15:0]	RW	N	0x8000	Maximum Power	0.2	W	SI
0x46	PMIN[15:0]	RW	N	0x7FFF	Minimum Power	0.2	W	SI
0x50	VMAX[15:0]	RW	N	0x8000	Maximum Voltage V_D	2	mV	SI
0x52	VMIN[15:0]	RW	N	0x7FFF	Minimum Voltage V_D	2	mV	SI
0x54	TEMPMAX[15:0]	RW	N	0x8000	Maximum Temperature = TEMPMAX • 0.204 + 5.5	–	°C	SI
0x56	TEMPMIN[15:0]	RW	N	0x7FFF	Minimum Temperature = TEMPMIN • 0.204 + 5.5	–	°C	SI
0x58	VDVCCMAX[15:0]	RW	N	0x8000	Maximum Voltage at DVCC	145	mV	SI
0x5A	VDVCCMIN[15:0]	RW	N	0x7FFF	Minimum Voltage at DVCC	145	mV	SI

Note that the Tracking registers for current and power report only the 16MSBs of the respective 18-bit result registers.

Control Registers

The Control registers control the accumulation of charge, energy and time, configure the GPIO pin, and setup the timebase if an external clock is used.

For details see the GPIO control section.

Table 11. GPIO Status and Control GPIOSTATCTL(0x67)

BIT	SYMBOL	TYPE	COR	DEFAULT	OPERATION
0	GPOEN	RW	N	0	Pin GPIO configured as input or output 0: Input 1: Output
4	GPI	RW (Note 13)	N	0	This register shows the applied level at pin GPIO 0: Logical level 0 at pin GPIO 1: Logical level 1 at pin GPIO
5	GPO	RW	N	0	This register sets the level at GPIO if set as output provided there is a pull-up resistor at GPIO 0: Pin GPIO is set to 0 if set as output 1: Pin GPIO is set to 1 if set as output
6	FANEN	RW	N	0	GPIO fan control enable 0: GPIO level controlled by GPO 1: GPIO level controlled by temperature measurement against fan temperature threshold high/low registers TEMPFANH (page1.0x9C) and TEMPFANL (page1.0x9E)
7	FANPOL	RW	N	0	GPIO polarity if GPIO fan control enable FANEN (bit 6) is enabled 0: GPIO is low active 1: GPIO is high active GPIO gets active when temperature measurement is higher than TEMPFANH (page1.0x9C). GPIO gets inactive when temperature measurement is lower than TEMPFANL (page1.0x9E). If temperature measurement is between TEMPFANH and TEMPFANL, GPIO does not change its level.

Note 13: If GPIO status and control is written and pin GPIO is configured as input, the register reporting bit GPI (0x67)[4] is set/cleared by this byte write. If the electrical input at pin GPIO is different than the value of the write, the GPI bit is updated after the next operation cycle(100ms(typ)).

REGISTER DESCRIPTION

The Accumulator Control Current Polarity register sets the polarity of current that is accumulated to calculate charge and energy. For example, one set of registers (e.g. Charge1, Energy1) can be configured to accumulate the total charge and energy, and the second set (e.g. Charge2 and Energy2) to only accumulate the negative charge and energy. This allows a system to keep track of total charge as well as charge into a battery, for example.

Table 12. Accumulator Control Current Polarity ACCICTL(0xE1)

BIT	SYMBOL	TYPE	COR	DEFAULT	OPERATION
[1:0]	ACC1I[1:0]	RW	N	00	Accumulation control of Charge1/Charge2 and Energy1/Energy2 by current polarity 00: Accumulation takes place always 01: Only if the current is positive 10: Only if the current is negative 11: No accumulation takes place
[3:2]	ACC2I[1:0]	RW	N	00	

The Accumulator Control GPIO register allows the GPIO pin to enable or disable the accumulated results registers.

Table 13. Accumulator Control GPIO ACCGPCTL(0xE3)

BIT	SYMBOL	TYPE	COR	DEFAULT	OPERATION
[1:0]	ACC1GP[1:0]	RW	N	00	Accumulation control of Charge1/Charge2, Energy1/Energy2 and TIME1/TIME2 by pin GPIO 00: Accumulation takes place always 01: Only if pin GPIO is 1 10: Only if pin GPIO is 0 11: Reserved
[3:2]	ACC2GP[1:0]	RW	N	00	

The Accumulation Dead Band register allows to set the level of current below which no accumulation takes place.

Table 14. Accumulation Deadband ACCIDB(0xE4)

BIT	SYMBOL	TYPE	COR	DEFAULT	OPERATION
[7:0]	ACCIDB	RW	N	0	Deadband current for accumulation If the absolute current value is higher than or equal this value, accumulation of Charge1/Charge2 and Energy1/Energy2 and comparison to their respective threshold takes place. If lower, Charge1/Charge2 and Energy1/Energy2 values are not accumulated and there is no comparison against thresholds. Unit is the same as LSB of current I(0x90): 3mA

The Alert Master Control Enable register allows the general enabling/disabling of the pin alert.

Table 15. Alert Master Control Enable ALERTBCTL(0xE8)

BIT	SYMBOL	TYPE	COR	DEFAULT	OPERATION
0	ALERTBEN	RW	N	1	0: Unmasked alerts (see MASK registers) are not forwarded to $\overline{\text{ALERT}}$ pin 1: Unmasked alerts (see MASK registers) are forwarded to $\overline{\text{ALERT}}$ pin.

The Time Base Control register selects between the internal and an external reference clock, and sets the time base parameters when an external reference clock is used. Set PRE[2:0] = 111b or 0x07 (default) to enable the internal reference clock. To use an external reference clock, set the values of PRE[2:0] and DIV[4:0] according to the external clock frequency; see the TimeBase: Internal/External Clock/Crystal section.

REGISTER DESCRIPTION

Table 16. Timebase Control TBCTL (0xE9), DEFAULT VALUE: 0x07

BIT	SYMBOL	TYPE	COR	DEFAULT	OPERATION (Note 14)
0	PRE[0]	RW	N	1	Prescaler value bit 0, binary coded
1	PRE[1]	RW	N	1	Prescaler value bit 1, binary coded
2	PRE[2]	RW	N	1	Prescaler value bit 2, binary coded
3	DIV[0]	RW	N	0	Divider value bit 0, binary coded
4	DIV[1]	RW	N	0	Divider value bit 1, binary coded
5	DIV[2]	RW	N	0	Divider value bit 2, binary coded
6	DIV[3]	RW	N	0	Divider value bit 3, binary coded
7	DIV[4]	RW	N	0	Divider value bit 4, binary coded

Note 14: For switching between internal and external clock the LTC2947 must be in Idle Mode.

Status Register

The Status register reports the status of register updates, undervoltage lockout, and reference clock errors. On power up, all undervoltage lockouts and the power-on reset bits [3:0] are set to 1. After exit from shutdown, bits UVLOA[0] and UVLOD[3] are set, all other bits are cleared and $\overline{\text{ALERT}}$ is released if the reason of being asserted before shutdown were only bits UVLOAO[0] and UVLOD[3]. This allows the system to distinguish between these two cases. In both cases, the bits can be cleared by reading the Status register. After they are cleared, the undervoltage registers and PORA are set again if an undervoltage event occurs at the AVCC/DVCC supply pins. Events can also trigger the $\overline{\text{ALERT}}$ pin if enabled in the Alert Master Control Enable register(0xE8) and the Status Mask register(0x88).

Bit[4] UPDATE is set to 1 when the LTC2947 has finished a measurement cycle and updated the Result registers, the Accumulation registers, and the Tracking registers. Measurement completion can be observed by polling bit[4] UPDATE or by using the alert mechanism via the $\overline{\text{ALERT}}$ pin. In case Threshold and Overflow Alert registers (0x81 to 0x87) are configured and used, the Status (0x80) and all Alert registers (0x81 to 0x87) must be read in one multi-byte transaction. This includes the above described polling of the UPDATE bit.

Bit[5] ADCERR is set to 1 if the supply voltage at AVCC is too low for proper operation of the ADCs. The values in the result registers are not valid and should be discarded if ADCERR is set.

Bit[6] TBERR is set to 1 if the internal time base overflows. This indicates an incorrect setting of the values PRE and DIV with respect to the external clock at CLKI. The values of Accumulated Results registers should be discarded if TBERR is set.

Table 17. Status STATUS (0x80)

BIT	SYMBOL	TYPE	COR	DEFAULT	OPERATION
0	UVLOA	RO	Y	1	1: Undervoltage in the analog domain including ADCs during a conversion
1	PORA	RO	Y	1	1: Power-on reset has occurred due to undervoltage in the analog domain
2	UVLOSTBY	RO	Y	1	1: Undervoltage in the standby domain
3	UVLOD	RO	Y	1	1: Undervoltage in the digital domain
4	UPDATE	RO	Y	0	1: Result registers have been updated
5	ADCERR	RO	Y	0	1: The ADC conversion is not valid due to undervoltage during a conversion
6	TBERR	RO	Y	0	1: Overflow of the internal timebase register. The values of accumulated result registers are invalid

REGISTER DESCRIPTION

Threshold and Overflow Alert Registers

Threshold and Overflow Alert registers are set when the respective threshold values are exceeded or when registers overflow. Thresholds are set in the Threshold Registers section.

The accumulated quantities are continuously checked against guard values to warn that a register is nearing overflow, nominally set to 90% of each register's maximum value. When any quantity crosses its guard threshold, the LTC2947 sets the corresponding overflow bit in the Status register, generates an alert (if enabled) and then continues accumulation. At the maximum current and voltage inputs, rollover typically happens several hours after an overflow alert is signaled, allowing the host time to take action to avoid data loss. The overflow threshold for 32-bit quantities (time) is 0xE6 66 66 65 LSB, the one for 48-bit quantities (charge, energy) is ±73 33 33 33 33 32 LSB.

The threshold and overflow comparators for accumulated quantities charge, energy and time use a floating point format internally. This can appear to cause slight bit-level comparison discrepancies, but the comparisons between Accumulated Result registers and their respective Threshold registers will always have an accuracy of better than 0.001%.

An alert condition needs to be present for at least 200ms to be reported by the Alert registers (0x81 to 0x87).

When Threshold and Overflow Alert registers (0x81 to 0x87) are configured and used, the Status (0x80) and all Alert registers (0x81 to 0x87) must be read in one multi-byte transaction.

Table 18. Voltage, Temperature Threshold Alerts STATVT (0x81)

BIT	SYMBOL	TYPE	COR	DEFAULT	OPERATION
0	VH	RO	Y	0	1: Voltage V_D high threshold exceeded
1	VL	RO	Y	0	1: Voltage V_D low threshold exceeded
2	TEMPH	RO	Y	0	1: Temperature high threshold exceeded
3	TEMPL	RO	Y	0	1: Temperature low threshold exceeded
4	FANH	RO	Y	0	1: Fan high temperature threshold exceeded
5	FANL	RO	Y	0	1: Fan low temperature threshold exceeded

Table 19. Current, Power Threshold Alerts STATIP (0x82)

BIT	SYMBOL	TYPE	COR	DEFAULT	OPERATION
0	IH	RO	Y	0	1: Current high threshold exceeded
1	IL	RO	Y	0	1: Current low threshold exceeded
2	PH	RO	Y	0	1: Power high threshold exceeded
3	PL	RO	Y	0	1: Power low threshold exceeded

Table 20. Charge Threshold Alerts STATC (0x83)

BIT	SYMBOL	TYPE	COR	DEFAULT	OPERATION
0	C1H	RO	Y	0	1: Charge1 high threshold exceeded
1	C1L	RO	Y	0	1: Charge1 low threshold exceeded
2	C2H	RO	Y	0	1: Charge2 high threshold exceeded
3	C2L	RO	Y	0	1: Charge2 low threshold exceeded

REGISTER DESCRIPTION

Table 21. Energy Threshold Alerts STATE (0x84)

BIT	SYMBOL	TYPE	COR	DEFAULT	OPERATION
0	E1H	RO	Y	0	1: Energy1 high threshold exceeded
1	E1L	RO	Y	0	1: Energy1 low threshold exceeded
2	E2H	RO	Y	0	1: Energy2 high threshold exceeded
3	E2L	RO	Y	0	1: Energy2 low threshold exceeded

Table 22. Charge, Energy Overflow Alerts STATCEOF (0x85)

BIT	SYMBOL	TYPE	COR	DEFAULT	OPERATION
0	C1OF	RO	Y	0	1: Charge1 overflow alert
1	C2OF	RO	Y	0	1: Charge2 overflow alert
4	E1OF	RO	Y	0	1: Energy1 overflow alert
5	E2OF	RO	Y	0	1: Energy2 overflow alert

Table 23. Time Base Alerts STATTB (0x86)

BIT	SYMBOL	TYPE	COR	DEFAULT	OPERATION
0	TB1TH	RO	Y	0	1: Time1 threshold exceeded
1	TB2TH	RO	Y	0	1: Time2 threshold exceeded
4	TB1OF	RO	Y	0	1: Time1 overflow
5	TB2OF	RO	Y	0	1: Time2 overflow

Table 24. VDVCC Threshold Alerts STATVDVCC (0x87)

BIT	SYMBOL	TYPE	COR	DEFAULT	OPERATION
0	VDVCCH	RO	Y	0	1: Voltage at DVCC high threshold exceeded
1	VDVCCL	RO	Y	0	1: Voltage at DVCC low threshold exceeded

Mask Registers

The Mask registers allow control of which alerts trigger the $\overline{\text{ALERT}}$ pin. If a Mask register bit is reset to 0, exceeding of the respective threshold causes the $\overline{\text{ALERT}}$ pin to pull low if ALERTBEN in the Alert Master Control Enable ALERTBCTL(0xE8) register is set to 1.

When a bit of the Status Mask register STATUSM is set to 0, the corresponding bits of register STATUS (0x80) will generate an alert.

For example, when the UPDATEM bit in Status Mask register(0x88) is reset to 0 and the ALERTBEN bit in the ALERTBCTL(0xE8) register is set, every update of the result registers will cause the $\overline{\text{ALERT}}$ pin to pull low.

Table 25. Status Mask STATUSM(0x88), DEFAULT VALUE 0x79

BIT	SYMBOL	TYPE	COR	DEFAULT	OPERATION
0	UVLOAM	RW	N	1	Mask UVLOA of STATUS(0x80) 0: Mask disabled 1: Mask enabled
3	UVLODM	RW	N	1	Mask UVLOD of STATUS(0x80) 0: Mask disabled 1: Mask enabled

REGISTER DESCRIPTION

Table 25. Status Mask STATUSM(0x88), DEFAULT VALUE 0x79 (continued)

4	UPDATEM	RW	N	1	Mask UPDATE of STATUS(0x80) 0: Mask disabled 1: Mask enabled
5	ADCERRM	RW	N	1	Mask ADCERR of STATUS(0x80) 0: Mask disabled 1: Mask enabled
6	TBCERRM	RW	N	1	Mask TBCERR of STATUS(0x80) 0: Mask disabled 1: Mask enabled

When bits of STATVTM are set to 0, corresponding bits of register STATVT (0x81) generate an alert.

Table 26. Voltage, Temperature Threshold Alert Mask STATVTM(0x89), DEFAULT VALUE 0x3F

BIT	SYMBOL	TYPE	COR	DEFAULT	OPERATION
0	VHM	RW	N	1	Mask VH of STATVT(0x81) 0: Mask disabled 1: Mask enabled
1	VLM	RW	N	1	Mask VL of STATVT(0x81) 0: Mask disabled 1: Mask enabled
2	TEMPHM	RW	N	1	Mask TEMPH of STATVT(0x81) 0: Mask disabled 1: Mask enabled
3	TEMPLM	RW	N	1	Mask TEMPL of STATVT(0x81) 0: Mask disabled 1: Mask enabled
4	FANHM	RW	N	1	Mask FANH of STATVT(0x81) 0: Mask disabled 1: Mask enabled
5	FANLM	RW	N	1	Mask FANL of STATVT(0x81) 0: Mask disabled 1: Mask enabled

When bits from STATIPM are set to 0, bits from register STATIP(0x82) generate an alert.

Table 27. Current, Power Threshold Alert Mask STATIPM(0x8A), DEFAULT VALUE 0xF

BIT	SYMBOL	TYPE	COR	DEFAULT	OPERATION
0	IHM	RW	N	1	Mask IH of STATIP(0x82) 0: Mask disabled 1: Mask enabled
1	ILM	RW	N	1	Mask IL of STATIP(0x82) 0: Mask disabled 1: Mask enabled
2	PHM	RW	N	1	Mask PH of STATIP(0x82) 0: Mask disabled 1: Mask enabled
3	PLM	RW	N	1	Mask PL of STATIP(0x82) 0: Mask disabled 1: Mask enabled

REGISTER DESCRIPTION

When bits from STATCM are set to 0, bits from register STATC(0x83) generate an alert.

Table 28. Charge Threshold Alerts Mask STATCM(0x8B), DEFAULT VALUE 0x3F

BIT	SYMBOL	TYPE	COR	DEFAULT	OPERATION
0	C1HM	RW	N	1	Mask C1H of STATC(0x83) 0: Mask disabled 1: Mask enabled
1	C1LM	RW	N	1	Mask C1L of STATC(0x83) 0: Mask disabled 1: Mask enabled
2	C2HM	RW	N	1	Mask C2H of STATC(0x83) 0: Mask disabled 1: Mask enabled
3	C2LM	RW	N	1	Mask C2L of STATC(0x83) 0: Mask disabled 1: Mask enabled

When bits from STATEM are set to 0, bits from register STATE(0x84) generate an alert.

Table 29. Energy Threshold Alerts Mask STATEM(0x8C), DEFAULT VALUE 0x3F

BIT	SYMBOL	TYPE	COR	DEFAULT	OPERATION
0	E1HM	RW	N	1	Mask E1H of STATE(0x84) 0: Mask disabled 1: Mask enabled
1	E1LM	RW	N	1	Mask E1L of STATE(0x84) 0: Mask disabled 1: Mask enabled
2	E2HM	RW	N	1	Mask E2H of STATE(0x84) 0: Mask disabled 1: Mask enabled
3	E2LM	RW	N	1	Mask E2L of STATE(0x84) 0: Mask disabled 1: Mask enabled

When bits from STATCEOFM are set to 0, bits from register STATCEOF(0x85) generate an alert.

Table 30. Charge, Energy Overflow Alerts Mask STATCEOFM(0x8D), DEFAULT VALUE 0x33

BIT	SYMBOL	TYPE	COR	DEFAULT	OPERATION
0	C1OFM	RW	N	1	Mask C1OF of STATCEOF(0x85) 0: Mask disabled 1: Mask enabled
1	C2OFM	RW	N	1	Mask C2OF of STATCEOF(0x85) 0: Mask disabled 1: Mask enabled
2	E1OFM	RW	N	1	Mask E1OF of STATCEOF(0x85) 0: Mask disabled 1: Mask enabled
3	E2OFM	RW	N	1	Mask E2OF of STATCEOF(0x85) 0: Mask disabled 1: Mask enabled

REGISTER DESCRIPTION

When bits from STATTBM are set to 0, bits from register STATTB(0x86) generate an alert.

Table 31. Timebase Alerts Mask STATTBM(0x8E), DEFAULT VALUE 0x33

BIT	SYMBOL	TYPE	COR	DEFAULT	OPERATION
0	TB1THM	RW	N	1	Mask TB1TH of STATTB(0x86) 0: Mask disabled 1: Mask enabled
1	TB2THM	RW	N	1	Mask TB2TH of STATTB(0x86) 0: Mask disabled 1: Mask enabled
4	TB1OFM	RW	N	1	Mask TB1OF of STATTB(0x86) 0: Mask disabled 1: Mask enabled
5	TB2OFM	RW	N	1	Mask TB2OF of STATTB(0x86) 0: Mask disabled 1: Mask enabled

When bits from STATDVCCM are set to 0, bits from register STATDVCC(0x87) generate an alert.

Table 32. VDVCC Threshold Alerts Mask STATVDVCCM(0x8F), DEFAULT VALUE 0x3

BIT	SYMBOL	TYPE	COR	DEFAULT	OPERATION
0	VDVCCHM	RW	N	1	Mask TB1TH of STATVDVCC(0x87) 0: Mask disabled 1: Mask enabled
1	VDVCCLM	RW	N	1	Mask TB1TH of STATVDVCC(0x87) 0: Mask disabled 1: Mask enabled

REGISTER MAP PAGE1

Threshold Registers

The Threshold registers set threshold values for each measured quantity. When a measured value exceeds its threshold, an alert is triggered and the corresponding bits in the Threshold and Overflow Alert registers(0x81 to 0x87) are set. When enabled in the Alert Master Control Enable register ALERTBCTL(0xE8) and the Mask registers(0x88 to 0x8F), the $\overline{\text{ALERT}}$ pin is also pulled low.

Value scaling is done in the same manner as in the corresponding Result register values, using LSB values from Table 33.

Table 33. Threshold Registers

ADDRESS	NAME	TYPE	COR	DEFAULT	PARAMETER	LSB	UNIT
Page1.0x00	C1TH[47:0]	RW	N	0x7F FF FF FF FF FF	Charge1 threshold high	see C1 (0x00)	A•s
Page1.0x06	C1TL[47:0]	RW	N	0x80 00 00 00 00 00	Charge1 threshold low	see C1 (0x00)	A•s
Page1.0x0C	TB1TH[31:0]	RW	N	0xFF FF FF FF	Time1 threshold high	see TB1 (0x0C)	s
Page1.0x10	E1TH[47:0]	RW	N	0x7F FF FF FF FF FF	Energy1 threshold high	see E1 (0x06)	W•s
Page1.0x16	E1TL[47:0]	RW	N	0x80 00 00 00 00	Energy1 threshold low	see E1 (0x06)	W•s
Page1.0x20	C2TH[47:0]	RW	N	0x7F FF FF FF FF FF	Charge2 threshold high	see C2 (0x10)	A•s

REGISTER DESCRIPTION

Table 33. Threshold Registers (continued)

ADDRESS	NAME	TYPE	COR	DEFAULT	PARAMETER	LSB	UNIT
Page1.0x26	C2TL[47:0]	RW	N	0x80 00 00 00 00 00	Charge2 threshold low	see C2 (0x10)	A•s
Page1.0x2C	TB2TH[31:0]	RW	N	0xFF FF FF FF	Time2 threshold high	see TB2 (0x1C)	s
Page1.0x30	E2TH[47:0]	RW	N	0x7F FF FF FF FF FF	Energy2 threshold high	see E2 (0x16)	W•s
Page1.0x36	E2TL[47:0]	RW	N	0x80 00 00 00 00 00	Energy2 threshold low	see E2 (0x16)	W•s
Page1.0x80	ITH[15:0]	RW	N	0x7F FF	Current threshold high	0.012	A
Page1.0x82	ITL[15:0]	RW	N	0x80 00	Current threshold low	0.012	A
Page1.0x84	PTH[15:0]	RW	N	0x7F FF	Power threshold high	0.2	W
Page1.0x86	PTL[15:0]	RW	N	0x80 00	Power threshold low	0.2	W
Page1.0x90	VTH[15:0]	RW	N	0x7F FF	V threshold high	2	mV
Page1.0x92	VTL[15:0]	RW	N	0x80 00	V threshold low	2	mV
Page1.0x94	TEMPTH[15:0]	RW	N	0x7F FF	Temperature threshold high = TEMPTH • 0.204 + 5.5		°C
Page1.0x96	TEMPTL[15:0]	RW	N	0x80 00	Temperature threshold low = TEMPTL • 0.204 + 5.5		°C
Page1.0x98	VDVCCTH[15:0]	RW	N	0X7F FF	V_{DVCC} threshold high	145	mV
Page1.0x9A	VDVCCTL[15:0]	RW	N	0X80 00	V_{DVCC} threshold low	145	mV
Page1.0x9C	TEMPFANH[15:0]	RW	N	0x7F FF	Fan temperature threshold high = TEMPFANH • 0.204 + 5.5		°C
Page1.0x9E	TEMPFANL[15:0]	RW	N	0x80 00	Fan temperature threshold low = TEMPFANL • 0.204 + 5.5		°C

The threshold comparators for accumulated quantities charge, energy and time use a floating point format internally. This can appear to cause slight bit-level comparison discrepancies, but the comparisons between Accumulated Results registers and their respective threshold registers will always have an accuracy of better than 0.001%.

Note that the threshold registers for current and power report only the 16 MSBs of the respective 18-bit result registers.

TYPICAL APPLICATIONS

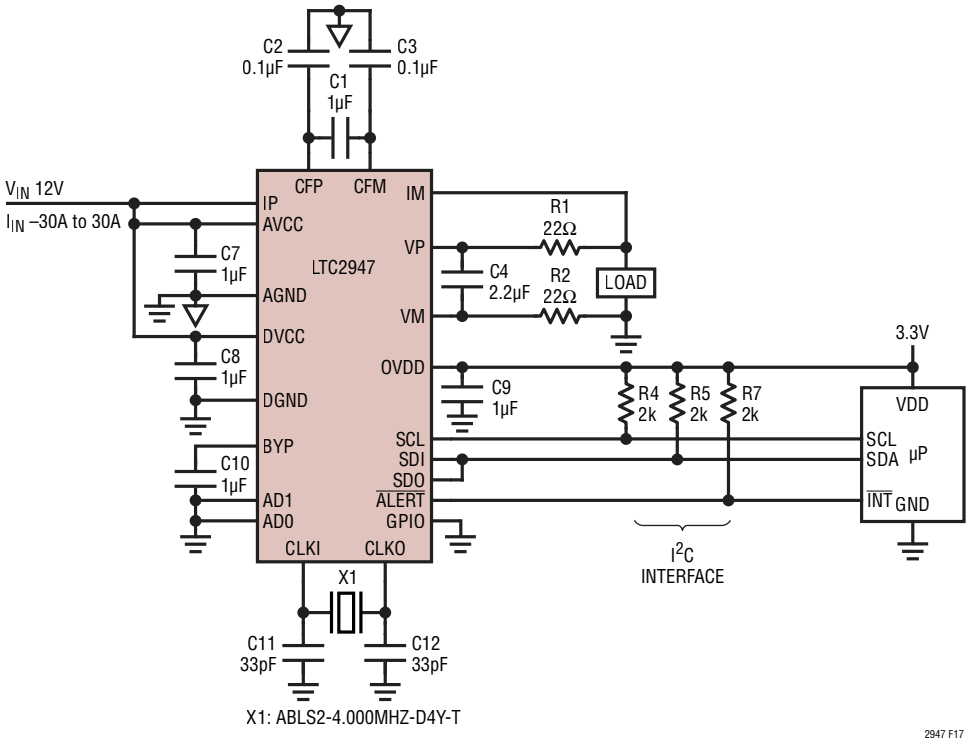


Figure 17. 12V, 30A Bidirectional Power, Energy and Charge Monitor with I²C Interface and High Side Sense

TYPICAL APPLICATIONS

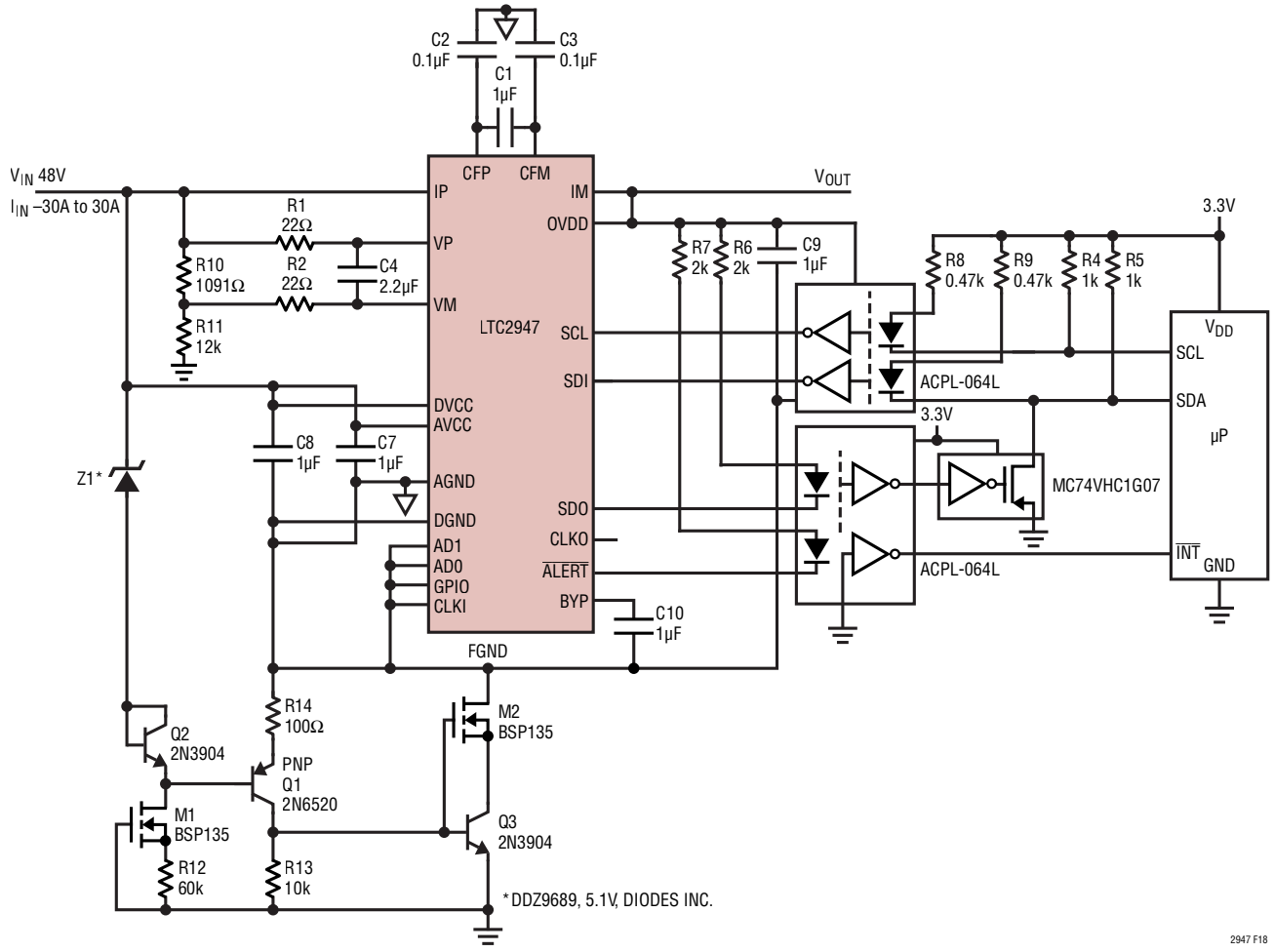
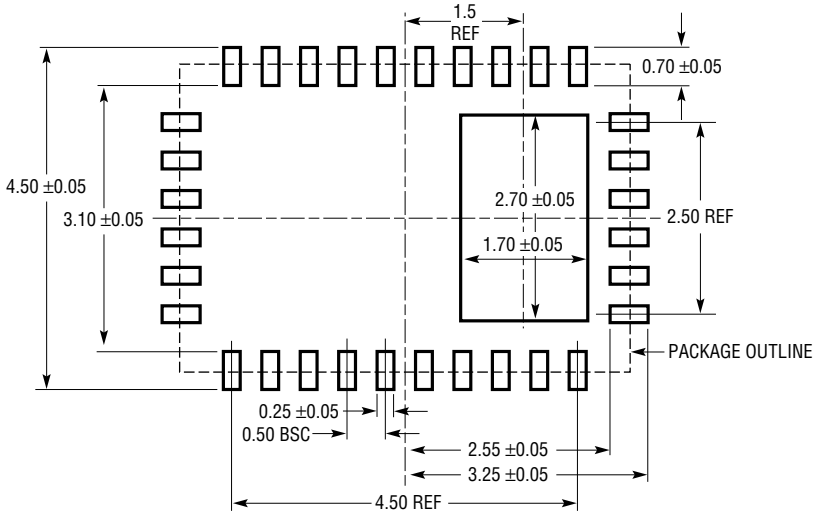


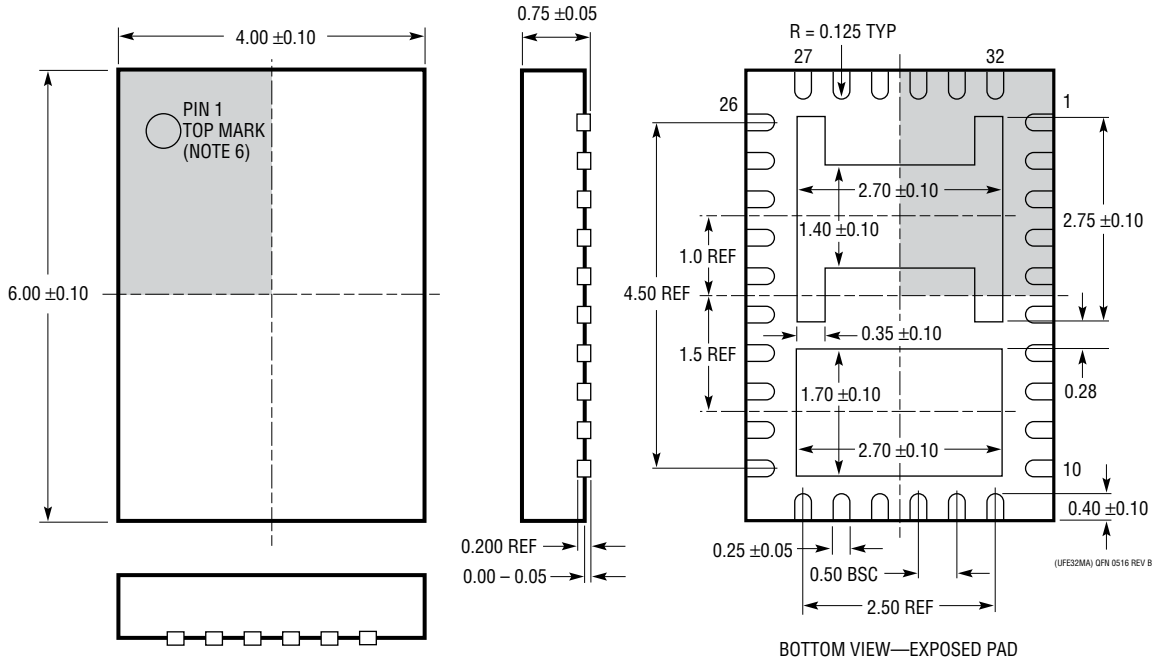
Figure 18. 48V Bidirectional Power, Energy and Charge Monitor with Isolated I²C Interface and High Side Sense

PACKAGE DESCRIPTION

UFE Package
Variation: UFE32MA
32-Lead Plastic QFN (4mm × 6mm)
(Reference LTC DWG # 05-08-1938 Rev B)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

Rev. B

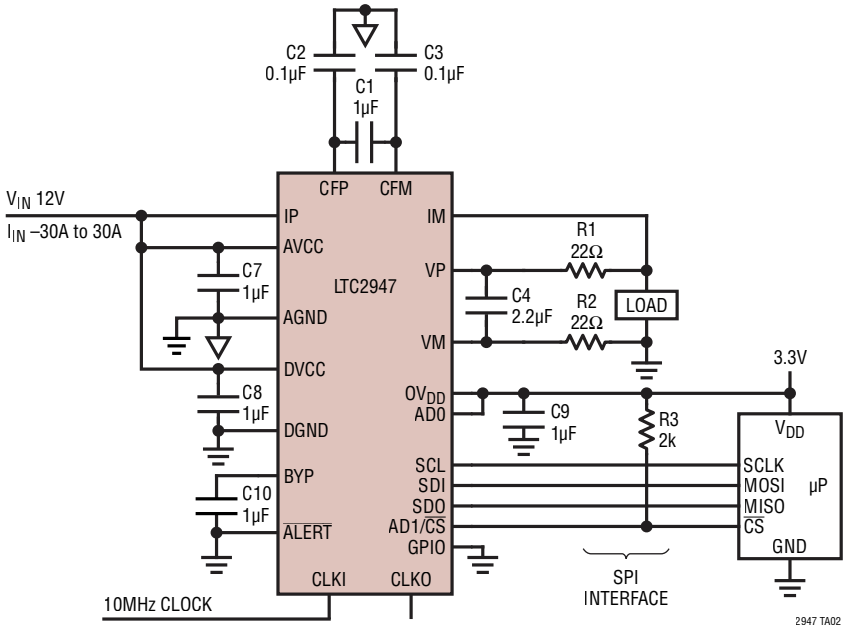
REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	02/17	Modified OVDD pin description.	10
B	03/19	Increased V_{AVCC}, V_{DVCC} min	4
		Increased V_{UVLO} max	4
		Updated website links	1-44

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TYPICAL APPLICATION

12V, 30A Bidirectional Power, Energy and Charge Monitor with SPI Interface



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT®2940	Power and Current Monitor	4-Quadrant Multiplication, ±5% Power Accuracy, 4V to 80V Operation
LTC2941	I²C Battery Gas Gauge	2.7V to 5.5V Operation, 1% Charge Accuracy
LTC2942	I²C Battery Gas Gauge with Temperature, Voltage Measurement	2.7V to 5.5V Operation, 1% Charge, Voltage and Temperature
LTC2943	Multicell Battery Gas Gauge with Temperature, Voltage and Current Measurement	3.6V to 20V Operation, 1% Charge, Voltage, Current and Temperature
LTC2945	Wide Range I²C Power Monitor	0V to 80V Operation, 12-Bit ADC with ±0.75% TUE
LTC2946	Wide Range I²C Power, Charge and Energy Monitor	2.7V to 100V Operation, 12-Bit Resolution
LTC2990	Quad I²C Temperature, Voltage and Current Monitor	3V to 5.5V Operation, 14-Bit ADC
LTC4150	Coulomb Counter/Battery Gas Gauge	2.7V to 8.5V Operation, Voltage-to-Frequency Converter
LTC4151	High Voltage I²C Current and Voltage Monitor	7V to 80V Operation, 12-Bit Resolution with ±1.25% TUE
LTC4215	Single Channel, Hot Swap Controller with I²C Monitoring	8-Bit ADC, Adjustable Current Limit and Inrush, 2.9V to 15V Operation
LTC4222	Dual Channel, Hot Swap Controller with I²C Monitoring	10-Bit ADC, Adjustable Current Limit and Inrush, 2.9V to 29V Operation
LTC4260	Positive High Voltage Hot Swap Controller with I²C Monitoring	8-Bit ADC, Adjustable Current Limit and Inrush, 8.5V to 80V Operation
LTC4261	Negative High Voltage Hot Swap Controller with I²C Monitoring	10-Bit ADC, Floating Topology, Adjustable Inrush
LTC4234	20A Guaranteed SOA Hot Swap Controller	2.9V to 15V Operation, 4mΩ MOSFET Including R_{SENSE}

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