RS232/RS485 Dual Multiprotocol Transceiver with Integrated Termination

FEATURES

- **Four RS232 and Two RS485 Transceivers**
- **3V to 5.5V Supply Voltage**
- **20Mbps RS485 and 500kbps RS232**
- **Automatic Selection of Integrated RS485 (120Ω) and RS232 (5kΩ) Termination Resistors**
- **Half-/Full-Duplex RS485 Switching**
- Logic Loopback Mode
- High ESD: ±16kV on Line I/O
- 1.7V to 5.5V Logic Interface
- Supports Up to 256 RS485 Nodes
- RS485 Receiver Full Failsafe Eliminates UART Lockup
- Available in 38-Pin 5mm × 7mm QFN Package

APPLICATIONS

- Flexible RS232/RS485/RS422 Interface
- Software Selectable Multiprotocol Interface Ports
- Point-of-Sale Terminals
- Cable Repeaters
- Protocol Translators
- PROFIBUS-DP Networks

DESCRIPTION

The LTC®2872 is a robust pin-configurable transceiver that supports RS232, RS485, and RS422 standards while operating on a single 3V to 5.5V supply. The LTC2872 can be configured as four RS232 single-ended transceivers or two RS485 differential transceivers, or combinations of both, on shared I/O lines.

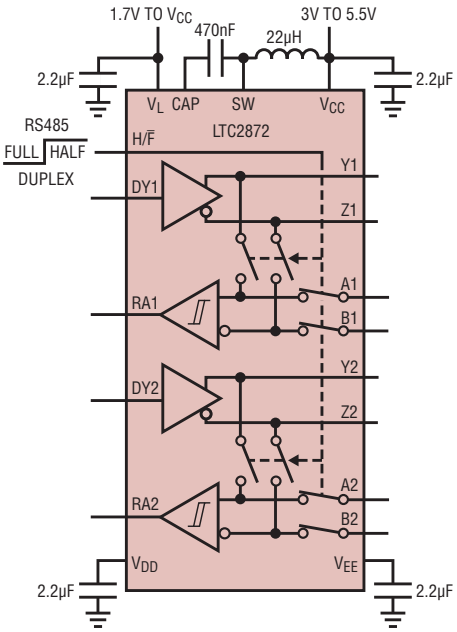
Pin-controlled integrated termination resistors allow for easy interface reconfiguration, eliminating external resistors and control relays. Half-duplex switches allow four-wire and two-wire RS485 configurations. Loopback mode steers the driver inputs to the receiver outputs for diagnostic self-test. The RS485 receivers support up to 256 nodes per bus, and feature full failsafe operation for floating, shorted or terminated inputs.

An integrated DC/DC boost converter uses a small inductor and one capacitor, eliminating the need for multiple supplies for driving RS232 levels.

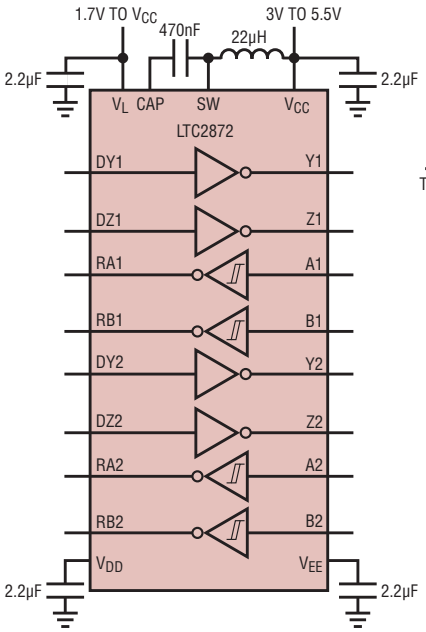
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TYPICAL APPLICATIONS

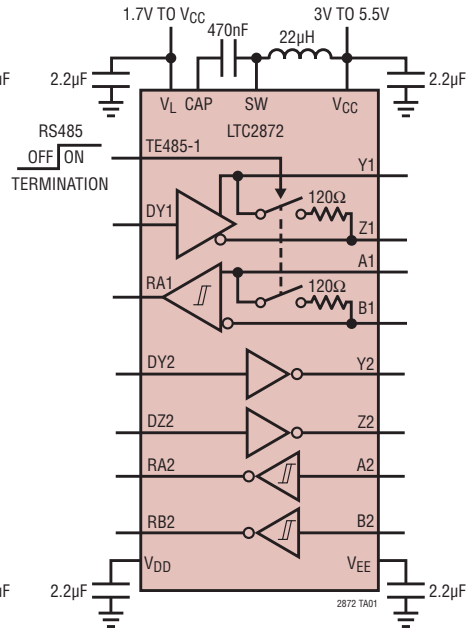
RS485 Mode with Duplex Control



RS232 Mode



Mixed Mode with RS485 Termination



ABSOLUTE MAXIMUM RATINGS

(Note 1)

Input Supplies

V_{CC}, V_L ..... –0.3V to 7V

Generated Supplies

V_{DD} ..... V_{CC} – 0.3V to 7.5V

V_{EE} ..... 0.3V to –7.5V

$V_{DD} – V_{EE}$ 15V

SW ..... –0.3V to (V_{DD} + 0.3V)

CAP ..... 0.3V to (V_{EE} – 0.3V)

A1, A2, B1, B2, Y1, Y2, Z1, Z2 ..... –15V to 15V

DY1, DY2, DZ1, DZ2, $\overline{RXEN1}$, $\overline{RXEN2}$, DXEN1, DXEN2, LB, H/$\overline{F}$, TE485_1, TE485_2, 485/$\overline{232}$_1, 485/$\overline{232}$_2 ..... –0.3V to 7V

FEN, RA1, RA2, RB1, RB2 ..... –0.3V to (V_L + 0.3V)

Differential Enabled Terminator Voltage

(A1-B1 or A2-B2 or Y1-Z1 or Y2-Z2) ..... ±6V

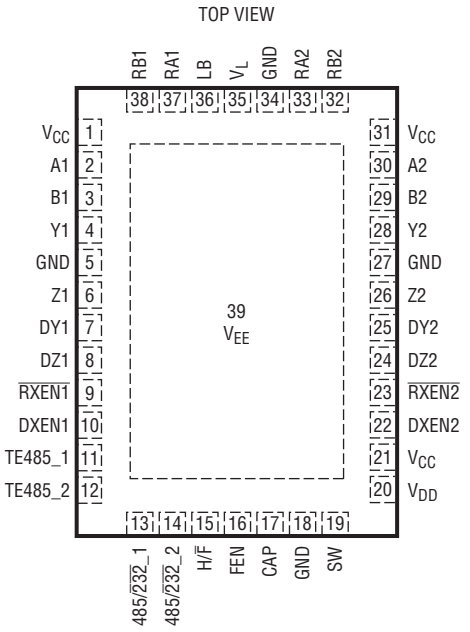
Operating Temperature

LTC2872C ..... 0°C to 70°C

LTC2872I ..... –40°C to 85°C

Storage Temperature Range ..... –65°C to 125°C

PIN CONFIGURATION



UHF PACKAGE
38-LEAD (5mm × 7mm) PLASTIC QFN

T_{JMAX} = 125°C, θ_{JA} = 34.7°C/W
EXPOSED PAD (PIN #39) IS V_{EE}, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC2872CUHF#PBF	LTC2872CUHF#TRPBF	2872	38-Lead (5mm × 7mm) Plastic QFN	0°C to 70°C
LTC2872IUHF#PBF	LTC2872IUHF#TRPBF	2872	38-Lead (5mm × 7mm) Plastic QFN	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = V_L = 3.3V, TE485_1 = TE485_2 = 0V, LB = 0V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Power Supply							
V_{CC}	Supply Voltage Operating Range		●	3		5.5	V
V_L	Logic Supply Voltage Operating Range	$V_L \le V_{CC}$	●	1.7		V_{CC}	V
	V_{CC} Supply Current in Shutdown Mode	$\overline{RXEN1}$ = $\overline{RXEN2}$ = V_L, DXEN1 = DXEN2 = FEN = H/$\overline{F}$ = 0V	●		8	60	µA
	V_{CC} Supply Current in RS485 Transceiver Mode (Outputs Unloaded) (Note 3)	485/$\overline{232}$_1 = 485/$\overline{232}$_2 = DXEN1 = DXEN2 = V_L, $\overline{RXEN1}$ = $\overline{RXEN2}$ = 0V	●		4.5	7	mA
	V_{CC} Supply Current in RS232 Transceiver Mode (Outputs Unloaded) (Note 3)	DXEN1 = DXEN2 = V_L; 485/$\overline{232}$_1 = 485/$\overline{232}$_2 = $\overline{RXEN1}$ = $\overline{RXEN2}$ = 0V	●		5.5	8	mA
	V_L Supply Current in RS485 or RS232 Transceive Mode (Outputs Unloaded)	DXEN1 = DXEN2 = V_L, $\overline{RXEN1}$ = $\overline{RXEN2}$ = 0V	●		0	5	µA
RS485 Drivers							
$\lvert V_{OD} \rvert$	Differential Output Voltage	R_L = ∞, V_{CC} = 3V (Figure 1)	●			6	V
		R_L = 27Ω, V_{CC} = 4.5V (Figure 1)	●	2.1		V_{CC}	V
		R_L = 27Ω, V_{CC} = 3V (Figure 1)	●	1.5		V_{CC}	V
		R_L = 50Ω, V_{CC} = 3.13V (Figure 1)	●	2		V_{CC}	V
$\Delta\lvert V_{OD} \rvert$	Difference in Magnitude of Differential Output Voltage for Complementary Output States	R_L = 27Ω, V_{CC} = 3V (Figure 1)	●			0.2	V
		R_L = 50Ω, V_{CC} = 3.13V (Figure 1)	●			0.2	V
V_{OC}	Common Mode Output Voltage	R_L = 27Ω or 50Ω (Figure 1)	●			3	V
$\Delta\lvert V_{OC} \rvert$	Difference in Magnitude of Common Mode Output Voltage for Complementary Output States	R_L = 27Ω or 50Ω (Figure 1)	●			0.2	V
I_{OZD485}	Three-State (High Impedance) Output Current	V_{OUT} = 12V or –7V, V_{CC} = 0V or 3.3V (Figure 2)	●	–100		125	µA
I_{OSD485}	Maximum Short-Circuit Current	–7V ≤ V_{OUT} ≤ 12V (Figure 2)	●	–250		250	mA
RS485 Receiver							
I_{IN485}	Input Current	V_{IN} = 12V or –7V, V_{CC} = 0V or 3.3V (Figure 3) (Note 5)	●	–100		125	µA
R_{IN485}	Input Resistance	V_{IN} = 12V or –7V, V_{CC} = 0V or 3.3V (Figure 3) (Note 5)			125		kΩ
	Differential Input Signal Threshold Voltage (A–B)	–7V ≤ (A or B) ≤ 12 (Note 5)	●			±200	mV
	Differential Input Signal Hysteresis	B = 0V (Notes 3, 5)			190		mV
	Differential Input DC Failsafe Threshold Voltage (A–B)	–7V ≤ (A or B) ≤ 12 (Note 5)	●	–200	–65	0	mV
	Differential Input DC Failsafe Hysteresis	B = 0V (Note 5)			30		mV
V_{OL}	Output Low Voltage	Output Low, I(RA) = 3mA (Sinking), 3V ≤ V_L ≤ 5.5V	●			0.4	V
		Output Low, I(RA) = 1mA (Sinking), 1.7V ≤ V_L < 3V	●			0.4	V
V_{OH}	Output High Voltage	Output High, I(RA) = –3mA (Sourcing), 3V ≤ V_L ≤ 5.5V	●	V_L – 0.4			V
		Output High, I(RA) = –1mA (Sourcing), 1.7V ≤ V_L < 3V	●	V_L – 0.4			V
	Three-State (High Impedance) Output Current	0V ≤ RA ≤ V_L, V_L = 5.5V	●		0	±5	µA
	Short-Circuit Output Current	0V ≤ RA ≤ V_L, V_L = 5.5V	●			±135	mA
R_{TERM}	Terminating Resistor	TE485 = V_L, A–B = 2V, B = –7V, 0V, 10V (Figure 8) (Note 5)	●	108	120	156	Ω

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = V_L = 3.3V, TE485_1 = TE485_2 = 0V, LB = 0V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
RS232 Driver							
V_{OLD}	Output Low Voltage	R_L = 3kΩ, V_{EE} ≤ –6V	●	–5	–5.7	V_{EE}	V
V_{OHD}	Output High Voltage	R_L = 3kΩ, V_{DD} ≥ 6.5V	●	5	6.2	V_{DD}	V
	Three-State (High Impedance) Output Current	Y or Z = ±15V	●			±156	µA
	Output Short-Circuit Current	Y or Z = 0V	●		±35	±90	mA
RS232 Receiver							
	Input Threshold Voltage		●	0.6	1.5	2.5	V
	Input Hysteresis		●	0.1	0.4	1.0	V
	Output Low Voltage	I(RA, RB) = 1mA (Sinking), 1.7V ≤ V_L ≤ 5.5V	●			0.4	V
	Output High Voltage	I(RA, RB) = –1mA (Sourcing), 1.7V ≤ V_L ≤ 5.5V	●	V_L – 0.4			V
	Input Resistance	–15V ≤ (A, B) ≤ 15V, Receiver Enabled	●	3	5	7	kΩ
	Three-State (High Impedance) Output Current	0V ≤ (RA, RB) ≤ V_L	●		0	±5	µA
	Output Short-Circuit Current	V_L = 5.5V, 0V ≤ (RA, RB) ≤ V_L	●		±25	±50	mA
Logic Inputs							
	Threshold Voltage		●	0.4		0.75•V_L	V
	Input Current		●		0	±5	µA
Power Supply Generator							
V_{DD}	Regulated V_{DD} Output Voltage	RS232 Drivers Enabled, Outputs Loaded with R_L = 3kΩ to GND, DY1 = DY2 = V_L, DZ1 = DZ2 = 0V (Note 3)			7		V
V_{EE}	Regulated V_{EE} Output Voltage				–6.3		V
ESD							
	Interface Pins (A, B, Y, Z)	Human Body Model to GND or V_{CC}, Powered or Unpowered (Note 7)			±16		kV
	All Other Pins	Human Body Model (Note 7)			±4		kV

SWITCHING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = V_L = 3.3V, TE485_1 = TE485_2 = 0V, LB = 0V unless otherwise noted. $V_L \le V_{CC}$.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
RS485 AC Characteristics							
	Maximum Data Rate	(Note 3)	●	20			Mbps
$t_{PLHD485}$ $t_{PHLD485}$	Driver Propagation Delay	R_{DIFF} = 54Ω, C_L = 100pF (Figure 4)	●		20	70	ns
	Driver Propagation Delay Difference $\lvert t_{PLHD485} - t_{PHLD485} \rvert$	R_{DIFF} = 54Ω, C_L = 100pF (Figure 4)	●		1	6	ns
$t_{SKEWD485}$	Driver Skew (Y to Z)	R_{DIFF} = 54Ω, C_L = 100pF (Figure 4)	●		1.5	±8	ns
t_{RD485}, t_{FD485}	Driver Rise or Fall Time	R_{DIFF} = 54Ω, C_L = 100pF (Figure 4)	●		7.6	15	ns
t_{ZLD485}, t_{ZHD485}, t_{LZD485}, t_{HZD485}	Driver Output Enable or Disable Time	FEN = V_L, R_L = 500Ω, C_L = 50pF (Figure 5)	●			120	ns
$t_{ZHSD485}$, $t_{ZLSD485}$	Driver Enable from Shutdown	FEN = 0V, R_L = 500Ω, C_L = 50pF (Figure 5)	●		0.2	2	ms
$t_{PLHR485}$, $t_{PHLR485}$	Receiver Input to Output	C_L = 15pF, V_{CM} = 1.5V, |A–B| = 1.5V, (Figure 6) (Note 5)	●		55	85	ns
$t_{SKEWR485}$	Differential Receiver Skew $\lvert t_{PLHR485} - t_{PHLR485} \rvert$	C_L = 15pF (Figure 6)	●		1	9	ns
t_{RR485}, t_{FR485}	Receiver Output Rise or Fall Time	C_L = 15pF (Figure 6)	●		3	15	ns
t_{ZLR485}, t_{ZHR485} t_{LZR485}, t_{HZR485}	Receiver Output Enable or Disable Time	FEN = V_L, R_L = 1k, C_L = 15pF (Figure 7)	●		30	85	ns
$t_{RTEN485}$, t_{RTZ485}	Termination Enable or Disable Time	FEN = V_L, V_B = 0V, V_{AB} = 2V (Figure 8) (Note 5)	●			100	µs
RS232 AC Characteristics							
	Maximum Data Rate	R_L = 3kΩ, C_L = 2500pF, R_L = 3kΩ, C_L = 500pF (Note 3)	● ●	100 500			kbps kbps
	Driver Slew Rate (Figure 9)	R_L = 3kΩ, C_L = 2500pF R_L = 3kΩ, C_L = 50pF	● ●	4		 30	V/µs V/µs
$t_{PHLD232}$, $t_{PLHD232}$	Driver Propagation Delay	R_L = 3kΩ, C_L = 50pF (Figure 9)	●		1	2	µs
$t_{SKEWD232}$	Driver Skew	R_L = 3kΩ, C_L = 50pF (Figure 9)			50		ns
t_{ZLD232}, t_{ZHD232} t_{LZD232}, t_{HZD232}	Driver Output Enable or Disable Time	FEN = V_L, R_L = 3kΩ, C_L = 50pF (Figure 10)	●		0.4	2	µs
$t_{PHLR232}$, $t_{PLHR232}$	Receiver Propagation Delay	C_L = 150pF (Figure 11)	●		60	200	ns
$t_{SKEWR232}$	Receiver Skew	C_L = 150pF (Figure 11)			25		ns
t_{RR232}, t_{FR232}	Receiver Rise or Fall Time	C_L = 150pF (Figure 11)	●		60	200	ns
t_{ZLR232}, t_{ZHR232}, t_{LZR232}, t_{HZR232}	Receiver Output Enable or Disable Time	FEN = V_L, R_L = 1kΩ, C_L = 150pF (Figure 12)	●		0.7	2	µs
Power Supply Generator							
	V_{DD}/V_{EE} Supply Rise Time	FEN = ↓, (Notes 3 and 4)	●		0.2	2	ms

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2. All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to device ground unless otherwise specified.

Note 3. Guaranteed by other measured parameters and not tested directly.

Note 4. Time from FEN ↓ until $V_{DD} \ge 5V$ and $V_{EE} \le -5V$. External components as shown in typical application.

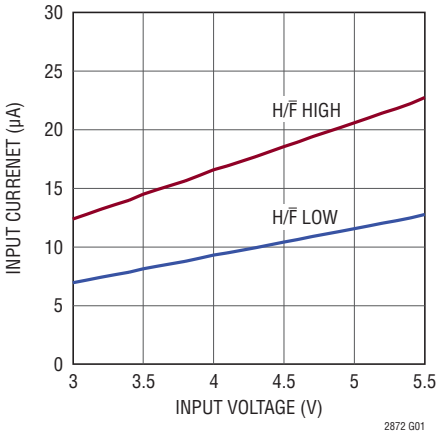
Note 5. Condition applies to A, B for H/$\overline{F}$ = 0V, and Y, Z for H/$\overline{F}$ = V_L.

Note 6. This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Overtemperature protection activates at a junction temperature exceeding 150°C. Continuous operation above the specified maximum operating junction temperature may result in device degradation or failure.

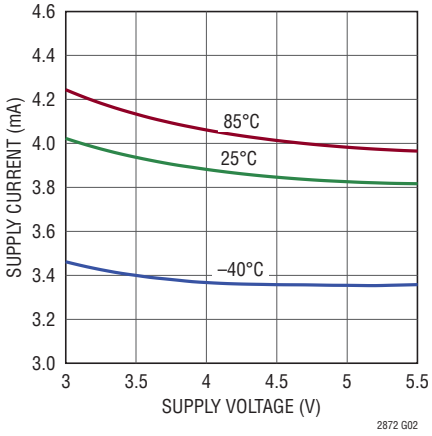
Note 7. Guaranteed by design and not subject to production test.

TYPICAL PERFORMANCE CHARACTERISTICS

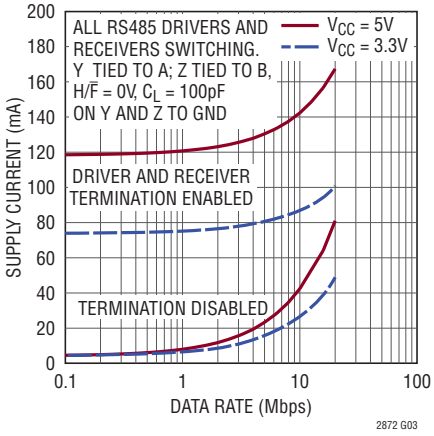
V_{CC} Supply Current vs Supply Voltage in Shutdown Mode



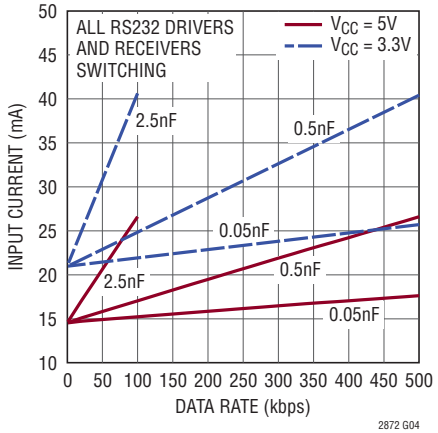
V_{CC} Supply Current vs Supply Voltage in Fast Enable Mode



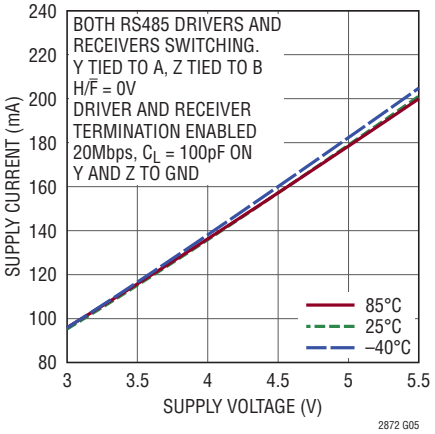
V_{CC} Supply Current vs RS485 Data Rate



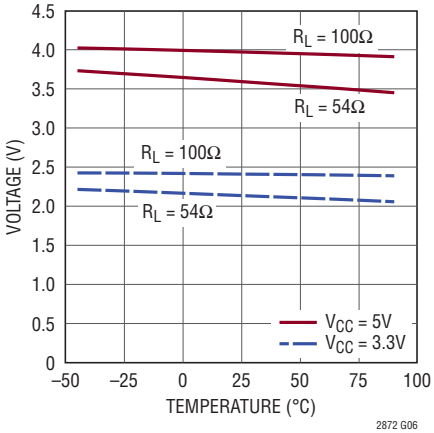
V_{CC} Supply Current vs RS232 Data Rate



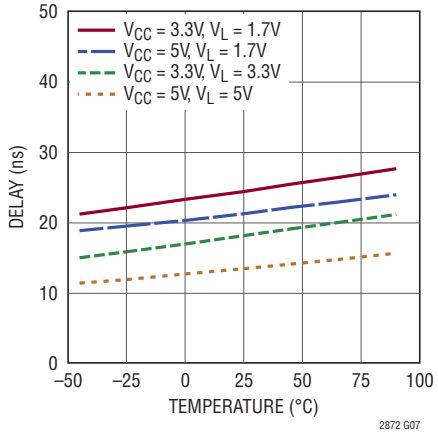
V_{CC} Supply Current vs Supply Voltage for RS485 at Maximum Data Rate



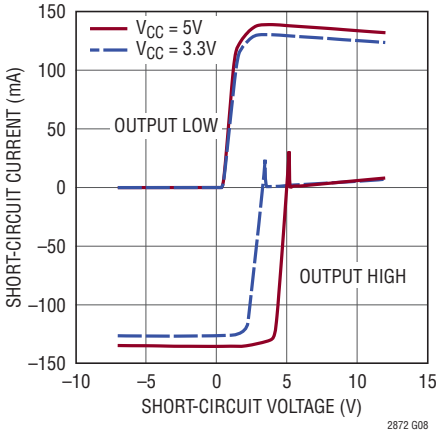
RS485 Driver Differential Output Voltage vs Temperature



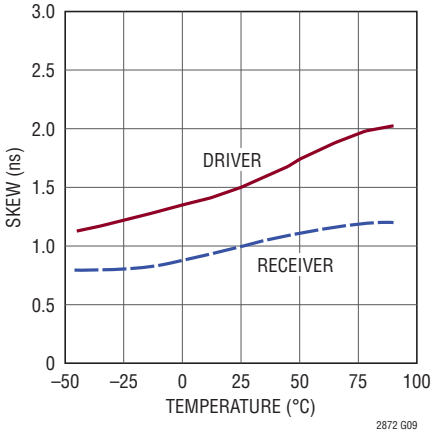
RS485 Driver Propagation Delay vs Temperature



RS485 Driver Short-Circuit Current vs Short-Circuit Voltage

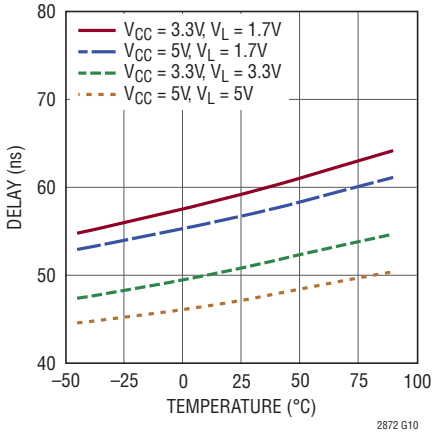


RS485 Driver and Receiver Skew vs Temperature

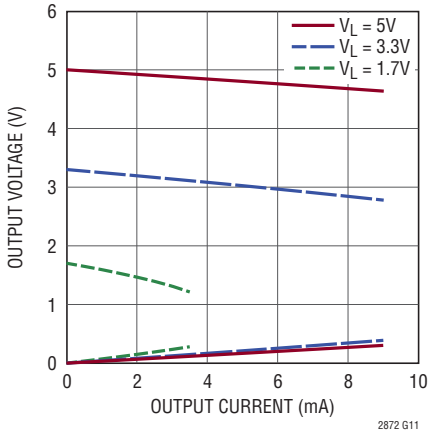


TYPICAL PERFORMANCE CHARACTERISTICS

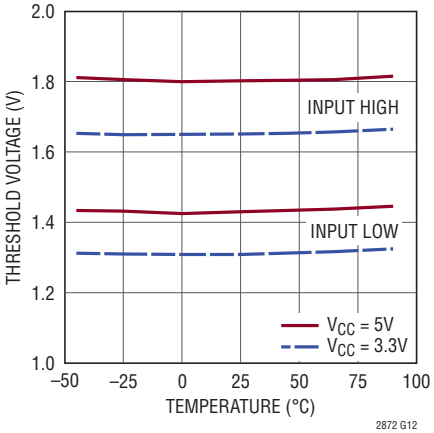
RS485 Receiver Propagation Delay vs Temperature



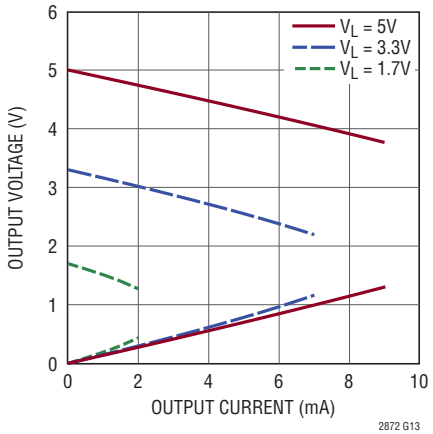
RS485 Receiver Output Voltage vs Load Current



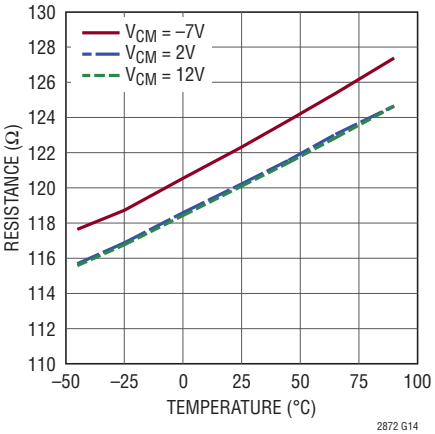
RS232 Receiver Input Threshold vs Temperature



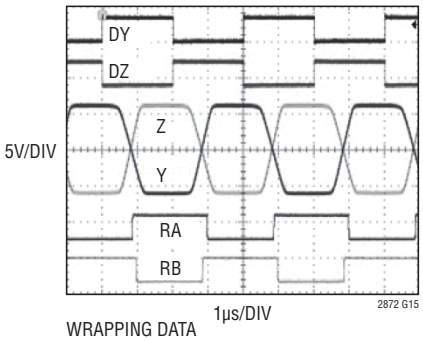
RS232 Receiver Output Voltage vs Load Current



RS485 Termination Resistance vs Temperature



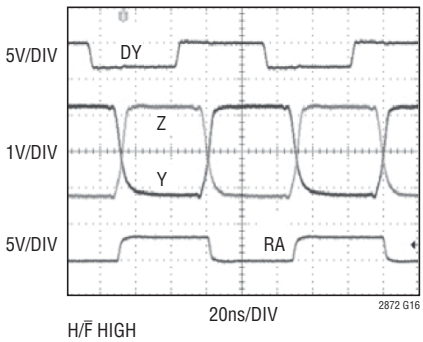
RS232 Operation at 500kbps



1µs/DIV

WRAPPING DATA
DOUT LOADS: 5kΩ + 50pF

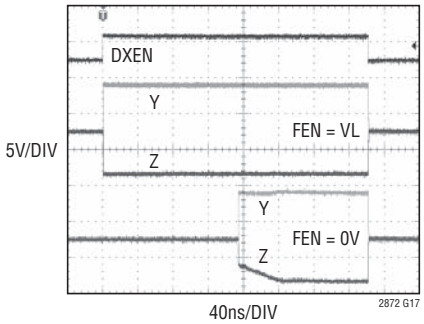
RS485 Operation at 20Mbps



20ns/DIV

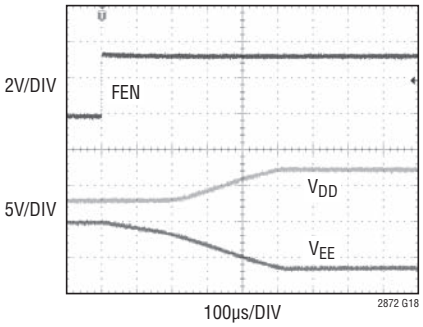
H/$\overline{F}$ HIGH
Y, Z LOADS: 120Ω (DIFF) + 50pF

RS232 Driver Outputs Enabling and Disabling



40ns/DIV

V_{DD} and V_{EE} Powering Up



100µs/DIV

PIN FUNCTIONS

V_{CC} (Pins 1, 21, 31): Input Supply (3.0V to 5.5V). Tie all three pins together and connect 2.2µF capacitor between VCC and GND.

V_L (Pin 35): Logic Supply (1.7V to 5.5V) for the receiver outputs, driver inputs, and control inputs. This pin should be bypassed to GND with a 0.1µF capacitor if it is not tied to V_{CC}. V_L must be less than or equal to V_{CC} for proper operation.

V_{DD} (Pin 20): Generated Positive Supply Voltage for RS232 Driver (7V). Connect 2.2µF capacitor between V_{DD} and GND.

V_{EE} (Pin 39): Generated Negative Supply Voltage for RS232 Driver (–6.3V). Tie all pins together and connect 2.2µF capacitor between V_{EE} and GND.

GND (Pins 5, 18, 27, 34): Ground. Tie all four pins together.

CAP (Pin 17): Charge Pump Capacitor for Generated Negative Supply Voltage. Connect a 470nF capacitor between CAP and SW.

SW (Pin 19): Switch Pin. Connect 22µH inductor between SW and V_{CC}.

A1 (Pin 2): RS485 Differential Receiver #1 Positive Input (Full-Duplex Mode) or RS232 Receiver #1a Input.

A2 (Pin 30): RS485 Differential Receiver #2 Positive Input (Full-Duplex Mode) or RS232 Receiver #2a Input.

B1 (PIn 3): RS485 Differential Receiver #1 Negative Input (Full-Duplex Mode) or RS232 Receiver #1b Input.

B2 (Pin 29): RS485 Differential Receiver #1 Negative Input (Full-Duplex Mode) or RS232 Receiver #2b Input.

RA1 (Pin 37): RS485 Differential Receiver #1 Output or RS232 Receiver #1a Output.

RA2 (Pin 33): RS485 Differential Receiver #2 Output or RS232 Receiver #2a Output.

RB1 (Pin 38): RS232 Receiver #1b Output.

RB2 (Pin 32): RS232 Receiver #2b Output.

DY1 (Pin 7): RS485 Differential Driver #1 Input or RS232 Driver #1y Input.

DY2 (Pin 25): RS485 Differential Driver #2 Input or RS232 Driver #2y Input.

DZ1 (Pin 8): RS232 Driver #1z Input.

DZ2 (Pin 24): RS232 Driver #2z Input.

Y1 (Pin 4): RS485 Differential Driver #1 Positive Output or RS232 Driver #1y Output, RS485 Differential Receiver #1 Positive Input (Half-Duplex Mode).

Y2 (Pin 28): RS485 Differential Driver #2 Positive Output or RS232 Driver #2y Output, RS485 Differential Receiver #2 Positive Input (Half-Duplex Mode).

Z1 (Pin 6): RS485 Differential Driver #1 Negative Output or RS232 Driver #1z Output, RS485 Differential Receiver #1 Negative Input (Half-Duplex Mode).

Z2 (Pin 26): RS485 Differential Driver #2 Negative Output or RS232 Driver #2z Output, RS485 Differential Receiver #2 Negative Input (Half-Duplex Mode).

485/$\overline{232}$_1 (Pin 13): Interface Select #1 Input. A logic low enables RS232 mode and a high enables RS485 mode for transceiver #1. The mode determines which transceiver inputs and outputs are accessible at the LTC2872 pins as well as which is controlled by the driver and receiver enable pins.

485/$\overline{232}$_2 (Pin 14): Interface Select #2 Input. A logic low enables RS232 mode and a high enables RS485 mode for transceiver #2. The mode determines which transceiver inputs and outputs are accessible at the LTC2872 pins as well as which is controlled by the driver and receiver enable pins.

$\overline{RXEN1}$ (Pin 9): Receivers #1 Enable. A logic high disables RS232 and RS485 receivers in transceiver #1, leaving their outputs Hi-Z. A logic low enables the RS232 or RS485 receivers in transceiver #1, depending on the state of the Interface Select Input 485/$\overline{232}$_1.

$\overline{RXEN2}$ (Pin 23): Receivers #2 Enable. A logic high disables RS232 and RS485 receivers in transceiver #2, leaving their outputs Hi-Z. A logic low enables the RS232 or RS485 receivers in transceiver #2, depending on the state of the Interface Select Input 485/$\overline{232}$_2.

PIN FUNCTIONS

DXEN1 (Pin 10): Drivers #1 Enable. A logic low disables the RS232 and RS485 drivers in transceiver #1, leaving their outputs in a Hi-Z state. A logic high enables the RS232 or RS485 drivers in transceiver #1, depending on the state of the Interface Select Input 485/$\overline{232}$_1.

DXEN2 (Pin 22): Drivers #2 Enable. A logic low disables the RS232 and RS485 drivers in transceiver #2, leaving their outputs in a Hi-Z state. A logic high enables the RS232 or RS485 drivers in transceiver #2, depending on the state of the Interface Select Input 485/$\overline{232}$_2.

TE485_1 (Pin 11): RS485 Termination Enable for Transceiver #1. A logic high enables a 120Ω resistor between pins A1 and B1. If DZ1 is also high, a 120Ω resistor is enabled between pins Y1 and Z1. A logic low on TE485_1 opens the resistors, leaving A1/B1 and Y1/Z1 unterminated, independent of DZ1. The differential termination resistors are never enabled in RS232 mode.

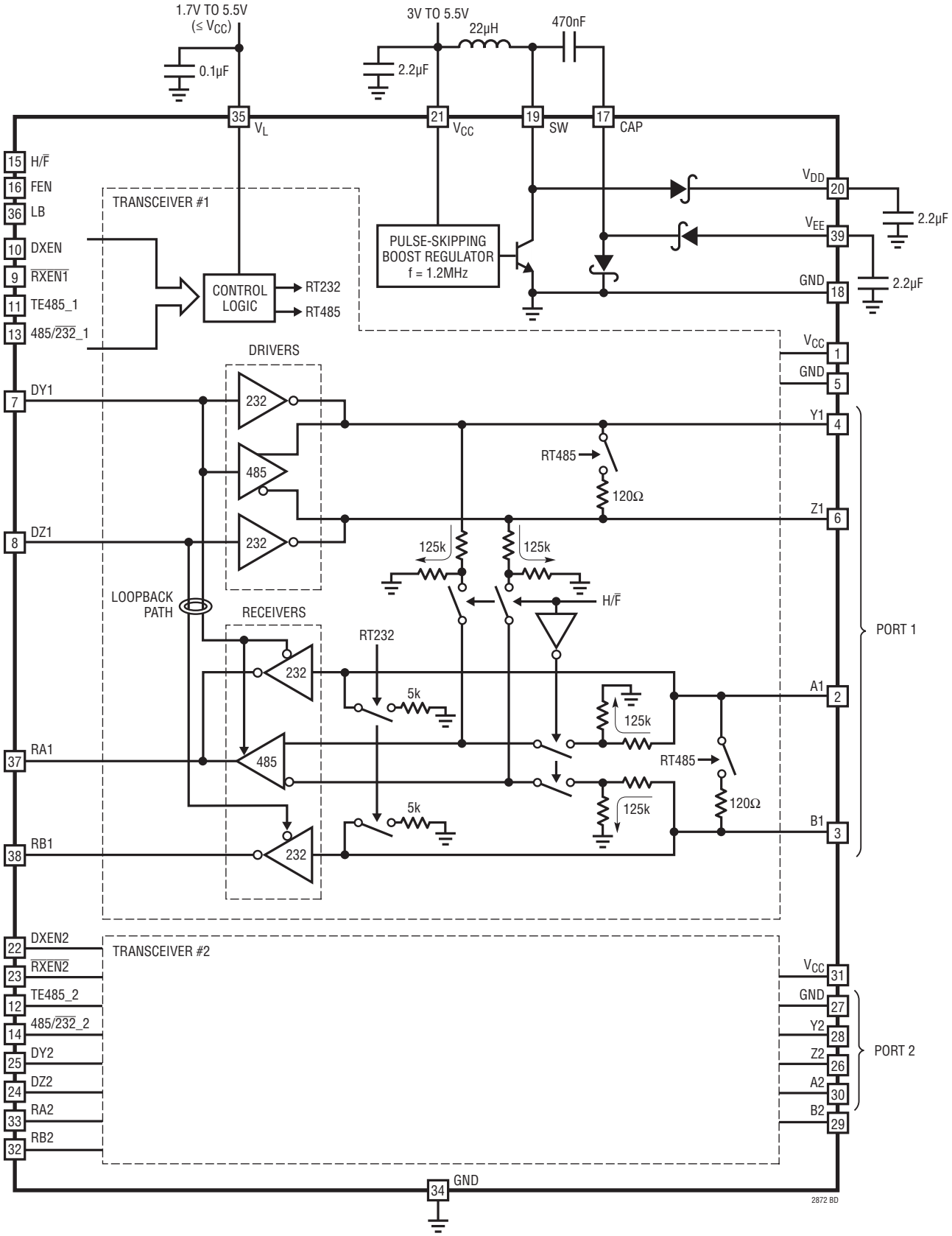
TE485_2 (Pin 12): RS485 Termination Enable for Transceiver #2. A logic high enables a 120Ω resistor between pins A2 and B2. If DZ2 is also high, a 120Ω resistor is enabled between pins Y2 and Z2. A logic low on TE485_2 opens the resistors, leaving A2/B2 and Y2/Z2 unterminated, independent of DZ2. The differential termination resistors are never enabled in RS232 mode.

H/$\overline{F}$ (Pin 15): RS485 Half-duplex Select Input for Transceivers #1 and #2. A logic low is used for full duplex operation where pins A and B are the receiver inputs and pins Y and Z are the driver outputs. A logic high is used for half duplex operation where pins Y and Z are both the receiver inputs and driver outputs and pins A and B do not serve as the receiver inputs. The impedance on A and B and state of differential termination between A and B is independent of the state of H/$\overline{F}$. The H/$\overline{F}$ pin has no effect on RS232 operation.

FEN (Pin 16): Fast Enable. A logic high enables Fast Enable Mode. In fast enable mode the integrated DC/DC converter is active independent of the state of driver, receiver, and termination enable pins allowing faster circuit enable times than are otherwise possible. A logic low disables Fast Enable Mode leaving the state of the DC/DC converter dependent on the state of driver, receiver, and termination enable control inputs. The DC/DC converter powers down only when FEN is low and all drivers, receivers, and terminators are disabled (refer to Table 1).

LB (Pin 36): Loopback Enable for Transceivers #1 and #2. A logic high enables Logic Loopback diagnostic mode, internally routing the driver input logic levels to the receiver output pins within the same transceiver. This applies to both RS232 channels as well as the RS485 driver/receiver. The targeted receiver must be enabled for the loopback signal to be available on its output. A logic low disables loopback mode. In loopback mode, signals are not inverted from driver inputs to receiver outputs.

BLOCK DIAGRAM



TEST CIRCUITS

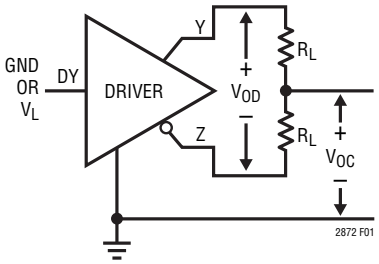


Figure 1. RS485 Driver DC Characteristics

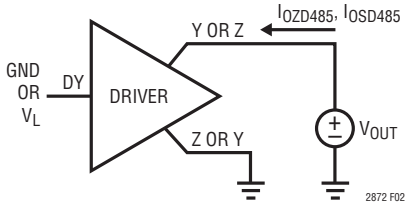


Figure 2. RS485 Driver Output Short-Circuit Current

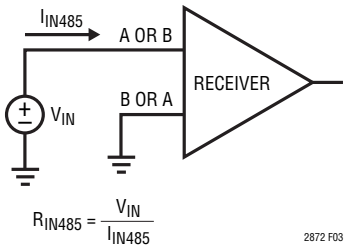


Figure 3. RS485 Receiver Input Current and Resistance (Note 5)

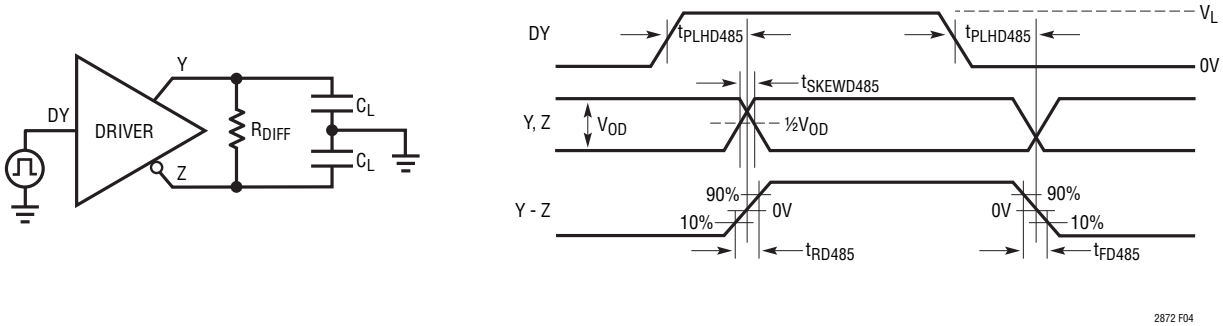


Figure 4. RS485 Driver Timing Measurement

TEST CIRCUITS

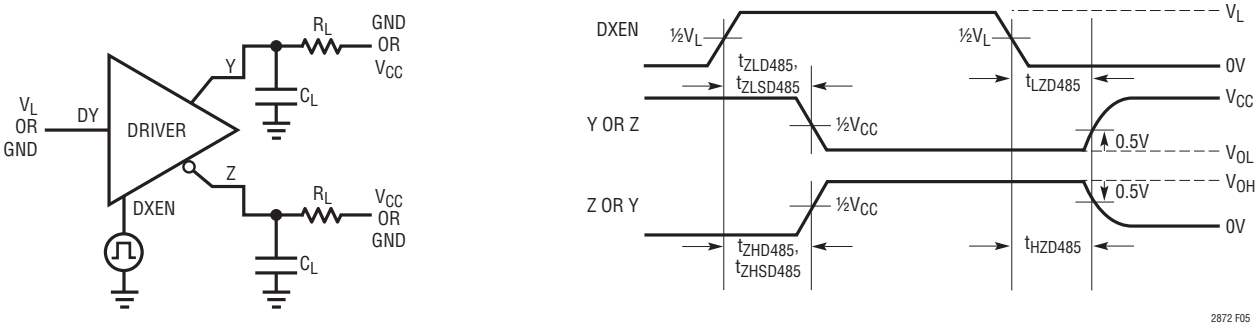


Figure 5. RS485 Driver Enable and Disable Timing Measurements

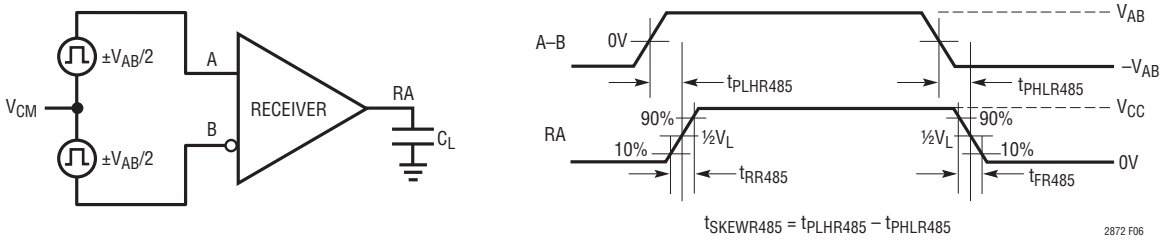


Figure 6. RS485 Receiver Propagation Delay Measurements (Note 5)

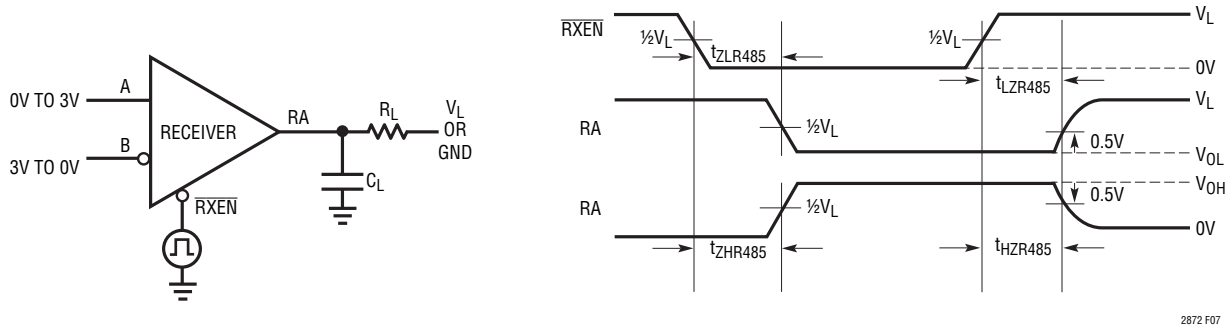


Figure 7. RS485 Receiver Enable and Disable Timing Measurements (Note 5)

TEST CIRCUITS

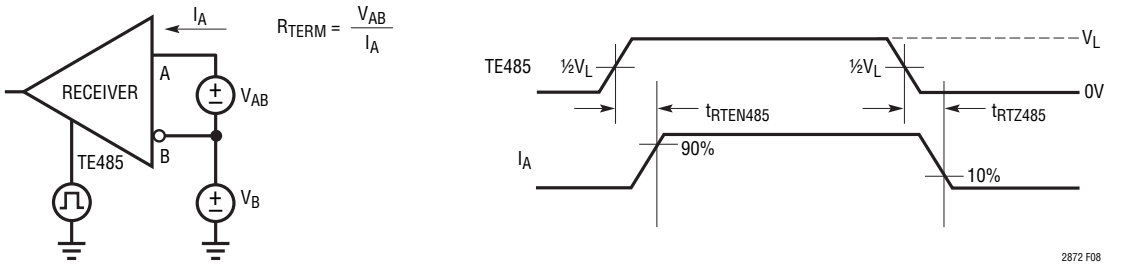


Figure 8. RS485 Termination Resistance and Timing Measurements (Note 5)

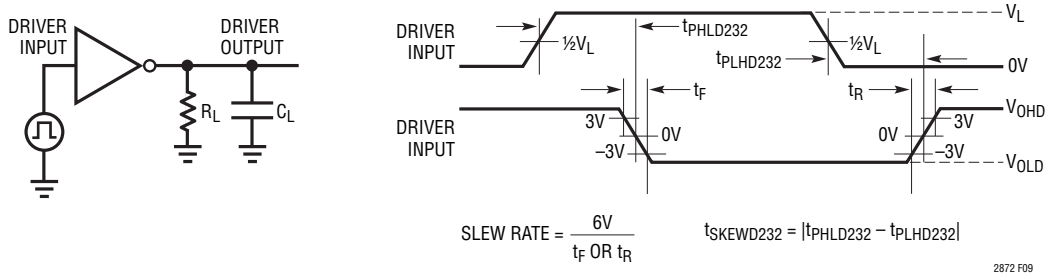


Figure 9. RS232 Driver Timing and Slew Rate Measurements

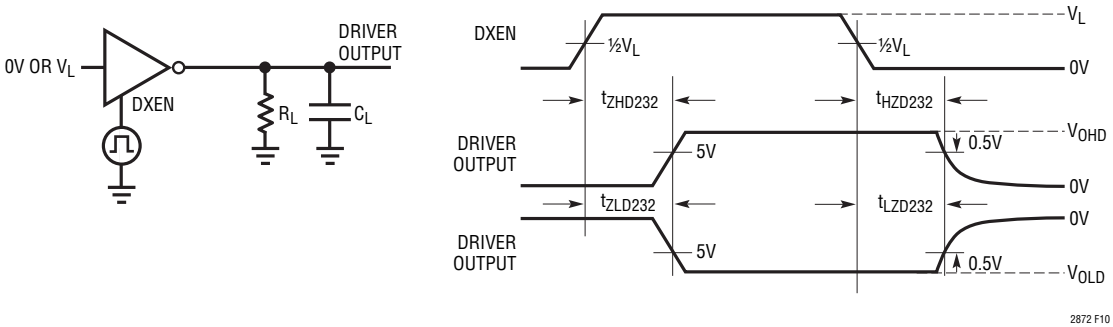


Figure 10. RS232 Driver Enable and Disable Times

TEST CIRCUITS

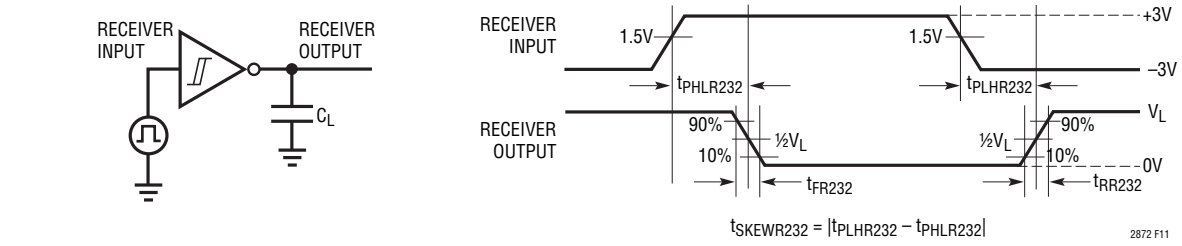


Figure 11. RS232 Receiver Timing Measurements

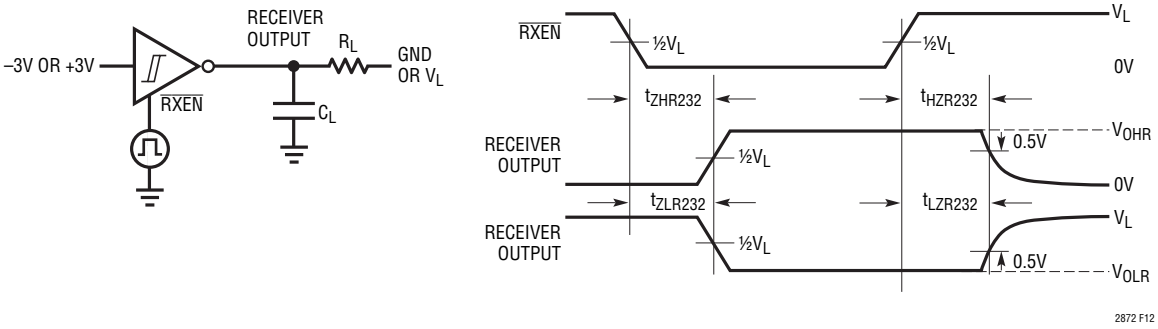


Figure 12. RS232 Receiver Enable and Disable Times

FUNCTION TABLES

Table 1. Shutdown and Fast Enable Modes

FEN	485/$\overline{232}$_1 AND 485/$\overline{232}$_2	$\overline{RXEN1}$ AND $\overline{RXEN2}$	DXEN1 AND DXEN2	TE485_1 AND TE485_2	H/$\overline{F}$	LB	DC/DC CONVERTER	MODE AND COMMENTS
0	X	1	0	0	X	X	OFF	Shutdown: All Main Functions Off
1	X	1	0	0	X	X	ON	Fast-Enable: DC/DC Converter On Only

Table 2. Mode Selection Table for a Given Port (FEX = X)

485/$\overline{232}$	RXEN	DXEN	TE485	H/$\overline{F}$	LB	DC/DC CONVERTER	MODE AND COMMENTS
0	X	1	X	X	0	ON	RS232 Drivers On
0	0	X	X	X	0	ON	RS232 Receivers On
1	X	1	X	X	0	ON	RS485 Driver On
1	0	X	X	X	0	ON	RS485 Receiver On
1	X	X	1	X	X	ON	RS485 Termination Mode (See Table 7)
1	X	X	X	0	0	X	RS485 Full Duplex Mode
1	X	X	X	1	0	X	RS485 Half Duplex Mode
1	0	X	X	X	1	ON	RS485 Loopback Mode
0	0	X	X	X	1	ON	RS232 Loopback Mode

Table 3. RS232 Receiver Mode for a Given Port (485/$\overline{232}$ = 0)

$\overline{RXEN}$	RECEIVER INPUT (A, B)	CONDITIONS	RECEIVER OUTPUTS (RA, RB)	RECEIVER INPUTS (A, B)
1	X	No Fault	Hi-Z	125kΩ
0	0	No Fault	1	5kΩ
0	1	No Fault	0	5kΩ
0	X	Thermal Fault	Hi-Z	5kΩ

Table 4. RS232 Driver Mode for a Given Port (485/$\overline{232}$ = 0)

DXENX	DRIVER INPUT (DY, DZ)	CONDITIONS	DRIVER OUTPUT (Y, Z)
0	X	No Fault	125kΩ
1	0	No Fault	1
1	1	No Fault	0
X	X	Thermal Fault	125kΩ

FUNCTION TABLES

Table 5. RS485 Driver Mode for a Given Port (485/$\overline{232}$ = 1, TE485 = 0)

DXEN	DY	CONDITIONS	Y	Z
0	X	No Fault	125kΩ	125kΩ
1	0	No Fault	0	1
1	1	No Fault	1	0
X	X	Thermal Fault	125kΩ	125kΩ

Table 6. RS485 Receiver Mode for a Given Port (485/$\overline{232}$ = 1, LB = 0)

$\overline{RXEN}$	A–B (NOTE 5)	CONDITIONS	RA
1	X	No Fault	Hi-Z
0	< –200mV	No Fault	0
0	> 200mV	No Fault	1
0	Inputs Open or Shorted Together (DC)	No Fault	1
X	X	Thermal Fault	Hi-Z

Table 7. RS485 Termination for a Given Port (485/$\overline{232}$ = 1)

TE485	DZ	H/$\overline{F}$, LB	CONDITIONS	R(A TO B)	R(Y TO Z)
0	X	X	No Fault	Hi-Z	Hi-Z
1	0	X	No Fault	120Ω	Hi-Z
1	1	X	No Fault	120Ω	120Ω
X	X	X	Thermal Fault	Hi-Z	Hi-Z

Table 8. RS485 Duplex Control for Given Port (485/$\overline{232}$ = 1)

H/$\overline{F}$	RS485 DRIVER OUTPUTS	RS485 RECEIVER INPUTS
0	Y, Z	A, B
1	Y, Z	Y, Z

Table 9. Loopback Functions for a Given Port

LB	$\overline{RXEN}$	TRANSCEIVER MODE
0	X	Not Loopback
1	1	Not Loopback
1	0	Loopback (RA = DY, RB = DZ)

APPLICATIONS INFORMATION

Overview

The LTC2872 is a flexible multiprotocol transceiver supporting RS485/RS422 and RS232 protocols. It can be powered from a single 3.0V to 5.5V supply with optional logic interface supply as low as 1.7V. An integrated DC/DC converter provides the positive and negative supply rails needed for RS232 operation. Automatically selected integrated termination resistors for both RS232 and RS485 protocols are included, eliminating the need for external components and switching relays. Both parts include loopback control for self-test and debug as well as logically-switchable half- and full-duplex control of the RS485 bus interface.

The LTC2872 offers two ports that can be independently configured as either two RS232 receivers and drivers or one RS485/RS422 receiver and driver depending on the state of its 485/$\overline{232}$ pins. Control inputs DXEN and $\overline{RXEN}$ provide independent control of driver and receiver operation for either RS232 or RS485 transceivers, depending on the selected operating protocol.

The LTC2872 features rugged operation with an ESD rating of ±15kV HBM on the receiver inputs and driver outputs, both powered and unpowered. All other pins offer protection exceeding ±4kV.

DC/DC Converter

The on-chip DC/DC converter operates from the V_{CC} input, generating a 7V V_{DD} supply and a charge pumped –6.3V V_{EE} supply, as shown in Figure 13. V_{DD} and V_{EE} power the output stage of the RS232 drivers and are regulated to levels that guarantee greater than ±5V output swing. The DC/DC converter requires a 22µH inductor (L1) and a bypass capacitor (C4) of 2.2µF or larger. The charge pump capacitor (C1) is 470nF and the storage capacitors (C2 and C3) are 2.2µF. Larger storage capacitors up to 4.7µF may be used if C1 and C4 are scaled proportionately. Locate C1-C4 close to their associated pins.

Bypass capacitor C5 on the logic supply pin can be omitted if V_L is connected to V_{CC}. See the V_L Logic Supply section for more details about the V_L logic supply.

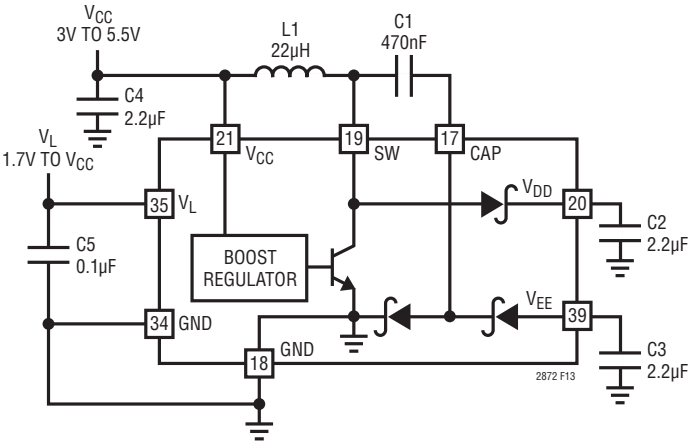


Figure 13. DC/DC Converter with Required External Components

Inductor Selection

An inductor with a value of 22µH ±20% is required. It must have a saturation current (I_{SAT}) rating of at least 200mA and a DCR (copper wire resistance) of less than 1.3Ω. Some small inductors meeting these requirements are listed in Table 10.

Table 10. Recommended Inductors

PART NUMBER	L (µH)	I_{SAT} (mA)	MAX DCR (Ω)	SIZE (mm)	MANUFACTURER
BRC2016T220M CBC2518T220M	22 22	310 320	1.3 1.0	2 × 1.6 × 1.6 2.5 × 1.8 × 1.8	Taiyo Yuden t-yuden.com
LQH32CN220K53	22	250	0.92	3.2 × 2.5 × 1.6	Murata murata.com

Capacitor Selection

The small size of ceramic capacitors makes them ideal for the LTC2872. Use X5R or X7R dielectric types; their ESR is low and they retain their capacitance over relatively wide voltage and temperature ranges. Use a voltage rating of at least 10V.

APPLICATIONS INFORMATION

Inrush Current and Supply Overshoot Precaution

In certain applications fast supply slew rates are generated when power is connected. If V_{CC}'s voltage is greater than 4.5V and its rise time is faster than 10µs, the pins V_{DD} and SW can exceed their Absolute Maximum values during start-up. When supply voltage is applied to V_{CC}, the voltage difference between V_{CC} and V_{DD} generates inrush current flowing through inductor L1 and capacitors C1 and C2. The peak inrush current must not exceed 2A. To avoid this condition, add a 1Ω resistor as shown in Figure 14. This precaution is not relevant for supply voltages below 4.5V or rise times longer than 10µs.

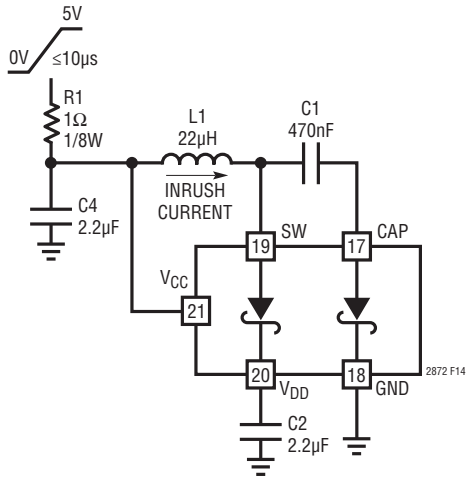


Figure 14. Supply Current Overshoot Protection for Input Supplies of 4.5V of Higher

V_L Logic Supply

A separate logic supply pin V_L allows the LTC2872 to interface with any logic signal from 1.7V to 5.5V. All logic I/Os use V_L as their high supply. For proper operation, V_L should not be greater than V_{CC}. During power-up, if V_L is higher than V_{CC}, the device will not be damaged, but behavior of the device is not guaranteed. If V_L is not connected to V_{CC}, bypass V_L with a 0.1µF capacitor.

RS232 and RS485 driver outputs are undriven and the RS485 termination resistors are disabled when V_L or V_{CC} is grounded or V_{CC} is disconnected.

Although all logic input pins reference V_L as their high supply, they can be driven up to 7V, independent of V_L and V_{CC}, with the exception of FEN, which must not exceed V_L by more than 1V for proper operation. Logic input pins do not have internal biasing devices to pull them up or down. They must be driven high or low to establish valid logic levels; do not float.

RS485 Driver

The RS485 driver provides full RS485/RS422 compatibility. When enabled, if DI is high, Y–Z is positive. When the driver is disabled, Y and Z output resistance is greater than 96k (typically 125k) to ground over the entire common mode range of –7V to 12V. This resistance is equivalent to the input resistance on these lines when the driver is configured in half-duplex mode and Y and Z act as the RS485 receiver inputs.

Driver Overvoltage and Overcurrent Protection

The RS232 and RS485 driver outputs are protected from short circuits to any voltage within the Absolute Maximum range ±15V. The maximum current in this condition is 90mA for the RS232 driver and 250mA for the RS485 driver.

If an RS485 driver output is shorted to a voltage greater than V_{CC}, when active high, positive current of about 100mA can flow from the driver output back to V_{CC}. If the system power supply or loading cannot sink this excess current, clamp V_{CC} to GND with a Zener diode (e.g., 5.6V, 1W, 1N4734) to prevent an overvoltage condition on V_{CC}.

All devices also feature thermal shutdown protection that disables the drivers, receivers, and RS485 terminators in case of excessive power dissipation (see Note 6).

RS485 Balanced Receiver with Full Failsafe Support

The LTC2872 RS485 receiver has a differential threshold voltage that is about 80mV for signals that are rising and –80mV for signals that are falling, as illustrated in Figure 15. If a differential input signal lingers in the window between these thresholds for more than about 2µs, the rising threshold changes from 80mV to –50mV, while the falling threshold remains at –80mV. Thus, differential inputs that are shorted, open, or terminated but not driven for more than 2µs produce a high on the receiver output, indicating a failsafe condition.

APPLICATIONS INFORMATION

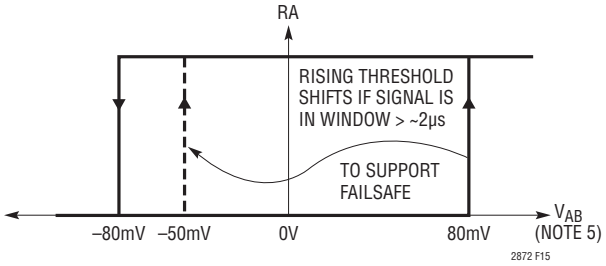


Figure 15. RS485 Receiver Input Threshold Characteristics with Typical Values Shown

The benefit of this dual threshold architecture is that it supports full failsafe operation yet offers a balanced threshold, centered on 0V, for normal data signals. This balance preserves duty cycle for small input signals with heavily slewed edges, typical of what might be seen at the end of a very long cable. This performance is highlighted in Figure 16, where a signal is driven through 4000 feet of CAT5e cable at 3Mbps. Even though the differential signal peaks at just over 100mV and is heavily slewed, the output maintains a nearly perfect signal with almost no duty cycle distortion.

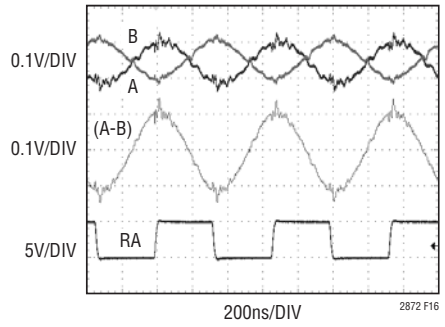


Figure 16. A 3Mbps Signal Driven Down 4000ft of CAT5e Cable. Top Traces: Received Signals After Transmission Through Cable; Middle Trace: Math Showing Differences of Top Two Signals; Bottom Trace: Receiver Output

An additional benefit of the balanced architecture is excellent noise immunity due to the wide effective differential input signal hysteresis of 160mV for signals transitioning through the window region in less than 2µs. Increasingly slower signals will have increasingly less effective hysteresis, limited by the DC failsafe hysteresis of about 30mV.

RS485 Biasing Network Not Required

RS485 networks are often biased with a resistive divider to generate a differential voltage of ≥200mV on the data lines, which establishes a logic-high state when all the transmitters on the network are disabled. The values of the biasing resistors depend on the number and type of transceivers on the line and the number and value of terminating resistors. Therefore, the values of the biasing resistors must be customized to each specific network installation, and may change if nodes are added to or removed from the network.

The internal failsafe feature of the LTC2872 eliminates the need for external network biasing resistors provided they are used in a network of transceivers with similar internal failsafe features. This also allows the network to support a high number of nodes, up to 256, by eliminating the bias resistor loading. The LTC2872 transceivers will operate correctly on biased, unbiased, or under-biased networks.

Receiver Outputs

The RS232 and RS485 receiver outputs are internally driven high (to V_L) or low (to GND) with no external pull-up needed. When the receivers are disabled, the output pin becomes Hi-Z with leakage of less than ±5µA for voltages within the V_L supply range.

RS485 Receiver Input Resistance

The RS485 receiver input resistance from A or B to GND (Y or Z to GND in half-duplex mode with driver disabled) is greater than 96k (typically 125k) when the integrated termination is disabled. This permits up to a total of 256 receivers per system without exceeding the RS485 receiver loading specification. The input resistance of the receiver is unaffected by enabling/disabling the receiver or whether the part is in half-duplex, full-duplex, loopback mode, or even unpowered. The equivalent input resistance looking into the RS485 receiver pins is shown in Figure 17.

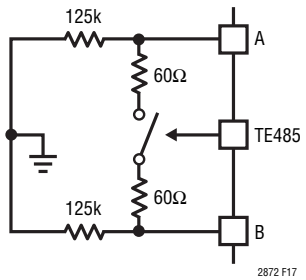


Figure 17. Equivalent RS485 Receiver Input Resistance Into A and B (Note 5)

APPLICATIONS INFORMATION

Selectable RS485 Termination

Proper cable termination is important for good signal fidelity. When the cable is not terminated with its characteristic impedance, reflections cause waveform distortion.

The LTC2872 offers integrated switchable 120Ω termination resistors between the differential receiver inputs and also between the differential driver outputs. This provides the advantage of being able to easily change, through logic control, the proper line termination for correct operation when configuring transceiver networks. Termination should be enabled on transceivers positioned at both ends of a network bus.

Termination on the driver nodes is important for cases where the driver is disabled but there is communication on the connecting bus from another node. Driver termination across Y and Z can be disabled independently from the termination across A and B by setting DZ low. See Table 7 for details.

The termination resistance is maintained over the entire RS485 common mode range of –7V to 12V as shown in Figure 18. The voltage across pins with the terminating resistor enabled should not exceed 6V as indicated in the Absolute Maximum Ratings table.

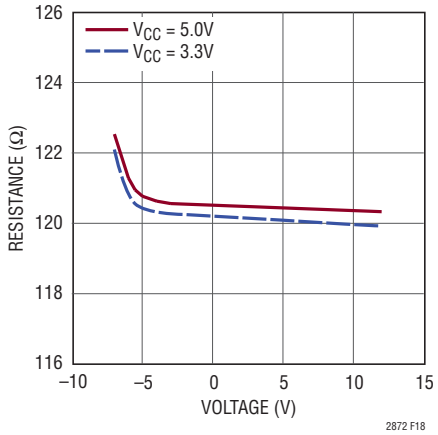


Figure 18. Typical Resistance of the Enabled RS485 Terminator vs Common Mode Voltage of A and B

RS485 Half- and Full-Duplex Control

The LTC2872 is equipped with a control to change the RS485 transceiver operation from full-duplex to half-duplex. With the H/$\overline{F}$ pin set to a logic-low, the A and B pins serve as the differential receiver inputs. With the H/$\overline{F}$ pin set to a logic-high, the Y and Z pins serve as the differential inputs. In either configuration, the RS485 driver outputs are always on Y and Z. The impedance looking into the A and B pins is not affected by H/$\overline{F}$ control, including the differential termination resistance. The H/$\overline{F}$ control does not affect RS232 operation.

Logic Loopback

A loopback mode connects the driver inputs to the receiver outputs (noninverting) for self test. This applies to both RS232 and RS485 transceivers. Loopback mode is entered when the LB pin is set to a logic-high and the relevant receiver is enabled.

In loopback mode, the drivers function normally. They can be disabled with output in a Hi-Z state or left enabled to allow loopback testing in normal operation. Loopback works in half- or full-duplex modes and does not affect the termination resistors.

RS485 Cable Length vs Data Rate

Many factors contribute to the maximum cable length that can be used for for RS485 or RS422 communication, including driver transition times, receiver threshold, duty cycle distortion, cable properties and data rate. A typical curve of cable length versus maximum data rate is shown in Figure 19. Various regions of this curve reflect different performance limiting factors in data transmission.

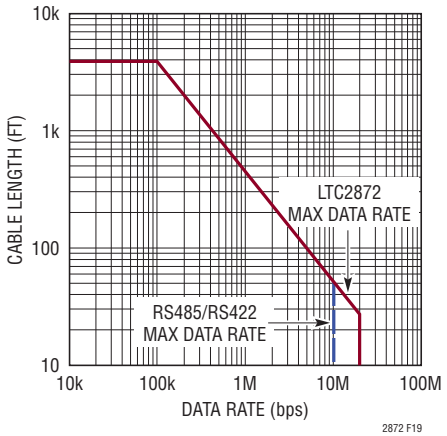


Figure 19. Cable Length vs Data Rate (RS485/RS422 Standard Shown in Vertical Solid Line)

APPLICATIONS INFORMATION

At frequencies below 100kbps, the maximum cable length is determined by DC resistance in the cable. In this example, a cable longer than 4000ft will attenuate the signal at the far end to less than what can be reliably detected by the receiver.

For data rates above 100kbps, the capacitive and inductive properties of the cable begin to dominate this relationship. The attenuation of the cable is frequency and length dependent, resulting in increased rise and fall times at the far end of the cable. At high data rates or long cable lengths, these transition times become a significant part of the signal bit time. Jitter and intersymbol interference aggravate this so that the time window for capturing valid data at the receiver becomes impossibly small.

The boundary at 20Mbps in Figure 19 represents the guaranteed maximum operating rate of the LTC2872. The dashed vertical line at 10Mbps represents the specified maximum data rate in the RS485 standard. This boundary is not a limit, but reflects the maximum data rate that the specification was written for.

It should be emphasized that the plot in Figure 19 shows a typical relation between maximum data rate and cable length. Results with the LTC2872 will vary, depending on cable properties such as conductor gauge, characteristic impedance, insulation material, and solid versus stranded conductors.

Layout Considerations

All V_{CC} pins must be connected together and all ground pins must be connected together on the PC board with very low impedance traces or dedicated planes. A 2.2µF, or larger, bypass capacitor should be placed less than 0.7cm away from V_{CC} Pin 21. This V_{CC} pin, as well as GND Pin 18, mainly service the DC/DC converter. Additional bypass capacitors of 0.1µF or larger, can be added to V_{CC} Pins 1 and 31 if the traces back to the 2.2µF capacitor are indirect or narrow. These V_{CC} pins mainly service the transceivers #1 and #2, respectively. Table 11 summarizes the bypass capacitor requirements. The capacitors listed in the table should be placed closest to their respective supply and ground pin.

Table 11. Bypass Capacitor Requirements

CAPACITOR	SUPPLY (PIN)	RETURN (PIN)	COMMENT
2.2µF	V_{CC} (21)	GND (18)	Required
2.2 µF	V_{DD} (20)	GND (18)	Required
2.2uF	V_{EE} (39)	GND (18)	Required
0.1µF	V_L (35)	GND (34)	Required*
0.1µF	V_{CC} (1)	GND (5)	Optional
0.1µF	V_{CC} (31)	GND (27)	Optional

* If V_L is not connected to V_{CC}.

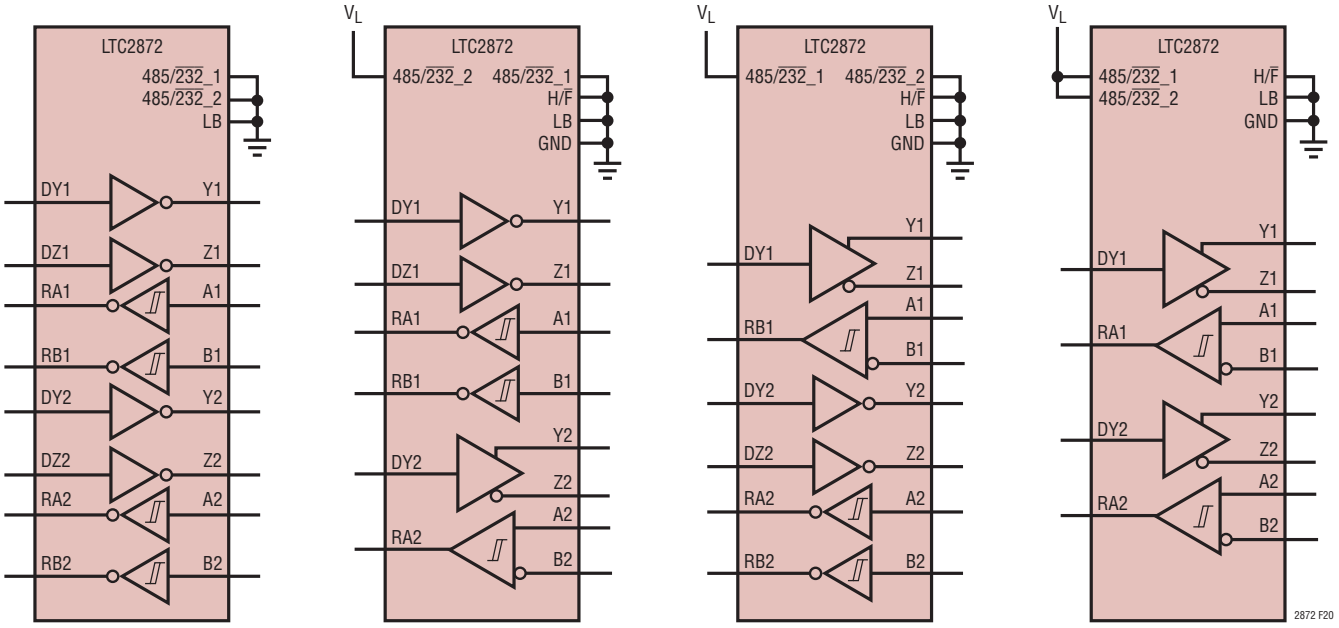
Place the charge pump capacitor, C1, directly adjacent to the SW and CAP pins, with no more than one centimeter of total trace length to maintain low inductance. Close placement of the inductor, L1, is of secondary importance compared to the placement of C1 but should include no more than two centimeters of total trace length.

The PC board traces connected to high speed signals A/B and Y/Z should be symmetrical and as short as possible to minimize capacitive imbalance and to maintain good differential signal integrity. To minimize capacitive loading effects, the differential signals should be separated by more than the width of a trace and should not be routed on top of each other if they are on different signal planes.

Care should be taken to route outputs away from any sensitive inputs to reduce feedback effects that might cause noise, jitter, or even oscillations. For example, DI and A/B should not be routed near the driver or receiver outputs.

TYPICAL APPLICATIONS

V_{CC} = 3V to 5.5V, V_L = 1.7V to V_{CC}. Logic input pins not shown are tied to a valid logic state. External components necessary for operation are not shown.



PORT 1: RS232
PORT 2: RS232

PORT 1: RS232
PORT 2: RS485

PORT 1: RS485
PORT 2: RS232

PORT 1: RS485
PORT 2: RS485

Figure 20. LTC2872 in Various Basic Port Configurations

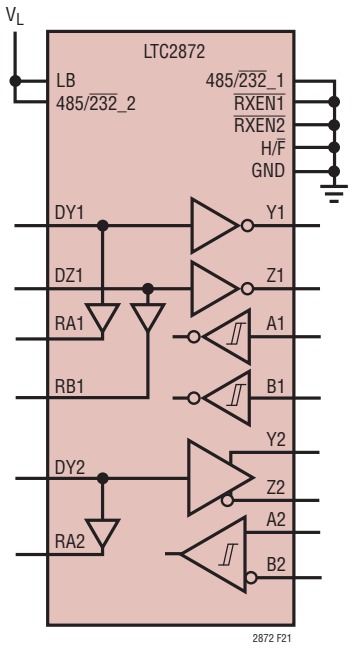


Figure 21. Loopback in RS232 and RS485 Modes

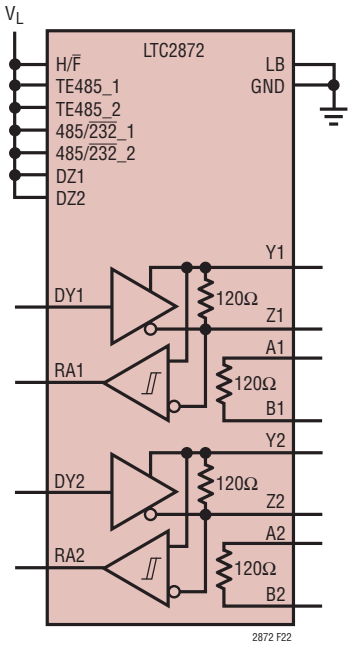


Figure 22. Half-Duplex RS485 Mode with Driver and Receiver Line Termination on Each Port

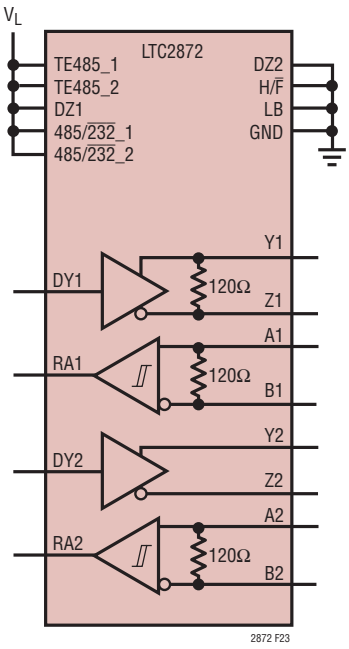


Figure 23. Full-Duplex RS485 Mode with Driver and Receiver Line Termination on Port 1, and Receiver-Only Termination on Port 2

TYPICAL APPLICATIONS

V_{CC} = 3V to 5.5V, V_L = 1.7V to V_{CC}. Logic input pins not shown are tied to a valid logic state. External components necessary for operation are not shown.

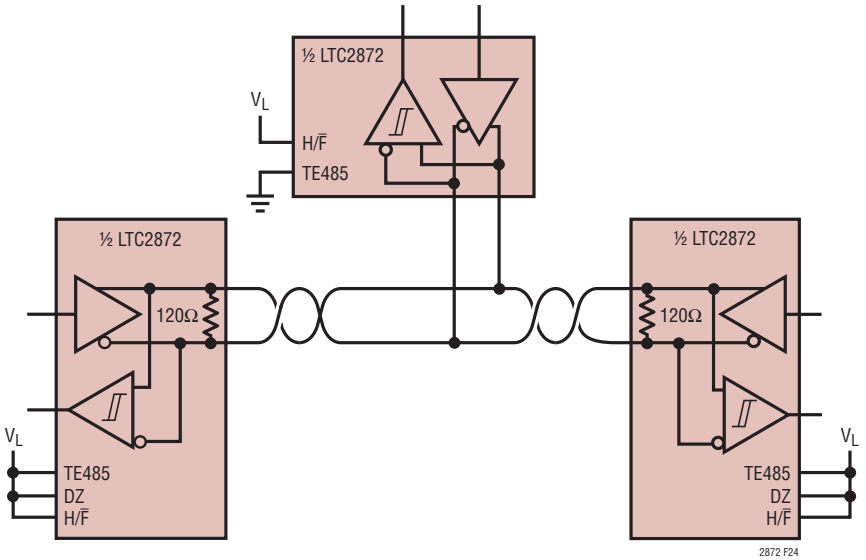


Figure 24. Typical RS485 Half Duplex Network

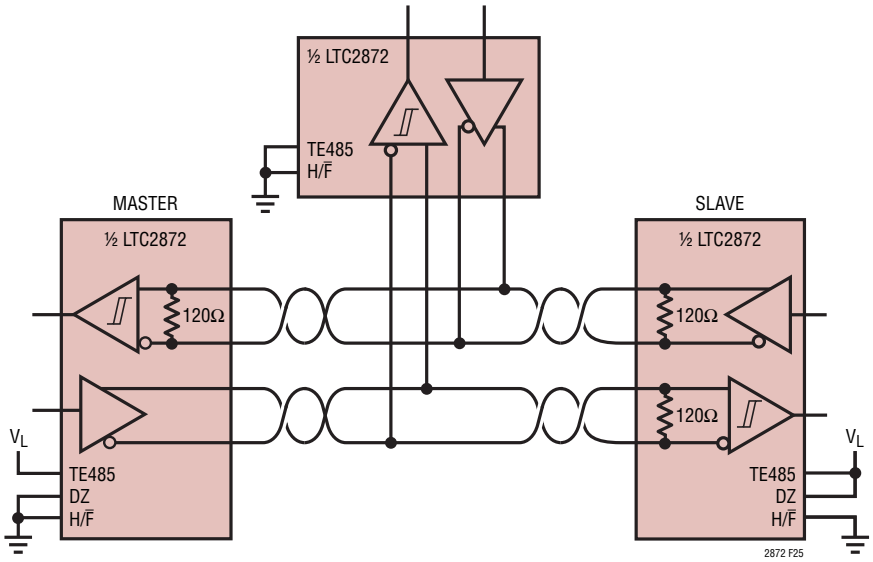
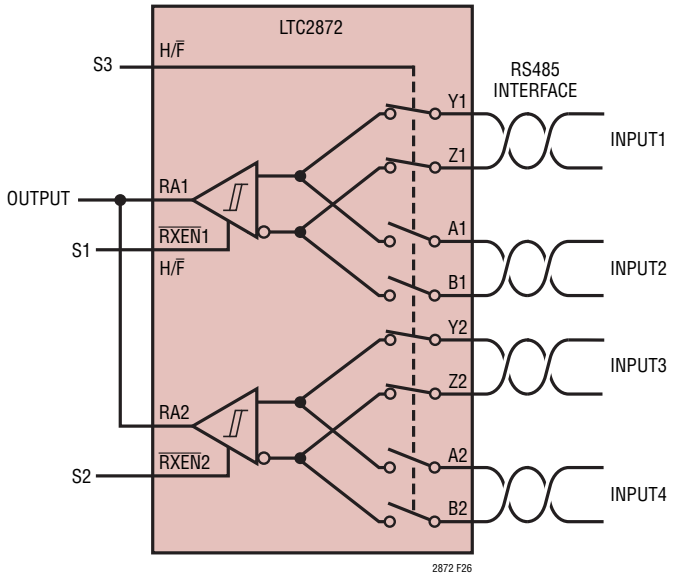


Figure 25. Typical RS485 Full Duplex Network

TYPICAL APPLICATIONS

V_{CC} = 3V to 5.5V, V_L = 1.7V to V_{CC}. Logic input pins not shown are tied to a valid logic state. External components necessary for operation are not shown.

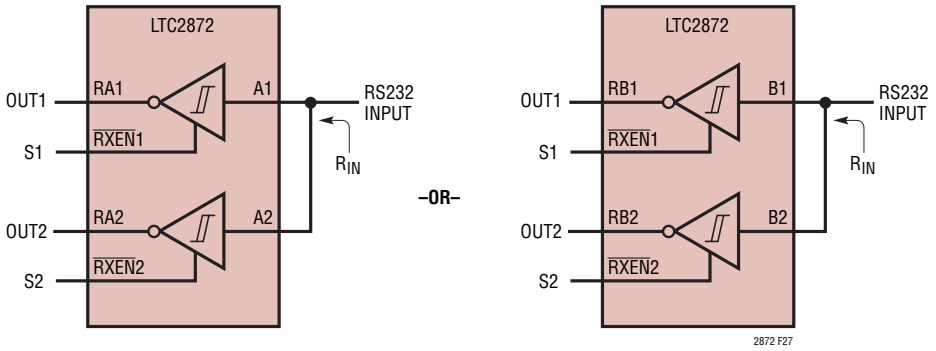


S1	S2	S3	SELECTED INPUT
0	1	1	INPUT1
0	1	0	INPUT2
1	0	1	INPUT3
1	0	0	INPUT4
1	1	X	NONE/Hi-Z
0	0	X	INVALID

Figure 26. RS485 Receiver with 4-Way Selectable Inputs

TYPICAL APPLICATIONS

V_{CC} = 3V to 5.5V, V_L = 1.7V to V_{CC}. Logic input pins not shown are tied to a valid logic state. External components necessary for operation are not shown.



S1	S2	R_{IN}	ACTIVE OUTPUT
0	1	5k	OUT1
1	0	5k	OUT2
1	1	62.5k	NONE (Hi-Z)
0	0	2.5k*	OUT1, OUT2

* DOES NOT MEET RS232 SPECIFICATIONS

Figure 27. Sharing RS232 Receiver Inputs

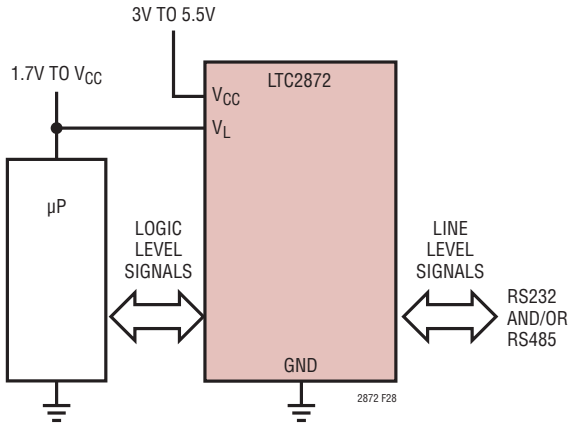


Figure 28. Low Voltage Microprocessor Interface

TYPICAL APPLICATIONS

V_{CC} = 3V to 5.5V, V_L = 1.7V to V_{CC}. Logic input pins not shown are tied to a valid logic state. External components necessary for operation are not shown.

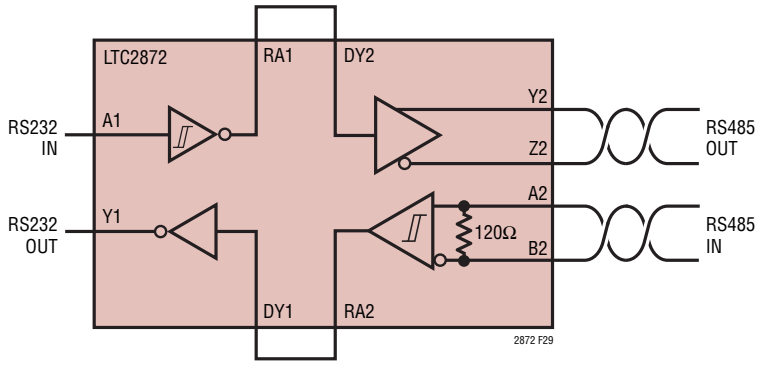


Figure 29. RS232 ↔ RS485 Conversion

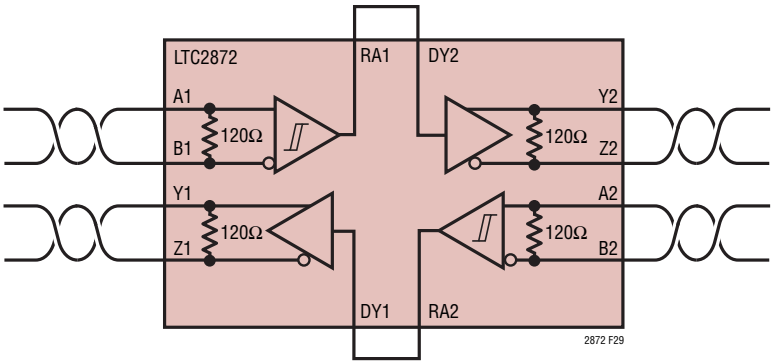
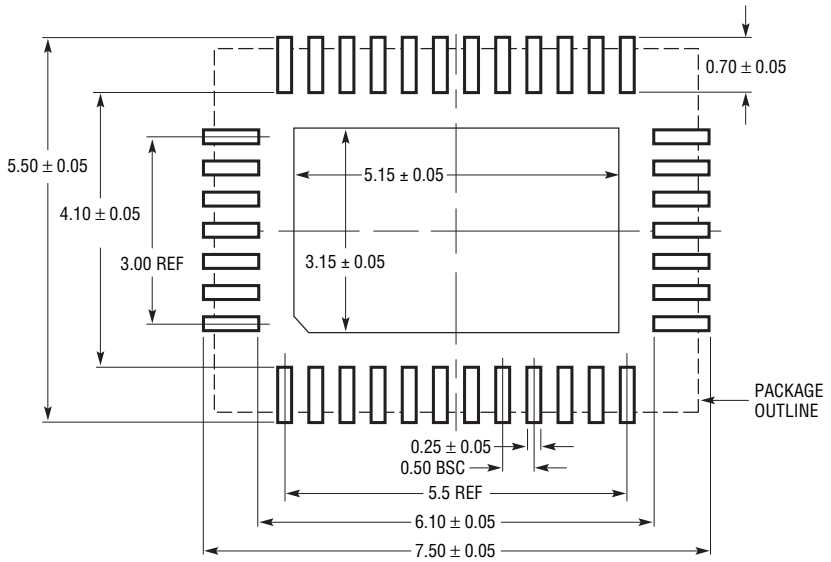


Figure 30. RS485 Repeater

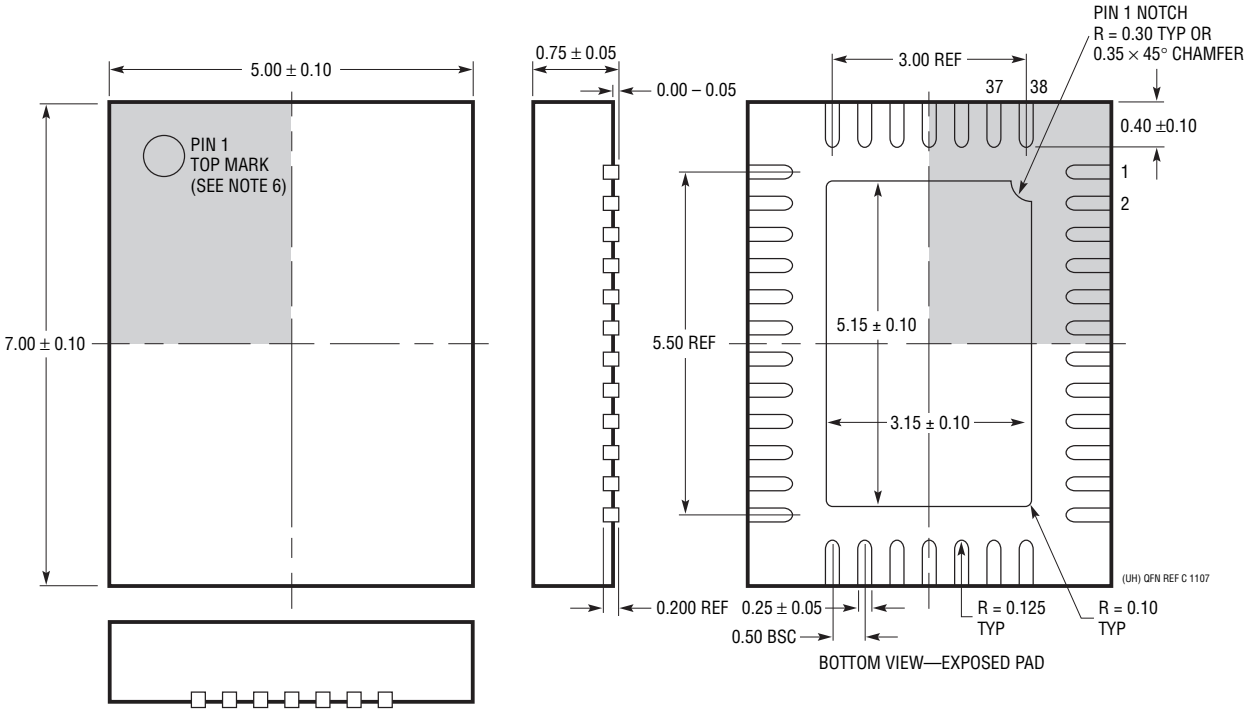
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

UHF Package
38-Lead Plastic QFN (5mm × 7mm)
(Reference LTC DWG # 05-08-1701 Rev C)



RECOMMENDED SOLDER PAD LAYOUT
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING CONFORMS TO JEDEC PACKAGE OUTLINE M0-220 VARIATION WHKD
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

TYPICAL APPLICATION

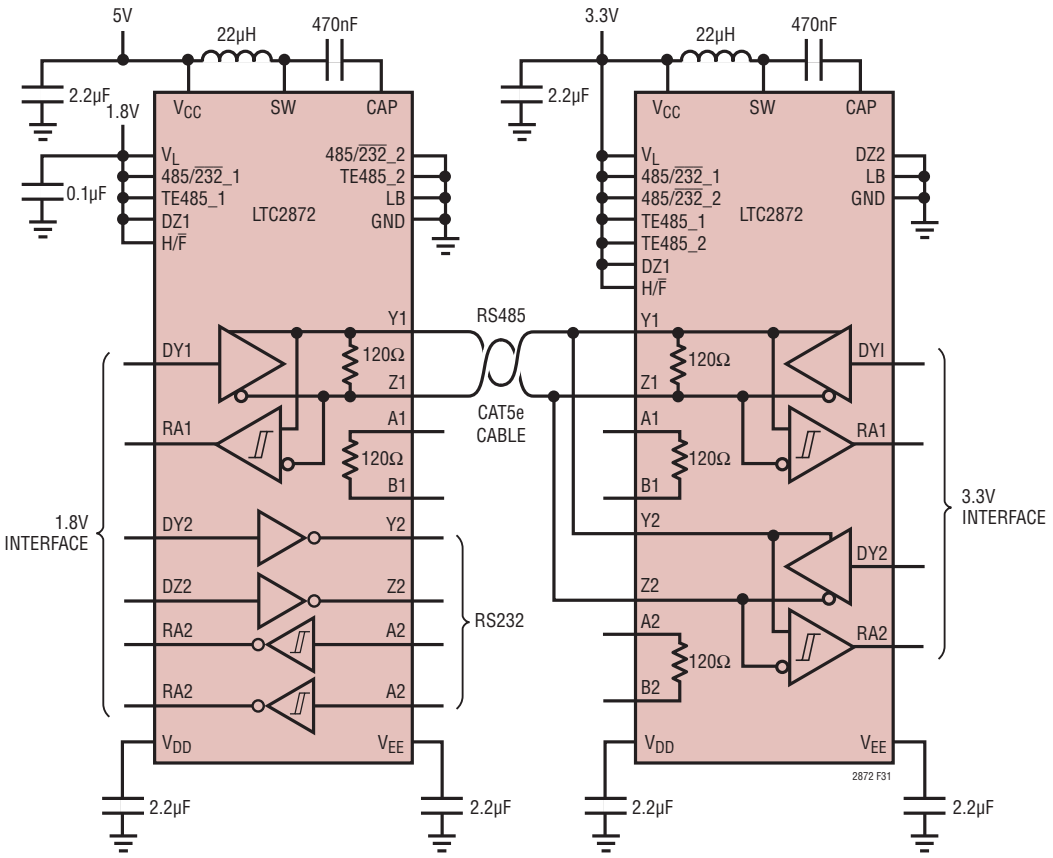


Figure 31. LTC2872 on Left: RS485 Half-Duplex and Terminated, Plus RS232. LTC2872 on Right: Dual RS485 Half-Duplex and Terminated. All External Components Shown

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC2870/LTC2871	RS232/RS485 Multiprotocol Transceivers with Integrated Termination	3V to 5.5V Supply, Automatic Selection of Termination Resistors, Duplex Control, Logic Supply Pin, ±26kV ESD
LTC1334	Single 5V RS232/RS485 Multiprotocol Transceiver	Dual Port, Single 5V Supply, Configurable, ±10kV ESD
LTC1387	Single 5V RS232/RS485 Multiprotocol Transceiver	Single Port, Configurable
LTC2801/LTC2802/ LTC2803/LTC2804	1.8V to 5.5V RS232 Single and Dual Transceivers	Up to 1Mbps, ±10kV ESD, Logic Supply Pin, Tiny DFN Packages
LTC2854/LTC2855	3.3V 20Mbps RS485 Transceiver with Integrated Switchable Termination	3.3V Supply, Integrated, Switchable, 120Ω Termination Resistor, ±25kV ESD
LTC2859/LTC2861	20Mbps RS485 Transceiver with Integrated Switchable Termination	5V Supply, Integrated, Switchable, 120Ω Termination Resistor, ±15kV ESD
LTM2881	Complete Isolated RS485/RS422 µModule® Transceiver + Power	20Mbps, 2500V_{RMS} Isolation with Integrated DC/DC Converter, Integrated Switchable 120Ω Termination Resistor, ±15kV ESD
LTM2882	Dual Isolated RS232 µModule Transceiver + Power	1Mbps, 2500V_{RMS} Isolation with Integrated DC/DC Converter, ±10kV ESD

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