14-Bit, 4.5Msps Serial Sampling ADC in TSOT

FEATURES

- **4.5Msps Throughput Rate**
- **Guaranteed 14-Bit No Missing Codes**
- **Internal Reference: 2.048V/4.096V Span**
- **Low Noise: 77.5dB SNR**
- **Low Power: 6.2mA at 4.5Msps and 5V**
- **Dual Supply Range: 3V/5V operation**
- Sleep Mode with < 1µA Typical Supply Current
- Nap Mode with Quick Wake-up < 1 conversion
- Separate 1.8V to 5V Digital I/O Supply
- High Speed SPI-Compatible Serial I/O
- Guaranteed Operation from –40°C to 125°C
- 8-Lead TSOT-23 Package

APPLICATIONS

- Communication Systems
- High Speed Data Acquisition
- Handheld Terminal Interface
- Medical Imaging
- Uninterrupted Power Supplies
- Battery Operated Systems
- Automotive

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DESCRIPTION

The LTC®2314-14 is a 14-bit, 4.5Msps, serial sampling A/D converter that draws only 6.2mA from a wide range analog supply adjustable from 2.7V to 5.25V. The LTC2314-14 contains an integrated bandgap and reference buffer which provide a low cost, high performance (20ppm/°C max) and space saving applications solution. The LTC2314-14 achieves outstanding AC performance of 77dB SINAD and –85dB THD while sampling a 500kHz input frequency. The extremely high sample rate-to-power ratio makes the LTC2314-14 ideal for compact, low power, high speed systems. The LTC2314-14 also provides both nap and sleep modes for further optimization of the device power within a system.

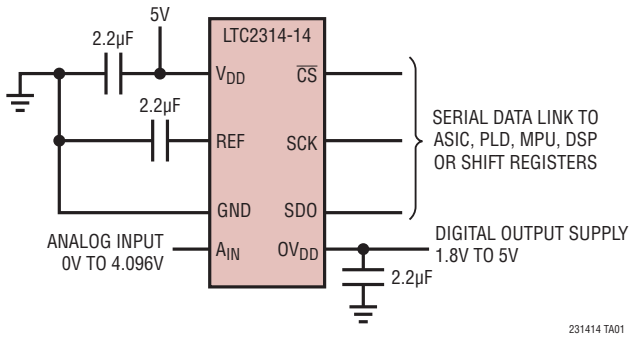
The LTC2314-14 has a high-speed SPI-compatible serial interface that supports 1.8V, 2.5V, 3V and 5V logic. The fast 4.5Msps throughput makes the LTC2314-14 ideally suited for a wide variety of high speed applications.

Complete 14-/12-Bit Pin-Compatible SAR ADC Family

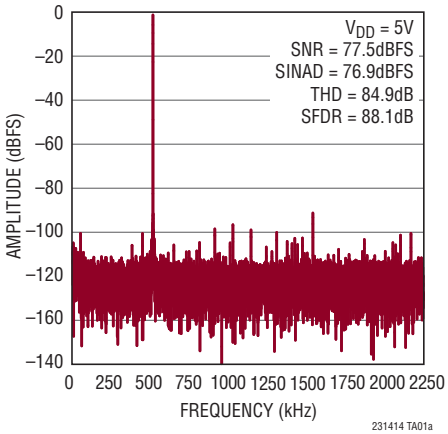
	500ksps	2.5Msps	4.5Msps	5Msps
14-Bit	LTC2312-14	LTC2313-14	LTC2314-14	
12-Bit	LTC2312-12	LTC2313-12		LTC2315-12
Power 3V/5V	9mW/15mW	14mW/25mW	18mW/31mW	19mW/32mW

TYPICAL APPLICATION

5V Supply, Internal Reference, 4.5Msps, 14-bit Sampling ADC



32k Point FFT, f_S = 4.5Msps, f_{IN} = 500kHz

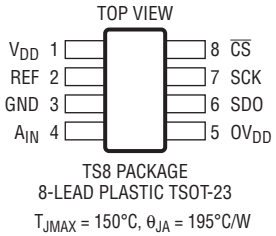


ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

Supply Voltage (V_{DD}, OV_{DD}) 6V
Reference (REF) and Analog Input (A_{IN}) Voltage
(Note 3).....(–0.3V) to (V_{DD} + 0.3V)
Digital Input Voltage (Note 3).. (–0.3V) to (OV_{DD} + 0.3V)
Digital Output Voltage..... (–0.3V) to (OV_{DD} + 0.3V)
Power Dissipation 100mW
Operating Temperature Range
LTC2314C ..... 0°C to 70°C
LTC2314I.....–40°C to 85°C
LTC2314H ..... –40°C to 125°C
Storage Temperature Range .....–65°C to 150°C
Lead Temperature Range (Soldering, 10 sec).....300°C

PIN CONFIGURATION



TS8 PACKAGE
8-LEAD PLASTIC TSOT-23

T_{JMAX} = 150°C, θ_{JA} = 195°C/W

ORDER INFORMATION

Lead Free Finish

TAPE AND REEL (MINI)	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC2314CTS8-14#TRMPBF	LTC2314CTS8-14#TRPBF	LTFZF	8-Lead Plastic TSOT-23	0°C to 70°C
LTC2314ITS8-14#TRMPBF	LTC2314ITS8-14#TRPBF	LTFZF	8-Lead Plastic TSOT-23	–40°C to 85°C
LTC2314HTS8-14#TRMPBF	LTC2314HTS8-14#TRPBF	LTFZF	8-Lead Plastic TSOT-23	–40°C to 125°C

TRM = 500 pieces. *Temperature grades are identified by a label on the shipping container.

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for information on lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{AIN}	Absolute Input Range		●	–0.05		V_{DD} + 0.05	V
V_{IN}	Input Voltage Range	(Note 11)		0		V_{REF}	V
I_{IN}	Analog Input DC Leakage Current		●	–1		1	µA
C_{IN}	Analog Input Capacitance	Sample Mode Hold Mode			13 3		pF pF

CONVERTER CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	Resolution		●	14			Bits
	No Missing Codes		●	14			Bits
	Transition Noise	(Note 6)			0.7		LSB_{RMS}
INL	Integral Linearity Error	V_{DD} = 5V (Note 5) V_{DD} = 3V (Note 5)	● ●	–3.75 –4.25	±1 ±1.5	3.75 4.25	LSB LSB
DNL	Differential Linearity Error	V_{DD} = 5V V_{DD} = 3V	● ●	–0.99 –0.99	±0.3 ±0.4	0.99 0.99	LSB LSB
	Offset Error	V_{DD} = 5V V_{DD} = 3V	● ●	–9 –22	±2 ±4	9 22	LSB LSB
	Full-Scale Error	V_{DD} = 5V V_{DD} = 3V	● ●	–18 –26	±5 ±7	18 26	LSB LSB
	Total Unadjusted Error	V_{DD} = 5V V_{DD} = 3V	● ●	–22 –30	±6 ±8	22 30	LSB LSB

DYNAMIC ACCURACY

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C and A_{IN} = –1dBFS. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
SINAD	Signal-to-(Noise + Distortion) Ratio	f_{IN} = 500kHz, V_{DD} = 5V f_{IN} = 500kHz, V_{DD} = 3V	● ●	72 69	77 72.6		dB dB
SNR	Signal-to-Noise Ratio	f_{IN} = 500kHz, V_{DD} = 5V f_{IN} = 500kHz, V_{DD} = 3V	● ●	73 69.5	77.5 73		dB dB
THD	Total Harmonic Distortion First 5 Harmonics	f_{IN} = 500kHz, V_{DD} = 5V f_{IN} = 500kHz, V_{DD} = 3V	● ●		–85 –85	–75 –74	dB dB
SFDR	Spurious Free Dynamic Range	f_{IN} = 500kHz, V_{DD} = 5V f_{IN} = 500kHz, V_{DD} = 3V	● ●		–87 –87	–77 –75	dB dB
IMD	Intermodulation Distortion 2nd Order Terms 3rd Order Terms	 f_{IN1} = 461kHz, f_{IN2} = 541kHz A_{IN1}, A_{IN2} = –7dBFS			 –79.4 –90.8		 dBc dBc
	Full Power Bandwidth	At 3dB At 0.1dB			130 20		MHz MHz
	–3dB Input Linear Bandwidth	SINAD ≥ 74dB			5		MHz
t_{AP}	Aperture Delay				1		ns
t_{JITTER}	Aperture Jitter				10		ps_{RMS}

REFERENCE INPUT/OUTPUT

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{REF}	V_{REF} Output Voltage	2.7V ≤ V_{DD} ≤ 3.6V 4.75 ≤ V_{DD} ≤ 5.25V	● ●	2.040 4.080	2.048 4.096	2.056 4.112	V V
	V_{REF} Temperature Coefficient		●		7	20	ppm/°C
	V_{REF} Output Resistance	Normal Operation Overdrive Condition (V_{REFIN} ≥ V_{REFOUT} + 50mV)			2 52		Ω kΩ
	V_{REF} Line Regulation	2.7V ≤ V_{DD} ≤ 3.6V 4.75 ≤ V_{DD} ≤ 5.25V			0.4 0.2		mV/V mV/V
	V_{REF} 2.048V/4.096V Supply Threshold				4.15		V
	V_{REF} 2.048V/4.096V Supply Threshold Hysteresis				150		mV
	V_{REF} Input Voltage Range (External Reference Input)	2.7V ≤ V_{DD} ≤ 3.6V 4.75 ≤ V_{DD} ≤ 5.25V	● ●	V_{REF} +50mV V_{REF} +50mV		V_{DD} 4.3	V V

DIGITAL INPUTS AND DIGITAL OUTPUTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage		●	0.8 • OV_{DD}			V
V_{IL}	Low Level Input Voltage		●			0.2 • OV_{DD}	V
I_{IN}	Digital Input Current	V_{IN} = 0V to OV_{DD}	●	–10		10	µA
C_{IN}	Digital Input Capacitance				5		pF
V_{OH}	High Level Output Voltage	I_O = –500µA (Source)	●	OV_{DD}–0.2			V
V_{OL}	Low Level Output Voltage	I_O = 500µA (Sink)	●			0.2	V
I_{OZ}	High-Z Output Leakage Current	V_{OUT} = 0V to OV_{DD}, $\overline{CS}$ = High	●	–10		10	µA
C_{OZ}	High-Z Output Capacitance	$\overline{CS}$ = High			4		pF
I_{SOURCE}	Output Source Current	V_{OUT} = 0V, OV_{DD} = 1.8V			–20		mA
I_{SINK}	Output Sink Current	V_{OUT} = OV_{DD} = 1.8V			20		mA

POWER REQUIREMENTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{DD}	Supply Voltage 3V Operational Range 5V Operational Range		 ● ●	 2.7 4.75	 3 5	 3.6 5.25	 V V
OV_{DD}	Digital Output Supply Voltage		●	1.71		5.25	V
I_{TOTAL} = I_{VDD} + I_{OVDD}	Supply Current, Static Mode Operational Mode Nap Mode Sleep Mode	$\overline{CS}$ = 0V, SCK = 0V	● ● ●		3.2 6.2 1.8 0.8	4 7.2 5	mA mA mA µA
P_D	Power Dissipation, Static Mode Operational Mode Nap Mode Sleep Mode	$\overline{CS}$ = 0V, SCK = 0V	● ● ●		16 31 9 4	20 36 25	mW mW mW µW

ADC TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$f_{SAMPLE(MAX)}$	Maximum Sampling Frequency	(Notes 7, 8)	●			4.5	MHz
f_{SCK}	Shift Clock Frequency	(Notes 7, 8)	●			87.5	MHz
t_{SCK}	Shift Clock Period		●	11.4			ns
$t_{THROUGHPUT}$	Minimum Throughput Time, $t_{ACQ} + t_{CONV}$		●			222	ns
t_{CONV}	Conversion Time		●	182			ns
t_{ACQ}	Acquisition Time		●	40			ns
t_1	Minimum $\overline{CS}$ Pulse Width	(Note 7)	●	10			ns
t_2	SCK↕ Setup Time After $\overline{CS}$↓	(Note 7)	●	5			ns
t_3	SDO Enable Time After $\overline{CS}$↓	(Notes 7, 8)	●			10	ns
t_4	SDO Data Valid Access Time after SCK↓	(Notes 7, 8, 9)	●			9.1	ns
t_5	SCLK Low Time		●	4.5			ns
t_6	SCLK High Time		●	4.5			ns
t_7	SDO Data Valid Hold Time After SCK↓	(Notes 7, 8, 9)	●	1			ns
t_8	SDO into Hi-Z State Time After 16th SCK↓	(Notes 7, 8, 10)	●	3		10	ns
t_9	SDO into Hi-Z State Time After $\overline{CS}$↑	(Notes 7, 8, 10)	●	3		10	ns
t_{10}	$\overline{CS}$↑ Setup Time After 14th SCK↓	(Note 7)	●	5			ns
	Latency		●		1 Cycle Latency		
t_{WAKE_NAP}	Power-Up Time from Nap Mode	See Nap Mode Section			50		ns
t_{WAKE_SLEEP}	Power-Up Time from Sleep Mode	See Sleep Mode Section			1.1		ms

Note 1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2. All voltage values are with respect to ground.

Note 3. When these pin voltages are taken below ground or above V_{DD} (A_{IN}, REF) or OV_{DD} (SCK, $\overline{CS}$, SDO) they will be clamped by internal diodes. This product can handle input currents up to 100mA below ground or above V_{DD} or OV_{DD} without latch-up.

Note 4. V_{DD} = 5V, OV_{DD} = 2.5V, f_{SMPL} = 4.5MHz, f_{SCK} = 87.5MHz, A_{IN} = –1dBFS and internal reference unless otherwise noted.

Note 5. Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

Note 6. Typical RMS noise at code transitions.

Note 7. Parameter tested and guaranteed at OV_{DD} = 2.5V. All input signals are specified with $t_r = t_f$ = 1nS (10% to 90% of OV_{DD}) and timed from a voltage level of $OV_{DD}/2$.

Note 8. All timing specifications given are with a 10pF capacitance load. Load capacitances greater than this will require a digital buffer.

Note 9. The time required for the output to cross the V_{IH} or V_{IL} voltage.

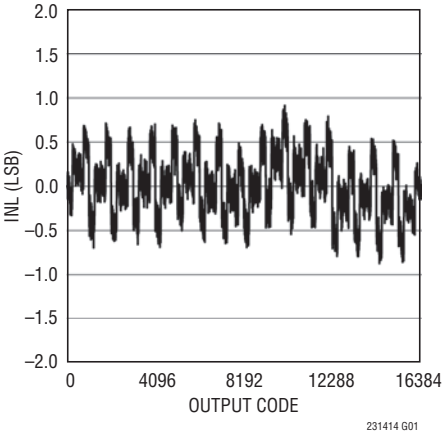
Note 10. Guaranteed by design, not subject to test.

Note 11. Recommended operating conditions.

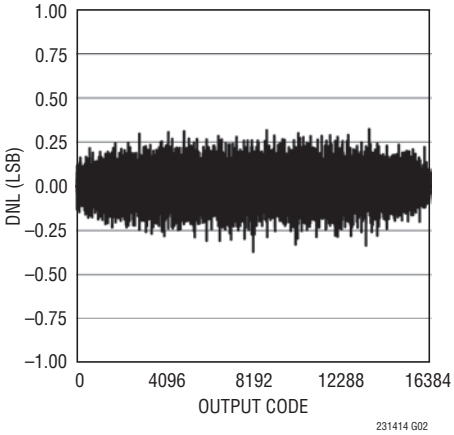
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{DD} = 5V, OV_{DD} = 2.5V, f_{SMPL} = 4.5Msps, unless otherwise noted.

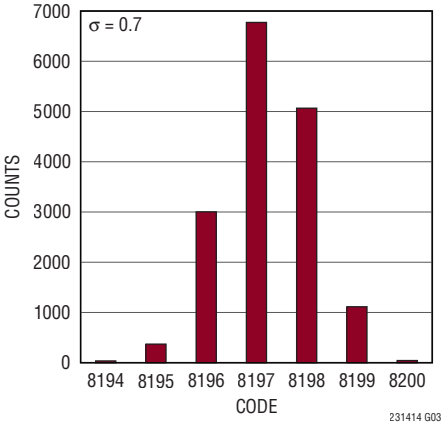
Integral Nonlinearity vs Output Code



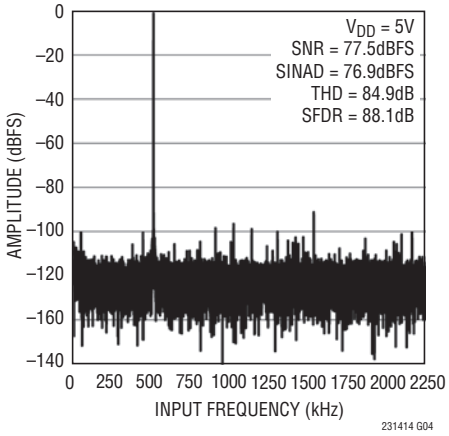
Differential Nonlinearity vs Output Code



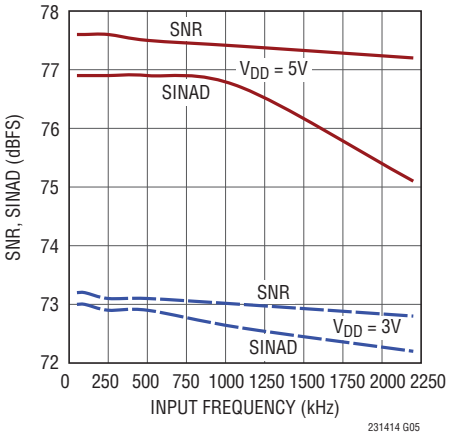
DC Histogram Near Mid-Scale (Code 8192)



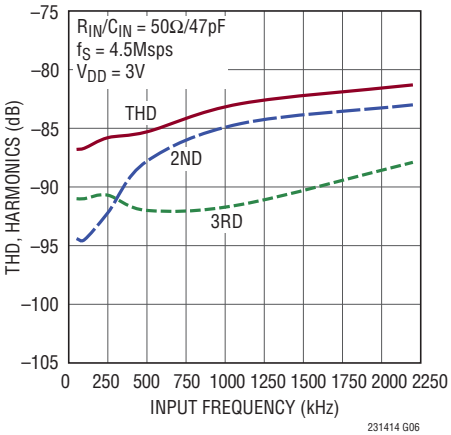
32k Point FFT, f_S = 4.5Msps f_{IN} = 500kHz



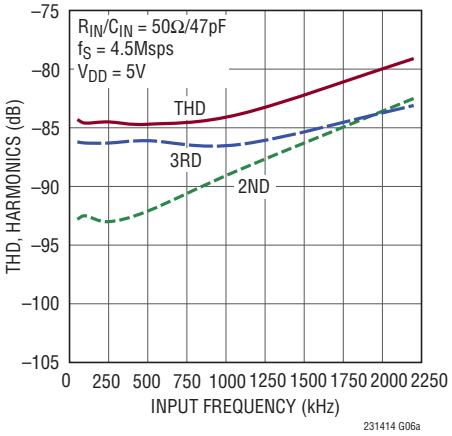
SNR, SINAD vs Input Frequency (100kHz to 2.2MHz)



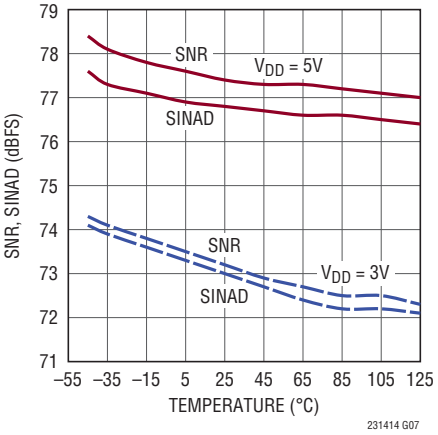
THD, Harmonics vs Input Frequency (100kHz to 2.2MHz)



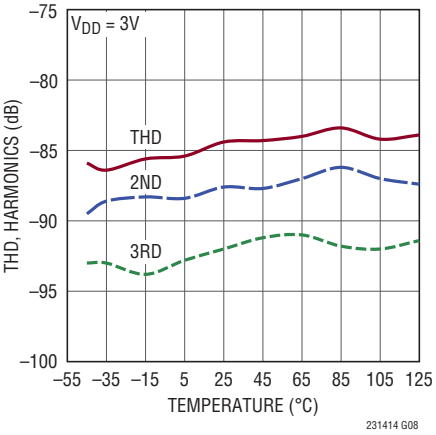
THD, Harmonics vs Input Frequency (100kHz to 2.2MHz)



SNR, SINAD vs Temperature, f_{IN} = 500kHz



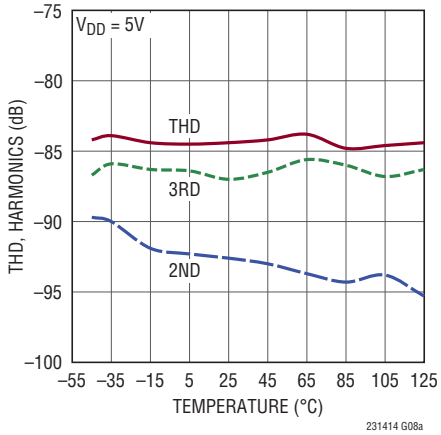
THD, Harmonics vs Temperature, f_{IN} = 500kHz



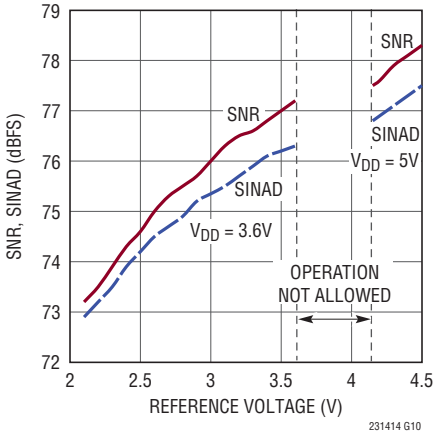
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{DD} = 5V, OV_{DD} = 2.5V, f_{SMPL} = 4.5Msps, unless otherwise noted.

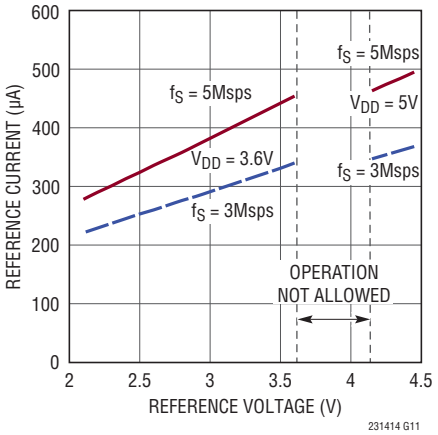
THD, Harmonics vs Temperature, f_{IN} = 500kHz



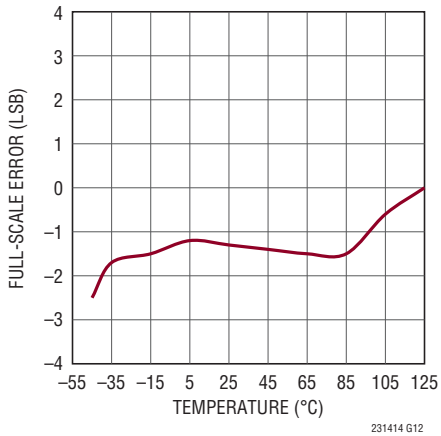
SNR, SINAD vs Reference Voltage f_{IN} = 500kHz



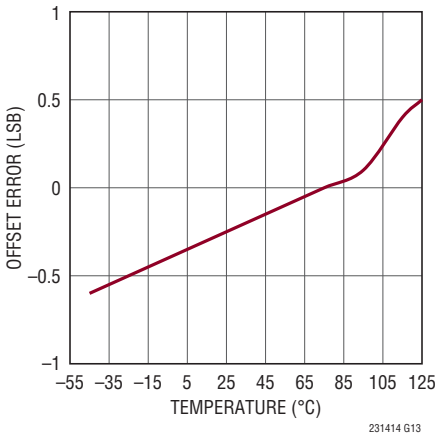
Reference Current vs Reference Voltage



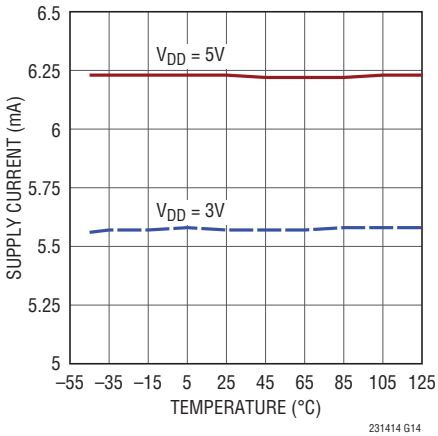
Full-Scale Error vs Temperature



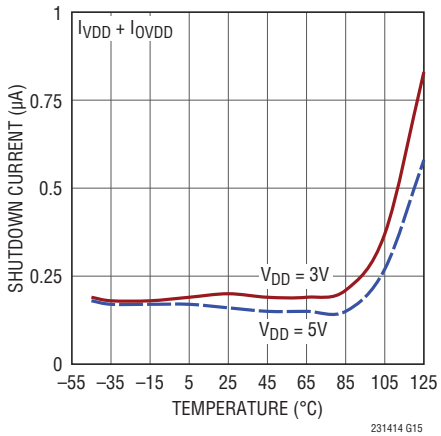
Offset Error vs Temperature



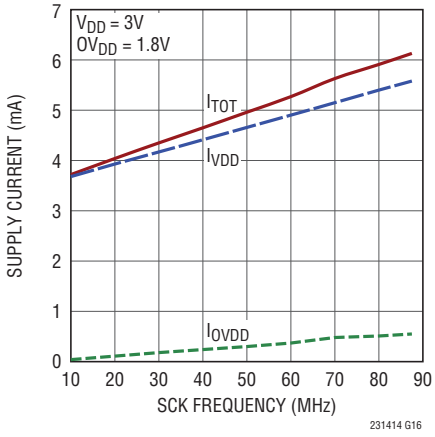
Supply Current vs Temperature



Shutdown Current vs Temperature



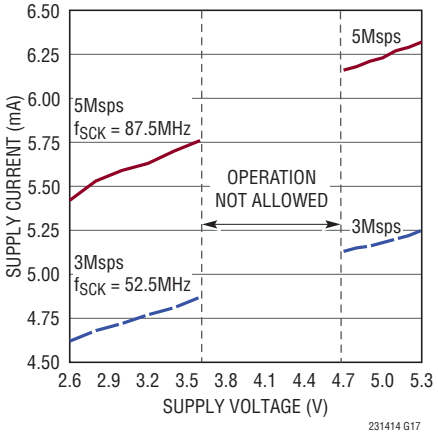
Supply Current vs SCK Frequency



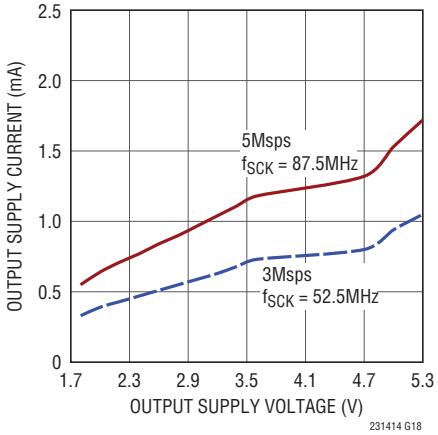
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{DD} = 5V, OV_{DD} = 2.5V, f_{SMPL} = 4.5Msps, unless otherwise noted.

Supply Current (I_{VDD}) vs Supply Voltage (V_{DD})



Output Supply Current (I_{OVDD}) vs Output Supply Voltage (OV_{DD})



PIN FUNCTIONS

V_{DD} (Pin 1): Power Supply. The ranges of V_{DD} are 2.7V to 3.6V and 4.75V to 5.25V. Bypass V_{DD} to GND with a 2.2µF ceramic chip capacitor.

REF (Pin 2): Reference Input/Output. The REF pin voltage defines the input span of the ADC, 0V to V_{REF}. By default, REF is an output pin and produces a reference voltage V_{REF} of either 2.048V or 4.096V depending on V_{DD} (see Table 2). Bypass to GND with a 2.2µF, low ESR, high quality ceramic chip capacitor. The REF pin may be overdriven with a voltage at least 50mV higher than the internal reference voltage output.

GND (Pin 3): Ground. The GND pin must be tied directly to a solid ground plane.

A_{IN} (Pin 4): Analog Input. A_{IN} is a single-ended input with respect to GND with a range from 0V to V_{REF}.

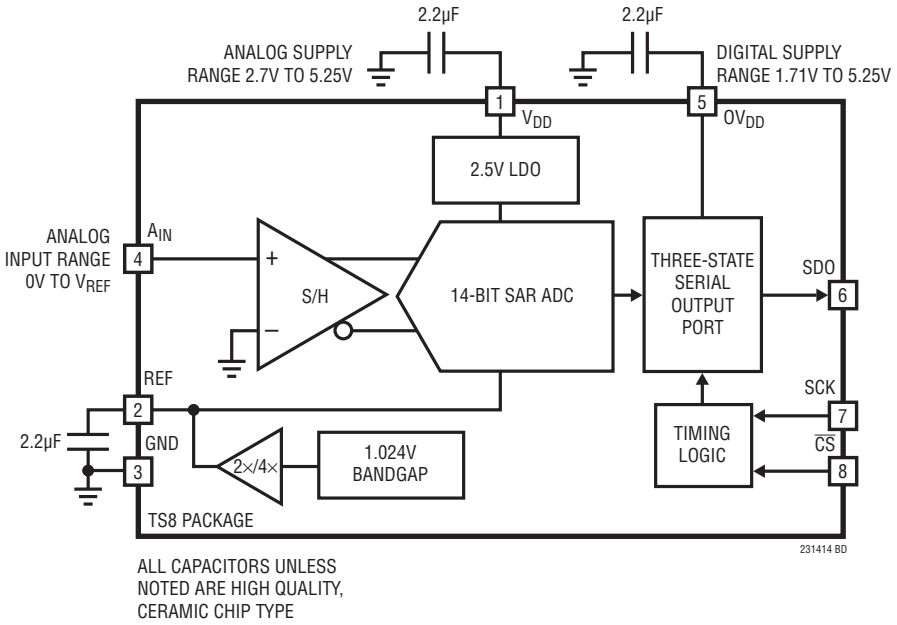
OV_{DD} (Pin 5): I/O Interface Digital Power. The OV_{DD} range is 1.71V to 5.25V. This supply is nominally set to the same supply as the host interface (1.8V, 2.5V, 3.3V or 5V). Bypass to GND with a 2.2µF ceramic chip capacitor.

SDO (Pin 6): Serial Data Output. The A/D conversion result is shifted out on SDO as a serial data stream with the MSB first through the LSB last. There is 1 cycle of conversion latency. Logic levels are determined by OV_{DD}.

SCK (Pin 7): Serial Data Clock Input. The SCK serial clock falling edge advances the conversion process and outputs a bit of the serialized conversion result, MSB first to LSB last. SDO data transitions on the falling edge of SCK. A continuous or burst clock may be used. Logic levels are determined by OV_{DD}.

$\overline{CS}$ (Pin 8): Chip Select Input. This active low signal starts a conversion on the falling edge and frames the serial data transfer. Bringing $\overline{CS}$ high places the sample-and-hold into sample mode and also forces the SDO pin into high impedance. Logic levels are determined by OV_{DD}.

BLOCK DIAGRAM



TIMING DIAGRAMS

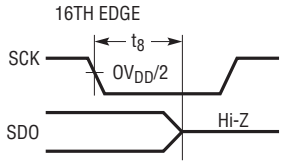


Figure 1. SDO Into Hi-Z after 16TH SCK↓

231414 TD01

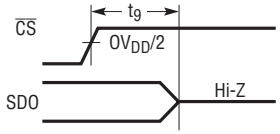


Figure 2. SDO Into Hi-Z after $\overline{CS}$↑

231414 TD02

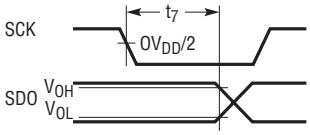


Figure 3. SDO Data Valid Hold after SCK↓

231414 TD03

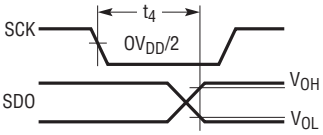


Figure 4. SDO Data Valid Access after SCK↓

231414 TD04

APPLICATIONS INFORMATION

Overview

The LTC2314-14 is a low noise, high speed, 14-bit successive approximation register (SAR) ADC. The LTC2314-14 operates over a wide supply range (2.7V to 5.25V) and provides a low drift (20ppm/°C maximum), internal reference and reference buffer. The internal reference buffer is automatically configured to a 2.048V span in low supply range (2.7V to 3.6V) and to a 4.096V span in the high supply range (4.75V to 5.25V). The LTC2314-14 samples at a 4.5Msps rate and supports an 87.5MHz data clock. The LTC2314-14 achieves excellent dynamic performance (77dB SINAD, 85dB THD) while dissipating only 31mW from a 5V supply at the 4.5Msps conversion rate.

The LTC2314-14 outputs the conversion data with one cycle of conversion latency on the SDO pin. The SDO pin output logic levels are supplied by the dedicated OV_{DD} supply pin which has a wide supply range (1.71V to 5.25V) allowing the LTC2314-14 to communicate with 1.8V, 2.5V, 3V or 5V systems.

The LTC2314-14 provides both nap and sleep power-down modes through serial interface control to reduce power dissipation during inactive periods.

Serial Interface

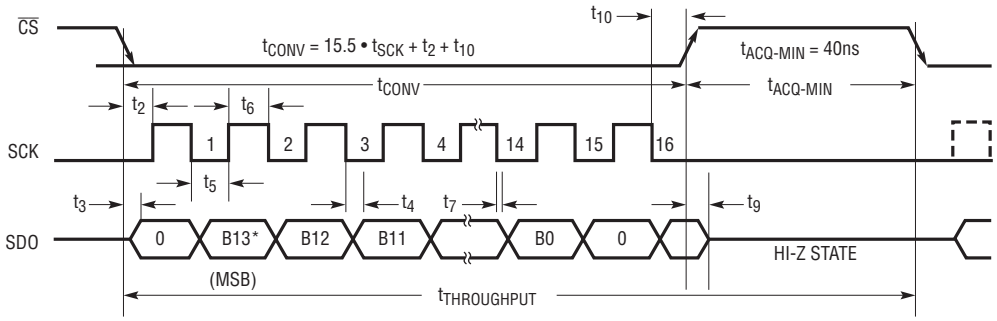
The LT2314-14 communicates with microcontrollers, DSPs and other external circuitry via a 3-wire interface. A falling CS edge starts a conversion and frames the serial data transfer. SCK provides the conversion clock for the current sample and controls the data readout on the SDO pin of the previous sample. CS transitioning low clocks out the first leading zero and subsequent SCK falling edges clock out the remaining data as shown in Figures 5, 6 and 7 for three different timing schemes. Data is serially output MSB first through LSB last, followed by trailing zeros if further SCK falling edges are applied. Figure 5 illustrates that during the case where SCK is held low during the acquisition phase, only one leading zero is output. Figures 6 and 7 illustrate that for the SCK held high during acquisition or continuous clocking mode two leading zeros are output. Leading zeros allow the 14-bit data result to be framed with both leading and trailing zeros for timing and data verification. Since the rising edge of SCK will be coincident with the falling edge of $\overline{CS}$, delay t_2 is the delay to the first falling edge of SCK, which is simply 0.5 • t_{SCK}. Delays t_2 ($\overline{CS}$ falling edge to SCK leading edge) and t_{10} (16th falling SCK edge to $\overline{CS}$ rising edge) must be observed for Figures 5, 6 and 7 and any timing implementation in order for the conversion process and data readout to occur correctly.

The user can bring $\overline{CS}$ high after the 16th falling SCK edge provided that timing delay t_{10} is observed. Prematurely terminating the conversion by bringing $\overline{CS}$ high before the 16th falling SCK edge plus delay t_{10} will cause a loss of conversion data for that sample. The sample-and-hold is placed in sample mode when $\overline{CS}$ is brought high. As shown in Figure 6, a sample rate of 4.5Msps can be achieved on the LTC2314-14 by using an 87.5MHz SCK data clock and a minimum acquisition time of 40ns which results in the minimum throughput time ($t_{THROUGHPUT}$) of 222ns. Note that the maximum throughput of 4.5Msps can only be achieved with the timing implementation of SCK held high during acquisition as shown in Figure 6.

The LTC2314-14 also supports a continuous data clock as shown in Figure 7. With a continuous data clock the acquisition time period and conversion time period must be designed as an exact integer number of data clock periods. Because the minimum acquisition time is not an exact multiple of the minimum SCK period, the maximum sample rate for the continuous SCK timing is less than 4.5Msps. For example, a 4.375Msps throughput is achieved using exactly 20 data clock periods with the maximum data clock frequency of 87.5MHz. For this particular case, the acquisition time period and conversion clock period are designed as 4 data clock periods (T_{ACQ} = 45.7ns) and 16data clock periods (T_{CONV} = 182.9ns) respectively, yielding a throughput time of 228.6ns.

The following table illustrates the maximum throughput achievable for each of the three timing patterns. Note that in order to achieve the maximum throughput rate of

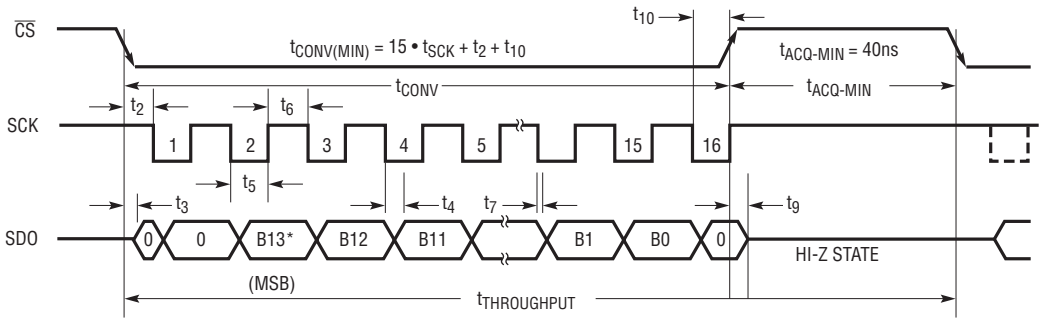
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*NOTE: SDO REPRESENTS THE ANALOG INPUT FROM THE PREVIOUS CONVERSION

231414 F05

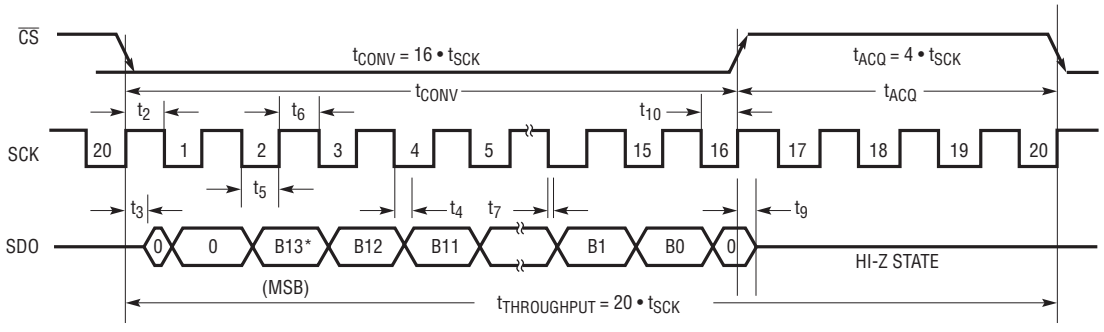
Figure 5: LTC2314-14 Serial Interface Timing Diagram (SCK Low During t_{ACQ})



*NOTE: SDO REPRESENTS THE ANALOG INPUT FROM THE PREVIOUS CONVERSION

231414 TD06

Figure 6: LTC2314-14 Serial Interface Timing Diagram (SCK High During t_{ACQ})



*NOTE: SDO REPRESENTS THE ANALOG INPUT FROM THE PREVIOUS CONVERSION

231414 TD07

Figure 7: LTC2314-14 Serial Interface Timing Diagram (SCK Continuous)

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4.5Msps, the timing pattern where SCK is held high during the acquisition time must be used.

Table 1: Maximum Throughput vs Timing Pattern

TIMING PATTERN	MAXIMUM THROUGHPUT
SCK high during T_{ACQ}	4.5Msps
SCK low during T_{ACQ}	4.375Msps
SCK continuous ($t_{THROUGHPUT}$ = 20 periods)	4.375Msps

Serial Data Output (SDO)

The SDO output is always forced into the high impedance state while $\overline{CS}$ is high. The falling edge of $\overline{CS}$ starts the conversion and enables SDO. The A/D conversion result is shifted out on the SDO pin as a serial data stream with the MSB first. The data stream consists of either one leading zero (SCK held low during acquisition, Fig. 5) or two leading zeros (SCK held high during acquisition, Fig. 6) followed by 14 bits of conversion data. There is 1 cycle of conversion latency. Subsequent falling SCK edges after the LSB is output will output zeros on the SDO pin. The SDO output returns to the high impedance state after the 16th falling edge of SCK.

The output swing on the SDO pin is controlled by the OV_{DD} pin voltage and supports a wide operating range from 1.71V to 5.25V independent of the V_{DD} pin voltage.

Power Considerations

The LTC2314-14 provides two sets of power supply pins: the analog 5V power supply (V_{DD}) and the digital input/output interface power supply (OV_{DD}). The flexible OV_{DD} supply allows the LTC2314-14 to communicate with any digital logic operating between 1.8V and 5V, including 2.5V and 3.3V systems.

Entering Nap/Sleep Mode

Pulsing $\overline{CS}$ two times and holding SCK static places the LTC2314-14 into nap mode. Pulsing $\overline{CS}$ four times and holding SCK static places the LTC2314-14 into sleep mode. In sleep mode, all bias circuitry is shut down, including the internal bandgap and reference buffer, and only leakage currents remain (0.8µA typical). Because the reference buffer is externally bypassed with a large capacitor (2.2µF), the LTC2314-14 requires a significant wait time (1.1ms) to recharge this capacitance before an accurate conversion can be made. In contrast, nap mode does not power down the internal bandgap or reference buffer allowing for a fast wake-up and accurate conversion within one conversion clock cycle. Supply current during nap mode is nominally 1.8mA.

Exiting Nap/Sleep Mode

Waking up the LTC2314-14 from either nap or sleep mode, as shown in Figures 8 and 9, requires SCK to be pulsed one time. A conversion may be started immediately following nap mode as shown in Figure 8. A period of time allowing the reference voltage to recover must follow waking up from sleep mode as shown in Figure 9. The wait period required before initiating a conversion for the recommended value of C_{REF} of 2.2µF is 1.1ms.

Power Supply Sequencing

The LTC2314-14 does not have any specific power supply sequencing requirements. Care should be taken to observe the maximum voltage relationships described in the Absolute Maximum Ratings section.

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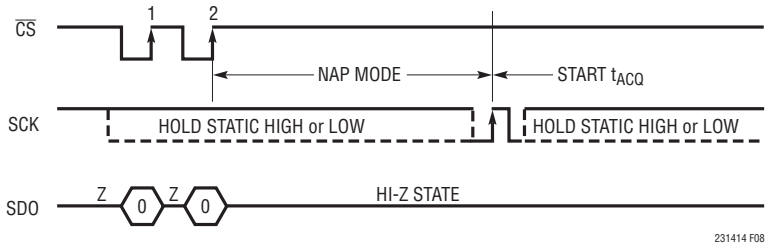


Figure 8: LTC2314-14 Entering/Exiting Nap Mode

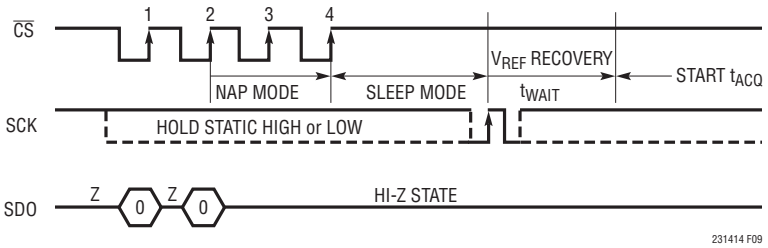


Figure 9: LTC2314-14 Entering/Exiting Sleep Mode

Single-Ended Analog Input Drive

The analog input of the LTC2314-14 is easy to drive. The input draws only one small current spike while charging the sample-and-hold capacitor at the end of conversion. During the conversion, the analog input draws only a small leakage current. If the source impedance of the driving circuit is low, then the input of the LTC2314-14 can be driven directly. As the source impedance increases, so will the acquisition time. For minimum acquisition time with high source impedance, a buffer amplifier should be used. The main requirement is that the amplifier driving the analog input must settle after the small current spike before the next conversion starts. Settling time must be less than $t_{ACQ\text{-}MIN}$ (40ns) for full performance at the maximum throughput rate. While choosing an input amplifier, also keep in mind the amount of noise and harmonic distortion the amplifier contributes.

Choosing an Input Amplifier

Choosing an input amplifier is easy if a few requirements are taken into consideration. First, to limit the magnitude of the voltage spike seen by the amplifier from charging the sampling capacitor, choose an amplifier that has a low output impedance (<50Ω) at the closed-loop bandwidth frequency. For example, if an amplifier is used in a gain of 1 and has a unity-gain bandwidth of 100MHz, then the output impedance at 100MHz must be less than 50Ω. The second requirement is that the closed-loop bandwidth must be greater than 100MHz to ensure adequate small signal settling for full throughput rate. If slower op amps are used, more time for settling can be provided by increasing the time between conversions. The best choice for an op amp to drive the LTC2314-14 will depend on the application. Generally, applications fall into two categories: AC applications where dynamic specifications are most

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critical and time domain applications where DC accuracy and settling time are most critical. The following list is a summary of the op amps that are suitable for driving the LTC2314-14. (More detailed information is available on the Linear Technology website at www.linear.com.)

LT6230: 215MHz GBWP, –80dBc Distortion at 1MHz, Unity-Gain Stable, Rail-to-Rail Input and Output, 3.5mA/Amplifier, 1.1nV/√Hz.

LT6200: 165MHz GBWP, –85dBc Distortion at 1MHz, Unity-Gain Stable, R-R In and Out, 15mA/Amplifier, 0.95nV/√Hz.

LT1818/1819: 400MHz GBWP, –85dBc Distortion at 5MHz, Unity-Gain Stable, 9mA/Amplifier, Single/Dual Voltage Mode Operational Amplifier.

Input Drive Circuits

The analog input of the LTC2314-14 is designed to be driven single-ended with respect to GND. A low impedance source can directly drive the high impedance analog input of the LTC2314-14 without gain error. A high impedance source should be buffered to minimize settling time during acquisition and to optimize the distortion performance of the ADC.

For best performance, a buffer amplifier should be used to drive the analog input of the LTC2314-14. The amplifier provides low output impedance to allow for fast settling of the analog signal during the acquisition phase. It also provides isolation between the signal source and the ADC inputs which draw a small current spike during acquisition.

Input Filtering

The noise and distortion of the buffer amplifier and other circuitry must be considered since they add to the ADC noise and distortion. Noisy input circuitry should be filtered prior to the analog inputs to minimize noise. A simple 1-pole RC filter is sufficient for many applications.

Large filter RC time constants slow down the settling at the analog inputs. It is important that the overall RC time constants be short enough to allow the analog inputs to completely settle to >12-bit resolution within the minimum acquisition time ($t_{ACQ-MIN}$) of 40ns.

A simple 1-pole RC filter is sufficient for many applications. For example, Figure 10 shows a recommended single-ended buffered drive circuit using the LT1818 in unity gain mode. The 47pF capacitor from A_{IN} to ground and 50Ω source resistor limits the input bandwidth to 68MHz. The 47pF capacitor also acts as a charge reservoir for the input sample-and-hold and isolates the LT1818 from sampling glitch kick-back. The 50Ω source resistor is used to help stabilize the settling response of the drive amplifier. When choosing values of source resistance and shunt capacitance, the drive amplifier data sheet should be consulted and followed for optimum settling response. If lower input bandwidths are desired, care should be taken to optimize the settling response of the driver amplifier with higher values of shunt capacitance or series resistance. High quality capacitors and resistors should be used in the RC filter since these components can add distortion. NP0/C0G and silver mica type dielectric capacitors have excellent linearity. Carbon surface mount resistors can generate distortion from self heating and from damage that may occur during soldering. Metal film surface mount resistors are much less susceptible to both problems. When high amplitude unwanted signals are close in frequency to the desired signal frequency, a multiple pole filter is required. High external source resistance, combined with external shunt capacitance at Pin 4 and 13pF of input capacitance on the LTC2314-14 in sample mode, will significantly reduce the internal 130MHz input bandwidth and may increase the required acquisition time beyond the minimum acquisition time ($t_{ACQ-MIN}$) of 40ns.

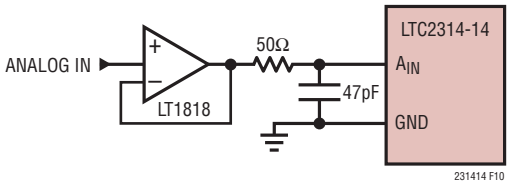


Figure 10. RC Input Filter

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ADC Reference

A low noise, low temperature drift reference is critical to achieving the full data sheet performance of the ADC. The LTC2314-14 provides an excellent internal reference with a guaranteed 20ppm/°C maximum temperature coefficient. For added flexibility, an external reference may also be used.

The high speed, low noise internal reference buffer is used only in the internal reference configuration. The reference buffer must be overdriven in the external reference configuration with a voltage 50mV higher than the nominal reference output voltage in the internal configuration.

Using the Internal Reference

The internal bandgap and reference buffer are active by default when the LTC2314-14 is not in sleep mode. The reference voltage at the REF pin scales automatically with the supply voltage at the V_{DD} pin. The scaling of the reference voltage with supply is shown in Table 2.

Table 2: Reference Voltage vs Supply Range

SUPPLY VOLTAGE (V_{DD})	REF VOLTAGE (V_{REF})
2.7V –> 3.6V	2.048V
4.75V –> 5.25V	4.096V

The reference voltage also determines the full-scale analog input range of the LTC2314-14. For example, a 2.048V reference voltage will accommodate an analog input range from 0V to 2.048V. An analog input voltage that goes below 0V will be coded as all zeros and an analog input voltage that exceeds 2.048V will be coded as all ones.

It is recommended that the REF pin be bypassed to ground with a low ESR, 2.2µF ceramic chip capacitor for optimum performance.

External Reference

An external reference can be used with the LTC2314-14 if better performance is required or to accommodate a larger input voltage span. The only constraints are that the external reference voltage must be 50mV higher than the internal reference voltage (see Table 2) and must be less than or equal to the supply voltage (or 4.3V for the 5V supply range). For example, a 3.3V external reference may be used with a 3.3V V_{DD} supply voltage to provide a 3.3V analog input voltage span (i.e. 3.3V > 2.048V + 50mV). Or alternatively, a 2.5V reference may be used with a 3V supply voltage to provide a 2.5V input voltage range (i.e. 2.5V > 2.048V + 50mV). The LTC6655-3.3, LTC6655-2.5, available from Linear Technology, may be suitable for many applications requiring a high performance external reference for either 3.3V or 2.5V input spans respectively.

Transfer Function

Figure 11 depicts the transfer function of the LTC2314-14. The code transitions occur midway between successive integer LSB values (i.e. 0.5LSB, 1.5LSB, 2.5LSB… FS-0.5LSB). The output code is straight binary with 1LSB = V_{REF}/16,384.

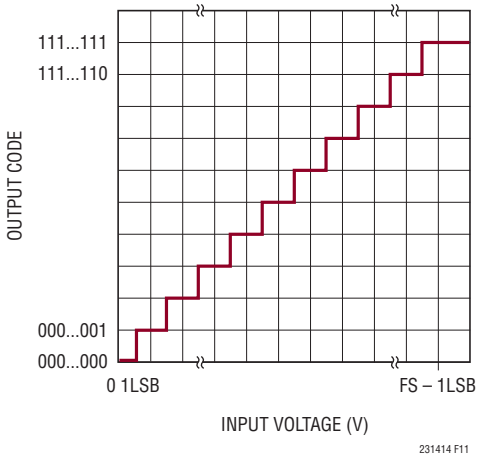


Figure 11. LTC2314-14 Transfer Function

DC Performance

The noise of an ADC can be evaluated in two ways: signal-to-noise ratio (SNR) in the frequency domain and histogram in the time domain. The LTC2314-14 excels in both. The noise in the time domain histogram is the

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transition noise associated with a 14-bit resolution ADC which can be measured with a fixed DC signal applied to the input of the ADC. The resulting output codes are collected over a large number of conversions. The shape of the distribution of codes will give an indication of the magnitude of the transition noise. In Figure 12, the distribution of output codes is shown for a DC input that has been digitized 16,384 times. The distribution is Gaussian and the RMS code transition noise is 0.7LSB. This corresponds to a noise level of 77.5dB relative to a full scale voltage of 4.096V.

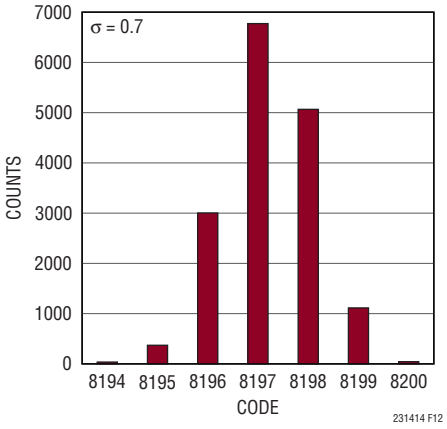


Figure 12. Histogram for 16384 Conversions

Dynamic Performance

The LTC2314-14 has excellent high speed sampling capability. Fast Fourier Transform (FFT) techniques are used to test the ADC's frequency response, distortion and noise at the rated throughput. By applying a low distortion sine wave and analyzing the digital output using an FFT algorithm, the ADC's spectral content can be examined for frequencies outside the applied fundamental. The LTC2314-14 provides guaranteed tested limits for both AC distortion and noise measurements.

Signal-to-Noise and Distortion Ratio (SINAD)

The signal-to-noise and distortion ratio (SINAD) is the ratio between the RMS amplitude of the fundamental input frequency and the RMS amplitude of all other frequency components at the A/D output. The output is band-limited to frequencies from above DC and below half the sampling frequency. Figure 14 shows the LTC2314-14 maintains a SINAD above 74dB up to the Nyquist input frequency of 2.25MHz.

Effective Number of Bits (ENOB)

The effective number of bits (ENOB) is a measurement of the resolution of an ADC and is directly related to SINAD by the equation where ENOB is the effective number of bits of resolution and SINAD is expressed in dB:

$$ENOB = (SINAD - 1.76)/6.02$$

At the maximum sampling rate of 5MHz, the LTC2314-14 maintains an ENOB above 12 bits up to the Nyquist input frequency of 2.25MHz. (Figure 14)

Signal-to-Noise Ratio (SNR)

The signal-to-noise ratio (SNR) is the ratio between the RMS amplitude of the fundamental input frequency and the RMS amplitude of all other frequency components except the first five harmonics and DC. Figure 13 shows that the LTC2314-14 achieves a typical SNR of 77.5dB at a 4.5MHz sampling rate with a 500kHz input frequency.

Total Harmonic Distortion (THD)

Total Harmonic Distortion (THD) is the ratio of the RMS sum of all harmonics of the input signal to the fundamental itself. The out-of-band harmonics alias into the frequency band between DC and half the sampling frequency ($f_{SMPL}/2$). THD is expressed as:

$$THD = 20\log\frac{\sqrt{V2^2 + V3^2 + V4^2 + V_N^2}}{V1}$$

where V1 is the RMS amplitude of the fundamental frequency and V2 through V_N are the amplitudes of the second through Nth harmonics. THD versus Input Frequency is shown in the Typical Performance Characteristics section. The LTC2314-14 has excellent distortion performance up to the Nyquist frequency.

Intermodulation Distortion (IMD)

If the ADC input signal consists of more than one spectral component, the ADC transfer function nonlinearity can produce intermodulation distortion (IMD) in addition to THD. IMD is the change in one sinusoidal input caused by the presence of another sinusoidal input at a different frequency.

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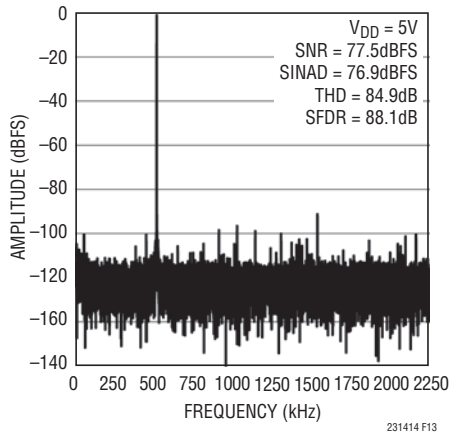


Figure 13. 32k Point FFT of the LTC2314-14 at f_{IN} = 500 kHz

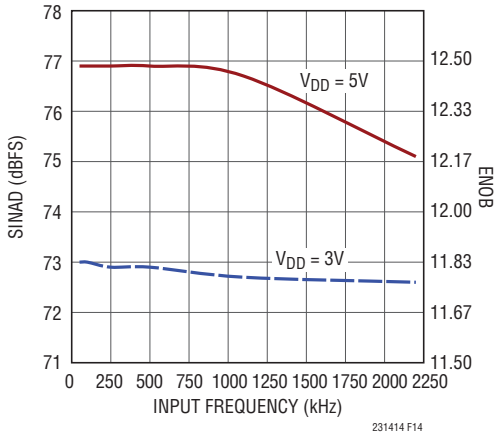


Figure 14. LTC2314-14 ENOB/SINAD vs f_{IN}

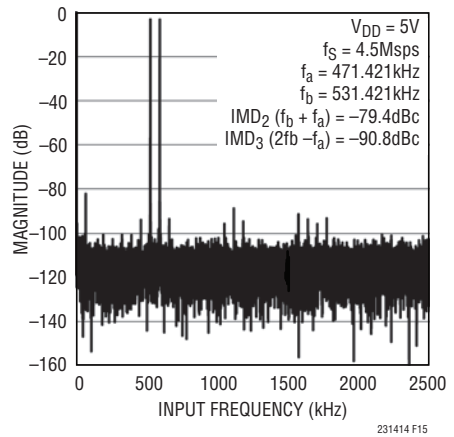


Figure 15. LTC2314-14 IMD Plot

If two pure sine waves of frequencies f_a and f_b are applied to the ADC input, nonlinearities in the ADC transfer function can create distortion products at the sum and difference frequencies $m \cdot f_a \pm n \cdot f_b$, where m and n = 0, 1, 2, 3, etc. For example, the 2nd order IMD terms include ($f_a \pm f_b$). If the two input sine waves are equal in magnitude, the value (in decibels) of the 2nd order IMD products can be expressed by the following formula:

$$IMD(f_a \pm f_b) = 20 \cdot \log[V_A (f_a \pm f_b)/V_A (f_a)]$$

The LTC2314-14 has excellent IMD as shown in Figure 15.

Spurious Free Dynamic Range (SFDR)

The spurious free dynamic range is the largest spectral component excluding DC, the input signal and the harmonics included in the THD. This value is expressed in decibels relative to the RMS value of a full-scale input signal.

Full-Power and Full-Linear Bandwidth

The full-power bandwidth is the input frequency at which the amplitude of the reconstructed fundamental is reduced by 3dB for a full-scale input signal.

The full-linear bandwidth is the input frequency at which the SINAD has dropped to 74dB (12 effective bits). The LTC2314-14 has been designed to optimize the input bandwidth, allowing the ADC to under-sample input signals with frequencies above the converter's Nyquist frequency. The noise floor stays very low at high frequencies and SINAD becomes dominated by distortion at frequencies beyond Nyquist.

Recommended Layout

To obtain the best performance from the LTC2314-14 a printed circuit board is required. Layout for the printed circuit board (PCB) should ensure the digital and analog signal lines are separated as much as possible. In particular, care should be taken not to run any digital clocks or signals alongside analog signals or underneath the ADC. The following is an example of a recommended PCB layout. A single solid ground plane is used. Bypass capacitors to the supplies are placed as close as possible to the supply pins. Low impedance common returns for these bypass

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capacitors are essential to the low noise operation of the ADC. The analog input traces are screened by ground. For more details and information refer to DC1563, the evaluation kit for the LTC2314-14.

Bypassing Considerations

High quality tantalum and ceramic bypass capacitors should be used at the V_{DD}, OV_{DD} and REF pins. For optimum performance, a 2.2µF ceramic chip capacitor should be used for the V_{DD} and OV_{DD} pins. The recommended bypassing for the REF pin is also a low ESR, 2.2µF ceramic capacitor. The traces connecting the pins and the bypass capacitors must be kept as short as possible and should be made as wide as possible avoiding the use of vias.

The following is an example of a recommended PCB layout. All analog circuitry grounds should be terminated at the LTC2314-14. The ground return from the LTC2314-14 to the power supply should be low impedance for noise free operation. Digital circuitry grounds must be connected to the digital supply common.

In applications where the ADC data outputs and control signals are connected to a continuously active microprocessor bus, it is possible to get errors in the conversion results. These errors are due to feed-through from the microprocessor to the successive approximation comparator. The problem can be eliminated by forcing the microprocessor into a "Wait" state during conversion or by using three-state buffers to isolate the ADC data bus.

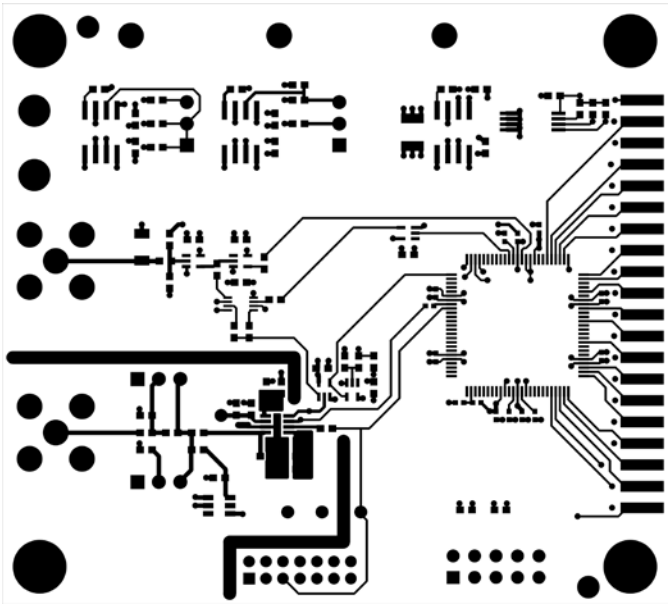


Figure 17. Layer 1 Top Layer

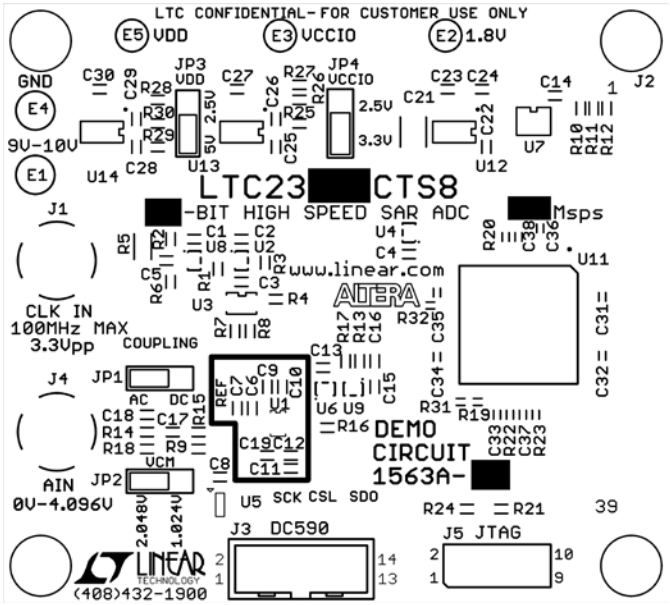


Figure 16. Top Silkscreen

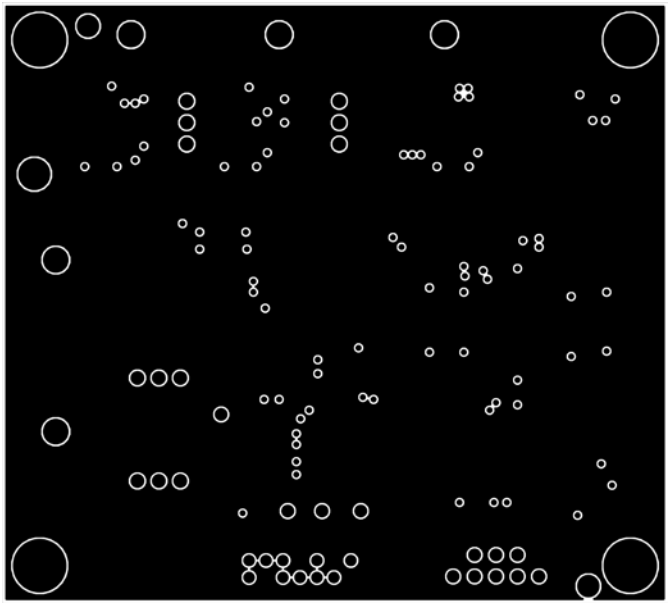


Figure 18. Layer 2 GND Plane

APPLICATIONS INFORMATION

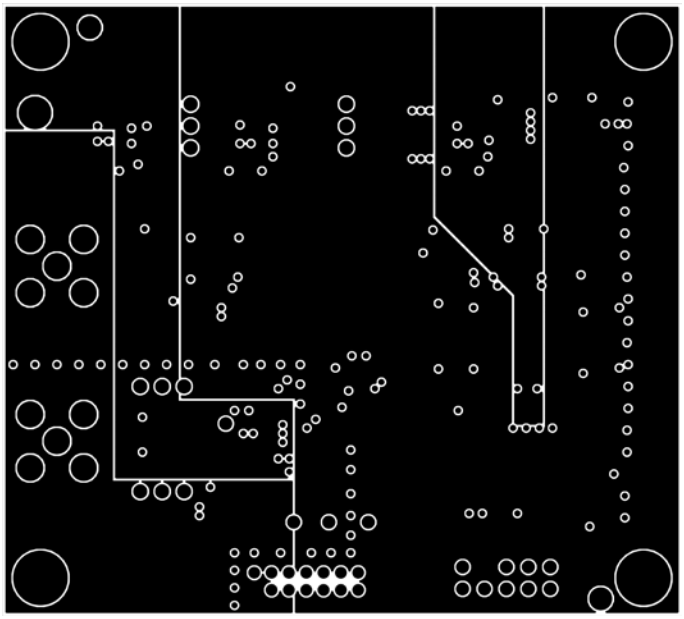


Figure 19. Layer 3 PWR Plane

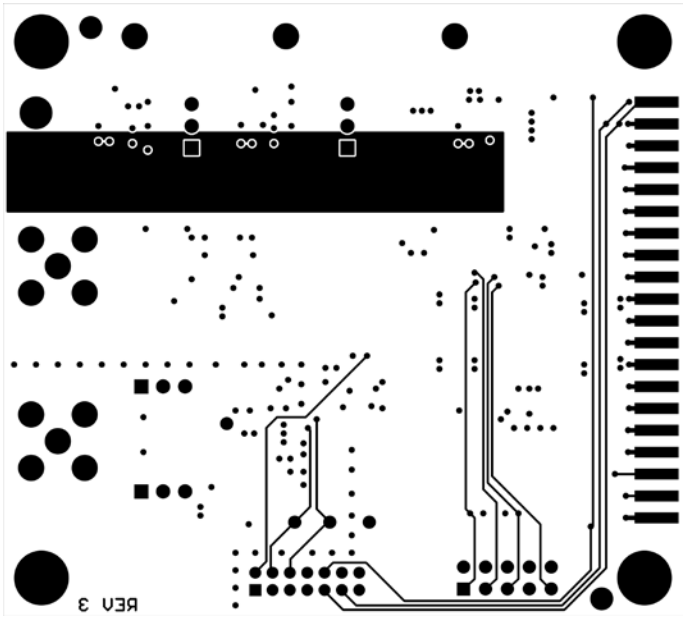


Figure 20. Layer 4 Bottom Layer

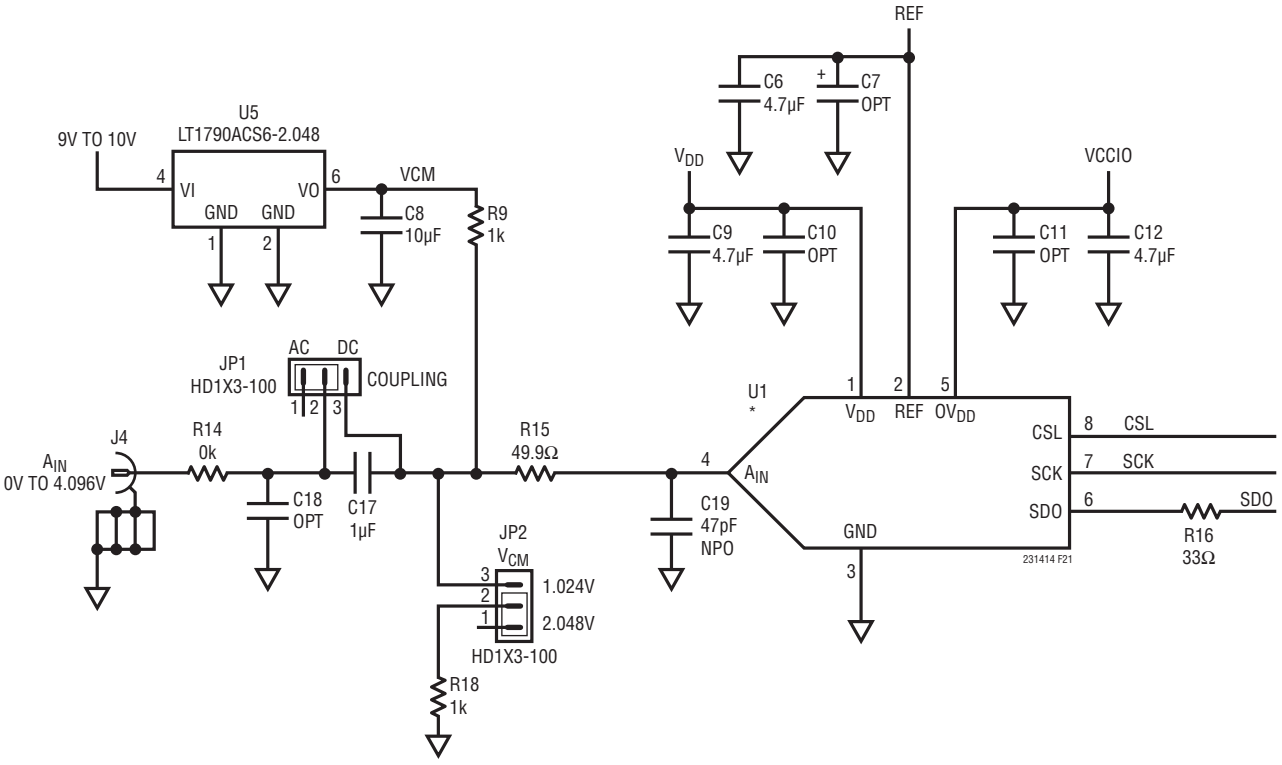
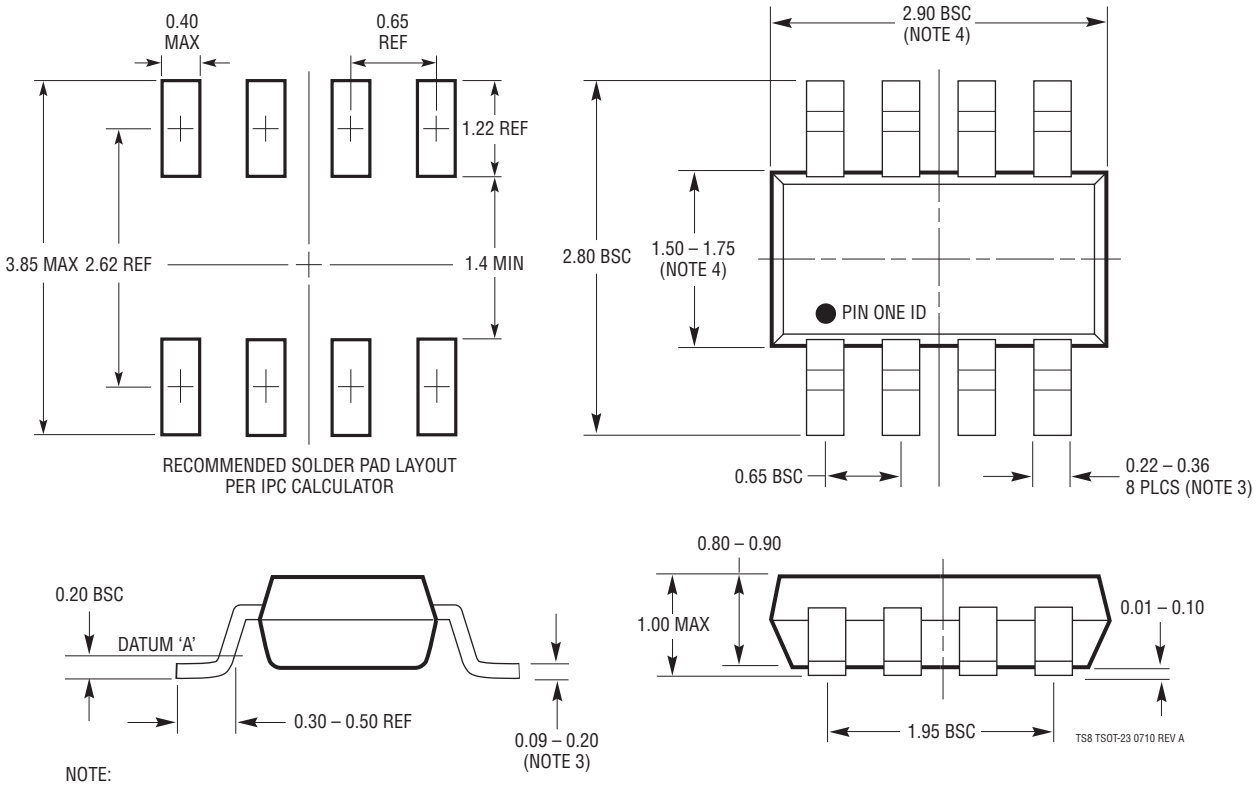


Figure 21. Partial 1563 Demo Board Schematic

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

TS8 Package
8-Lead Plastic TSOT-23
(Reference LTC DWG # 05-08-1637 Rev A)



NOTE:
1. DIMENSIONS ARE IN MILLIMETERS
2. DRAWING NOT TO SCALE
3. DIMENSIONS ARE INCLUSIVE OF PLATING
4. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH AND METAL BURR
5. MOLD FLASH SHALL NOT EXCEED 0.254mm
6. JEDEC PACKAGE REFERENCE IS MO-193

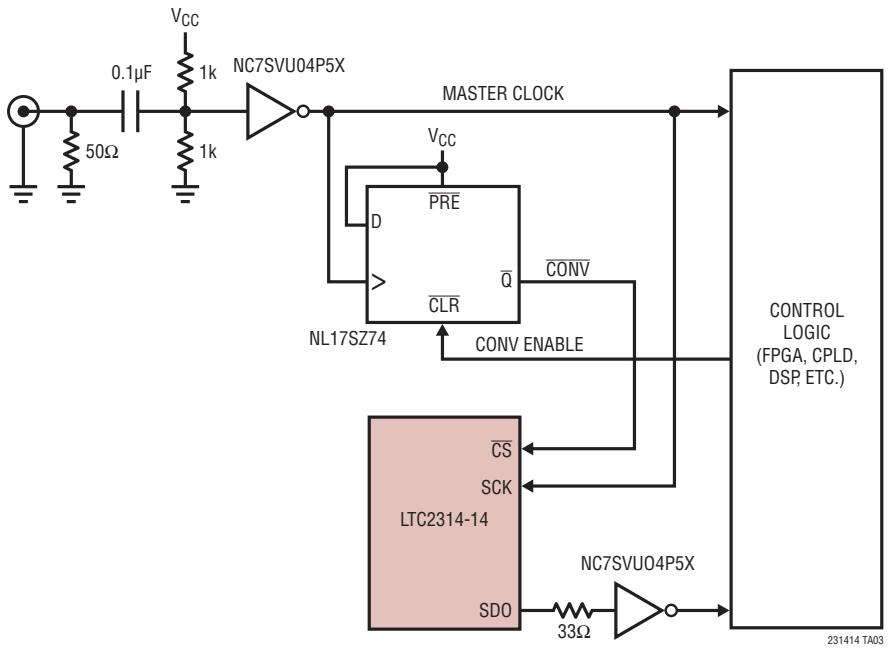
REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	10/13	Added pin-compatible family table	1
		Changed T_{JMAX} to 150°C	2
		Changed SINAD condition for –3dB Input Linear Bandwidth to ≥74dB	3
		Reordered/Renumbered Notes	3, 4, 5

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

TYPICAL APPLICATION

Low-Jitter Clock Timing with RF Sine Generator Using Clock Squaring/Level-Shifting Circuit and Re-Timing Flip-Flop



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
ADCs		
LTC2313-14	14-Bit, 2.5Msps Serial ADC	3V/5V, 14mW/25mW, 20ppm/°C Max Internal Reference, Single-Ended Input, 8-Lead TSOT-23 Package
LTC2312-14	14-Bit, 500ksps Serial ADC	3V/5V, 9mW/15mW, 20ppm/°C Max Internal Reference, Single-Ended Input, 8-Lead TSOT-23 Package
LTC1403A/LTC1403A-1	14-Bit, 2.8Msps Serial ADC	3V, 14mW, Unipolar/Bipolar Inputs, MSOP Package
LTC1407A/LTC1407A-1	14-Bit, 3Msps Simultaneous Sampling ADC	3V, 2-Channel Differential, Unipolar/Bipolar Inputs, 14mW, MSOP Package
LTC2355/LTC2356	12-/14-Bit, 3.5Msps Serial ADC	3.3V Supply, Differential Input, 18mW, MSOP Package
LTC2365/LTC2366	12-Bit, 1Msps/3Msps Serial Sampling ADC	3.3V Supply, 8mW, TSOT-23 Package
Amplifiers		
LT6200/LT6201	Single/Dual Operational Amplifiers	165MHz, 0.95nV/$\sqrt{Hz}$
LT6230/LT6231	Single/Dual Operational Amplifiers	215MHz, 3.5mA/Amplifier, 1.1nV/$\sqrt{Hz}$
LT6236/LT6237	Single/Dual Operational Amplifier with Low Wideband Noise	215MHz, 3.5mA/Amplifier, 1.1nV/$\sqrt{Hz}$
LT1818/LT1819	Single/Dual Operational Amplifiers	400MHz, 9mA/Amplifier, 6nV/$\sqrt{Hz}$
References		
LTC6655-2.5/LTC6655-3.3	Precision Low Drift Low Noise Buffered Reference	2.5V/3.3V, 5ppm/°C, 0.25ppm Peak-to-Peak Noise, MSOP-8 Package
LT1461-3/LT1461-3.3V	Precision Series Voltage Family	0.05% Initial Accuracy, 3ppm Drift

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