16-Bit, 125/105/80Msps Low Power Dual ADCs

FEATURES

- 2-Channel Simultaneous Sampling ADC
- Serial LVDS Outputs: 1, 2 or 4 Bits per Channel
- 76.8dB SNR
- 90dB SFDR
- Low Power: 432mW/360mW/249mW Total
- 216mW/180mW/125mW per Channel
- Single 1.8V Supply
- Selectable Input Ranges: $1V_{P-P}$ to $2V_{P-P}$
- 550MHz Full-Power Bandwidth S/H
- Shutdown and Nap Modes
- Serial SPI Port for Configuration
- 52-Pin (7mm × 8mm) QFN Package

APPLICATIONS

- Communications
- Cellular Base Stations
- Software-Defined Radios
- Portable Medical Imaging
- Multi-Channel Data Acquisition
- Nondestructive Testing

DESCRIPTION

The LTC®2195/LTC2194/LTC2193 are 2-channel, simultaneous sampling 16-bit A/D converters designed for digitizing high frequency, wide dynamic range signals. They are perfect for demanding communications applications with AC performance that includes 76.8dB SNR and 90dB spurious free dynamic range (SFDR). Ultralow jitter of $0.07ps_{RMS}$ allows undersampling of IF frequencies with excellent noise performance.

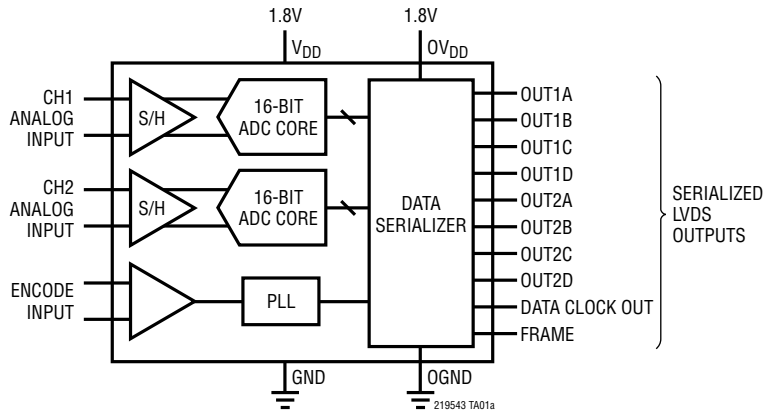
DC specs include ±2LSB INL (typ), ±0.5LSB DNL (typ) and no missing codes over temperature. The transition noise is $3.4LSB_{RMS}$.

To minimize the number of data lines the digital outputs are serial LVDS. Each channel outputs two bits or four bits at a time. At lower sampling rates there is a one bit per channel option. The LVDS drivers have optional internal termination and adjustable output levels to ensure clean signal integrity.

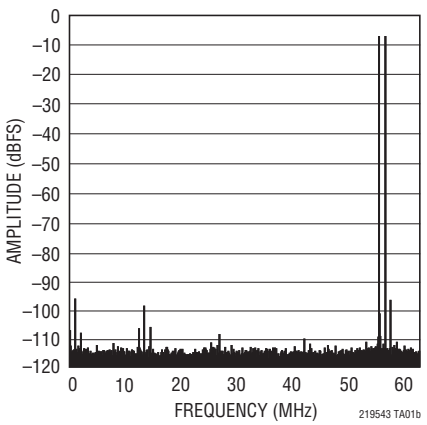
The ENC^+ and ENC^- inputs may be driven differentially or single ended with a sine wave, PECL, LVDS, TTL or CMOS inputs. An internal clock duty cycle stabilizer allows high performance at full speed for a wide range of clock duty cycles.

, LT, LTC, LTM, Linear Technology and the Linear logo are registered trademarks of Linear Technology Corporation. All other trademarks are the property of their respective owners.

TYPICAL APPLICATION



2-Tone FFT, f_{IN} = 70MHz and 69MHz



ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

Supply Voltages

V_{DD}, OV_{DD} ..... –0.3V to 2V

Analog Input Voltage

$A_{IN}+$, $A_{IN}–$, PAR/$\overline{SER}$, SENSE

(Note 3) .....–0.3V to (V_{DD} + 0.2V)

Digital Input Voltage

ENC^+, $ENC^–$, $\overline{CS}$, SDI, SCK (Note 4)..... –0.3V to 3.9V

SDO (Note 4) ..... –0.3V to 3.9V

Digital Output Voltage ..... –0.3V to (OV_{DD} + 0.3V)

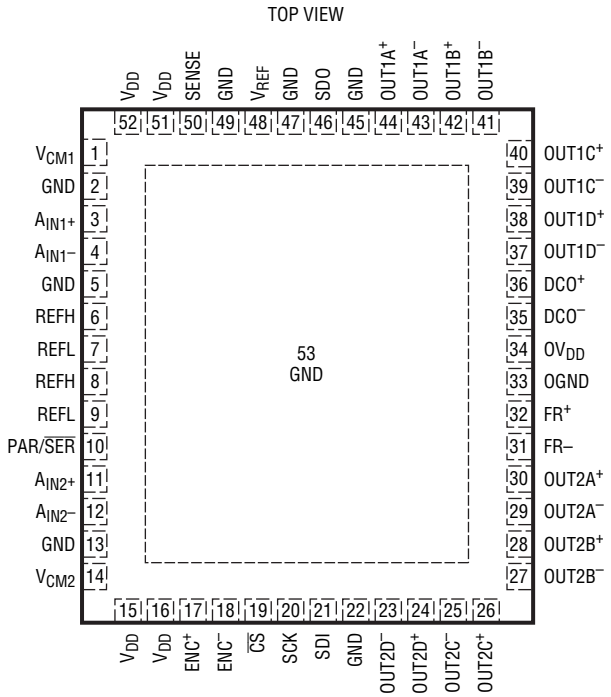
Operating Temperature Range

LTC2195C, LTC2194C, LTC2193C..... 0°C to 70°C

LTC2195I, LTC2194I, LTC2193I..... –40°C to 85°C

Storage Temperature Range..... –65°C to 150°C

PIN CONFIGURATION



UKG PACKAGE
52-LEAD (7mm × 8mm) PLASTIC QFN

T_{JMAX} = 150°C, θ_{JA} = 28°C/W
EXPOSED PAD (PIN 53) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC2195CUKG#PBF	LTC2195CUKG#TRPBF	LTC2195UKG	52-Lead (7mm × 8mm) Plastic QFN	0°C to 70°C
LTC2195IUKG#PBF	LTC2195IUKG#TRPBF	LTC2195UKG	52-Lead (7mm × 8mm) Plastic QFN	–40°C to 85°C
LTC2194CUKG#PBF	LTC2194CUKG#TRPBF	LTC2194UKG	52-Lead (7mm × 8mm) Plastic QFN	0°C to 70°C
LTC2194IUKG#PBF	LTC2194IUKG#TRPBF	LTC2194UKG	52-Lead (7mm × 8mm) Plastic QFN	–40°C to 85°C
LTC2193CUKG#PBF	LTC2193CUKG#TRPBF	LTC2193UKG	52-Lead (7mm × 8mm) Plastic QFN	0°C to 70°C
LTC2193IUKG#PBF	LTC2193IUKG#TRPBF	LTC2193UKG	52-Lead (7mm × 8mm) Plastic QFN	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

CONVERTER CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 5)

PARAMETER	CONDITIONS		LTC2195 MIN	LTC2195 TYP	LTC2195 MAX	LTC2194 MIN	LTC2194 TYP	LTC2194 MAX	LTC2193 MIN	LTC2193 TYP	LTC2193 MAX	UNITS
Resolution (No Missing Codes)		●	16			16			16			Bits
Integral Linearity Error	Differential Analog Input (Note 6)	●	–7	±2	7	–7.5	±2	7.5	–7.5	±2	7.5	LSB
Differential Linearity Error	Differential Analog Input	●	–0.9	±0.5	0.9	–0.9	±0.5	0.9	–0.9	±0.5	0.9	LSB
Offset Error	(Note 7)	●	–7	±1.5	7	–7	±1.5	7	–7	±1.5	7	mV
Gain Error	Internal Reference External Reference	 ●	 –2.0	±1.5 –0.7	 0.6	 –1.8	±1.5 –0.5	 0.8	 –1.8	±1.5 –0.5	 0.8	%FS %FS
Offset Drift				±10			±10			±10		µV/°C
Full-Scale Drift	Internal Reference External Reference			±30 ±10			±30 ±10			±30 ±10		ppm/°C ppm/°C
Gain Matching				±0.3			±0.3			±0.3		%FS
Offset Matching				±1.5			±1.5			±1.5		mV
Transition Noise				3.4			3.5			3.2		LSB_{RMS}

ANALOG INPUT

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Analog Input Range ($A_{IN}+ – A_{IN}–$)	1.7V < V_{DD} < 1.9V	●		1 to 2		V_{P-P}
$V_{IN(CM)}$	Analog Input Common Mode ($A_{IN}+ + A_{IN}–$)/2	Differential Analog Input (Note 8)	●	0.7	V_{CM}	1.25	V
V_{SENSE}	External Voltage Reference Applied to SENSE	External Reference Mode	●	0.625	1.250	1.300	V
I_{INCM}	Analog Input Common Mode Current	Per Pin, 125Msps Per Pin, 105Msps Per Pin, 80Msps			200 170 130		µA µA µA
I_{IN1}	Analog Input Leakage Current (No Encode)	0 < $A_{IN}+$, $A_{IN}–$ < V_{DD}	●	–1		1	µA
I_{IN2}	PAR/$\overline{SER}$ Input Leakage Current	0 < PAR/$\overline{SER}$ < V_{DD}	●	–3		3	µA
I_{IN3}	SENSE Input Leakage Current	0.625V < SENSE < 1.3V	●	–6		6	µA
t_{AP}	Sample-and-Hold Acquisition Delay Time				0		ns
t_{JITTER}	Sample-and-Hold Acquisition Delay Jitter	Single-Ended Encode Differential Encode			0.07 0.09		ps_{RMS} ps_{RMS}
CMRR	Analog Input Common Mode Rejection Ratio				80		dB
BW–3B	Full-Power Bandwidth	Figure 6 Test Circuit			550		MHz

DYNAMIC ACCURACY

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. A_{IN} = –1dBFS. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		LTC2195 MIN	LTC2195 TYP	LTC2195 MAX	LTC2194 MIN	LTC2194 TYP	LTC2194 MAX	LTC2193 MIN	LTC2193 TYP	LTC2193 MAX	UNITS
SNR	Signal-to-Noise Ratio	5MHz Input			76.8			76.7			77.1		dBFS
		70MHz Input	●	74.5	76.6		74.8	76.5		75.1	76.9		dBFS
		140MHz Input			76.1			76			76.4		dBFS
SFDR	Spurious Free Dynamic Range 2nd Harmonic	5MHz Input			90			90			90		dBFS
		70MHz Input	●	79	89		81	89		81	89		dBFS
		140MHz Input			84			84			84		dBFS
	Spurious Free Dynamic Range 3rd Harmonic	5MHz Input			90			90			90		dBFS
		70MHz Input	●	81	89		81	89		82	89		dBFS
		140MHz Input			84			84			84		dBFS
	Spurious Free Dynamic Range 4th Harmonic or Higher	5MHz Input			95			95			95		dBFS
		70MHz Input	●	88	95		89	95		89	95		dBFS
		140MHz Input			95			95			95		dBFS
S/(N+D)	Signal-to-Noise Plus Distortion Ratio	5MHz Input			76.6			76.5			76.9		dBFS
		70MHz Input	●	73.3	76.2		74	76.1		74.4	76.5		dBFS
		140MHz Input			75.1			75			75.3		dBFS
	Crosstalk	10MHz Input			–110			–110			–110		dBc

INTERNAL REFERENCE CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 5)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CM} Output Voltage	I_{OUT} = 0	0.5 • V_{DD} – 25mV	0.5 • V_{DD}	0.5 • V_{DD} + 25mV	V
V_{CM} Output Temperature Drift			±25		ppm/°C
V_{CM} Output Resistance	–600µA < I_{OUT} < 1mA		4		Ω
V_{REF} Output Voltage	I_{OUT} = 0	1.225	1.250	1.275	V
V_{REF} Output Temperature Drift			±25		ppm/°C
V_{REF} Output Resistance	–400µA < I_{OUT} < 1mA		7		Ω
V_{REF} Line Regulation	1.7V < V_{DD} < 1.9V		0.6		mV/V

DIGITAL INPUTS AND OUTPUTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
ENCODE INPUTS (ENC^+, ENC^-)							
Differential Encode Mode (ENC^- Not Tied to GND)							
V_{ID}	Differential Input Voltage	(Note 8)	●	0.2			V
V_{ICM}	Common Mode Input Voltage	Internally Set			1.2		V
		Externally Set (Note 8)	●	1.1		1.6	V
V_{IN}	Input Voltage Range	ENC^+, ENC^- to GND (Note 8)	●	0.2		3.6	V
R_{IN}	Input Resistance	See Figure 10			10		kΩ
C_{IN}	Input Capacitance	(Note 8)			3.5		pF

DIGITAL INPUTS AND OUTPUTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Single-Ended Encode Mode (ENC^- Tied to GND)							
V_{IH}	High Level Input Voltage	V_{DD} =1.8V	●	1.2			V
V_{IL}	Low Level Input Voltage	V_{DD} =1.8V	●			0.6	V
V_{IN}	Input Voltage Range	ENC^+ to GND	●	0		3.6	V
R_{IN}	Input Resistance	See Figure 11			30		kΩ
C_{IN}	Input Capacitance	(Note 8)			3.5		pF
DIGITAL INPUTS ($\overline{CS}$, SDI, SCK in Serial or Parallel Programming Mode. SDO in Parallel Programming Mode)							
V_{IH}	High Level Input Voltage	V_{DD} =1.8V	●	1.3			V
V_{IL}	Low Level Input Voltage	V_{DD} =1.8V	●			0.6	V
I_{IN}	Input Current	V_{IN} = 0V to 3.6V	●	–10		10	µA
C_{IN}	Input Capacitance	(Note 8)			3		pF
SDO OUTPUT (Serial Programming Mode. Open-Drain Output. Requires 2k Pull-Up Resistor if SDO is Used)							
R_{OL}	Logic Low Output Resistance to GND	V_{DD} =1.8V, SDO = 0V			200		Ω
I_{OH}	Logic High Output Leakage Current	SDO = 0V to 3.6V	●	–10		10	µA
C_{OUT}	Output Capacitance	(Note 8)			3		pF
DIGITAL DATA OUTPUTS							
V_{OD}	Differential Output Voltage	100Ω Differential Load, 3.5mA Mode 100Ω Differential Load, 1.75mA Mode	● ●	247 125	350 175	454 250	mV mV
V_{OS}	Common Mode Output Voltage	100Ω Differential Load, 3.5mA Mode 100Ω Differential Load, 1.75mA Mode	● ●	1.125 1.125	1.250 1.250	1.375 1.375	V V
R_{TERM}	On-Chip Termination Resistance	Termination Enabled, OV_{DD} = 1.8V			100		Ω

POWER REQUIREMENTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 9)

SYMBOL	PARAMETER	CONDITIONS		LTC2195 MIN	LTC2195 TYP	LTC2195 MAX	LTC2194 MIN	LTC2194 TYP	LTC2194 MAX	LTC2193 MIN	LTC2193 TYP	LTC2193 MAX	UNITS
V_{DD}	Analog Supply Voltage	(Note 10)	●	1.7	1.8	1.9	1.7	1.8	1.9	1.7	1.8	1.9	V
OV_{DD}	Output Supply Voltage	(Note 10)	●	1.7	1.8	1.9	1.7	1.8	1.9	1.7	1.8	1.9	V
I_{VDD}	Analog Supply Current	Sine Wave Input	●		224	248		185	205		123	138	mA
I_{OVDD}	Digital Supply Current	2-Lane Mode, 1.75mA Mode 2-Lane Mode, 3.5mA Mode 4-Lane Mode, 1.75mA Mode 4-Lane Mode, 3.5mA Mode	● ● ● ●		16 27 23 42	20 32 27 49		15 27 23 42	19 32 27 49		15 26 22 41	19 31 26 48	mA mA mA mA
P_{DISS}	Power Dissipation	2-Lane Mode, 1.75mA Mode 2-Lane Mode, 3.5mA Mode 4-Lane Mode, 1.75mA Mode 4-Lane Mode, 3.5mA Mode	● ● ● ●		432 452 445 479	482 504 495 535		360 382 375 409	403 427 418 457		249 269 261 295	283 304 295 335	mW mW mW mW
P_{SLEEP}	Sleep Mode Power				1			1			1		mW
P_{NAP}	Nap Mode Power				50			50			50		mW
$P_{DIFFCLK}$	Power Increase with Diffential Encode Mode Enabled (No Increase for Sleep Mode)				20			20			20		mW

TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		LTC2195 MIN	LTC2195 TYP	LTC2195 MAX	LTC2194 MIN	LTC2194 TYP	LTC2194 MAX	LTC2193 MIN	LTC2193 TYP	LTC2193 MAX	UNITS
f_S	Sampling Frequency	(Notes 10, 11)	●	5		125	5		105	5		80	MHz
t_{ENCL}	ENC Low Time (Note 8)	Duty Cycle Stabilizer Off Duty Cycle Stabilizer On	● ●	3.8 2	4 4	100 100	4.52 2	4.76 4.76	100 100	5.93 2	6.25 6.25	100 100	ns ns
t_{ENCH}	ENC High Time (Note 8)	Duty Cycle Stabilizer Off Duty Cycle Stabilizer On	● ●	3.8 2	4 4	100 100	4.52 2	4.76 4.76	100 100	5.93 2	6.25 6.25	100 100	ns ns
t_{AP}	Sample-and-Hold Acquistion Delay Time				0			0			0		ns
SYMBOL	**PARAMETER**	**CONDITIONS**		**MIN**			**TYP**			**MAX**			**UNITS**
Digital Data Outputs (R_{TERM} = 100Ω Differential, C_L = 2pF to GND On Each Output)													
t_{SER}	Serial Data Bit Period	4-Lane Output Mode 2-Lane Output Mode 1-Lane Output Mode					$1/(4 \cdot f_S)$ $1/(8 \cdot f_S)$ $1/(16 \cdot f_S)$						Sec
t_{FRAME}	FR to DCO Delay	(Note 8)	●		$0.35 \cdot t_{SER}$			$0.5 \cdot t_{SER}$			$0.65 \cdot t_{SER}$		Sec
t_{DATA}	Data to DCO Delay	(Note 8)	●		$0.35 \cdot t_{SER}$			$0.5 \cdot t_{SER}$			$0.65 \cdot t_{SER}$		Sec
t_{PD}	Propagation Delay	(Note 8)	●		$0.7n + 2 \cdot t_{SER}$			$1.1n + 2 \cdot t_{SER}$			$1.5n + 2 \cdot t_{SER}$		Sec
t_r	Output Rise Time	Data, DCO, FR, 20% to 80%						0.17					ns
t_f	Output Fall Time	Data, DCO, FR, 20% to 80%						0.17					ns
	DCO Cycle-Cycle Jitter	t_{SER} = 1ns						60					ps_{P-P}
	Pipeline Latency							7					Cycles
SPI Port Timing (Note 8)													
t_{SCK}	SCK Period	Write Mode Readback Mode, C_{SDO} = 20pF, R_{PULLUP} = 2k	● ●		40 250								ns ns
t_S	$\overline{CS}$-to-CLK Setup Time		●		5								ns
t_H	SCK-to-$\overline{CS}$ Setup Time		●		5								ns
t_{DS}	SDI Setup Time		●		5								ns
t_{DH}	SDI Hold Time		●		5								ns
t_{DO}	SCK Falling to SDO Valid	Readback Mode, C_{SDO} = 20pF, R_{PULLUP} = 2k	●						125				ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All voltage values are with respect to GND with GND and OGND shorted (unless otherwise noted).

Note 3: When these pin voltages are taken below GND or above V_{DD}, they will be clamped by internal diodes. This product can handle input currents of greater than 100mA below GND or above V_{DD} without latchup.

Note 4: When these pin voltages are taken below GND they will be clamped by internal diodes. When these pin voltages are taken above V_{DD} they will not be clamped by internal diodes. This product can handle input currents of greater than 100mA below GND without latchup.

Note 5: V_{DD} = OV_{DD} = 1.8V, f_{SAMPLE} = 125MHz (LTC2195), 105MHz (LTC2194), or 80MHz (LTC2193), 2-lane output mode, differential ENC^+/ENC^- = $2V_{P-P}$ sine wave, input range = $2V_{P-P}$ with differential drive, unless otherwise noted.

Note 6: Integral nonlinearity is defined as the deviation of a code from a best fit straight line to the transfer curve. The deviation is measured from the center of the quantization band.

Note 7: Offset error is the offset voltage measured from –0.5LSB when the output code flickers between 0000 0000 0000 0000 and 1111 1111 1111 1111 in 2's complement output mode.

Note 8: Guaranteed by design, not subject to test.

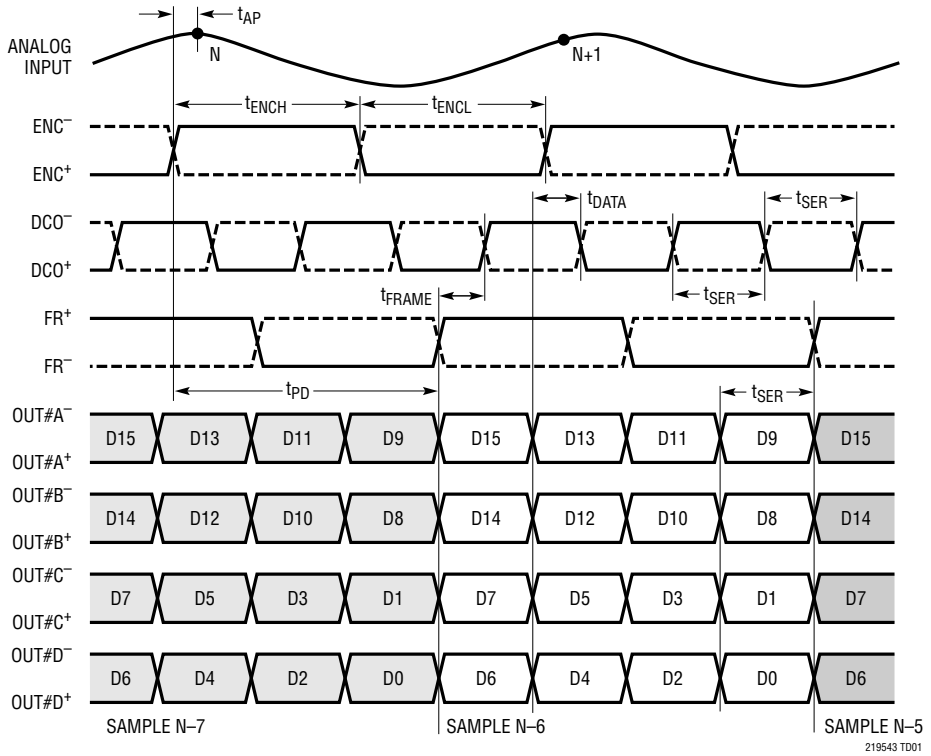
Note 9: V_{DD} = OV_{DD}=1.8V, f_{SAMPLE} = 125MHz (LTC2195), 105MHz (LTC2194), or 80MHz (LTC2193), 2-lane output mode, ENC^+ = single-ended 1.8V square wave, ENC^- = 0V, input range = $2V_{P-P}$ with differential drive, unless otherwise noted. The supply current and power dissipation specifications are totals for the entire IC, not per channel.

Note 10: Recommended operating conditions.

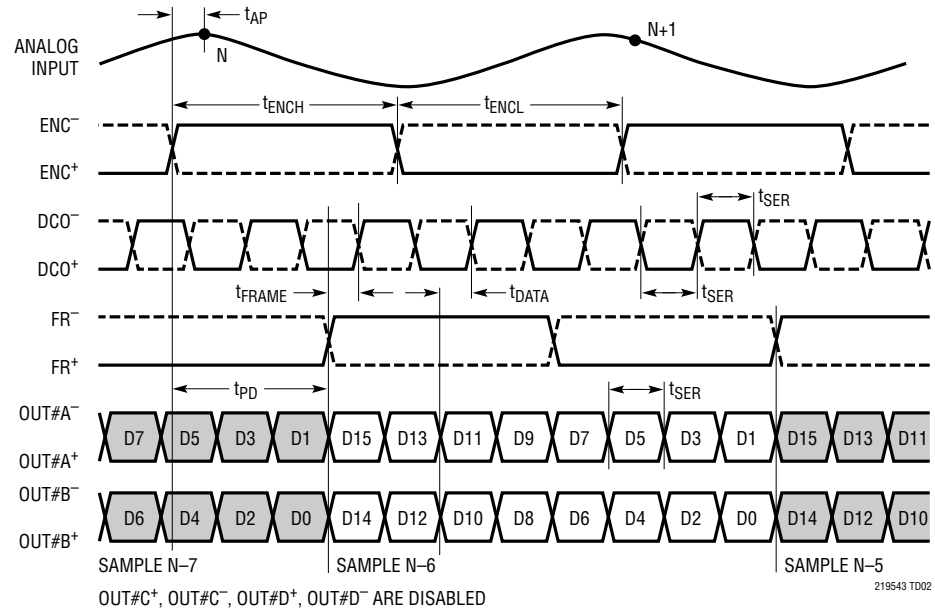
Note 11: The maximum sampling frequency depends on the speed grade of the part and also which serialization mode is used. The maximum serial data rate is 1000Mbps, so t_{SER} must be greater than or equal to 1ns.

TIMING DIAGRAMS

4-Lane Output Mode



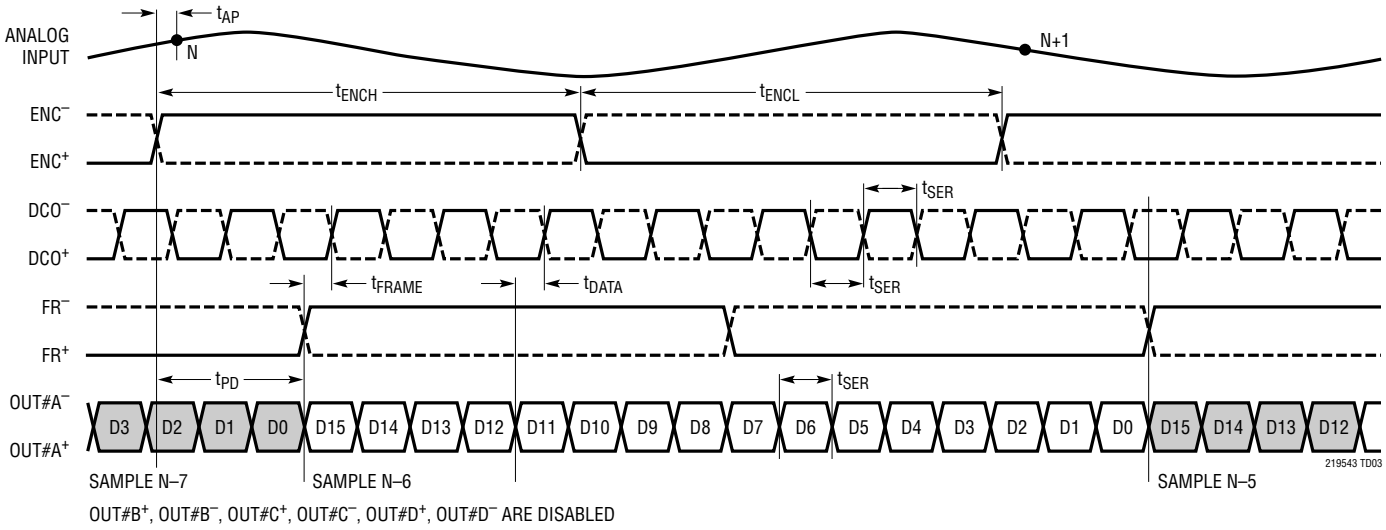
2-Lane Output Mode



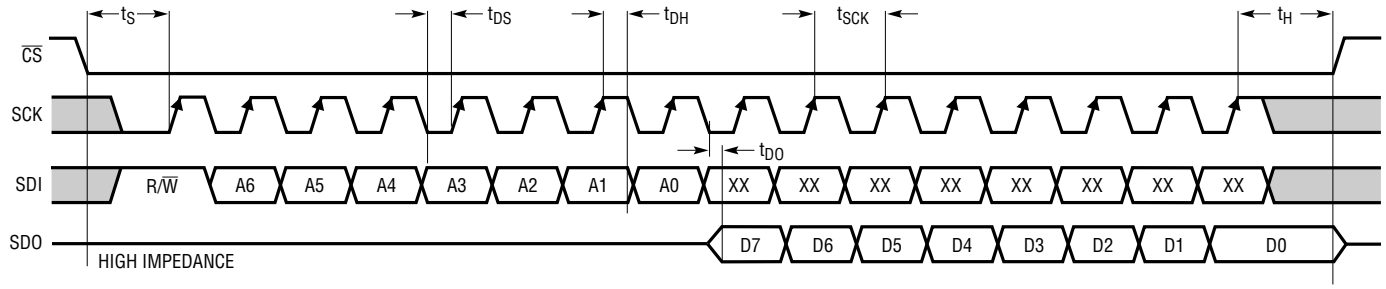
OUT#C+, OUT#C–, OUT#D+, OUT#D– ARE DISABLED

TIMING DIAGRAMS

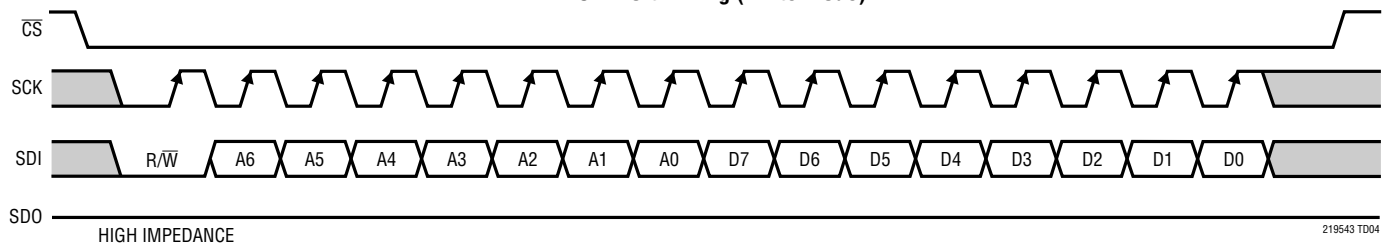
1-Lane Output Mode



SPI Port Timing (Readback Mode)

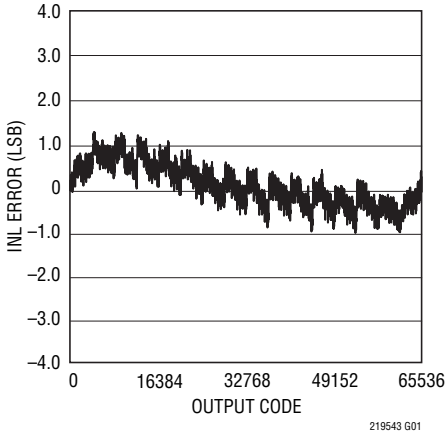


SPI Port Timing (Write Mode)

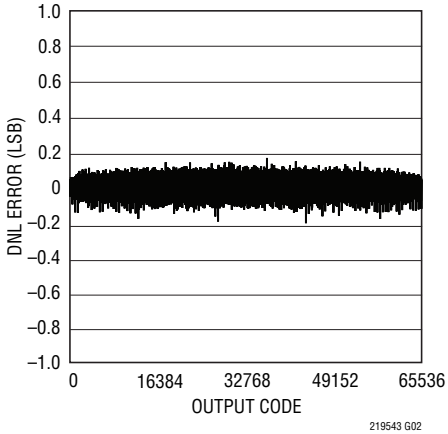


TYPICAL PERFORMANCE CHARACTERISTICS

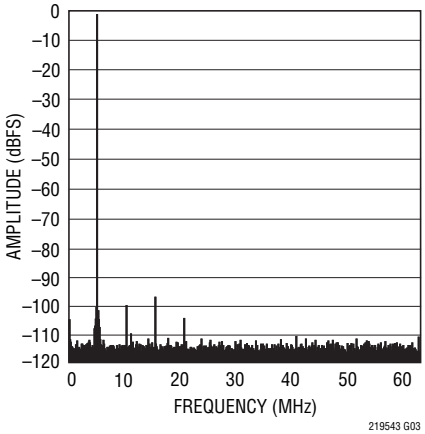
LTC2195: Integral Nonlinearity (INL)



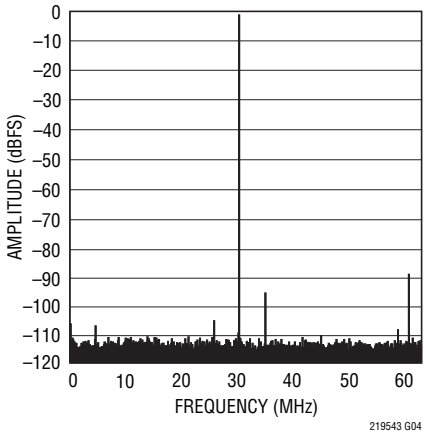
LTC2195: Differential Nonlinearity (DNL)



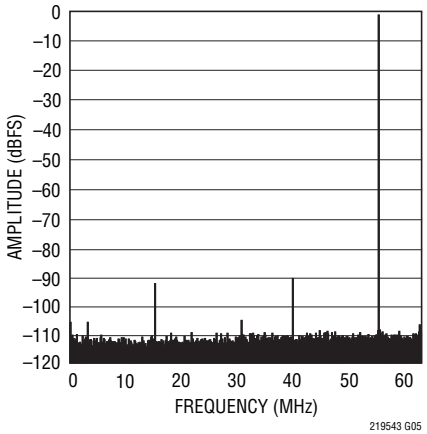
LTC2195: 64k Point FFT, f_{IN} = 5MHz, –1dBFS, 125Msps



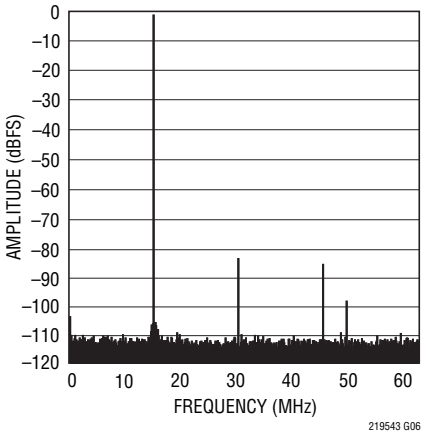
LTC2195: 64k Point FFT, f_{IN} = 30MHz, –1dBFS, 125Msps



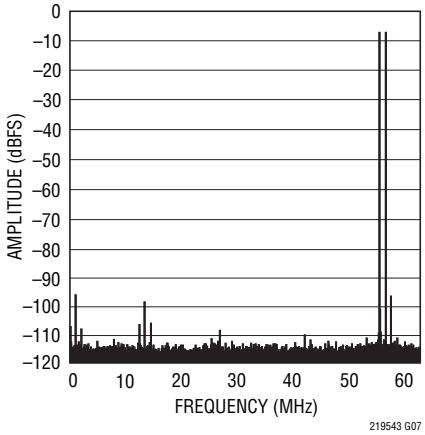
LTC2195: 64k Point FFT, f_{IN} = 70MHz, –1dBFS, 125Msps



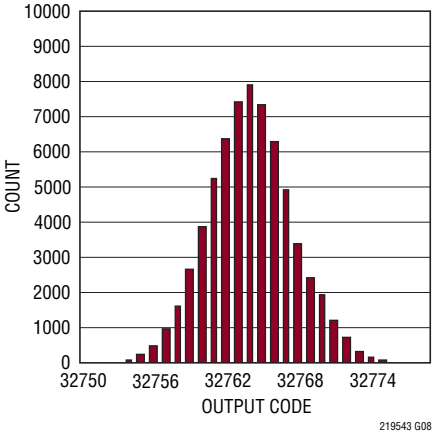
LTC2195: 64k Point FFT, f_{IN} = 140MHz, –1dBFS, 125Msps



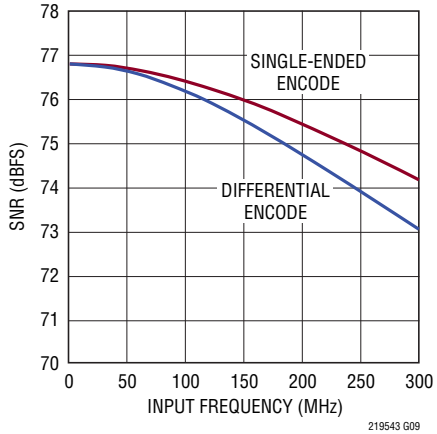
LTC2195: 64k Point 2-Tone FFT, f_{IN} = 69MHz, 70MHz, –7dBFS, 125Msps



LTC2195: Shorted Input Histogram

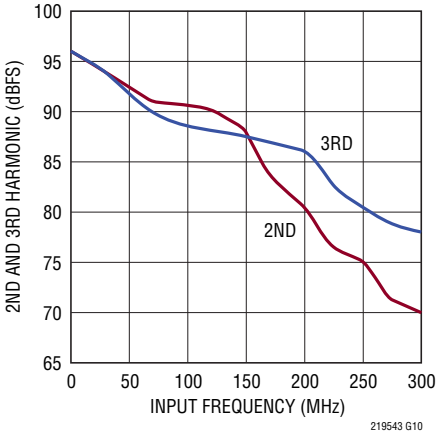


LTC2195: SNR vs Input Frequency, –1dBFS, 125Msps, 2V Range

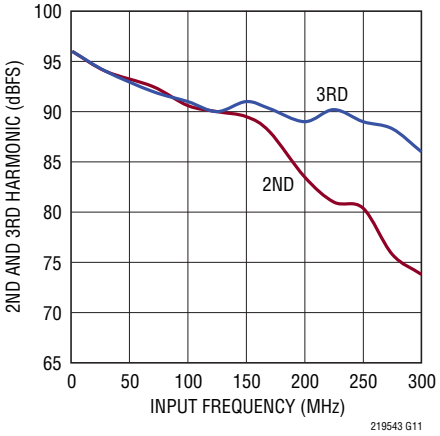


TYPICAL PERFORMANCE CHARACTERISTICS

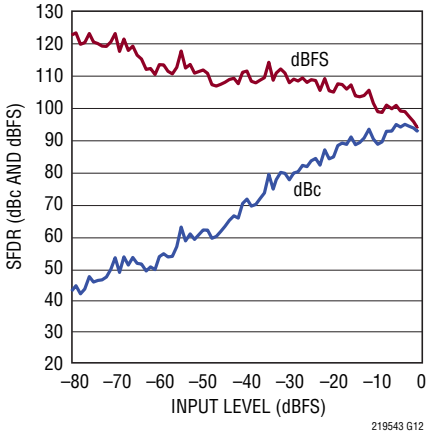
LTC2195: 2nd, 3rd Harmonic vs Input Frequency, –1dBFS, 125Msps, 2V Range



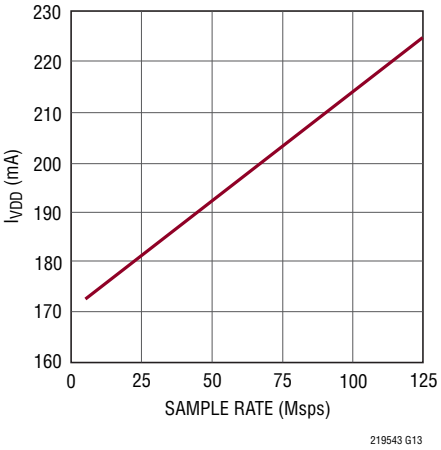
LTC2195: 2nd, 3rd Harmonic vs Input Frequency, –1dBFS, 125Msps, 1V Range



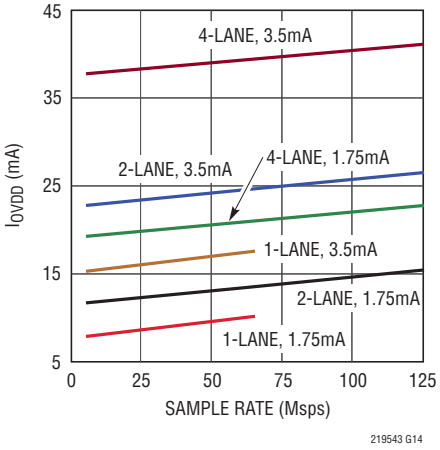
LTC2195: SFDR vs Input Level, f_{IN} = 70MHz, 125Msps, 2V Range



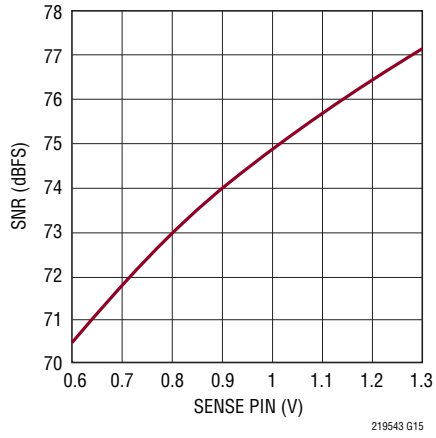
LTC2195: I_{VDD} vs Sample Rate, 5MHz, –1dBFS Sine Wave Input



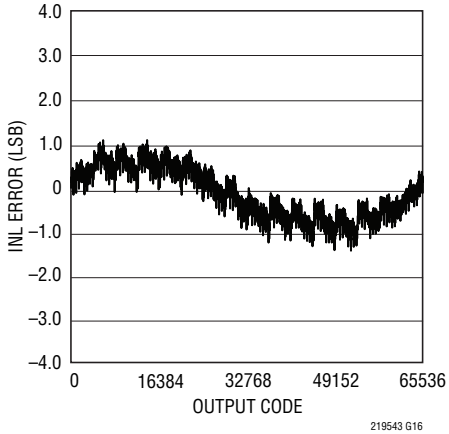
LTC2195: I_{OVDD} vs Sample Rate, 5MHz, –1dBFS Sine Wave Input



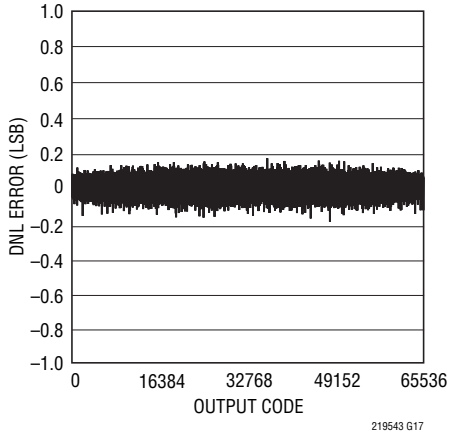
LTC2195: SNR vs SENSE, f_{IN} = 5MHz, –1dBFS



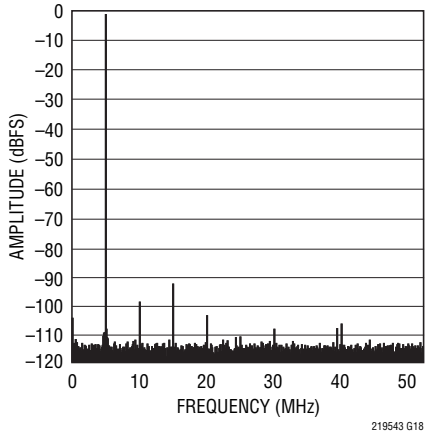
LTC2194: Integral Nonlinearity (INL)



LTC2194: Differential Nonlinearity (DNL)

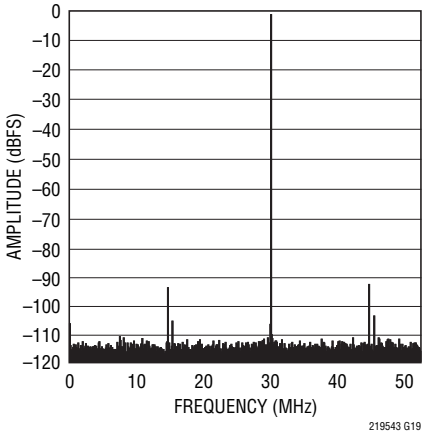


LTC2194: 64k Point FFT, f_{IN} = 5MHz, –1dBFS, 105Msps

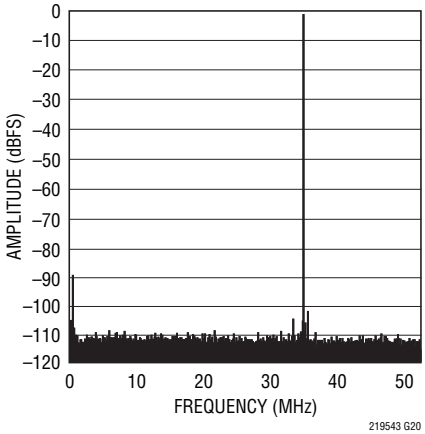


TYPICAL PERFORMANCE CHARACTERISTICS

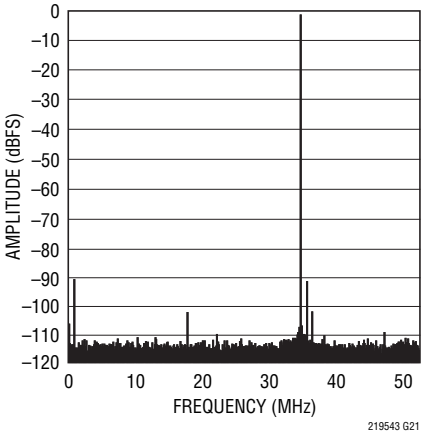
LTC2194: 64k Point FFT, f_{IN} = 30MHz, –1dBFS, 105Msps



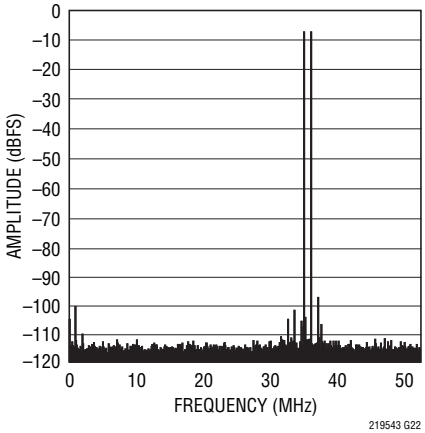
LTC2194: 64k Point FFT, f_{IN} = 70MHz, –1dBFS, 105Msps



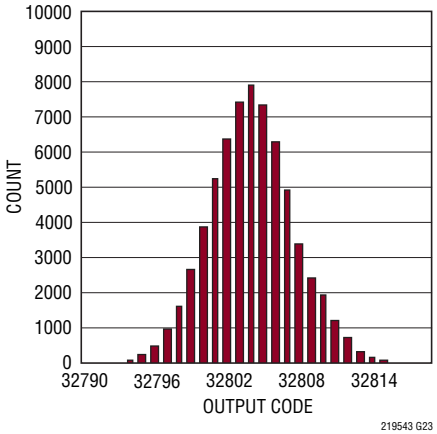
LTC2194: 64k Point FFT, f_{IN} = 140MHz, –1dBFS, 105Msps



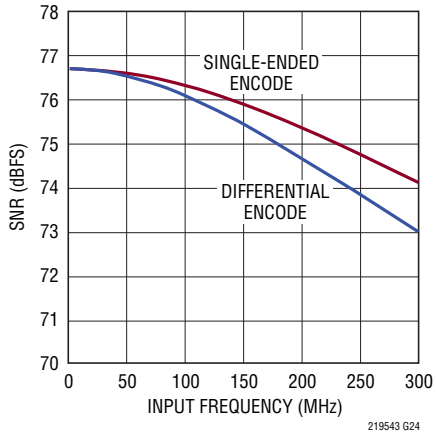
LTC2194: 64k Point 2-Tone FFT, f_{IN} = 69MHz, 70MHz, –7dBFS, 105Msps



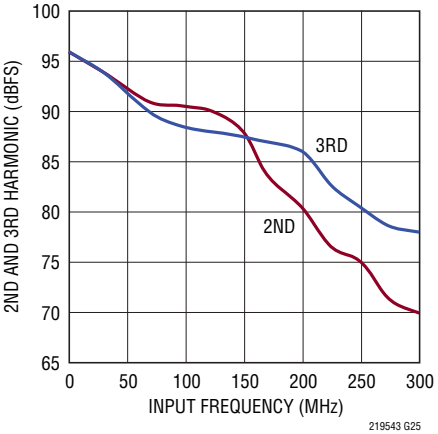
LTC2194: Shorted Input Histogram



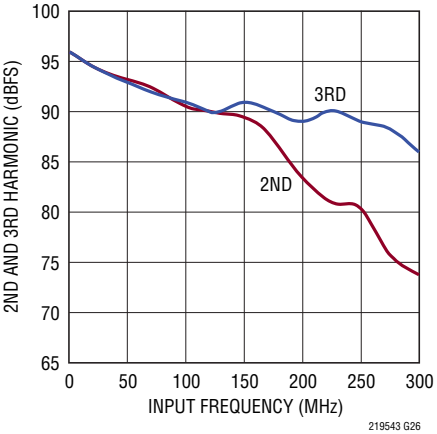
LTC2194: SNR vs Input Frequency, –1dBFS, 105Msps, 2V Range



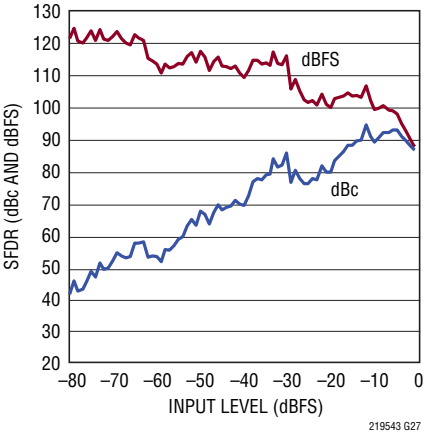
LTC2194: 2nd, 3rd Harmonic vs Input Frequency, –1dBFS, 105Msps, 2V Range



LTC2194: 2nd, 3rd Harmonic vs Input Frequency, –1dBFS, 105Msps, 1V Range

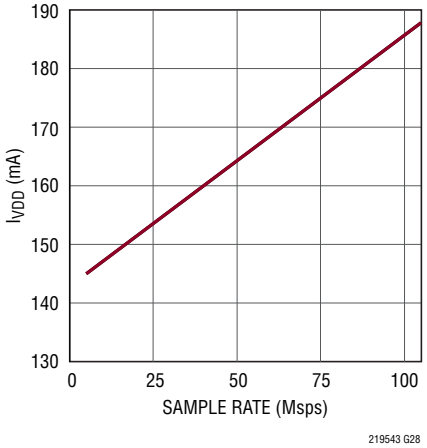


LTC2194: SFDR vs Input Level, f_{IN} = 70MHz, 105Msps, 2V Range

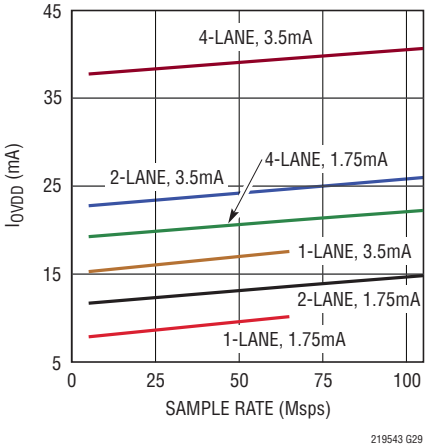


TYPICAL PERFORMANCE CHARACTERISTICS

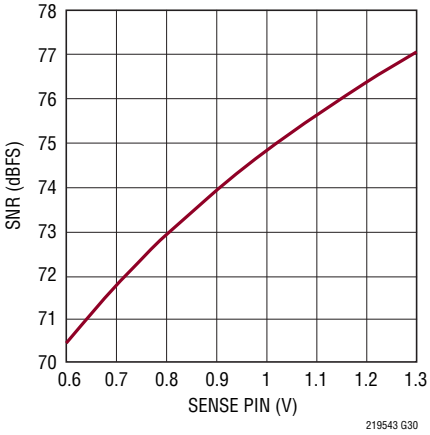
LTC2194: I_{VDD} vs Sample Rate, 5MHz, –1dBFS Sine Wave Input



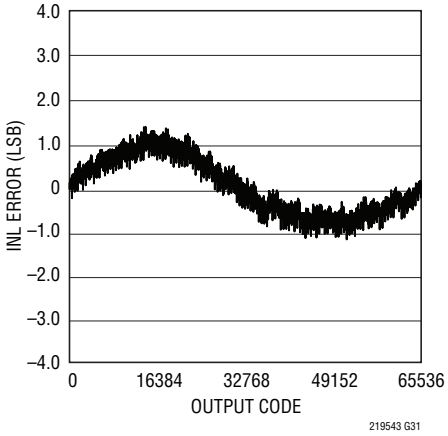
LTC2194: I_{OVDD} vs Sample Rate, 5MHz, –1dBFS Sine Wave Input



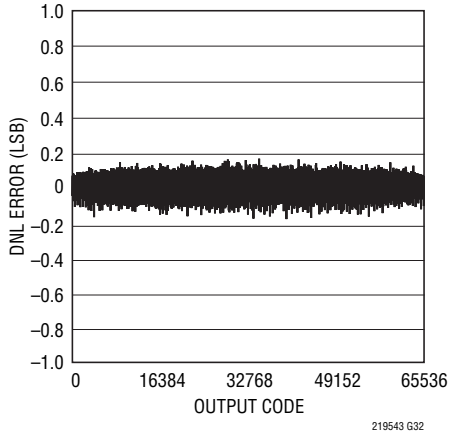
LTC2194: SNR vs SENSE, f_{IN} = 5MHz, –1dBFS



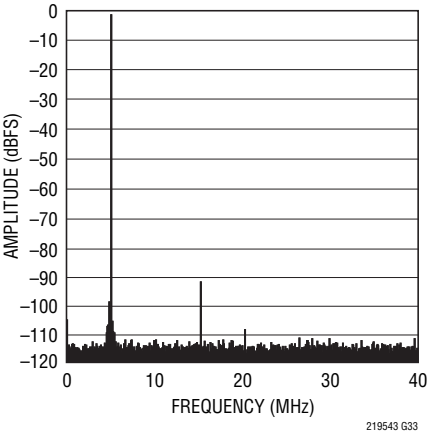
LTC2193: Integral Nonlinearity (INL)



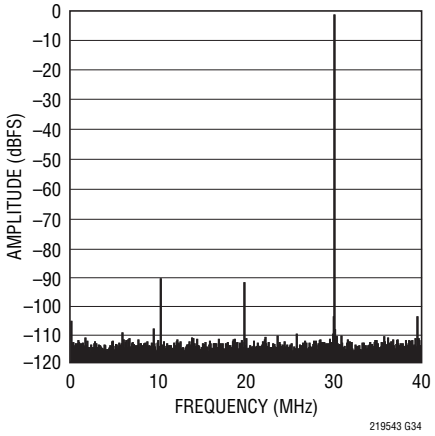
LTC2193: Differential Nonlinearity (DNL)



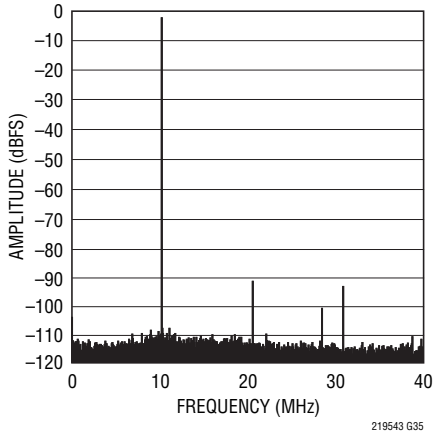
LTC2193: 64k Point FFT, f_{IN} = 5MHz, –1dBFS, 80Msps



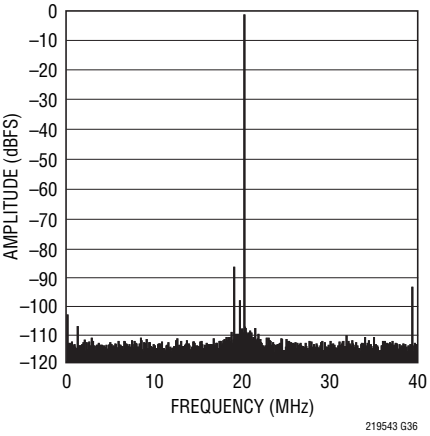
LTC2193: 64k Point FFT, f_{IN} = 30MHz, –1dBFS, 80Msps



LTC2193: 64k Point FFT, f_{IN} = 70MHz, –1dBFS, 80Msps

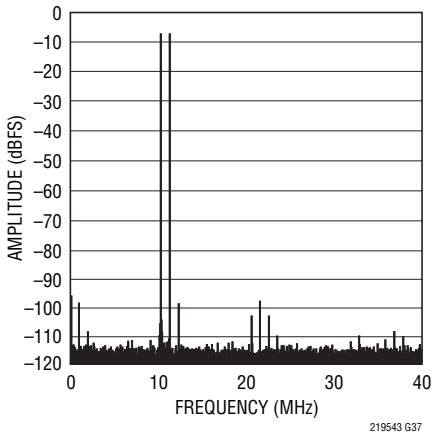


LTC2193: 64k Point FFT, f_{IN} = 140MHz, –1dBFS, 80Msps

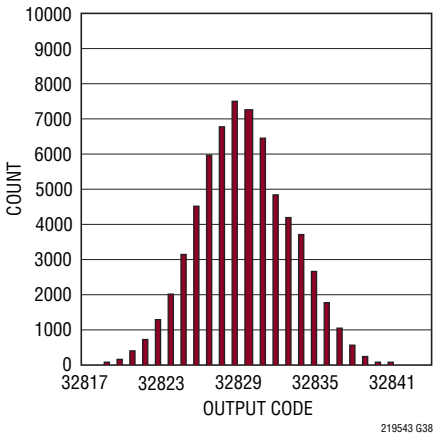


TYPICAL PERFORMANCE CHARACTERISTICS

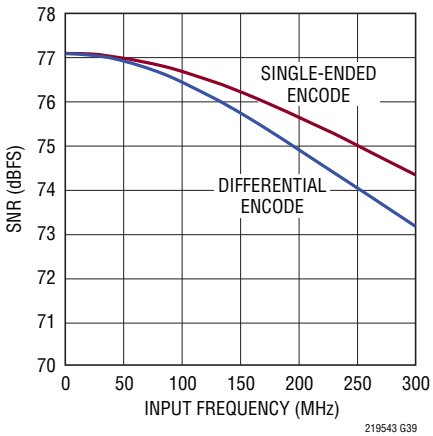
LTC2193: 64k Point, 2-Tone FFT, f_{IN} = 69MHz, 70MHz, –7dBFS, 80Msps



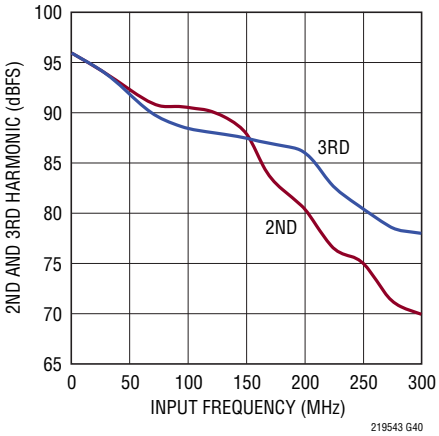
LTC2193: Shorted Input Histogram



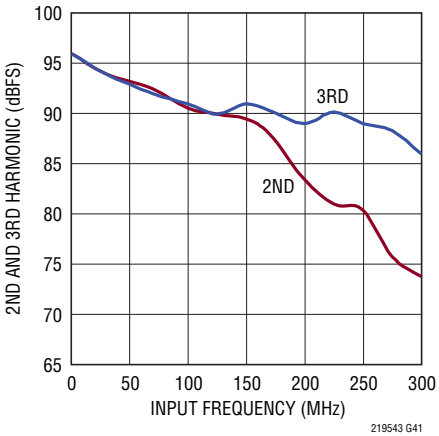
LTC2193: SNR vs Input Frequency, –1dBFS, 80Msps, 2V Range



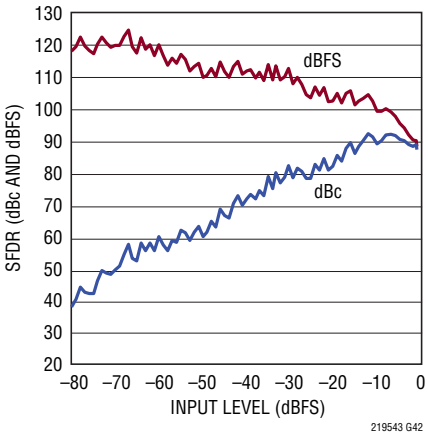
LTC2193: 2nd, 3rd Harmonic vs Input Frequency, –1dBFS, 80Msps, 2V Range



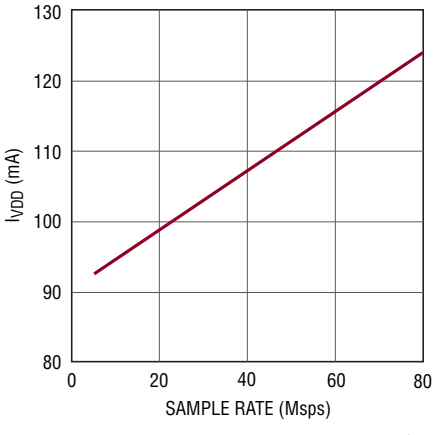
LTC2193: 2nd, 3rd Harmonic vs Input Frequency, –1dBFS, 80Msps, 1V Range



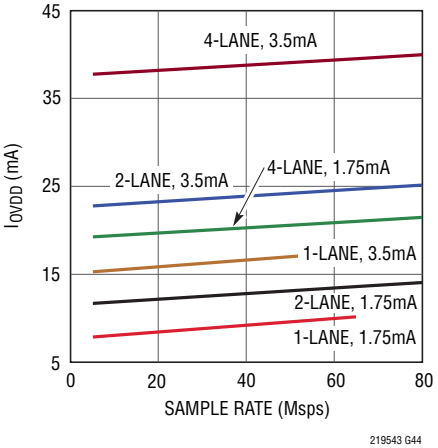
LTC2193: SFDR vs Input Level, f_{IN} = 70MHz, 80Msps, 2V Range



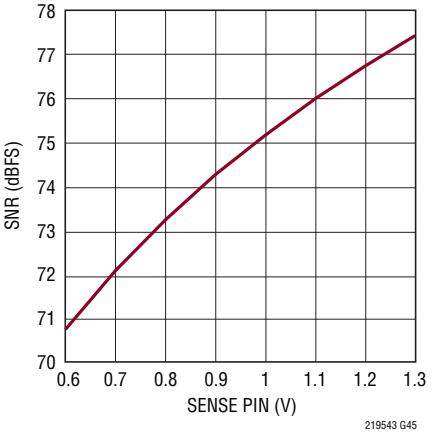
LTC2193: I_{VDD} vs Sample Rate, 5MHz, –1dBFS Sine Wave Input



LTC2193: I_{OVDD} vs Sample Rate, 5MHz, –1dBFS Sine Wave Input



LTC2193: SNR vs SENSE, f_{IN} = 5MHz, –1dBFS



PIN FUNCTIONS

V_{CM1} (Pin 1): Common Mode Bias Output, Nominally Equal to $V_{DD}/2$. V_{CM1} should be used to bias the common mode of the analog inputs of channel 1. Bypass to ground with a 0.1µF ceramic capacitor.

GND (Pins 2, 5, 13, 22, 45, 47, 49, Exposed Pad Pin 53): ADC Power Ground. The exposed pad must be soldered to the PCB ground.

A_{IN1}+ (Pin 3): Channel 1 Positive Differential Analog Input.

A_{IN1}– (Pin 4): Channel 1 Negative Differential Analog Input.

REFH (Pins 6, 8): ADC High Reference. See the Reference section in the Applications Information for recommended bypassing circuits for REFH and REFL.

REFL (Pins 7, 9): ADC Low Reference. See the Reference section in the Applications Information for recommended bypassing circuits for REFH and REFL.

PAR/$\overline{SER}$ (Pin 10): Programming Mode Selection Pin. Connect to ground to enable the serial programming mode. $\overline{CS}$, SCK, SDI, SDO become a serial interface that control the A/D operating modes. Connect to V_{DD} to enable the parallel programming mode where $\overline{CS}$, SCK, SDI, SDO become parallel logic inputs that control a reduced set of the A/D operating modes. PAR/$\overline{SER}$ should be connected directly to ground or the V_{DD} of the part and not be driven by a logic signal.

A_{IN2}+ (Pin 11): Channel 2 Positive Differential Analog Input.

A_{IN2}– (Pin 12): Channel 2 Negative Differential Analog Input.

V_{CM2} (Pin 14): Common Mode Bias Output, Nominally Equal to $V_{DD}/2$. V_{CM2} should be used to bias the common mode of the analog inputs of channel 2. Bypass to ground with a 0.1µF ceramic capacitor.

V_{DD} (Pins 15, 16, 51, 52): Analog Power Supply, 1.7V to 1.9V. Bypass to ground with 0.1µF ceramic capacitors. Adjacent pins can share a bypass capacitor.

ENC^+ (Pin 17): Encode Input. Conversion starts on the rising edge.

$ENC^–$ (Pin 18): Encode Complement Input. Conversion starts on the falling edge. Tie to GND for single-ended encode mode.

$\overline{CS}$ (Pin 19): In serial programming mode, (PAR/$\overline{SER}$ = 0V), $\overline{CS}$ is the serial interface chip select input. When $\overline{CS}$ is low, SCK is enabled for shifting data on SDI into the mode control registers. In the parallel programming mode (PAR/$\overline{SER}$ = V_{DD}), $\overline{CS}$ along with SCK selects 1-, 2- or 4-lane output mode (see Table 3). $\overline{CS}$ can be driven with 1.8V to 3.3V logic.

SCK (Pin 20): In serial programming mode, (PAR/$\overline{SER}$ = 0V), SCK is the serial interface clock input. In the parallel programming mode (PAR/$\overline{SER}$ = V_{DD}), SCK along with $\overline{CS}$ selects 1-, 2- or 4-lane output mode (see Table 3). SCK can be driven with 1.8V to 3.3V logic.

SDI (Pin 21): In Serial Programming Mode, (PAR/$\overline{SER}$ = 0V), SDI is the Serial Interface Data Input. Data on SDI is clocked into the mode control registers on the rising edge of SCK. In the parallel programming pode (PAR/$\overline{SER}$ = V_{DD}), SDI can be used to power down the part. SDI can be driven with 1.8V to 3.3V logic.

OGND (Pin 33): Output Driver Ground. This pin must be shorted to the ground plane by a very low inductance path. Use multiple vias close to the pin.

OV_{DD} (Pin 34): Output Driver Supply. Bypass to ground with a 0.1µF ceramic capacitor.

SDO (Pin 46): In serial programming mode, (PAR/$\overline{SER}$ = 0V), SDO is the optional serial interface data output. Data on SDO is read back from the mode control registers and can be latched on the falling edge of SCK. SDO is an open-drain NMOS output that requires an external 2k pull-up resistor to 1.8V to 3.3V. If read back from the mode control registers is not needed, the pull-up resistor is not necessary and SDO can be left unconnected. In the parallel programming mode (PAR/$\overline{SER}$ = V_{DD}), SDO selects 3.5mA or 1.75mA LVDS output currents. When used as an input, SDO can be driven with 1.8V to 3.3V logic through a 1k series resistor.

PIN FUNCTIONS

V_{REF} (Pin 48): Reference Voltage Output. Bypass to ground with a 2.2µF ceramic capacitor. The reference output is nominally 1.25V.

SENSE (Pin 50): Reference Programming Pin. Connecting SENSE to V_{DD} selects the internal reference and a ±1V input range. Connecting SENSE to ground selects the internal reference and a ±0.5V input range. An external reference between 0.625V and 1.3V applied to SENSE selects an input range of ±0.8 • V_{SENSE}.

LVDS Outputs

The following pins are differential LVDS outputs. The output current level is programmable. There is an optional internal 100Ω termination resistor between the pins of each LVDS output pair.

$OUT2D^-$/$OUT2D^+$, $OUT2C^-$/$OUT2C^+$, $OUT2B^-$/$OUT2B^+$, $OUT2A^-$/$OUT2A^+$ (Pins 23/24, 25/26, 27/28, 29/30): Serial Data Outputs for Channel 2. In 1-lane output mode only $OUT2A^-$/$OUT2A^+$ are used. In 2-lane output mode only $OUT2A^-$/$OUT2A^+$ and $OUT2B^-$/$OUT2B^+$ are used.

FR^-/FR^+ (Pins 31/32): Frame Start Outputs.

DCO^-/DCO^+ (Pins 35/36): Data Clock Outputs.

$OUT1D^-$/$OUT1D^+$, $OUT1C^-$/$OUT1C^+$, $OUT1B^-$/$OUT1B^+$, $OUT1A^-$/$OUT1A^+$ (Pins 37/38, 39/40, 41/42, 43/44): Serial Data Outputs for Channel 1. In 1-lane output mode only $OUT1A^-$/$OUT1A^+$ are used. In 2-lane output mode only $OUT1A^-$/$OUT1A^+$ and $OUT1B^-$/$OUT1B^+$ are used.

FUNCTIONAL BLOCK DIAGRAM

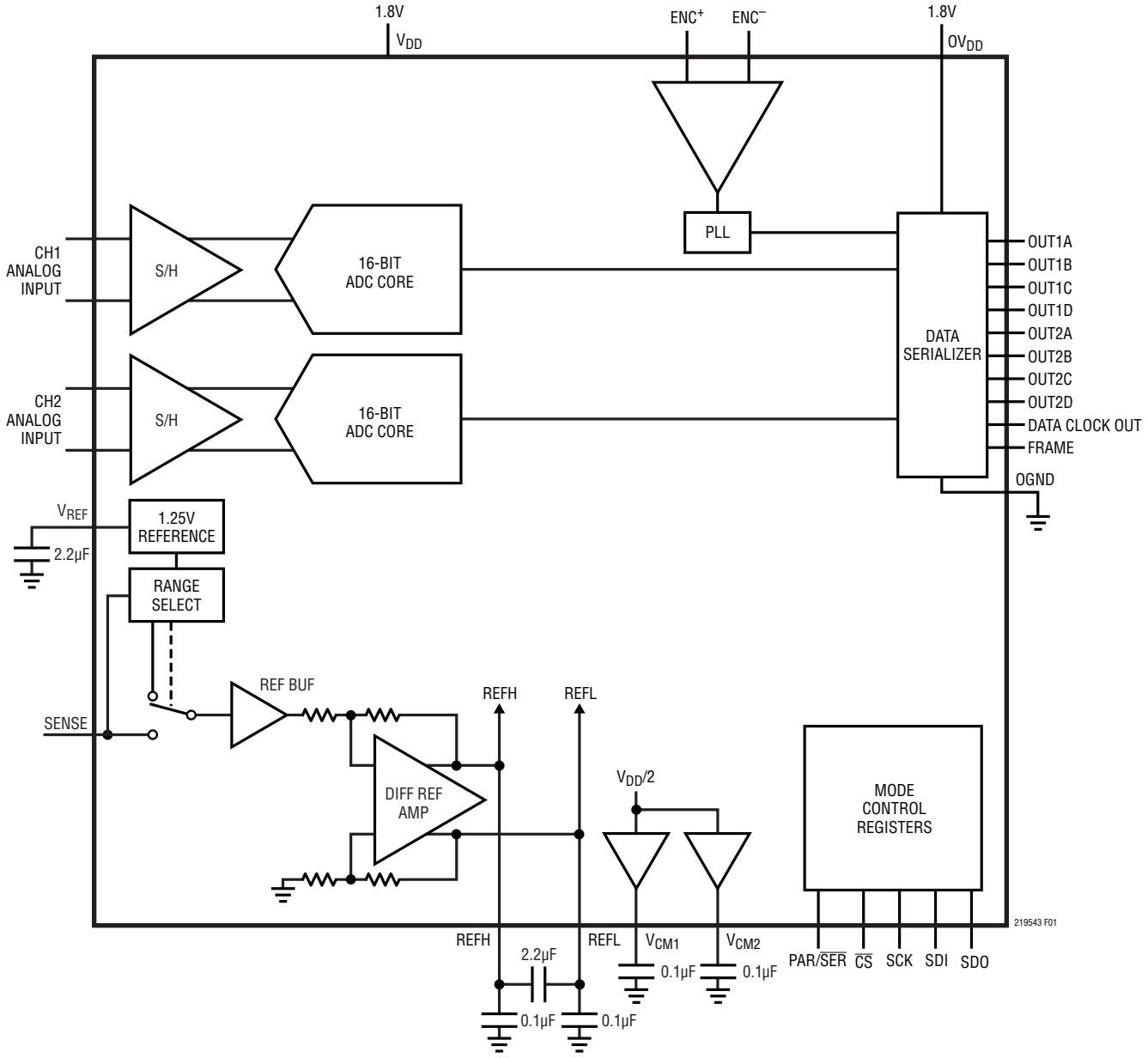


Figure 1. Functional Block Diagram

APPLICATIONS INFORMATION

CONVERTER OPERATION

The LTC2195/LTC2194/LTC2193 are low power, 2-channel, 16-bit, 125/105/80Msps A/D converters that are powered by a single 1.8V supply. The analog inputs should be driven differentially. The encode input can be driven differentially or single ended for lower power consumption. To minimize the number of data lines the digital outputs are serial LVDS. Each channel outputs two bits at a time (2-lane mode) or four bits at a time (4-lane mode). At lower sampling rates there is a one bit per channel option (1-lane mode). Many additional features can be chosen by programming the mode control registers through a serial SPI port.

ANALOG INPUT

The analog inputs are differential CMOS sample-and-hold circuits (Figure 2). The inputs should be driven differentially around a common mode voltage set by the V_{CM1} or V_{CM2} output pins, which are nominally $V_{DD}/2$. For the 2V input range, the inputs should swing from V_{CM} – 0.5V to V_{CM} + 0.5V. There should be 180° phase difference between the inputs.

The two channels are simultaneously sampled by a shared encode circuit (Figure 2).

Single-Ended Input

For applications less sensitive to harmonic distortion, the A_{IN}^+ input can be driven singled ended with a $1V_{P-P}$ signal centered around V_{CM}. The A_{IN}^- input should be connected to V_{CM} and the V_{CM} bypass capacitor should be increased to 2.2µF. With a singled-ended input the harmonic distortion and INL will degrade, but the noise and DNL will remain unchanged.

INPUT DRIVE CIRCUITS

Input Filtering

If possible, there should be an RC lowpass filter right at the analog inputs. This lowpass filter isolates the drive circuitry from the A/D sample-and-hold switching, and also limits wideband noise from the drive circuitry. Figure 3 shows an example of an input RC filter. The RC component values should be chosen based on the application's input frequency.

Transformer Coupled Circuits

Figure 3 shows the analog input being driven by an RF transformer with a center-tapped secondary. The center

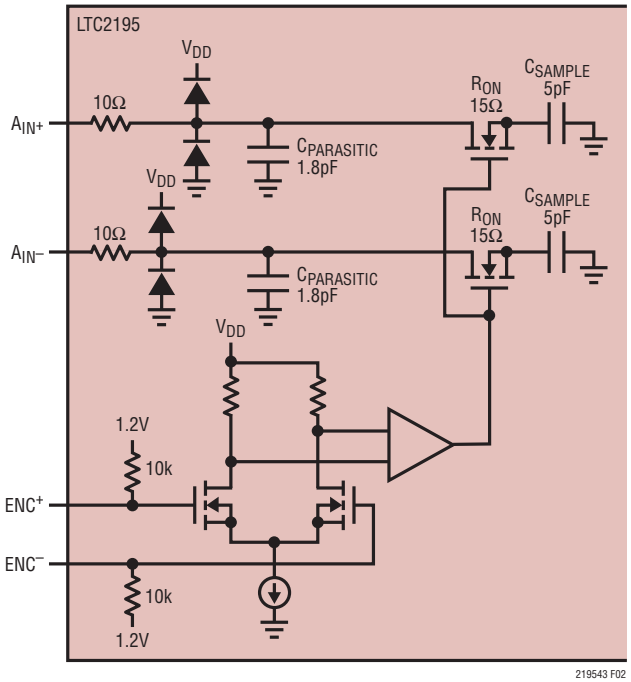


Figure 2. Equivalent Input Circuit. Only One of Two Analog Channels is Shown

APPLICATIONS INFORMATION

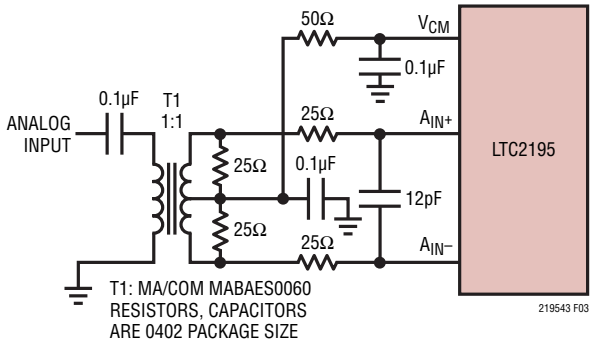


Figure 3. Analog Input Circuit Using a Transformer. Recommended for Input Frequencies from 5MHz to 70MHz

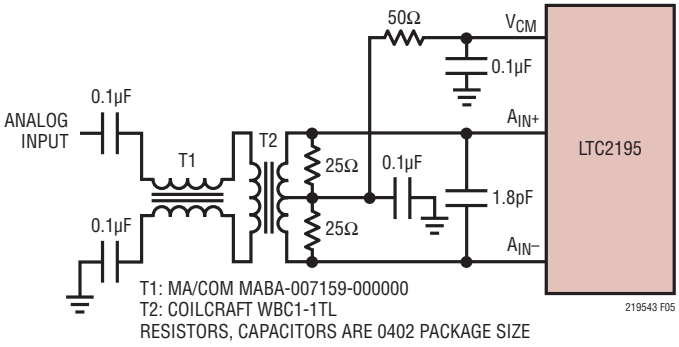


Figure 5. Recommended Front-End Circuit for Input Frequencies from 150MHz to 250MHz

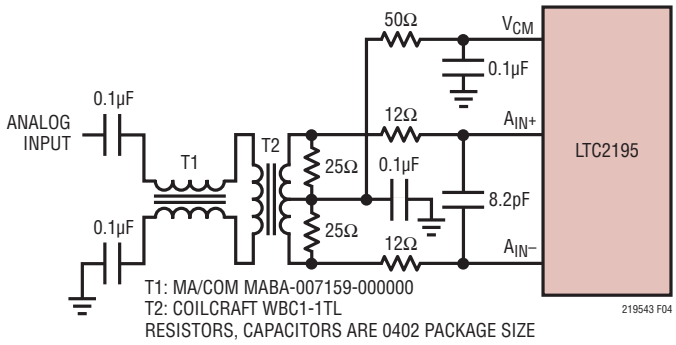


Figure 4. Recommended Front-End Circuit for Input Frequencies from 5MHz to 150MHz

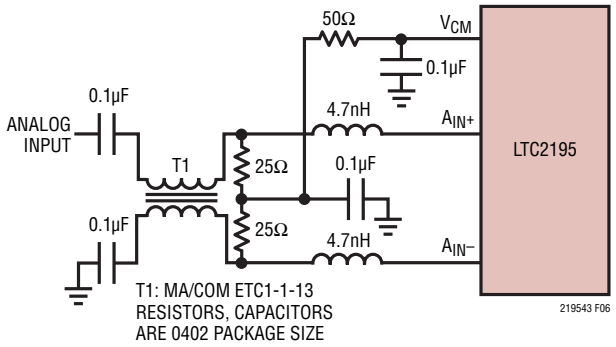


Figure 6. Recommended Front-End Circuit for Input Frequencies Above 250MHz

tap is biased with V_{CM}, setting the A/D input at its optimal DC level. At higher input frequencies a transmission line balun transformer (Figures 4 to 6) has better balance, resulting in lower A/D distortion.

Amplifier Circuits

Figure 7 shows the analog input being driven by a high speed differential amplifier. The output of the amplifier is AC coupled to the A/D so the amplifier's output common mode voltage can be optimally set to minimize distortion.

At very high frequencies an RF gain block will often have lower distortion than a differential amplifier. If the gain block is single ended, then a transformer circuit (Figures 4 to 6) should convert the signal to differential before driving the A/D.

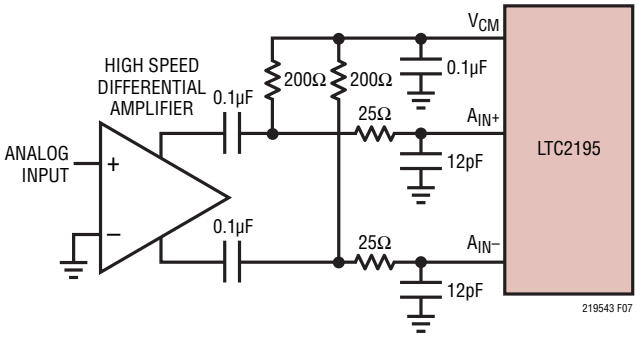


Figure 7. Front-End Circuit Using a High Speed Differential Amplifier

APPLICATIONS INFORMATION

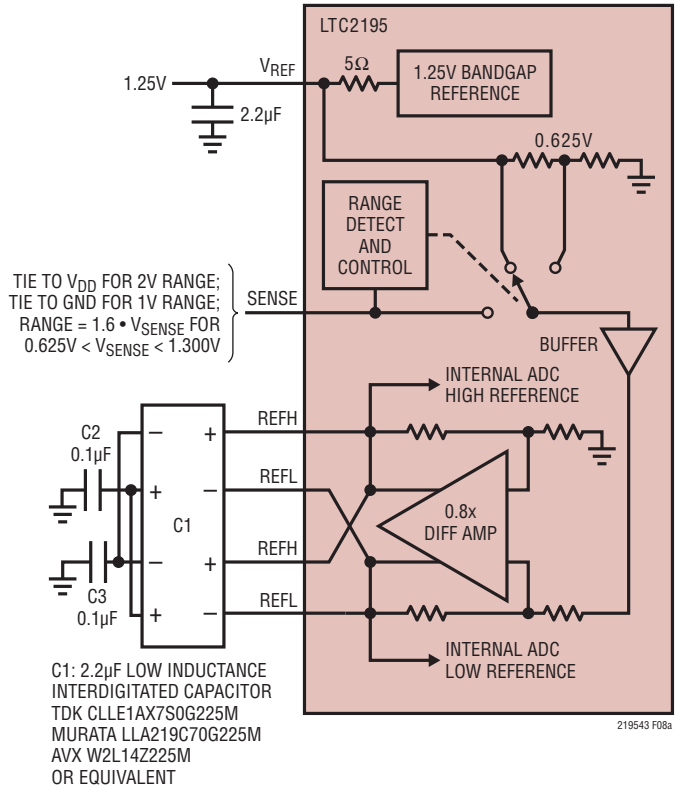
Reference

The LTC2195/LTC2194/LTC2193 have an internal 1.25V voltage reference. For a 2V input range using the internal reference, connect SENSE to V_{DD}. For a 1V input range using the internal reference, connect SENSE to ground. For a 2V input range with an external reference, apply a 1.25V reference voltage to SENSE (Figure 9).

The input range can be adjusted by applying a voltage to SENSE that is between 0.625V and 1.30V. The input range will then be 1.6 • V_{SENSE}.

The V_{REF}, REFH and REFL pins should be bypassed as shown in Figure 8. A low inductance 2.2µF interdigitated capacitor is recommended for the bypass between REFH and REFL. This type of capacitor is available at a low cost from multiple suppliers.

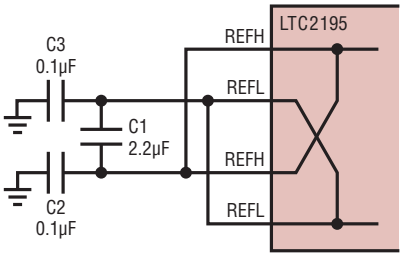
At sample rates below 110Msps an interdigitated capacitor is not necessary for good performance and C1 can be replaced by a standard 2.2µF capacitor between REFH and REFL. The capacitors should be as close to the pins as possible (not on the back side of the circuit board).



C1: 2.2µF LOW INDUCTANCE
INTERDIGITATED CAPACITOR
TDK CLLE1AX7S0G225M
MURATA LLA219C70G225M
AVX W2L14Z225M
OR EQUIVALENT

Figure 8a. Reference Circuit

Figure 8c and 8d show the recommended circuit board layout for the REFH/REFL bypass capacitors. Note that in Figure 8c, every pin of the interdigitated capacitor (C1) is connected since the pins are not internally connected in some vendors' capacitors. In Figure 8d the REFH and REFL pins are connected by short jumpers in an internal layer. To minimize the inductance of these jumpers they can be placed in a small hole in the GND plane on the second board layer.



CAPACITORS ARE 0402 PACKAGE SIZE

Figure 8b. Alternative REFH/REFL Bypass Circuit

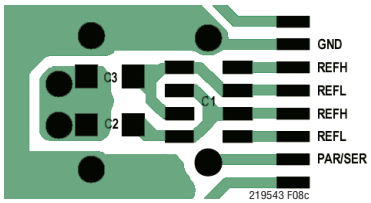


Figure 8c. Recommended Layout for the REFH/REFL Bypass Circuit in Figure 8a

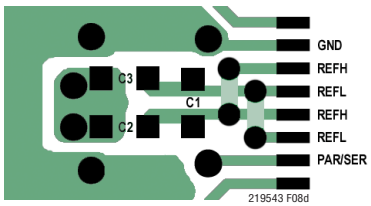


Figure 8d. Recommended Layout for the REFH/REFL Bypass Circuit in Figure 8b

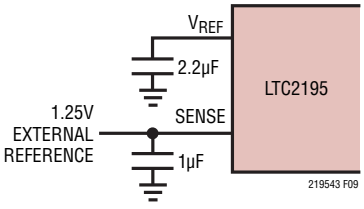


Figure 9. Using an External 1.25V Reference

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Encode Input

The signal quality of the encode inputs strongly affects the A/D noise performance. The encode inputs should be treated as analog signals—do not route them next to digital traces on the circuit board. There are two modes of operation for the encode inputs: the differential encode mode (Figure 10), and the single-ended encode mode (Figure 11).

The differential encode mode is recommended for sinusoidal, PECL, or LVDS encode inputs (Figures 12, 13). The encode inputs are internally biased to 1.2V through 10k equivalent resistance. The encode inputs can be taken above V_{DD} (up to 3.6V), and the common mode range is from 1.1V to 1.6V. In the differential encode mode, ENC$^-$ should stay at least 200mV above ground to avoid falsely triggering the single-ended encode mode. For good jitter performance ENC$^+$ should have fast rise and fall times.

The single-ended encode mode should be used with CMOS encode inputs. To select this mode, ENC$^-$ is connected to ground and ENC$^+$ is driven with a square wave

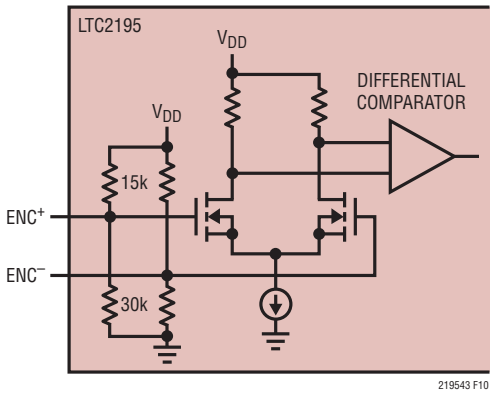


Figure 10. Equivalent Encode Input Circuit for Differential Encode Mode

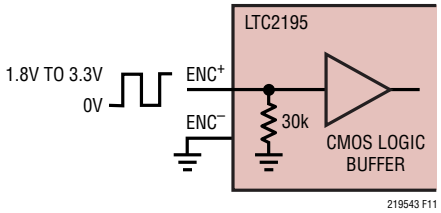


Figure 11. Equivalent Encode Input Circuit for Single-Ended Encode Mode

encode input. ENC$^+$ can be taken above V_{DD} (up to 3.6V) so 1.8V to 3.3V CMOS logic levels can be used. The ENC$^+$ threshold is 0.9V. For good jitter performance ENC$^+$ should have fast rise and fall times. If the encode signal is turned off or drops below approximately 500kHz, the A/D enters nap mode.

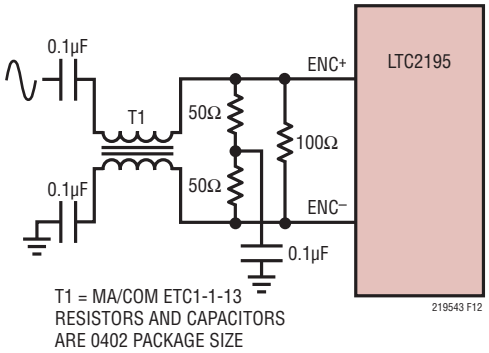


Figure 12. Sinusoidal Encode Drive

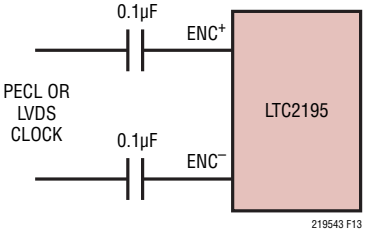


Figure 13. PECL or LVDS Encode Drive

Clock PLL and Duty Cycle Stabilizer

The encode clock is multiplied by an internal phase-locked loop (PLL) to generate the serial digital output data. If the encode signal changes frequency or is turned off, the PLL requires 25µs to lock onto the input clock.

A clock duty cycle stabilizer circuit allows the duty cycle of the applied encode signal to vary from 30% to 70%. In the serial programming mode it is possible to disable the duty cycle stabilizer, but this is not recommended. In the parallel programming mode the duty cycle stabilizer is always enabled.

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DIGITAL OUTPUTS

The digital outputs of the LTC2195/LTC2194/LTC2193 are serialized LVDS signals. Each channel outputs two bits at a time (2-lane mode) or four bits at a time (4-lane mode). At lower sampling rates there is a one bit per channel option (1-lane mode). Please refer to the Timing Diagrams for details. In 4-lane mode the clock duty cycle stabilizer must be enabled.

The output data should be latched on the rising and falling edges of the data clock out (DCO). A data frame output (FR) can be used to determine when the data from a new conversion result begins.

The maximum serial data rate for the data outputs is 1Gbps, so the maximum sample rate of the ADC will depend on the serialization mode as well as the speed grade of the ADC (See Table 1). The minimum sample rate for all serialization modes is 5Msps.

By default the outputs are standard LVDS levels: 3.5mA output current and a 1.25V output common mode voltage. An external 100Ω differential termination resistor is required for each LVDS output pair. The termination resistors should be located as close as possible to the LVDS receiver.

The outputs are powered by OVDD and OGND which are isolated from the A/D core power and ground.

Table 1. Maximum Sampling Frequency for All Serialization Modes. Note That These Limits are for the LTC2195. The Sampling Frequency for the Slower Speed Grades Cannot Exceed 105MHz (LTC2194) or 80MHz (LTC2193).

SERIALIZATION MODE	MAXIMUM SAMPLING FREQUENCY, f_S (MHz)	DCO FREQUENCY	FR FREQUENCY	SERIAL DATA RATE
4-Lane	125	2 • f_S	f_S	4 • f_S
2-Lane	125	4 • f_S	f_S	8 • f_S
1-Lane	62.5	8 • f_S	f_S	16 • f_S

Programmable LVDS Output Current

In LVDS mode, the default output driver current is 3.5mA. This current can be adjusted by control register A2 in the serial programming mode. Available current levels are 1.75mA, 2.1mA, 2.5mA, 3mA, 3.5mA, 4mA and 4.5mA. In the parallel programming mode the SDO pin can select either 3.5mA or 1.75mA.

Optional LVDS Driver Internal Termination

In most cases using just an external 100Ω termination resistor will give excellent LVDS signal integrity. In addition, an optional internal 100Ω termination resistor can be enabled by serially programming mode control register A2. The internal termination helps absorb any reflections caused by imperfect termination at the receiver. When the internal termination is enabled, the output driver current is doubled to maintain the same output voltage swing. Internal termination can only be selected in serial programming mode.

DATA FORMAT

Table 2 shows the relationship between the analog input voltage and the digital data output bits. By default the output data format is offset binary. The 2's complement format can be selected by serially programming mode control register A1.

Table 2. Output Codes vs Input Voltage

A_{IN}^+-A_{IN}^- (2V RANGE)	D15-D0 (OFFSET BINARY)	D15-D0 (2's COMPLEMENT)
>1.000000V	1111 1111 1111 1111	0111 1111 1111 1111
+0.999970V	1111 1111 1111 1111	0111 1111 1111 1111
+0.999939V	1111 1111 1111 1110	0111 1111 1111 1110
+0.000030V	1000 0000 0000 0001	0000 0000 0000 0001
+0.000000V	1000 0000 0000 0000	0000 0000 0000 0000
–0.000030V	0111 1111 1111 1111	1111 1111 1111 1111
–0.000061V	0111 1111 1111 1110	1111 1111 1111 1110
–0.999939V	0000 0000 0000 0001	1000 0000 0000 0001
–1.000000V	0000 0000 0000 0000	1000 0000 0000 0000
<–1.000000V	0000 0000 0000 0000	1000 0000 0000 0000

Digital Output Randomizer

Interference from the A/D digital outputs is sometimes unavoidable. Digital interference may be from capacitive or inductive coupling or coupling through the ground plane. Even a tiny coupling factor can cause unwanted tones in the ADC output spectrum. By randomizing the digital output before it is transmitted off-chip, these unwanted tones can be randomized which reduces the unwanted tone amplitude.

The digital output is randomized by applying an exclusive OR logic operation between the LSB and all other data output bits. To decode, the reverse operation is

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applied—an exclusive OR operation is applied between the LSB and all other bits. The FR and DCO outputs are not affected. The output randomizer is enabled by serially programming mode control register A1.

Digital Output Test Pattern

To allow in-circuit testing of the digital interface to the A/D, there is a test mode that forces the A/D data outputs (D15-D0) of both channels to known values. The digital output test patterns are enabled by serially programming mode control registers A2, A3 and A4. When enabled, the test patterns override all other formatting modes: 2's complement and randomizer.

Output Disable

The digital outputs may be disabled by serially programming mode control register A2. The current drive for all digital outputs including DCO and FR are disabled to save power or enable in-circuit testing. When disabled the common mode of each output pair becomes high impedance, but the differential impedance may remain low.

Sleep and Nap Modes

The A/D may be placed in sleep or nap modes to conserve power. In sleep mode the entire device is powered down, resulting in 1mW power consumption. Sleep mode is enabled by mode control register A1 (serial programming mode), or by SDI (parallel programming mode). The amount of time required to recover from sleep mode depends on the size of the bypass capacitors on V_{REF}, REFH and REFL. For the suggested values in Figure 8, the A/D will stabilize after 2ms.

In nap mode any combination of A/D channels can be powered down while the internal reference circuits and the PLL stay active, allowing faster wake up than from sleep mode. Recovering from nap mode requires at least 100 clock cycles. If the application demands very accurate DC settling then an additional 50µs should be allowed so the on-chip references can settle from the slight temperature shift caused by the change in supply current as the A/D leaves nap mode. Nap mode is enabled by mode control register A1 in the serial programming mode.

DEVICE PROGRAMMING MODES

The operating modes of the LTC2195/LTC2194/LTC2193 can be programmed by either a parallel interface or a simple serial interface. The serial interface has more flexibility and can program all available modes. The parallel interface is more limited and can only program some of the more commonly used modes.

Parallel Programming Mode

To use the parallel programming mode, PAR/$\overline{SER}$ should be tied to V_{DD}. The $\overline{CS}$, SCK, SDI and SDO pins are binary logic inputs that set certain operating modes. These pins can be tied to V_{DD} or ground, or driven by 1.8V, 2.5V or 3.3V CMOS logic. When used as an input, SDO should be driven through a 1k series resistor. Table 3 shows the modes set by $\overline{CS}$, SCK, SDI and SDO.

Table 3. Parallel Programming Mode Control Bits (PAR/$\overline{SER}$ = V_{DD})

PIN	DESCRIPTION
$\overline{CS}$/SCK	**2-Lane/4-Lane/1-Lane Selection Bits** 00 = 2-Lane Output Mode 01 = 4-Lane Output Mode 10 = 1-Lane Output Mode 11 = Not Used
SDI	**Power Down Control Bit** 0 = Normal Operation 1 = Sleep Mode
SDO	**LVDS Current Selection Bit** 0 = 3.5mA LVDS Current Mode 1 = 1.75mA LVDS Current Mode

Serial Programming Mode

To use the serial programming mode, PAR/$\overline{SER}$ should be tied to ground. The $\overline{CS}$, SCK, SDI and SDO pins become a serial interface that program the A/D mode control registers. Data is written to a register with a 16-bit serial word. Data can also be read back from a register to verify its contents.

Serial data transfer starts when $\overline{CS}$ is taken low. The data on the SDI pin is latched at the first 16 rising edges of SCK. Any SCK rising edges after the first 16 are ignored. The data transfer ends when $\overline{CS}$ is taken high again.

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The first bit of the 16-bit input word is the R/$\overline{W}$ bit. The next seven bits are the address of the register (A6:A0). The final eight bits are the register data (D7:D0).

If the R/$\overline{W}$ bit is low, the serial data (D7:D0) will be written to the register set by the address bits (A6:A0). If the R/$\overline{W}$ bit is high, data in the register set by the address bits (A6:A0) will be read back on the SDO pin (see the Timing Diagrams). During a read back command the register is not updated and data on SDI is ignored.

The SDO pin is an open-drain output that pulls to ground with a 200Ω impedance. If register data is read back through SDO, an external 2k pull-up resistor is required. If serial data is only written and read back is not needed, then SDO can be left floating and no pull-up resistor is needed.

Table 4 shows a map of the mode control registers.

Software Reset

If serial programming is used, the mode control registers should be programmed as soon as possible after the power supplies turn on and are stable. The first serial command must be a software reset which will reset all register data bits to logic 0. To perform a software reset, bit D7 in the reset register is written with a logic 1. After the reset SPI write command is complete, bit D7 is automatically set back to zero.

Table 4. Serial Programming Mode Register Map (PAR/$\overline{SER}$ = GND)

REGISTER A0: RESET REGISTER (ADDRESS 00h)

D7	D6	D5	D4	D3	D2	D1	D0
RESET	X	X	X	X	X	X	X

Bit 7 **RESET** Software Reset Bit

0 = Not Used
1 = Software Reset. All Mode Control Registers are Reset to 00h. The ADC is Momentarily Placed in Sleep Mode. This Bit is Automatically Set Back to Zero at the End of the SPI Write Command. The Reset Register Is Write Only. Data Read Back from the Reset Register Will Be Random

Bits 6-0 Unused, Don't Care Bits.

REGISTER A1: FORMAT AND POWER-DOWN REGISTER (ADDRESS 01h)

D7	D6	D5	D4	D3	D2	D1	D0
DCSOFF	RAND	TWOSCOMP	SLEEP	NAP_2	X	X	NAP_1

Bit 7 **DCSOFF** Clock Duty Cycle Stabilizer Bit
0 = Clock Duty Cycle Stabilizer On
1 = Clock Duty Cycle Stabilizer Off. This is not recommended.

Bit 6 **RAND** Data Output Randomizer Mode Control Bit
0 = Data Output Randomizer Mode Off
1 = Data Output Randomizer Mode On

Bit 5 **TWOSCOMP** Two's Complement Mode Control Bit
0 = Offset Binary Data Format
1 = Two's Complement Data Format

Bits 4, 3, 0 **SLEEP:NAP_2:NAP_1** Sleep/Nap Mode Control Bits
000 = Normal Operation
0X1 = Channel 1 in Nap Mode
01X = Channel 2 in Nap Mode
1XX = Sleep Mode. Both Channels are Disabled.
Note: Any Combination of Channels Can Be Placed in Nap Mode

Bits 1, 2 Unused, Don't Care Bits

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REGISTER A2: OUTPUT MODE REGISTER (ADDRESS 02h)

D7	D6	D5	D4	D3	D2	D1	D0
ILVDS2	ILVDS1	ILVDS0	TERMON	OUTOFF	OUTTEST	OUTMODE1	OUTMODE0

Bits 7-5 **ILVDS2:ILVDS0** LVDS Output Current Bits
000 = 3.5mA LVDS Output Driver Current
001 = 4.0mA LVDS Output Driver Current
010 = 4.5mA LVDS Output Driver Current
011 = Not Used
100 = 3.0mA LVDS Output Driver Current
101 = 2.5mA LVDS Output Driver Current
110 = 2.1mA LVDS Output Driver Current
111 = 1.75mA LVDS Output Driver Current

Bit 4 **TERMON** LVDS Internal Termination Bit
0 = Internal Termination Off
1 = Internal Termination On. LVDS Output Driver Current is 2× the Current Set by ILVDS2:ILVDS0

Bit 3 **OUTOFF** Output Disable Bit
0 = Digital Outputs are Enabled
1 = Digital Outputs are Disabled

Bit 2 **OUTTEST** Digital Output Test Pattern Control Bit
0 = Digital Output Test Pattern Off
1 = Digital Output Test Pattern On

Bits 1-0 **OUTMODE1:OUTMODE0** Digital Output Mode Control Bits
00 = 2-Lane Output Mode
01 = 4-Lane Output Mode
10 = 1-Lane Output Mode
11 = Not Used

REGISTER A3: TEST PATTERN MSB REGISTER (ADDRESS 03h)

D7	D6	D5	D4	D3	D2	D1	D0
TP15	TP14	TP13	TP12	TP11	TP10	TP9	TP8

Bits 7-0 **TP15:TP8** Test Pattern Data Bits (MSB)
TP15:TP8 Set the Test Pattern for Data Bit 15 (MSB) Through Data Bit 8.

REGISTER A4: TEST PATTERN LSB REGISTER (ADDRESS 04h)

D7	D6	D5	D4	D3	D2	D1	D0
TP7	TP6	TP5	TP4	TP3	TP2	TP1	TP0

Bits 7-0 **TP7:TP0** Test Pattern Data Bits (LSB)
TP7:TP0 Set the Test Pattern for Data Bit 7 Through Data Bit 0 (LSB).

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GROUNDING AND BYPASSING

The LTC2195/LTC2194/LTC2193 require a printed circuit board with a clean unbroken ground plane. A multilayer board with an internal ground plane in the first layer beneath the ADC is recommended. Layout for the printed circuit board should ensure that digital and analog signal lines are separated as much as possible. In particular, care should be taken not to run any digital track alongside an analog signal track or underneath the ADC.

High quality ceramic bypass capacitors should be used at the V_{DD}, OV_{DD}, V_{CM}, V_{REF}, REFH and REFL pins. Bypass capacitors must be located as close to the pins as possible. Size 0402 ceramic capacitors are recommended. The traces connecting the pins and bypass capacitors must be kept short and should be made as wide as possible.

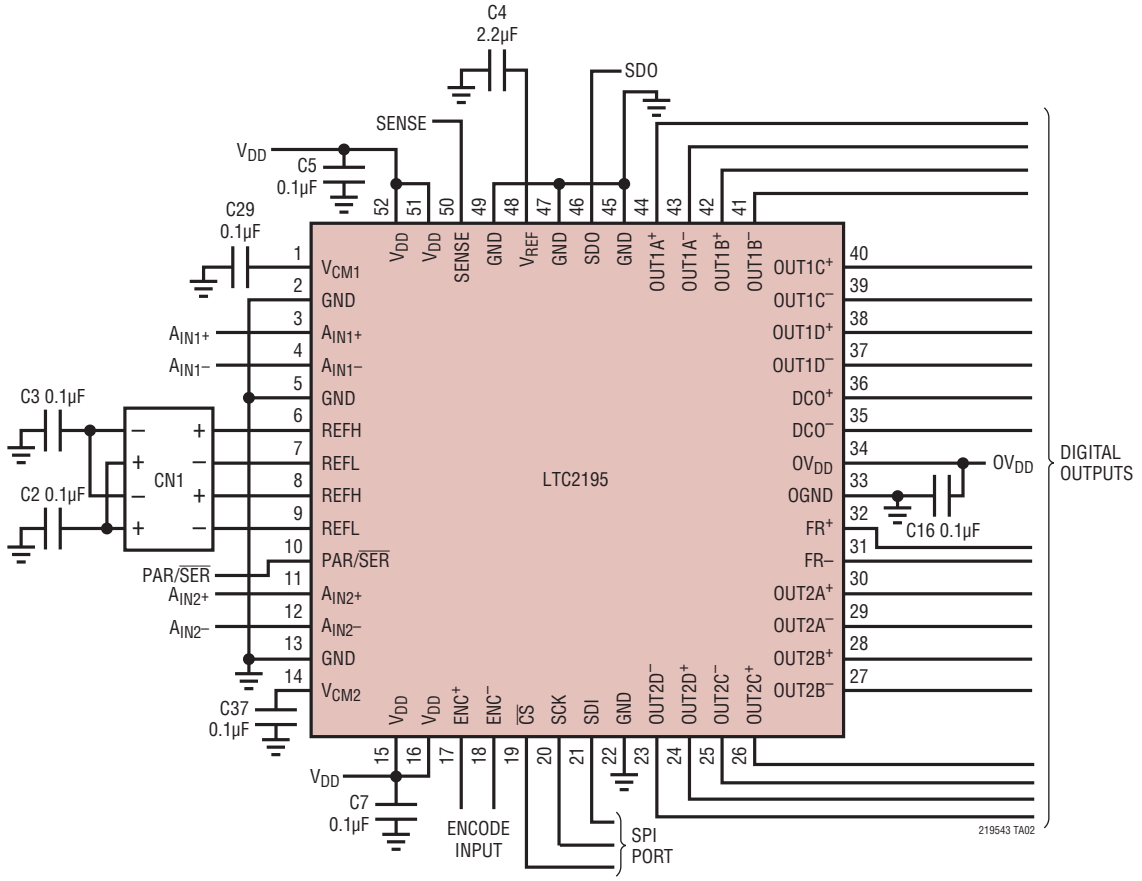
Of particular importance is the capacitor between REFH and REFL. This capacitor should be on the same side of the circuit board as the A/D, and as close to the device as possible. A low inductance interdigitated capacitor is suggested for REFH/REFL if the sampling frequency is greater than 110Msps.

The analog inputs, encode signals, and digital outputs should not be routed next to each other. Ground fill and grounded vias should be used as barriers to isolate these signals from each other.

HEAT TRANSFER

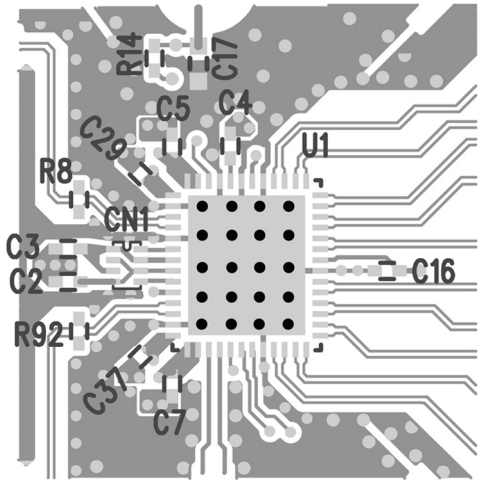
Most of the heat generated by the LTC2195/LTC2194/LTC2193 is transferred from the die through the bottom-side exposed pad and package leads onto the printed circuit board. For good electrical and thermal performance, the exposed pad must be soldered to a large grounded pad on the PC board. This pad should be connected to the internal ground planes by an array of vias.

TYPICAL APPLICATIONS

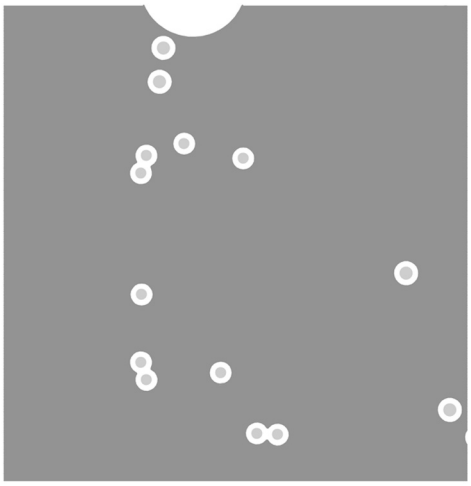


TYPICAL APPLICATIONS

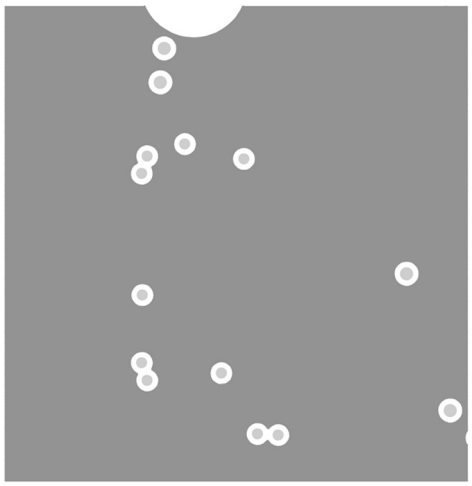
Top Side



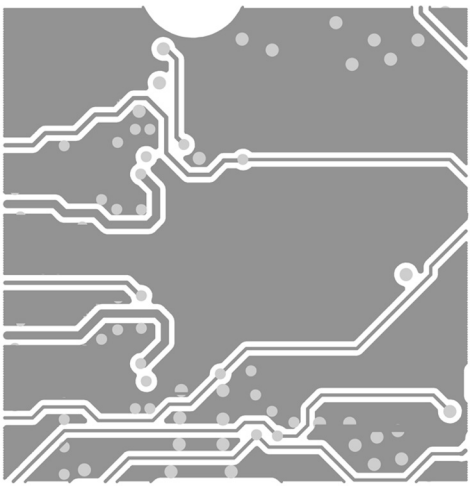
Inner Layer 2



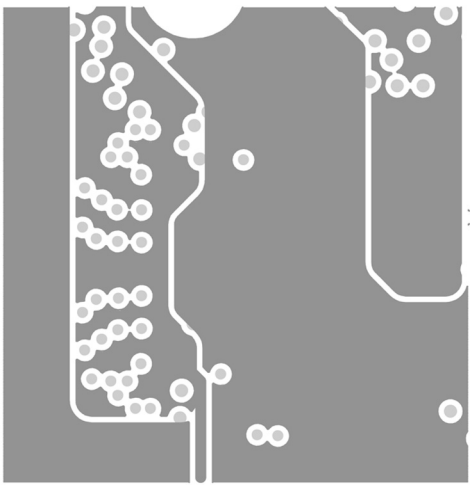
Inner Layer 3



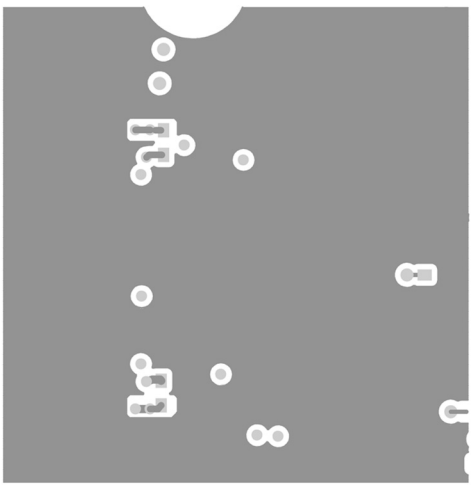
Inner Layer 4



Inner Layer 5

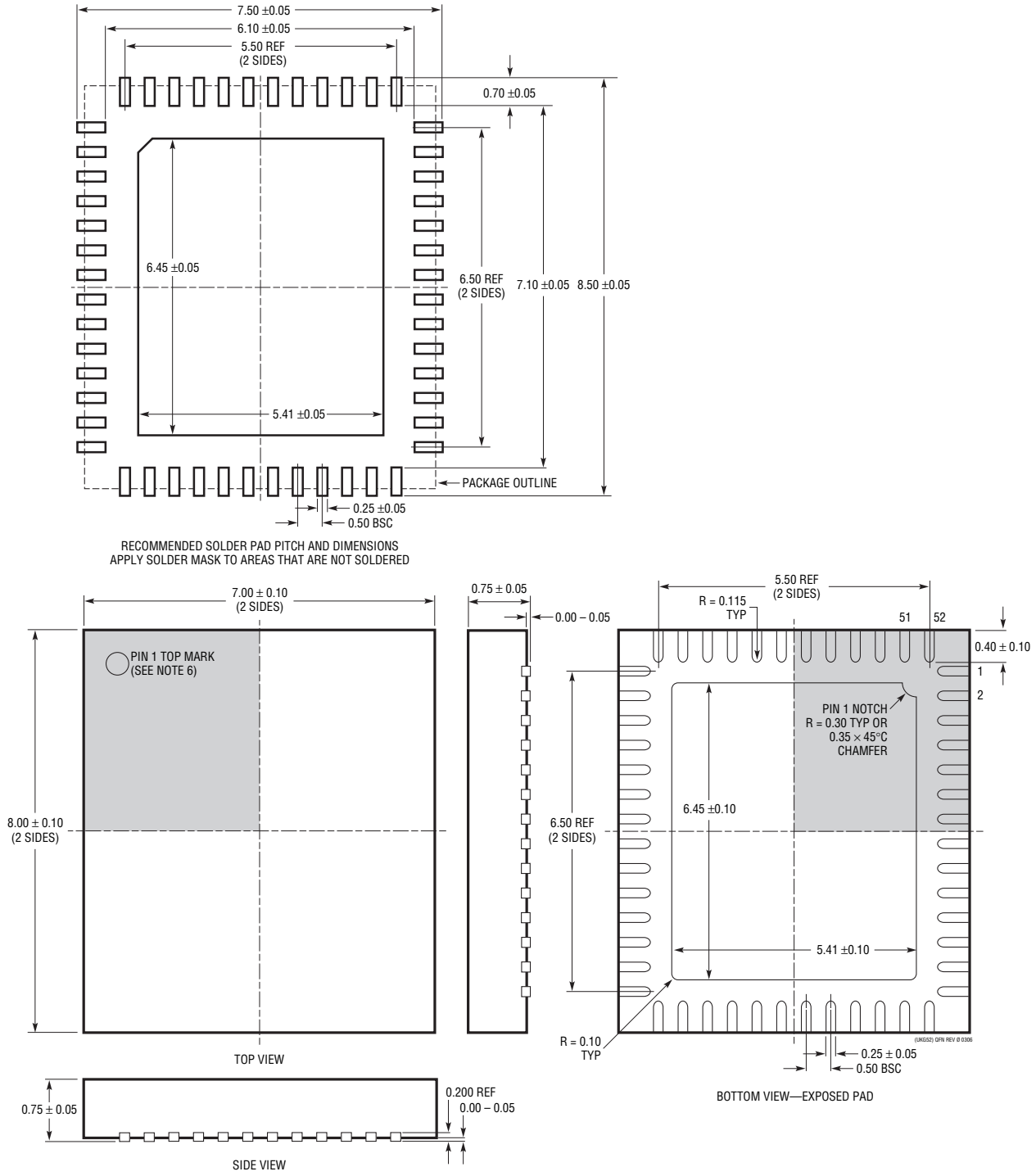


Bottom Side



PACKAGE DESCRIPTION

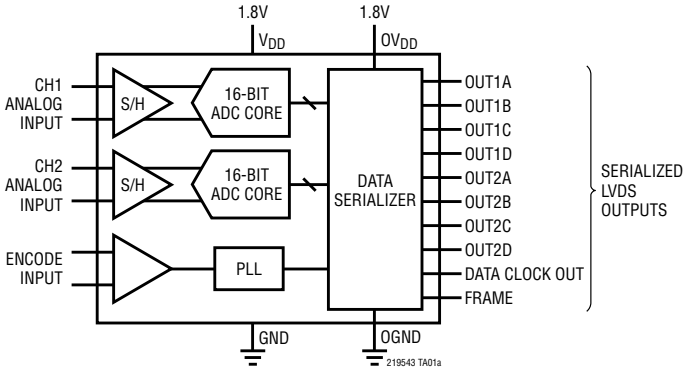
UKG Package
52-Lead Plastic QFN (7mm × 8mm)
(Reference LTC DWG # 05-08-1729 Rev Ø)



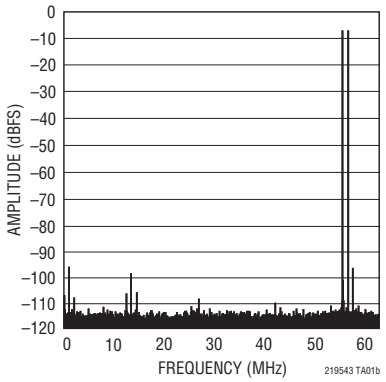
NOTE:
1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE, IF PRESENT
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

TYPICAL APPLICATION



2-Tone FFT, f_{IN} = 70MHz and 69MHz



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
ADCs		
LTC2259-14/LTC2260-14/ LTC2261-14	14-Bit, 80Msps/105Msps/125Msps 1.8V ADCs, Ultralow Power	89mW/106mW/127mW, 73.4dB SNR, 85dB SFDR, DDR LVDS/DDR CMOS/CMOS Outputs, 6mm × 6mm QFN-40
LTC2262-14	14-Bit, 150Msps 1.8V ADC, Ultralow Power	149mW, 72.8dB SNR, 88dB SFDR, DDR LVDS/DDR CMOS/CMOS Outputs, 6mm × 6mm QFN-40
LTC2266-14/LTC2267-14/ LTC2268-14	14-Bit, 80Msps/105Msps/125Msps 1.8V Dual ADCs, Ultralow Power	216mW/250mW/293mW, 73.4dB SNR, 85dB SFDR, Serial LVDS Outputs, 6mm × 6mm QFN-40
LTC2266-12/LTC2267-12/ LTC2268-12	12-Bit, 80Msps/105Msps/125Msps 1.8V VDual ADCs, Ultralow Power	216mW/250mW/293mW, 70.5dB SNR, 85dB SFDR, Serial LVDS Outputs, 6mm × 6mm QFN-40
LTC2208	16-Bit, 130Msps 3.3V ADC	1250mW, 77.7dB SNR, 100dB SFDR, CMOS/LVDS Outputs, 9mm × 9mm QFN-64
LTC2207/LTC2206	16-Bit, 105Msps/80Msps 3.3V ADCs	900mW/725mW, 77.9dB SNR, 100dB SFDR, CMOS Outputs, 7mm × 7mm QFN-48
LTC2217/LTC2216	16-Bit, 105Msps/80Msps 3.3V ADCs	1190mW/970mW, 81.2dB SNR, 100dB SFDR, CMOS/LVDS Outputs, 9mm × 9mm QFN-64
RF Mixers/Demodulators		
LTC5517	40MHz to 900MHz Direct Conversion Quadrature Demodulator	High IIP3: 21dBm at 800MHz, Integrated LO Quadrature Generator
LTC5527	400MHz to 3.7GHz High Linearity Downconverting Mixer	24.5dBm IIP3 at 900MHz, 23.5dBm IIP3 at 3.5GHz, NF = 12.5dB, 50Ω Single-Ended RF and LO Ports
LTC5557	400MHz to 3.8GHz High Linearity Downconverting Mixer	23.7dBm IIP3 at 2.6GHz, 23.5dBm IIP3 at 3.5GHz, NF = 13.2dB, 3.3V Supply Operation, Integrated Transformer
LTC5575	800MHz to 2.7GHz Direct Conversion Quadrature Demodulator	High IIP3: 28dBm at 900MHz, Integrated LO Quadrature Generator, Integrated RF and LO Transformer
Amplifiers/Filters		
LTC6412	800MHz, 31dB Range, Analog-Controlled Variable Gain Amplifier	Continuously Adjustable Gain Control, 35dBm OIP3 at 240MHz, 10dB Noise Figure, 4mm × 4mm QFN-24
LTC6420-20	1.8GHz Dual Low Noise, Low Distortion Differential ADC Drivers for 300MHz IF	Fixed Gain 10V/V, 1nV/√Hz Total Input Noise, 80mA Supply Current per Amplifier, 3mm × 4mm QFN-20
LTC6421-20	1.3GHz Dual Low Noise, Low Distortion Differential ADC Drivers	Fixed Gain 10V/V, 1nV/√Hz Total Input Noise, 40mA Supply Current per Amplifier, 3mm × 4mm QFN-20
LTC6605-7/LTC6605-10/ LTC6605-14	Dual Matched 7MHz/10MHz/14MHz Filters with ADC Drivers	Dual Matched 2nd Order Lowpass Filters with Differential Drivers, Pin-Programmable Gain, 6mm × 3mm DFN-22
Signal Chain Receivers		
LTM9002	14-Bit Dual Channel IF/Baseband Receiver Subsystem	Integrated High Speed ADC, Passive Filters and Fixed Gain Differential Amplifiers

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408) 432-1900 • FAX: (408) 434-0507 • www.linear.com
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