Constant Frequency Current Mode Step-Down DC/DC Controller in SOT-23

FEATURES

- **High Efficiency: Up to 94%**
- **High Output Currents Easily Achieved**
- **Wide V_{IN} Range: 2.5V to 9.8V**
- **Constant Frequency 550kHz Operation**
- **Burst Mode® Operation at Light Load**
- **Low Dropout: 100% Duty Cycle**
- **Tiny 6-Lead SOT-23 Package**
- 0.8V Reference Allows Low Output Voltages
- Current Mode Operation for Excellent Line and Load Transient Response
- Low Quiescent Current: 270µA
- Shutdown Mode Draws Only 8µA Supply Current
- ±2.5% Reference Accuracy

APPLICATIONS

- One or Two Lithium-Ion-Powered Applications
- Cellular Telephones
- Wireless Modems
- Portable Computers
- Distributed 3.3V, 2.5V or 1.8V Power Systems
- Scanners

DESCRIPTION

The LTC®1772 is a constant frequency current mode step-down DC/DC controller providing excellent AC and DC load and line regulation. The device incorporates an accurate undervoltage lockout feature that shuts down the LTC1772 when the input voltage falls below 2.0V.

The LTC1772 provides a ±2.5% output voltage accuracy and consumes only 270µA of quiescent current. For applications where efficiency is a prime consideration, the LTC1772 is configured for Burst Mode operation, which enhances efficiency at low output current.

To further maximize the life of a battery source, the external P-channel MOSFET is turned on continuously in dropout (100%dutycycle).In shutdown, the device draws a mere 8µA. High constant operating frequency of 550kHz allows the use of a small external inductor.

The LTC1772 is available in a small footprint 6-lead SOT-23.

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Burst Mode is a registered trademark of Linear Technology Corporation.
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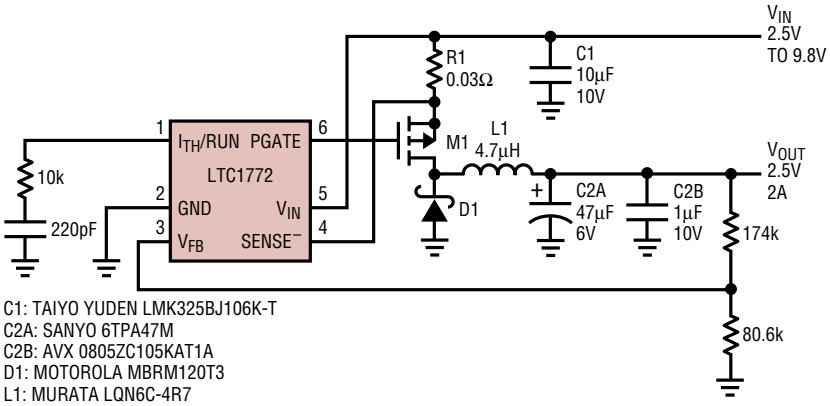
TYPICAL APPLICATION



C1: TAIYO YUDEN LMK325BJ106K-T
C2A: SANYO 6TPA47M
C2B: AVX 0805ZC105KAT1A
D1: MOTOROLA MBRM120T3
L1: MURATA LQN6C-4R7
M1: FAIRCHILD FDC638P
R1: IRC LRC-LR1206-01-R030F

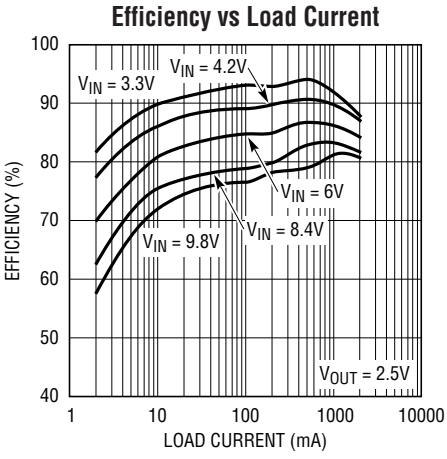


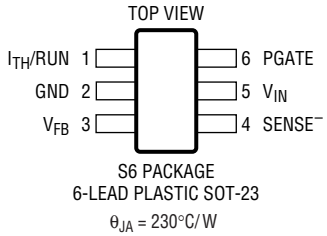
Figure 1. High Efficiency, High Output Current 2.5V/2A Regulator

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Input Supply Voltage (V_{IN}) ..... –0.3V to 10V
SENSE⁻, PGATE Voltages ..... –0.3V to (V_{IN} + 0.3V)
V_{FB}, I_{TH} /RUN Voltages ..... –0.3V to 2.4V
PGATE Peak Output Current (<10µs) 1A
Storage Ambient Temperature Range ... –65°C to 150°C
Operating Temperature Range
LTC1772CS6 ..... 0°C to 70°C
LTC1772ES6 (Note 2) ..... –40°C to 85°C
LTC1772IS6 (Note 2) ..... –40°C to 85°C
LTC1772HS6 (Notes 2,3) ..... –40°C to 140°C
Junction Temperature (Note 3) ..... 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



S6 PACKAGE
6-LEAD PLASTIC SOT-23
θ_{JA} = 230°C/W

ORDER PART NUMBER
LTC1772CS6 LTC1772ES6 LTC1772IS6 LTC1772HS6
S6 PART MARKING
LTIL LTIM LTB7 LTBRY

Order Options Tape and Reel: Add #TR
Lead Free: Add #PBF Lead Free Tape and Reel: Add #TRPBF
Lead Free Part Marking: http://www.linear.com/leadfree/

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes specifications that apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 4.2V unless otherwise specified. (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input DC Supply Current	Typicals at V_{IN} = 4.2V (Note 4)					
Normal Operation	2.4V ≤ V_{IN} ≤ 9.8V			270	420	µA
Sleep Mode	2.4V ≤ V_{IN} ≤ 9.8V			230	370	µA
Shutdown	2.4V ≤ V_{IN} ≤ 9.8V, V_{ITH} /RUN = 0V			8	22	µA
UVLO	V_{IN} < UVLO Threshold			6	10	µA
Undervoltage Lockout Threshold	V_{IN} Falling (LTC1772C)	●	1.60	2.00	2.30	V
	V_{IN} Falling (LTC1772E, LTC1772I, LTC1772H)	●	1.55	2.00	2.35	V
	V_{IN} Rising		1.85	2.10	2.40	V
Shutdown Threshold (at I_{TH} /RUN)	(LTC1772C)	●	0.20	0.35	0.50	V
	(LTC1772E, LTC1772I, LTC1772H)	●	0.15	0.35	0.55	V
Start-Up Current Source	V_{ITH}/RUN = 0V		0.25	0.5	0.85	µA
Regulated Feedback Voltage	(Note 5) (LTC1772C)	●	0.780	0.800	0.820	V
	(Note 5) (LTC1772E, LTC1772I, LTC1772H)	●	0.770	0.800	0.830	V
Output Voltage Line Regulation	2.4V ≤ V_{IN} ≤ 9.8V (Note 5)			0.05		mV/V
Output Voltage Load Regulation	I_{TH}/RUN Sinking 5µA (Note 5)			2.5		mV/µA
	I_{TH}/RUN Sourcing 5µA (Note 5)			2.5		mV/µA
V_{FB} Input Current	(Note 5)			10	50	nA
Overvoltage Protect Threshold	Measured at V_{FB}		0.820	0.860	0.895	V
Overvoltage Protect Hysteresis				20		mV
Oscillator Frequency	V_{FB} = 0.8V		500	550	650	kHz
	V_{FB} = 0V			120		kHz
Gate Drive Rise Time	C_{LOAD} = 3000pF			40		ns
Gate Drive Fall Time	C_{LOAD} = 3000pF			40		ns
Peak Current Sense Voltage	(Note 6)			120		mV

ELECTRICAL CHARACTERISTICS

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: The LTC1772E is guaranteed to meet specifications from 0°C to 70°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls. The LTC1772I is guaranteed to meet specified performance from –40°C to 85°C. The LTC1772H is guaranteed to meet specified performance from –40°C to 140°C.

Note 3: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formula:

$T_J = T_A + (P_D \bullet \theta_{JA}°C/W)$

Operation at high junction temperatures degrades operating lifetimes. Operating lifetimes at junction temperatures greater than 125°C is derated to 1000 hours.

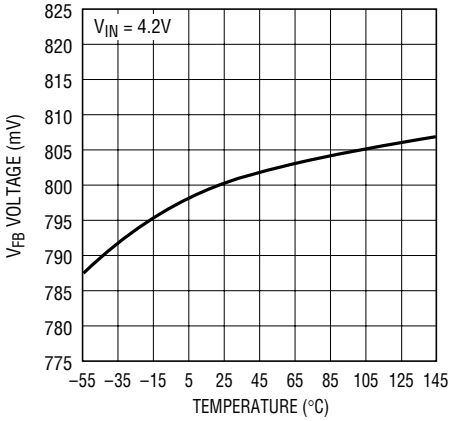
Note 4: Dynamic supply current is higher due to the gate charge being delivered at the switching frequency.

Note 5: The LTC1772 is tested in a feedback loop that servos V_{FB} to the output of the error amplifier.

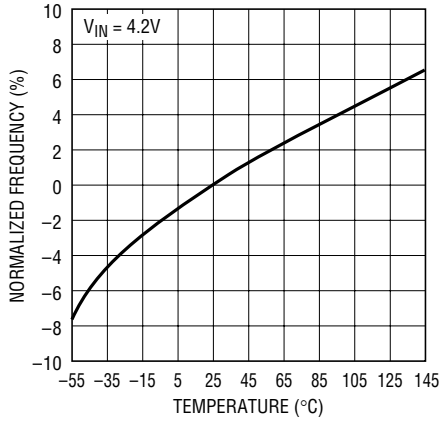
Note 6: Peak current sense voltage is reduced dependent on duty cycle to a percentage of value as given in Figure 2.

TYPICAL PERFORMANCE CHARACTERISTICS

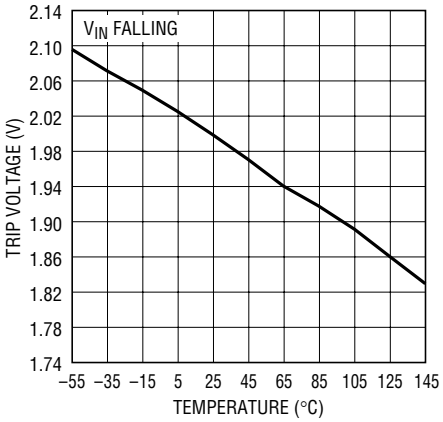
Reference Voltage vs Temperature



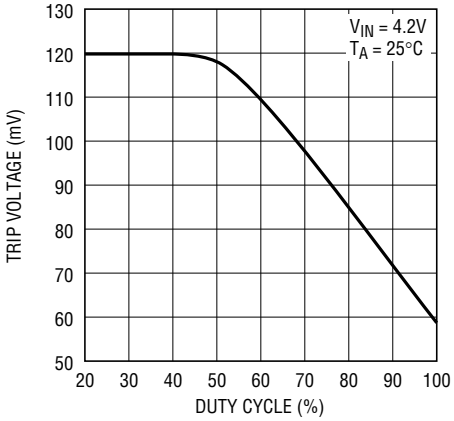
Normalized Frequency vs Temperature



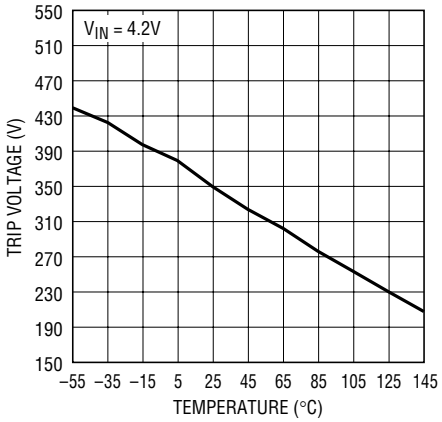
Undervoltage Lockout Trip Voltage vs Temperature



Maximum (V_{IN} – $SENSE^-$) Voltage vs Duty Cycle



Shutdown Threshold vs Temperature



PIN FUNCTIONS

I_{TH}/RUN (Pin 1): This pin performs two functions. It serves as the error amplifier compensation point as well as the run control input. The current comparator threshold increases with this control voltage. Nominal voltage range for this pin is 0.7V to 1.9V. Forcing this pin below 0.35V causes the device to be shut down. In shutdown all functions are disabled and the PGATE pin is held high.

GND (Pin 2): Ground Pin.

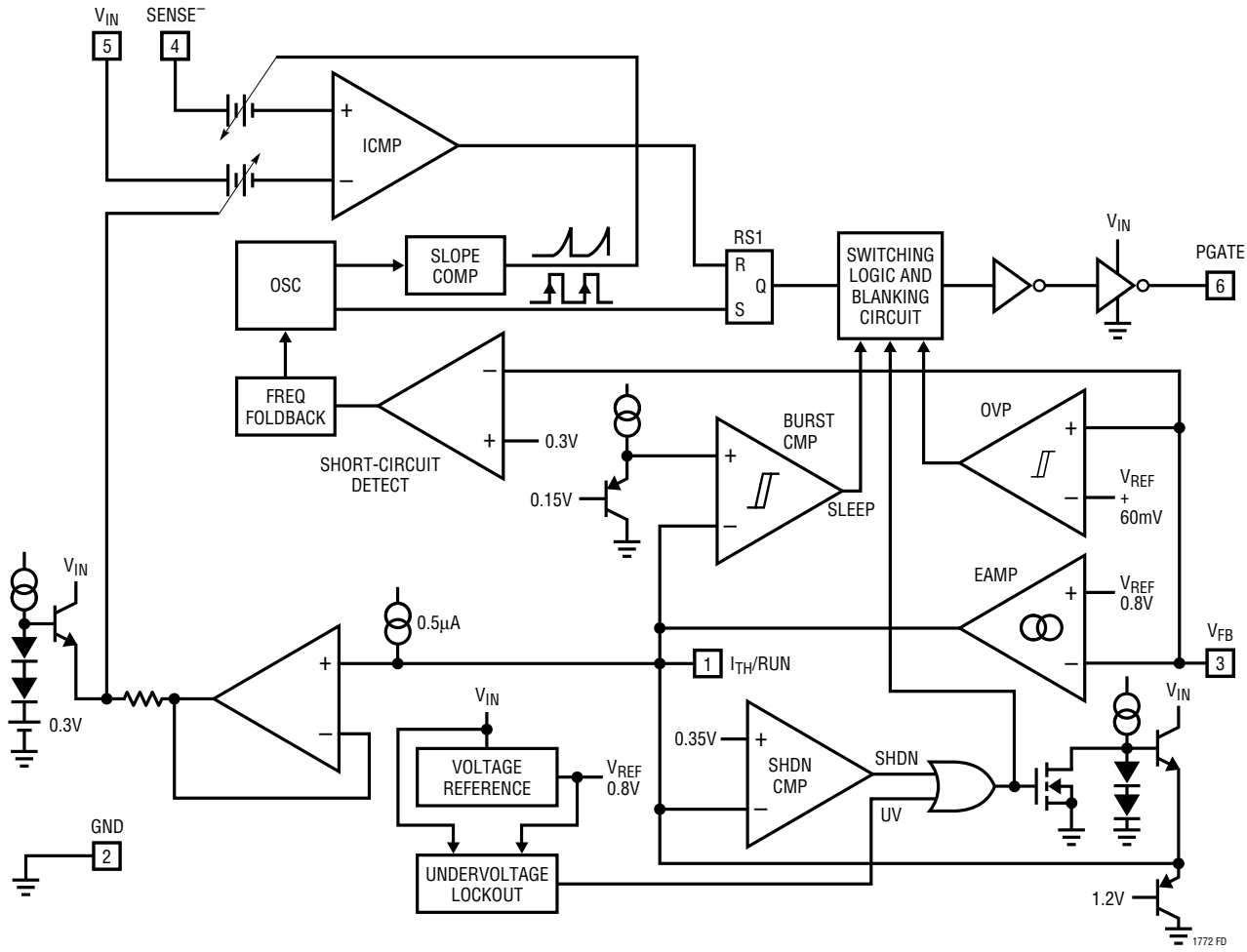
V_{FB} (Pin 3): Receives the feedback voltage from an external resistive divider across the output.

SENSE$^-$ (Pin 4): The Negative Input to the Current Comparator.

V_{IN} (Pin 5): Supply Pin. Must be closely decoupled to GND Pin 2.

PGATE (Pin 6): Gate Drive for the External P-Channel MOSFET. This pin swings from 0V to V_{IN}.

FUNCTIONAL DIAGRAM



OPERATION (Refer to Functional Diagram)

Main Control Loop

The LTC1772 is a constant frequency current mode switching regulator. During normal operation, the external P-channel power MOSFET is turned on each cycle when the oscillator sets the RS latch (RS1) and turned off when the current comparator (ICMP) resets the latch. The peak inductor current at which ICMP resets the RS latch is controlled by the voltage on the I_{TH}/RUN pin, which is the output of the error amplifier EAMP. An external resistive divider connected between V_{OUT} and ground allows the EAMP to receive an output feedback voltage V_{FB}. When the load current increases, it causes a slight decrease in V_{FB} relative to the 0.8V reference, which in turn causes the I_{TH}/RUN voltage to increase until the average inductor current matches the new load current.

The main control loop is shut down by pulling the I_{TH}/RUN pin low. Releasing I_{TH}/RUN allows an internal 0.5µA current source to charge up the external compensation network. When the I_{TH}/RUN pin reaches 0.35V, the main control loop is enabled with the I_{TH}/RUN voltage then pulled up to its zero current level of approximately 0.7V. As the external compensation network continues to charge up, the corresponding output current trip level follows, allowing normal operation.

Comparator OVP guards against transient overshoots >7.5% by turning off the external P-channel power MOSFET and keeping it off until the fault is removed.

Burst Mode Operation

The LTC1772 enters Burst Mode operation at low load currents. In this mode, the peak current of the inductor is set as if V_{ITH}/RUN = 1V (at low duty cycles) even though the voltage at the I_{TH}/RUN pin is at a lower value. If the inductor's average current is greater than the load requirement, the voltage at the I_{TH}/RUN pin will drop. When the I_{TH}/RUN voltage goes below 0.85V, the sleep signal goes high, turning off the external MOSFET. The sleep signal goes low when the I_{TH}/RUN voltage goes above 0.925V and the LTC1772 resumes normal operation. The next oscillator cycle will turn the external MOSFET on and the switching cycle repeats.

Dropout Operation

When the input supply voltage decreases towards the output voltage, the rate of change of inductor current during the ON cycle decreases. This reduction means that the external P-channel MOSFET will remain on for more than one oscillator cycle since the inductor current has not ramped up to the threshold set by EAMP. Further reduction in input supply voltage will eventually cause the P-channel MOSFET to be turned on 100%, i.e., DC. The output voltage will then be determined by the input voltage minus the voltage drop across the MOSFET, the sense resistor and the inductor.

Undervoltage Lockout

To prevent operation of the P-channel MOSFET below safe input voltage levels, an undervoltage lockout is incorporated into the LTC1772. When the input supply voltage drops below approximately 2.0V, the P-channel MOSFET and all circuitry is turned off except the undervoltage block, which draws only several microamperes.

Short-Circuit Protection

When the output is shorted to ground, the frequency of the oscillator will be reduced to about 120kHz. This lower frequency allows the inductor current to safely discharge, thereby preventing current runaway. The oscillator's frequency will gradually increase to its designed rate when the feedback voltage again approaches 0.8V.

Overvoltage Protection

As a further protection, the overvoltage comparator in the LTC1772 will turn the external MOSFET off when the feedback voltage has risen 7.5% above the reference voltage of 0.8V. This comparator has a typical hysteresis of 20mV.

OPERATION (Refer to Functional Diagram)

Slope Compensation and Inductor's Peak Current

The inductor's peak current is determined by:

$$I_{PK} = \frac{V_{ITH} - 0.7}{10(R_{SENSE})}$$

when the LTC1772 is operating below 40% duty cycle. However, once the duty cycle exceeds 40%, slope compensation begins and effectively reduces the peak inductor current. The amount of reduction is given by the curves in Figure 2.

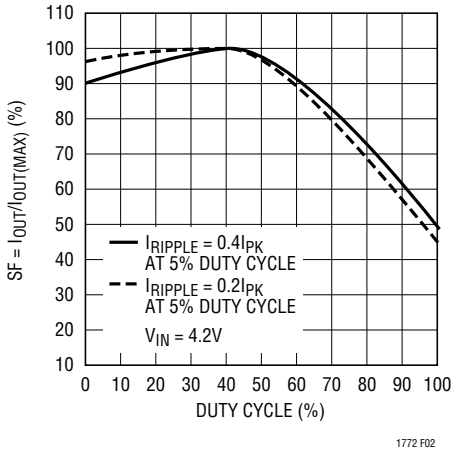


Figure 2. Maximum Output Current vs Duty Cycle

APPLICATIONS INFORMATION

The basic LTC1772 application circuit is shown in Figure 1. External component selection is driven by the load requirement and begins with the selection of L1 and R_{SENSE} (= R1). Next, the power MOSFET, M1 and the output diode D1 are selected followed by C_{IN} (= C1) and C_{OUT} (= C2).

R_{SENSE} Selection for Output Current

R_{SENSE} is chosen based on the required output current. With the current comparator monitoring the voltage developed across R_{SENSE}, the threshold of the comparator determines the inductor's peak current. The output current the LTC1772 can provide is given by:

$$I_{OUT} = \frac{0.12}{R_{SENSE}} - \frac{I_{RIPPLE}}{2}$$

where I_{RIPPLE} is the inductor peak-to-peak ripple current (see Inductor Value Calculation section).

A reasonable starting point for setting ripple current is $I_{RIPPLE} = (0.4)(I_{OUT})$. Rearranging the above equation, it becomes:

$$R_{SENSE} = \frac{1}{(10)(I_{OUT})} \text{ for Duty Cycle } < 40\%$$

However, for operation that is above 40% duty cycle, slope compensation effect has to be taken into consideration to select the appropriate value to provide the required amount of current. Using Figure 2, the value of R_{SENSE} is:

$$R_{SENSE} = \frac{SF}{(10)(I_{OUT})(100)}$$

Inductor Value Calculation

The operating frequency and inductor selection are interrelated in that higher operating frequencies permit the use of a smaller inductor for the same amount of inductor ripple current. However, this is at the expense of efficiency due to an increase in MOSFET gate charge losses.

The inductance value also has a direct effect on ripple current. The ripple current, I_{RIPPLE}, decreases with higher inductance or frequency and increases with higher V_{IN} or V_{OUT}. The inductor's peak-to-peak ripple current is given by:

$$I_{RIPPLE} = \frac{V_{IN} - V_{OUT}}{f(L)}\left(\frac{V_{OUT} + V_D}{V_{IN} + V_D}\right)$$

APPLICATIONS INFORMATION

where f is the operating frequency. Accepting larger values of I_{RIPPLE} allows the use of low inductances, but results in higher output voltage ripple and greater core losses. A reasonable starting point for setting ripple current is $I_{RIPPLE} = 0.4(I_{OUT(MAX)})$. Remember, the maximum I_{RIPPLE} occurs at the maximum input voltage.

In Burst Mode operation on the LTC1772, the ripple current is normally set such that the inductor current is continuous during the burst periods. Therefore, the peak-to-peak ripple current must not exceed:

$$I_{RIPPLE} \leq \frac{0.03}{R_{SENSE}}$$

This implies a minimum inductance of:

$$L_{MIN} = \frac{V_{IN} - V_{OUT}}{f\left(\frac{0.03}{R_{SENSE}}\right)}\left(\frac{V_{OUT} + V_D}{V_{IN} + V_D}\right)$$

(Use $V_{IN(MAX)} = V_{IN}$)

A smaller value than L_{MIN} could be used in the circuit; however, the inductor current will not be continuous during burst periods.

Inductor Core Selection

Once the value for L is known, the type of inductor must be selected. High efficiency converters generally cannot afford the core loss found in low cost powdered iron cores, forcing the use of more expensive ferrite, molypermalloy or Kool Mμ® cores. Actual core loss is independent of core size for a fixed inductor value, but it is very dependent on inductance selected. As inductance increases, core losses go down. Unfortunately, increased inductance requires more turns of wire and therefore copper losses will increase. Ferrite designs have very low core losses and are preferred at high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates "hard," which means that inductance collapses abruptly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current and consequent output voltage ripple. Do not allow the core to saturate!

Molypermalloy (from Magnetics, Inc.) is a very good, low loss core material for toroids, but it is more expensive than ferrite. A reasonable compromise from the same manufacturer is Kool Mμ. Toroids are very space efficient, especially when you can use several layers of wire. Because they generally lack a bobbin, mounting is more difficult. However, new designs for surface mount that do not increase the height significantly are available.

Power MOSFET Selection

An external P-channel power MOSFET must be selected for use with the LTC1772. The main selection criteria for the power MOSFET are the threshold voltage $V_{GS(TH)}$ and the "on" resistance $R_{DS(ON)}$, reverse transfer capacitance C_{RSS} and total gate charge.

Since the LTC1772 is designed for operation down to low input voltages, a sublogic level threshold MOSFET ($R_{DS(ON)}$ guaranteed at $V_{GS} = 2.5V$) is required for applications that work close to this voltage. When these MOSFETs are used, make sure that the input supply to the LTC1772 is less than the absolute maximum V_{GS} rating, typically 8V.

The required minimum $R_{DS(ON)}$ of the MOSFET is governed by its allowable power dissipation. For applications that may operate the LTC1772 in dropout, i.e., 100% duty cycle, at its worst case the required $R_{DS(ON)}$ is given by:

$$R_{DS(ON)_{DC=100\%}} = \frac{P_P}{\left(I_{OUT(MAX)}\right)^2(1+\delta p)}$$

where P_P is the allowable power dissipation and δp is the temperature dependency of $R_{DS(ON)}$. $(1 + \delta p)$ is generally given for a MOSFET in the form of a normalized $R_{DS(ON)}$ vs temperature curve, but $\delta p = 0.005/°C$ can be used as an approximation for low voltage MOSFETs.

In applications where the maximum duty cycle is less than 100% and the LTC1772 is in continuous mode, the $R_{DS(ON)}$ is governed by:

$$R_{DS(ON)} \cong \frac{P_P}{(DC)I_{OUT}{}^2(1+\delta p)}$$

where DC is the maximum operating duty cycle of the LTC1772.

APPLICATIONS INFORMATION

Output Diode Selection

The catch diode carries load current during the off-time. The average diode current is therefore dependent on the P-channel switch duty cycle. At high input voltages the diode conducts most of the time. As V_{IN} approaches V_{OUT} the diode conducts only a small fraction of the time. The most stressful condition for the diode is when the output is short-circuited. Under this condition the diode must safely handle I_{PEAK} at close to 100% duty cycle. Therefore, it is important to adequately specify the diode peak current and average power dissipation so as not to exceed the diode ratings.

Under normal load conditions, the average current conducted by the diode is:

$$I_D = \left(\frac{V_{IN} - V_{OUT}}{V_{IN} + V_D}\right) I_{OUT}$$

The allowable forward voltage drop in the diode is calculated from the maximum short-circuit current as:

$$V_F \approx \frac{P_D}{I_{SC(MAX)}}$$

where P_D is the allowable power dissipation and will be determined by efficiency and/or thermal requirements.

A fast switching diode must also be used to optimize efficiency. Schottky diodes are a good choice for low forward drop and fast switching times. Remember to keep lead length short and observe proper grounding (see Board Layout Checklist) to avoid ringing and increased dissipation.

C_{IN} and C_{OUT} Selection

In continuous mode, the source current of the P-channel MOSFET is a square wave of duty cycle $(V_{OUT} + V_D)/(V_{IN} + V_D)$. To prevent large voltage transients, a low ESR input capacitor sized for the maximum RMS current must be used. The maximum RMS capacitor current is given by:

$$C_{IN}\ \text{Required}\ I_{RMS} \approx I_{MAX} \frac{\left[V_{OUT}\left(V_{IN} - V_{OUT}\right)\right]^{1/2}}{V_{IN}}$$

This formula has a maximum value at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that capacitor manufacturer's ripple current ratings are often based on 2000 hours of life. This makes it advisable to further derate the capacitor, or to choose a capacitor rated at a higher temperature than required. Several capacitors may be paralleled to meet the size or height requirements in the design. Due to the high operating frequency of the LTC1772, ceramic capacitors can also be used for C_{IN}. Always consult the manufacturer if there is any question.

The selection of C_{OUT} is driven by the required effective series resistance (ESR). Typically, once the ESR requirement is satisfied, the capacitance is adequate for filtering. The output ripple (ΔV_{OUT}) is approximated by:

$$\Delta V_{OUT} \approx I_{RIPPLE}\left(ESR + \frac{1}{4fC_{OUT}}\right)$$

where f is the operating frequency, C_{OUT} is the output capacitance and I_{RIPPLE} is the ripple current in the inductor. The output ripple is highest at maximum input voltage since ΔI_L increases with input voltage.

Manufacturers such as Nichicon, United Chemicon and Sanyo should be considered for high performance through-hole capacitors. The OS-CON semiconductor dielectric capacitor available from Sanyo has the lowest ESR (size) product of any aluminum electrolytic at a somewhat higher price. Once the ESR requirement for C_{OUT} has been met, the RMS current rating generally far exceeds the $I_{RIPPLE(P-P)}$ requirement.

In surface mount applications, multiple capacitors may have to be paralleled to meet the ESR or RMS current handling requirements of the application. Aluminum electrolytic and dry tantalum capacitors are both available in surface mount configurations. In the case of tantalum, it is critical that the capacitors are surge tested for use in switching power supplies. An excellent choice is the AVX TPS, AVX TPSV and KEMET T510 series of surface mount tantalum, available in case heights ranging from 2mm to 4mm. Other capacitor types include Sanyo OS-CON, Nichicon PL series and Panasonic SP.

APPLICATIONS INFORMATION

Low Supply Operation

Although the LTC1772 can function down to approximately 2V, the maximum allowable output current is reduced when V_{IN} decreases below 3V. Figure 3 shows the amount of change as the supply is reduced down to 2V. Also shown in Figure 3 is the effect of V_{IN} on V_{REF} as V_{IN} goes below 2.3V.

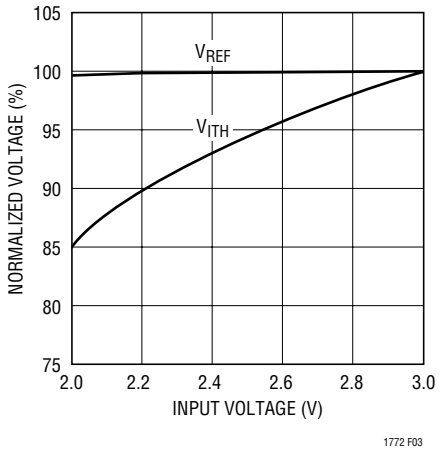


Figure 3. Line Regulation of V_{REF} and V_{ITH}

Setting Output Voltage

The LTC1772 develops a 0.8V reference voltage between the feedback (Pin 3) terminal and ground (see Figure 4). By selecting resistor R1, a constant current is caused to flow through R1 and R2 to set the overall output voltage. The regulated output voltage is determined by:

$$V_{OUT} = 0.8\left(1+\frac{R2}{R1}\right)$$

For most applications, an 80k resistor is suggested for R1. To prevent stray pickup, locate resistors R1 and R2 close to LTC1772.

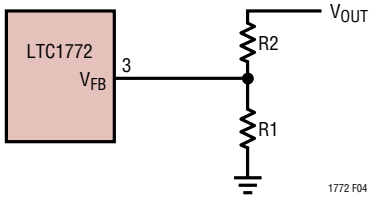


Figure 4. Setting Output Voltage

Efficiency Considerations

The efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Efficiency can be expressed as:

$$\text{Efficiency} = 100\% - (\eta 1 + \eta 2 + \eta 3 + ...)$$

where $\eta 1$, $\eta 2$, etc. are the individual losses as a percentage of input power.

Although all dissipative elements in the circuit produce losses, four main sources usually account for most of the losses in LTC1772 circuits: 1) LTC1772 DC bias current, 2) MOSFET gate charge current, 3) I^2R losses and 4) voltage drop of the output diode.

1. The V_{IN} current is the DC supply current, given in the electrical characteristics, that excludes MOSFET driver and control currents. V_{IN} current results in a small loss which increases with V_{IN}.
2. MOSFET gate charge current results from switching the gate capacitance of the power MOSFET. Each time a MOSFET gate is switched from low to high to low again, a packet of charge dQ moves from V_{IN} to ground. The resulting dQ/dt is a current out of V_{IN} which is typically much larger than the DC supply current. In continuous mode, $I_{GATECHG} = f(Qp)$.
3. I^2R losses are predicted from the DC resistances of the MOSFET, inductor and current shunt. In continuous mode the average output current flows through L but is "chopped" between the P-channel MOSFET (in series with R_{SENSE}) and the output diode. The MOSFET $R_{DS(ON)}$ plus R_{SENSE} multiplied by duty cycle can be summed with the resistances of L and R_{SENSE} to obtain I^2R losses.
4. The output diode is a major source of power loss at high currents and gets worse at high input voltages. The diode loss is calculated by multiplying the forward voltage times the diode duty cycle multiplied by the load current. For example, assuming a duty cycle of 50% with a Schottky diode forward voltage drop of

APPLICATIONS INFORMATION

0.4V, the loss increases from 0.5% to 8% as the load current increases from 0.5A to 2A.

5. Transition losses apply to the external MOSFET and increase at higher operating frequencies and input voltages. Transition losses can be estimated from:

   Transition Loss = $2(V_{IN})^2 I_{O(MAX)} C_{RSS}(f)$

Other losses including C_{IN} and C_{OUT} ESR dissipative losses, and inductor core losses, generally account for less than 2% total additional loss.

Foldback Current Limiting

As described in the Output Diode Selection, the worst-case dissipation occurs with a short-circuited output when the diode conducts the current limit value almost continuously. To prevent excessive heating in the diode, foldback current limiting can be added to reduce the current in proportion to the severity of the fault.

Foldback current limiting is implemented by adding diodes D_{FB1} and D_{FB2} between the output and the I_{TH}/RUN pin as shown in Figure 5. In a hard short (V_{OUT} = 0V), the current will be reduced to approximately 50% of the maximum output current.

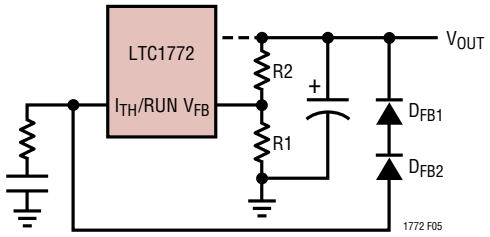


Figure 5. Foldback Current Limiting

PC Board Layout Checklist

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the LTC1772. These items are illustrated graphically in the layout diagram in Figure 6. Check the following in your layout:

1. Is the Schottky diode closely connected between ground (Pin 2) and drain of the external MOSFET?
2. Does the (+) plate of C_{IN} connect to the sense resistor as closely as possible? This capacitor provides AC current to the MOSFET.
3. Is the input decoupling capacitor (0.1µF) connected closely between V_{IN} (Pin 5) and ground (Pin 2)?
4. Connect the end of R_{SENSE} as close to V_{IN} (Pin 5) as possible. The V_{IN} pin is the SENSE$^+$ of the current comparator.
5. Is the trace from SENSE$^-$ (Pin 4) to the Sense resistor kept short? Does the trace connect close to R_{SENSE}?
6. Keep the switching node PGATE away from sensitive small signal nodes.
7. Does the V_{FB} pin connect directly to the feedback resistors? The resistive divider R1 and R2 must be connected between the (+) plate of C_{OUT} and signal ground.

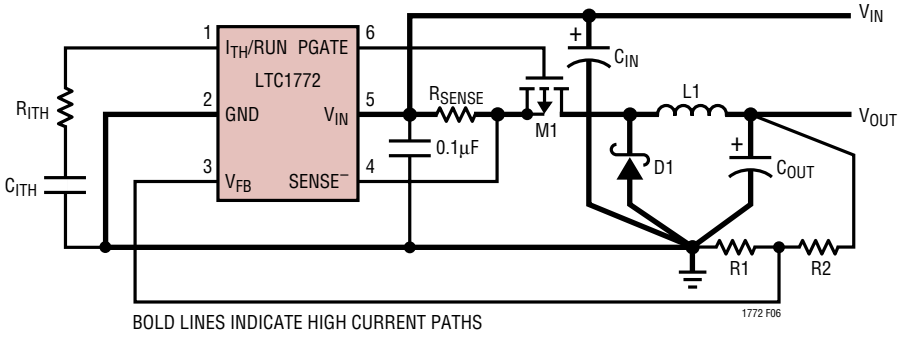
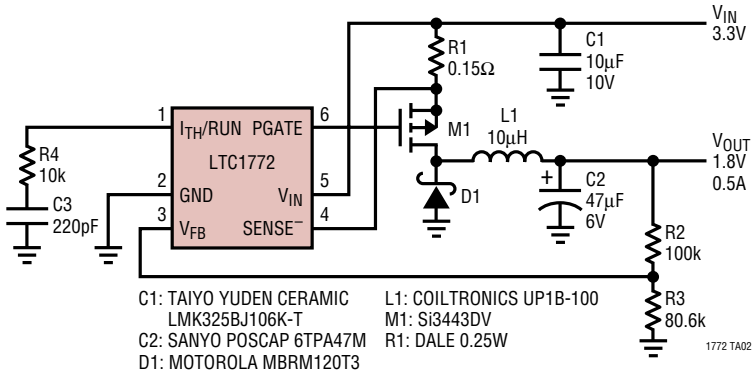


Figure 6. LTC1772 Layout Diagram (See PC Board Layout Checklist)

TYPICAL APPLICATION

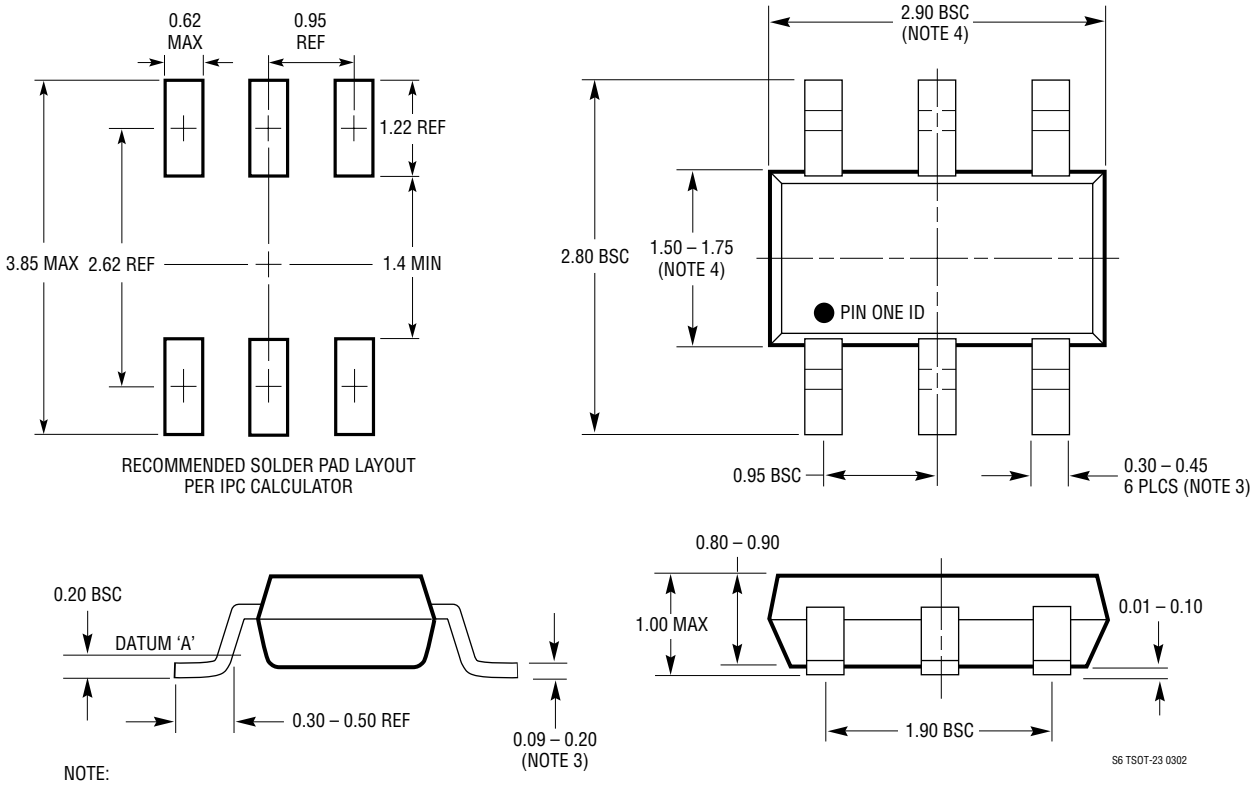
LTC1772 High Efficiency, Small Footprint 3.3V to 1.8V/0.5A Regulator



C1: TAIYO YUDEN CERAMIC LMK325BJ106K-T
C2: SANYO POSCAP 6TPA47M
D1: MOTOROLA MBRM120T3
L1: COILTRONICS UP1B-100
M1: Si3443DV
R1: DALE 0.25W

PACKAGE DESCRIPTION

S6 Package
6-Lead Plastic TSOT-23
(Reference LTC DWG # 05-08-1636)

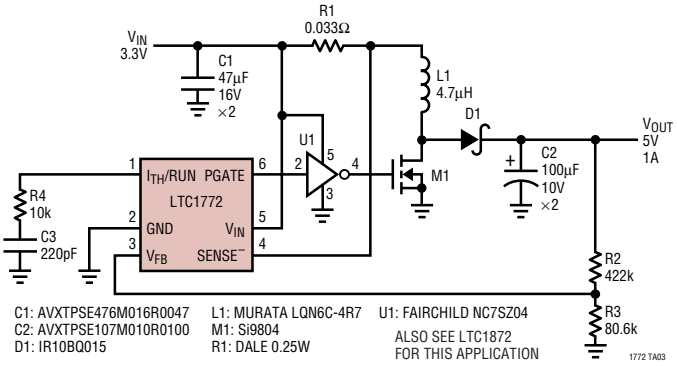


NOTE:
1. DIMENSIONS ARE IN MILLIMETERS
2. DRAWING NOT TO SCALE
3. DIMENSIONS ARE INCLUSIVE OF PLATING
4. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH AND METAL BURR
5. MOLD FLASH SHALL NOT EXCEED 0.254mm
6. JEDEC PACKAGE REFERENCE IS MO-193

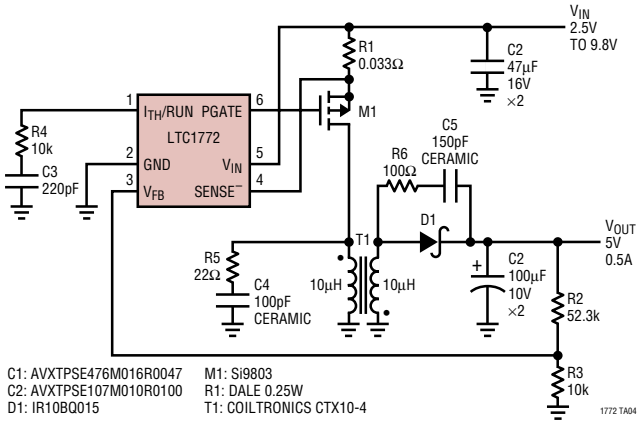
Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

TYPICAL APPLICATIONS

LTC1772 3.3V to 5V/1A Boost Regulator



LTC1772 5V/0.5A Flyback Regulator



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1147 Series	High Efficiency Step-Down Switching Regulator Controllers	100% Duty Cycle, 3.5V ≤ V_{IN} ≤ 16V
LT1375/LT1376	1.5A, 500kHz Step-Down Switching Regulators	High Frequency, Small Inductor, High Efficiency
LTC1622	Low Input Voltage Current Mode Step-Down DC/DC Controller	V_{IN} 2V to 10V, I_{OUT} Up to 4.5A, Synchronizable to 750kHz Optional Burst Mode Operation, 8-Lead MSOP
LTC1624	High Efficiency SO-8 N-Channel Switching Regulator Controller	N-Channel Drive, 3.5V ≤ V_{IN} ≤ 36V
LTC1625	No R_{SENSE}™ Synchronous Step-Down Regulator	97% Efficiency, No Sense Resistor
LTC1627	Low Voltage, Monolithic Synchronous Step-Down Regulator	Low Supply Voltage Range: 2.65V to 8V, I_{OUT} = 0.5A
LTC1649	3.3V Input Synchronous Controller	No Need for 5V Supply, Uses Standard Logic Gate MOSFETs; I_{OUT} up to 15A
LTC1702	550kHz, 2 Phase, Dual Synchronous Controller	Two Channels; Minimum C_{IN} and C_{OUT}, I_{OUT} up to 15A
LTC1735	Single, High Efficiency, Low Noise Synchronous Switching Controller	High Efficiency 5V to 3.3V Conversion at up to 15A
LTC1771	Ultra-Low Supply Current Step-Down DC/DC Controller	10µA Supply Current, 93% Efficiency, 1.23V ≤ V_{OUT} ≤ 18V; 2.8V ≤ V_{IN} ≤ 20V
LTC1872	SOT-23 Step-Up Controller	2.5V ≤ V_{IN} ≤ 9.8V; 550kHz; 90% Efficiency

No R_{SENSE} is a trademark of Linear Technology Corporation.

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