14-Bit, 6Msps, Sampling ADC

FEATURES

- **6Msps Sample Rate**
- **79dB S/(N + D) and 91dB SFDR at 2.5MHz f_{IN}**
- **Single 5V Supply or ±5V Supplies**
- Integral Nonlinearity Error: <1LSB
- Differential Nonlinearity: <0.5LSB
- 80MHz Full-Power Bandwidth Sampling
- ±2.5V and ±1.25V Bipolar Input Ranges
- 2.5V Signal Ground Available
- Out-of-Range Indicator
- True Differential Inputs with 75dB CMRR
- Power Dissipation: 245mW
- 36-Pin SSOP Package (0.209 Inch Width)

APPLICATIONS

- Telecommunications
- Multiplexed Data Acquisition Systems
- High Speed Data Acquisition
- Spectral Analysis
- Imaging Systems

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DESCRIPTION

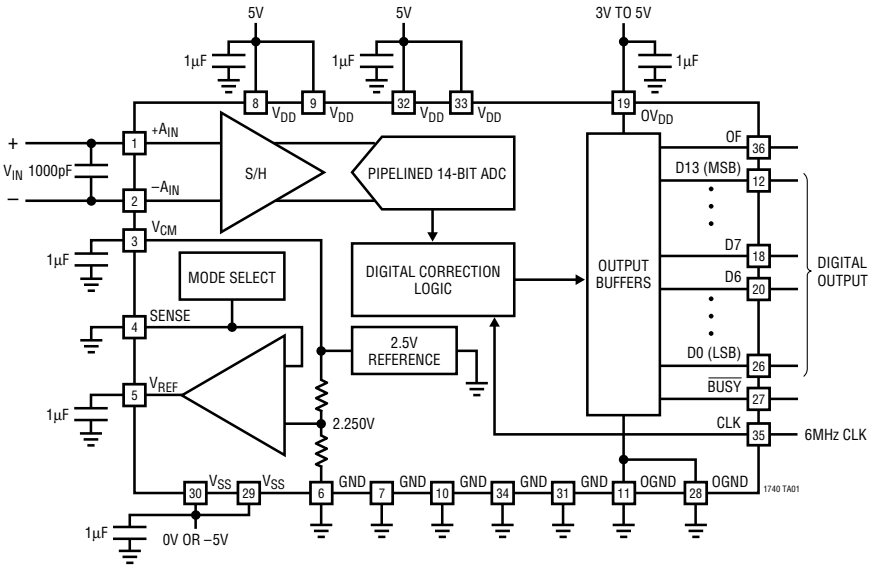
The LTC®1740 is a 6Msps, 14-bit sampling A/D converter that draws only 245mW from either a single 5V or dual ±5V supplies. This easy-to-use device includes a high dynamic range sample-and-hold and a programmable precision reference.

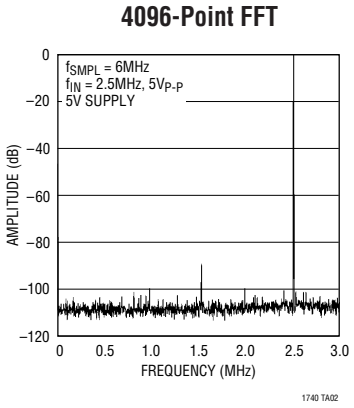
The LTC1740 has a flexible input circuit that allows differential full-scale input ranges of ±2.5V and ±1.25V with the internal reference, or any full-scale input range up to ±2.5V with an external reference. The input common mode voltage is arbitrary, though a 2.5V reference is provided for single supply applications.

DC specifications include 1LSB typical INL, 0.5LSB typical DNL and no missing codes over temperature. Outstanding AC performance includes 79dB S/(N + D) and 91dB SFDR at an input frequency of 2.5MHz.

The unique differential input sample-and-hold can acquire single-ended or differential input signals up to its 80MHz bandwidth. The 75dB common mode rejection allows users to eliminate ground loops and common mode noise by measuring signals differentially from the source. A separate output logic supply allows direct connection to 3V components.

BLOCK DIAGRAM



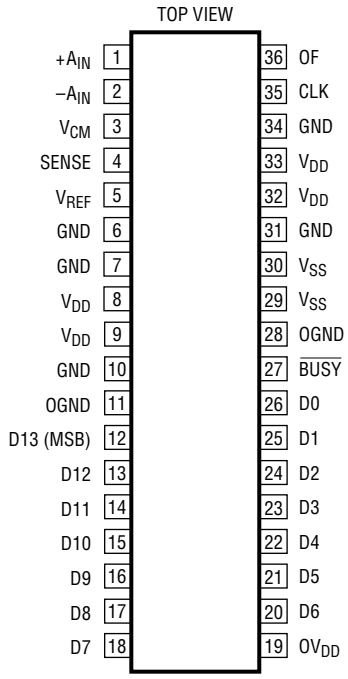


ABSOLUTE MAXIMUM RATINGS

$OV_{DD} = V_{DD}$ (Notes 1, 2)

Supply Voltage (V_{DD}) 6V
Negative Supply Voltage (V_{SS}) ..... –6V
Total Supply Voltage (V_{DD} to V_{SS}) 12V
Analog Input Voltage
(Note 3) ..... (V_{SS} – 0.3V) to (V_{DD} + 0.3V)
Digital Input Voltage
(Note 3) ..... (V_{SS} – 0.3V) to (V_{DD} + 0.3V)
Digital Output Voltage ..... (V_{SS} – 0.3V) to (V_{DD} + 0.3V)
Power Dissipation 500mW
Operating Temperature Range
LTC1740C ..... 0°C to 70°C
LTC1740I ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



G PACKAGE
36-LEAD PLASTIC SSOP

T_{JMAX} = 125°C, θ_{JA} = 95°C/W

ORDER PART NUMBER
LTC1740CG
LTC1740IG

Consult LTC Marketing for parts specified with wider operating temperature ranges.

CONVERTER CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. With internal 4.500V reference. Specifications are guaranteed for both dual supply and single supply operation. (Notes 4, 5)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Resolution (No Missing Codes)		●	14			Bits
Integral Linearity Error	(Note 6)			1	±2.5	LSB
Differential Linearity Error		●	–1	0.5	1.25	LSB
Offset Error	(Note 7)	 ●		±15	±60 ±80	LSB LSB
Full-Scale Error				±30	±75	LSB
Full-Scale Tempco	$I_{OUT(REF)}$ = 0			±15		ppm/°C

ANALOG INPUT

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. Specifications are guaranteed for both dual supply and single supply operation. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Analog Input Range	V_{REF} = 4.5V (SENSE = 0V) V_{REF} = 2.25V (SENSE Tied to V_{REF}) External V_{REF} (SENSE = 5V)	● ● ●		±2.50 ±1.25 ±V_{REF}/1.8		V V V
I_{IN}	Analog Input Leakage Current		●			±10	µA
C_{IN}	Analog Input Capacitance	Between Conversions During Conversions			12 4		pF pF
t_{ACQ}	Sample-and-Hold Acquisition Time				67		ns
t_{AP}	Sample-and-Hold Aperture Delay Time				–900		ps
t_{jitter}	Sample-and-Hold Aperture Delay Time Jitter				0.6		ps_{RMS}
CMRR	Analog Input Common Mode Rejection Ratio	V_{SS} < (–A_{IN} = +A_{IN}) < V_{DD}			75		dB

DYNAMIC ACCURACY

V_{DD} = 0V$_{DD}$ = 5V, V_{SS} = 0V, V_{REF} = 4.5V, A_{IN} = –0.1dBFS, AC coupled differential input.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
S/(N + D)	Signal-to-Noise Plus Distortion Ratio	1MHz Input Signal 2.5MHz Input Signal		79.1 79.0		dB dB
THD	Total Harmonic Distortion	1MHz Input Signal, First 5 Harmonics 2.5MHz Input Signal, First 5 Harmonics		–90 –89		dB dB
SFDR	Spurious Free Dynamic Range	1MHz Input Signal 2.5MHz Input Signal		92 91		dB dB
	Full-Power Bandwidth			80		MHz
	Input Referred Noise			0.45		LSB_{RMS}

INTERNAL REFERENCE CHARACTERISTICS

T_A = 25°C. Specifications are guaranteed for both dual supply and single supply operation. (Note 4)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CM} Output Voltage	I_{OUT} = 0	2.475	2.500	2.525	V
V_{CM} Output Tempco	I_{OUT} = 0		±15		ppm/°C
V_{CM} Line Regulation	4.75V ≤ V_{DD} ≤ 5.25V –5.25V ≤ V_{SS} ≤ –4.75V		0.6 0.03		mV/V mV/V
V_{CM} Output Resistance	0.1mA ≤ |I_{OUT}| ≤ 0.1mA		8		Ω
V_{REF} Output Voltage	SENSE = GND, I_{OUT} = 0 SENSE = V_{REF}, I_{OUT} = 0 SENSE = V_{DD}		4.500 2.250 Drive V_{REF} with External Reference		V V V
V_{REF} Output Tempco			±15		ppm/°C

DIGITAL INPUTS AND DIGITAL OUTPUTS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. Specifications are guaranteed for both dual supply and single supply operation. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage	V_{DD} = 5.25V, V_{SS} = 0V V_{DD} = 5.25V, V_{SS} = –5V	● ●	2.4 2.4			V V
V_{IL}	Low Level Input Voltage	V_{DD} = 4.75V, V_{SS} = 0V V_{DD} = 4.75V, V_{SS} = –5V	● ●			0.8 0.8	V V
I_{IN}	Digital Input Current	V_{IN} = 0V to V_{DD}	●			±10	µA
C_{IN}	Digital Input Capacitance				1.8		pF
V_{OH}	High Level Output Voltage	$0V_{DD}$ = 4.75V, I_O = –10µA $0V_{DD}$ = 4.75V, I_O = –200µA $0V_{DD}$ = 2.7V, I_O = –10µA $0V_{DD}$ = 2.7V, I_O = –200µA	 ● ●	 4.0 2.3	4.74 4.71 2.6 	 	V V V V
V_{OL}	Low Level Output Voltage	$0V_{DD}$ = 4.75V, I_O = 160µA $0V_{DD}$ = 4.75V, I_O = 1.6mA $0V_{DD}$ = 2.7V, I_O = 160µA $0V_{DD}$ = 2.7V, I_O = 1.6mA	 ● ●	 	0.05 0.10 0.05 0.10	 0.4 0.4	V V V V
I_{SOURCE}	Output Source Current	V_{OUT} = 0V, $0V_{DD}$ = 5V			50		mA
I_{SINK}	Output Sink Current	V_{OUT} = V_{DD}, $0V_{DD}$ = 5V			35		mA

POWER REQUIREMENTS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. Specifications are guaranteed for both dual supply and single supply operation. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{DD}	Positive Supply Voltage	(Note 9)		4.75		5.25	V
OV_{DD}	Output Supply Voltage	(Note 9)		2.7		V_{DD}	V
V_{SS}	Negative Supply Voltage	Dual Supply Mode Single Supply Mode		–5.25	 0	–4.75	V V
I_{DD}	Positive Supply Current		●		47	60	mA
I_{SS}	Negative Supply Current		●		2.3	2.6	mA
P_D	Power Dissipation		●		245	300	mW

TIMING CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. Specifications are guaranteed for both dual supply and single supply operation. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
f_{SAMPLE}	Sampling Frequency		●	0.05		6	MHz
t_{CONV}	Conversion Time		●		100	135	ns
t_{ACQ}	Acquisition Time	(Note 9)	●	31	67		ns
t_H	CLK High Time	(Note 9)	●	20	83.3		ns
t_L	CLK Low Time	(Note 9)	●	20	83.3		ns
t_{AP}	Aperature Delay of Sample-and-Hold				–900		ps
t_1	CLK↑ to $\overline{BUSY}$↓				3.5		ns
t_2	$\overline{BUSY}$↑ to Outputs Valid				1.5		ns
	Data Latency				3		Cycles

TIMING CHARACTERISTICS

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: All voltage values are with respect to ground with GND and OGND wired together (unless otherwise noted).

Note 3: When these pin voltages are taken below V_{SS} or above V_{DD}, they will be clamped by internal diodes. This product can handle input currents greater than 100mA below V_{SS} or above V_{DD} without latchup.

Note 4: V_{DD} = 5V, V_{SS} = –5V or 0V, f_{SAMPLE} = 6MHz, $t_r = t_f$ = 5ns unless otherwise specified.

Note 5: Linearity, offset and full-scale specifications apply for a single-ended $+A_{IN}$ input with $–A_{IN}$ tied to V_{CM} for single supply and 0V for dual supply.

Note 6: Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

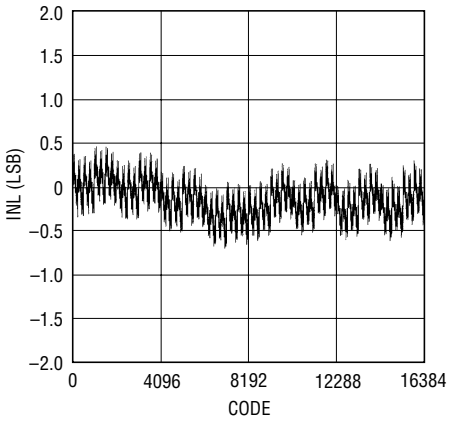
Note 7: Bipolar offset is the offset voltage measured from –0.5LSB when the output code flickers between 00 0000 0000 0000 and 11 1111 1111 1111.

Note 8: Guaranteed by design, not subject to test.

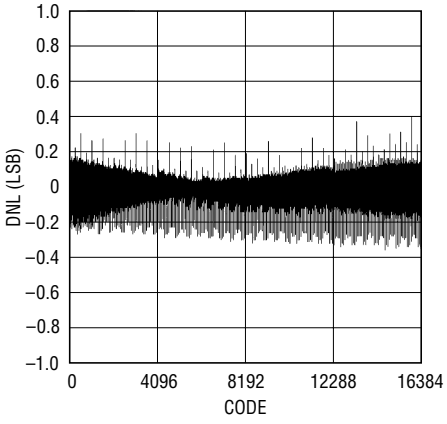
Note 9: Recommended operating conditions.

TYPICAL PERFORMANCE CHARACTERISTICS

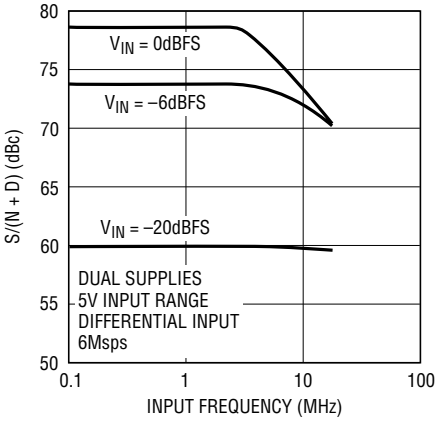
Typical INL at 6Msps



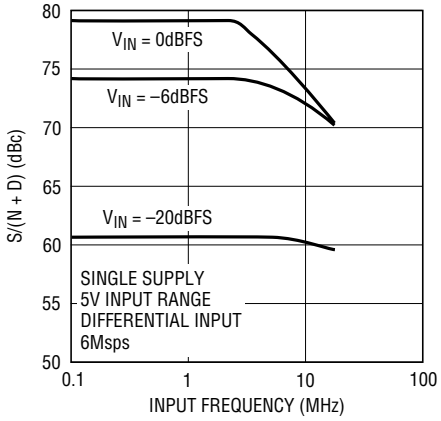
Typical DNL at 6Msps



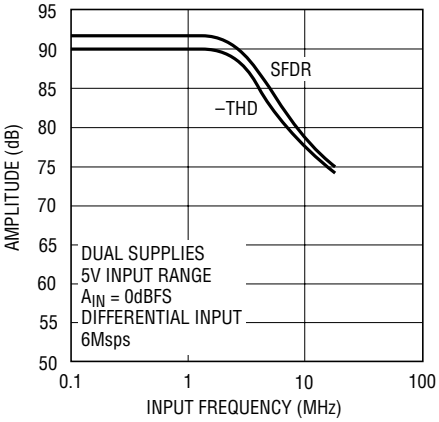
S/(N + D) vs Input Frequency and Amplitude



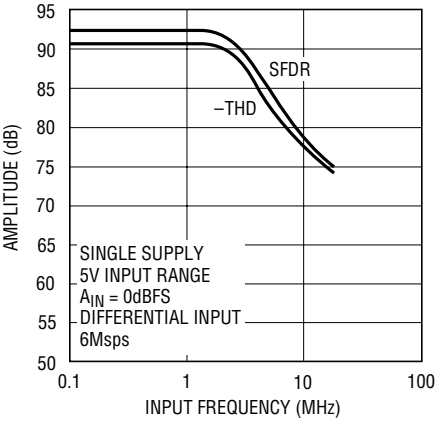
S/(N + D) vs Input Frequency and Amplitude



SFDR and THD vs Input Frequency

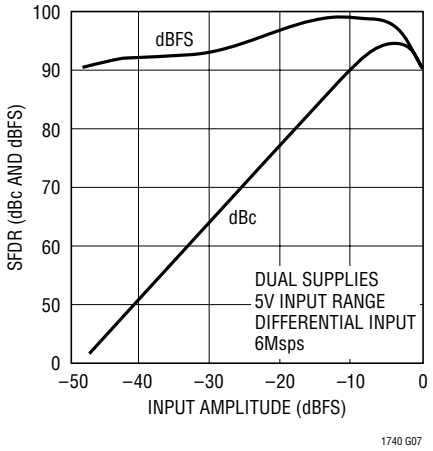


SFDR and THD vs Input Frequency

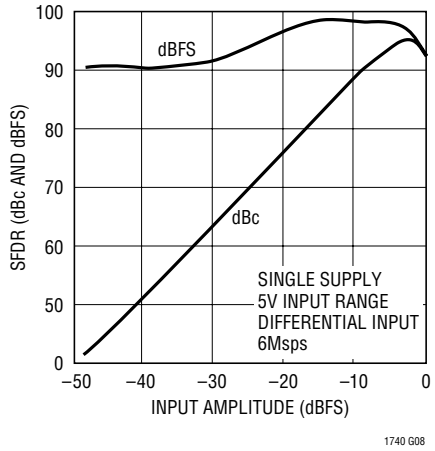


TYPICAL PERFORMANCE CHARACTERISTICS

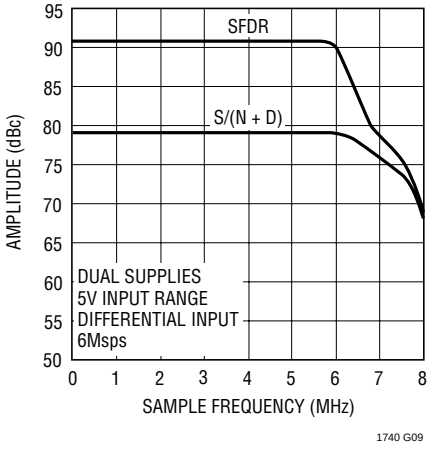
Spurious-Free Dynamic Range vs Input Amplitude



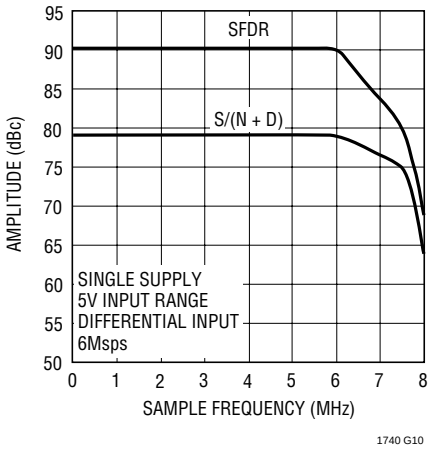
Spurious-Free Dynamic Range vs Input Amplitude



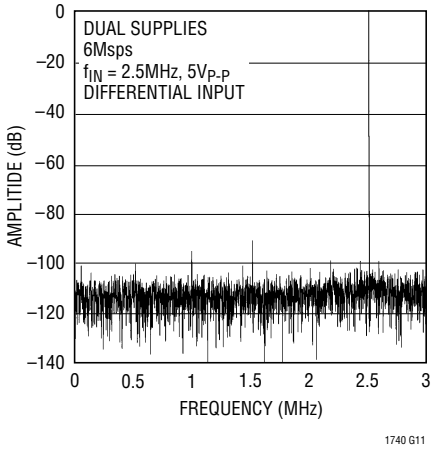
S/(N + D) and SFDR vs Sample Frequency



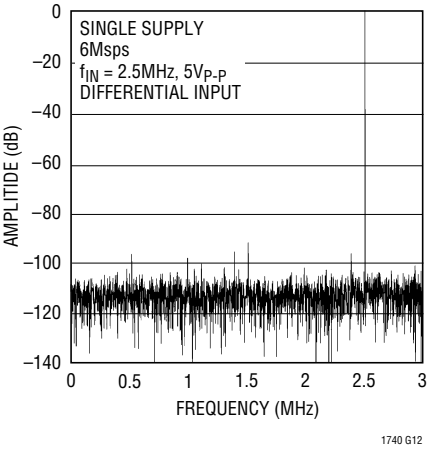
S/(N + D) and SFDR vs Sample Frequency



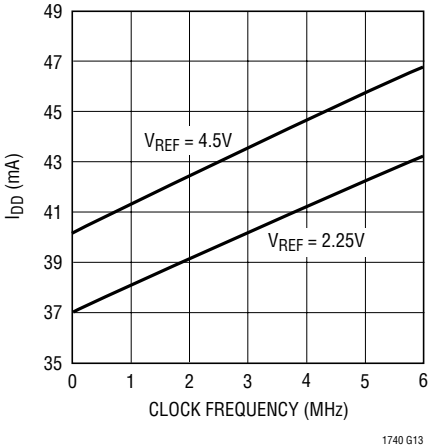
Nonaveraged 4096 Point FFT



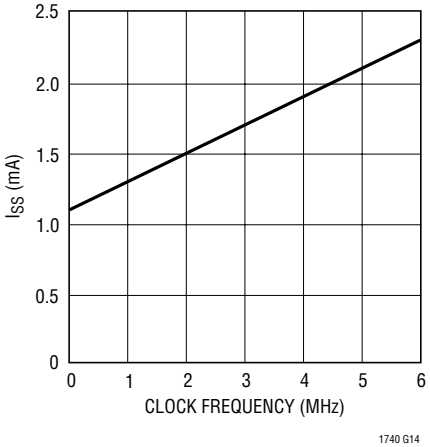
Nonaveraged 4096 Point FFT



I_{DD} vs Clock Frequency



I_{SS} vs Clock Frequency



PIN FUNCTIONS

$+A_{IN}$ (Pin 1): Positive Analog Input.

$-A_{IN}$ (Pin 2): Negative Analog Input.

V_{CM} (Pin 3): 2.5V Reference Output. Optional input common mode for single supply operation. Bypass to GND with a 1µF to 10µF ceramic capacitor.

SENSE (Pin 4): Reference Programming Pin. Ground selects V_{REF} = 4.5V. Short to V_{REF} for V_{REF} = 2.25V. Connect SENSE to V_{DD} to drive V_{REF} with an external reference. Connect SENSE directly to V_{DD}, V_{REF} or GND. Do not drive SENSE with a logic signal.

V_{REF} (Pin 5): DAC Reference. Bypass to GND with a 1µF to 10µF ceramic capacitor.

GND (Pins 6, 7, 10, 31, 34): Analog Power Ground.

V_{DD} (Pins 8, 9): Analog 5V Supply. Bypass to GND with a 1µF to 10µF ceramic capacitor. (Do not share a capacitor with Pins 32 and 33.)

OGND (Pins 11, 28): Output Logic Ground. Connect to GND.

D13 to D0 (Pins 12 to 18, 20 to 26): Data Outputs. The output format is two's complement.

OV_{DD} (Pin 19): Positive Supply for the Output Logic. Can be 2.7V to 5.25V. Bypass to GND with a 1µF to 10µF ceramic capacitor.

$\overline{BUSY}$ (Pin 27): $\overline{BUSY}$ is low when a conversion is in progress. When a conversion is finished and the ADC is acquiring the input signal, $\overline{BUSY}$ is high. Either the falling edge of $\overline{BUSY}$ or the rising edge of CLK can be used to latch the output data.

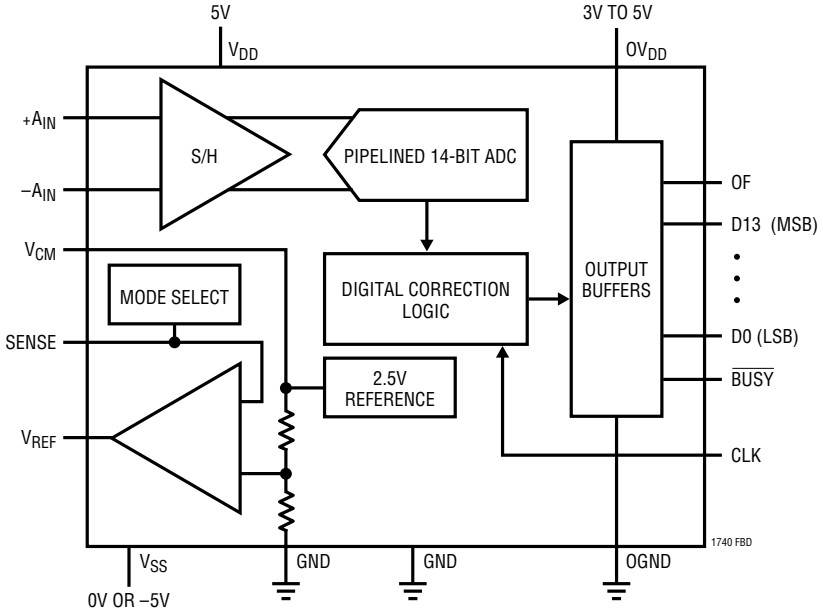
V_{SS} (Pins 29, 30): Negative Supply. Can be –5V or 0V. If V_{SS} is not shorted to GND, bypass to GND with a 1µF ceramic capacitor.

V_{DD} (Pins 32, 33): Analog 5V Supply. Bypass to GND with a 1µF to 10µF ceramic capacitor (do not share a capacitor with Pins 8, 9).

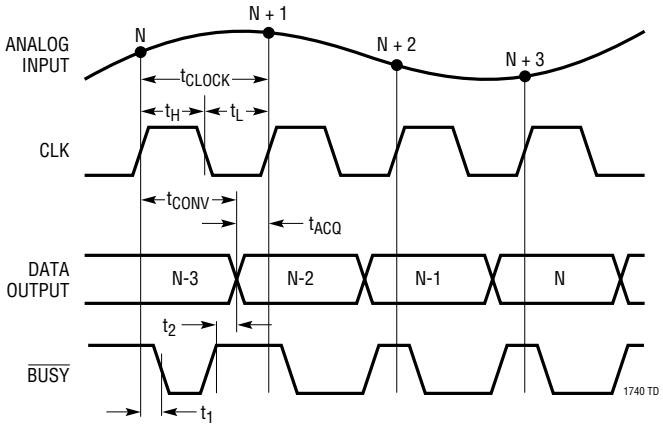
CLK (Pin 35): Conversion Start Signal. This active high signal starts a conversion on its rising edge.

OF (Pin 36): Overflow Output. This signal is high when the digital output is 01 1111 1111 1111 or 10 0000 0000 0000.

FUNCTIONAL BLOCK DIAGRAM



TIMING DIAGRAM



APPLICATIONS INFORMATION

Conversion Details

The LTC1740 is a high performance 14-bit A/D converter that operates up to 6Msps. It is a complete solution with an on-chip sample-and-hold, a 14-bit pipelined CMOS ADC and a low drift programmable reference. The digital output is parallel, with a 14-bit two's complement format and an out-of-range (overflow) bit.

The rising edge of the CLK begins the conversion. The differential analog inputs are simultaneously sampled and passed on to the pipelined A/D. After two more conversion starts (plus a 100ns conversion time) the digital outputs are updated with the conversion result and will be ready for capture on the third rising clock edge. Thus even though a new conversion is begun every time CLK goes high, each result takes three clock cycles to reach the output.

The analog signals that are passed from stage to stage in the pipelined A/D are stored on capacitors. The signals on these capacitors will be lost if the delay between conversions is too long. For accurate conversion results, the part should be clocked faster than 50kHz.

In some pipelined A/D converters if there is no clock present, dynamic logic on the chip will droop and the power consumption sharply increases. The LTC1740 doesn't have this problem. If the part is not clocked for 1ms, an internal timer will refresh the dynamic logic. Thus the clock can be turned off for long periods of time to save power.

Power Supplies

The LTC1740 will operate from either a single 5V or dual ±5V supply, making it easy to interface the analog input to single or dual supply systems. The digital output drivers have their own power supply pin (OV_{DD}) which can be set from 3V to 5V, allowing direct connection to either 3V or 5V digital systems. For single supply operation, V_{SS} should be connected to analog ground. For dual supply operation, V_{SS} should be connected to –5V. All V_{DD} pins should be connected to a clean 5V analog supply. (Don't connect V_{DD} to a noisy system digital supply.)

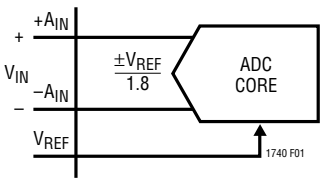


Figure 1. Analog Input Circuit

Analog Input Range

The LTC1740 has a flexible analog input with a wide selection of input ranges. The input range is always differential and is set by the voltage at the V_{REF} pin (Figure 1). The input range of the A/D core is fixed at $\pm V_{REF}/1.8$. The reference voltage, V_{REF}, is either set by the on-chip voltage reference or directly driven by an external voltage.

Internal Reference

Figure 2 shows a simplified schematic of the LTC1740 reference circuitry. An on-chip temperature compensated bandgap reference (V_{CM}) is factory trimmed to 2.500V. The voltage at the V_{REF} pin sets the input span of the ADC to $\pm V_{REF}/1.8$. An internal voltage divider converts V_{CM} to 2.250V, which is connected to a reference amplifier. The reference programming pin, SENSE, controls how the

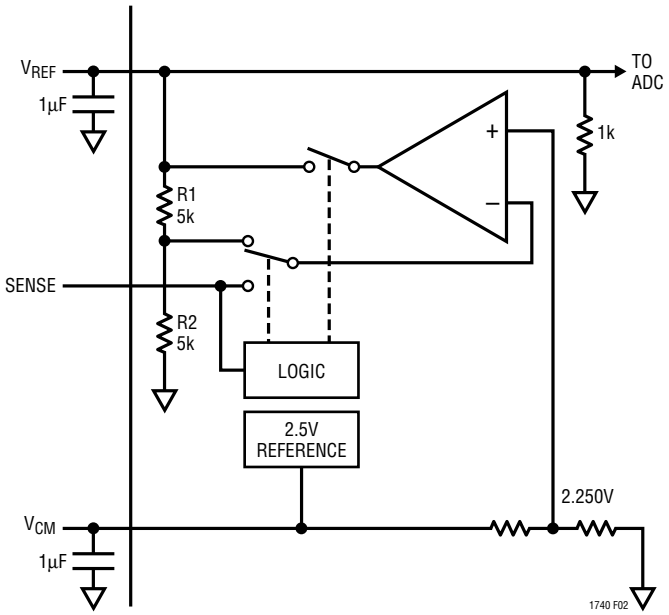


Figure 2. Reference Circuit

APPLICATIONS INFORMATION

reference amplifier drives the V_{REF} pin. If SENSE is tied to ground, the reference amplifier feedback is connected to the R1/R2 voltage divider, thus making V_{REF} = 4.500V. If SENSE is tied to V_{REF}, the reference amplifier feedback is connected to SENSE thus making V_{REF} = 2.250V. If SENSE is tied to V_{DD}, the reference amplifier is disconnected from V_{REF} and V_{REF} can be driven by an external voltage. With additional resistors between V_{REF} and SENSE, and SENSE and GND, V_{REF} can be set to any voltage between 2.250V and 4.5V.

An external reference or a DAC can be used to drive V_{REF} over a 0V to 5V range (Figures 3a and 3b). The input impedance of the V_{REF} pin is 1kΩ, so a buffer may be required for high accuracy. Driving V_{REF} with a DAC is useful in applications where the peak input signal amplitude may vary. The input span of the ADC can then be adjusted to match the peak input signal, maximizing the signal-to-noise ratio.

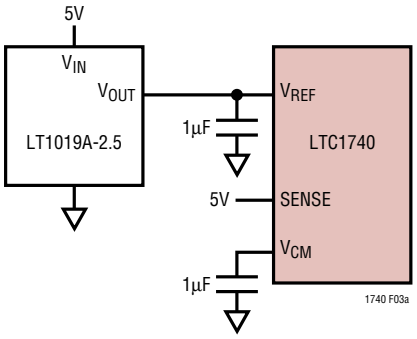


Figure 3a. Using the LT1019-2.5 as an External Reference; Input Range = ±1.39V

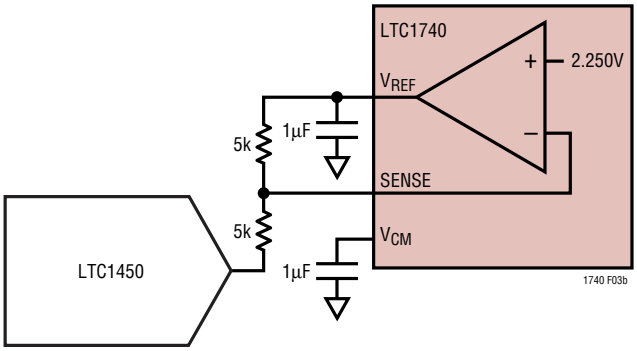


Figure 3b. Driving V_{REF} with a DAC

Both the V_{CM} and V_{REF} pins must be bypassed with capacitors to ground. For best performance, 1µF or larger ceramic capacitors are recommended. For the case of external circuitry driving V_{REF}, a smaller capacitor can be used at V_{REF} so the input range can be changed quickly. In this case, a 0.2µF or larger ceramic capacitor is acceptable.

The V_{CM} pin is a low output impedance 2.5V reference that can be used by external circuitry. For single 5V supply applications it is convenient to connect A_{IN}^- directly to the V_{CM} pin.

Driving the Analog Inputs

The differential inputs of the LTC1740 are easy to drive. The inputs may be driven differentially or single-ended (i. e., the A_{IN}^- input is held at a fixed value). The A_{IN}^- and A_{IN}^+ inputs are simultaneously sampled and any common mode signal is reduced by the high common mode rejection of the sample-and-hold circuit. Any common mode input value is acceptable as long as the input pins stay between V_{DD} and V_{SS}. During conversion the analog inputs are high impedance. At the end of conversion the inputs draw a small current spike while charging the sample-and-hold.

For superior dynamic performance in dual supply mode, the LTC1740 should be operated with the analog inputs centered at ground, and in single supply mode the inputs should be centered at 2.5V. For the best dynamic performance, the analog inputs can be driven differentially via a transformer or differential amplifier.

DC Coupling the Input

In many applications the analog input signal can be directly coupled to the LTC1740 inputs. If the input signal is centered around ground, such as when dual supply op amps are used, simply connect A_{IN}^- to ground and connect V_{SS} to –5V (Figure 4). In a single power supply system with the input signal centered around 2.5V, connect A_{IN}^- to V_{CM} and V_{SS} to ground (Figure 5). If the input signal is not centered around ground or 2.5V, the voltage for A_{IN}^- must be generated externally by a resistor divider or a voltage reference (Figure 6).

APPLICATIONS INFORMATION

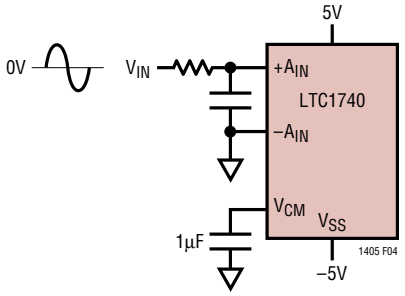


Figure 4. DC Coupling a Ground Centered Signal (Dual Supply System)

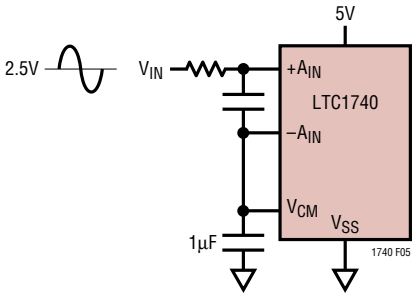


Figure 5. DC Coupling a Signal Centered Around 2.5V (Single Supply System)

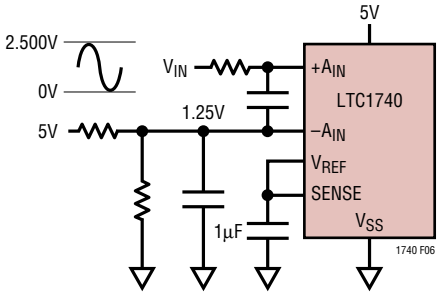


Figure 6. DC Coupling a 0V to 2.5V Signal

AC Coupling the Input

The analog inputs to the LTC1740 can also be AC coupled through a capacitor, though in most cases it is simpler to directly couple the input to the ADC. Figure 7 shows an example where the input signal is centered around ground and the ADC operates from a single 5V supply. Note that the performance would improve if the ADC was operated from a dual supply and the input was directly coupled (as in Figure 4). With AC coupling the DC resistance to ground should be roughly matched for A_{IN}^+ and A_{IN}^- to maintain offset accuracy.

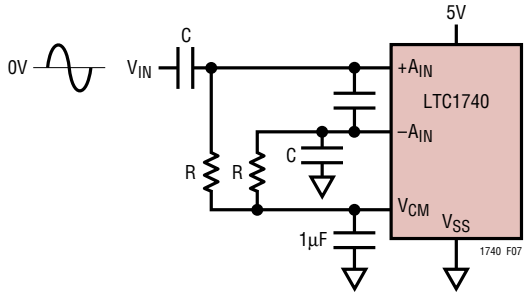


Figure 7. AC Coupling to the LTC1740. Note That the Input Signal Can Almost Always Be Directly Coupled with Better Performance

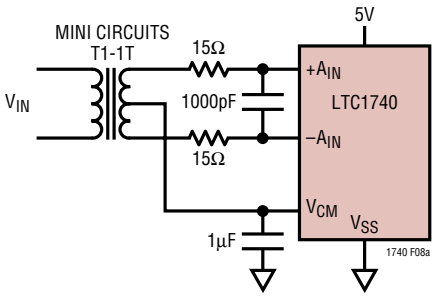


Figure 8a. Single Supply Transformer Coupled Input

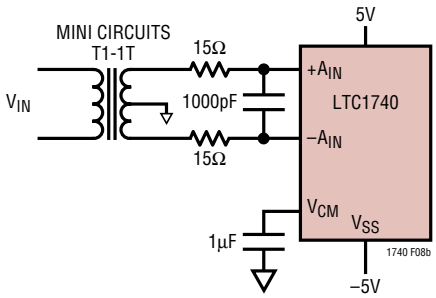


Figure 8b. Dual Supply Transformer Coupled Input

Differential Operation

The THD and SFDR performance of the LTC1740 can be improved by using a center tap RF transformer to drive the inputs differentially. Though the signal can no longer be DC coupled, the improvement in dynamic performance makes this an attractive solution for some applications. Typical connections for single and dual supply systems are shown in Figures 8a and 8b. Good choices for transformers are the Mini Circuits T1-1T (1:1 turns ratio) and T4-6T (1:4 turns ratio). For best results the transformer should be located close to the LTC1740 on the printed circuit board.

APPLICATIONS INFORMATION

Choosing an Input Amplifier

Choosing an input amplifier is easy if a few requirements are taken into consideration. First, to limit the magnitude of the voltage spike seen by the amplifier from charging the sampling capacitor, choose an amplifier that has a low output impedance (<100Ω) at the closed-loop bandwidth frequency. For example, if an amplifier is used in a gain of 1 and has a unity-gain bandwidth of 50MHz, then the output impedance at 50MHz must be less than 100Ω. The second requirement is that the closed-loop bandwidth must be greater than 50MHz to ensure adequate small-signal settling for full throughput rate. If slower op amps are used, more settling time can be provided by increasing the time between conversions.

The best choice for an op amp to drive the LTC1740 will depend on the application. Generally applications fall into two categories: AC applications where dynamic specifications are most critical and time domain applications where DC accuracy and settling time are most critical.

Input Filtering

The noise and the distortion of the input amplifier and other circuitry must be considered since they will add to the LTC1740 noise and distortion. The small-signal bandwidth of the sample-and-hold circuit is 80MHz. Any noise or distortion products that are present at the analog inputs will be summed over this entire bandwidth. Noisy input circuitry should be filtered prior to the analog inputs to minimize noise. A simple 1-pole RC filter is sufficient for many applications.

For example, Figure 9 shows a 1000pF capacitor from $+A_{IN}$ to $-A_{IN}$ and a 30Ω source resistor to limit the input bandwidth to 5.3MHz. The 1000pF capacitor also acts as a charge reservoir for the input sample-and-hold and isolates the amplifier driving V_{IN} from the ADC's small current glitch. In undersampling applications, an input capacitor this large may prohibitively limit the input bandwidth. If this is the case, use as large an input capacitance as possible. High quality capacitors and resistors should be used since these components can add distortion. NPO and silver mica type dielectric capacitors have excellent linearity. Carbon surface mount resistors can generate distortion from self-heating and from damage that may occur during soldering. Metal film surface mount resistors are much less susceptible to both problems.

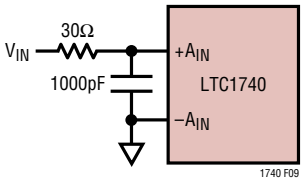


Figure 9. RC Input Filter

Digital Outputs and Overflow Bit (OF)

Figure 10 shows the ideal input/output characteristics for the LTC1740. The output data is two's complement binary for all input ranges and for both single and dual supply operation. One LSB = $V_{REF}/(0.9 \bullet 16384)$. To create a straight binary output, invert the MSB (D13). The overflow bit (OF) indicates when the analog input is outside the input range of the converter. OF is high when the output code is 10 0000 0000 0000 or 01 1111 1111 1111.

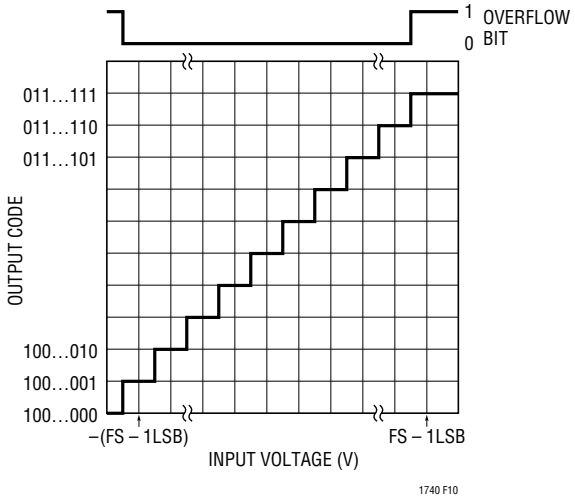


Figure 10. LTC1740 Transfer Characteristics

APPLICATIONS INFORMATION

Full-Scale and Offset Adjustment

In applications where absolute accuracy is important, offset and full-scale errors can be adjusted to zero. Offset error should be adjusted before full-scale error. Figure 11 shows a method for error adjustment for a dual supply, 5.00V input range application. For zero offset error apply –0.15mV (i. e., –0.5LSB) at $+A_{IN}$ and adjust R1 until the output code flickers between 00 0000 0000 0000 and 11 1111 1111 1111. For full-scale adjustment, apply an input voltage of 2.49954V (FS – 1.5LSBs) at $+A_{IN}$ and adjust R2 until the output code flickers between 01 1111 1111 1110 and 01 1111 1111 1111.

Digital Output Drivers

The LTC1740 output drivers can interface to logic operating from 3V to 5V by setting OV_{DD} to the logic power supply. OV_{DD} requires a 1µF decoupling capacitor. To prevent digital noise from affecting performance, the load capacitance on the digital outputs should be minimized. If large capacitive loads are required, (>30pF) external buffers or 100Ω resistors in series with the digital outputs are suggested.

Timing

The conversion start is controlled by the rising edge of the CLK pin. Once a conversion is started it cannot be stopped or restarted until the conversion cycle is complete. Output data is updated at the end of conversion, or about 100ns after a conversion is begun. There is an additional two cycle pipeline delay, so the data for a given conversion is output two full clock cycles plus 100ns after the convert start. Thus output data can be latched on the third CLK rising edge after the rising edge that samples the input.

Clock Input

The LTC1740 only uses the rising edge of the CLK pin for internal timing, and CLK doesn't necessarily need to have a 50% duty cycle. For optimal AC performance the rise time of the CLK should be less than 5ns. If the available clock has a rise time slower than 5ns, it can be locally sped up with a logic gate. The clock can be driven with 5V CMOS, 3V CMOS or TTL logic levels.

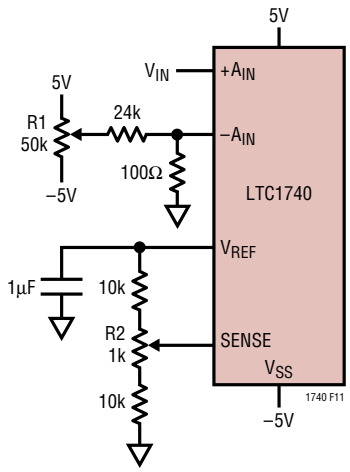


Figure 11. Offset and Full-Scale Adjust Circuit

APPLICATIONS INFORMATION

As with all fast ADCs, the noise performance of the LTC1740 is sensitive to clock jitter when high speed inputs are present. The SNR performance of an ADC when the performance is limited by jitter is given by:

$$SNR = -20\log(2\pi f_{IN} t_J)dB$$

where f_{IN} is the frequency of an input sine wave and t_J is the root-mean-square jitter due to the clock, the analog input and the A/D aperture jitter. To minimize clock jitter, use a clean clock source such as a crystal oscillator, treat the clock signals as sensitive analog traces and use dedicated packages with good supply bypassing for any clock drivers.

Board Layout

To obtain the best performance from the LTC1740, a printed circuit board with a ground plane is required. Layout for the printed circuit board should ensure that digital and analog signal lines are separated as much as possible. In particular, care should be taken not to run any digital track alongside an analog signal track.

An analog ground plane separate from the logic system ground should be placed under and around the ADC. Pins 6, 7, 10, 31, 34 (GND), Pins 11, 28 (OGND) and all other analog grounds should be connected to this ground plane. In single supply mode, Pins 29, 30 (V_{SS}) should also be connected to this ground plane. All bypass capacitors for the LTC1740 should also be connected to this ground plane (Figure 12). The digital system ground should be connected to the analog ground plane at only one point, near the OGND pin (Pin 28).

The analog ground plane should be as close to the ADC as possible. Care should be taken to avoid making holes in the analog ground plane under and around the part. To accomplish this, we recommend placing vias for power and signal traces outside the area containing the part and the decoupling capacitors (Figure 13).

Supply Bypassing

High quality, low series resistance ceramic 1µF capacitors should be used at the V_{DD} pins, V_{CM} and V_{REF}. If V_{SS} is connected to –5V it should also be bypassed to ground with 1µF. In single supply operation V_{SS} should be shorted to the ground plane as close to the part as possible. OV_{DD} requires a 1µF decoupling capacitor to ground. Surface mount capacitors such as the AVX 0805ZC105KAT provide excellent bypassing in a small board space. The traces connecting the pins and the bypass capacitors must be kept short and should be made as wide as possible.

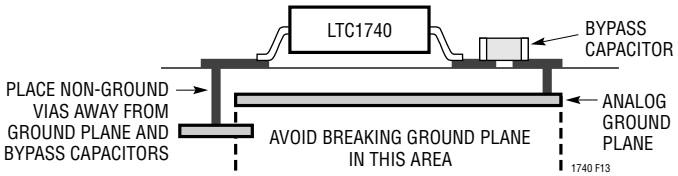


Figure 13. Cross Section of the LTC1740 Printed Circuit Board

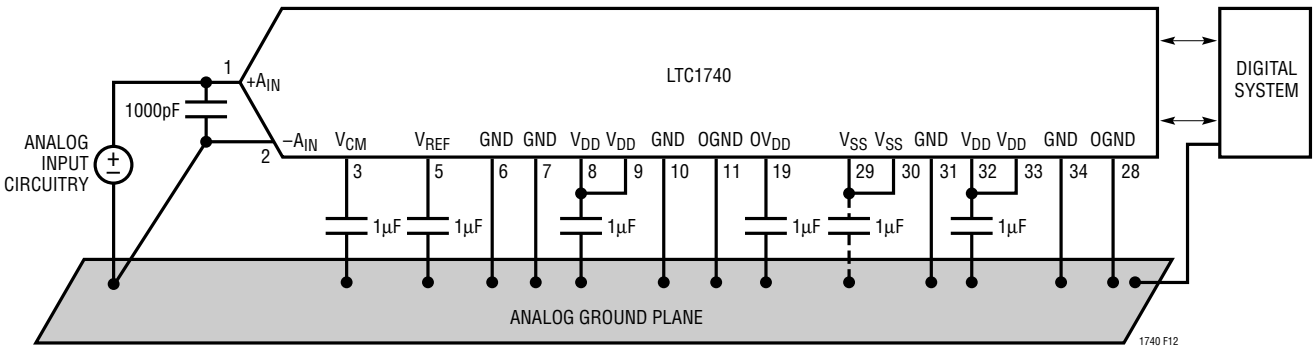
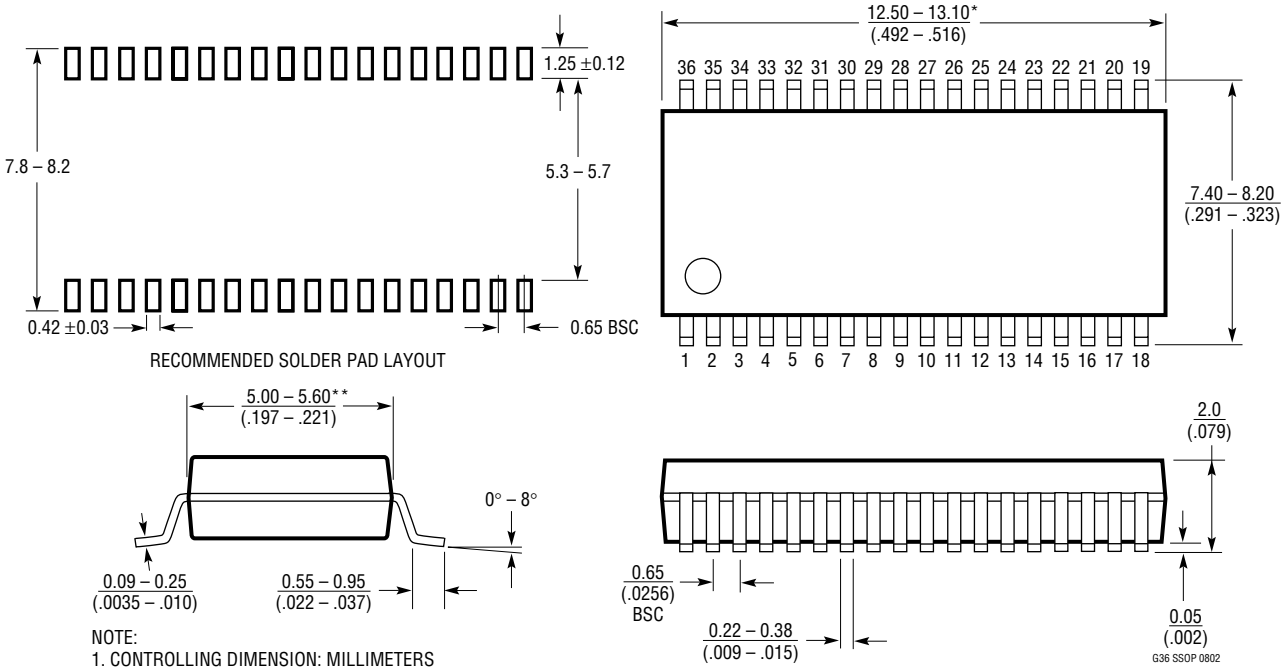


Figure 12. Power Supply Grounding

PACKAGE DESCRIPTION

G Package
36-Lead Plastic SSOP (5.3mm)
(Reference LTC DWG # 05-08-1640)



NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN $\frac{\text{MILLIMETERS}}{(\text{INCHES})}$
3. DRAWING NOT TO SCALE
*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .152mm (.006") PER SIDE
**DIMENSIONS DO NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED .254mm (.010") PER SIDE

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1405	12-Bit, 5Msps Sampling ADC with Parallel Output	Pin Compatible with the LTC1420
LTC1406	8-Bit, 20Msps ADC	Undersampling Capability up to 70MHz
LTC1411	14-Bit, 2.5Msps ADC	5V, No Pipeline Delay, 80dB SINAD
LTC1412	12-Bit, 3Msps, Sampling ADC	±5V, No Pipeline Delay, 72dB SINAD
LTC1414	14-Bit, 2.2Msps ADC	±5V, 81dB SINAD and 95dB SFDR
LTC1420	12-Bit, 10Msps ADC	71dB SINAD and 83dB SFDR at Nyquist
LT1461	Micropower Precision Series Reference	0.04% Max Initial Accuracy, 3ppm/°C Drift
LTC1666	12-Bit, 50Msps DAC	Pin Compatible with the LTC1668, LTC1667
LTC1667	14-Bit, 50Msps DAC	Pin Compatible with the LTC1668, LTC1666
LTC1668	16-Bit, 50Msps DAC	16-Bit, No Missing Codes, 90dB SINAD, –100dB THD
LTC1741	12-Bit, 65Msps ADC	Pin Compatible with the LTC1748
LTC1742	14-Bit, 65Msps ADC	Pin Compatible with the LTC1748
LTC1743	12-Bit, 50Msps ADC	Pin Compatible with the LTC1748
LTC1744	14-Bit, 50Msps ADC	Pin Compatible with the LTC1748
LTC1745	12-Bit, 25Msps ADC	Pin Compatible with the LTC1748
LTC1746	14-Bit, 25Msps ADC	Pin Compatible with the LTC1748
LTC1747	12-Bit, 80Msps ADC	Pin Compatible with the LTC1748
LTC1748	14-Bit, 80Msps ADC	76.3dB SNR and 90dB SFDR
LT1807	325MHz, Low Distortion Dual Op Amp	Rail-to-Rail Input and Output

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