10-Bit Rail-to-Rail Micropower DAC with 2-Wire Interface

FEATURES

- **Micropower 10-Bit DAC in SOT-23**
- **Low Operating Current: 60μA**
- **Ultralow Power Shutdown Mode: 10μA**
- **2-Wire Serial Interface Compatible with SMBus and I²C™**
- Single 2.7V to 5.5V Operation
- **Selectable Internal Reference or Ratiometric to V_{CC}**
- Buffered True Rail-to-Rail Voltage Output
- **Maximum DNL Error: 0.75LSB**
- Power-On Reset
- **8 User Selectable Addresses (MSOP Package)**
- 0.6V V_{IL} and 1.4V V_{IH} for SDA and SCL
- **Small 5-Lead SOT-23 and 8-Lead MSOP Packages**

APPLICATIONS

- Digital Calibration
- Offset/Gain Adjustment
- Industrial Process Control
- Automatic Test Equipment
- Arbitrary Function Generators
- Battery-Powered Data Conversion Products

DESCRIPTION

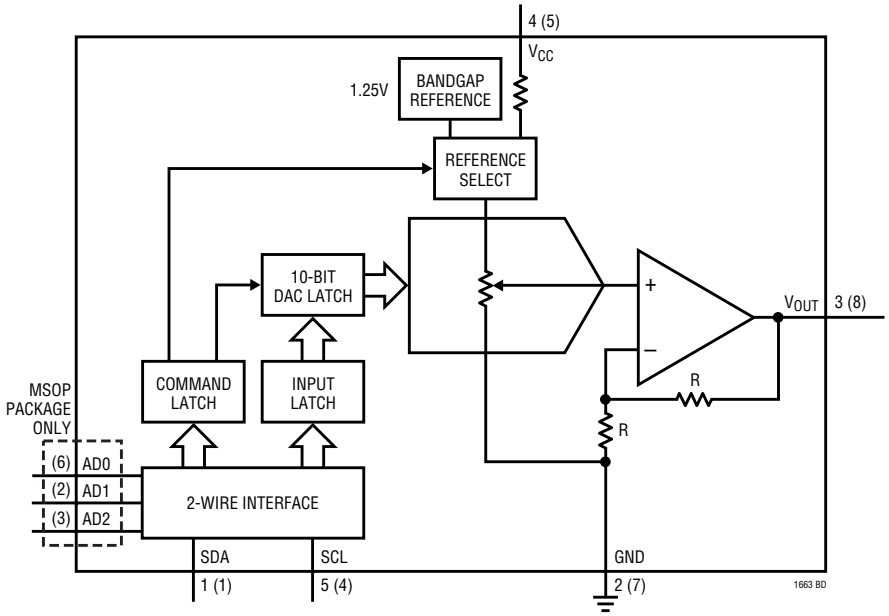
The LTC®1663 is a 10-bit voltage output DAC with true buffered rail-to-rail output voltage capability. It operates from a single supply with a range of 2.7V to 5.5V. The reference for the DAC is selectable between the supply voltage or an internal bandgap reference. Selecting the internal bandgap reference will set the full-scale output voltage range to 2.5V. Selecting the supply as the reference sets the output voltage range to the supply voltage.

The part features a simple 2-wire serial interface compatible with SMBus and I²C that allows communication between many devices. The internal data registers are double buffered to allow for simultaneous update of several devices at once. The DAC can be put in low current power-down mode for use in power conscious systems.

Power-on reset ensures the DAC output is at 0V when power is initially applied, and all internal registers are cleared.

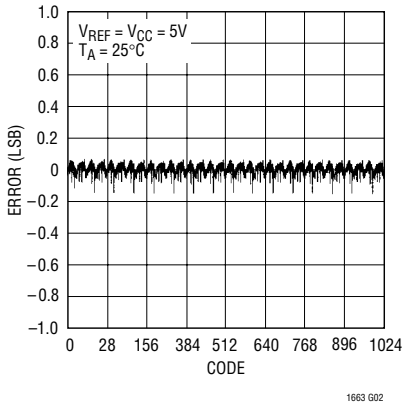
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I²C is a trademark of Philips Electronics N.V.

BLOCK DIAGRAM



NOTE: PIN NUMBERS IN PARENTHESES REFER TO THE MSOP PACKAGE

Differential Nonlinearity (DNL)

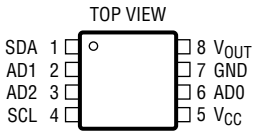


ABSOLUTE MAXIMUM RATINGS (Note 1)

V_{CC} to GND ..... –0.3V to 7.5V
SDA, SCL .....–0.3V to 7.5V
AD0, AD1, AD2 (MSOP Only) ..... –0.3V to (V_{CC} + 0.3V)
V_{OUT} ..... –0.3V to (V_{CC} + 0.3V)

Operating Temperature Range
LTC1663C ..... 0°C to 70°C
LTC1663I ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

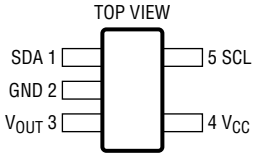
PACKAGE/ORDER INFORMATION



MS8 PACKAGE
8-LEAD PLASTIC MSOP

T_{JMAX} = 125°C, θ_{JA} = 150°C/W

ORDER PART NUMBER
LTC1663CMS8 LTC1663IMS8
MS8 PART MARKING
LTEQ LTJJ



S5 PACKAGE
5-LEAD PLASTIC SOT-23

T_{JMAX} = 125°C, θ_{JA} = 250°C/W

ORDER PART NUMBER
LTC1663CS5
S5 PART MARKING
LTEP

Consult factory for Military grade parts.

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 2.7V to 5.5V, V_{CC} set as reference, V_{OUT} unloaded, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
DAC							
	Resolution		●	10			Bits
	Monotonicity	(Note 2)	●	10			Bits
DNL	Differential Nonlinearity	Guaranteed Monotonic (Note 2)	●		±0.2	±0.75	LSB
INL	Integral Nonlinearity	(Note 2)	●		±0.5	±2.5	LSB
V_{OS}	Offset Error	Measured at Code 20	●		±10	±30	mV
V_{OSTC}	Offset Error Temperature Coefficient				±15		µV/°C
FSE	Full-Scale Error	Reference Set to V_{CC} Reference Set to Internal Bandgap	● ●		±3 ±3	±15 ±15	LSB LSB
V_{OUT}	DAC Output Span	Reference Set to V_{CC} Reference Set to Internal Bandgap			0 to V_{CC} 0 to 2.5		V V
V_{FSTC}	Full-Scale Voltage Temperature Coefficient				±30		µV/°C
PSRR	Power Supply Rejection Ratio	Reference Set to Internal Bandgap, Code = 1023			±0.4		LSB/V
Power Supply							
V_{CC}	Positive Supply Voltage		●	2.7		5.5	V
I_{CC}	Supply Current	V_{CC} = 3V (Note 3) V_{CC} = 5V (Note 3)	● ●		60 75	100 125	µA µA
I_{SD}	Supply Current in Shutdown Mode	(Note 3)	●		10	16	µA
Op Amp DC Performance							
	Short-Circuit Current (Sourcing)	V_{OUT} Shorted to GND, Input Code = 1023	●		25	100	mA
	Short-Circuit Current (Sinking)	V_{OUT} Shorted to V_{CC}, Input Code = 0	●		30	120	mA
	Output Impedance to GND	Input Code = 0, V_{CC} = 5V Input Code = 0, V_{CC} = 3V In Shutdown Mode			65 150 500		Ω Ω kΩ

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 2.7V to 5.5V, V_{CC} set as reference, V_{OUT} unloaded, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	Output Impedance to V_{CC}	Input Code = 1023, V_{CC} = 5V Input Code = 1023, V_{CC} = 3V			80 120		Ω Ω
AC Performance							
	Voltage Output Slew Rate	Rising (Notes 4, 5) Falling (Notes 4, 5)			0.75 0.25		V/µs V/µs
	Voltage Output Settling Time	To ±0.5LSB (Notes 4, 5)			30		µs
	Digital Feedthrough				0.75		nV • s
	Digital-to-Analog Glitch Impulse	1LSB Change Around Major Carry			70		nV • s
Digital Inputs SCL, SDA							
V_{IH}	High Level Input Voltage		●	1.4			V
V_{IL}	Low Level Input Voltage		●			0.6	V
V_{LTH}	Logic Threshold Voltage				1		V
I_{LEAK}	Digital Input Leakage	V_{CC} = 5.5V and 0V, V_{IN} = GND to V_{CC}	●			±1	µA
C_{IN}	Digital Input Capacitance	(Note 7)	●			10	pF
Digital Output SDA							
V_{OL}	Digital Output Low Voltage	I_{PULLUP} = 350µA	●			0.4	V
Address Inputs AD0, AD1, AD2 (MSOP Only)							
I_{UP}	Address Pin Pull-Up Current	V_{IN} = 0V	●		0.5	1.5	µA
V_{IH}	High Level Input Voltage		●	V_{CC} – 0.3			V
V_{IL}	Low Level Input Voltage		●			0.8	V

TIMING CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 2.7V to 5.5V, V_{CC} set as reference, V_{OUT} unloaded, unless otherwise noted.

SYMBOL	PARAMETER		MIN	TYP	MAX	UNITS
SMBus Timing Characteristics (Notes 6, 7)						
f_{SMB}	SMBus Operating Frequency	●	10		100	kHz
t_{BUF}	Bus Free Time Between Stop and Start Condition	●	4.7			µs
$t_{HD, STA}$	Hold Time After (Repeated) Start Condition	●	4.0			µs
$t_{SU, STA}$	Repeated Start Condition Setup Time	●	4.7			µs
$t_{SU, STO}$	Stop Condition Setup Time	●	4.0			µs
$t_{HD, DAT}$	Data Hold Time	●	300			ns
$t_{SU, DAT}$	Data Setup Time	●	250			ns
t_{LOW}	Clock Low Period	●	4.7			µs
t_{HIGH}	Clock High Period	●	4.0		50	µs
t_f	Clock, Data Fall Time	●			300	ns
t_r	Clock, Data Rise Time	●			1000	ns

Note 1: Absolute maximum ratings are those values beyond which the life of a device may be impaired.

Note 2: Nonlinearity and monotonicity are defined from code 20 to code 1003 (full scale). See Applications Information.

Note 3: Digital inputs at 0V or V_{CC}.

Note 4: Load is 10kΩ in parallel with 100pF.

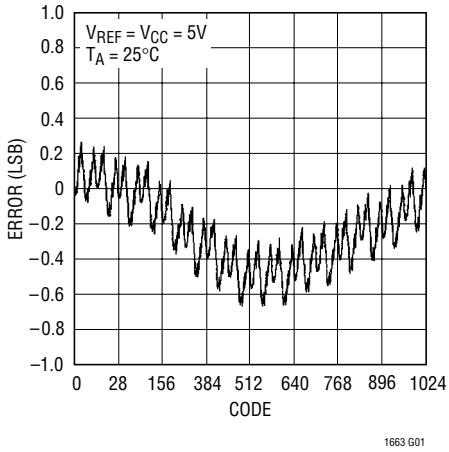
Note 5: V_{CC} = V_{REF} = 5V. DAC switched between 0.1V_{FS} and 0.9V_{FS}, i.e., codes k = 102 and k = 922.

Note 6: All values are referenced to V_{IH} and V_{IL} levels.

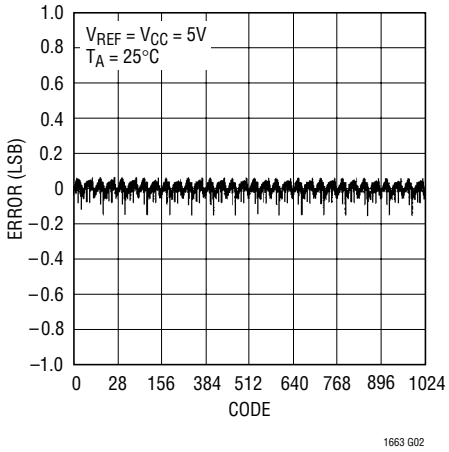
Note 7: Guaranteed by design and not subject to test.

TYPICAL PERFORMANCE CHARACTERISTICS

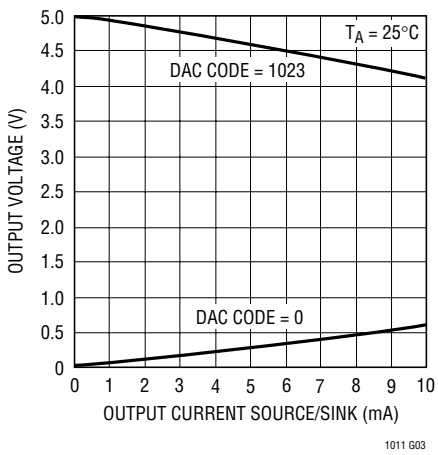
Integral Nonlinearity (INL)



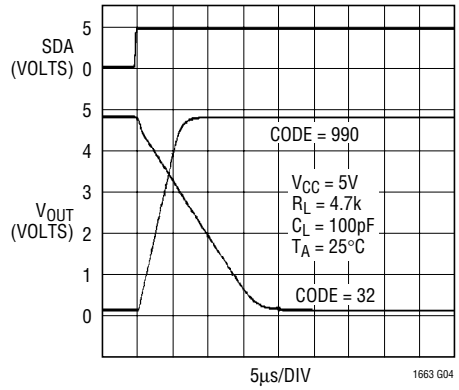
Differential Nonlinearity (DNL)



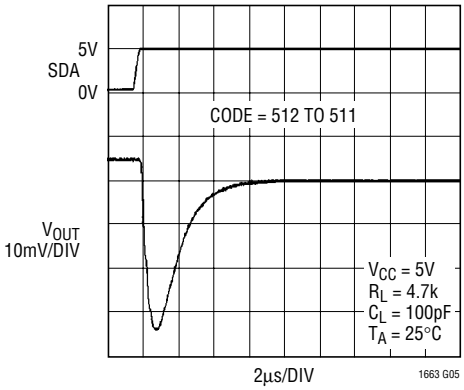
Source and Sink Current Capability with $V_{CC} = 5V$



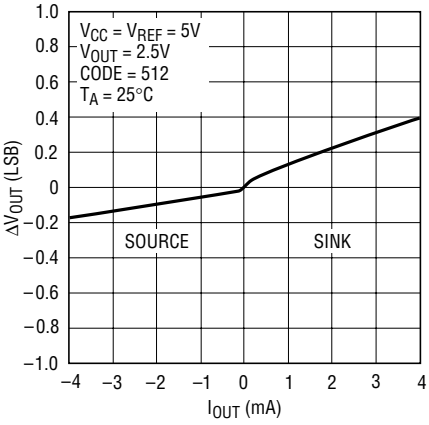
Large-Signal Step Response



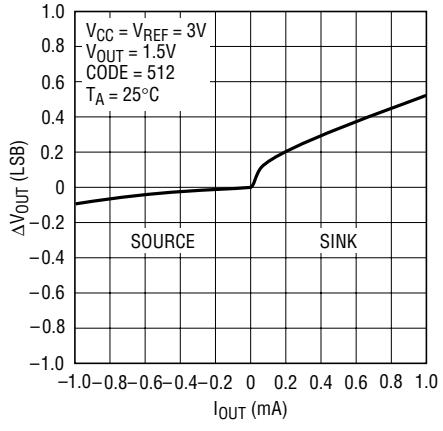
Midscale Glitch



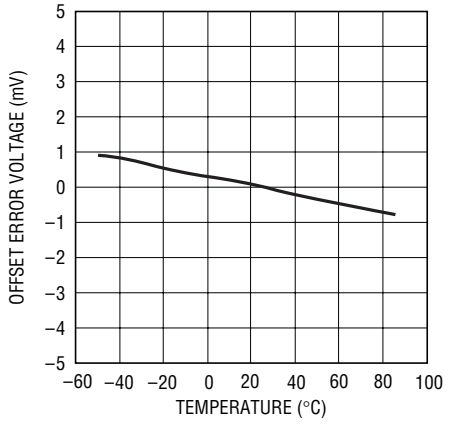
Load Regulation vs Output Current



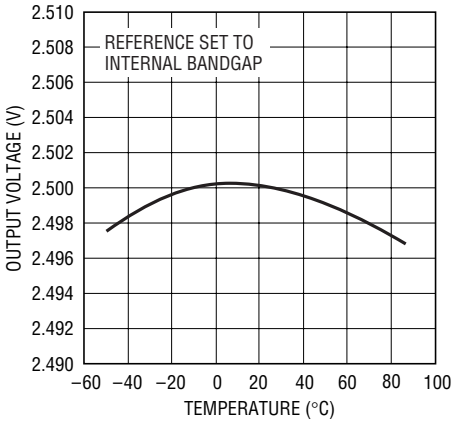
Load Regulation vs Output Current



Offset Error Voltage vs Temperature



Full-Scale Output Voltage vs Temperature



PIN FUNCTIONS

SDA (Pin 1, Pin 1 on SOT-23): Serial Data Bidirectional Pin. Data is shifted into the SDA pin and acknowledged by the SDA pin. High impedance pin while data is shifted in. Open-drain N-channel output during acknowledgment. Requires a pull-up resistor or current source to V_{CC}.

AD1 (Pin 2): Slave Address Select Bit 1. Tie this pin to either V_{CC} or GND to modify the corresponding bit of the LTC1663's slave address.

AD2 (Pin 3): Slave Address Select Bit 2. Tie this pin to either V_{CC} or GND to modify the corresponding bit of the LTC1663's slave address.

SCL (Pin 4, Pin 5 on SOT-23): Serial Clock Input Pin. Data is shifted into the SDA pin at the rising edges of the clock. This high impedance pin requires a pull-up resistor or current source to V_{CC}.

V_{CC} (Pin 5, Pin 4 on SOT-23): Power Supply. $2.7V \leq V_{CC} \leq 5.5V$. Also used as the reference voltage input when the part is programmed to use V_{CC} as the reference.

AD0 (Pin 6): Slave Address Select Bit 0. Tie this pin to either V_{CC} or GND to modify the corresponding bit of the LTC1663's slave address.

GND (Pin 7, Pin 2 on SOT-23): System Ground.

V_{OUT} (Pin 8, Pin 3 on SOT-23): Voltage Output. Buffered rail-to-rail DAC output.

DEFINITIONS

Differential Nonlinearity (DNL): The difference between the measured change and the ideal 1LSB change for any two adjacent codes. The DNL error between any two codes is calculated as follows:

$$DNL = (\Delta V_{OUT} - LSB)/LSB$$

Where ΔV_{OUT} is the measured voltage difference between two adjacent codes.

Digital Feedthrough: The glitch that appears at the analog output caused by AC coupling from the digital inputs when they change state. The area of the glitch is specified in (nV)(sec).

Full-Scale Error (FSE): The deviation of the actual full-scale voltage from ideal. FSE includes the effects of offset and gain errors (see Applications Information).

Integral Nonlinearity (INL): The deviation from a straight line passing through the endpoints of the DAC transfer curve (Endpoint INL). Because the output cannot go below zero, the linearity is measured between full scale and the lowest code that guarantees the output will be greater than zero. The INL error at a given input code is calculated as follows:

$$INL = [V_{OUT} - V_{OS} - (V_{FS} - V_{OS})(code/1023)]/LSB$$

Where V_{OUT} is the output voltage of the DAC measured at the given input code.

Least Significant Bit (LSB): The ideal voltage difference between two successive codes.

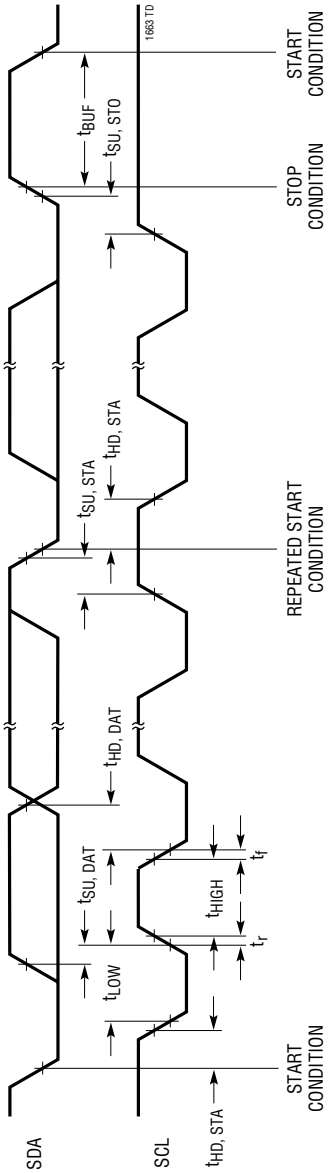
$$LSB = V_{REF}/1024$$

Resolution (n): Defines the number of DAC output states (2^n) that divide the full-scale range. Resolution does not imply linearity.

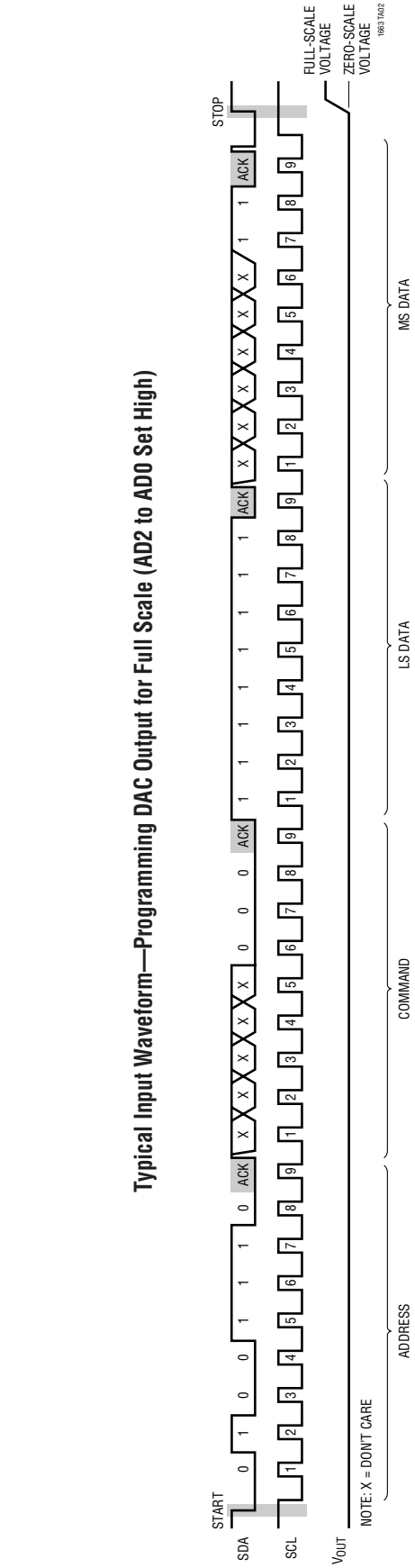
Voltage Offset Error (V_{OS}): Nominally, the voltage at the output when the DAC is loaded with all zeros. A single supply DAC can have a true negative offset, but the output cannot go below zero (see Applications Information).

For this reason, single supply DAC offset is measured at the lowest code that guarantees the output will be greater than zero.

TIMING DIAGRAM

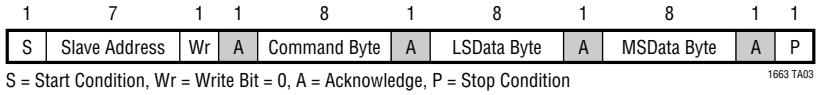


Typical Input Waveform—Programming DAC Output for Full Scale (AD2 to AD0 Set High)



APPLICATIONS INFORMATION

Write Word Protocol Used by the LTC1663



Serial Digital Interface

The LTC1663 communicates with a host (master) using the standard 2-wire interface. The Timing Diagram shows the timing relationship of the signals on the bus. The two bus lines, SDA and SCL, must be high when the bus is not in use. External pull-up resistors or current sources, such as the LTC1694 SMBus Accelerator, are required on these lines.

The LTC1663 is a receive-only (slave) device. The master can communicate with the LTC1663 using the Quick Command, Send Byte or Write Word protocols as explained later.

The START and STOP Conditions

When the bus is not in use, both SCL and SDA must be high. A bus master signals the beginning of a communication to a slave device by transmitting a START condition. A START condition is generated by transitioning SDA from high to low while SCL is high.

When the master has finished communicating with the slave, it issues a STOP condition. A STOP condition is generated by transitioning SDA from low to high while SCL is high. The bus is then free for communication with another SMBus device.

Acknowledge

The Acknowledge signal is used for handshaking between the master and the slave. An Acknowledge (active LOW) generated by the slave lets the master know that the latest byte of information was received. The Acknowledge related clock pulse is generated by the master. The master releases the SDA line (HIGH) during the Acknowledge clock pulse. The slave-receiver must pull down the SDA line during the Acknowledge clock pulse so that it remains a stable LOW during the HIGH period of this clock pulse.

Write Word Protocol

The master initiates communication with the LTC1663 with a START condition and a 7-bit address followed by the Write Bit (Wr) = 0. The LTC1663 acknowledges and the master delivers the command byte. The LTC1663 acknowledges and latches the command byte into the command byte input register. The master then delivers the least significant data byte. Again the LTC1663 acknowledges and the data is latched into the least significant data byte input register. The master then delivers the most significant data byte. The LTC1663 acknowledges once more and latches the data into the most significant data byte input register. Lastly, the master terminates the communication with a STOP condition. On the reception of the STOP condition, the LTC1663 transfers the input register information to output registers and the DAC output is updated.

Slave Address (MSOP Package Only)

The LTC1663 can respond to one of eight 7-bit addresses. The first 4 bits (MSBs) have been factory programmed to 0100. The three address bits, AD2, AD1 and AD0 are programmed by the user and determine the LSBs of the slave address, as shown in the table below:

AD2	AD1	AD0	0100 xxx
L	L	L	0100 000
L	L	H	0100 001
L	H	L	0100 010
L	H	H	0100 011
H	L	L	0100 100
H	L	H	0100 101
H	H	L	0100 110
H	H	H	0100 111

APPLICATIONS INFORMATION

Slave Address (SOT-23 Package)

The slave address for the SOT-23 package has been factory programmed to be "0100 000." If another address is required, please consult the factory.

Command Byte

7	6	5	4	3	2	1	0
X	X	X	X	X	BG	SD	SY

SY	1 0	Allows update on Acknowledge of SYNC Address only Update on Stop condition only (Power-On Default)
SD	1 0	Puts the device in power-down mode Puts the device in standard operating mode (Power-On Default)
BG	1 0	Selects the internal bandgap reference Selects the supply as the reference (Power-On Default)
X	X	Don't Care

The stop condition normally initiates the update of the DAC's output latches. This allows for simultaneous update of more than one DAC or other devices on the bus. This can be overridden by setting the "SY" bit of the command byte. Setting this bit sets the device to update the DAC output latches at the reception of a SYNC address quick command. The actual update occurs on the rising edge of SCL during the Acknowledge. In this way, all devices can update on the reception of the SYNC address quick command instead of the STOP condition.

A Shutdown (SD) bit = HIGH will put the device in a low power state but retain all data latch information. Shutdown will occur at the reception of a STOP condition. This way shutdown could be synchronized to other devices. The output impedance of the DAC will go to a high impedance state (≈500kΩ to GND).

The Bandgap (BG) bit when set to "0" selects the DAC supply voltage as its voltage reference. The full-scale output of the DAC with this setting is equal to the supply voltage. When the BG bit is set to "1," the internal bandgap reference (≈1.25V) is selected as the DAC's reference. The full-scale output voltage for this setting is 2.5V.

Data Bytes

Least Significant Data Byte

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

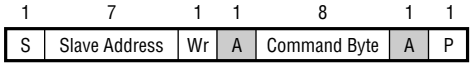
Most Significant Data Byte

7	6	5	4	3	2	1	0
X	X	X	X	X	X	D9	D8

X = Don't care

Send Byte Protocol

The Send Byte protocol used on the LTC1663 is actually a subset of the Write Word protocol described previously. The Send Byte protocol can only be used to send the command byte information to the LTC1663.



S = Start Condition, Wr = Write Bit, A = Acknowledge, P = Stop Condition

1663 TA04

The Send Byte protocol is also used whenever the Write Word protocol is interrupted for any reason. Reception of a START or STOP condition after the Acknowledge of the command byte, but before the Acknowledge of the last data byte, will cause both data bytes to be ignored and the command byte to be accepted.

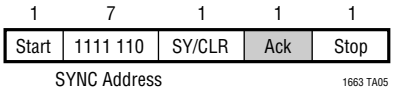
Reception of a START or STOP condition before the Acknowledge of the command byte will cause the interrupted command byte to be ignored.

APPLICATIONS INFORMATION

SYNC Address/Quick Command

In addition to the slave address, the LTC1663 has an address that can be shared by other devices so that they may be updated synchronously. The address is called to the SYNC address and uses the quick command protocol.

The SYNC Address is 1111 110



SY/CLR	1	Update output latches on rising edge of SCL during Acknowledge of SYNC Address
	0	Clear all internal latches on rising edge of SCL during Acknowledge of SYNC Address

The SY/CLR bit set high only has meaning when the "SY" bit of the command byte was previously set HIGH. On the otherhand, the SY/CLR bit set LOW will always clear the part, independent of the state of the "SY" bit in the command byte.

Input Threshold

Anticipating the trend toward lower supply voltages, the SMBus is specified with a V_{IH} of 1.4V and a V_{IL} of 0.6V. While some SMBus parts may violate this stringent SMBus specification by allowing a higher V_{IH} value for a correspondingly higher input supply voltage, the LTC1663 meets and maintains the constant SMBus input threshold specification across the entire supply voltage range of 2.7V to 5.5V. The logic input threshold is designed to be 1V with 50mV of hysteresis.

Voltage Output

The output amplifier contained in the LTC1663 can source or sink up to 5mA. The output stage swings to within a few millivolts of either supply rail when unloaded and has an equivalent output resistance of 85Ω when driving a load to the rails. The output amplifier is stable driving capacitive loads up to 1000pF.

A small resistor placed in series with the output can be used to achieve stability for any load capacitance greater than 1000pF. For example, a 0.1µF load can be driven by the LTC1663 if a 110Ω series resistance is used. The phase margin of the resulting circuit is 45° and increases monotonically from this point if larger values of resistance, capacitance or both are substituted for the values given.

Rail-to-Rail Output Considerations

As in any rail-to-rail device, the output is limited to voltages within the supply range.

If the DAC offset is negative, the output for the lowest codes limits at 0V as shown in Figure 1b.

Similarly, limiting can occur near full scale when V_{CC} is used as the reference. If $V_{REF} = V_{CC}$ and the DAC full-scale error (FSE) is positive, the output for the highest codes limits at V_{CC} as shown in Figure 1c. No full-scale limiting can occur if the internal reference is used.

Offset and linearity are defined and tested over the region of the DAC transfer function where no output limiting can occur.

Internal Reference

In applications where a predictable output is required that is independent of supply voltage, the LTC1663 has a user-selectable internal reference. Selecting the internal reference will set the full-scale output voltage to 2.5V. This can be useful in applications where the supply voltage is poorly regulated.

Using the LT®1460 Micropower Series Reference as a Power Supply for the LTC1663

In applications where the advantages of using the internal reference are required but the full-scale range needs to be greater than 2.5V, an external series reference can be used. The LT1460 is ideal for use as a power supply for the LTC1663 and can provide 3V, 3.3V and 5V full-scale output voltage ranges. The LT1460 provides accuracy, noise immunity and extended supply range to the LTC1663 when the LTC1663 is operated ratiometric to V_{CC}. Since both parts are available in SOT-23 packages, the PC board space for this application is extremely small. See Figure 2.

APPLICATIONS INFORMATION

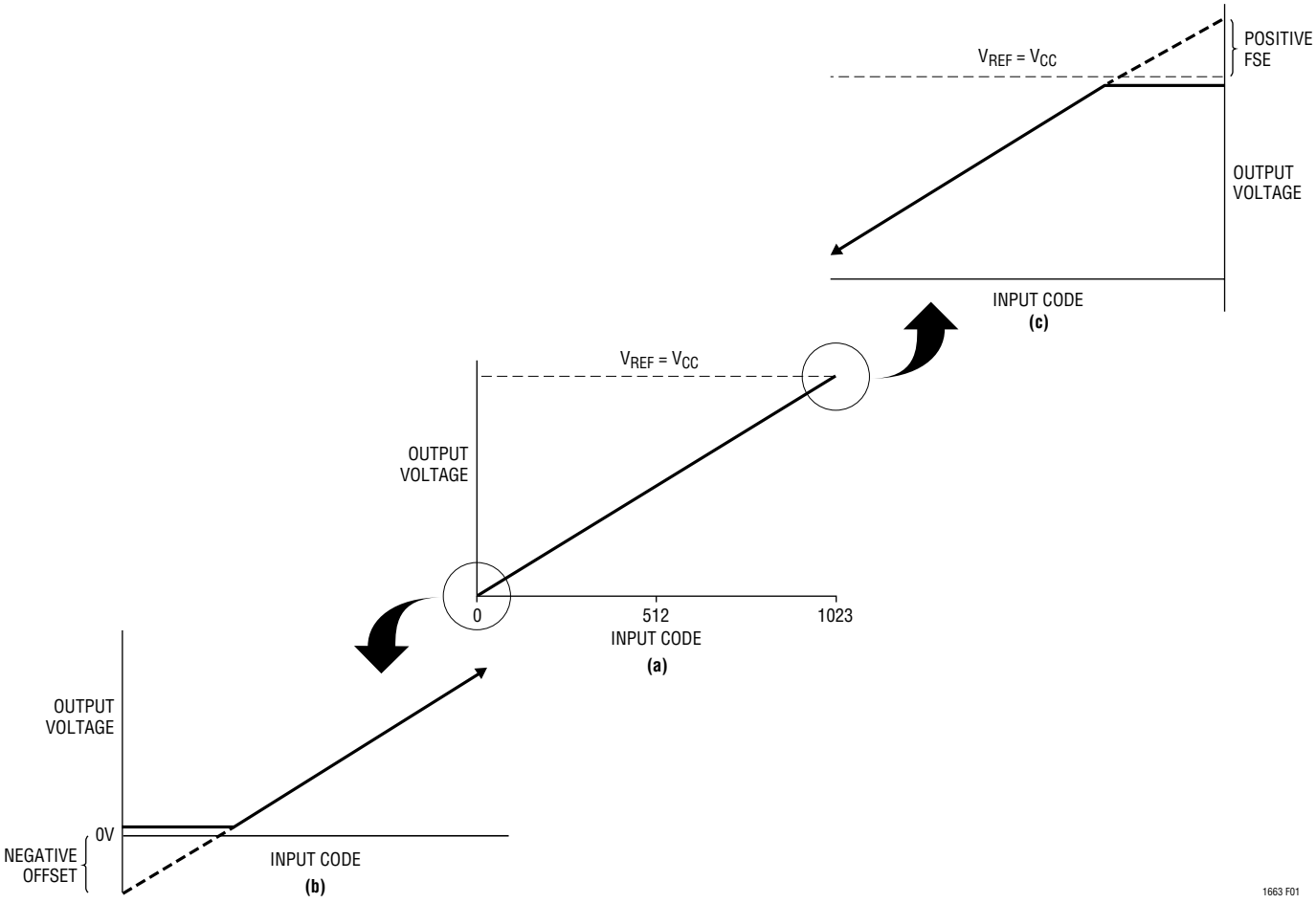


Figure 1. Effects of Rail-to-Rail Operation On a DAC Transfer Curve. (a) Overall Transfer Function (b) Effect of Negative Offset for Codes Near Zero Scale (c) Effect of Positive Full-Scale Error for Input Codes Near Full Scale When $V_{REF} = V_{CC}$

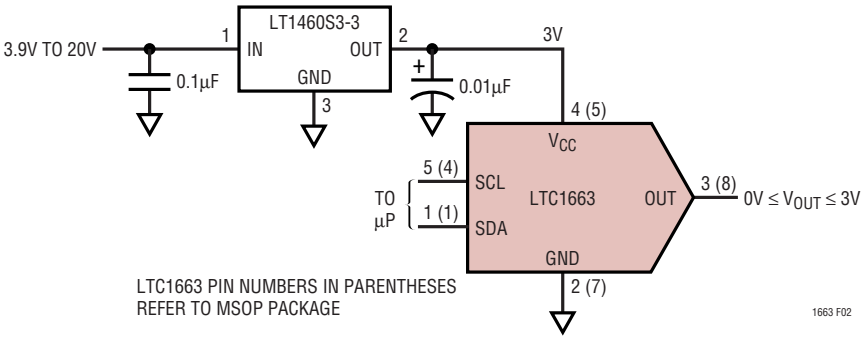
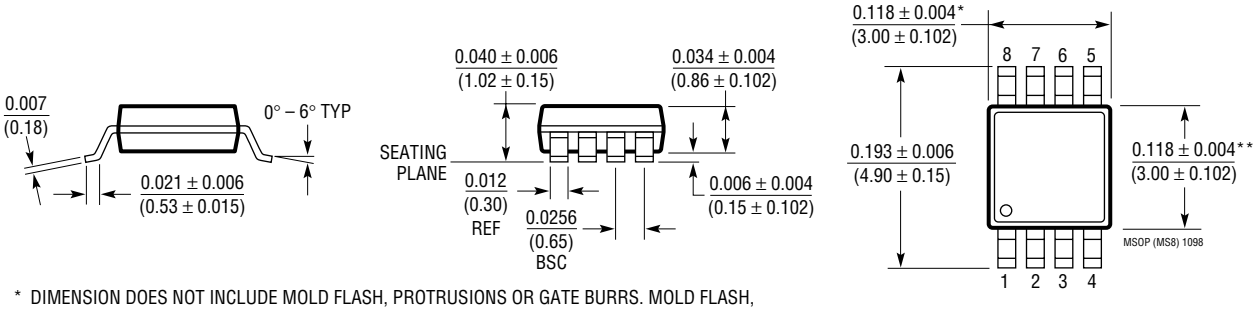


Figure 2. LT1460 As Power Supply for the LTC1663

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

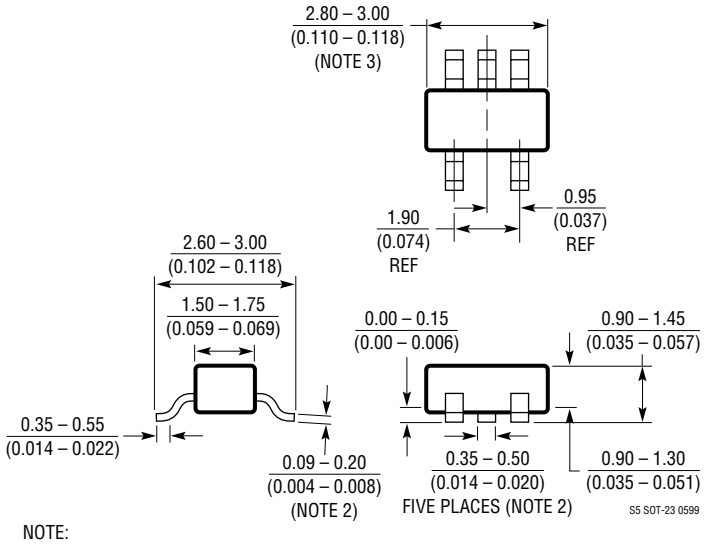
MS8 Package
8-Lead Plastic MSOP
(LTC DWG # 05-08-1660)



* DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

** DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

S5 Package
5-Lead Plastic SOT-23
(LTC DWG # 05-08-1633)

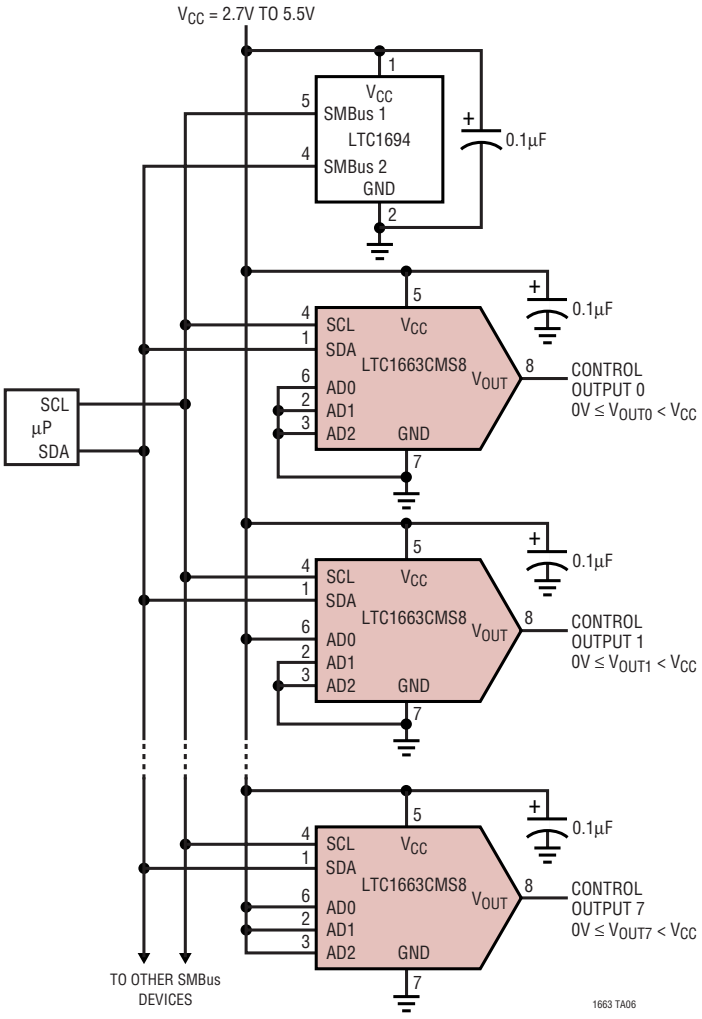


NOTE:
1. DIMENSIONS ARE IN MILLIMETERS
2. DIMENSIONS ARE INCLUSIVE OF PLATING
3. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH AND METAL BURR
4. MOLD FLASH SHALL NOT EXCEED 0.254mm
5. PACKAGE EIAJ REFERENCE IS SC-74A (EIAJ)

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

TYPICAL APPLICATION

Program Up to 8 Control Outputs Per BUS and Place Them Where They Are Needed



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1694	SMBus I^2C Accelerator	Dual SMBus Accelerator with Active AC and DC Pull-Up Current Sources
LTC1694-1	SMBus I^2C Accelerator	Dual SMBus Accelerator with Active AC Pull-Up Current Only
DACs		
LTC1659	Single Rail-to-Rail 12-Bit V_{OUT} DAC in 8-Lead MSOP Package. V_{CC} = 2.7V to 5.5V	Low Power Multiplying V_{OUT} DAC. Output Swings from GND to REF. REF Input Can Be Tied to V_{CC}. 3-Wire Interface.
LTC1660/LTC1664	Octal/Quad 10-Bit V_{OUT} DACs in 16-Pin Narrow SSOP	V_{CC} = 2.7V to 5.5V Micropower Rail-to-Rail Output. 3-Wire Interface.
LTC1661	Dual 10-Bit V_{OUT} in 8-Lead MSOP Package	V_{CC} = 2.7V to 5.5V Micropower Rail-to-Rail Output. 3-Wire Interface.
ADCs		
LTC1285/LTC1288	8-Pin SO, 3V Micropower ADCs	1- or 2-Channel, Autoshutdown
LTC1286/LTC1298	8-Pin SO, 5V Micropower ADCs	1- or 2-Channel, Autoshutdown
LTC1594/LTC1598	4/8-Channel, 5V Micropower 12-Bit ADCs	Low Power, Small Size, Low Cost

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