High Efficiency Low Noise Synchronous Step-Down Switching Regulator

FEATURES

- Dual N-Channel MOSFET Synchronous Drive
- **Programmable Fixed Frequency**
- **Wide V_{IN} Range: 3.5V to 36V Operation**
- **Low Minimum On-Time (≤300ns) for High Frequency, Low Duty Cycle Applications**
- Very Low Dropout Operation: 99% Duty Cycle
- Low Standby Current
- Secondary Feedback Control
- Programmable Soft Start
- Remote Output Voltage Sense
- Logic Controlled Micropower Shutdown: I_Q < 25µA
- Foldback Current Limiting (Optional)
- Current Mode Operation for Excellent Line and Load Transient Response
- Output Voltages from 1.19V to 9V
- Available in 16-Lead Narrow SO and SSOP Packages

APPLICATIONS

- Notebook and Palmtop Computers, PDAs
- Cellular Telephones and Wireless Modems
- Portable Instruments
- Battery-Operated Devices
- DC Power Distribution Systems

DESCRIPTION

The LTC®1435A is a synchronous step-down switching regulator controller that drives external N-channel power MOSFETs using a fixed frequency architecture. A wide duty cycle range of 5% to 99% allows high V_{IN} to low V_{OUT} DC/DC conversion, as well as low dropout operation that extends operating time in battery-operated systems. Burst Mode™ operation provides high efficiency at low load currents.

The operating frequency is set by an external capacitor allowing maximum flexibility in optimizing efficiency. A secondary winding feedback control pin, SFB, guarantees regulation regardless of load on the main output by forcing continuous operation. Burst Mode operation is inhibited when the SFB pin is pulled low, which reduces noise and RF interference.

Soft start is provided by an external capacitor that can be used to properly sequence supplies. The operating current level is user-programmable via an external current sense resistor. Wide input supply range allows operation from 3.5V to 30V (36V maximum).

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Burst Mode is a trademark of Linear Technology Corporation.

TYPICAL APPLICATION

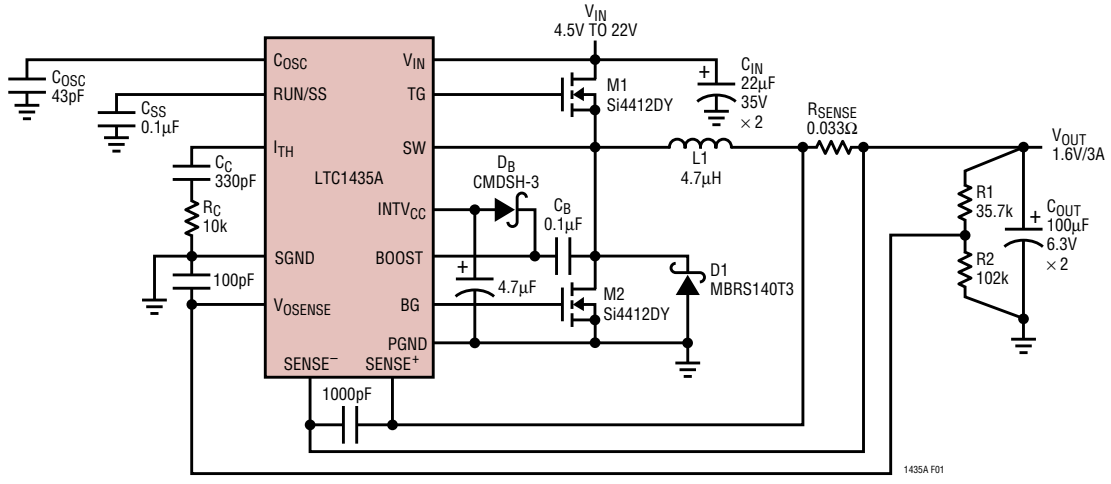
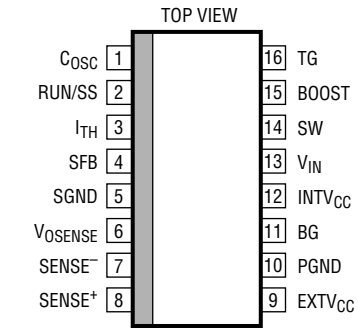


Figure 1. High Efficiency Step-Down Converter

ABSOLUTE MAXIMUM RATINGS

Input Supply Voltage (V_{IN}) ..... 36V to –0.3V
Topside Driver Supply Voltage (BOOST) .... 42V to –0.3V
Switch Voltage (SW) ..... V_{IN} + 5V to –5V
$EXTV_{CC}$ Voltage ..... 10V to –0.3V
$SENSE^+$, $SENSE^-$ Voltages ..... $INTV_{CC}$ + 0.3V to –0.3V
I_{TH}, V_{OSENSE} Voltages ..... 2.7V to –0.3V
SFB, Run/SS Voltages ..... 10V to –0.3V
Peak Driver Output Current < 10µs (TG, BG) 2A
$INTV_{CC}$ Output Current 50mA
Operating Ambient Temperature Range
LTC1435AC ..... 0°C to 70°C
LTC1435AI ..... –40°C to 85°C
Junction Temperature (Note 1) ..... 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



G PACKAGE
16-LEAD PLASTIC SSOP

S PACKAGE
16-LEAD PLASTIC SO

T_{JMAX} = 125°C, θ_{JA} = 130°C/W (G)
T_{JMAX} = 125°C, θ_{JA} = 110°C/W (S)

ORDER PART NUMBER

LTC1435ACG
LTC1435ACS
LTC1435AIG
LTC1435AIS

Consult factory for Military grade parts.

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{IN} = 15V, $V_{RUN/SS}$ = 5V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Main Control Loop							
I_{IN} V_{OSENSE}	Feedback Current	(Note 2)			10	50	nA
V_{OSENSE}	Feedback Voltage	(Note 2)	●	1.178	1.19	1.202	V
$\Delta V_{LINEREG}$	Reference Voltage Line Regulation	V_{IN} = 3.6V to 20V (Note 2)			0.002	0.01	%/V
$\Delta V_{LOADREG}$	Output Voltage Load Regulation	I_{TH} Sinking 5µA (Note 2) I_{TH} Sourcing 5µA	● ●		0.5 –0.5	0.8 –0.8	% %
V_{SFB}	Secondary Feedback Threshold	V_{SFB} Ramping Negative	●	1.16	1.19	1.22	V
I_{SFB}	Secondary Feedback Current	V_{SFB} = 1.5V			–1	–2	µA
V_{OVL}	Output Overvoltage Lockout			1.24	1.28	1.32	V
I_Q	Input DC Supply Current Normal Mode Shutdown	$EXTV_{CC}$ = 5V (Note 3) 3.6V < V_{IN} < 30V $V_{RUN/SS}$ = 0V, 3.6V < V_{IN} < 15V			 280 16	 25	 µA µA
$V_{RUN/SS}$	Run Pin Threshold		●	0.8	1.3	2	V
$I_{RUN/SS}$	Soft Start Current Source	$V_{RUN/SS}$ = 0V		1.5	3	4.5	µA
$\Delta V_{SENSE(MAX)}$	Maximum Current Sense Threshold	V_{OSENSE} = 0V, 5V		130	150	180	mV
$t_{ON(MIN)}$	Minimum On-Time	Tested with Square Wave, $SENSE^-$ = 1.6V, ΔV_{SENSE} = 20mV (Note 5)			250	300	ns
TG t_r TG t_f	TG Transition Time Rise Time Fall Time	 C_{LOAD} = 3000pF C_{LOAD} = 3000pF			 50 50	 150 150	 ns ns
BG t_r BG t_f	BG Transition Time Rise Time Fall Time	 C_{LOAD} = 3000pF C_{LOAD} = 3000pF			 50 40	 150 150	 ns ns
Internal V_{CC} Regulator							
V_{INTVCC}	Internal V_{CC} Voltage	6V < V_{IN} < 30V, V_{EXTVCC} = 4V	●	4.8	5.0	5.2	V
V_{LDO} INT	$INTV_{CC}$ Load Regulation	I_{INTVCC} = 15mA, V_{EXTVCC} = 4V			–0.2	–1	%
V_{LDO} EXT	$EXTV_{CC}$ Voltage Drop	I_{INTVCC} = 15mA, V_{EXTVCC} = 5V			130	230	mV
V_{EXTVCC}	$EXTV_{CC}$ Switchover Voltage	I_{INTVCC} = 15mA, V_{EXTVCC} Ramping Positive	●	4.5	4.7		V

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{IN} = 15V, $V_{RUN/SS}$ = 5V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Oscillator						
f_{OSC}	Oscillator Frequency	C_{OSC} = 100pF (Note 4)	112	125	138	kHz

The ● denotes specifications which apply over the full operating temperature range.

LTC1435ACG/LTC1435ACS: 0°C ≤ T_A ≤ 70°C

LTC1435AIG/LTC1435AIS: –40°C ≤ T_A ≤ 85°C

Note 1: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formula:

LTC1435ACG/LTC1435AIG: $T_J = T_A + (P_D)(130°C/W)$

LTC1435ACS/LTC1435AIS: $T_J = T_A + (P_D)(110°C/W)$

Note 2: The LTC1435A is tested in a feedback loop which servos V_{OSENSE} to the balance point for the error amplifier (V_{ITH} = 1.19V).

Note 3: Dynamic supply current is higher due to the gate charge being delivered at the switching frequency. See Applications Information.

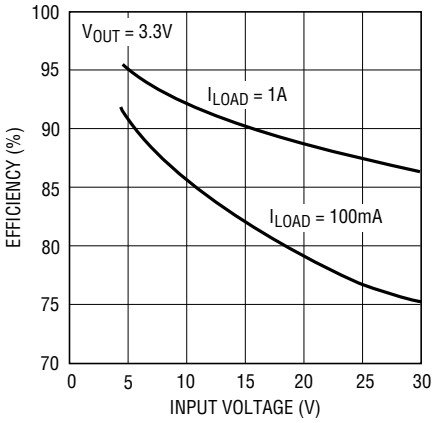
Note 4: Oscillator frequency is tested by measuring the C_{OSC} charge and discharge currents and applying the formula:

$$f_{OSC}\ (kHz) = \left(\frac{8.4(10^8)}{C_{OSC}\ (pF) + 11}\right)\left(\frac{1}{I_{CHG}} + \frac{1}{I_{DIS}}\right)^{-1}$$

Note 5: The minimum on-time test condition corresponds to an inductor peak-to-peak ripple current ≥40% of I_{MAX} (see Minimum On-Time Considerations in the Applications Information section).

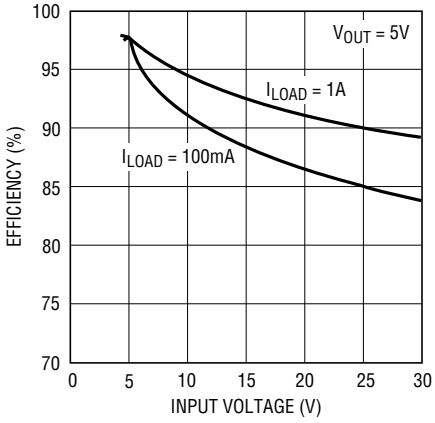
TYPICAL PERFORMANCE CHARACTERISTICS

Efficiency vs Input Voltage
V_{OUT} = 3.3V



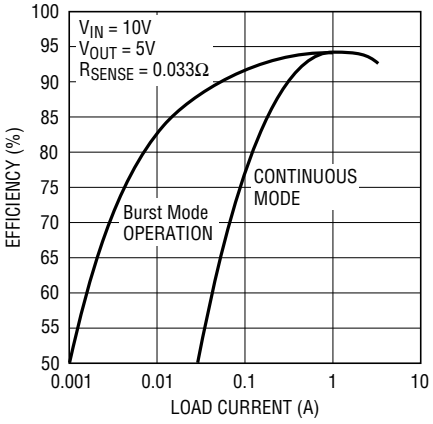
1435A G01

Efficiency vs Input Voltage
V_{OUT} = 5V



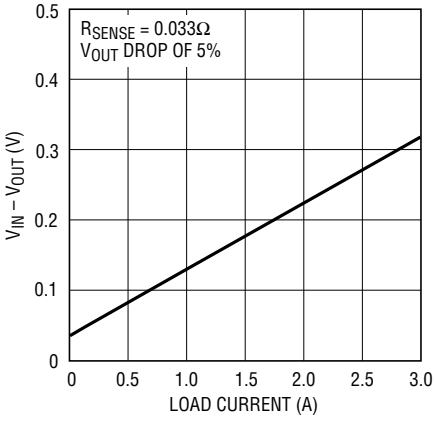
1435A G02

Efficiency vs Load Current



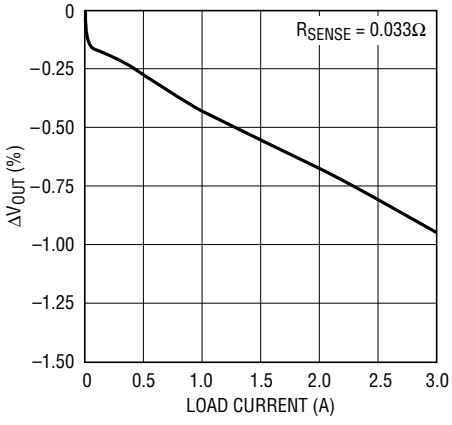
1435A G03

V_{IN} – V_{OUT} Dropout Voltage vs Load Current



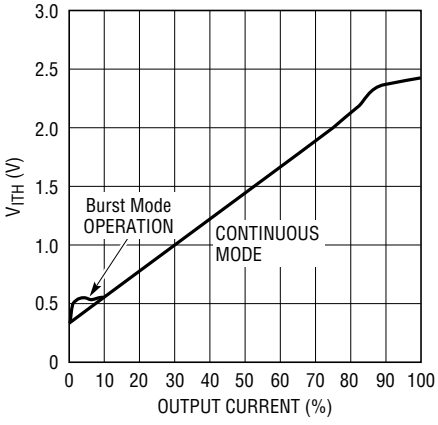
1435A G04

Load Regulation



1435A G05

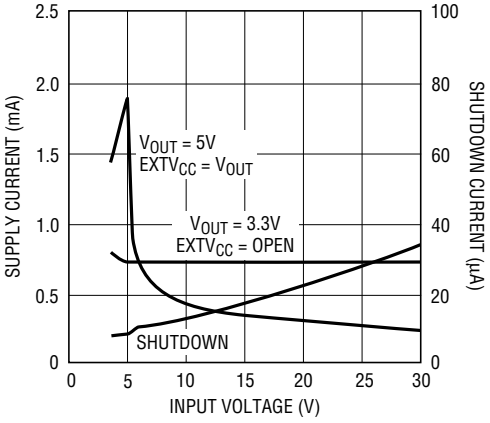
V_{ITH} Pin Voltage vs Output Current



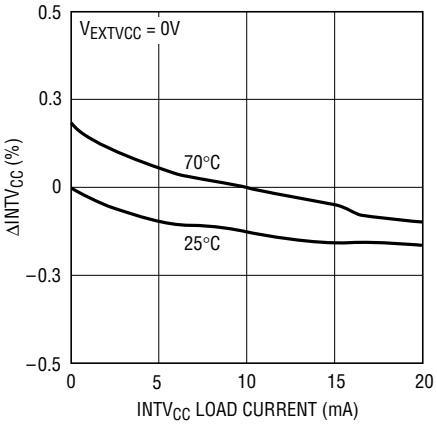
1435A G06

TYPICAL PERFORMANCE CHARACTERISTICS

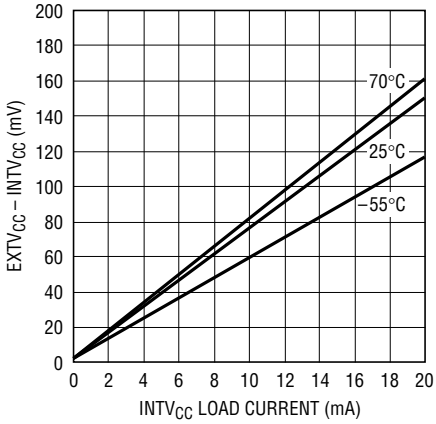
Input Supply and Shutdown Current vs Input Voltage



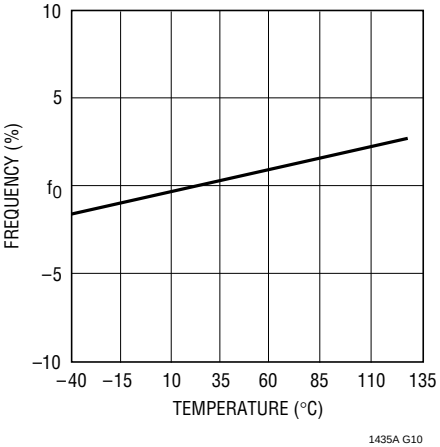
INTVCC Regulation vs INTVCC Load Current



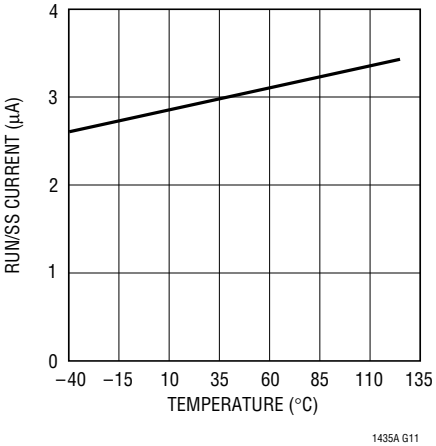
EXTVCC Switch Drop vs INTVCC Load Current



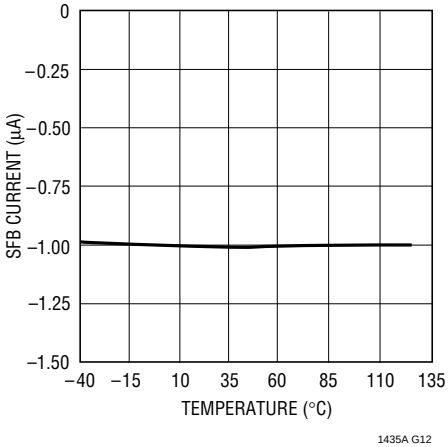
Normalized Oscillator Frequency vs Temperature



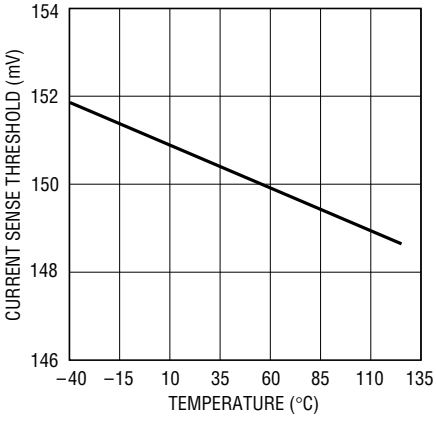
RUN/SS Pin Current vs Temperature



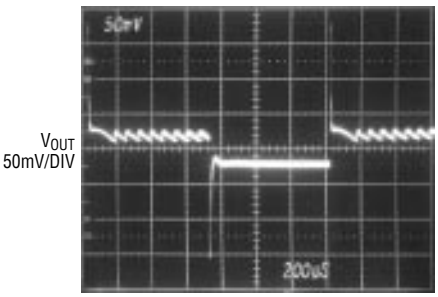
SFB Pin Current vs Temperature



Maximum Current Sense Threshold Voltage vs Temperature



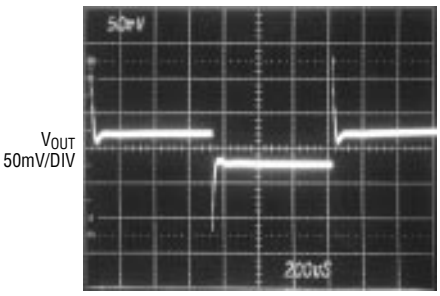
Transient Response



ILOAD = 50mA to 1A

1435A G14

Transient Response

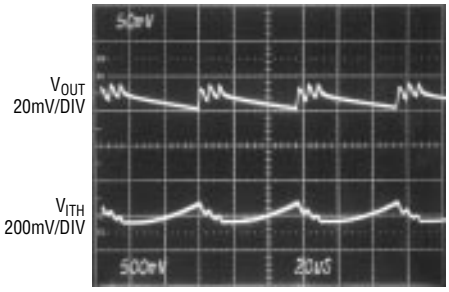


ILOAD = 1A to 3A

1435A G15

TYPICAL PERFORMANCE CHARACTERISTICS

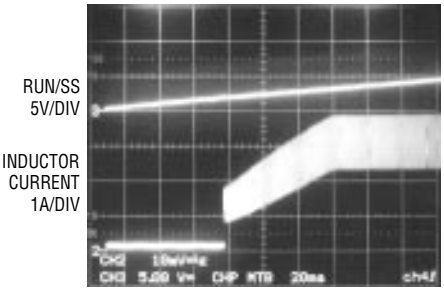
Burst Mode Operation



I_{LOAD} = 50mA

1435A G16

Soft Start: Load Current vs Time



1435A G17

PIN FUNCTIONS

C_{OSC} (Pin 1): External capacitor C_{OSC} from this pin to ground sets the operating frequency.

RUN/SS (Pin 2): Combination of Soft Start and Run Control Inputs. A capacitor to ground at this pin sets the ramp time to full current output. The time is approximately 0.5s/µF. Forcing this pin below 1.3V causes the device to be shut down. In shutdown all functions are disabled.

I_{TH} (Pin 3): Error Amplifier Compensation Point. The current comparator threshold increases with this control voltage. Nominal voltage range for this pin is 0V to 2.5V.

SFB (Pin 4): Secondary Winding Feedback Input. Normally connected to a feedback resistive divider from the secondary winding. This pin should be tied to: ground to force continuous operation; $INTV_{CC}$ in applications that don't use a secondary winding; and a resistive divider from the output in applications using a secondary winding.

SGND (Pin 5): Small-Signal Ground. Must be routed separately from other grounds to the (–) terminal of C_{OUT}.

V_{OSENSE} (Pin 6): Receives the feedback voltage from an external resistive divider across the output.

$SENSE^-$ (Pin 7): The (–) Input to the Current Comparator.

$SENSE^+$ (Pin 8): The (+) Input to the Current Comparator. Built-in offsets between $SENSE^-$ and $SENSE^+$ pins in conjunction with R_{SENSE} set the current trip thresholds.

$EXTV_{CC}$ (Pin 9): Input to the Internal Switch Connected to $INTV_{CC}$. This switch closes and supplies V_{CC} power whenever $EXTV_{CC}$ is higher than 4.7V. See $EXTV_{CC}$ connection in Applications Information section. Do not exceed 10V on this pin. Connect to V_{OUT} if $V_{OUT} \geq 5V$.

PGND (Pin 10): Driver Power Ground. Connects to source of bottom N-channel MOSFET and the (–) terminal of C_{IN}.

BG (Pin 11): High Current Gate Drive for Bottom N-Channel MOSFET. Voltage swing at this pin is from ground to $INTV_{CC}$.

$INTV_{CC}$ (Pin 12): Output of the Internal 5V Regulator and $EXTV_{CC}$ Switch. The driver and control circuits are powered from this voltage. Must be closely decoupled to power ground with a minimum of 2.2µF tantalum or electrolytic capacitor.

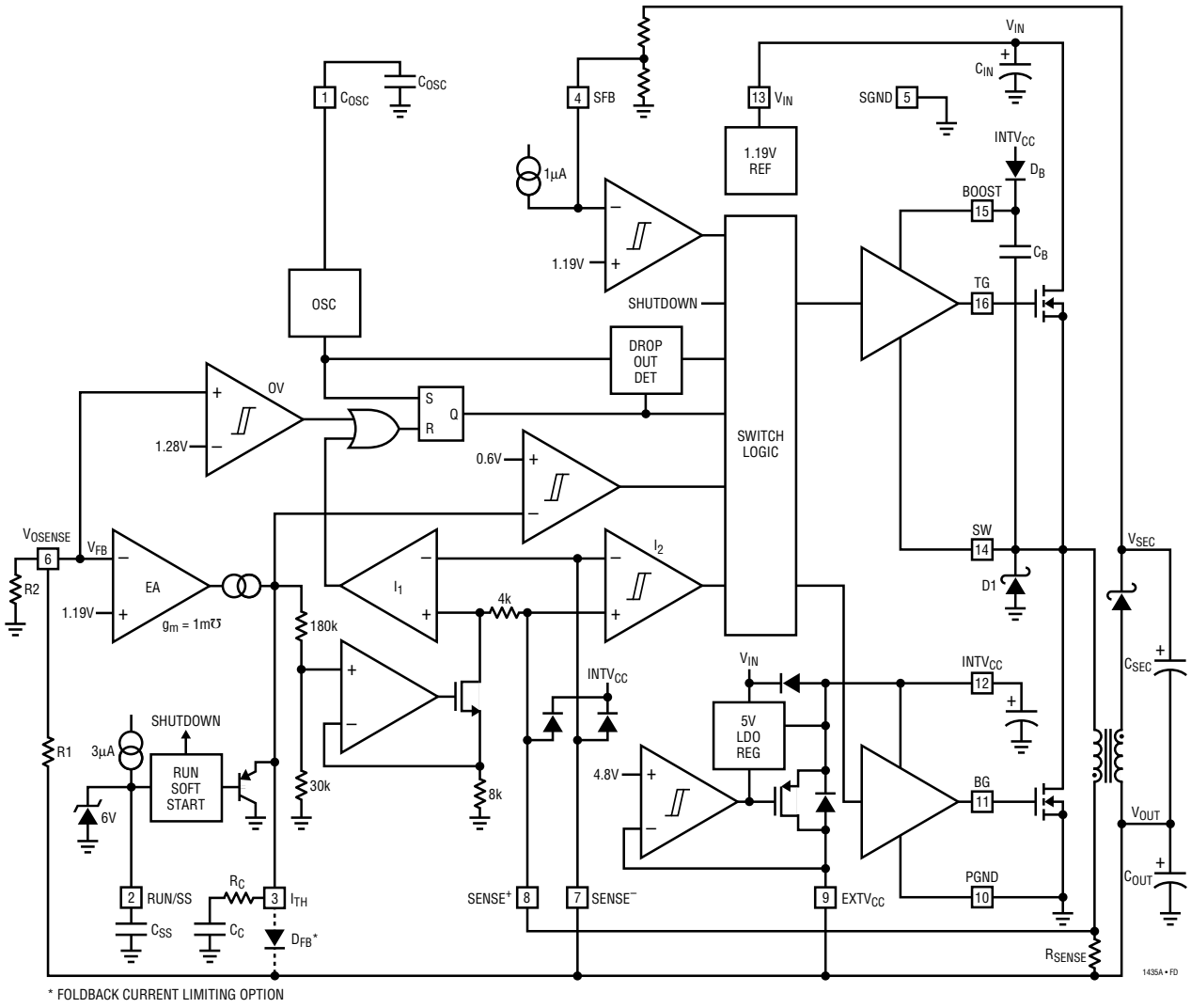
V_{IN} (Pin 13): Main Supply Pin. Must be closely decoupled to the IC's signal ground pin.

SW (Pin 14): Switch Node Connection to Inductor. Voltage swing at this pin is from a Schottky diode (external) voltage drop below ground to V_{IN}.

BOOST (Pin 15): Supply to Topside Floating Driver. The bootstrap capacitor is returned to this pin. Voltage swing at this pin is from $INTV_{CC}$ to V_{IN} + $INTV_{CC}$.

TG (Pin 16): High Current Gate Drive for Top N-Channel MOSFET. This is the output of a floating driver with a voltage swing equal to $INTV_{CC}$ superimposed on the switch node voltage SW.

FUNCTIONAL DIAGRAM



* FOLDBACK CURRENT LIMITING OPTION

OPERATION (Refer to Functional Diagram)

Main Control Loop

The LTC1435A uses a constant frequency, current mode step-down architecture. During normal operation, the top MOSFET is turned on each cycle when the oscillator sets the RS latch, and turned off when the main current comparator I_1 resets the RS latch. The peak inductor current at which I_1 resets the RS latch is controlled by the voltage on the I_{TH} pin , which is the output of error amplifier EA. The V_{OSENSE} pin, described in the Pin Functions section, allows EA to receive an output feedback voltage V_{FB} from an external resistive divider. When the load current increases, it causes a slight decrease in V_{FB} relative to the 1.19V reference, which in turn causes the I_{TH} voltage to increase until the average inductor current matches the new load current. While the top MOSFET is off, the bottom MOSFET is turned on until either the inductor current starts to reverse, as indicated by current comparator I_2, or the beginning of the next cycle.

The top MOSFET driver is biased from floating bootstrap capacitor C_B, which normally is recharged during each off cycle. However, when V_{IN} decreases to a voltage close to V_{OUT}, the loop may enter dropout and attempt to turn on the top MOSFET continuously. The dropout detector counts the number of oscillator cycles that the top MOSFET remains

OPERATION (Refer to Functional Diagram)

on and periodically forces a brief off period to allow C_B to recharge.

The main control loop is shut down by pulling the RUN/SS pin low. Releasing RUN/SS allows an internal 3μA current source to charge soft start capacitor C_{SS}. When C_{SS} reaches 1.3V, the main control loop is enabled with the I_{TH} voltage clamped at approximately 30% of its maximum value. As C_{SS} continues to charge, I_{TH} is gradually released allowing normal operation to resume.

Comparator OV guards against transient overshoots > 7.5% by turning off the top MOSFET and keeping it off until the fault is removed.

Low Current Operation

The LTC1435A is capable of Burst Mode operation in which the external MOSFETs operate intermittently based on load demand. The transition to low current operation begins when comparator I_2 detects current reversal and turns off the bottom MOSFET. If the voltage across R_{SENSE} does not exceed the hysteresis of I_2 (approximately 20mV) for one full cycle, then on following cycles the top and bottom drives are disabled. This continues until an inductor current peak exceeds 20mV/R_{SENSE} or the I_{TH} voltage exceeds 0.6V, either of which causes drive to be returned to the TG pin on the next cycle.

Two conditions can force continuous synchronous operation, even when the load current would otherwise dictate low current operation. One is when the common mode voltage of the SENSE$^+$ and SENSE$^-$ pins is below 1.4V and the other is when the SFB pin is below 1.19V. The latter condition is used to assist in secondary winding regulation as described in the Applications Information section.

$INTV_{CC}/EXTV_{CC}$ Power

Power for the top and bottom MOSFET drivers and most of the other LTC1435A circuitry is derived from the $INTV_{CC}$ pin. The bottom MOSFET driver supply pin is internally connected to $INTV_{CC}$ in the LTC1435A. When the $EXTV_{CC}$ pin is left open, an internal 5V low dropout regulator supplies $INTV_{CC}$ power. If $EXTV_{CC}$ is taken above 4.8V, the 5V regulator is turned off and an internal switch is turned on to connect $EXTV_{CC}$ to $INTV_{CC}$. This allows the $INTV_{CC}$ power to be derived from a high efficiency external source such as the output of the regulator itself or a secondary winding, as described in the Applications Information section.

APPLICATIONS INFORMATION

The basic LTC1435A application circuit is shown in Figure 1, High Efficiency Step-Down Converter. External component selection is driven by the load requirement and begins with the selection of R_{SENSE}. Once R_{SENSE} is known, C_{OSC} and L can be chosen. Next, the power MOSFETs and D1 are selected. Finally, C_{IN} and C_{OUT} are selected. The circuit shown in Figure 1 can be configured for operation up to an input voltage of 28V (limited by the external MOSFETs).

R_{SENSE} Selection for Output Current

R_{SENSE} is chosen based on the required output current. The LTC1435A current comparator has a maximum threshold of 150mV/R_{SENSE} and an input common mode range of SGND to $INTV_{CC}$. The current comparator threshold sets the peak of the inductor current, yielding a maximum average output current I_{MAX} equal to the peak value less half the peak-to-peak ripple current ΔI_L.

Allowing a margin for variations in the LTC1435A and external component values yields:

$$R_{SENSE} = \frac{100mV}{I_{MAX}}$$

The LTC1435A works well with R_{SENSE} values ≥ 0.005Ω.

C_{OSC} Selection for Operating Frequency

The LTC1435A uses a constant frequency architecture with the frequency determined by an external oscillator capacitor C_{OSC}. Each time the topside MOSFET turns on, the voltage C_{OSC} is reset to ground. During the on-time, C_{OSC} is charged by a fixed current. When the voltage on the capacitor reaches 1.19V, C_{OSC} is reset to ground. The process then repeats.

APPLICATIONS INFORMATION

The value of C_{OSC} is calculated from the desired operating frequency:

$$C_{OSC}\,(pF) = \left[\frac{1.37(10^4)}{\text{Frequency (kHz)}}\right] - 11$$

A graph for selecting C_{OSC} vs frequency is given in Figure 2. As the operating frequency is increased the gate charge losses will be higher, reducing efficiency (see Efficiency Considerations). The maximum recommended switching frequency is 400kHz.

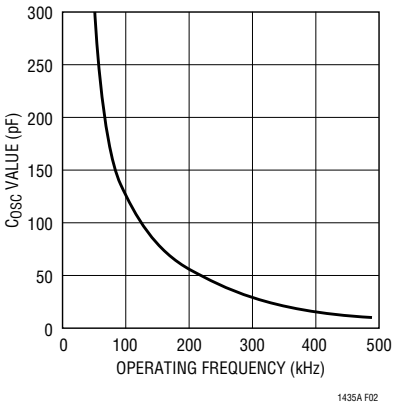


Figure 2. Timing Capacitor Value

Inductor Value Calculation

The operating frequency and inductor selection are interrelated in that higher operating frequencies allow the use of smaller inductor and capacitor values. So why would anyone ever choose to operate at lower frequencies with larger components? The answer is efficiency. A higher frequency generally results in lower efficiency because of MOSFET gate charge losses. In addition to this basic tradeoff, the effect of inductor value on ripple current and low current operation must also be considered.

The inductor value has a direct effect on ripple current. The inductor ripple current ΔI_L decreases with higher inductance or frequency and increases with higher V_{IN} or V_{OUT}:

$$\Delta I_L = \frac{1}{(f)(L)} V_{OUT}\left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Accepting larger values of ΔI_L allows the use of low inductances, but results in higher output voltage ripple and greater core losses. A reasonable starting point for setting ripple current is $\Delta I_L = 0.4(I_{MAX})$. Remember, the maximum ΔI_L occurs at the maximum input voltage.

The inductor value also has an effect on low current operation. The transition to low current operation begins when the inductor current reaches zero while the bottom MOSFET is on. Lower inductor values (higher ΔI_L) will cause this to occur at higher load currents, which can cause a dip in efficiency in the upper range of low current operation. In Burst Mode operation, lower inductance values will cause the burst frequency to decrease.

The Figure 3 graph gives a range of recommended inductor values vs operating frequency and V_{OUT}.

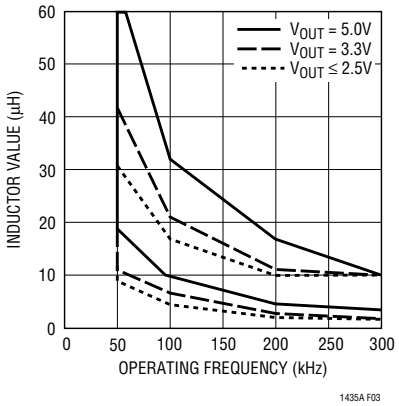


Figure 3. Recommended Inductor Values

For low duty cycle, high frequency applications where the required minimum on-time,

$$t_{ON(MIN)} = \frac{V_{OUT}}{\left(V_{IN(MAX)}\right)\left(f\right)},$$

is less than 350ns, there may be further restrictions on the inductance to ensure proper operation. See Minimum On-Time Considerations section for more details.

Inductor Core Selection

Once the value for L is known, the type of inductor must be selected. High efficiency converters generally cannot afford the core loss found in low cost powdered iron cores, forcing the use of more expensive ferrite, molypermalloy or Kool Mμ® cores. Actual core loss is independent of core size for

Kool Mμ is a registered trademark of Magnetics, Inc.

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a fixed inductor value, but it is very dependent on inductance selected. As inductance increases, core losses go down. Unfortunately, increased inductance requires more turns of wire and therefore copper losses will increase.

Ferrite designs have very low core loss and are preferred at high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates "hard," which means that inductance collapses abruptly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current and consequent output voltage ripple. **Do not allow the core to saturate!**

Molypermalloy (from Magnetics, Inc.) is a very good, low loss core material for toroids, but it is more expensive than ferrite. A reasonable compromise from the same manufacturer is Kool Mμ. Toroids are very space efficient, especially when you can use several layers of wire. Because they generally lack a bobbin, mounting is more difficult. However, designs for surface mount are available which do not increase the height significantly.

Power MOSFET and D1 Selection

Two external power MOSFETs must be selected for use with the LTC1435A: an N-channel MOSFET for the top (main) switch and an N-channel MOSFET for the bottom (synchronous) switch.

The peak-to-peak gate drive levels are set by the $INTV_{CC}$ voltage. This voltage is typically 5V during start-up (see $EXTV_{CC}$ Pin Connection). Consequently, logic level threshold MOSFETs must be used in most LTC1435A applications. The only exception is applications in which $EXTV_{CC}$ is powered from an external supply greater than 8V (must be less than 10V), in which standard threshold MOSFETs ($V_{GS(TH)} < 4V$) may be used. Pay close attention to the BV_{DSS} specification for the MOSFETs as well; many of the logic level MOSFETs are limited to 30V or less.

Selection criteria for the power MOSFETs include the "ON" resistance $R_{DS(ON)}$, reverse transfer capacitance C_{RSS}, input voltage and maximum output current. When the LTC1435A is operating in continuous mode the duty cycles for the top and bottom MOSFETs are given by:

$$\text{Main Switch Duty Cycle} = \frac{V_{OUT}}{V_{IN}}$$

$$\text{Synchronous Switch Duty Cycle} = \frac{(V_{IN} - V_{OUT})}{V_{IN}}$$

The MOSFET power dissipations at maximum output current are given by:

$$P_{MAIN} = \frac{V_{OUT}}{V_{IN}}(I_{MAX})^2(1+\delta)R_{DS(ON)} + k(V_{IN})^{1.85}(I_{MAX})(C_{RSS})(f)$$

$$P_{SYNC} = \frac{V_{IN} - V_{OUT}}{V_{IN}}(I_{MAX})^2(1+\delta)R_{DS(ON)}$$

where δ is the temperature dependency of $R_{DS(ON)}$ and k is a constant inversely related to the gate drive current.

Both MOSFETs have I^2R losses while the topside N-channel equation includes an additional term for transition losses, which are highest at high input voltages. For $V_{IN} < 20V$ the high current efficiency generally improves with larger MOSFETs, while for $V_{IN} > 20V$ the transition losses rapidly increase to the point that the use of a higher $R_{DS(ON)}$ device with lower C_{RSS} actual provides higher efficiency. The synchronous MOSFET losses are greatest at high input voltage or during a short circuit when the duty cycle in this switch is nearly 100%. Refer to the Foldback Current Limiting section for further applications information.

The term $(1 + \delta)$ is generally given for a MOSFET in the form of a normalized $R_{DS(ON)}$ vs Temperature curve, but $\delta = 0.005/°C$ can be used as an approximation for low voltage MOSFETs. C_{RSS} is usually specified in the MOSFET characteristics. The constant k = 2.5 can be used to estimate the contributions of the two terms in the main switch dissipation equation.

The Schottky diode D1 shown in Figure 1 conducts during the dead-time between the conduction of the two large power MOSFETs. This prevents the body diode of the bottom MOSFET from turning on and storing charge during the dead-time, which could cost as much as 1% in efficiency. A 1A Schottky is generally a good size for 3A regulators.

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C_{IN} and C_{OUT} Selection

In continuous mode, the source current of the top N-channel MOSFET is a square wave of duty cycle V_{OUT}/V_{IN}. To prevent large voltage transients, a low ESR input capacitor sized for the maximum RMS current must be used. The maximum RMS capacitor current is given by:

$$C_{IN} \text{ required } I_{RMS} \approx I_{MAX} \frac{\left[V_{OUT}\left(V_{IN} - V_{OUT}\right)\right]^{1/2}}{V_{IN}}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that capacitor manufacturer's ripple current ratings are often based on only 2000 hours of life. This makes it advisable to further derate the capacitor or to choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design. Always consult the manufacturer if there is any question.

The selection of C_{OUT} is driven by the required effective series resistance (ESR). Typically, once the ESR requirement is satisfied the capacitance is adequate for filtering. The output ripple (ΔV_{OUT}) is approximated by:

$$\Delta V_{OUT} \approx \Delta I_L \left(ESR + \frac{1}{4fC_{OUT}} \right)$$

where f = operating frequency, C_{OUT} = output capacitance and ΔI_L = ripple current in the inductor. The output ripple is highest at maximum input voltage since ΔI_L increases with input voltage. With $\Delta I_L = 0.4 I_{OUT(MAX)}$ the output ripple will be less than 100mV at max V_{IN} assuming:

$$C_{OUT} \text{ required } ESR < 2R_{SENSE}$$

Manufacturers such as Nichicon, United Chemicon and Sanyo should be considered for high performance through-hole capacitors. The OS-CON semiconductor dielectric capacitor available from Sanyo has the lowest ESR(size) product of any aluminum electrolytic at a somewhat higher price. Once the ESR requirement for C_{OUT} has been met, the RMS current rating generally far exceeds the $I_{RIPPLE(P-P)}$ requirement.

In surface mount applications multiple capacitors may have to be paralleled to meet the ESR or RMS current handling requirements of the application. Aluminum electrolytic and dry tantalum capacitors are both available in surface mount configurations. In the case of tantalum, it is critical that the capacitors are surge tested for use in switching power supplies. An excellent choice is the AVX TPS series of surface mount tantalum, available in case heights ranging from 2mm to 4mm. Other capacitor types include Sanyo OS-CON, Nichicon PL series and Sprague 593D and 595D series. Consult the manufacturer for other specific recommendations.

$INTV_{CC}$ Regulator

An internal P-channel low dropout regulator produces the 5V supply that powers the drivers and internal circuitry within the LTC1435A. The $INTV_{CC}$ pin can supply up to 15mA and must be bypassed to ground with a minimum of 2.2µF tantalum or low ESR electrolytic. Good bypassing is necessary to supply the high transient currents required by the MOSFET gate drivers.

High input voltage applications, in which large MOSFETs are being driven at high frequencies, may cause the maximum junction temperature rating for the LTC1435A to be exceeded. The IC supply current is dominated by the gate charge supply current when not using an output derived $EXTV_{CC}$ source. The gate charge is dependent on operating frequency as discussed in the Efficiency Considerations section. The junction temperature can be estimated by using the equations given in Note 1 of the Electrical Characteristics. For example, the LTC1435A is limited to less than 17mA from a 30V supply:

$$T_J = 70°C + (17mA)(30V)(100°C/W) = 126°C$$

To prevent maximum junction temperature from being exceeded, the input supply current must be checked when operating in continuous mode at maximum V_{IN}.

$EXTV_{CC}$ Connection

The LTC1435A contains an internal P-channel MOSFET switch connected between the $EXTV_{CC}$ and $INTV_{CC}$ pins. The switch closes and supplies the $INTV_{CC}$ power whenever the $EXTV_{CC}$ pin is above 4.8V, and remains closed until $EXTV_{CC}$ drops below 4.5V. This allows the MOSFET driver and

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control power to be derived from the output during normal operation (4.8V < V_{OUT} < 9V) and from the internal regulator when the output is out of regulation (start-up, short circuit). Do not apply greater than 10V to the $EXTV_{CC}$ pin and ensure that $EXTV_{CC} \leq V_{IN}$.

Significant efficiency gains can be realized by powering $INTV_{CC}$ from the output, since the V_{IN} current resulting from the driver and control currents will be scaled by a factor of Duty Cycle/Efficiency. For 5V regulators this supply means connecting the $EXTV_{CC}$ pin directly to V_{OUT}. However, for 3.3V and other lower voltage regulators, additional circuitry is required to derive $INTV_{CC}$ power from the output.

The following list summarizes the four possible connections for $EXTV_{CC}$:

1. $EXTV_{CC}$ left open (or grounded). This will cause $INTV_{CC}$ to be powered from the internal 5V regulator resulting in an efficiency penalty of up to 10% at high input voltages.
2. $EXTV_{CC}$ connected directly to V_{OUT}. This is the normal connection for a 5V regulator and provides the highest efficiency.
3. $EXTV_{CC}$ connected to an output-derived boost network. For 3.3V and other low voltage regulators, efficiency gains can still be realized by connecting $EXTV_{CC}$ to an output-derived voltage which has been boosted to greater than 4.8V. This can be done with either the inductive boost winding as shown in Figure 4a or the capacitive charge pump shown in Figure 4b. The charge pump has the advantage of simple magnetics.
4. $EXTV_{CC}$ connected to an external supply. If an external supply is available in the 5V to 10V range ($EXTV_{CC} \leq V_{IN}$), it may be used to power $EXTV_{CC}$ providing it is compatible with the MOSFET gate drive requirements. When driving standard threshold MOSFETs, the external supply must always be present during operation to prevent MOSFET failure due to insufficient gate drive.

Topside MOSFET Driver Supply (C_B, D_B)

An external bootstrap capacitor C_B connected to the Boost pin supplies the gate drive voltage for the topside MOSFET. Capacitor C_B in the Functional Diagram is charged through diode D_B from $INTV_{CC}$ when the SW pin is low. When the

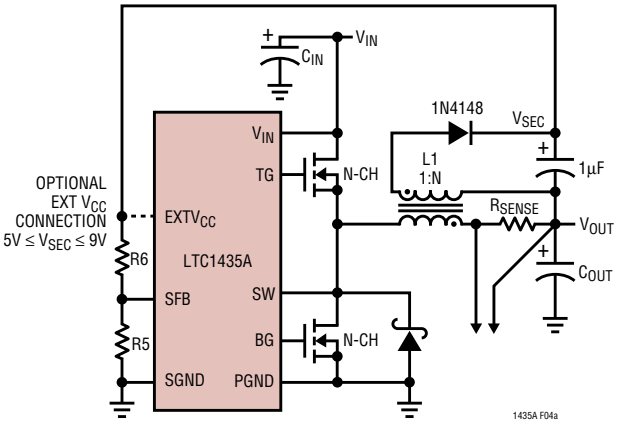


Figure 4a. Secondary Output Loop and $EXTV_{CC}$ Connection

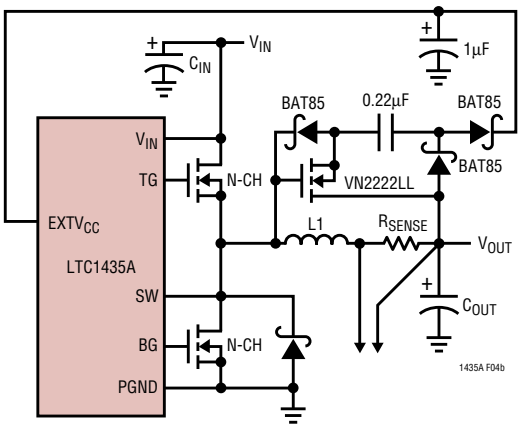


Figure 4b. Capacitive Charge Pump for $EXTV_{CC}$

topside MOSFET is to be turned on, the driver places the C_B voltage across the gate source of the MOSFET. This enhances the MOSFET and turns on the topside switch. The switch node voltage SW rises to V_{IN} and the Boost pin rises to $V_{IN} + INTV_{CC}$. The value of the boost capacitor C_B needs to be 100 times greater than the total input capacitance of the topside MOSFET. In most applications 0.1µF is adequate. The reverse breakdown on D_B must be greater than $V_{IN(MAX)}$.

Output Voltage Programming

The output voltage is set by a resistive divider according to the following formula:

$$V_{OUT} = 1.19V\left(1+\frac{R2}{R1}\right), V_{OUT} \geq 1.19\,V$$

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The external resistive divider is connected to the output as shown in Figure 5 allowing remote voltage sensing.

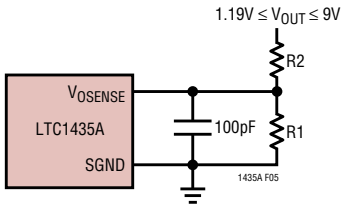


Figure 5. Setting the LTC1435A Output Voltage

Run/Soft Start Function

The RUN/SS pin is a dual purpose pin that provides the soft start function and a means to shut down the LTC1435A. Soft start reduces surge currents from V_{IN} by gradually increasing the internal current limit. *Power supply sequencing* can also be accomplished using this pin.

An internal 3µA current source charges up an external capacitor C_{SS}. When the voltage on RUN/SS reaches 1.3V the LTC1435A begins operating. As the voltage on RUN/SS continues to ramp from 1.3V to 2.4V, the internal current limit is also ramped at a proportional linear rate. The current limit begins at approximately $50mV/R_{SENSE}$ (at $V_{RUN/SS} = 1.3V$) and ends at $150mV/R_{SENSE}$ ($V_{RUN/SS} \geq 2.7V$). The output current thus ramps up slowly, charging the output capacitor. If RUN/SS has been pulled all the way to ground there is a delay before starting of approximately 500ms/µF, followed by an additional 500ms/µF to reach full current.

$$t_{DELAY} = 5(10^5)C_{SS} \text{ Seconds}$$

Pulling the RUN/SS pin below 1.3V puts the LTC1435A into a low quiescent current shutdown ($I_Q < 25\mu A$). This pin can be driven directly from logic as shown in Figure 6. Diode D1 in Figure 6 reduces the start delay but allows C_{SS} to ramp up slowly for the soft start function; this diode and C_{SS} can be deleted if soft start is not needed. The RUN/SS pin has an internal 6V Zener clamp (See Functional Diagram).

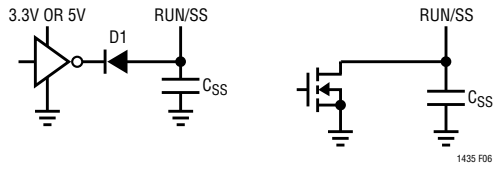


Figure 6. RUN/SS Pin Interfacing

Foldback Current Limiting

As described in Power MOSFET and D1 Selection, the worst-case dissipation for either MOSFET occurs with a short-circuited output, when the synchronous MOSFET conducts the current limit value almost continuously. In most applications this will not cause excessive heating, even for extended fault intervals. However, when heat sinking is at a premium or higher $R_{DS(ON)}$ MOSFETs are being used, foldback current limiting should be added to reduce the current in proportion to the severity of the fault.

Foldback current limiting is implemented by adding diode D_{FB} between the output and the I_{TH} pin as shown in the Functional Diagram. In a hard short ($V_{OUT} = 0V$) the current will be reduced to approximately 25% of the maximum output current. This technique may be used for all applications with regulated output voltages of 1.8V or greater.

SFB Pin Operation

When the SFB pin drops below its ground referenced 1.19V threshold, continuous mode operation is forced. In continuous mode, the large N-channel main and synchronous switches are used regardless of the load on the main output.

In addition to providing a logic input to force continuous synchronous operation, the SFB pin provides a means to regulate a flyback winding output. Continuous synchronous operation allows power to be drawn from the auxiliary windings without regard to the primary output load. The SFB pin provides a way to force continuous synchronous operation as needed by the flyback winding.

The secondary output voltage is set by the turns ratio of the transformer in conjunction with a pair of external resistors returned to the SFB pin as shown in Figure 4a. The secondary regulated voltage, V_{SEC}, in Figure 4a is given by:

$$V_{SEC} \approx (N+1)V_{OUT} > 1.19\left(1+\frac{R6}{R5}\right)$$

where N is the turns ratio of the transformer and V_{OUT} is the main output voltage sensed by V_{OSENSE}.

Minimum On-Time Considerations

Minimum on-time, $t_{ON(MIN)}$, is the smallest amount of time that the LTC1435A is capable of turning the top MOSFET

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on and off again. It is determined by internal timing delays and the gate charge required to turn on the top MOSFET. Low duty cycle applications may approach this minimum on-time limit. If the duty cycle falls below what can be accommodated by the minimum on-time, the LTC1435A will begin to skip cycles. The output voltage will continue to be regulated, but the ripple current and ripple voltage will increase. Therefore this limit should be avoided.

The minimum on-time for the LTC1435A in a properly configured application is less than 300ns but increases at low ripple current amplitudes (see Figure 7). If an application is expected to operate close to the minimum on-time limit, an inductor value must be chosen that is low enough to provide sufficient ripple amplitude to meet the minimum on-time requirement. To determine the proper value, use the following procedure:

1. Calculate on-time at maximum supply, $t_{ON(MIN)} = (1/f)(V_{OUT}/V_{IN(MAX)})$.
2. Use Figure 7 to obtain the peak-to-peak inductor ripple current as a percentage of I_{MAX} necessary to achieve the calculated $t_{ON(MIN)}$.
3. Ripple amplitude $\Delta I_{L(MIN)}$ = (% from Figure 7)(I_{MAX}) where $I_{MAX} = 0.1/R_{SENSE}$.
4. $$L_{MAX} = t_{ON(MIN)}\left(\frac{V_{IN(MAX)} - V_{OUT}}{\Delta I_{L(MIN)}}\right)$$

Choose an inductor less than or equal to the calculated L_{MAX} to ensure proper operation.

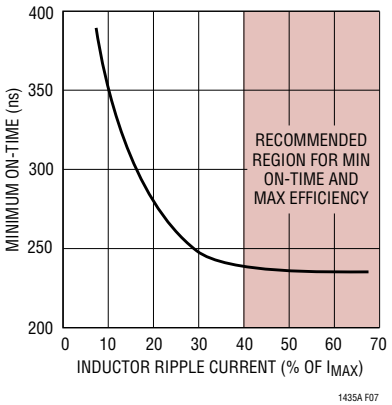


Figure 7. Minimum On-Time vs Inductor Ripple Current

Because of the sensitivity of the LTC1435A current comparator when operating close to the minimum on-time limit, it is important to prevent stray magnetic flux generated by the inductor from inducing noise on the current sense resistor, which may occur when axial type cores are used. By orienting the sense resistor on the radial axis of the inductor (see Figure 8), this noise will be minimized.

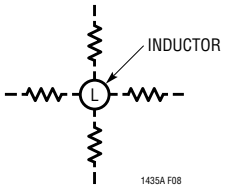


Figure 8. Allowable Inductor/R_{SENSE} Layout Orientations

Efficiency Considerations

The efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Efficiency can be expressed as:

Efficiency = 100% – (L1 + L2 + L3 + ...)

where L1, L2, etc. are the individual losses as a percentage of input power.

Although all dissipative elements in the circuit produce losses, four main sources usually account for most of the losses in LTC1435A circuits. LTC1435A V_{IN} current, $INTV_{CC}$ current, I^2R losses, and topside MOSFET transition losses.

1. The V_{IN} current is the DC supply current given in the electrical characteristics which excludes MOSFET driver and control currents. V_{IN} current results in a small (< 1%) loss which increases with V_{IN}.
2. $INTV_{CC}$ current is the sum of the MOSFET driver and control currents. The MOSFET driver current results from switching the gate capacitance of the power MOSFETs. Each time a MOSFET gate is switched from low to high to low again, a packet of charge dQ moves from $INTV_{CC}$ to ground. The resulting dQ/dt is a current out of $INTV_{CC}$ that is typically much larger than the control circuit current. In continuous mode, $I_{GATECHG} = f(Q_T + Q_B)$, where Q_T and Q_B are the gate charges of the topside and bottom side MOSFETs.

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By powering $EXTV_{CC}$ from an output-derived source, the additional V_{IN} current resulting from the driver and control currents will be scaled by a factor of Duty Cycle/Efficiency. For example, in a 20V to 5V application, 10mA of $INTV_{CC}$ current results in approximately 3mA of V_{IN} current. This reduces the midcurrent loss from 10% or more (if the driver was powered directly from V_{IN}) to only a few percent.

3. I^2R losses are predicted from the DC resistances of the MOSFET, inductor and current shunt. In continuous mode the average output current flows through L and R_{SENSE}, but is "chopped" between the topside main MOSFET and the synchronous MOSFET. If the two MOSFETs have approximately the same $R_{DS(ON)}$, then the resistance of one MOSFET can simply be summed with the resistances of L and R_{SENSE} to obtain I^2R losses. For example, if each $R_{DS(ON)} = 0.05\Omega$, $R_L = 0.15\Omega$, and $R_{SENSE} = 0.05\Omega$, then the total resistance is 0.25Ω. This results in losses ranging from 3% to 10% as the output current increases from 0.5A to 2A. I^2R losses cause the efficiency to drop at high output currents.

4. Transition losses apply only to the topside MOSFET(s), and only when operating at high input voltages (typically 20V or greater). Transition losses can be estimated from:

$$\text{Transition Loss} = 2.5\ (V_{IN})^{1.85}(I_{MAX})(C_{RSS})(f)$$

Other losses, including C_{IN} and C_{OUT} ESR dissipative losses, Schottky conduction losses during dead-time, and inductor core losses, generally account for less than 2% total additional loss.

Checking Transient Response

The regulator loop response can be checked by looking at the load transient response. Switching regulators take several cycles to respond to a step in DC (resistive) load current. When a load step occurs, V_{OUT} immediately shifts by an amount equal to $(\Delta I_{LOAD})(ESR)$, where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT} which generates a feedback error signal. The regulator loop then acts to return V_{OUT} to its steady-state value. During this recovery time V_{OUT} can be monitored for overshoot or ringing, which would indicate a stability problem. The I_{TH} external components shown in the Figure 1 circuit will provide adequate compensation for most applications.

A second, more severe transient is caused by switching in loads with large (>1µF) supply bypass capacitors. The discharged bypass capacitors are effectively put in parallel with C_{OUT}, causing a rapid drop in V_{OUT}. No regulator can deliver enough current to prevent this problem if the load switch resistance is low and it is driven quickly. The only solution is to limit the rise time of the switch drive so that the load rise time is limited to approximately $(25)(C_{LOAD})$. Thus a 10µF capacitor would require a 250µs rise time, limiting the charging current to about 200mA.

Automotive Considerations: Plugging into the Cigarette Lighter

As battery-powered devices go mobile, there is a natural interest in plugging into the cigarette lighter in order to conserve or even recharge battery packs during operation. But before you connect, be advised: you are plugging into the supply from hell. The main battery line in an automobile is the source of a number of nasty potential transients, including load dump, reverse battery and double battery.

Load dump is the result of a loose battery cable. When the cable breaks connection, the field collapse in the alternator can cause a positive spike as high as 60V which takes several hundred milliseconds to decay. Reverse battery is just what it says, while double battery is a consequence of tow truck operators finding that a 24V jump start cranks cold engines faster than 12V.

The network shown in Figure 9 is the most straightforward approach to protect a DC/DC converter from the ravages of an automotive battery line. The series diode prevents current from flowing during reverse battery, while the transient suppressor clamps the input voltage during load dump. Note that the transient suppressor should not

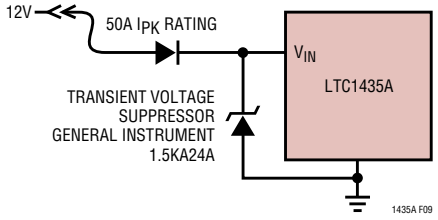


Figure 9. Automotive Application Protection

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conduct during double battery operation, but must still clamp the input voltage below breakdown of the converter. Although the LTC1435A has a maximum input voltage of 36V, most applications will be limited to 30V by the MOSFET BV_{DSS}.

Design Example

As a design example, assume V_{IN} = 12V(nominal), V_{IN} = 22V(max), V_{OUT} = 1.6V, I_{MAX} = 3A and f = 250kHz, R_{SENSE} and C_{OSC} can immediately be calculated:

$R_{SENSE} = 100mV/3A = 0.033\Omega$

$C_{OSC} = 1.37(10^4)/250 - 11 = 43pF$

Referring to Figure 3, a 4.7µH inductor falls within the recommended range. To check the actual value of the ripple current the following equation is used:

$$\Delta I_L = \frac{V_{OUT}}{(f)(L)}\left(1-\frac{V_{OUT}}{V_{IN}}\right)$$

The highest value of the ripple current occurs at the maximum input voltage:

$$\Delta I_L = \frac{1.6V}{250kHz(4.7\mu H)}\left(1-\frac{1.6V}{22V}\right) = 1.3A$$

The lowest duty cycle also occurs at maximum input voltage. The on-time during this condition should be checked to make sure it doesn't violate the LTC1435A's minimum on-time and cause cycle skipping to occur. The required on-time at $V_{IN(MAX)}$ is:

$$t_{ON(MIN)} = \frac{V_{OUT}}{(V_{IN(MAX)})(f)} = \frac{1.6V}{(22V)(250kHz)} = 291ns$$

The ΔI_L was previously calculated to be 1.3A, which is 43% of I_{MAX}. From Figure 7, the LTC1435A minimum on-time at 43% ripple is about 235ns. Therefore, the minimum on-time is sufficient and no cycle skipping will occur.

The power dissipation on the topside MOSFET can be easily estimated. Choosing a Siliconix Si4412DY results in: $R_{DS(ON)} = 0.042\Omega$, C_{RSS} = 100pF. At maximum input voltage with T(estimated) = 50°C:

$$P_{MAIN} = \frac{1.6V}{22V}(3)^2\left[1+(0.005)(50°C-25°C)\right](0.042\Omega) + 2.5(22V)^{1.85}(3A)(100pF)(250kHz) = 88mW$$

The most stringent requirement for the synchronous N-channel MOSFET occurs when V_{OUT} = 0 (i.e. short circuit). In this case the worst-case dissipation rises to:

$$P_{SYNC} = (I_{SC(AVG)})^2(1+\delta)R_{DS(ON)}$$

With the 0.033Ω sense resistor $I_{SC(AVG)}$ = 4A will result, increasing the Si4412DY dissipation to 950mW at a die temperature of 105°C.

C_{IN} is chosen for an RMS current rating of at least 1.5A at temperature. C_{OUT} is chosen with an ESR of 0.03Ω for low output ripple. The output ripple in continuous mode will be highest at the maximum input voltage. The output voltage ripple due to ESR is approximately:

$V_{ORIPPLE} = R_{ESR}(\Delta I_L) = 0.03\Omega(1.3A) = 39mV_{P-P}$

PC Board Layout Checklist

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the LTC1435A. These items are also illustrated graphically in the layout diagram of Figure 10. Check the following in your layout:

1. Are the signal and power grounds segregated? The LTC1435A signal ground pin must return to the (–) plate of C_{OUT}. The power ground connects to the source of the bottom N-channel MOSFET, anode of the Schottky diode, and (–) plate of C_{IN}, which should have as short lead lengths as possible.
2. Does the V_{OSENSE} pin connect directly to the feedback resistors? The resistive divider R1, R2 must be connected between the (+) plate of C_{OUT} and signal ground. The 100pF capacitor should be as close as possible to the LTC1435A.
3. Are the $SENSE^-$ and $SENSE^+$ leads routed together with minimum PC trace spacing? The filter capacitor between $SENSE^+$ and $SENSE^-$ should be as close as possible to the LTC1435A.

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4. Does the (+) plate of C_{IN} connect to the drain of the topside MOSFET(s) as closely as possible? This capacitor provides the AC current to the MOSFET(s).
5. Is the $INTV_{CC}$ decoupling capacitor connected closely between $INTV_{CC}$ and the power ground pin? This capacitor carries the MOSFET driver peak currents.
6. Keep the switching node SW away from sensitive small-signal nodes. Ideally the switch node should be placed at the furthest point from the LTC1435A.
7. SGND should be exclusively used for grounding external components on C_{OSC}, I_{TH}, V_{OSENSE} and SFB pins.
8. If operating close to the minimum on-time limit, is the sense resistor oriented on the radial axis of the inductor? See Figure 8.

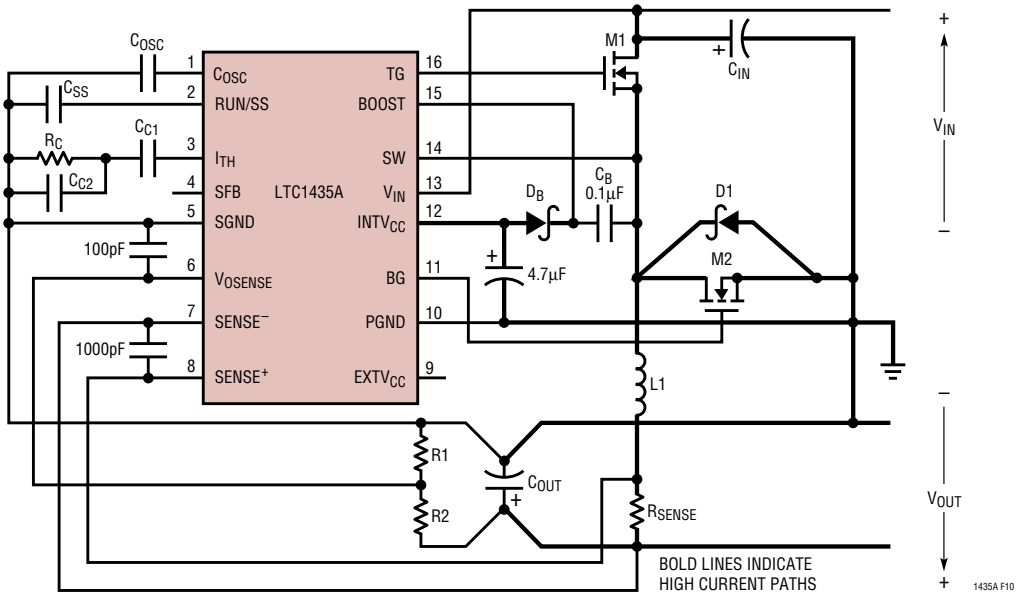
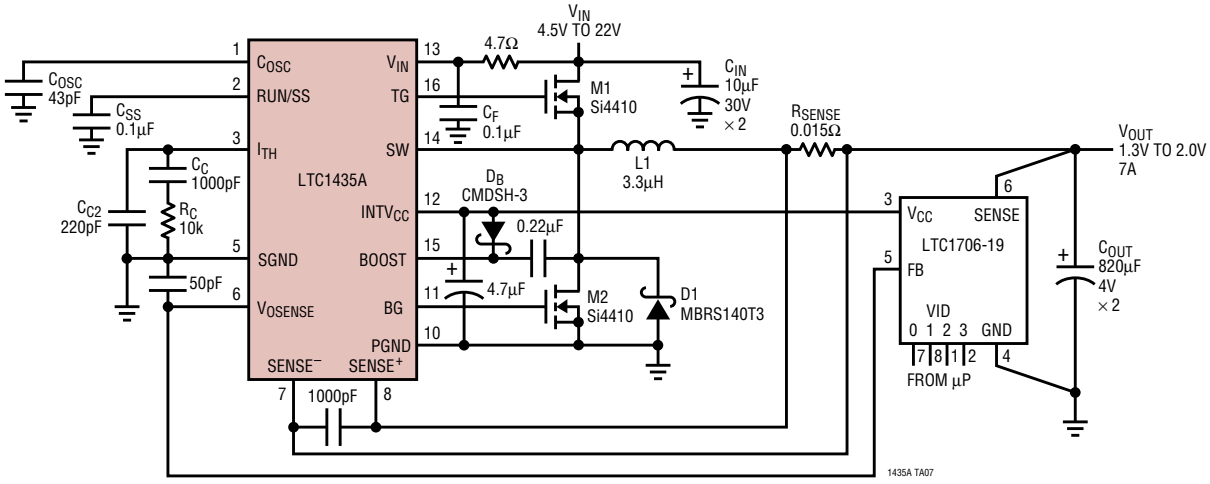


Figure 10. LTC1435A Layout Diagram

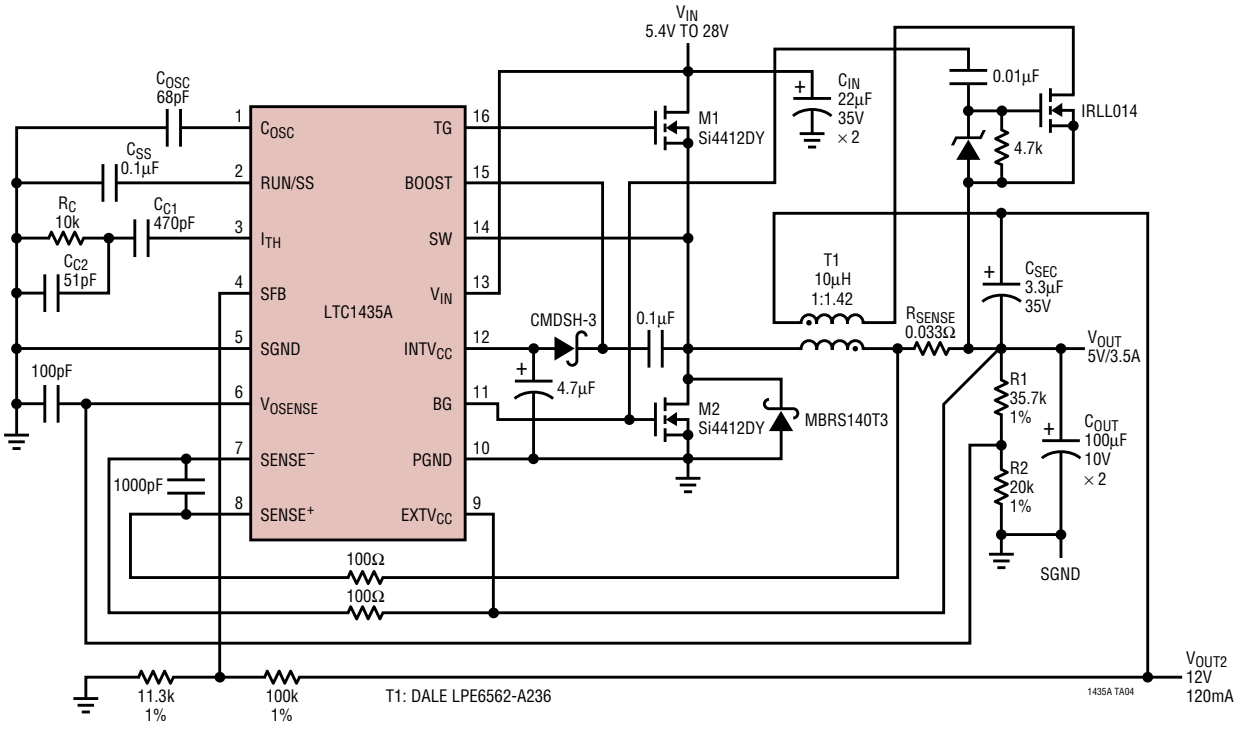
TYPICAL APPLICATIONS

Intel Mobile CPU VID Power Converter

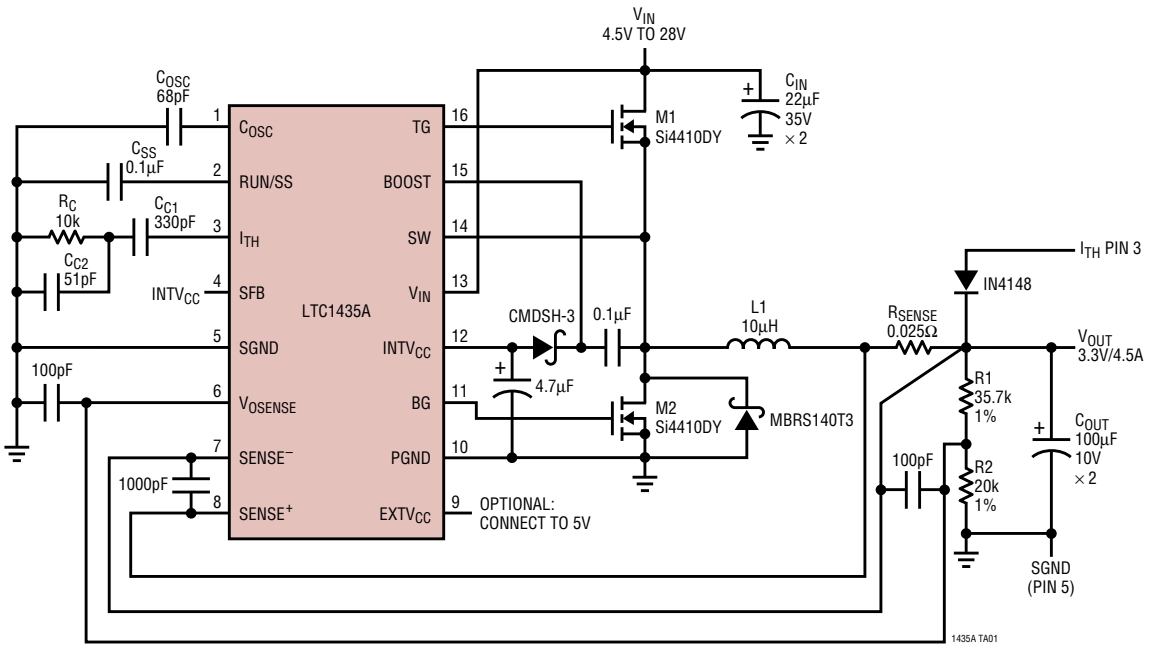


TYPICAL APPLICATIONS

Dual Output 5V and Synchronous 12V Application

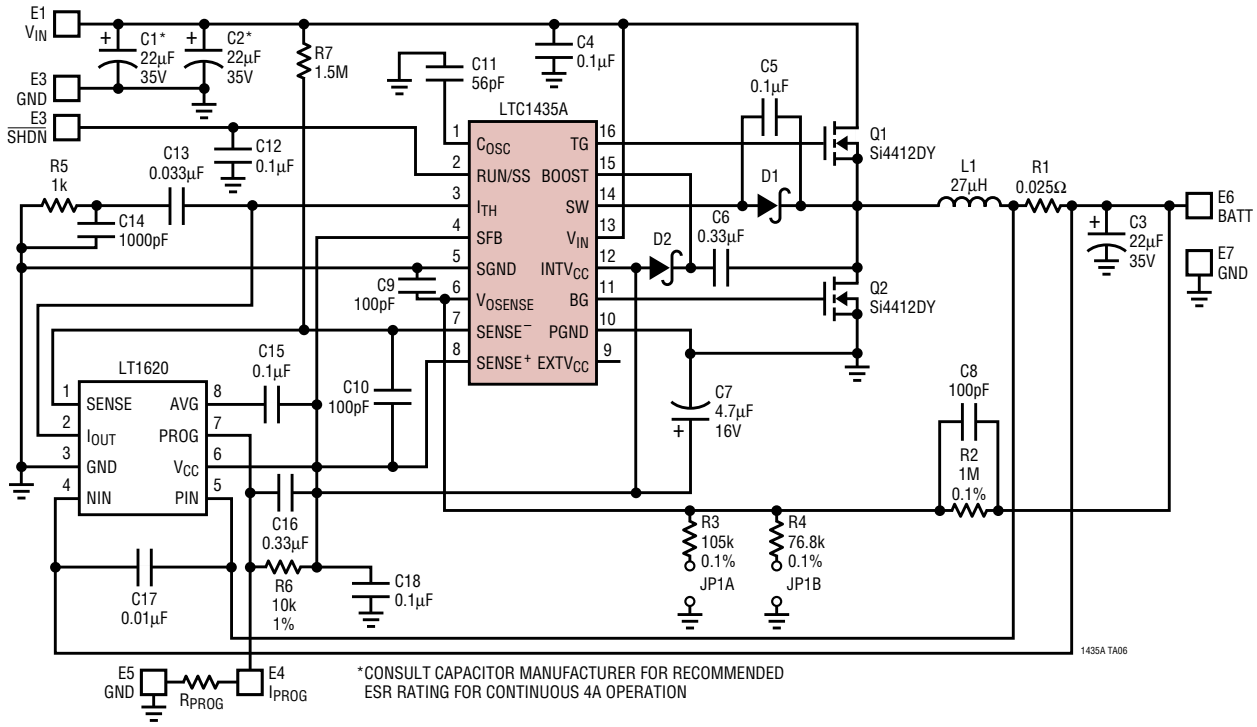


3.3V/4.5A Converter with Foldback Current Limiting



TYPICAL APPLICATIONS

Constant-Current/Constant-Voltage High Efficiency Battery Charger

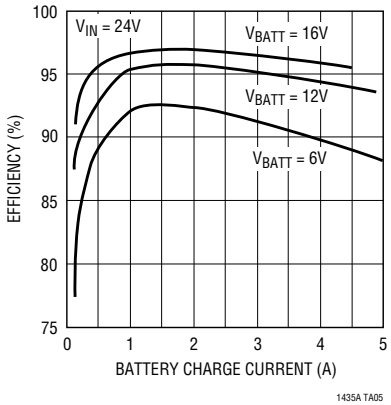


*CONSULT CAPACITOR MANUFACTURER FOR RECOMMENDED ESR RATING FOR CONTINUOUS 4A OPERATION

Current Programming Equation

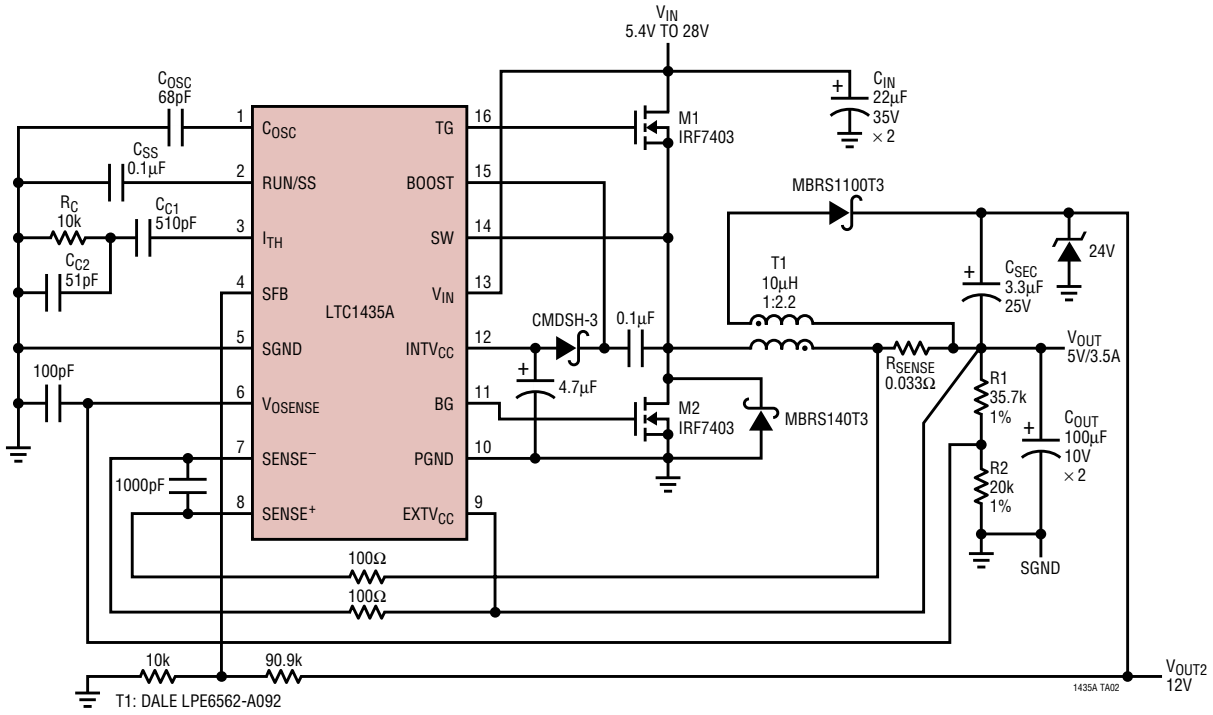
$$I_{BATT} = \frac{(I_{PROG})(R6) - 0.04}{10(R1)}$$

Efficiency



TYPICAL APPLICATIONS

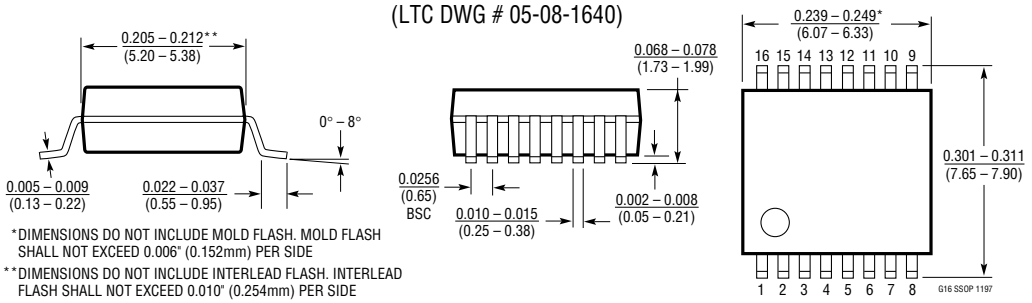
Dual Output 5V and 12V Application



PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

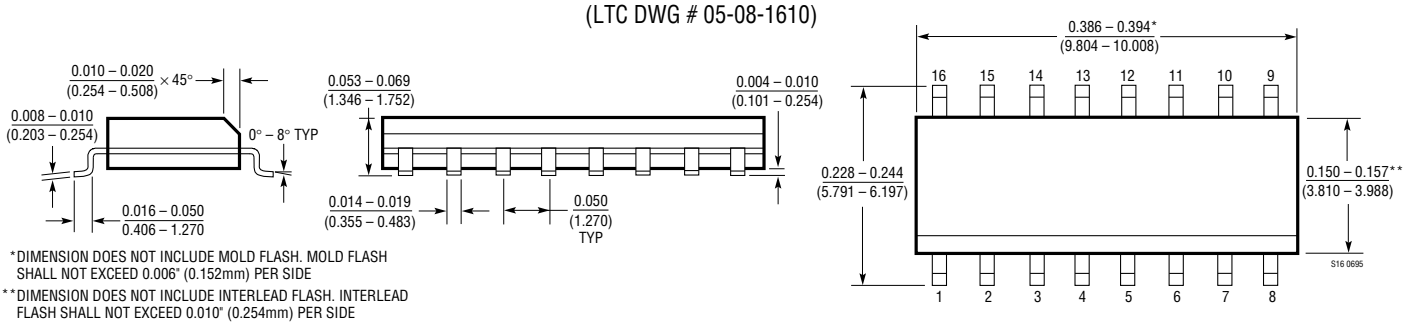
G Package
16-Lead Plastic SSOP (0.209)
(LTC DWG # 05-08-1640)



*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSIONS DO NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

S Package
16-Lead Plastic Small Outline (Narrow 0.150)
(LTC DWG # 05-08-1610)



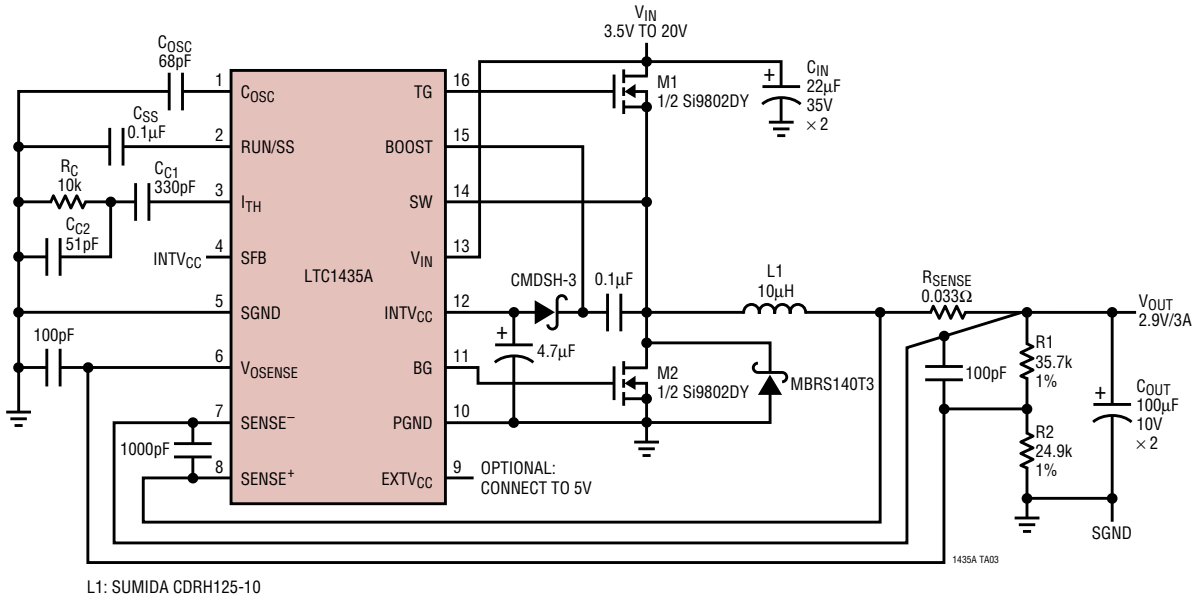
*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

TYPICAL APPLICATION

Low Dropout 2.9V/3A Converter



L1: SUMIDA CDRH125-10

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1142HV/LTC1142	Dual High Efficiency Synchronous Step-Down Switching Regulators	Dual Synchronous, $V_{IN} \leq 20V$
LTC1148HV/LTC1148	High Efficiency Sychronous Step-Down Switching Regulator Controllers	Synchronous, $V_{IN} \leq 20V$
LTC1159	High Efficiency Synchronous Step-Down Switching Regulator	Synchronous, $V_{IN} \leq 40V$, For Logic Threshold FETs
LT®1375/LT1376	1.5A, 500kHz Step-Down Switching Regulators	High Frequency, Small Inductor, High Efficiency Switchers, 1.5A Switch
LTC1430	High Power Step-Down Switching Regulator Controller	High Efficiency 5V to 3.3V Conversion at Up to 15A
LTC1436A/LTC1436A-PLL/ LTC1437A	High Efficiency Low Noise Synchronous Step-Down Switching Regulators	Full-Featured Single Controller
LTC1438/LTC1439	Dual High Efficiency, Low Noise, Synchronous Step-Down Switching Regulators	Full-Featured Dual Controllers
LT1510	Constant-Voltage/ Constant-Current Battery Charger	1.3A, Li-Ion, NiCd, NiMH, Pb-Acid Charger
LTC1538-AUX	Dual High Efficiency, Low Noise, Synchronous Step-Down Switching Regulator	5V Standby in Shutdown
LTC1539	Dual High Efficiency, Low Noise, Synchronous Step-Down Switching Regulator	5V Standby in Shutdown
LTC1706-19	VID Voltage Programmer	Creates a Programmable 1.3V to 2V Supply for Intel Mobile Pentium® II Processor When Used with the LTC1435A

Pentium is a registered trademark of Intel Corporation.

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