Clock-Synchronized Switched Capacitor Regulated Voltage Inverter

OBSOLETE:
FOR INFORMATION PURPOSES ONLY
Contact Linear Technology for Potential Replacement

FEATURES

- **Regulated Negative Voltage from a Single Positive Supply**
- **External Clock for Synchronization in Noise Sensitive Systems**
- **REG Output Indicates Output is in Regulation**
- **Low Output Ripple: 5mV Typ**
- Can Provide Regulated –5V from a 3V Supply
- Supply Current: 600µA Typ
- Shutdown Mode Drops Supply Current to 0.2µA
- Up to 12mA Output Current
- Adjustable or Fixed Output Voltages
- Requires Only Three or Four External Caps
- Output Regulation: 5%
- Available in SO-8 Packages

APPLICATIONS

- GaAs FET Bias Generators
- Negative Supply Generators
- Battery Powered Systems
- Single Supply Applications

DESCRIPTION

The LTC®1429 is a switched-capacitor voltage inverter designed to provide a regulated negative voltage from a single positive supply and permits clock synchronization in noise sensitive systems. The LTC1429CS operates from a single 3V to 8V supply and provides an adjustable output voltage from –1.25V to –8V. An on-chip resistor string allows the LTC1429CS to be configured for output voltages of –3.5V, –4V, –4.5V or –5V. The LTC1429CS8 is optimized for applications which require a fixed –4V output from a 5V supply and requires only a single external 0.1µF flying capacitor. The LTC1429CS requires one or two external 0.1µF capacitors, depending on input voltage. Both versions require additional external input and output bypass capacitors. An optional compensation capacitor at ADJ/COMP can be used to reduce the output voltage ripple.

Each version of the LTC1429 guarantees output regulation of 5%. The LTC1429 includes an open-drain REG output which pulls low when the output is within 5% of the set value. Output ripple is typically as low as 5mV. The LTC1429 requires an external clock applied to the SYNC/SD for normal operation and consumes a typical quiescent current of 600µA. Holding the SYNC/SD either high or low brings the device into shutdown and the supply current drops to 0.2µA. For applications which don't have a clock signal available, the LTC1261 provides the same functionality with an internal oscillator. For applications which require output ripple below 1mV, see the LTC1550/LTC1551. The LTC1429CS is available in a 14-pin SO package and the LTC1429CS8 is available in an 8-pin SO package.

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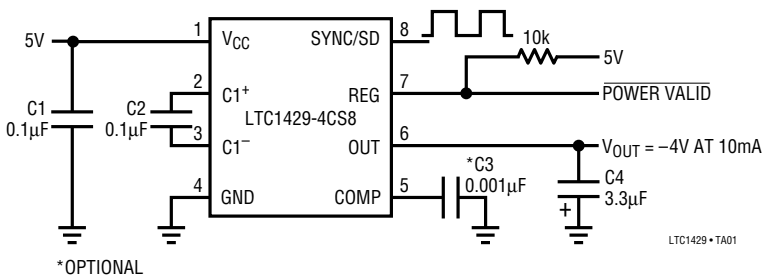
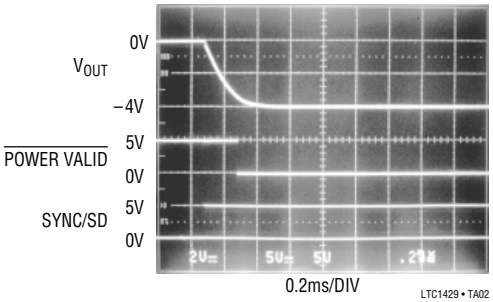
TYPICAL APPLICATION

–4V Generator with $\overline{\text{Power Valid}}$



Waveforms for –4V Generator with $\overline{\text{Power Valid}}$

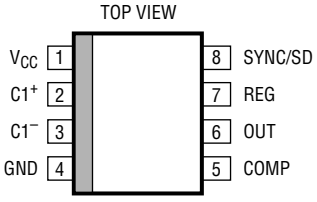


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage (Note 2) 9V
Output Voltage ..... 0.3V to –9V
Total Voltage, V_{CC} to V_{OUT} (Note 2) 12V
Input Voltage (SYNC/SD Pin) ..... –0.3V to (V_{CC} + 0.3V)
Input Voltage (REG Pin) ..... –0.3V to 12V
Input Voltage (ADJ, RO-1, R_{ADJ}) ..... (V_{OUT} – 0.3V) to (V_{CC} + 0.3V)
Output Short Circuit Duration ..... Indefinite
Operating Temperature Range ..... 0°C to 70°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

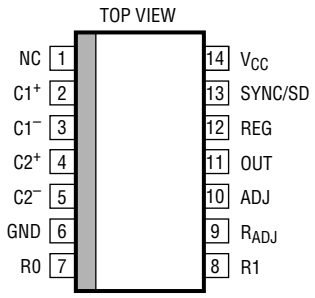
PACKAGE/ORDER INFORMATION



S8 PACKAGE
8-LEAD PLASTIC SO

T_{JMAX} = 150°C, θ_{JA} = 150°C/W

ORDER PART NUMBER
LTC1429CS8-4*
S8 PART MARKING
14294



S PACKAGE
14-LEAD PLASTIC SO

T_{JMAX} = 150°C, θ_{JA} = 110°C/W

ORDER PART NUMBER
LTC1429CS

Consult factory for Industrial and Military grade parts. *Contact factory for other output voltages or 8-pin adjustable parts.

ELECTRICAL CHARACTERISTICS

V_{CC} = 3V to 6.5V. C1 = C2 = 0.1μF (Note 4), C_{OUT} = 3.3μF, F_{SYNC} = 700kHz with 50% duty cycle square wave, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LTC1429CS8/LTC1429CS MIN	TYP	MAX	UNITS
V_{REF}	Reference Voltage		●	1.20	1.24	1.28	V
I_S	Supply Current	V_{CC} = 3.3V	●		600	1500	μA
		V_{CC} = 5V	●		600	1500	μA
		$V_{SYNC/SD}$ = V_{CC} or GND	●		0.2	5	μA
F_{SYNC}	Synchronous Clock Frequency (Note 8)	$V_{CC} \leq$ 5V		60	700	2000	kHz
		V_{CC} = 6.5V		100	700	2000	kHz
P_{EFF}	Power Efficiency				65		%
V_{OL}	REG Output Low Voltage	I_{REG} = 1mA	●		0.1	0.8	V
I_{REG}	REG Sink Current	V_{REG} = 0.8V, V_{CC} = 3.3V	●	5	8		mA
		V_{REG} = 0.8V, V_{CC} = 5V	●	8	15		mA
I_{ADJ}	Adjust Pin Current	V_{ADJ} = 1.24V (Note 5)	●		0.01	1	μA
V_{IH}	SYNC/SD Input High Voltage	V_{CC} = 5V	●	2.0			V
V_{IL}	SYNC/SD Input Low Voltage	V_{CC} = 5V	●			0.8	V
I_{IN}	SYNC/SD Input Current	$V_{SYNC/SD}$ = V_{CC} or GND	●			±1	μA
T_{ON}	Turn On Time	I_{OUT} = 10mA			200		μs

ELECTRICAL CHARACTERISTICS

Tripler Mode, V_{CC} = 3.3V, C1 = C2 = 0.1μF (Note 4), C_{OUT} = 3.3μF, F_{SYNC} = 700kHz with 50% duty cycle square wave, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LTC1429CS MIN	TYP	MAX	UNITS
ΔV_{OUT}	Output Regulation	$-1.24V \geq V_{OUT} \geq -4V$, $0 \leq I_{OUT} \leq 12mA$	●		1	5	%
		$-4V \geq V_{OUT} \geq -5V$, $0 \leq I_{OUT} \leq 8mA$	●		2	5	%
I_{SC}	Output Short Circuit Current	V_{OUT} = 0V	●		35	75	mA
V_{RIP}	Output Ripple Voltage	I_{OUT} = 5mA, V_{OUT} = −4V			5		mV

Doubler Mode, V_{CC} = 5V, C1 = 0.1μF, C2 = 0 (Note 4), C_{OUT} = 3.3μF, F_{SYNC} =700kHz with 50% duty cycle, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LTC1429CS8/LTC1429CS MIN	TYP	MAX	UNITS
ΔV_{OUT}	Output Regulation	$-1.24V \geq V_{OUT} \geq -4V$, $0 \leq I_{OUT} \leq 10mA$	●		1	5	%
		$-4V \geq V_{OUT} \geq -4.5V$, $0 \leq I_{OUT} \leq 10mA$ (Note 6)	●		2	5	%
V_{OUT}	Output Voltage	V_{OUT} Set to −4V, $0 \leq I_{OUT} \leq 10mA$	●	−3.80	−4.00	−4.20	V
I_{SC}	Output Short Circuit Current	V_{OUT} = 0V	●		80	125	mA
V_{RIP}	Output Ripple Voltage	I_{OUT} = 5mA, V_{OUT} = −4V			10		mV

The ● denotes specifications which apply over the full operating temperature range.

Note 1: Absolute Maximum Ratings are those values beyond which the life of the device may be impaired.

Note 2: Setting output to < −7V will exceed the total voltage maximum rating with a 5V supply. With supplies higher than 4V the output should never be set to exceed (V_{CC} – 12V).

Note 3: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground, unless otherwise specified. All typicals are given at T_A = 25°C.

Note 4: C1 = C2 = 0.1μF means the specifications apply to tripler mode where $V_{CC} - V_{OUT} = 3.3V_{CC}$ (LTC1429CS only; the LTC1429CS8 cannot be connected in tripler mode), with C1 connected between $C1^+$ and $C1^-$ and C2 connected between $C2^+$ and $C2^-$. C2 = 0 implies doubler mode where $V_{CC} - V_{OUT} = 2V_{CC}$; for the LTC1429CS, this means C1 connects from $C1^+$ to $C2^-$ with $C1^-$ and $C2^+$ floating. For the LTC1429CS8 in doubler mode, C1 connects from $C1^+$ to $C1^-$; there are no C2 pins.

Note 5: Adjustable output parts only; does not apply to fixed output parts.

Note 6: For output voltages below −4.5V, the LTC1429 may reach 50% duty cycle and fall out of regulation with heavy load or low input voltages. Beyond this point, the output will follow the input with no regulation.

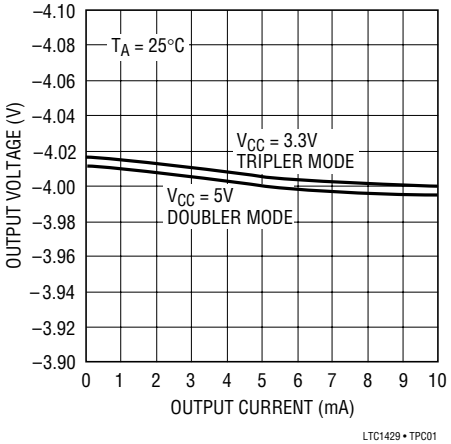
Note 7: LTC1429 will operate with square wave of 40% to 60% duty cycle. For best performance, use a square wave with 50% duty cycle.

Note 8: Maximum frequency is not tested. Typical part can be used beyond 2MHz.

TYPICAL PERFORMANCE CHARACTERISTICS

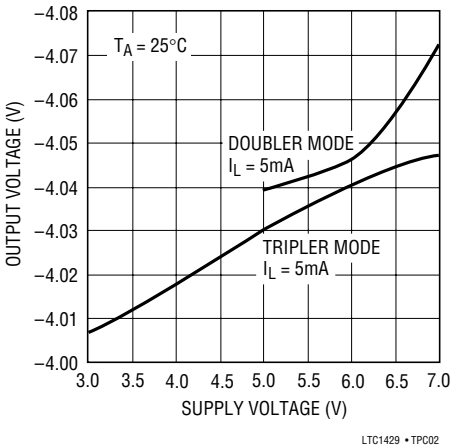
(See Test Circuits; Figure 1 for Doubler Mode, Figure 2 for Tripler Mode)

Output Voltage vs Output Current



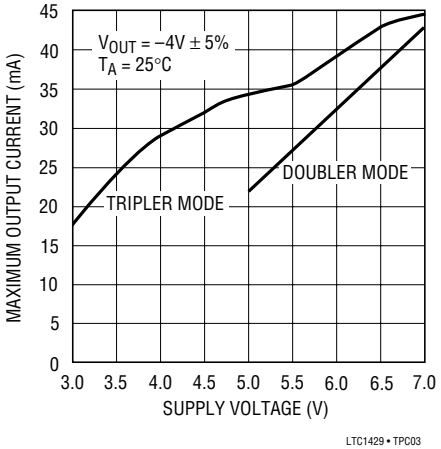
LTC1429 • TPC01

Output Voltage vs Supply Voltage



LTC1429 • TPC02

Maximum Output Current vs Supply Voltage

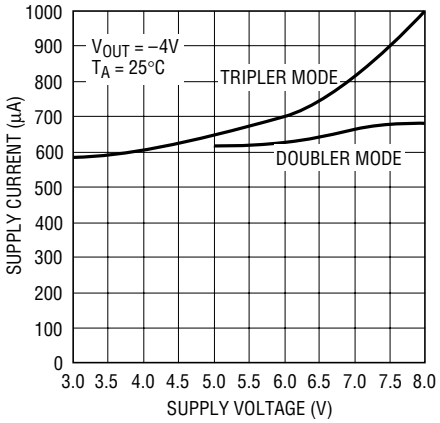


LTC1429 • TPC03

TYPICAL PERFORMANCE CHARACTERISTICS

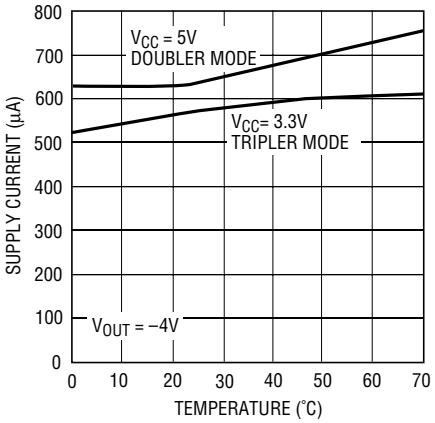
(See Test Circuits: Figure 1 for Doubler Mode, Figure 2 for Tripler Mode)

Supply Current vs Supply Voltage



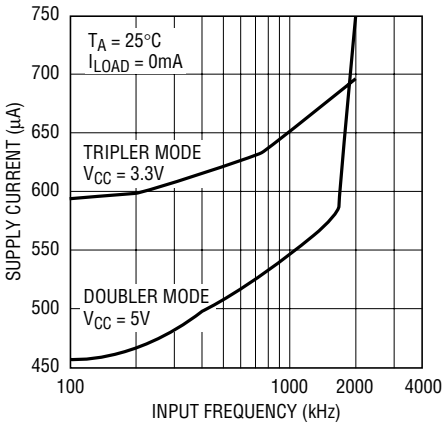
LTC1429 • TPC04

Supply Current vs Temperature



LTC1429 • TPC05

Supply Current vs Input Frequency



LTC1429 • TPC06

PIN FUNCTIONS

Pin numbers are shown as (LTC1429CS/LTC1429CS8).

NC (Pin 1/NA): No Internal Connection.

C1+ (Pin 2/Pin 2): C1 Positive Input. Connect an 0.1µF capacitor between C1+ and C1–. With the LTC1429CS in doubler mode, connect a 0.1µF capacitor from C1+ to C2–.

C1– (Pin 3/Pin 3): C1 Negative Input. Connect a 0.1µF capacitor from C1+ to C1–. With the LTC1429CS in doubler mode only, C1– should float.

C2+ (Pin 4/NA): C2 Positive Input. In tripler mode, connect a 0.1µF capacitor from C2+ to C2– . This pin is used with the LTC1429CS in tripler mode only; in doubler mode, this pin should float.

C2– (Pin 5/NA): C2 Negative Input. In tripler mode, connect a 0.1µF capacitor from C2+ to C2–. In doubler mode, connect a 0.1µF capacitor from C1+ to C2–.

GND (Pin 6/Pin 4): Ground. Connect to a low-impedance ground. A ground plane will help to minimize regulation errors.

R0 (Pin 7/NA): Internal Resistor String-1st Tap. See Table 3 in the Applications Information section for information on internal resistor string pin connections vs output voltage.

R1 (Pin 8/NA): Internal Resistor String-2nd Tap.

R_{ADJ} (Pin 9/NA): Internal Resistor String Output. Connect this pin to ADJ to use the internal resistor divider. See Table 3 in the Applications Information section for information on internal resistor string pin connections vs output voltage.

ADJ (COMP for fixed output versions) (Pin 10/Pin 5): Output Adjust/Compensation. For adjustable parts, this pin is used to set the output voltage. The output voltage should be divided down with a resistor divider and fed back to this pin to set the regulated output voltage. The resistor divider can be external or the internal divider string can be used if it can provide the required output voltage. Typically the resistor string should draw ≥ 10µA from the output to minimize errors due to the bias current at the adjust pin. Fixed output parts have the internal resistor string connected to this pin inside the package; the pin can be used to trim the output voltage if desired. It can also be used as an optional feedback compensation pin to reduce output ripple on both adjustable and fixed output voltage parts. See the Applications Information section for more on compensation and output ripple.

OUT (Pin 11/Pin 6): Negative Voltage Output. This pin must be bypassed to ground with a 1.0µF or larger capacitor; it must be at least 3.3µF to provide specified output ripple. The size of the output capacitor has a strong

PIN FUNCTIONS

effect on output ripple; see the Applications Information section for more details.

REG (Pin 12/Pin 7): This is an open drain output that pulls low when the output voltage is within 5% of the set value. It will sink 10mA to ground with a 5V supply. The external circuitry must provide a pull-up or REG will not swing high. The voltage at REG may exceed V_{CC}; it can be pulled up to 12V above ground without damage.

SYNC/SD (Pin 13/Pin 8): Synchronous Clock Input. A minimum input clock frequency (60kHz with $V_{CC} \leq 5V$ and 100kHz with V_{CC} = 6.5V) must be applied to this input to keep the LTC1429 operating normally. An input clock below the minimum frequency may cause the charge pump to operate erratically or the device to shut down. A logic high or low at the SYNC/SD pin will put the device into SHUTDOWN and drop the supply current to 0.2μA. The LTC1429 will operate with input square wave of 40% to 60% duty cycle. For best performance, use a square wave of 50% duty cycle.

V_{CC} (Pin 14/Pin 1): Power Supply. This requires an input voltage between 3V and 6.5V. Certain combinations of output voltage and operating mode may place additional restrictions on the input voltage; see the Applications Information section for details. V_{CC} must be bypassed to ground with at least a 0.1μF capacitor, placed in close proximity to the chip; again, see the Applications Information section.

TEST CIRCUITS

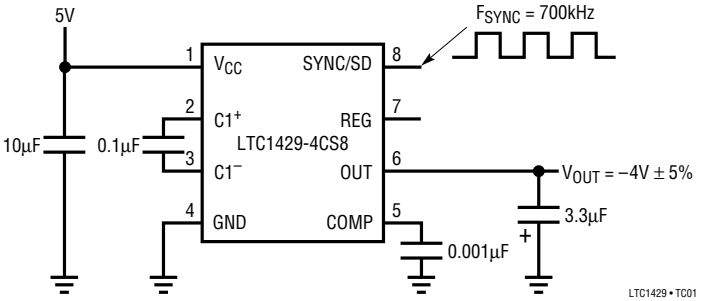


Figure 1. Doubler Mode

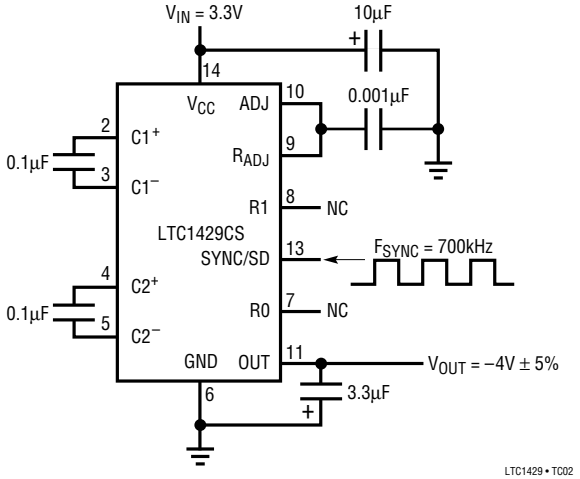


Figure 2. Tripler Mode

APPLICATIONS INFORMATION

MODES OF OPERATION

The LTC1429 uses a charge pump to generate a negative output voltage that can be regulated to a value either higher or lower than the original input voltage. It has two modes of operation: a doubler inverting mode, which can provide a negative output equal to or less than the positive power supply, and a tripler inverting mode, which can provide negative output voltages either larger or smaller in magnitude than the original positive supply. The tripler offers greater versatility and wider input range but requires four external capacitors and a 14-pin package; the doubler offers the SO-8 package and requires only three external capacitors. The optional compensation capacitor at ADJ/COMP is used to reduce the ripple output voltage.

Doubler Mode

This mode allows the LTC1429 to generate negative output voltage magnitudes up to that of the supply voltage,

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creating a voltage between V_{CC} and OUT of up to $2 \times V_{CC}$. In doubler mode, the LTC1429 uses a single flying capacitor to invert the input supply voltage and the output voltage is stored on the output bypass capacitor between switch cycles. The LTC1429CS8 is always configured in doubler mode and has only one pair of flying capacitor pins (Figure 3a). The LTC1429CS can be configured in doubler mode by connecting a single flying capacitor between the $C1^+$ and $C2^-$ pins; $C1^-$ and $C2^+$ should be left floating (Figure 3b).

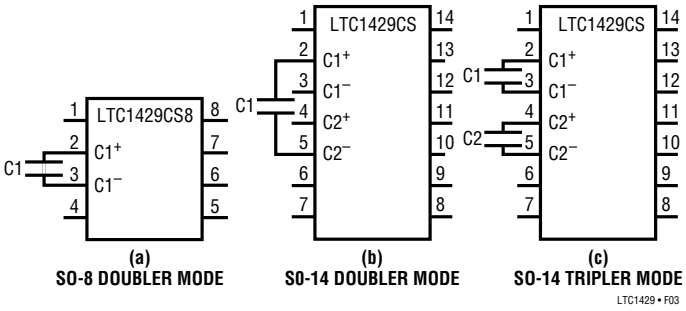

Figure 3. Flying Capacitor Connections

Tripler Mode

The LTC1429CS can be used in a tripler mode which can generate negative output voltages up to twice the supply voltage; the total voltage between the V_{CC} and OUT pins is $3 \times V_{CC}$. Tripler mode can be used to generate –5V from a single positive 3.3V supply, for example. Tripler mode requires two external flying capacitors. The first connects between $C1^+$ and $C1^-$ and the second between $C2^+$ and $C2^-$ (Figure 3c). Because of the relatively high voltages that can be generated in this mode, care must be taken to ensure that the total input-to-output voltage never exceeds 12V, or the LTC1429 may be damaged. This is possible with supply voltages above 4V in tripler mode and above 6V in doubler mode, although in most applications the output voltage will be kept in check by the regulation loop. As the input supply voltage rises, the allowable output voltage drops, finally reaching –4V with a 8.5V supply. To avoid this problem, use doubler mode whenever possible with high input supply voltages.

THEORY OF OPERATION

A block diagram of the LTC1429 is shown in Figure 4. The heart of the LTC1429 is the charge pump core, shown in the dashed line. It generates a negative output voltage by first charging the flying caps between V_{CC} and ground. It then

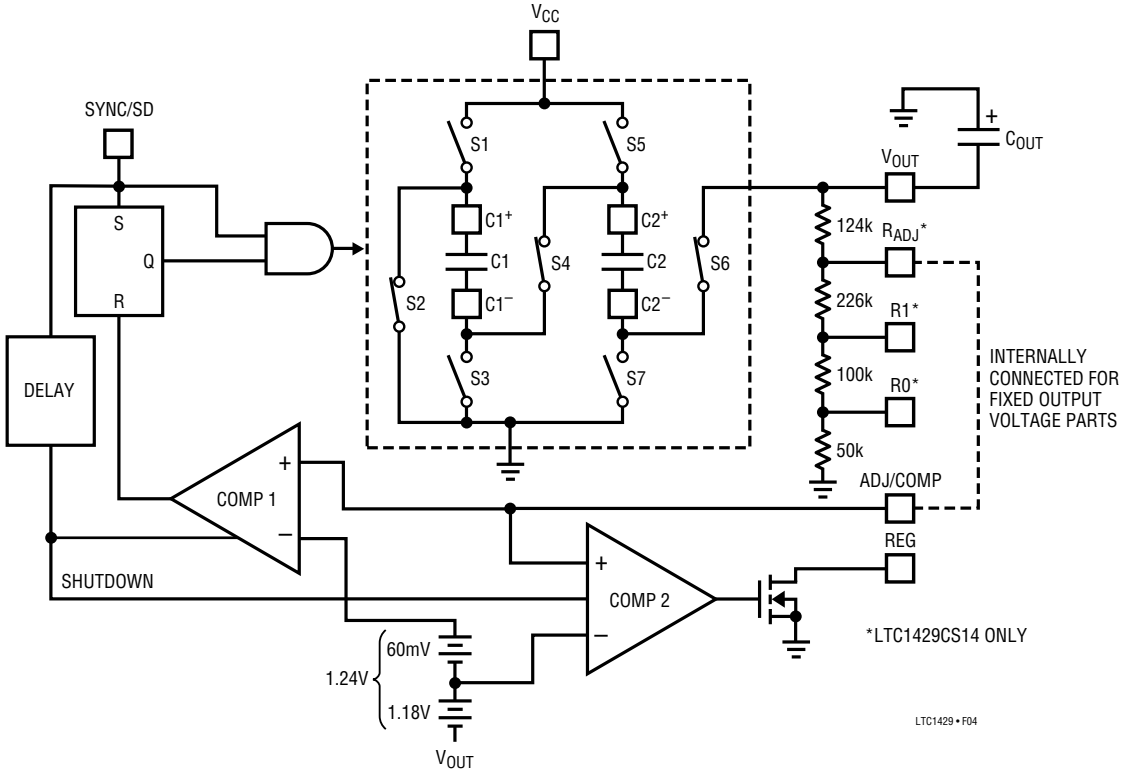

Figure 4. Block Diagram

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stacks the flying caps on top of each other and connects the top of the stack to ground; this forces the bottom of the stack to a negative voltage. The charge on the flying capacitors is transferred to the output bypass cap, leaving it charged to the negative output voltage. This process is driven by the external 700kHz clock via the SYNC/SD pin.

Figure 4 shows the charge pump configured in tripler mode. With the external input clock low, C1 and C2 are charged to V_{CC} by S1, S3, S5 and S7. At the next rising clock edge, S1, S3, S5 and S7 open and S2, S4 and S6 close, stacking C1 and C2 on top of each other. S2 connects $C1^+$ to ground, S4 connects $C1^-$ to $C2^+$ and $C2^-$ is connected to the output by S6. The charge in C1 and C2 is transferred to C_{OUT}, setting it to a negative voltage. Doubler mode works the same way except that the single flying capacitor (C1) is connected between $C1^+$ and $C2^-$. S3, S4 and S5 don't do anything useful in doubler mode. C1 is charged initially by S1 and S7, and connected to the output by S2 and S6.

The output voltage is monitored by COMP1, which compares a divided replica of the output at ADJ (COMP for fixed output parts) to the internal reference. At the beginning of a cycle, the clock is low, forcing the output of the AND gate low and charging the flying caps. The next rising clock edge sets the RS latch, setting the charge pump to transfer charge from the flying caps to the output capacitor. As long as the output is below the set point, COMP1 stays low, the latch stays set and the charge pump runs at the duty cycle of the input clock signal, gated through the AND gate. As the output approaches the set voltage, COMP1 will trip whenever the divided signal exceeds the internal 1.24V reference, relative to OUT. This resets the RS latch and truncates the clock pulses, internally reducing the amount of charge transferred to the output capacitor and regulating the output voltage. If the output exceeds the set point, COMP1 stays high, inhibiting the RS latch and disabling the charge pump.

COMP2 also monitors the divided signal at ADJ, but it is connected to a 1.18V reference, 5% below the main reference voltage. When the divided output exceeds this lower reference voltage, indicating that the output is within 5% of the set value, COMP2 goes high, turning on the REG output transistor. This is an open drain N-channel device capable of sinking 8mA with a 3.3V V_{CC} and 15mA with a 5V V_{CC}. When in "off" state (divided output more than 5% below V_{REF}) the drain can be pulled above V_{CC} without damage, up to a maximum of 12V above ground. Note that the REG output only indicates if the magnitude of the output is *below* the magnitude of the set point by 5% (i.e., $V_{OUT} > -4.75V$ for a $-5V$ set point). If the magnitude of the output is forced *higher* than the magnitude of the set point (i.e., to $-6V$ when the output is set for $-5V$) the REG output will stay low.

OUTPUT RIPPLE

Output ripple in the LTC1429 comes from two sources: voltage droop at the output capacitor between clocks and frequency response of the regulation loop. Voltage droop is easy to calculate. With a typical external input clock frequency of 700kHz, the charge on the output capacitor is refreshed once every 1.43µs. With a 15mA load and a 3.3µF output capacitor, the output will droop by:

$$I_{LOAD} \times \left(\frac{\Delta t}{C_{OUT}}\right) = 15mA \times \left(\frac{1.43\mu s}{3.3\mu F}\right) = 6.5mV$$

There can be a significant ripple component when the output is heavily loaded, especially if the output capacitor is small or the external input clock frequency is low. If absolute minimum output ripple is required, a 10µF or greater output capacitor, high input clock rate (F_{SYNC}) and lower value (<0.1µF) of flying capacitor should be used.

Regulation loop frequency response is the other major contributor to output ripple. The LTC1429 regulates the output voltage by limiting the amount of charge transferred to the output capacitor on a cycle-by-cycle basis. The output voltage is sensed at the ADJ pin (COMP for fixed output versions) through an internal or external resistor divider from the OUT pin to ground. As the flying caps are first connected to the output, the output voltage begins to change quite rapidly. As soon as it exceeds the set point, COMP1 trips, switching the state of the charge pump and stopping the charge transfer. Because the RC time constant of the capacitors and the switches is quite short, the ADJ pin must have a wide AC bandwidth to be able to respond to the output in time. External parasitic capacitance at the ADJ pin can reduce the bandwidth to the point where the comparator cannot respond by the time

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the clock pulse finishes. When this happens, the comparator will allow a few complete pulses through, then overcorrect and disable the charge pump until the output drops below the set point. Under these conditions, the output will remain in regulation, but the output ripple will increase as the comparator "hunts" for the correct value.

To help prevent this from happening, an external capacitor can be connected from ADJ (or COMP for fixed output parts) to ground to compensate for external parasitics and increase the regulation loop bandwidth (Figure 5). This sounds counter-intuitive until we remember that the internal reference is generated with respect to OUT, not ground. The feedback loop actually sees ground as its "output"; thus the compensation capacitor should be connected across the "top" of the resistor divider from ADJ (or COMP) to ground. By the same token, avoid adding capacitance between ADJ (or COMP) and V_{OUT}; this will slow down the feedback loop and increase output ripple. A 1000pF capacitor from ADJ or COMP to ground will compensate the loop properly under most conditions.

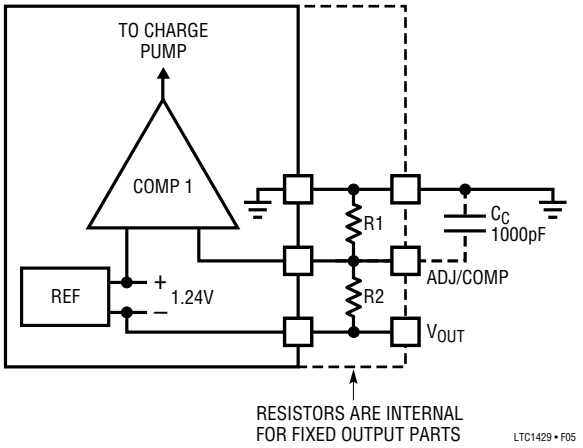


Figure 5. Regulator Loop Compensation

EXTERNAL CLOCK

The LTC1429 requires an external clock to operate. This clock signal should be TTL or CMOS compatible and should be applied to the SYNC/SD pin. The external clock allows the user to control the frequency at which the LTC1429 operates, preventing it from interfering with other frequency-sensitive circuitry. The LTC1429 can be synchronized to any frequency between 60kHz (100kHz for V_{CC} > 5) and 2MHz. Higher clock frequencies can help reduce output ripple at the cost of additional quiescent current. The clock signal should have a duty cycle between 40% and 60% for proper regulation loop performance.

The LTC 1429 can be shut down by stopping the clock. An internal circuit monitors the time between clock edges at the SYNC/SD pin. If a 10μs period elapses without a rising or falling edge, LTC1429 assumes the clock has stopped and goes into shutdown mode and the quiescent current drops to below 1μA. The next clock edge at the SYNC/SD pin will reawaken the LTC1429. At clock frequencies below 50kHz (50% duty cycle) the LTC1429 may enter shutdown mode briefly during each clock cycle causing erratic operation. Minimum operating frequency should be kept above 60kHz (above 100kHz with V_{CC} > 5) to prevent this from happening.

Radiation from the clock signal at the SYNC/SD pin can interfere with the feedback node at the ADJ/COMP pin causing errors in the output voltage. The clock line should be routed away from the circuitry at the ADJ/COMP pin and should be shielded with a ground plane or with coaxial cable. A compensation capacitor from the ADJ/COMP pin to ground can also help to reduce this effect: 0.001μF is adequate for most applications.

OUTPUT FILTERING

If extremely low output ripple (<10mV) is required, additional output filtering is required. Because the LTC1429 uses a high, external control switching frequency, fairly low value RC or LC networks can be used at the output to effectively filter the output ripple. With F_{SYNC} = 700kHz, a 10Ω series output resistor and a 3.3μF capacitor will cut output ripple to below 3mV (see Figure 6). Further reduc-

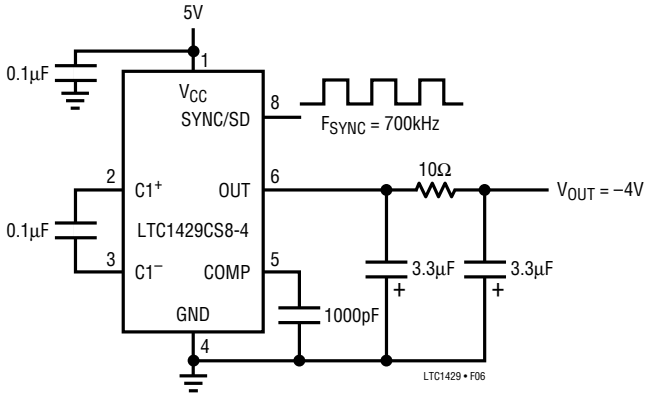


Figure 6. Output Filter Cuts Ripple Below 3mV

APPLICATIONS INFORMATION

tions can be obtained with larger filter capacitors or by using an LC output filter or higher F_{SYNC} clock rate with a lower value (<0.1μF) of flying capacitor. Also see the section on Output Capacitor ESR. For applications requiring ripple below 1mV, see the LTC1550/LTC1551 data sheet.

CAPACITOR SELECTION

Capacitor Sizing

The performance is dependent on the type of capacitors used. The LTC1429 requires bypass caps to ground for both the V_{CC} and OUT pins. The input cap provides most of the LTC1429's supply current while it is charging the flying caps. It should be mounted as close to the package as possible, its value should be equal to or larger than the flying cap in doubling mode and at least twice the value of the flying caps in tripling mode. Ceramic capacitors generally provide adequate performance; avoid using a tantalum capacitor as the input bypass unless there is at least a 0.1μF ceramic cap in parallel with it. The charge pump caps are somewhat less critical, since their peak currents are limited by the switches inside the LTC1429. Most applications should use 0.1μF as the flying cap value; conveniently, ceramic caps are the most common type of 0.1μF cap and they work well here. Usually the easiest solution is to use the same type of capacitor for both the input bypass and flying caps.

The output cap performs two functions; it provides output current to the load during half of the charge pump cycle and its value helps to set the output ripple voltage. For applications that are insensitive to output ripple, the output bypass cap can be as small as 1μF. To achieve specified low output ripple, a 3.3μF or greater output capacitor, high input clock rate (F_{SYNC}) and lower value (<0.1μF) of flying capacitor should be used. Larger output caps will reduce output ripple further, at the expense of turn on time.

In an application where the maximum load current is well-defined and output ripple is critical or input peak currents need to be minimized, the flying capacitor values can be tailored to the application. Reducing the value of the flying capacitors reduces the amount of charge transferred with each clock cycle. The smaller capacitors draw smaller pulses of current out of V_{CC} as well, limiting peak currents and reducing the demands on the input supply. Tables 1 and 2 show recommended values of flying capacitors vs maximum load capacity at F_{SYNC} = 400kHz and 700kHz respectively.

Table 1. Typical Max Load (mA) vs Flying Capacitor Value at T_A = 25°C, V_{OUT} = –4V, F_{SYNC} = 400kHz

FLYING CAPACITOR VALUE (μF)	MAX LOAD (mA) V_{CC} = 5V DOUBLER MODE	MAX LOAD (mA) V_{CC} = 3.3V TRIPLER MODE
0.1	22	20
0.047	16	15
0.033	8	11
0.022	4	5
0.01	1	3

Table 2. Typical Max Load (mA) vs Flying Capacitor Value at T_A = 25°C, V_{OUT} = –4V, F_{SYNC} = 700kHz

FLYING CAPACITOR VALUE (μF)	MAX LOAD (mA) V_{CC} = 5V DOUBLER MODE	MAX LOAD (mA) V_{CC} = 3.3V TRIPLER MODE
0.1	18	25
0.047	17	22
0.033	14	20
0.022	12	17
0.01	3	9

Output Capacitor ESR

Output capacitor the Equivalent Series Resistance (ESR) is another factor to consider. Excessive ESR in the output capacitor can fool the regulation loop into keeping the output artificially low by prematurely terminating the charging cycle. As the charge pump switches to recharge the output, a brief surge of current flows from the flying caps to the output cap. This current surge can be as high as 100mA under full load conditions. A typical 3.3μF tantalum capacitor has 1Ω or 2Ω of ESR; 100mA × 2Ω = 200mV. If the output is within 200mV of the set point, this additional 200mV surge will trip the feedback comparator and terminate the charging cycle. The pulse dissipates quickly and the comparator returns to the correct state, but the RS latch will not allow the charge pump to respond until the next clock edge. This prevents the charge pump from

APPLICATIONS INFORMATION

going into very high frequency oscillation under such conditions. It also creates an output error as the feedback loop regulates based on the top of the spike, not the average value of the output (Figure 7). The resulting output voltage behaves as if a resistor of value $C_{ESR} \times (I_{PK}/I_{AVE})\Omega$ was placed in series with the output. To minimize this effect, output capacitor ESR should be as low as possible or smaller value high frequency bypass (typically a 0.1µF ceramic) should be added in parallel with the output capacitor.

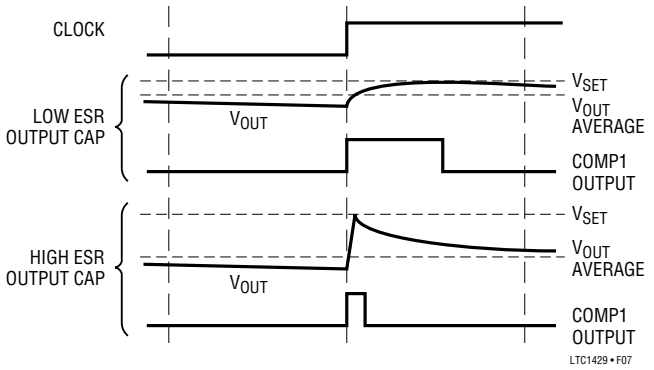


Figure 7. Output Ripple with Low and High ESR Caps

Note that ESR in the flying caps will not cause the same condition; in fact, it may actually improve the situation by cutting the peak currents and lowering the amplitude of the spike. More flying cap ESR is not necessarily better, however; as soon as the RC time constant approaches half of a clock period (the time the capacitors have to share charge at full duty cycle) the output current capability of the LTC1429 will begin to diminish. For 0.1µF flying capacitors and typical 700kHz external clock, this gives a maximum total series resistance of:

$$\frac{1}{2}\left(\frac{t_{CLK}}{C_{FLY}}\right) = \frac{1}{2}\left(\frac{1}{700kHz}\right) / 0.1\mu F = 7.14\Omega$$

Most of this resistance is already provided by the internal switches in the LTC1429 (especially in tripler mode). More than 1Ω or 2Ω of ESR on the flying caps will start to affect the regulation at maximum load.

RESISTOR SELECTION

Resistor selection is easy with the fixed output versions of the LTC1429; no resistors are needed! Selecting the right resistors for the adjustable parts is only a little more difficult. A resistor divider should be used to divide the signal at the output to give 1.24V at the ADJ pin *with respect to* V_{OUT} (Figure 8). The LTC1429 uses a positive reference with respect to V_{OUT}, not a negative reference with respect to ground (Figure 4 shows reference connection). Be sure to keep this in mind when connecting the resistors! If the initial output is not what you expected, try swapping the two resistors.

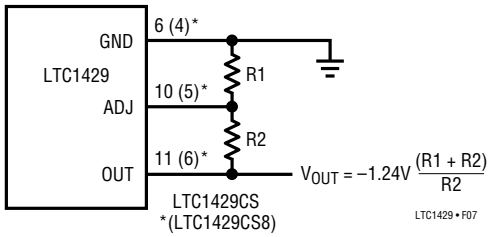


Figure 8. External Resistor Connections

The 14-pin adjustable parts include a built-in resistor string which can provide an assortment of output voltages by using different pin-strapping options at the RO, R1 and R_{ADJ} pins (Table 3). The internal resistors are roughly 124k, 226k, 100k and 50k (see Figure 4) giving output options of –3.5V, –4V, –4.5V and –5V. The resistors are carefully matched to provide accurate divider ratios, but the absolute values can vary substantially from part to part. It's not a good idea to create a divider using an external resistor and one of the internal resistors unless the output voltage accuracy is not critical.

Table 3. Output Voltages Using the Internal Resistor Divider

PIN CONNECTIONS	OUTPUT VOLTAGE
ADJ - R_{ADJ}	–5.0V
ADJ - R_{ADJ}, RO - GND	–4.5V
ADJ - R_{ADJ}, R1 - RO	–4.0V
ADJ - R_{ADJ}, R1-GND	–3.5V
ADJ - R1	–1.77V
ADJ - R0	–1.38V
ADJ - GND	–1.24V

There are some oddball output voltages available as well. They are obtained by connecting ADJ to R0 or R1 and shorting out some of the internal resistors. If one of them gives you the output voltage you want, by all means use it!

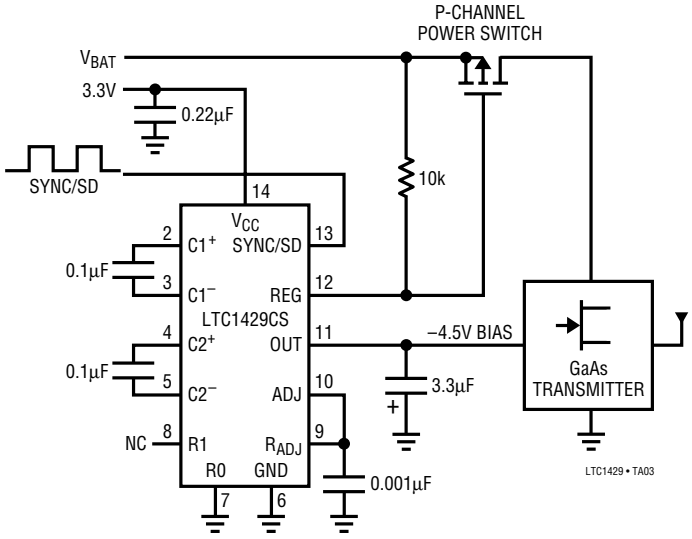
APPLICATIONS INFORMATION

The internal resistor values are the same for the fixed output versions of the LTC1429 as they are for the adjustable parts. The output voltage can be trimmed, if desired, by connecting external resistance from the COMP pin to OUT or ground to alter the divider ratio. As in the adjustable parts, the absolute value of the internal resistors may vary significantly from unit to unit. As a result, the further the trim shifts the output voltage, the less accurate the output voltage will be. If a precise output voltage other than one of the available fixed voltages is required, it's better to use an adjustable LTC1429 and use precision external resistors. The internal reference is trimmed at the factory to within 3.5% of 1.24V. With 1% external resistors, the output will be within 5.5% of the nominal value, even under worst case conditions.

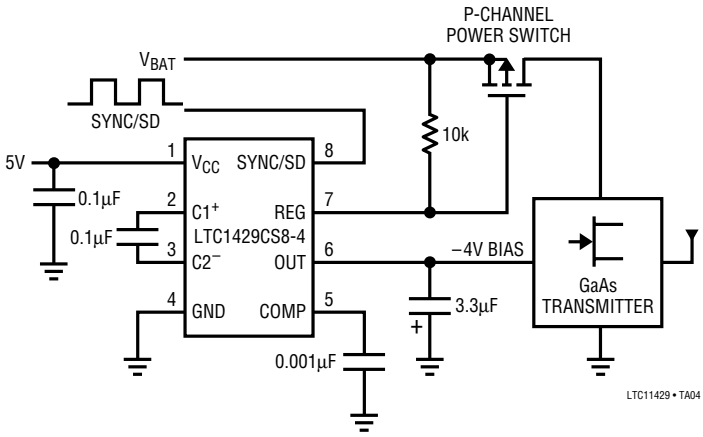
The LTC1429 can be internally configured with nonstandard fixed output voltages. For details, contact the Linear Technology Marketing Department.

TYPICAL APPLICATIONS

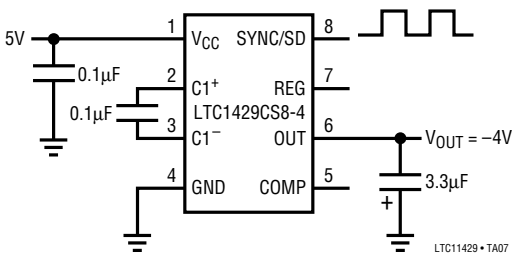
3.3V In, –4.5V Out GaAs FET Bias Generator



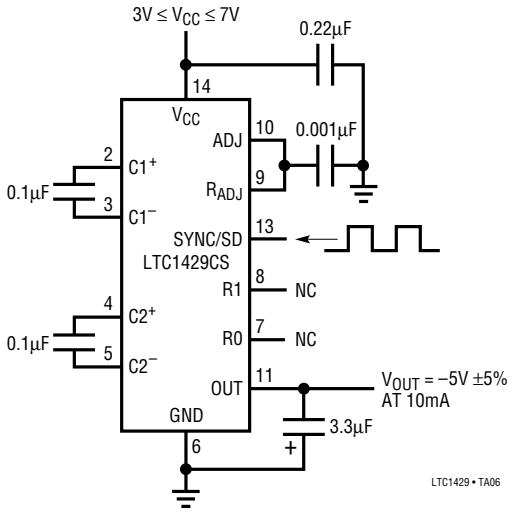
5V In, –4V Out GaAs FET Bias Generator



Minimum Parts Count –4V Generator



–5V Supply Generator



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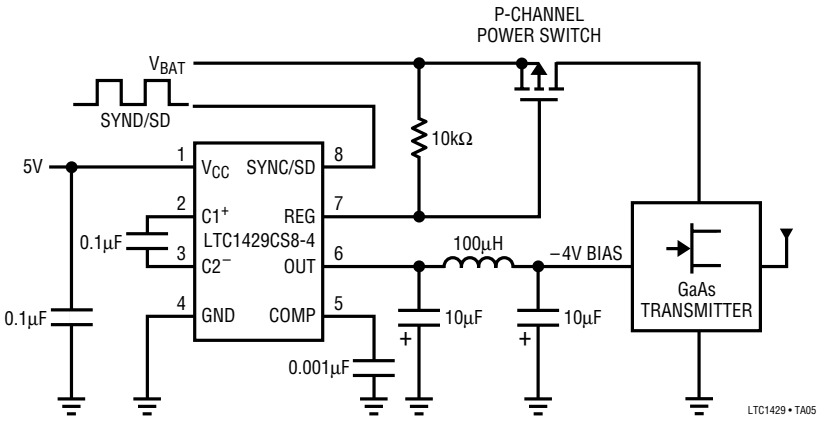
TYPICAL APPLICATIONS

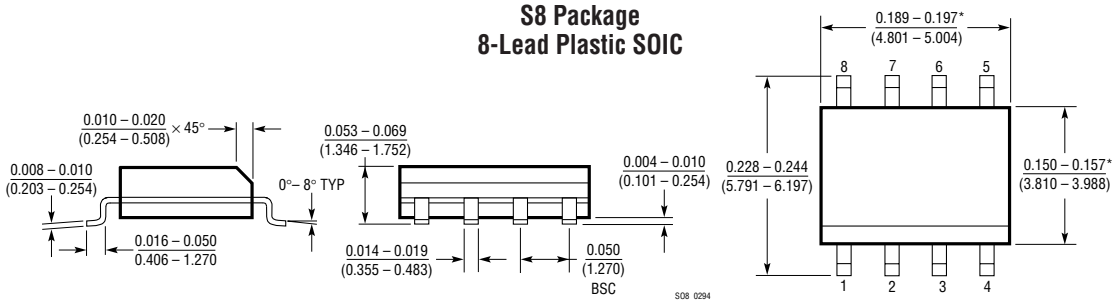
1mV Ripple, 5V In, –4V Out GaAs FET Bias Generator



PACKAGE DESCRIPTION

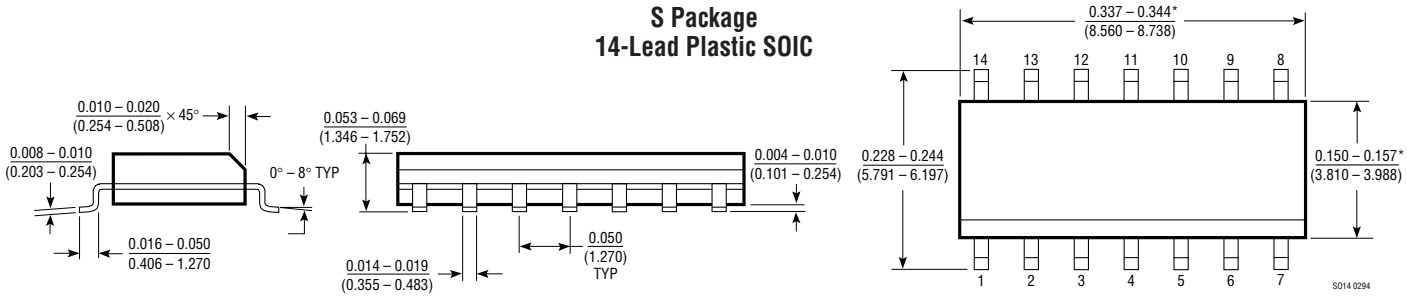
Dimension in inches (millimeters) unless otherwise noted.

S8 Package
8-Lead Plastic SOIC



*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 INCH (0.15mm).

S Package
14-Lead Plastic SOIC



*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 INCH (0.15mm).

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1121	Micropower Low Dropout Regulators with Shutdown	0.4V Dropout Voltage at 150mA, Low Noise, Switched Capacitor Regulated Voltage Inverter
LTC1261	Switched Capacitor Regulated Voltage Inverter	Selectable Fixed Output Voltage
LTC1550/LTC1551	Low Noise Switched Capacitor Regulated Voltage Inverter	GaAs FET Bias with Linear Regulator 1mV Ripple

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