Hot Swap Controller

FEATURES

- **Allows Safe Board Insertion and Removal from a Live Backplane**
- **System Reset and Power Good Control Outputs**
- **Programmable Electronic Circuit Breaker**
- User Programmable Supply Voltage Power-Up Rate
- High Side Driver for Two External N-Channels
- Controls Supply Voltages from 3V to 12V
- Connection Inputs Detect Board Insertion or Removal
- Undervoltage Lockout
- Power-On Reset Input

APPLICATIONS

- Hot Board Insertion
- Electronic Circuit Breaker

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Hot Swap is a trademark of Linear Technology Corporation.

DESCRIPTION

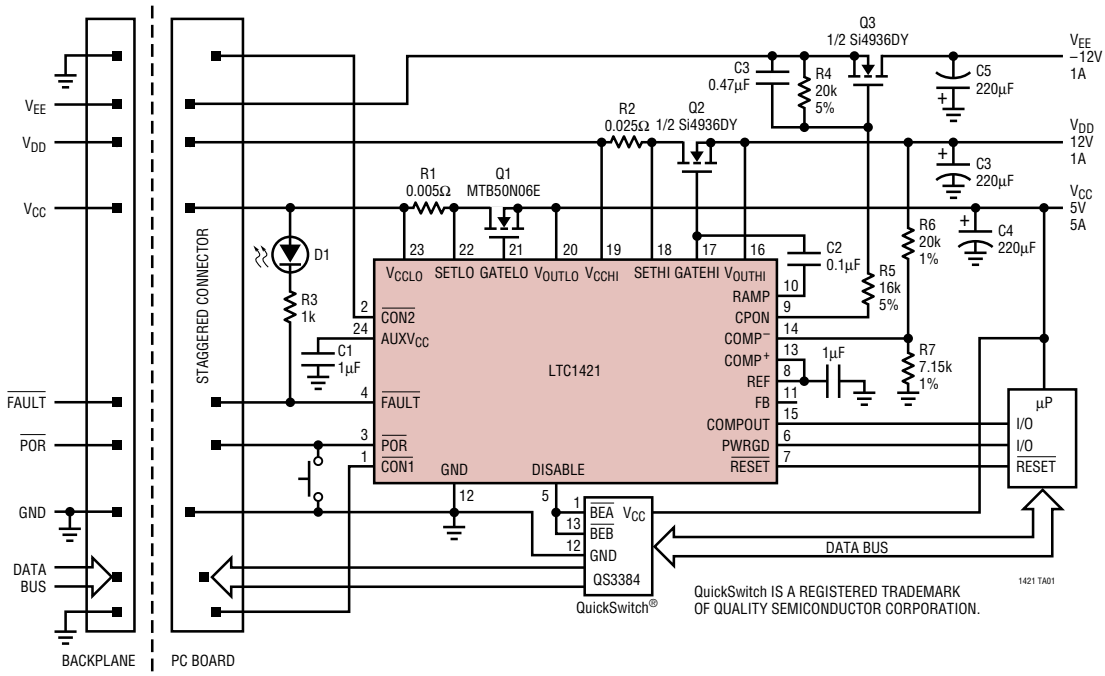
The LTC®1421/LTC1421-2.5 are Hot Swap™ controllers that allow a board to be safely inserted and removed from a live backplane. Using external N-channel pass transistors, the board supply voltages can be ramped up at a programmable rate. Two high side switch drivers control the N-channel gates for supply voltages ranging from 3V to 12V.

A programmable electronic circuit breaker protects against shorts. Warning signals indicate that the circuit breaker has tripped, a power failure has occurred or that the switch drivers are turned off. The reset output can be used to generate a system reset when the power cycles or a fault occurs. The two connect inputs can be used with staggered connector pins to indicate board insertion or removal. The power-on reset input can be used to cycle the board power or clear the circuit breaker.

The trip point of the ground sense comparator is set at 0.1V for LTC1421 and 2.5V for LTC1421-2.5.

The LTC1421/LTC1421-2.5 are available in 24-pin SO and SSOP packages.

TYPICAL APPLICATION

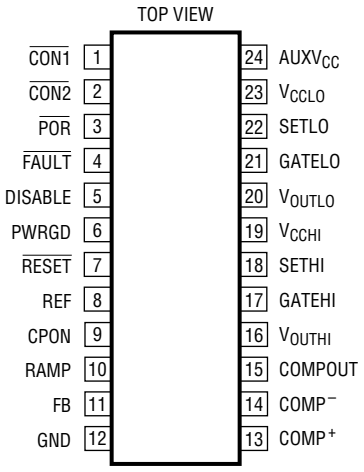


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage (V_{CCLO}, V_{CCHI}, $AUXV_{CC}$) 13.2V
Input Voltage (Analog Pins) ..... – 0.3V to (V_{CCHI} + 0.3V)
Input Voltage (Digital Pins) ..... – 0.3V to 13.2V
Output Voltage (Digital Pins) .. – 0.3V to (V_{CCLO} + 0.3V)
Output Voltage (CPON) ..... – 13.2V to (V_{CCLO} + 0.3V)
Output Voltage (V_{OUTLO}, V_{OUTHI}) ..... –0.3V to 13.2V
Output Voltage (GATELO, GATEHI) ..... –0.3V to 20V
Operating Temperature Range ..... 0°C to 70°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)..... 300°C

PACKAGE/ORDER INFORMATION



G PACKAGE
24-LEAD PLASTIC SSOP

SW PACKAGE
24-LEAD PLASTIC SO

T_{JMAX} = 125°C, θ_{JA} = 100°C/W (G)
T_{JMAX} = 125°C, θ_{JA} = 85°C/W (SW)

ORDER PART NUMBER

LTC1421CG
LTC1421CSW
LTC1421-2.5CG
LTC1421-2.5CSW

Consult factory for Industrial and Military grade parts.

ELECTRICAL CHARACTERISTICS

V_{CCHI} = 12V, V_{CCLO} = 5V, T_A = 25°C unless otherwise noted (Note 2).

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
DC Characteristics							
I_{CCLO}	V_{CCLO} Supply Current	$\overline{CON1}$ = $\overline{CON2}$ = GND, $\overline{POR}$ = V_{CCLO}	●		1.5	3	mA
I_{CCHI}	V_{CCHI} Supply Current	$\overline{CON1}$ = $\overline{CON2}$ = GND, $\overline{POR}$ = V_{CCLO}	●		0.6	1	mA
V_{LKO}	Undervoltage Lockout	V_{CCLO} and V_{CCHI}		2.28	2.45	2.60	V
V_{LKH}	Undervoltage Lockout Hysteresis	V_{CCLO} and V_{CCHI}			100		mV
V_{REF}	Reference Output Voltage	No Load	●	1.220	1.232	1.244	V
ΔV_{LNR}	Reference Line Regulation	3V ≤ V_{CCLO} ≤ 12V, No Load	●		4	8	mV
ΔV_{LDR}	Reference Load Regulation	I_O = 0mA to –5mA, Sourcing Only	●		1	3	mV
I_{RSC}	Reference Short-Circuit Current	V_{REF} = 0V			–45		mA
V_{COF}	Comparator Offset Voltage	0V ≤ V_{CM} ≤ (V_{CCLO} – 1.3V)	●			±10	mV
V_{CPSR}	Comparator Power Supply Rejection	0V ≤ V_{CM} ≤ (V_{CCLO} – 1.3V), 3V ≤ V_{CCLO} ≤ 12V	●			1	mV/V
V_{CHST}	Comparator Hysteresis	0V ≤ V_{CM} ≤ (V_{CCLO} – 1.3V)			7		mV
V_{RST}	Reset Voltage Threshold (V_{OUTLO})	FB = V_{OUTLO} FB = Floating FB = GND	● ● ●	2.80 4.50 5.75	2.90 4.65 5.88	3.00 4.75 6.01	V V V
V_{RHST}	Reset Threshold Hysteresis (V_{OUTLO})	FB = V_{OUTLO} FB = Floating FB = GND			7 12 15		mV mV mV
R_{FB}	FB Pin Input Resistance	0V ≤ V_{FB} ≤ V_{CCLO}			95		kΩ
V_{CB}	Circuit Breaker Trip Voltage	V_{CB} = (V_{CCLO} – V_{SETLO}) or V_{CB} = (V_{CCHI} – V_{SETHI})	●	40	50	60	mV
V_{TRIP}	Output Voltage for Re-Power-Up	LTC1421 (Note 3) LTC1421-2.5 (Note 4)			0.1 2.5		V V

ELECTRICAL CHARACTERISTICS

V_{CCHI} = 12V, V_{CCLO} = 5V, T_A = 25°C unless otherwise noted (Note 2).

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_{RAMP}	RAMP Pin Output Current	Charge Pump On, V_{RAMP} = 0.4V	●	11	17	23	µA
I_{CP}	Charge Pump Output Current	Charge Pump On, GATEHI = 0V GATELO = 0V			–600 –300		µA µA
ΔV_{GATEHI}	GATEHI N-Channel Gate Drive	$V_{GATEHI} - V_{OUTHI}$		6		16	V
ΔV_{GATELO}	GATELO N-Channel Gate Drive	$V_{GATELO} - V_{OUTLO}$		10		16	V
V_{AUXVCC}	Auxiliary V_{CC} Output Voltage	V_{CCLO} = 5V, Unloaded			4.5		V
V_{IL}	Input Low Voltage	$\overline{CON1}$, $\overline{CON2}$, $\overline{POR}$	●			0.8	V
V_{IH}	Input High Voltage	$\overline{CON1}$, $\overline{CON2}$, $\overline{POR}$	●	2			V
I_{IN}	Input Current	$\overline{CON1}$, $\overline{CON2}$, $\overline{POR}$ = GND	●	–30	–60	–90	µA
V_{OL}	Output Low Voltage	$\overline{RESET}$, COMPOUT, PWRGD, DISABLE, $\overline{FAULT}$, I_O = 3mA	●			0.4	V
		CPON, I_O = 3mA	●			1.45	V
V_{OH}	Output High Voltage	DISABLE, I_O = –3mA	●	4			V
		CPON, I_O = –1mA	●	3.4			V
I_{PU}	Logic Output Pull-Up Current	$\overline{RESET}$, PWRGD, $\overline{FAULT}$ = GND			–15		µA
AC CHARACTERISTICS							
t_1	$\overline{CON1}$ or $\overline{CON2}$↓ to CPON↑	Figure 1, C_L = 15pF	●	15	20	30	ms
t_2	PWRGD↑ to $\overline{RESET}$↑	Figure 1, R_L = 10k to V_{CCLO}, C_L = 15pF	 ●	160 140	200 200	240 280	ms ms
t_3	PWRGD↑ to DISABLE↓	Figure 1, C_L = 15pF	 ●	160 140	200 200	240 280	ms ms
t_4	$\overline{POR}$↓ to CPON↓	Figure 1, C_L = 15pF	●	15	20	30	ms
t_5	PWRGD↓ to $\overline{RESET}$↓	Figure 1, R_L = 10k to V_{CCLO}, C_L = 15pF			32		µs
t_6	$\overline{POR}$↑ to CPON↑	Figure 1, C_L = 15pF			50		ns
t_7	$\overline{CON1}$ or $\overline{CON2}$↑ to CPON↓	Figure 1, C_L = 15pF			50		ns
t_9	Short-Circuit Detect to $\overline{FAULT}$↓	Figure 1, R_L = 10k to V_{CCLO}, C_L = 15pF V_{CCLO} – SETLO = 0mV to 100mV			20		µs
t_{10}	Short-Circuit Detect to CPON↓	Figure 2, C_L = 15pF V_{CCLO} – SETLO = 0mV to 100mV			20		µs
t_{11}	$\overline{POR}$↑ to $\overline{FAULT}$↑	Figure 2, R_L = 10k to V_{CCLO}, C_L = 15pF			20		ns
t_{CHL}	Comparator High to Low	$COMP^-$ = 1.232V, 10mV Overdrive R_L = 10k to V_{CCLO}, C_L = 15pF	●		0.25	0.5	µs
t_{CLH}	Comparator Low to High	$COMP^-$ = 1.232V, 10mV Overdrive R_L = 10k to V_{CCLO}, C_L = 15pF	●		1	1.5	µs

The ● denotes specifications which apply over the full operating temperature range.

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

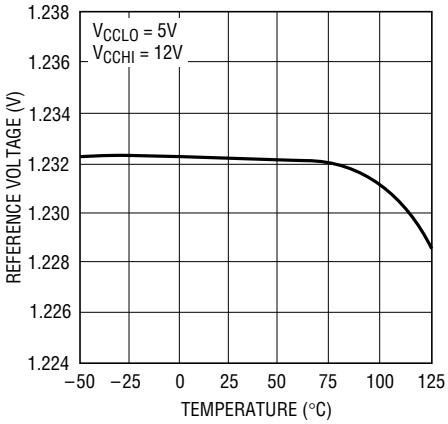
Note 2: All currents into device pins are positive; all currents out of device pins are negative. All voltages are reference to ground unless otherwise specified.

Note 3: After power-on reset, the V_{OUTLO} and V_{OUTHI} have to drop below the V_{TRIP} point before the charge pump is restarted.

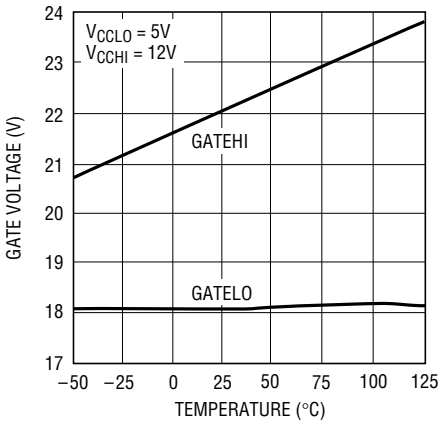
Note 4: After power-on reset, the V_{OUTLO} has to drop below the V_{TRIP} point before the charge pump is restarted.

TYPICAL PERFORMANCE CHARACTERISTICS

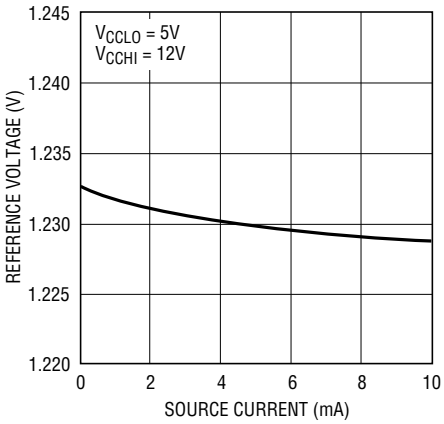
Reference Voltage vs Temperature



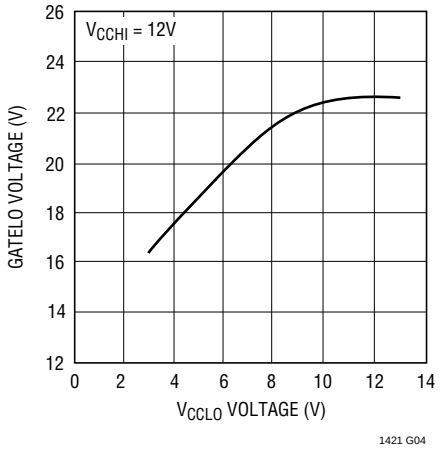
Gate Voltage vs Temperature



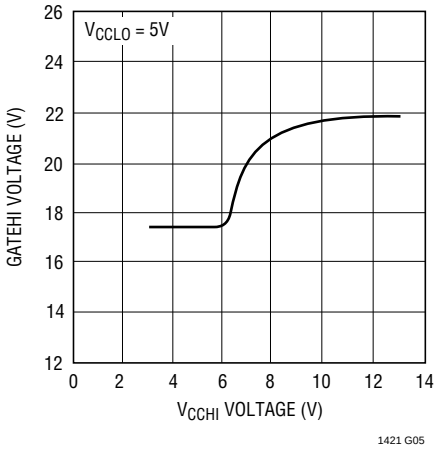
Reference Voltage vs Source Current



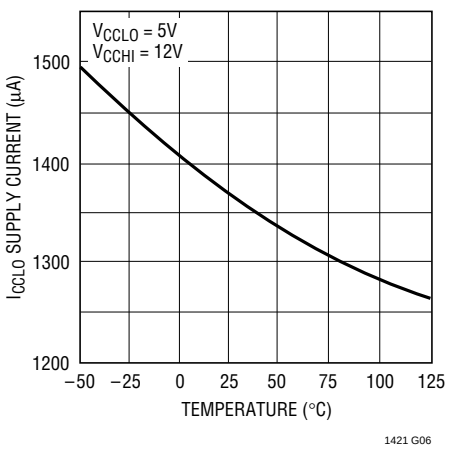
GATELO Voltage vs V_{CCLO} Voltage



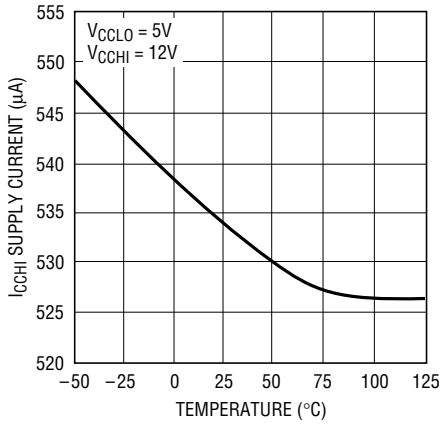
GATEHI Voltage vs V_{CCHI} Voltage



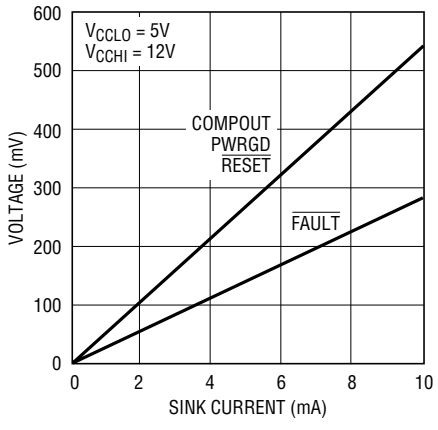
I_{CCLO} Supply Current vs Temperature



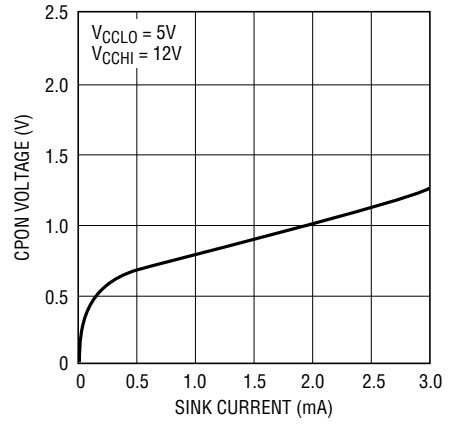
I_{CCHI} Supply Current vs Temperature



V_{OL} vs I_{SINK}

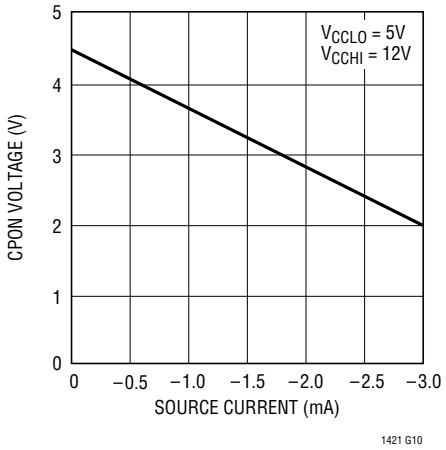


CPON Voltage vs Sink Current (Charge Pump Off)

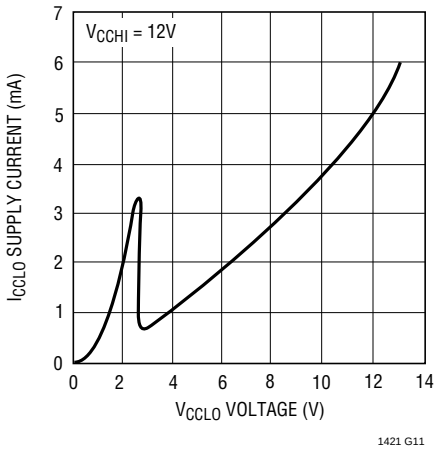


TYPICAL PERFORMANCE CHARACTERISTICS

CPON Voltage vs Source Current (Charge Pump On)



I_{CCLO} Supply Current vs V_{CCLO} Voltage



PIN FUNCTIONS

$\overline{CON1}$ (Pin 1): TTL Level Input with a Pull-Up to V_{CCLO}. Together with $\overline{CON2}$, it is used to indicate board connection. The pin must be tied to ground on the host side of the connector. When using staggered connector pins, $\overline{CON1}$ and $\overline{CON2}$ must be the shortest and must be placed at opposite corners of the connector. Board insertion is assumed after $\overline{CON1}$ and $\overline{CON2}$ are both held low for 20ms after power-up.

$\overline{CON2}$ (Pin 2): TTL Level Input with a Pull-Up to V_{CCLO}. Together with $\overline{CON1}$ it is used to indicate board connection.

$\overline{POR}$ (Pin 3): TTL Level Input with a Pull-Up to V_{CCLO}. When the pin is pulled low for at least 20ms, a hard reset is generated. Both V_{OUTLO} and V_{OUTHI} will turn off at a controlled rate. A power-up sequence will not start until the $\overline{POR}$ pin is pulled high. If $\overline{POR}$ is pulled high before V_{OUTLO} and V_{OUTHI} are fully discharged, a power-up sequence will not begin until the voltage at V_{OUTLO} and V_{OUTHI} are below V_{TRIP}. The electronic circuit breaker will be reset by pulling $\overline{POR}$ low.

$\overline{FAULT}$ (Pin 4): Open Drain Output to GND with a Weak Pull-Up to V_{CCLO}. The pin is pulled low when an overcurrent fault is detected at V_{OUTLO} or V_{OUTHI}.

DISABLE (Pin 5): CMOS Output. The signal is used to disable the board's data bus during insertion or removal.

PWRGD (Pin 6): Open Drain Output to GND with a Weak Pull-Up to V_{CCLO}. The pin is pulled low immediately after V_{OUTLO} falls below its reset threshold voltage. The pin is pulled high immediately after V_{OUTLO} rises above its reset threshold voltage.

$\overline{RESET}$ (Pin 7): Open Drain Output to GND with a Weak Pull-Up to V_{CCLO}. The pin is pulled low when a reset condition is detected. A reset will be generated when any of the following conditions are met: Either $\overline{CON1}$ or $\overline{CON2}$ is high, $\overline{POR}$ is pulled low, V_{CCLO} or V_{CCHI} are below their respective undervoltage lockout thresholds, PWRGD goes low or an overcurrent fault is detected at V_{OUTLO} or V_{OUTHI}. $\overline{RESET}$ will go high 200ms after PWRGD goes high. On power failure, $\overline{RESET}$ will go low 32µs after PWRGD goes low.

REF (Pin 8): The Reference Voltage Output. V_{OUT} = 1.232V ±1%. The reference can source up to 5mA of current. A 1µF bypass capacitor is recommended.

CPON (Pin 9): CMOS Output That Can Be Pulled Below Ground. CPON is pulled high when the internal charge pumps for GATELO and GATEHI are turned on. CPON is pulled low when the charge pumps are turned off. The pin can be used to control an external MOSFET for a –5V to –12V supply.

PIN FUNCTIONS

RAMP (Pin 10): Analog Power-Up Ramp Control Pin. By connecting an external capacitor between the RAMP and GATEHI, a positive linear voltage ramp on GATEHI and GATELO is generated on power-up with a slope equal to $20\mu A/C_{RAMP}$.

FB (Pin 11): Analog Feedback Input. FB is used to set the reset threshold voltage on V_{CCLO}. For a 5V supply leave FB floating. For a 3.3V supply, short FB to V_{CCLO}.

GND (Pin 12): Ground

$COMP^+$ (Pin 13): Noninverting Comparator Input.

$COMP^-$ (Pin 14): Inverting Comparator Input.

COMPOUT (Pin 15): Open Drain Comparator Output.

V_{OUTHI} (Pin 16): High Supply Voltage Output. This must be the higher of the two supply voltage outputs.

GATEHI (Pin 17): The High Side Gate Drive for the High Supply N-Channel. An internal charge pump guarantees at least 6V of gate drive. The slope of the voltage rise at GATEHI is set by the external capacitor connected between GATEHI and RAMP. When the circuit breaker trips, GATEHI is immediately pulled to GND.

SETHI (Pin 18): The Circuit Breaker Set Pin for the High Supply. With a sense resistor placed in the supply path between V_{CCHI} and SETHI, the circuit breaker will trip when the voltage across the resistor exceeds 50mV for more than 20μs. To disable the circuit breaker, V_{CCHI} and SETHI should be shorted together.

V_{CCHI} (Pin 19): The Positive Supply Input. This must be the higher of the two input supply voltages. An undervoltage lockout circuit disables the chip until the voltage at V_{CCHI} is greater than 2.45V.

V_{OUTLO} (Pin 20): Low Supply Voltage Output. This must be the lower of the two supply voltage outputs.

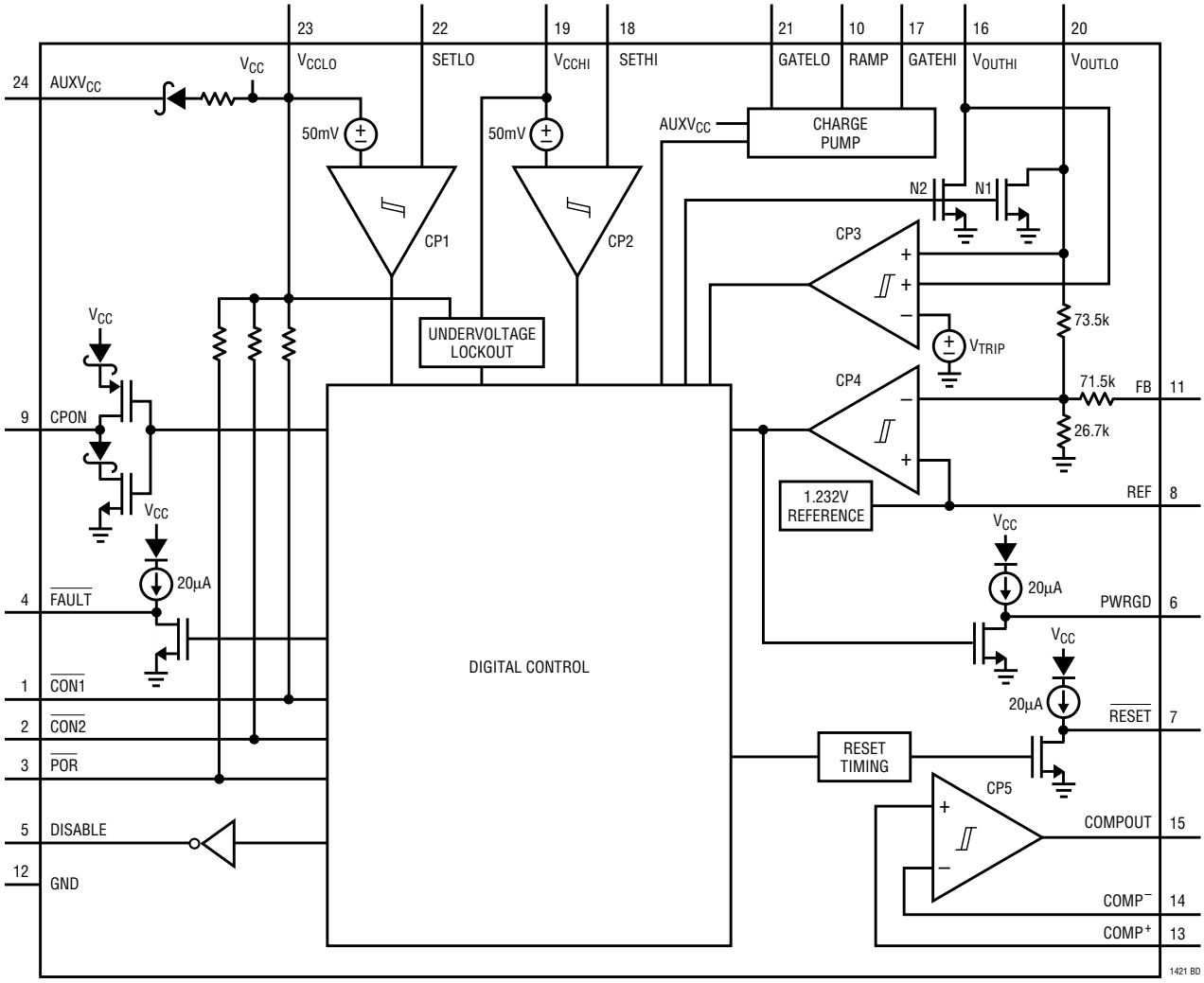
GATELO (Pin 21): The High Side Gate Drive for the Low Supply N-Channel Pass Transistor. An internal charge pump guarantees at least 10V of gate drive. The slope of the voltage rise at GATELO is set by the external capacitor connected between GATEHI and RAMP. When the circuit breaker trips GATELO is immediately pulled to GND.

SETLO (Pin 22): The Circuit Breaker Set Pin for the Low Supply. With a sense resistor placed in the supply path between V_{CCLO} and SETLO, the circuit breaker will trip when the voltage across the resistor exceeds 50mV for more than 20μs. To disable the circuit breaker, V_{CCLO} and SETLO should be shorted together.

V_{CCLO} (Pin 23): The Positive Supply Input. V_{CCLO} must be equal to or lower voltage than V_{CCHI}. An undervoltage lockout circuit disables the chip until the voltage at V_{CCLO} is greater than 2.45V.

$AUXV_{CC}$ (Pin 24): The supply input for the GATELO and GATEHI discharge circuitry. Connect a 1μF capacitor to ground. $AUXV_{CC}$ is powered from V_{CCLO} via an internal Schottky diode and series resistor.

BLOCK DIAGRAM



SWITCHING TIME WAVEFORMS

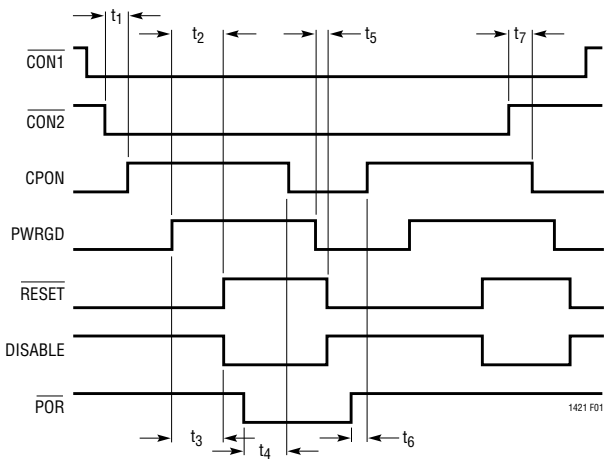


Figure 1. Nominal Operation Switching Waveforms

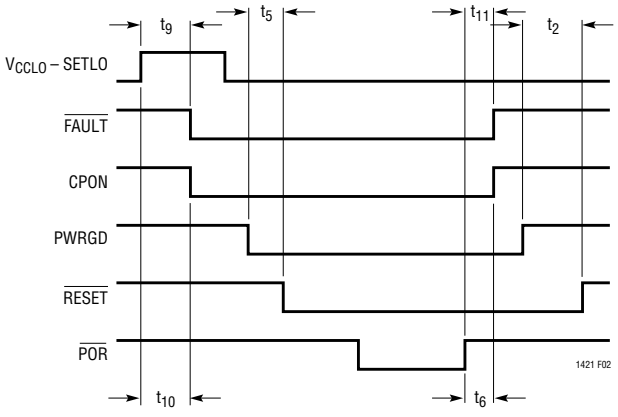


Figure 2. Fault Detection Switching

APPLICATIONS INFORMATION

Hot Circuit Insertion

When circuit boards are inserted into a live backplane, the supply bypass capacitors on the board can draw huge transient currents from the backplane power bus as they charge up. The transient currents can cause permanent damage to the connector pins and cause glitches on the system supply, causing other boards in the system to reset. At the same time, the system data bus can be disrupted when the board's data pins make or break connection.

The LTC1421 is designed to turn a board's supply voltages on and off in a controlled manner, allowing the board to be safely inserted or removed from a live backplane. The chip also provides a disable signal for the board's data bus buffer during insertion or removal and provides all the necessary supply supervisory functions for the board.

Power Supply Ramping

The power supplies on a board are controlled by placing external N-channel pass transistors in the power path (Figure 3). R1 and R2 provide current fault detection. By ramping the gate of the pass transistor up at a controlled rate, the transient surge current ($I = C \bullet dV/dt$) drawn from the main backplane supply can be limited to a safe value when the board makes connection.

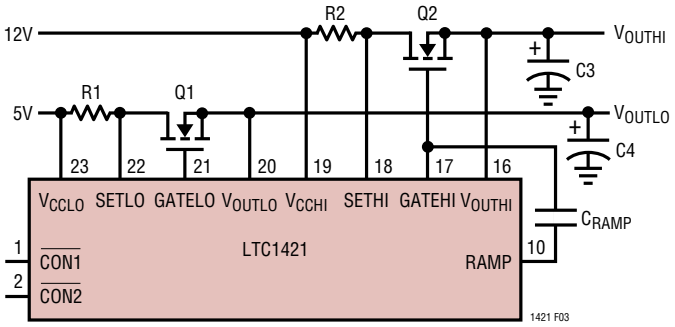


Figure 3: Supply Control Circuitry

When power is first applied to the chip, the gates of both N-channels, GATELO and GATEHI are pulled low. After the connection sense pins, $\overline{CON1}$ and $\overline{CON2}$ are both held low for at least 20ms, a 20µA reference current is connected from the RAMP pin to GND. The voltage at GATEHI begins to rise with a slope equal to $20\mu A/C_{RAMP}$ (Figure 4), where C_{RAMP} is an external capacitor connected between the RAMP and GATEHI pins. The voltage at the GATELO pin is clamped one Schottky diode drop below GATEHI.

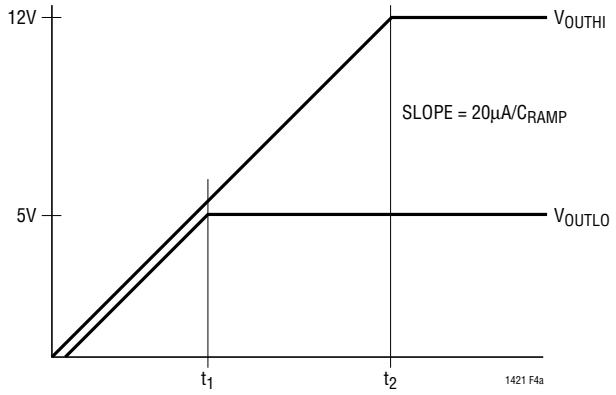


Figure 4. Supplies Turning On

The ramp time for each supply is equal to: $t = (V_{CC})(C_{RAMP})/20\mu A$. During power down the gates are actively pulled down by two internal NFETs.

A negative supply voltage can be controlled using the CPON pin as shown in Figure 5.

When the board makes connection, the transistor Q3 is turned off because it's gate is pulled low to –12V by R4. CPON is also pulled to –12V. When the charge pump is turned on, CPON is pulled to V_{CCLO} and the gate of Q3 will ramp up with a time constant determined by R4, R5 and C2. When the charge pump is turned off, CPON goes into a high impedance state, the gate of Q3 is discharged to V_{EE} with a time constant determined by R4 and C2, and Q3 turns off.

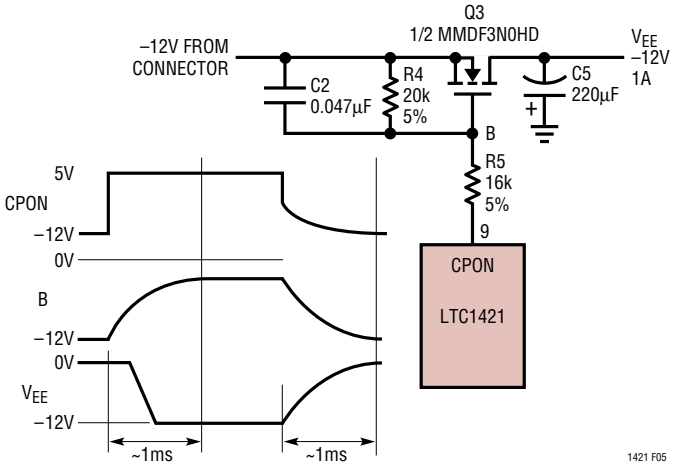


Figure 5. Negative Supply Control

APPLICATIONS INFORMATION

PWRGD and $\overline{\text{RESET}}$

The LTC1421 uses a 1.232V bandgap reference, internal resistive divider and a precision voltage comparator to monitor V_{OUTLO} (Figure 6).

The reset threshold voltage for V_{OUTLO} is determined by the FB pin connection as summarized in Table 1.

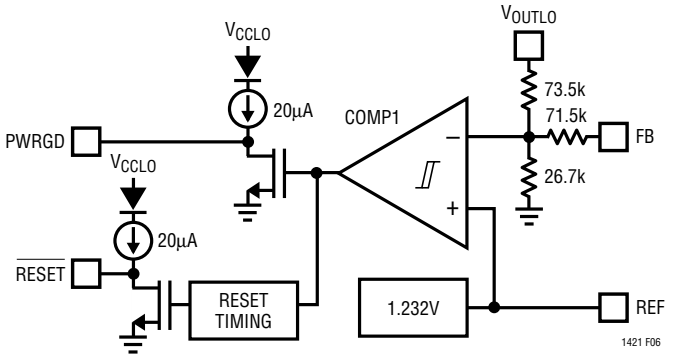


Figure 6. Supply Monitor Block Diagram

Table 1

FEEDBACK PIN	V_{OUTLO} RESET VOLTAGE
Floating	4.65V
V_{OUTLO}	2.90V
GND	5.88V

When the V_{OUTLO} voltage rises above its reset threshold voltage, the comparator output goes low, and PWRGD is immediately pulled high to V_{CCLO} by a weak pull-up current source or external resistor (Figure 7, time points 1 and 4). After a 200ms delay, $\overline{\text{RESET}}$ is pulled high. The weak pull-up current source to V_{CCLO} on PWRGD and $\overline{\text{RESET}}$ have a series diode so the pins can be pulled above V_{CCLO} by an external pull-up resistor without forcing current back into V_{CCLO}.

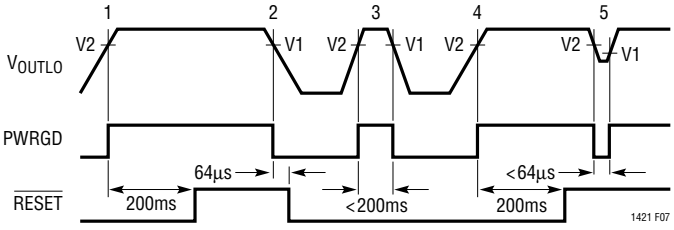


Figure 7. Power Monitor Waveforms

When V_{OUTLO} drops below its reset threshold, the comparator output goes high, and PWRGD is immediately pulled low (time point 2). After a 32µs delay, $\overline{\text{RESET}}$ is pulled low. The $\overline{\text{RESET}}$ delay allows the PWRGD signal to be used as an early warning that a reset is about to occur. If the PWRGD signal is used as a interrupt input to a microprocessor, a short power-down routine can be run before the reset occurs.

If V_{OUTLO} rises above the reset threshold for less than 200ms, the PWRGD output will trip, but the $\overline{\text{RESET}}$ output is not affected (time point 3). If V_{OUTLO} drops below the reset threshold for less than 32µs, the PWRGD output will trip, but again the $\overline{\text{RESET}}$ output will not be affected (time point 5).

Voltage Comparator

The uncommitted voltage comparator (COMP2) can be used to monitor output voltages other than V_{OUTLO}. Figure 8a shows how the comparator can be used to monitor a 12V supply (V_{OUTHI}), while the 5V supply (V_{OUTLO}) generates a reset when it dips below 4.65V. When the 12V supply drops below 10.8V, COMPOUT will pull low. The FB pin is left floating.

Figure 8b shows how the comparator can be used to monitor the 5V supply (V_{OUTHI}) while the 3.3V supply (V_{OUTLO}) generates a reset when it dips below 2.9V. When the 5V supply drops below 4.65V, COMPOUT will pull low. The FB pin is tied to V_{OUTLO}.

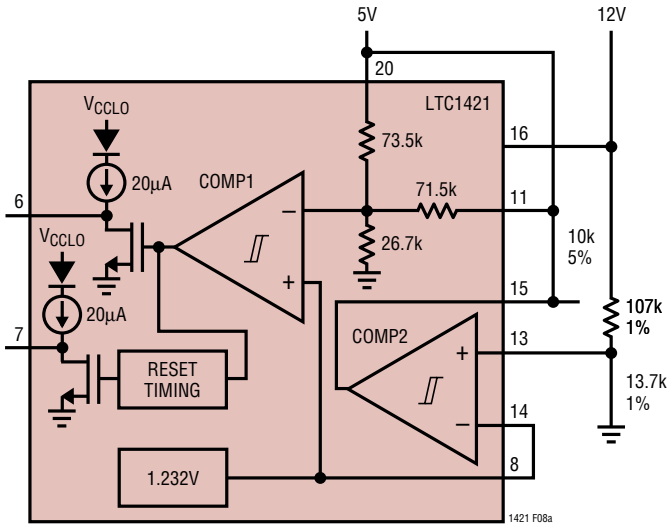


Figure 8a. Monitor 12V, Reset 5V at 4.65V

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Figure 8c shows how the comparator can be used to generate a reset when the 12V supply (V_{OUTHI}) drops below 10.8V. The 5V supply (V_{OUTLO}) also generates a reset when it dips below 4.65V. When the 12V supply drops below 10.8V, COMPOUT will pull the FB pin low setting the internal threshold voltage for comparator 1 to 5.88V. Since V_{OUTLO} is less than 5.88V, PWRGD immediately goes low and a reset is generated 200ms later.

Figure 8d shows how the comparator can be used to override the internal reset voltage for a 5V supply on V_{OUTLO}.

A 5k resistor is tied from the FB pin to V_{OUTLO}, setting the internal threshold to about 2.9V. The new reset threshold voltage is set by the external resistive divider connected to COMP2. When V_{OUTLO} drops below the new threshold, COMPOUT pulls FB to ground, changing the internal threshold at COMP1 to 5.88V and generating a reset.

Finally, the comparator may be used to monitor a negative supply as shown in Figure 8e. The external resistor divider

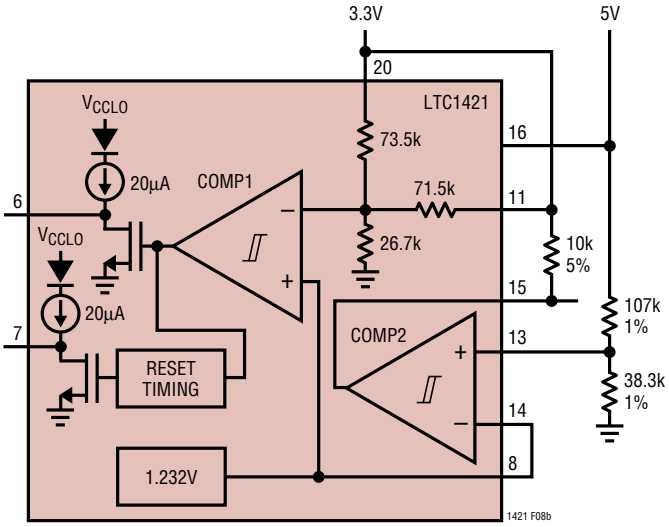


Figure 8b. Monitor 5V, Reset 3.3V at 2.9V

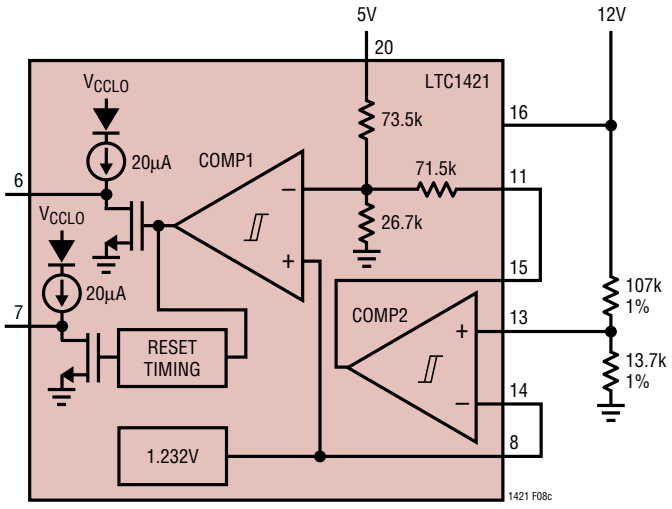


Figure 8c. Reset 12V at 10.8V, Reset 5V at 4.65V

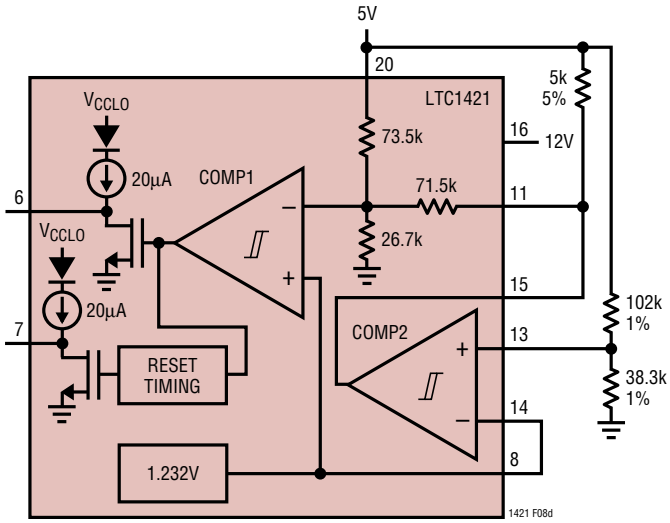


Figure 8d. Reset 5V at 4.5V

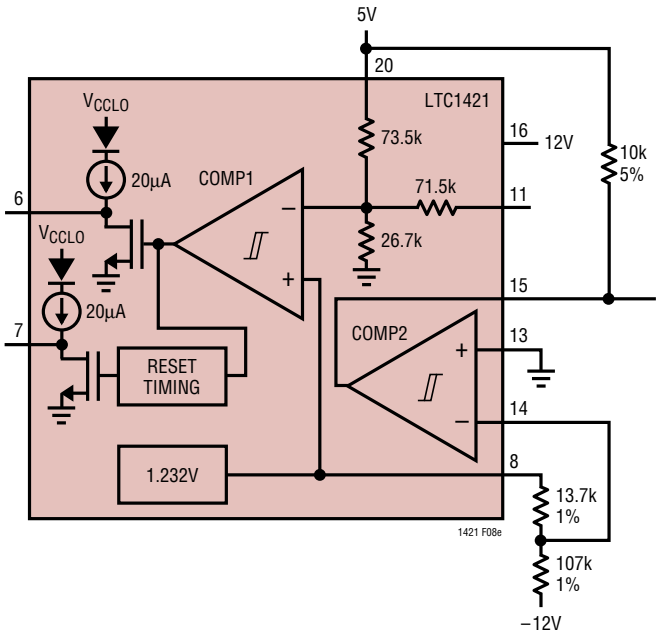


Figure 8e. Monitor –12V at –10.8V, Reset 5V at 4.65V

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is connected between REF (Pin 8) and the negative supply and the trip point of Comparator 2 set to GND.

Soft Reset Generation

A soft reset that doesn't cycle the supply voltage can be generated externally using Pin 11 (FB) as shown in Figure 9. For a 5V supply the FB pin is left floating to set the internal supply monitor trip voltage to 4.65V. However, if the FB pin is pulled to ground for more than 64µs via a push button or open-collector logic gate, the internal trip point will go to 5.88V and the $\overline{\text{RESET}}$ pin will pull low. $\overline{\text{RESET}}$ will remain low for 200ms after the FB pin is released. The $\overline{\text{RESET}}$ signal will also be pulled low when the voltage at the V_{OUTLO} pin dips below 4.65V for more than 32µs. When using a 3.3V supply, a 1k resistor must be connected from the FB pin to V_{CCLO} to set the internal trip point to 2.90V.

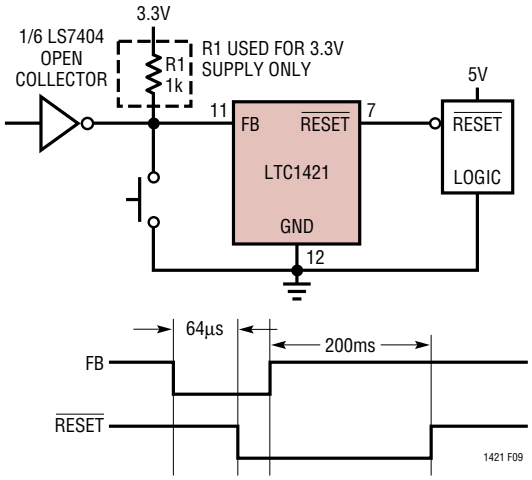


Figure 9. Generating a Soft Reset

Undervoltage Lockout

On power-up, an undervoltage lockout circuit prevents the GATELO and GATEHI charge pumps from turning on until V_{CCLO} and V_{CCHI} have both exceeded 2.45V.

Electronic Circuit Breaker

The LTC1421 features an electronic circuit breaker function that protects against short circuits or excessive currents on the supplies. By placing a sense resistor between the supply input and set pin of either supply, the circuit breaker will be tripped whenever the voltage across the sense resistor is greater than 50mV for more than 20µs. When the circuit breaker trips, both N-channel MOSFETs are quickly turned off, $\overline{\text{FAULT}}$ and PWRGD go low and $\overline{\text{RESET}}$ is pulled low 32µs later. $\overline{\text{FAULT}}$ can be connected to a LED or a logic signal back to the host to indicate a faulty board. The chip will remain in the tripped state until a power-on reset is generated, or the power on V_{CCHI} and V_{CCLO} is cycled. If the circuit breaker feature is not used, short V_{CCLO} to SETLO and V_{CCHI} to SETHI.

If more than 20µs of response time is needed to reject supply noise, an external resistor and capacitor can be added to the sense circuit as shown in Figure 10.

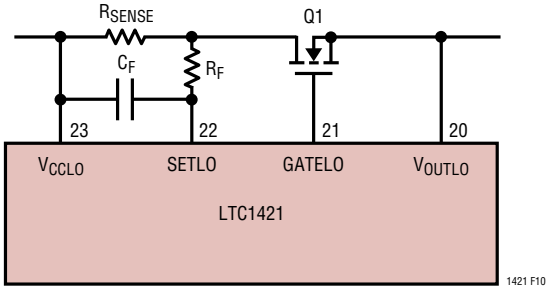


Figure 10. Short-Circuit Protection Circuit

Auxiliary V_{CC}

When a short circuit occurs on the board, it is possible to draw enough current to cause the backplane supply voltage to collapse. If the input supply voltage collapses to a low enough voltage and the LTC1421 gate drive circuitry is unable to shut off the N-channel pass transistors, the system might freeze up in a permanent short condition.

To prevent this from occurring, the gate discharge circuitry inside the LTC1421 is powered from $AUXV_{CC}$, which is in turn powered from V_{CCLO} through an internal Schottky diode and current limiting resistor (Figure 11).

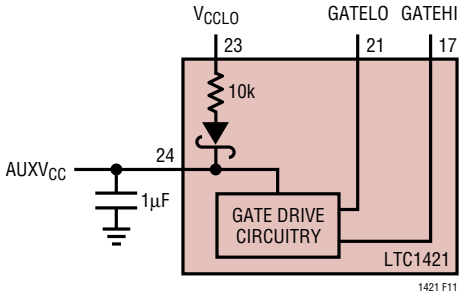


Figure 11. $AUXV_{CC}$ Circuitry

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When V_{CCLO} collapses, there is enough energy stored on the 1µF capacitor connected to $AUXV_{CC}$ to keep the gate discharge circuitry alive long enough to fully turn off the external N-channels.

Power N-Channel Selection

The $R_{DS(ON)}$ of the external pass transistor must be low enough so that the voltage drop across it is about 200mV or less at full current. If the $R_{DS(ON)}$ is too high, the voltage drop across the transistor might cause the output voltage to trip the reset circuit. Table 2 lists the transistors that are recommended for use with the LTC1421.

Table 2. N-Channel Selection Guide

CURRENT LEVEL (A)	PART NUMBER	MANUFACTURER	DESCRIPTION
0 to 1	MMDF2N02E	Motorola	Dual N-Channel SO-8 $R_{DS(ON)}$ = 0.1Ω
1 to 2	MMDF3NO2HD	Motorola	Dual N-Channel SO-8 $R_{DS(ON)}$ = 0.09Ω
2 to 5	MTB30N06	Motorola	Single 30A N-Channel DD Pak $R_{DS(ON)}$ = 0.05Ω
5 to 10	MTB50N06E	Motorola	Single N-Channel DD Pak $R_{DS(ON)}$ = 0.025Ω
10 to 20	MTB75N05HD	Motorola	Single N-Channel DD Pak $R_{DS(ON)}$ = 0.0095Ω

Data Bus

When a board is inserted or removed from the host, care must be given to prevent the system data bus from being corrupted when the data pins make or break contact. One problem is that the fully discharged input or output capacitance of the logic gates on the board will draw an inrush current when the data bus pins first make contact. The inrush current can temporarily corrupt the data bus, but usually will not cause long term damage. The problem can be minimized by insuring the input or output data bus capacitance is kept as small as possible.

The second, and more serious problem involves the diodes to V_{CC} at the input and output of most logic families (Figure 12).

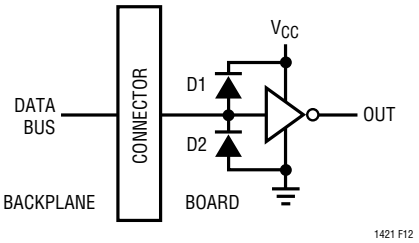


Figure 12. Typical Logic Gate Loading the Data Bus

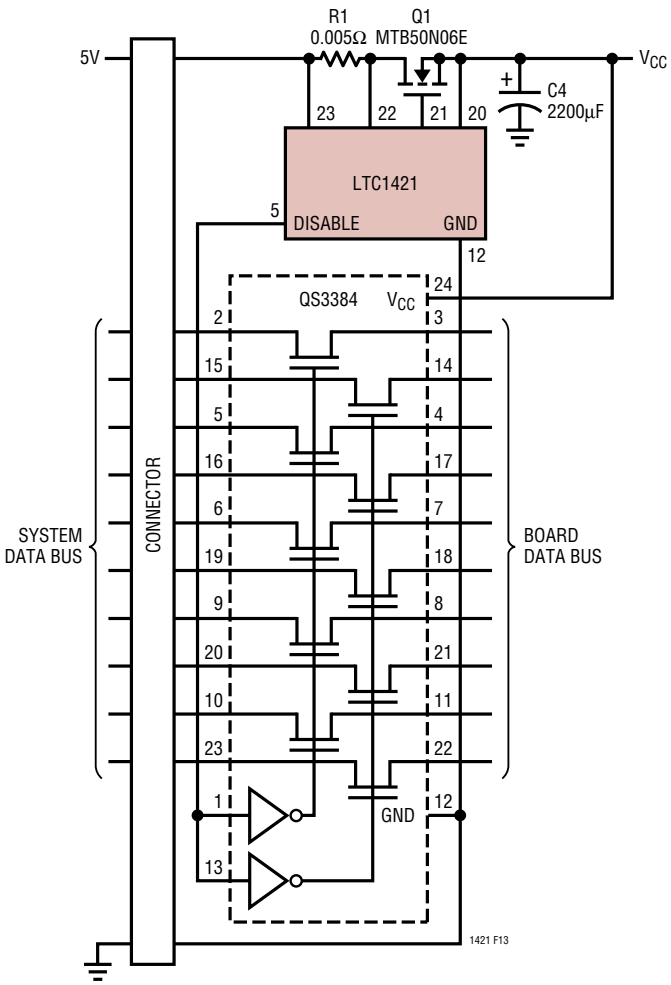


Figure 13: Buffering the Data Bus

With the board initially unpowered, the V_{CC} input to the logic gate is at ground potential. When the data bus pins make contact, the bus line is clamped to ground through the input diode D1 to V_{CC}. Large amounts of current can flow through the diode and cause the logic gate to latch up and destroy itself when the power is finally applied. This

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can usually be prevented by using logic that does not include the clamping diodes such as the QSI 74FCTT family from Quality Semiconductor, or by using a data bus switch such as the 10-bit QS3384 QuickSwitch also from Quality Semiconductor (Tel: 408-450-8000). The QuickSwitch bus switch contains an N-channel placed in series with the data bus. The switch is turned off when the board is inserted and then enabled after the power is stable. The switch inputs and outputs do not have a parasitic diode back to V_{CC} and have very low capacitance.

The LTC1421 is designed to work directly with the QuickSwitch bus switch as shown in Figure 13.

The DISABLE signal is connected to the enable pins of the QS3384, and each switch is placed in series with a data bus signal. When the board is inserted, the DISABLE signal is pulled high, turning off the switches. After the board supply voltage ramps up and $\overline{RESET}$ goes high, DISABLE will pull low enabling the switches.

Board Insertion Timing

When the board is inserted, GND pin makes contact first, followed by V_{CCHI} and V_{CCLO} (Figure 14, time point 1). DISABLE is immediately pulled high, so the data bus switch is disabled. At the same time $\overline{CON1}$ and $\overline{CON2}$ make contact and are shorted to ground on the host side (time point 3). Since most boards need to be rocked back and forth to get them in place, there is a period of time when only one side of the connector is making contact. $\overline{CON1}$ and $\overline{CON2}$ should be located at opposite ends of the connector.

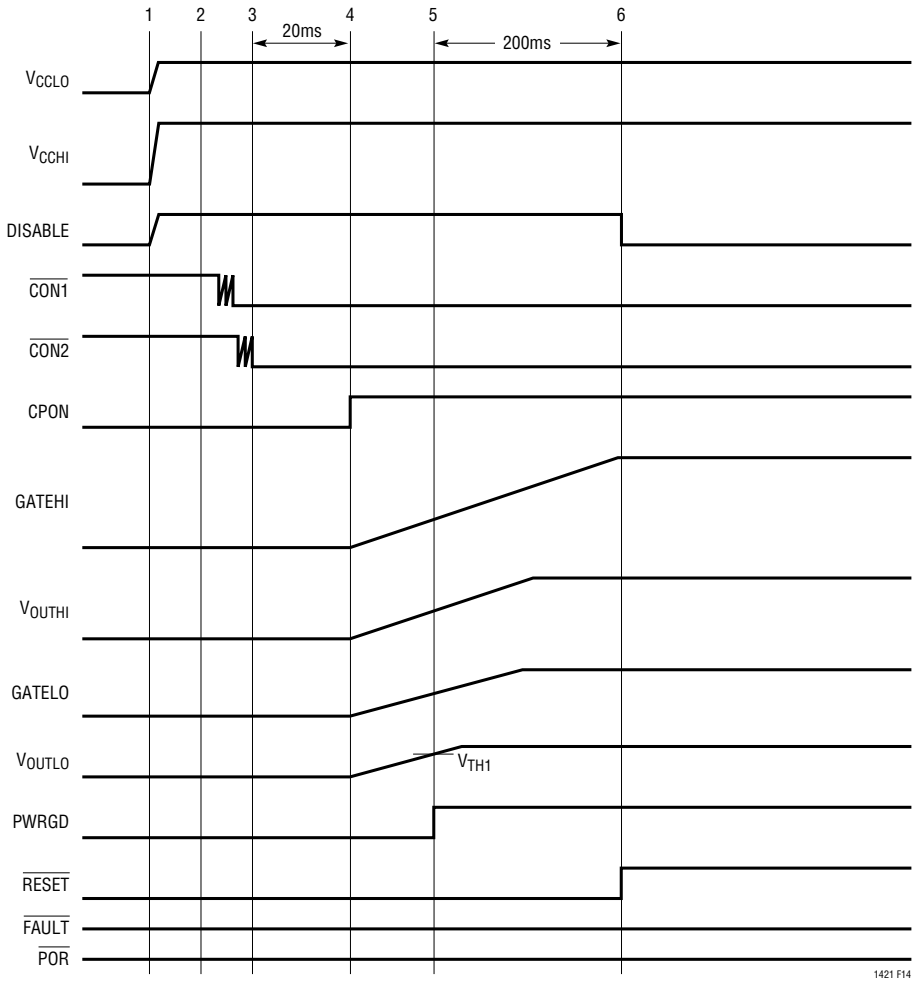


Figure 14. Board Insertion Timing

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When $\overline{CON1}$ and $\overline{CON2}$ are both forced to ground for more than 20ms, the LTC1421 assumes that the board is fully connected to the host and power-up can begin. When V_{CCLO} and V_{CCHI} exceed the 2.45V undervoltage lockout threshold, the 20µA current reference is connected from RAMP to GND, the charge pumps are turned on and CPON is forced high (time point 4). V_{OUTHI} and V_{OUTLO} begin to ramp up. When V_{OUTLO} exceeds the reset threshold voltage, PWRGD will immediately be forced high (time point 5). After a 200ms delay, $\overline{RESET}$ will be pulled high and DISABLE will be pulled low, enabling the data bus (time point 6).

Ground Sense Comparator

When $\overline{POR}$ is pulled low for more than 20ms, GATELO and GATEHI are pulled to ground and V_{OUTLO} and V_{OUTHI} will be discharged. If $\overline{POR}$ is pulled back high while V_{OUTLO} and V_{OUTHI} are still ramping down, the discharge will continue. When they drop below the V_{TRIP} point, a power-up sequence will begin automatically. The trip point potential for LTC1421 is set at 0.1V and 2.5V for LTC1421-2.5.

In applications, where either V_{OUTLO} or V_{OUTHI} might be forced above 100mV before power-up, the LTC1421-2.5 should be used. This could occur when leakage through the body diode of the logic chips keeps V_{OUTLO} high or in the case where logic lines are precharged.

In other applications, where outputs need to drop to near ground potential before ramping up again to ensure proper initial state for the logic chips, the LTC1421 should be used.

Power-On Reset Timing

The $\overline{POR}$ input is used to completely cycle the power supplies on the board or to reset the electronic circuit breaker feature. The $\overline{POR}$ pin can be connected to a grounded push button, toggle switch or a logic signal from the host. When $\overline{POR}$ is pulled low for more than 20ms, a power-on reset sequence begins (Figure 15,

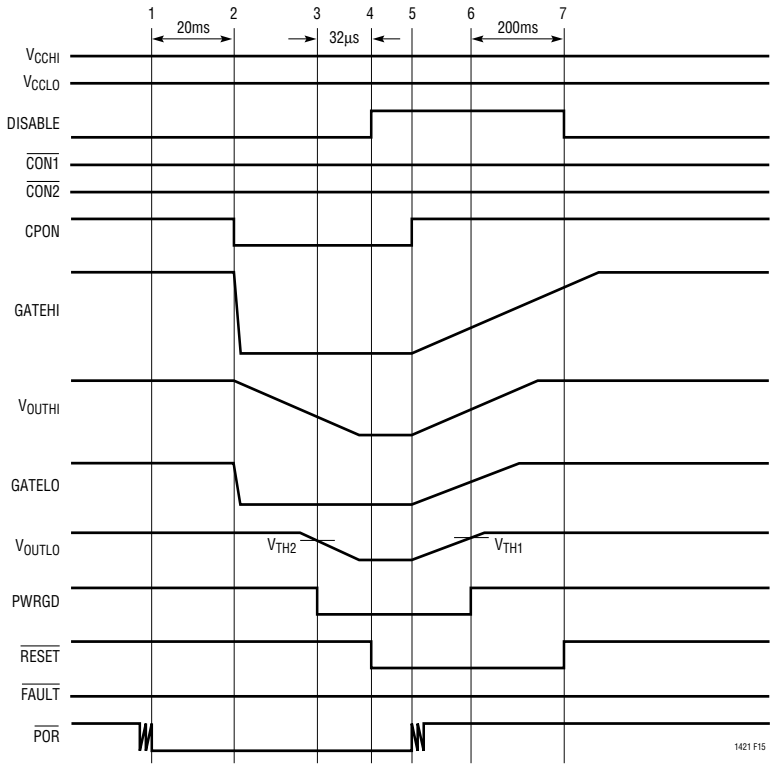


Figure 15. Power-On Reset Timing

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time point 2). Pulses less than 20ms on $\overline{POR}$ are ignored. CPON goes low. Both GATEHI and GATELO will be actively pulled down to GND. When V_{OUTLO} drops below its reset threshold voltage, PWRGD will immediately pull low (time point 3) followed by $\overline{RESET}$ and DISABLE 32µs later (time point 4). Both supplies will be discharged to ground and stay there until $\overline{POR}$ is pulled high.

The circuit breaker can be reset by pulling $\overline{POR}$ low. After $\overline{POR}$ is low for more than 20ms, the chip will immediately try to power up the supplies.

Circuit Breaker Timing

The waveforms for the circuit when a short occurs on either supply during board insertion are shown in Figure 16. Time points 1 to 4 are the same as the board insertion example, but at time point 5, a short circuit is detected on one of the supplies. The charge pumps are immediately turned off, the outputs V_{OUTHI} and V_{OUTLO} are actively pulled to GND and the CPON and $\overline{FAULT}$ pins are pulled low. At time point 6, the circuit breaker is reset by pulling $\overline{POR}$ low. After $\overline{POR}$ has been low for 20ms (time point 7), CPON and $\overline{FAULT}$ are pulled high, the 20µA reference current is connected to RAMP and the charge pumps are enabled. V_{OUTHI} and V_{OUTLO} ramp up at a controlled rate. When V_{OUTLO} has exceeded its reset threshold, the PWRGD signal is pulled high (time point 8). After a 200ms delay, $\overline{RESET}$ is pulled high and DISABLE goes low.

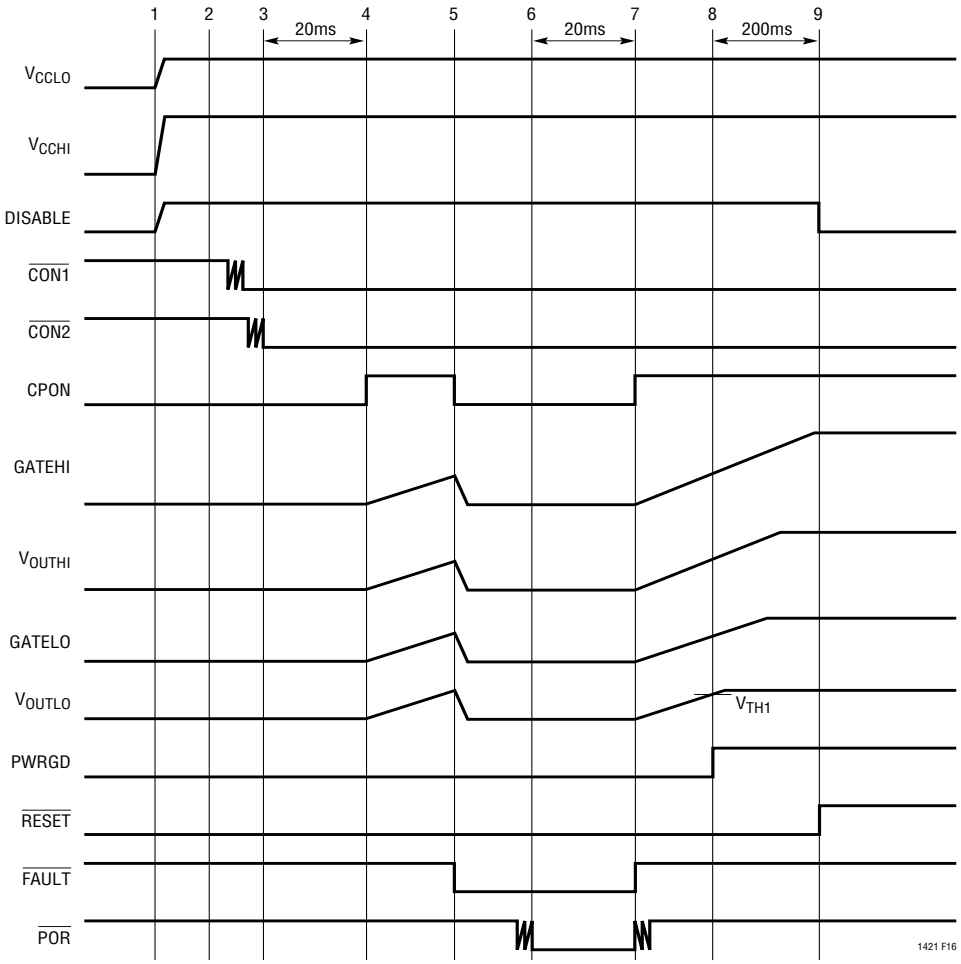


Figure 16. Circuit Breaker Timing

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Board Removal Timing

When the board is removed from the host, the sequence happens in reverse (Figure 17). Since $\overline{CON1}$ and $\overline{CON2}$ are the shortest pins, they break connection first and are internally pulled high (time point 1). The charge pumps are turned off, CPON is pulled low. V_{OUTLO} and V_{OUTHI} are actively pulled down. When V_{OUTLO} falls below its reset threshold (time point 2) PWRGD is pulled low. To allow time for power fail information to be stored in nonvolatile memory, the falling edge of $\overline{RESET}$ (time point 3) is delayed by 32µs from the falling edged of PWRGD.

Finally, the input supply pins V_{CCHI} and V_{CCLO} break contact (time point 4). If staggered pins are not used, the board may be powered down prior to removal by switching the $\overline{POR}$ pin to ground with a toggle switch.

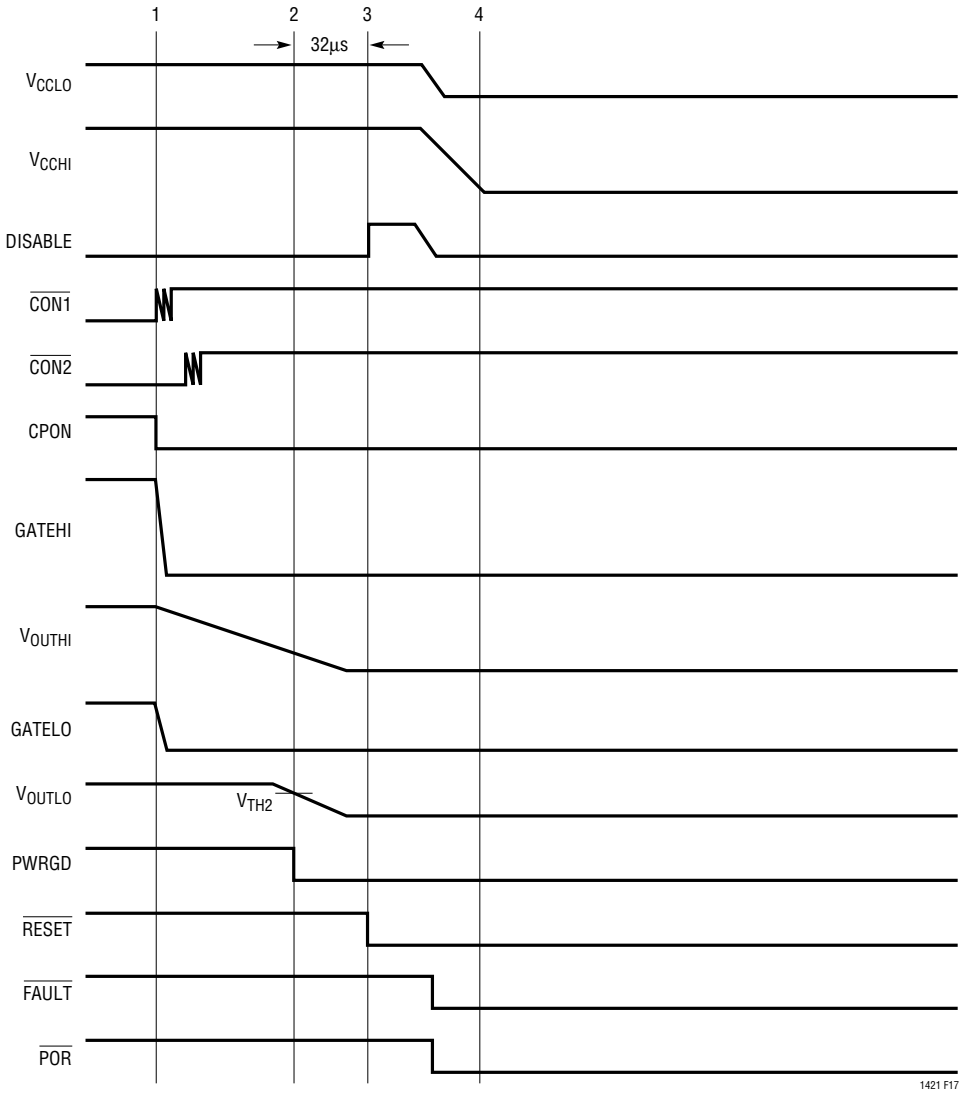


Figure 17. Board Removal Timing

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5V Only Applications

The LTC1421 may be used in 5V only applications as shown in Figure 18. A soft reset can be generated from the backplane via an open-collector inverter driving the FB (Pin 11) or by a push button to ground. A hard power reset is generated from the backplane via an open-collector inverter driving the $\overline{POR}$ (Pin 3). A hard reset cycles the power on the board or resets the electronic circuit breaker. The comparator is used to monitor the board supply voltage and will pull the $\overline{POWERGOOD}$ signal low as long as the supply remains above 4.65V. Note that a soft reset will not affect the $\overline{POWERGOOD}$ signal. The $\overline{FAULT}$ signal is also monitored to determine that the circuit breaker has tripped.

–48V and 24V Applications

The LTC1421 may be used in –48V applications as shown in Figure 19. The LTC1421 provides the hot insertion protection, while the 5V supply is generated by a power

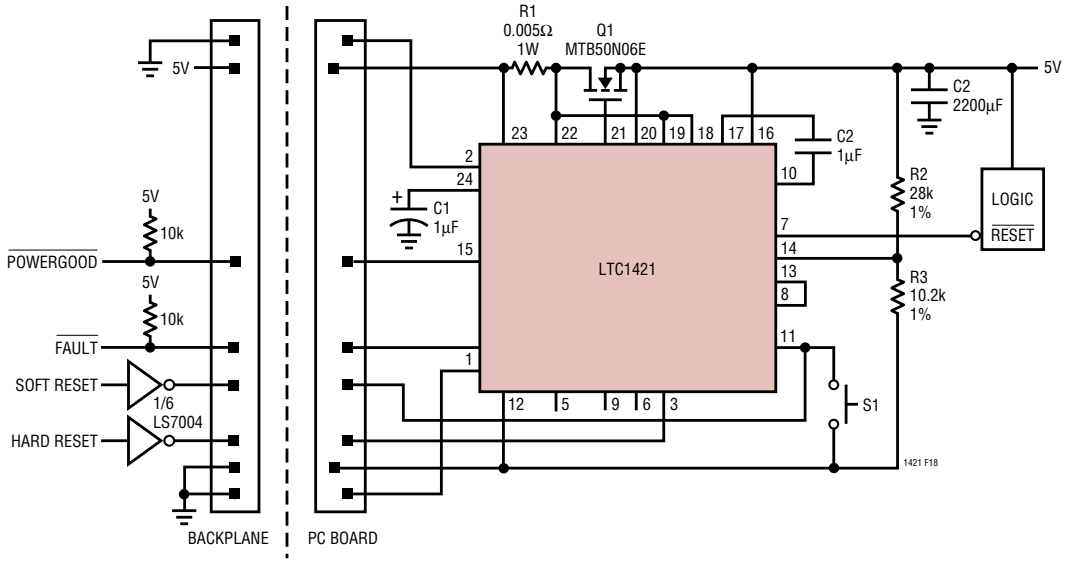


Figure 18. 5V Only Application with Soft Reset

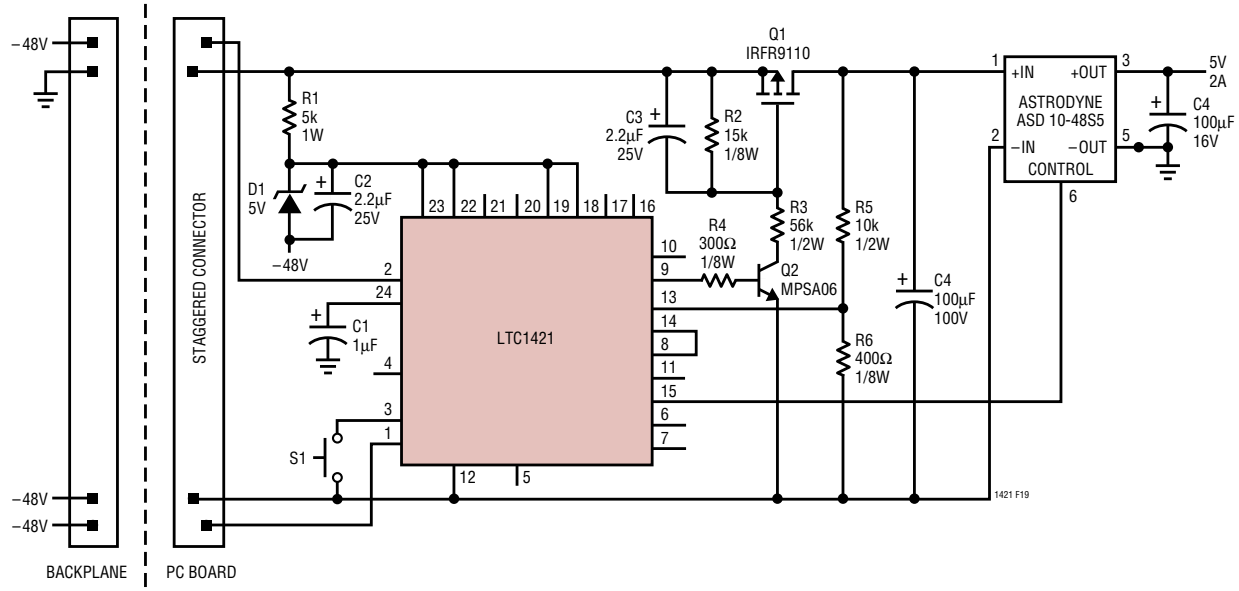


Figure 19. –48V to 5V Hot Swappable Supply

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module. The ground pin for the LTC1421 is connected to –48V; Zener diode D1 and resistor R1 provide the positive supply for the chip. Bypass capacitor C4 is protected against inrush current by P-channel Q1. When the board is inserted into the backplane, transistor Q1 is turned off by resistor R2. When the connection sense pins, $\overline{CON1}$ and $\overline{CON2}$ have been connected to –48V for more than 20ms, CPON pulls high turning on Q2 and the gate of Q1 starts to pull low with a time constant determined by R2, R3 and C3. At the same time, the voltage at the input to the power module starts to ramp up. When the voltage across the inputs to the power module reaches the comparator trip level set by R5 and R6, in this case –32V, the comparator output pulls high and turns on the 5V supply.

A cheaper solution is shown in Figure 20 using the LT®1170HV switcher. Again P-channel transistor Q1 protects the bypass capacitors against inrush current and resistors R5 and R6 set the comparator trip voltage. The LT1170HV is turned on via the V_C pin. Resistors R11, R14 and transistor Q4 provide a monitoring path for the RESET signal which is level shifted up to 5V through an optoisolator.

The P-channel power FET is being replaced by an N-channel FET in Figure 21 for the –48V application. Again, Zener Diode D1 and resistor R1 provide the positive supply for the chip. Capacitor C1 is to insure Q1 stays off when the board is being hot inserted into the backplane. The resistor divider R1 and R2, along with the internal comparator, perform the undervoltage lock out function. Q1 would only be turned on when the input supply voltage is lower than –42V. The power module would then be turned on by the optoisolator, 4N25, when the module's input voltage reaches 47V.

Figure 22 shows how to use the LTC1421 with a 24V supply and a LT1074CT step-down switcher. Resistors R5 and R6 set the turn-on threshold to 22V. All of the supervisory signals can be used without level shifting.

Figure 23 shows how to use the LTC1421 with a 5V supply and an LTC1430CS8 synchronous step-down switching regulator to generate 3.3V output at up to 10A for microprocessors. Resistors R4, R8 and R9 set the turn-on voltage at 4.8V and the turn-off at 4.25V. Pushbutton switch S1 provides users a way to reset the output while S2 is used to soft-reset the microprocessor only.

Figure 24 shows how to use the LTC1421 with a 5V supply and a –48V supply that is used to generate a ±12V supply using a supply module. Resistors R3 and R4 are used to monitor the input voltage to the supply module. The module is prevented from turning on via the optoisolator until the input voltage reaches –36V. Zener diode D2 prevents the CPON pin of the LTC1421 from being damaged by excessive voltage.

Figure 25 shows how to use the LTC1421 to do overvoltage protection. Resistors R3 and R4 set the trip point at 7V. When the input supply voltage rises above 7V, Q2 is turned on and Q1 turned off while Q3 helps to discharge the output voltage.

Figure 26 shows how to use the LTC1421 to control both the power-up and power-down sequence of the outputs. The 5V output would be powered up first followed by the 3V output. At power-down sequence, the 3V output would go down first followed by the 5V supply.

Figure 27 shows how to use the LTC1421 to switch 3.3V, 5V, 12V and –12V supplies for PCI application. The ramp-up rate for 3.3V, 5V and 12V is determined by the ramp capacitor C2 while the –12V supply is controlled by R7 and C3. The internal comparator is being used to do the overcurrent protection for Q4 with the trip point set by resistors R6 and R8. The –12V supply does not have overcurrent protection. R10 is used to set the power good signal trip point at 10V. When the 12V output rises above 10V, the PCI controller gets a power good signal followed by $\overline{RESET}$ after 200ms.

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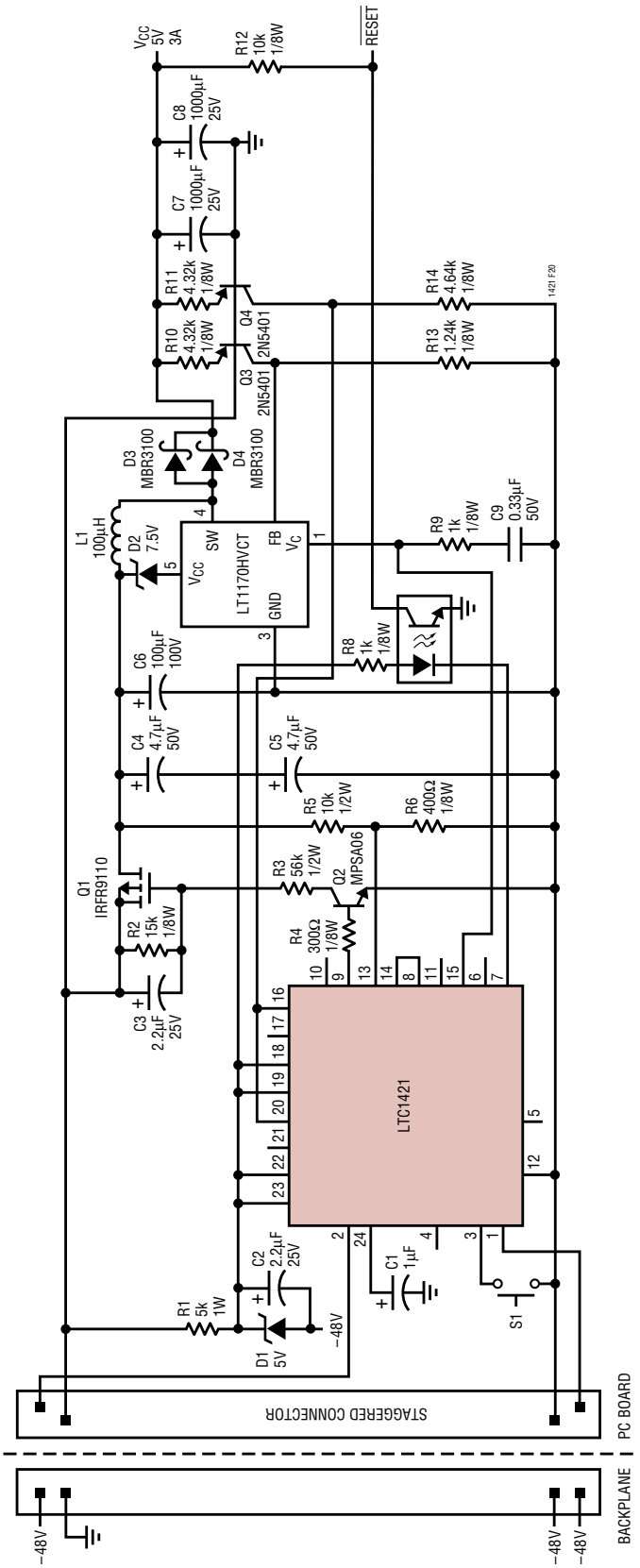


Figure 20. –48V to 5V Hot Swappable Supply Using the LT1170HVCT

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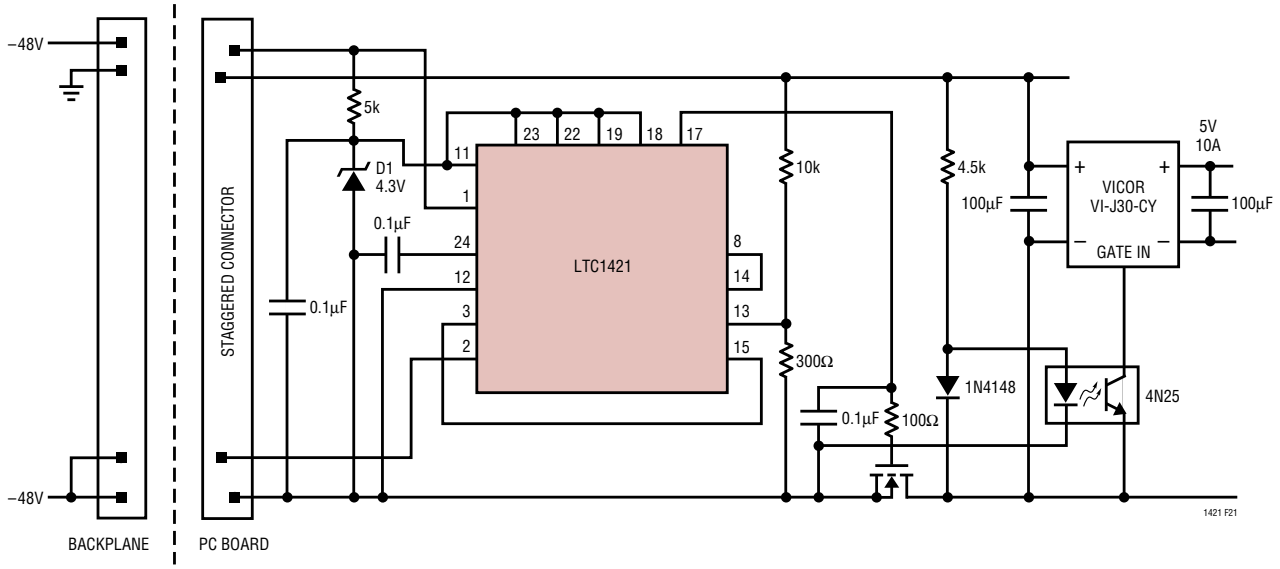


Figure 21. –48V to 5V Hot Swappable Supply

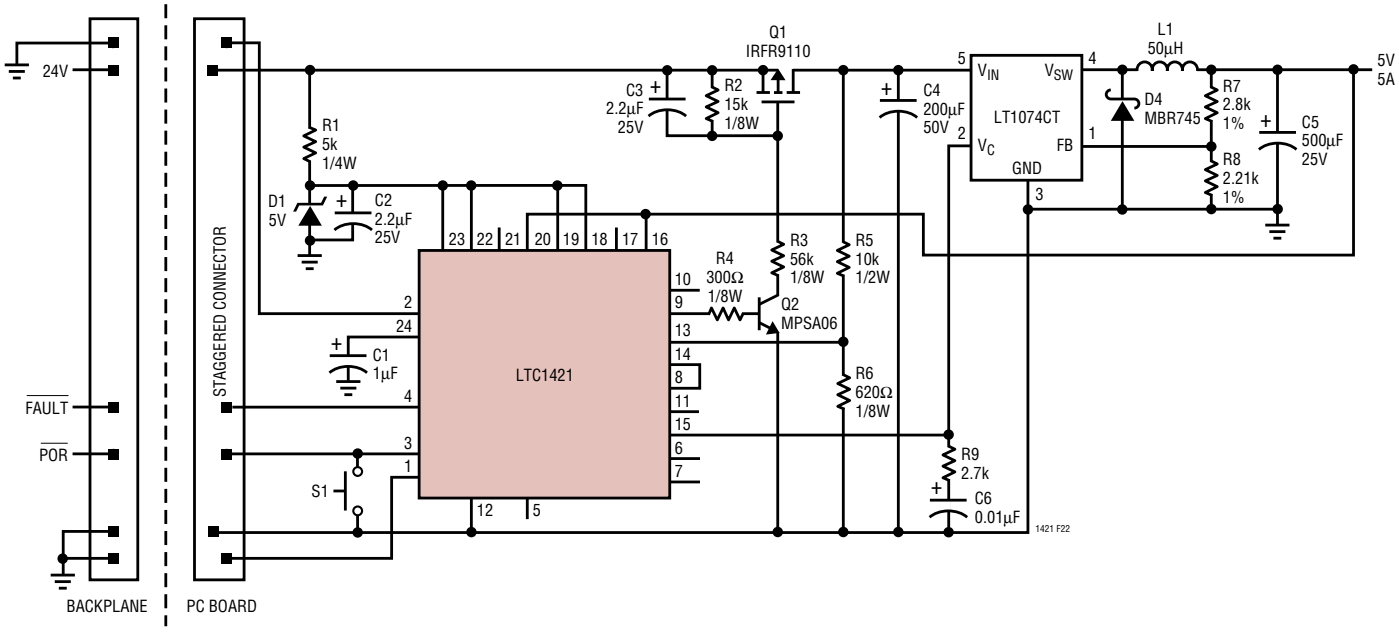


Figure 22. 24V to 5V Hot Swappable Supply Using the LT1074CT

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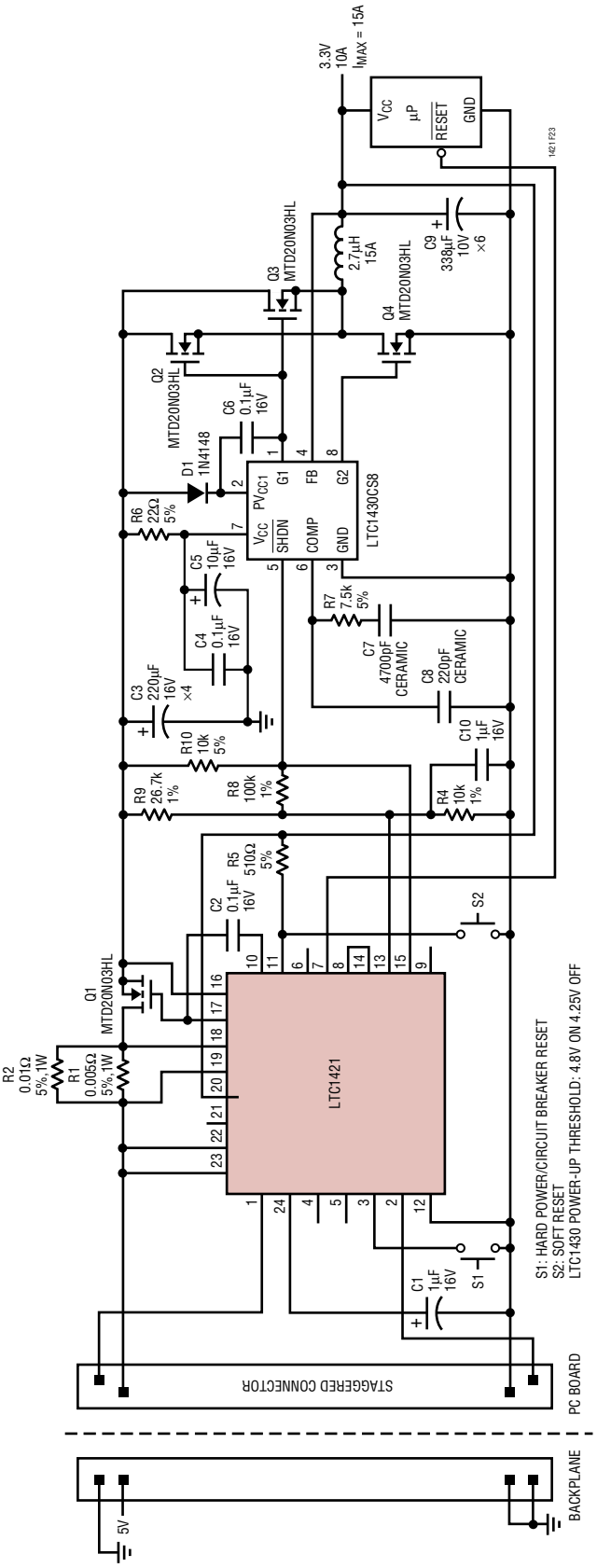


Figure 23. 5V to 3.3V Hot Swappable Supply Using the LTC1430CS8

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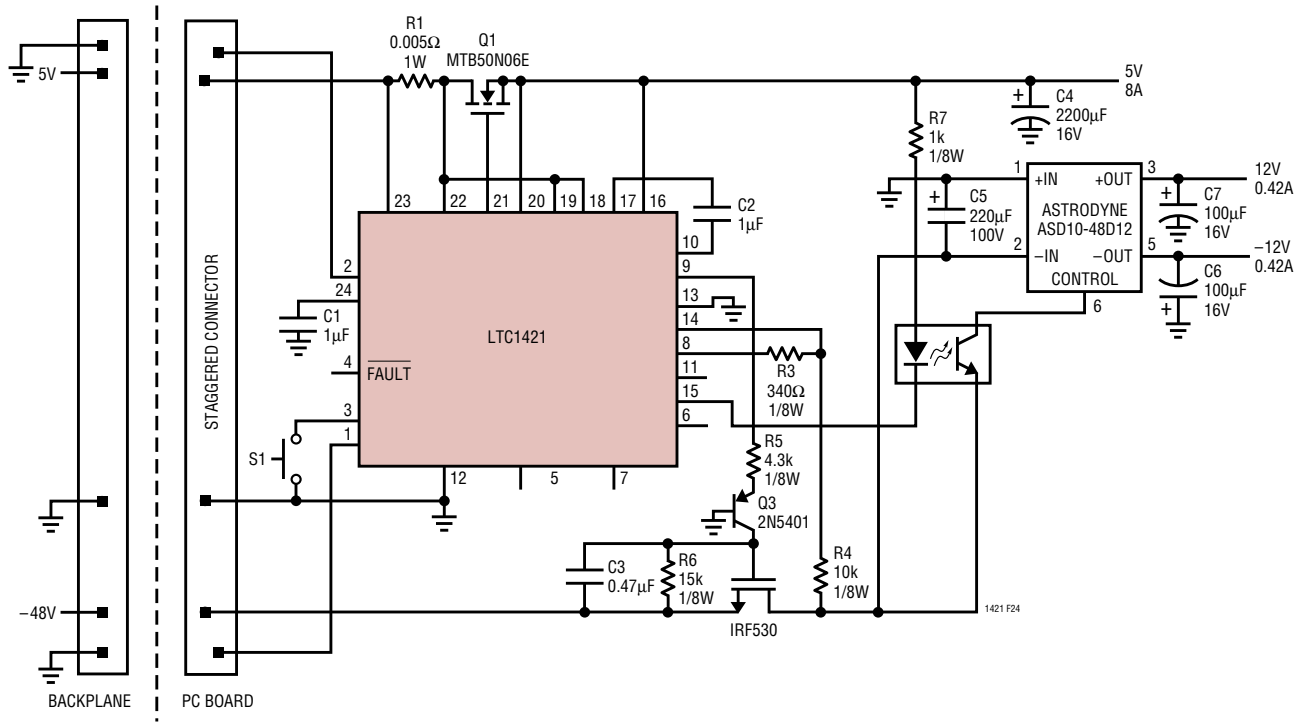


Figure 24. 5V and –48V to ±12V Hot Swappable Supply

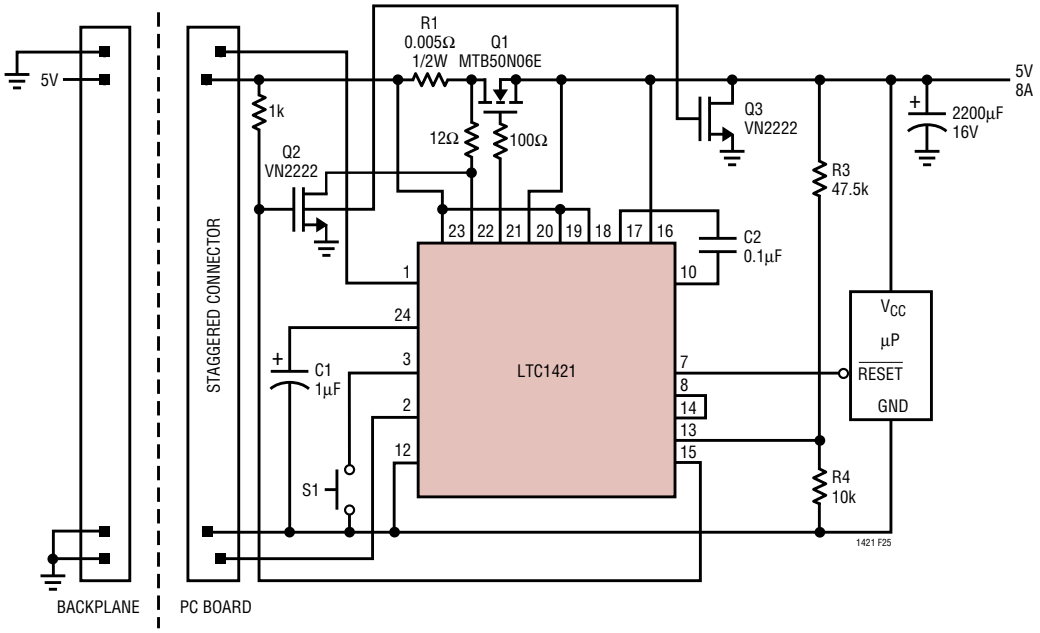


Figure 25. Hot Swappable 5V Supply with Overvoltage Protection

APPLICATIONS INFORMATION

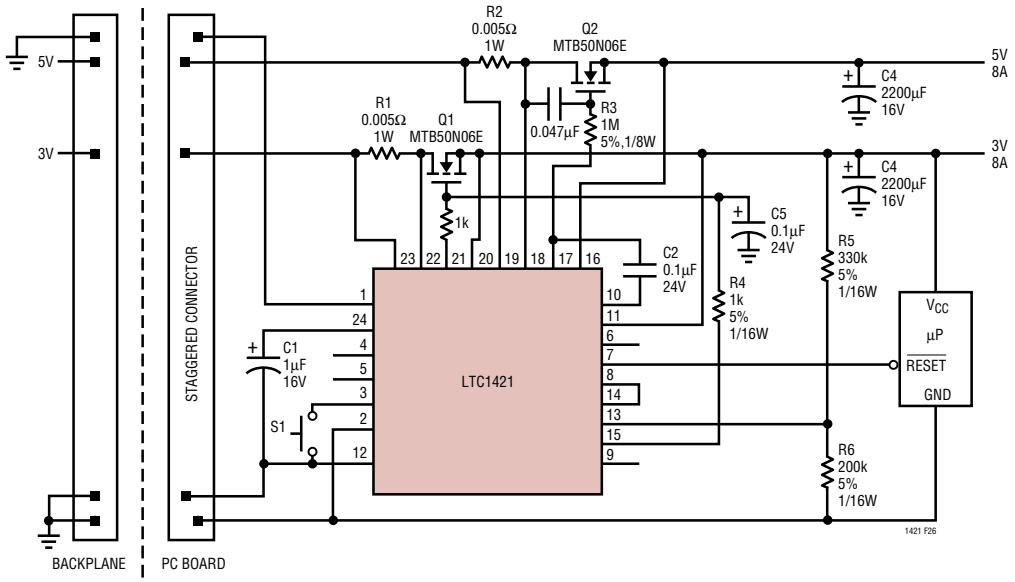
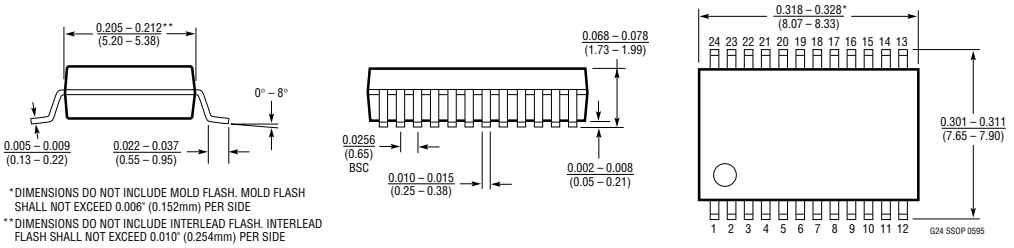


Figure 26. Power-Up and Power-Down Sequence Controller

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

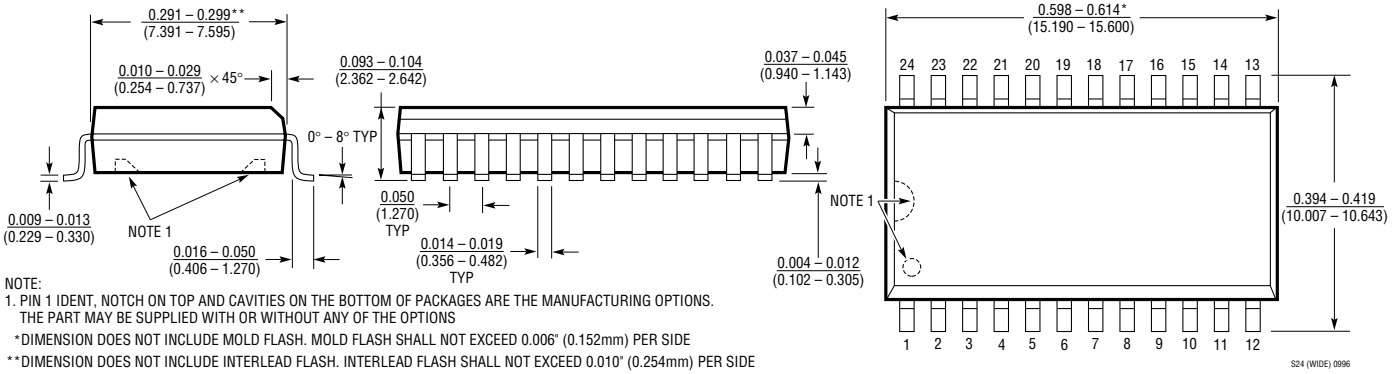
G Package
24-Lead Plastic SSOP (0.209)
(LTC DWG # 05-08-1640)



*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSIONS DO NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

SW Package
24-Lead Plastic Small Outline (Wide 0.300)
(LTC DWG # 05-08-1620)



NOTE:
1. PIN 1 IDENT, NOTCH ON TOP AND CAVITIES ON THE BOTTOM OF PACKAGES ARE THE MANUFACTURING OPTIONS. THE PART MAY BE SUPPLIED WITH OR WITHOUT ANY OF THE OPTIONS

*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

TYPICAL APPLICATION

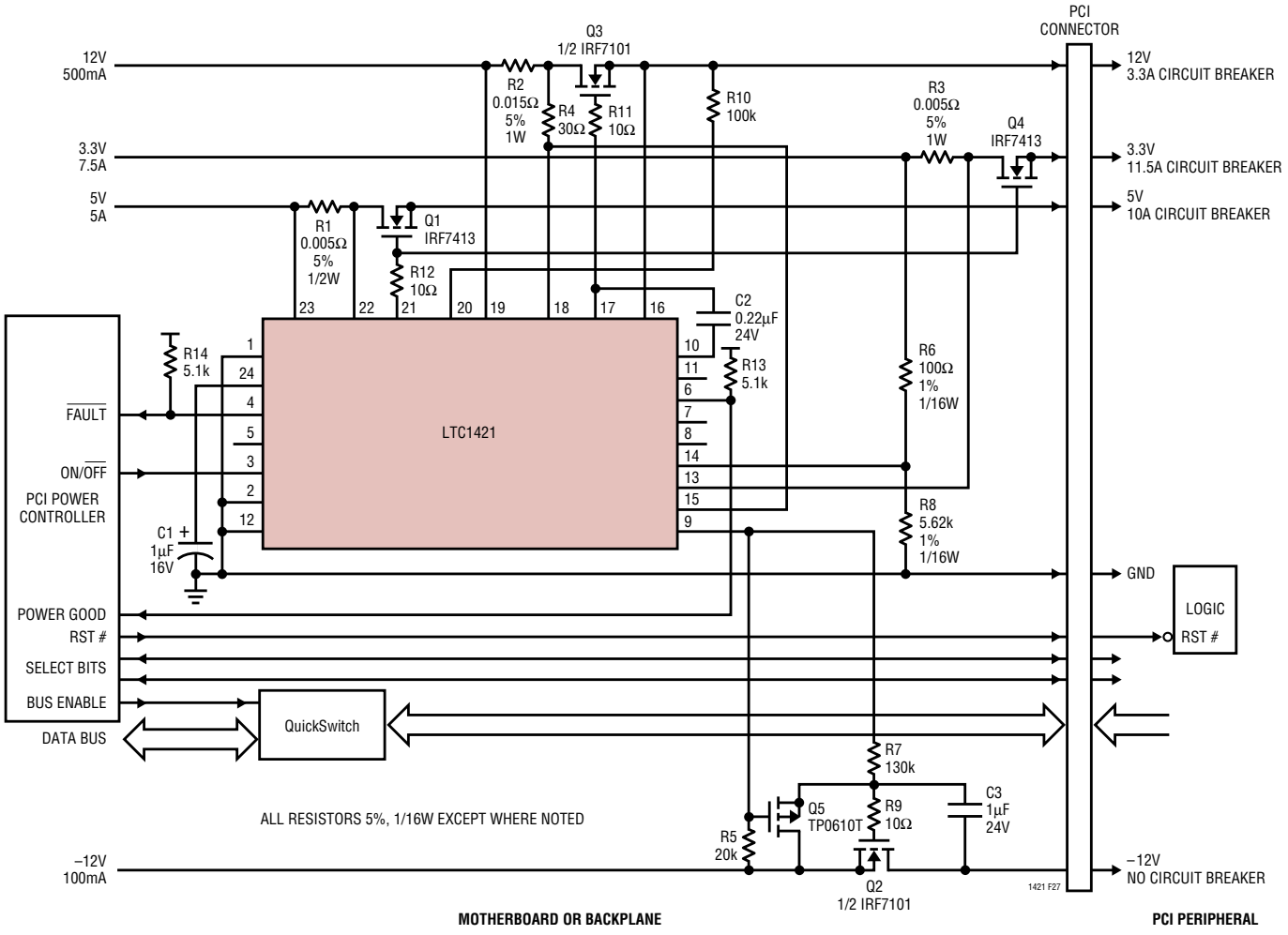


Figure 27. PCI Power Controller

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1155	Dual High Side Switch Driver	Short-Circuit Protection and Micropower Standby Operation
LTC1477/LTC1478	Single and Dual Protected High Side Switches	Inrush Current Limited, Built-In 2A Short-Circuit Protection

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