6 Channel, 14-Bit, 600ksps Simultaneous Sampling ADC with Shutdown

FEATURES

- **600ksps ADC with 6 Simultaneously Sampled Differential Inputs**
- **100ksps Throughput per Channel**
- **76dB SINAD**
- **Low Power Dissipation: 15mW**
- **3V Single Supply Operation**
- 2.5V Internal Bandgap Reference, Can be Overdriven with External Reference
- 3-Wire Serial Interface
- Internal Conversion Triggered by CONV
- SLEEP (6µW) Shutdown Mode
- NAP (3.3mW) Shutdown Mode
- 0V to 2.5V Unipolar, or ±1.25V Bipolar Differential Input Range
- 90dB Common Mode Rejection
- Tiny 32-Pin (5mm × 5mm) QFN Package

APPLICATIONS

- Multiphase Power Measurement
- Multiphase Motor Control
- Data Acquisition Systems
- Uninterruptable Power Supplies

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DESCRIPTION

The LTC®1408 is a 14-bit, 600ksps ADC with six simultaneously sampled differential inputs. The device draws only 5mA from a single 3V supply, and comes in a tiny 32 pin (5mm × 5mm) QFN package. A SLEEP shutdown feature lowers power consumption to 6µW. The combination of low power and tiny package makes the LTC1408 suitable for portable applications.

The LTC1408 contains six separate differential inputs that are sampled simultaneously on the rising edge of the CONV signal. These six sampled inputs are then converted at a rate of 100ksps per channel.

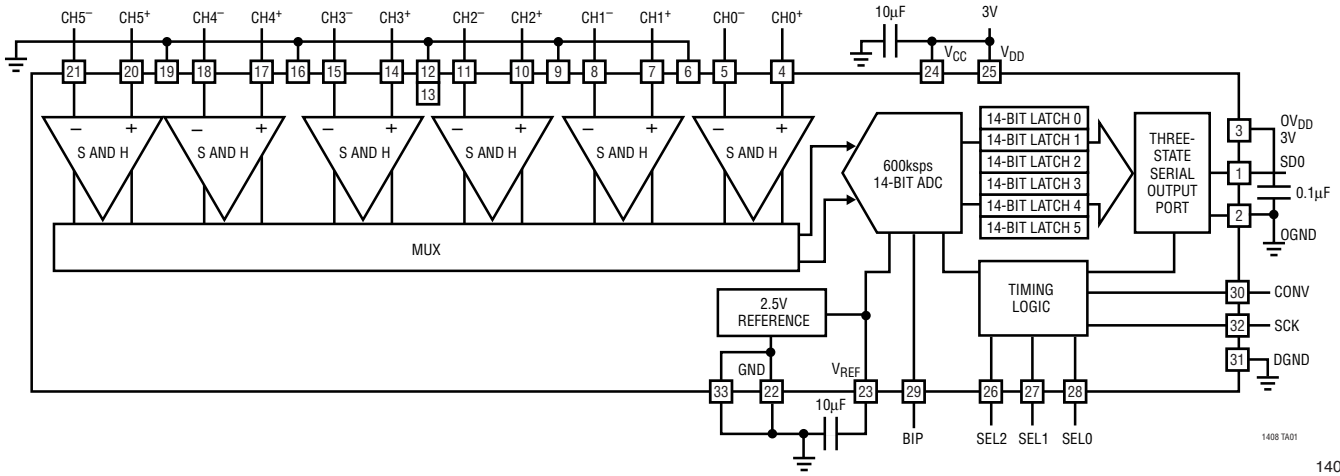
The 90dB common mode rejection allows users to eliminate ground loops and common mode noise by measuring signals differentially from the source.

The device converts 0V to 2.5V unipolar inputs differentially, or ±1.25V bipolar inputs also differentially, depending on the state of the BIP pin. Any analog input may swing rail-to-rail as long as the differential input range is maintained.

The conversion sequence can be abbreviated to convert fewer than six channels, depending on the logic state of the SEL2, SEL1 and SEL0 inputs.

The serial interface sends out the six conversion results in 96 clocks for compatibility with standard serial interfaces.

BLOCK DIAGRAM

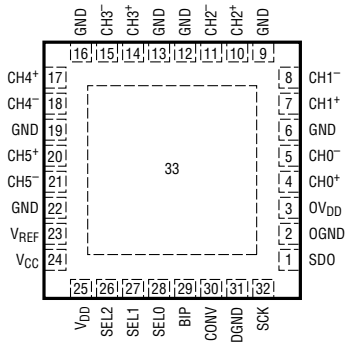


ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

Supply Voltage (V_{DD}, V_{CC}, OV_{DD}) 4V
Analog Input Voltage
(Note 3) ..... –0.3V to (V_{DD} + 0.3V)
Digital Input Voltage ..... –0.3V to (V_{DD} + 0.3V)
Digital Output Voltage ..... –0.3V to (V_{DD} + 0.3V)
Power Dissipation 100mW
Operation Temperature Range
LTC1408C ..... 0°C to 70°C
LTC1408I ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 125°C

PACKAGE/ORDER INFORMATION



QFN PACKAGE
32-PIN (5mm × 5mm) PLASTIC QFN
T_{JMAX} = 125°C, θ_{JA} = 34°C/W
EXPOSED PIN IS GND (PAD 33)
MUST BE SOLDERED TO PCB

ORDER PART NUMBER
LTC1408CUH LTC1408IUH
QFN PART MARKING
1408

Order Options Tape and Reel: Add #TR
Lead Free: Add #PBF Lead Free Tape and Reel: Add #TRPBF
Lead Free Part Marking: http://www.linear.com/leadfree/

Consult LTC Marketing for parts specified with wider operating temperature ranges.

CONVERTER CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. With internal reference, V_{DD} = 3V, V_{DD} = V_{CC} = 3V.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Resolution (No Missing Codes)		●	14			Bits
Integral Linearity Error	(Note 5)	●	–3	±0.5	3	LSB
Offset Error	(Note 4)	●	–4.5	±1	4.5	mV
Offset Match from CH0 to CH5			–3	±0.5	3	mV
Range Error	(Note 4)	●	–12	±2	12	mV
Range Match from CH0 to CH5			–5	±1	5	mV
Range Tempco	Internal Reference (Note 4) External Reference			±15 ±1		ppm/°C ppm/°C

ANALOG INPUT

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. With internal reference, V_{DD} = 3V, V_{DD} = V_{CC} = 3V.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Analog Differential Input Range (Notes 3, 8, 9)	2.7V ≤ V_{DD} ≤ 3.3V			0 to 2.5		V
V_{CM}	Analog Common Mode + Differential Input Range	(Note 8)			0 to V_{DD}		V
I_{IN}	Analog Input Leakage Current		●			1	µA
C_{IN}	Analog Input Capacitance				13		pF
t_{ACQ}	Sample-and-Hold Acquisition Time	(Note 6)	●			39	ns
t_{AP}	Sample-and-Hold Aperture Delay Time				1		ns
t_{JITTER}	Sample-and-Hold Aperture Delay Time Jitter				0.3		ps
t_{SK}	Channel to Channel Aperture Skew				200		ps
CMRR	Analog Input Common Mode Rejection Ratio	f_{IN} = 100kHz, V_{IN} = 0V to 3V f_{IN} = 10MHz, V_{IN} = 0V to 3V			–83 –67		dB dB

DYNAMIC ACCURACY

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. With internal reference, V_{DD} = 3V, V_{DD} = V_{CC} = 3V.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
SINAD	Signal-to-Noise Plus Distortion Ratio	100kHz Input Signal 300kHz Input Signal 100kHz Input Signal, External V_{REF} = 3.3V, $V_{DD} \geq$ 3.3V 300kHz Input Signal, External V_{REF} = 3.3V, $V_{DD} \geq$ 3.3V	●	73	76 76 79 79		dB dB dB dB
THD	Total Harmonic Distortion	100kHz First 5 Harmonics 300kHz First 5 Harmonics	●	–80	–90 –86		dB dB
SFDR	Spurious Free Dynamic Range	100kHz Input Signal 300kHz Input Signal			90 86		dB dB
IMD	Intermodulation Distortion	0.625V_{P-P}, 833kHz into CH0+, 0.625V_{P-P}, 841kHz into CH0–. Bipolar Mode. Also Applicable to Other Channels			–80		dB
	Code-to-Code Transition Noise	V_{REF} = 2.5V (Note 17)			0.7		LSB_{RMS}
	Full Power Bandwidth	V_{IN} = 2.5V_{P-P}, SDO = 11585LSB_{P-P} (–3dBFS) (Note 15)			50		MHz
	Full Linear Bandwidth	S/(N + D) ≥ 68dB, Bipolar Differential Input			5		MHz

INTERNAL REFERENCE CHARACTERISTICS

T_A = 25°C. V_{DD} = V_{CC} = 3V.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{REF} Output Voltage	I_{OUT} = 0			2.5		V
V_{REF} Output Tempco				15		ppm/°C
V_{REF} Line Regulation	V_{DD} = 2.7V to 3.6V, V_{REF} = 2.5V			600		µV/V
V_{REF} Output Resistance	Load Current = 0.5mA			0.2		Ω
V_{REF} Settling Time				2		ms

DIGITAL INPUTS AND DIGITAL OUTPUTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{DD} = V_{CC} = 3V.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage	V_{DD} = 3.3V	●	2.4			V
V_{IL}	Low Level Input Voltage	V_{DD} = 2.7V	●			0.6	V
I_{IN}	Digital Input Current	V_{IN} = 0V to V_{DD}	●			±10	µA
C_{IN}	Digital Input Capacitance				5		pF
V_{OH}	High Level Output Voltage	V_{DD} = 3V, I_{OUT} = –200µA	●	2.5	2.9		V
V_{OL}	Low Level Output Voltage	V_{DD} = 2.7V, I_{OUT} = 160µA V_{DD} = 2.7V, I_{OUT} = 1.6mA	 ●		0.05	 0.4	V V
I_{OZ}	Hi-Z Output Leakage D_{OUT}	V_{OUT} = 0V and V_{DD}	●			±10	µA
C_{OZ}	Hi-Z Output Capacitance D_{OUT}				1		pF
I_{SOURCE}	Output Short-Circuit Source Current	V_{OUT} = 0V, V_{DD} = 3V			20		mA
I_{SINK}	Output Short-Circuit Sink Current	V_{OUT} = V_{DD} = 3V			15		mA

POWER REQUIREMENTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. With internal reference, V_{DD} = V_{CC}= 3V.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{DD}, V_{CC}	Supply Voltage			2.7		3.6	V
I_{DD} + I_{CC}	Supply Current	Active Mode, f_{SAMPLE} = 600ksps	●		5	7	mA
		Nap Mode	●		1.1	1.9	mA
		Sleep Mode			2.0	15	µA
PD	Power Dissipation	Active Mode with SCK, f_{SAMPLE} = 600ksps			15		mW

TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{DD} = 3V.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$f_{SAMPLE(MAX)}$	Maximum Sampling Frequency per Channel (Conversion Rate)		●	100			kHz
$t_{THROUGHPUT}$	Minimum Sampling Period (Conversion + Acquisiton Period)		●			667	ns
t_{SCK}	Clock Period	(Note 16)	●	100		10000	ns
t_{CONV}	Conversion Time	(Notes 6, 17)		96			SCLK cycles
t_1	Minimum Positive or Negative SCLK Pulse Width	(Note 6)		2			ns
t_2	CONV to SCK Setup Time	(Notes 6, 10)		3		10000	ns
t_3	SCK Before CONV	(Note 6)		0			ns
t_4	Minimum Positive or Negative CONV Pulse Width	(Note 6)		4			ns
t_5	SCK to Sample Mode	(Note 6)		4			ns
t_6	CONV to Hold Mode	(Notes 6, 11)		1.2			ns
t_7	96th SCK↑ to CONV↑ Interval (Affects Acquisition Period)	(Notes 6, 7, 13)		45			ns
t_8	Minimum Delay from SCK to Valid Bits 0 Through 11	(Notes 6, 12)		8			ns
t_9	SCK to Hi-Z at SDO	(Notes 6, 12)		6			ns
t_{10}	Previous SDO Bit Remains Valid After SCK	(Notes 6, 12)		2			ns
t_{11}	V_{REF} Settling Time After Sleep-to-Wake Transition	(Notes 6, 14)			2		ms

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliabilty and lifetime.

Note 2: All voltage values are with respect to ground GND.

Note 3: When these pins are taken below GND or above V_{DD}, they will be clamped by internal diodes. This product can handle input currents greater than 100mA below GND or greater than V_{DD} without latchup.

Note 4: Offset and range specifications apply for a single-ended $CH0^+$ – $CH5^+$ input with $CH0^-$ – $CH5^-$ grounded and using the internal 2.5V reference.

Note 5: Integral linearity is tested with an external 2.55V reference and is defined as the deviation of a code from the straight line passing through the actual endpoints of a transfer curve. The deviation is measured from the center of quantization band. Linearity is tested for CH0 only.

Note 6: Guaranteed by design, not subject to test.

Note 7: Recommended operating conditions.

Note 8: The analog input range is defined for the voltage difference between CHx^+ and CHx^-, x = 0–5.

Note 9: The absolute voltage at CHx^+ and CHx^- must be within this range.

Note 10: If less than 3ns is allowed, the output data will appear one clock cycle later. It is best for CONV to rise half a clock before SCK, when running the clock at rated speed.

Note 11: Not the same as aperture delay. Aperture delay (1ns) is the difference between the 2.2ns delay through the sample-and-hold and the 1.2ns CONV to Hold mode delay.

Note 12: The rising edge of SCK is guaranteed to catch the data coming out into a storage latch.

Note 13: The time period for acquiring the input signal is started by the 96th rising clock and it is ended by the rising edge of CONV.

Note 14: The internal reference settles in 2ms after it wakes up from Sleep mode with one or more cycles at SCK and a 10µF capacitive load.

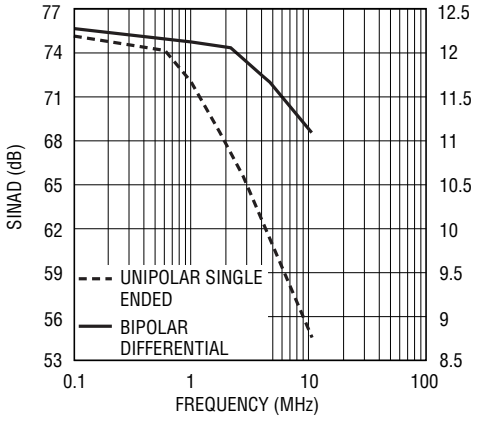
Note 15: The full power bandwidth is the frequency where the output code swing drops by 3dB with a $2.5V_{P-P}$ input sine wave.

Note 16: Maximum clock period guarantees analog performance during conversion. Output data can be read with an arbitrarily long clock period.

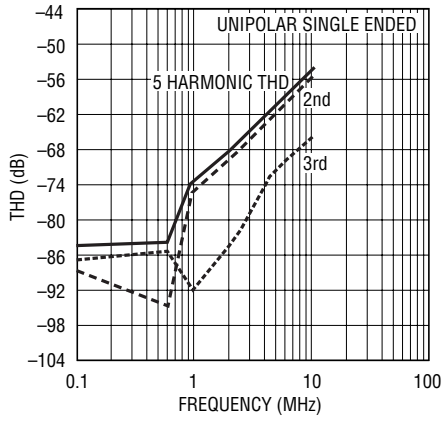
Note 17: The conversion process takes 16 clocks for each channel that is enabled, up to 96 clocks for all 6 channels.

TYPICAL PERFORMANCE CHARACTERISTICS V_{DD} = 3V, T_A = 25°C

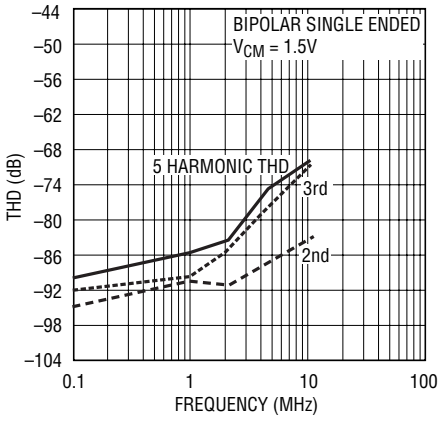
SINAD, ENOBs vs Frequency



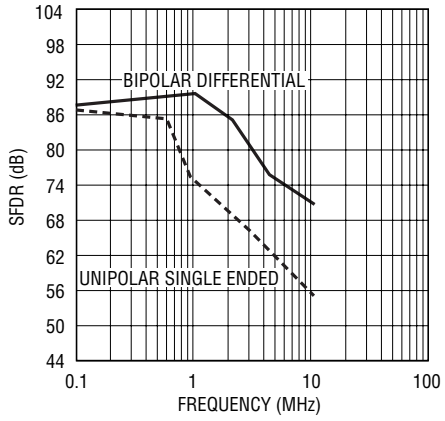
THD, 2nd and 3rd vs Input Frequency



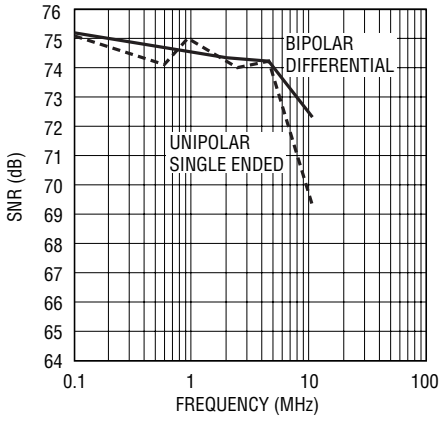
THD, 2nd and 3rd vs Input Frequency



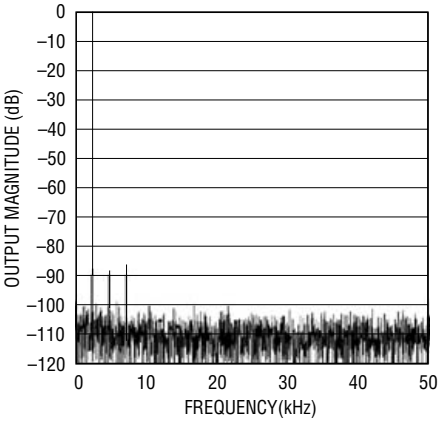
SFDR vs Input Frequency



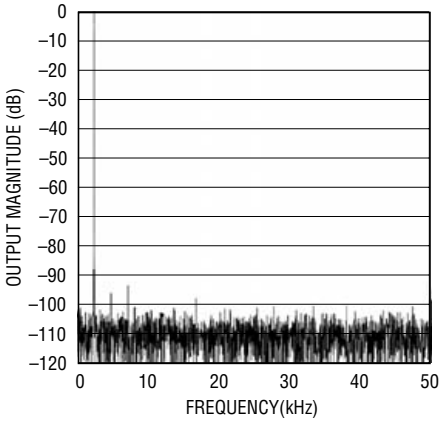
SNR vs Input Frequency



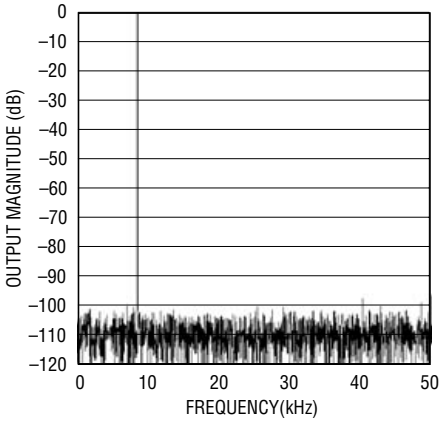
98kHz Unipolar Sine Wave 4096 Point FFT Plot, 100 ksps



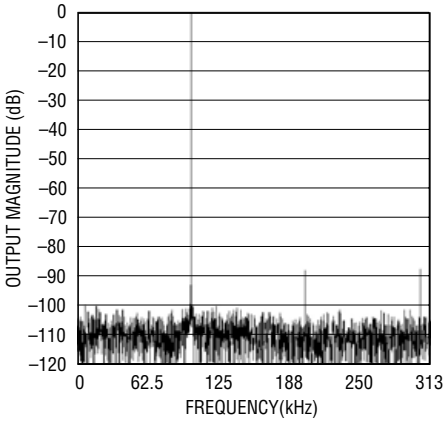
98kHz Bipolar Sine Wave 4096 Point FFT Plot, 100 ksps



591kHz Bipolar Differential Sine Wave 4096 Point FFT Plot, 100 ksps

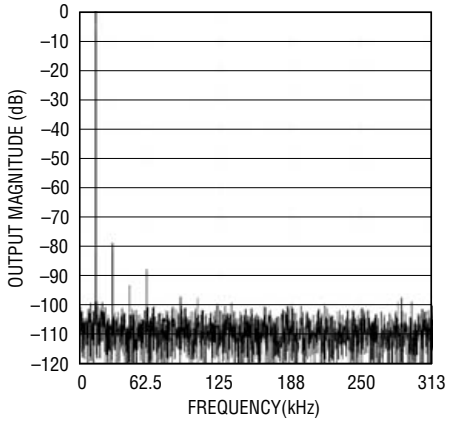


101kHz Unipolar Single Ended Sine Wave 4096 Point FFT Plot, 625 ksps

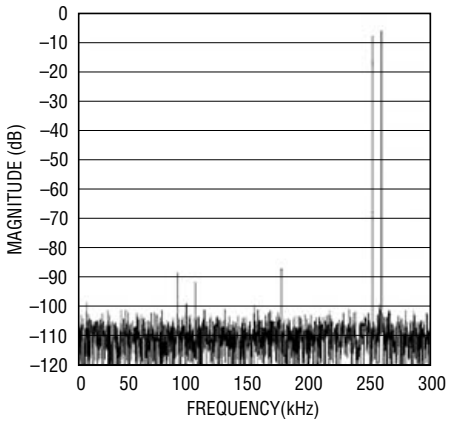


TYPICAL PERFORMANCE CHARACTERISTICS V_{DD} = 3V, T_A = 25°C

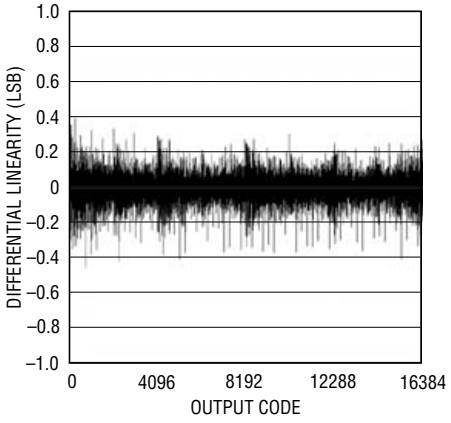
610kHz Unipolar Single Ended Input Sine Wave 4096 Point FFT, 625ksps



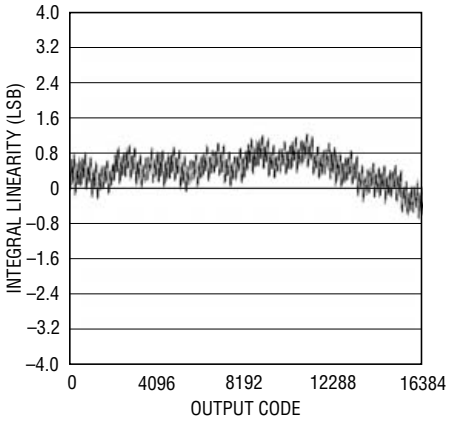
833kHz into CH0 +, 841kHz into CH0 –, 588ksps Bipolar Mode 4096 Point FFT



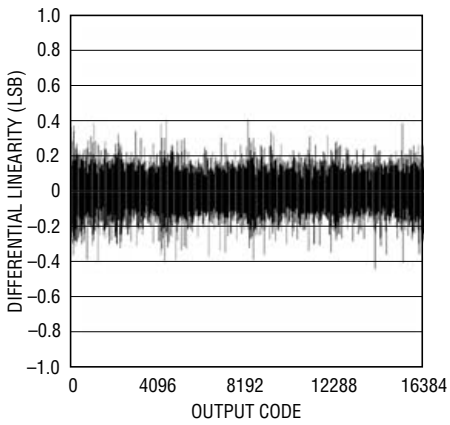
Differential Linearity for CH0 with Internal 2.5V Reference, Unipolar Mode



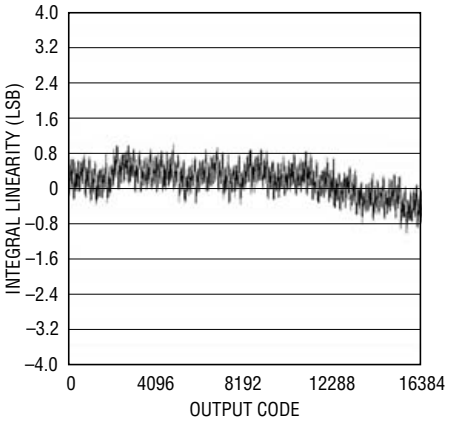
Integral Linearity End Point Fit for CH0 with Internal 2.5V Reference, Unipolar Mode



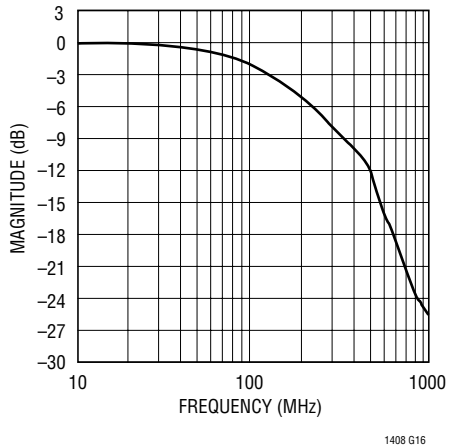
Differential Linearity for CH0 with Internal 2.5V Reference, Differential Input in Bipolar Mode



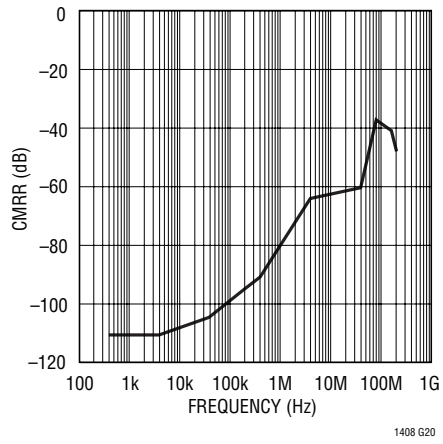
Integral Linearlty End Point Fit



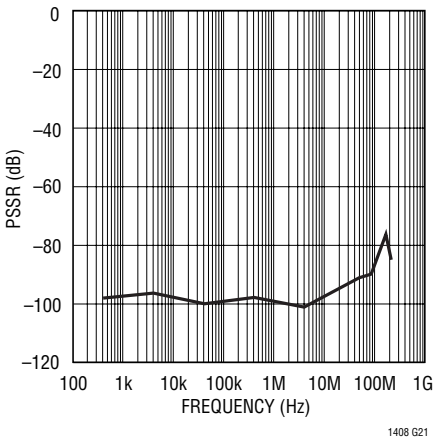
Full Scale Signal Response



CMRR vs Frequency

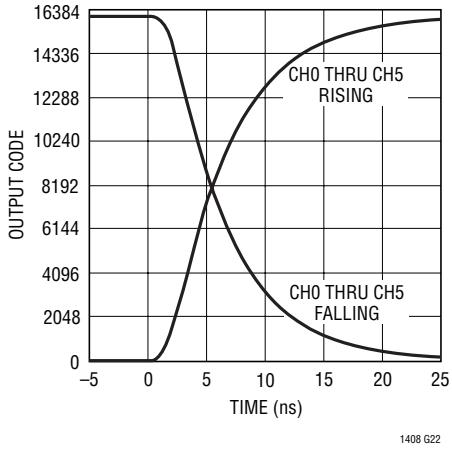


CROSSTALK vs Frequency

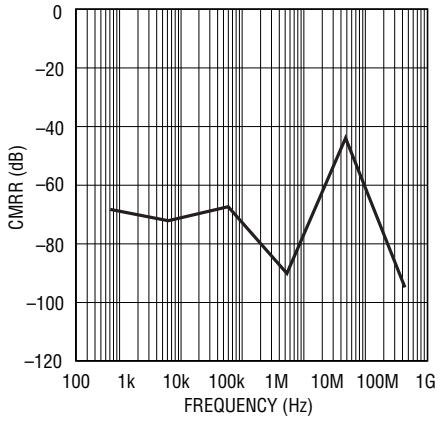


TYPICAL PERFORMANCE CHARACTERISTICS V_{DD} = 3V, T_A = 25°C

Simultaneous Step at all 6 Channels from 25Ω Source Sampling Frequency = 625ksps Input Frequency = 625.0381MHz



PSRR vs Frequency



PIN FUNCTIONS

SDO (Pin 1): Three-State Serial Data Output. Each set of six output data words represent the six analog input channels at the start of the previous conversion. Data for CH0 comes out first and data for CH5 comes out last. Each data word comes out MSB first.

OGND (Pin 2): Ground Return for SDO Currents. This pad must always be within 300mV of the ground plane potential.

OV_{DD} (Pin 3): Power Supply for the SDO Pin. OV_{DD} must be no more than 300mV higher than V_{DD} and can be brought to a lower voltage to interface to low voltage logic families. The unloaded high state at SDO is at the potential of OV_{DD}.

$CH0^+$ (Pin 4): Non-Inverting Channel 0. $CH0^+$ operates fully differentially with respect to $CH0^-$ with a 0V to 2.5V, or ±1.25V differential swing and a 0V to V_{DD} absolute input range.

$CH0^-$ (Pin 5): Inverting Channel 0. $CH0^-$ operates fully differentially with respect to $CH0^+$ with a –2.5V to 0V, or ±1.25V differential swing and a 0V to V_{DD} absolute input range.

GND (Pins 6, 9, 12, 13, 16, 19): Analog Grounds. These ground pins must be tied directly to the solid ground plane under the part. Analog signal currents flow through these connections.

$CH1^+$ (Pin 7): Non-Inverting Channel 1. $CH1^+$ operates fully differentially with respect to $CH1^-$ with a 0V to 2.5V, or ±1.25V differential swing and a 0V to V_{DD} absolute input range.

$CH1^-$ (Pin 8): Inverting Channel 1. $CH1^-$ operates fully differentially with respect to $CH1^+$ with a –2.5V to 0V, or ±1.25V differential swing and a 0V to V_{DD} absolute input range.

$CH2^+$ (Pin 10): Non-Inverting Channel 2. $CH2^+$ operates fully differentially with respect to $CH2^-$ with a 0V to 2.5V, or ±1.25V differential swing and a 0V to V_{DD} absolute input range.

$CH2^-$ (Pin 11): Inverting Channel 2. $CH2^-$ operates fully differentially with respect to $CH2^+$ with a –2.5V to 0V, or ±1.25V differential swing and a 0V to V_{DD} absolute input range.

PIN FUNCTIONS

CH3$^+$ (Pin 14): Non-Inverting Channel 3. CH3$^+$ operates fully differentially with respect to CH3$^-$ with a 0V to 2.5V, or ±1.25V differential swing and a 0V to V_{DD} absolute input range.

CH3$^-$ (Pin 15): Inverting Channel 3. CH3$^-$ operates fully differentially with respect to CH3$^+$ with a –2.5V to 0V, or ±1.25V differential swing and a 0V to V_{DD} absolute input range.

CH4$^+$ (Pin 17): Non-Inverting Channel 4. CH4$^+$ operates fully differentially with respect to CH4$^-$ with a 0V to 2.5V, or ±1.25V differential swing and a 0V to V_{DD} absolute input range.

CH4$^-$ (Pin 18): Inverting Channel 4. CH4$^-$ operates fully differentially with respect to CH4$^+$ with a –2.5V to 0V, or ±1.25V differential swing and a 0V to V_{DD} absolute input range.

CH5$^+$ (Pin 20): Non-Inverting Channel 5. CH5$^+$ operates fully differentially with respect to CH5$^-$ with a 0V to 2.5V, or ±1.25V differential swing and a 0V to V_{DD} absolute input range.

CH5$^-$ (Pin 21): Inverting Channel 5. CH5$^-$ operates fully differentially with respect to CH5$^+$ with a –2.5V to 0V, or ±1.25V differential swing and a 0V to V_{DD} absolute input range.

GND (PIN 22): Analog Ground for Reference. Analog ground must be tied directly to the solid ground plane under the part. Analog signal currents flow through this connection. The 10µF reference bypass capacitor should be returned to this pad.

V_{REF} (Pin 23): 2.5V Internal Reference. Bypass to GND and a solid analog ground plane with a 10µF ceramic capacitor (or 10µF tantalum in parallel with 0.1µF ceramic). Can be overdriven by an external reference voltage between 2.55% and V_{DD}, V_{CC}.

V_{CC} (Pin 24): 3V Positive Analog Supply. This pin supplies 3V to the analog section. Bypass to the solid analog ground plane with a 10µF ceramic capacitor (or 10µF tantalum) in parallel with 0.1µF ceramic. Care should be taken to place the 0.1µF bypass capacitor as close to Pin 24 as possible. Pin 24 must be tied to Pin 25.

V_{DD} (Pin 25): 3V Positive Digital Supply. This pin supplies 3V to the logic section. Bypass to DGND pin and solid analog ground plane with a 10µF ceramic capacitor (or 10µF tantalum in parallel with 0.1µF ceramic). Keep in mind that internal digital output signal currents flow through this pin. Care should be taken to place the 0.1µF bypass capacitor as close to Pin 25 as possible. Pin 25 must be tied to Pin 24.

SEL2 (Pin 26): Most significant bit controlling the number of channels being converted. In combination with SEL1 and SEL0, 000 selects just the first channel (CH0) for conversion. Incrementing SELx selects additional channels(CH0–CH5) for conversion. 101, 110 or 111 select all 6 channels for conversion. Must be kept in a fixed state during conversion and during the subsequent conversion to read data.

SEL1 (Pin 27): Middle significance bit controlling the number of channels being converted. In combination with SEL0 and SEL2, 000 selects just the first channel (CH0) for conversion. Incrementing SELx selects additional channels for conversion. 101, 110 or 111 select all 6 channels (CH0–CH5) for conversion. Must be kept in a fixed state during conversion and during the subsequent conversion to read data.

SEL0 (Pin 28): Least significant bit controlling the number of channels being converted. In combination with SEL1 and SEL2, 000 selects just the first channel (CH0) for conversion. Incrementing SELx selects additional channels for conversion. 101, 110 or 111 select all 6 channels (CH0–CH5) for conversion. Must be kept in a fixed state during conversion and during the subsequent conversion to read data.

BIP (Pin 29): Bipolar/Unipolar Mode. The input differential range is 0V – 2.5V when BIP is LOW, and it is ±1.25 when BIP is HIGH. Must be kept in fixed state during conversion and during subsequent conversion to read data. When changing BIP between conversions the full acquisition time must be allowed before starting the next conversion. The output data is in 2's complement format for bipolar mode and straight binary format for unipolar mode.

PIN FUNCTIONS

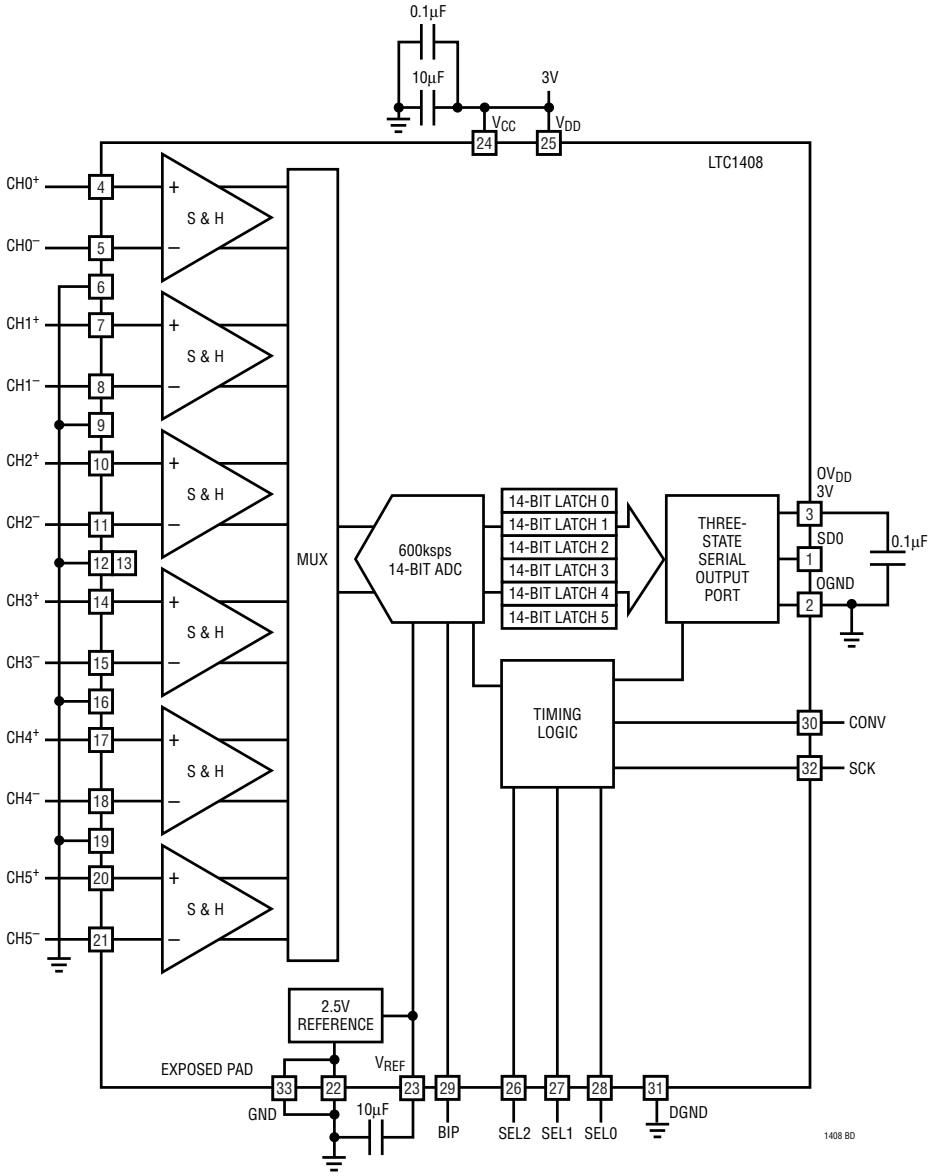
CONV (Pin 30): Convert Start. Holds the six analog input signals and starts the conversion on the rising edge. Two pulses with SCK in fixed high or fixed low state starts Nap mode. Four or more pulses with SCK in fixed high or fixed low state starts Sleep mode.

DGND (Pin 31): Digital Ground. This ground pin must be tied directly to the solid ground plane. Digital input signal currents flow through this pin.

SCK (Pin 32): External Clock Input. Advances the conversion process and sequences the output data at SD0 (Pin1) on the rising edge. One or more pulses wake from sleep or nap power saving modes. 16 clock cycles are needed for each of the channels that are activated by SELx (Pins 26, 27, 28), up to a total of 96 clock cycles needed to convert and read out all 6 channels.

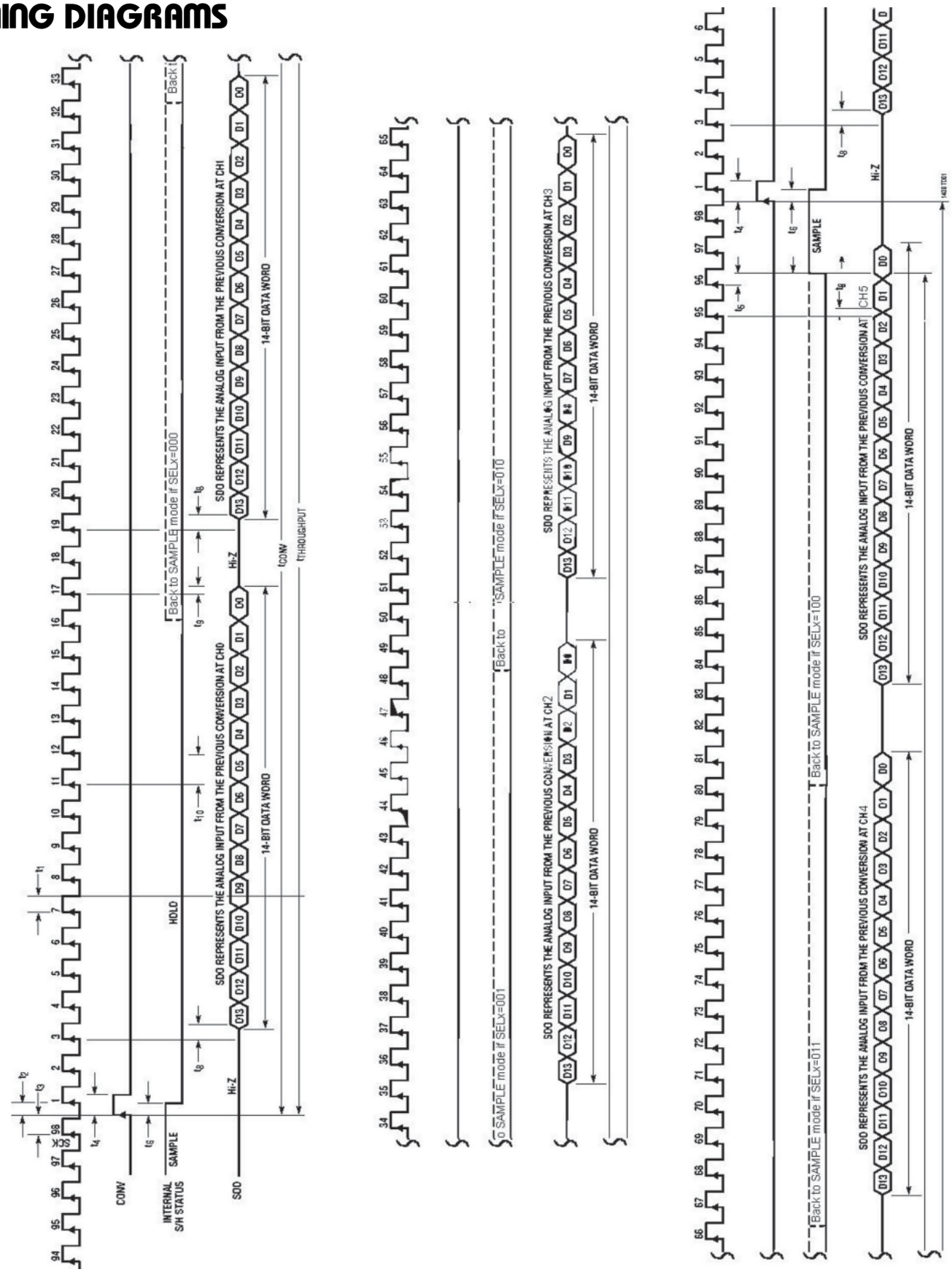
EXPOSED PAD (Pin 33): GND. Must be tied directly to the solid ground plane.

BLOCK DIAGRAM



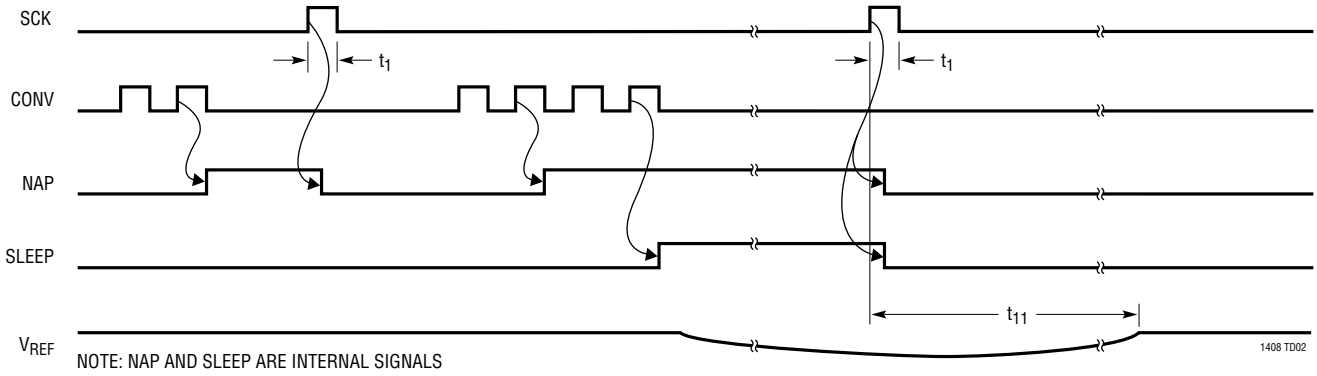
TIMING DIAGRAMS

LTC1408 Timing Diagram



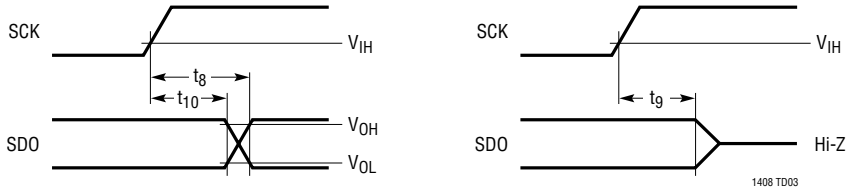
TIMING DIAGRAMS

Nap Mode and Sleep Mode Waveforms



NOTE: NAP AND SLEEP ARE INTERNAL SIGNALS

SCK to SDO Delay



APPLICATIONS INFORMATION

SELECT NUMBER OF CONVERTED CHANNELS (SEL2, SEL1, SEL0)

These three control pins select the number of channels being converted. 000 selects only the first channel (CH0) for conversion. Incrementing SELx selects additional channels for conversion, up to 6 channels. 101, 110 or 111 select all 6 channels for conversion. These pins must be kept in a fixed state during conversion and during the subsequent conversion to read data. When changing modes between conversions, keep in mind that the output data of a particular channel will remain unchanged until after that channel is converted again. For example: convert a sequence of 4 channels (CH0, CH1, CH2, CH3) with SELx = 011, then, after these channels are converted change SELx to 001 to convert just CH0 and CH1. See Table 1. During the conversion of the first set of two channels you will be able to read the data from the same two channels converted as part of the previous group of 4 channels. Later, you could convert 4 or more channels to read back the unread CH2 and CH3 data that was converted in the first set of 4 channels. These pins are often hardwired to enable the right number of channels for a particular application.

BIPOLAR/UNIPOLAR MODE

The input voltage range for each of the CHx input differential pairs is UNIPOLAR 0V – 2.5V when BIP is LOW, and BIPOLAR ±1.25V when BIP is HIGH. This pin must be kept in fixed state during conversion and during subsequent conversion to read data. When changing BIP between conversions the full acquisition time must be allowed before starting the next conversion. After changing modes from BIPOLAR to UNIPOLAR, or from UNIPOLAR to BIPOLAR, you can still read the first set of channels in the new mode, by inverting the MSB to read these channels in the mode that they were converted in.

DRIVING THE ANALOG INPUT

The differential analog inputs of the LTC1408 are easy to drive. The inputs may be driven differentially or as a single-ended input (i.e., the $CH0^-$ input is grounded). All twelve analog inputs of all six differential analog input pairs, $CH0^+$ with $CH0^-$, $CH1^+$ with $CH1^-$, $CH2^+$ with $CH2^-$, $CH3^+$ with $CH3^-$, $CH4^+$ with $CH4^-$ and $CH5^+$ with $CH5^-$, are sampled at the same instant. Any unwanted signal that is common to both inputs of each input pair will be reduced by the common mode rejection of the sample-and-hold circuit. The inputs draw only one small current spike while charging the sample-and-hold capacitors at the end of conversion. During conversion, the analog inputs draw only a small leakage current. If the source impedance of the driving circuit is low, then the LTC1408 inputs can be driven directly. As source impedance increases, so will acquisition time. For minimum acquisition time with high source impedance, a buffer amplifier must be used. The main requirement is that the amplifier driving the analog input(s) must settle after the small current spike before the next conversion starts (the time allowed for settling must be at least 39ns for full throughput rate). Also keep in mind, while choosing an input amplifier, the amount of noise and harmonic distortion added by the amplifier.

Table 1. Conversion Sequence Control
("acquire" represents simultaneous sampling of all channels; CHx represents conversion of channels)

SEL2	SEL1	SEL0	CHANNEL ACQUISITION AND CONVERSION SEQUENCE
0	0	0	acquire, CH0, acquire, CH0...
0	0	1	acquire, CH0, CH1, acquire, CH0, CH1...
0	1	0	acquire, CH0, CH1, CH2, acquire, CH0, CH1, CH2...
0	1	1	acquire, CH0, CH1, CH2, CH3, acquire, CH0, CH1, CH2, CH3...
1	0	0	acquire, CH0, CH1, CH2, CH3, CH4, acquire, CH0,CH1,CH2, CH3, CH4...
1	0	1	acquire, CH0, CH1, CH2, CH3, CH4, CH5, acquire, CH0, CH1, CH2, CH3, CH4, CH5...
1	1	0	acquire, CH0, CH1, CH2, CH3, CH4, CH5, acquire, CH0, CH1, CH2, CH3, CH4, CH5...
1	1	1	acquire, CH0, CH1, CH2, CH3, CH4, CH5, acquire, CH0, CH1, CH2, CH3, CH4, CH5...

APPLICATIONS INFORMATION

CHOOSING AN INPUT AMPLIFIER

Choosing an input amplifier is easy if a few requirements are taken into consideration. First, to limit the magnitude of the voltage spike seen by the amplifier from charging the sampling capacitor, choose an amplifier that has a low output impedance (< 100Ω) at the closed-loop bandwidth frequency. For example, if an amplifier is used in a gain of 1 and has a unity-gain bandwidth of 50MHz, then the output impedance at 50MHz must be less than 100Ω. The second requirement is that the closed-loop bandwidth must be greater than 40MHz to ensure adequate small-signal settling for full throughput rate. If slower op amps are used, more time for settling can be provided by increasing the time between conversions. The best choice for an op amp to drive the LTC1408 depends on the application. Generally, applications fall into two categories: AC applications where dynamic specifications are most critical and time domain applications where DC accuracy and settling time are most critical. The following list is a summary of the op amps that are suitable for driving the LTC1408. (More detailed information is available in the Linear Technology Databooks and on the website at www.linear.com.)

LinearView is a trademark of Linear Technology Corporation.

LTC1566-1: Low Noise 2.3MHz Continuous Time Lowpass Filter.

LT®1630: Dual 30MHz Rail-to-Rail Voltage FB Amplifier. 2.7V to ±15V supplies. Very high A_{VOL}, 500μV offset and 520ns settling to 0.5LSB for a 4V swing. THD and noise are –93dB to 40kHz and below 1LSB to 320kHz (A_V = 1, $2V_{P-P}$ into 1kΩ, V_S = 5V), making the part excellent for AC applications (to 1/3 Nyquist) where rail-to-rail performance is desired. Quad version is available as LT1631.

LT1632: Dual 45MHz Rail-to-Rail Voltage FB Amplifier. 2.7V to ±15V supplies. Very high A_{VOL}, 1.5mV offset and 400ns settling to 0.5LSB for a 4V swing. It is suitable for applications with a single 5V supply. THD and noise are –93dB to 40kHz and below 1LSB to 800kHz (A_V = 1, $2V_{P-P}$ into 1kΩ, V_S = 5V), making the part excellent for AC applications where rail-to-rail performance is desired. Quad version is available as LT1633.

LT1801: 80MHz GBWP, –75dBc at 500kHz, 2mA/amplifier, 8.5nV/√Hz.

LT1806/LT1807: 325MHz GBWP, –80dBc distortion at 5MHz, unity gain stable, rail-to-rail in and out, 10mA/amplifier, 3.5nV/√Hz.

LT1810: 180MHz GBWP, –90dBc distortion at 5MHz, unity gain stable, rail-to-rail in and out, 15mA/amplifier, 16nV/√Hz.

LT1818/LT1819: 400MHz, 2500V/μs, 9mA, Single/Dual Voltage Mode Operational Amplifier.

LT6200: 165MHz GBWP, –85dBc distortion at 1MHz, unity gain stable, rail-to-rail in and out, 15mA/amplifier, 0.95nV/√Hz.

LT6203: 100MHz GBWP, –80dBc distortion at 1MHz, unity gain stable, rail-to-rail in and out, 3mA/amplifier, 1.9nV/√Hz.

LT6600: Amplifier/Filter Differential In/Out with 10MHz Cutoff.

APPLICATIONS INFORMATION

INPUT FILTERING AND SOURCE IMPEDANCE

The noise and the distortion of the input amplifier and other circuitry must be considered since they will add to the LTC1408 noise and distortion. The small-signal bandwidth of the sample-and-hold circuit is 50MHz. Any noise or distortion products that are present at the analog inputs will be summed over this entire bandwidth. Noisy input circuitry should be filtered prior to the analog inputs to minimize noise. A simple 1-pole RC filter is sufficient for many applications. For example, Figure 1 shows a 47pF capacitor from CHO^+ to ground and a 51Ω source resistor to limit the net input bandwidth to 30MHz. The 47pF capacitor also acts as a charge reservoir for the input sample-and-hold and isolates the ADC input from sampling-glitch sensitive circuitry. High quality capacitors and resistors should be used since these components can add distortion. NPO and silvermica type dielectric capacitors have excellent linearity. Carbon surface mount resistors can generate distortion from self heating and from damage that may occur during soldering. Metal film surface mount resistors are much less susceptible to both problems. When high amplitude unwanted signals are close in frequency to the desired signal frequency a multiple pole filter is required.

High external source resistance, combined with 13pF of input capacitance, will reduce the rated 50MHz input bandwidth and increase acquisition time beyond 39ns.

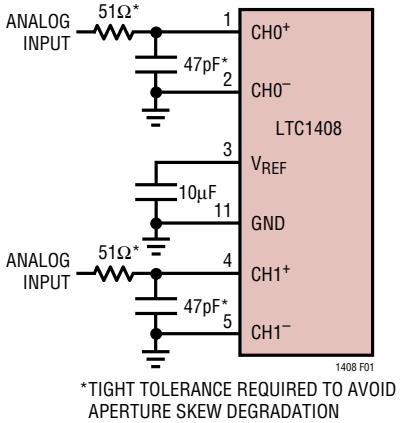


Figure 1. RC Input Filter

INPUT RANGE

The analog inputs of the LTC1408 may be driven fully differentially with a single supply. Either input may swing up to V_{CC}, provided the differential swing is no greater than 2.5V with BIP (Pin 29) Low, or ±1.25V with (BIP Pin 29) High. The 0V to 2.5V range is also ideally suited for single-ended input use with single supply applications. The common mode range of the inputs extend from ground to the supply voltage V_{CC}. If the difference between the CH^+ and $CH^–$ at any input pair exceeds 2.5V (unipolar) or 1.25V (bipolar), the output code will stay fixed at positive full-scale, and if this difference goes below 0V (unipolar) or –1.25V (bipolar), the output code will stay fixed at negative full-scale.

INTERNAL REFERENCE

The LTC1408 has an on-chip, temperature compensated, bandgap reference that is factory trimmed near 2.5V to obtain a precise 2.5V input span. The reference amplifier output V_{REF}, (Pin 23) must be bypassed with a capacitor to ground. The reference amplifier is stable with capacitors of 1µF or greater. For the best noise performance, a 10µF ceramic or a 10µF tantalum in parallel with a 0.1µF ceramic is recommended. The V_{REF} pin can be overdriven with an external reference as shown in Figure 2. The voltage of the external reference must be higher than the 2.5V of the open-drain P-channel output of the internal reference. The recommended range for an external reference is 2.55V to V_{DD}. An external reference at 2.55V will see a DC quiescent load of 0.75mA and as much as 3mA

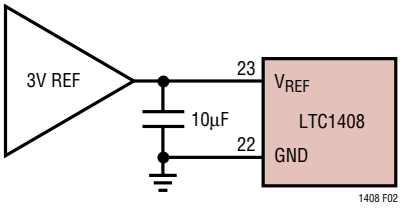


Figure 2. External Reference

APPLICATIONS INFORMATION

during conversion.

INPUT SPAN VERSUS REFERENCE VOLTAGE

The differential input range has a unipolar voltage span that equals the difference between the voltage at the reference buffer output V_{REF} (Pin 23) and the voltage at ground. The differential input range of the ADC is 0V to 2.5V when using the internal reference. The internal ADC is referenced to these two nodes. This relationship also holds true with an external reference.

DIFFERENTIAL INPUTS

The ADC will always convert the difference of CH^+ minus CH^-, independent of the common mode voltage at any pair of inputs. The common mode rejection holds up at high frequencies (see Figure 3.) The only requirement is that both inputs not go below ground or exceed V_{DD}.

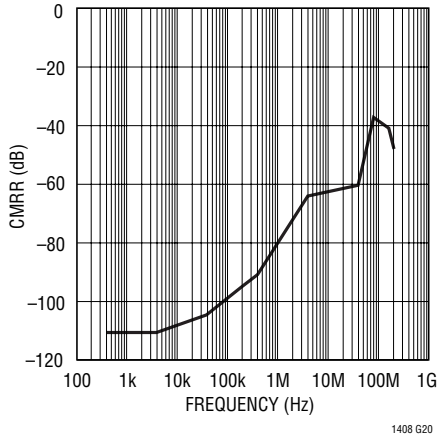


Figure 3. CMRR vs Frequency

Integral nonlinearity errors (INL) and differential nonlinearity errors (DNL) are largely independent of the common mode voltage. However, the offset error will vary. DC CMRR is typically better than –90dB.

Figure 4 shows the ideal input/output characteristics for the LTC1408 in unipolar mode (BIP = Low). The code transitions occur midway between successive integer LSB values (i.e., 0.5LSB, 1.5LSB, 2.5LSB, FS – 1.5LSB). The output code is straight binary with 1LSB = 2.5V/16384 = 153µV for the LTC1408. The LTC1408 has 0.7 LSB RMS of Gaussian white noise.

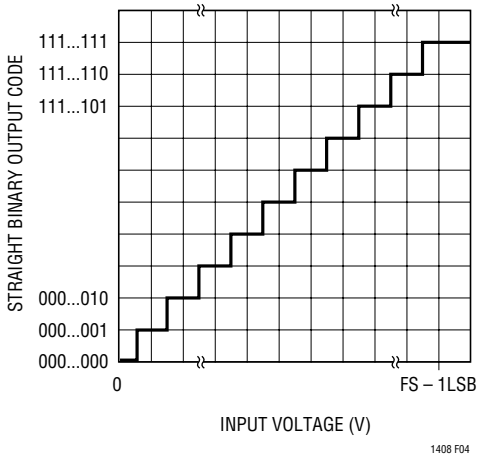


Figure 4. LTC1408 Transfer Characteristic in Unipolar Mode (BIP = Low)

Figure 5 shows the ideal input/output characteristics for the LTC1408 in bipolar mode (BIP = High). The code transitions occur midway between successive integer LSB values (i.e., 0.5LSB, 1.5LSB, 2.5LSB, FS – 1.5LSB). The output code is 2's complement with 1LSB = 2.5V/16384 = 153µV for the LTC1408. The LTC1408 has 0.7 LSB RMS of Gaussian white noise.

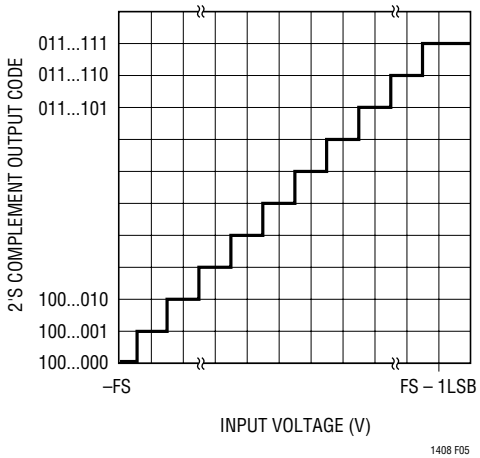


Figure 5. LTC1408 Transfer Characteristic in Bipolar Mode (BIP = High)

APPLICATIONS INFORMATION

POWER-DOWN MODES

Upon power-up, the LTC1408 is initialized to the active state and is ready for conversion. The Nap and Sleep mode waveforms show the power down modes for the LTC1408. The SCK and CONV inputs control the power down modes (see Timing Diagrams). Two rising edges at CONV, without any intervening rising edges at SCK, put the LTC1408 in Nap mode and the power drain drops from 15mW to 3.3mW. The internal reference remains powered in Nap mode. One or more rising edges at SCK wake up the LTC1408 for service very quickly and CONV can start an accurate conversion within a clock cycle. Four rising edges at CONV, without any intervening rising edges at SCK, put the LTC1408 in Sleep mode and the power drain drops from 15mW to 10µW. One or more rising edges at SCK wake up the LTC1408 for operation. The internal reference (V_{REF}) takes 2ms to slew and settle with a 10µF load. Using sleep mode more frequently compromises the accuracy of the output data. Note that for slower conversion rates, the Nap and Sleep modes can be used for substantial reductions in power consumption.

DIGITAL INTERFACE

The LTC1408 has a 3-wire SPI (Serial Peripheral Interface) interface. The SCK and CONV inputs and SDO output implement this interface. The SCK and CONV inputs accept swings from 3V logic and are TTL compatible, if the logic swing does not exceed V_{DD}. A detailed description of the three serial port signals follows:

Conversion Start Input (CONV)

The rising edge of CONV starts a conversion, but subsequent rising edges at CONV are ignored by the LTC1408 until the following 96 SCK rising edges have occurred. The duty cycle of CONV can be arbitrarily chosen to be used as a frame sync signal for the processor serial port. A simple approach to generate CONV is to create a pulse that is one SCK wide to drive the LTC1408 and then buffer this signal to drive the frame sync input of the processor serial port. It is good practice to drive the LTC1408 CONV input first to avoid digital noise interference during the sample-to-hold transition triggered by CONV at the start of conversion. It is also good practice to keep the width of the low portion of the CONV signal greater than 15ns to avoid introducing glitches in the front end of the ADC just before the sample-and-hold goes into Hold mode at the rising edge of CONV.

APPLICATIONS INFORMATION

Minimizing Jitter on the CONV Input

In high speed applications where high amplitude sinewaves above 100kHz are sampled, the CONV signal must have as little jitter as possible (10ps or less). The square wave output of a common crystal clock module usually meets this requirement easily. The challenge is to generate a CONV signal from this crystal clock without jitter corruption from other digital circuits in the system. A clock divider and any gates in the signal path from the crystal clock to the CONV input should not share the same integrated circuit with other parts of the system. The SCK and CONV inputs should be driven first, with digital buffers used to drive the serial port interface. Also note that the master clock in the DSP may already be corrupted with jitter, even if it comes directly from the DSP crystal. Another problem with high speed processor clocks is that they often use a low cost, low speed crystal (i.e., 10MHz) to generate a fast, but jittery, phase-locked-loop system clock (i.e., 40MHz). The jitter in these PLL-generated high speed clocks can be several nanoseconds. Note that if you choose to use the frame sync signal generated by the DSP port, this signal will have the same jitter of the DSP's master clock.

The Typical Application Figure on page 20 shows a circuit for level-shifting and squaring the output from an RF signal generator or other low-jitter source. A single D-type flip flop is used to generate the CONV signal to the LTC1408. Re-timing the master clock signal eliminates clock jitter introduced by the controlling device (DSP, FPGA, etc.) Both the inverter and flip flop must be treated as analog components and should be powered from a clean analog supply.

Serial Clock Input (SCK)

The rising edge of SCK advances the conversion process and also udpates each bit in the SDO data stream. After CONV rises, the third rising edge of SCK sends out up to six sets of 14 data bits, with the MSB sent first. A simple approach is to generate SCK to drive the LTC1408 first and then buffer this signal with the appropriate number of inverters to drive the serial clock input of the processor serial port. Use the falling edge of the clock to latch data from the Serial Data Output (SDO) into your processor serial port. The 14-bit Serial Data will be received right justified, in six 16-bit words with 96 or more clocks per frame sync. If fewer than 6 channels are selected by SEL0–SEL2 for conversion, then 16 clocks are needed per channel to convert the analog inputs and read out the resulting data after the next convert pulse. It is good practice to drive the LTC1408 SCK input first to avoid digital noise interference during the internal bit comparison decision by the internal high speed comparator. Unlike the CONV input, the SCK input is not sensitive to jitter because the input signal is already sampled and held constant.

Serial Data Output (SDO)

Upon power-up, the SDO output is automatically reset to the high impedance state. The SDO output remains in high impedance until a new conversion is started. SDO sends out up to six sets of 14 bits in the output data stream after the third rising edge of SCK after the start of conversion with the rising edge of CONV. The six or fewer 14-bit words are separated by two clock cycles in high impedance mode. Please note the delay specification from SCK to a valid SDO. SDO is always guaranteed to be valid by the next rising edge of SCK. The 16 – 96-bit output data stream is compatible with the 16-bit or 32-bit serial port of most processors.

APPLICATIONS INFORMATION

BOARD LAYOUT AND BYPASSING

Wire wrap boards are not recommended for high resolution and/or high speed A/D converters. To obtain the best performance from the LTC1408, a printed circuit board with ground plane is required. Layout for the printed circuit board should ensure that digital and analog signal lines are separated as much as possible. In particular, care should be taken not to run any digital track alongside an analog signal track. If optimum phase match between the inputs is desired, the length of the twelve input wires of the six input channels should be kept matched. But each pair of input wires to the six input channels should be kept separated by a ground trace to avoid high frequency crosstalk between channels.

High quality tantalum and ceramic bypass capacitors should be used at the V_{CC}, V_{DD} and V_{REF} pins as shown in the Block Diagram on the first page of this data sheet. For optimum performance, a 10µF surface mount tantalum capacitor with a 0.1µF ceramic is recommended for the V_{CC}, V_{DD} and V_{REF} pins. Alternatively, 10µF ceramic chip capacitors such as X5R or X7R may be used. The capacitors must be located as close to the pins as possible. The traces connecting the pins and the bypass capacitors must be kept short and should be made as wide as possible. The V_{CC} and V_{DD} bypass capacitor returns to the ground plane and the V_{REF} bypass capacitor returns to the Pin 22. Care should be taken to place the 0.1µF V_{CC} and V_{DD} bypass capacitor as close to Pins 24 and 25 as possible.

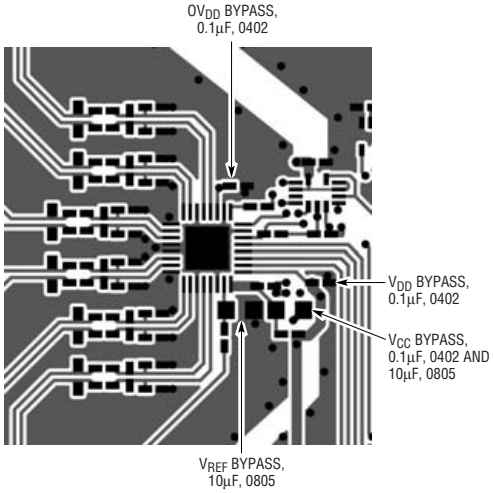


Figure 6. Recommended Layout

Figure 6 shows the recommended system ground connections. All analog circuitry grounds should be terminated at the LTC1408 Exposed Pad. The ground return from the LTC1408 to the power supply should be low impedance for noise-free operation. The Exposed Pad of the 32-pin QFN package is also internally tied to the ground pads. The Exposed Pad should be soldered on the PC board to reduce ground connection inductance. All ground pins (GND, DGND, OGND) must be connected directly to the same ground plane under the LTC1408.

HARDWARE INTERFACE TO TMS320C54x

The LTC1408 is a serial output ADC whose interface has been designed for high speed buffered serial ports in fast digital signal processors (DSPs). Figure 7 shows an example of this interface using a TMS320C54X.

The buffered serial port in the TMS320C54x has direct access to a 2kB segment of memory. The ADC's serial data can be collected in two alternating 1kB segments, in real time, at the full 600ksps conversion rate of the LTC1408. The DSP assembly code sets frame sync mode at the BFSR pin to accept an external positive going pulse and the serial clock at the BCLKR pin to accept an external positive edge clock. Buffers near the LTC1408 may be added to drive long tracks to the DSP to prevent corruption of the signal to LTC1408. This configuration is adequate to traverse a typical system board, but source resistors at the buffer outputs and termination resistors at the DSP, may be needed to match the characteristic impedance of very long transmission lines. If you need to terminate the SDO transmission line, buffer it first with one or two 74ACxx gates. The TTL threshold inputs of the DSP port respond properly to the 3V swing used with the LTC1408.

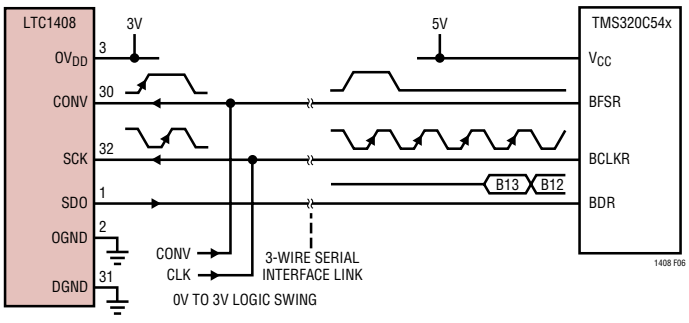
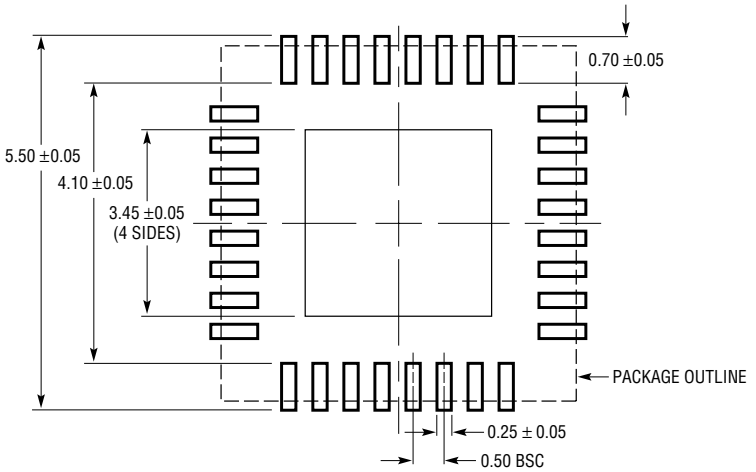
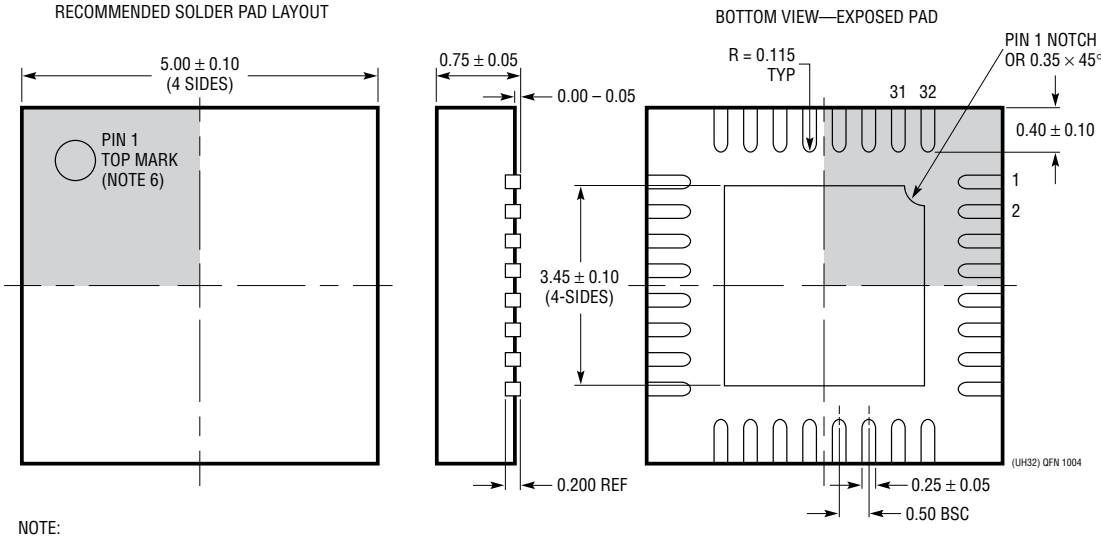


Figure 7. DSP Serial Interface to TMS320C54x

PACKAGE DESCRIPTION

UH Package
32-Lead Plastic QFN (5mm × 5mm)
(Reference LTC DWG # 05-08-1693)





NOTE:
1. DRAWING PROPOSED TO BE A JEDEC PACKAGE OUTLINE
   M0-220 VARIATION WHHD-(X) (TO BE APPROVED)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE
   MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION
   ON THE TOP AND BOTTOM OF PACKAGE

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

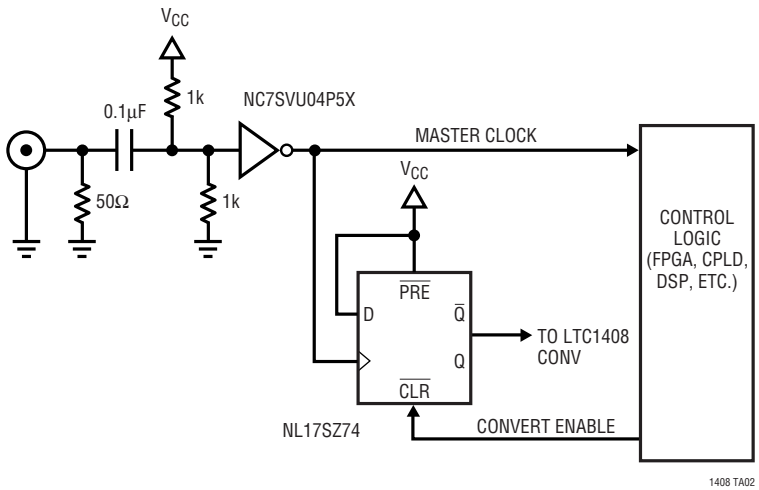
RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
ADCs		
LTC1402	12-Bit, 2.2Msps Serial ADC	5V or ±5V Supply, 4.096V or ±2.5V Span
LTC1403/LTC1403A	12-/14-Bit, 2.8Msps Serial ADC	3V, 15mW, Unipolar Inputs, MSOP Package
LTC1403-1/LTC1403A-1	12-/14-Bit, 2.8Msps Serial ADC	3V, 15mW, Bipolar Inputs, MSOP Package
LTC1405	12-Bit, 5Msps Parallel ADC	5V, Selectable Spans, 115mW
LTC1407/LTC1407A	12-/14-Bit, 3Msps Simultaneous Sampling ADC	3V, 14mW, 2-Channel Unipolar Input Range
LTC1407-1/LTC1407A-1	12-/14-Bit, 3Msps Simultaneous Sampling ADC	3V, 14mW, 2-Channel Bipolar Input Range
LTC1411	14-Bit, 2.5Msps Parallel ADC	5V, Selectable Spans, 80dB SINAD
LTC1412	12-Bit, 3Msps Parallel ADC	±5V Supply, ±2.5V Span, 72dB SINAD
LTC1420	12-Bit, 10Msps Parallel ADC	5V, Selectable Spans, 72dB SINAD
LTC1608	16-Bit, 500ksps Parallel ADC	±5V Supply, ±2.5V Span, 90dB SINAD
LTC1609	16-Bit, 250ksps Serial ADC	5V Configurable Bipolar/Unipolar Inputs
LTC1864/LTC1865 LTC1864L/LTC1865L	16-Bit, 250ksps 1-/2-Channel Serial ADCs	5V or 3V (L-Version), Micropower, MSOP Package
DACs		
LTC1592	16-Bit, Serial SoftSpan™ I_{OUT} DAC	±1LSB INL/DNL, Software Selectable Spans
LTC1666/LTC1667 LTC1668	12-/14-/16-Bit, 50Msps DAC	87dB SFDR, 20ns Settling Time
References		
LT1460-2.5	Micropower Series Voltage Reference	0.10% Initial Accuracy, 10ppm Drift
LT1461-2.5	Precision Voltage Reference	0.04% Initial Accuracy, 3ppm Drift
LT1790-2.5	Micropower Series Reference in SOT-23	0.05% Initial Accuracy, 10ppm Drift

SoftSpan is a trademark of Linear Technology Corporation.

TYPICAL APPLICATION

Clock Squaring/Level Shifting Circuit Allows Testing with RF Sine Generator. Convert Re-Timing Flip-Flop Preserves Low-Jitter Clock Timing



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