3 Volt Single Chip 12-Bit Data Acquisition System

FEATURES

- Single Supply 3.3V or ±3.3V Operation
- Software Programmable Features
  - Unipolar/Bipolar Conversions
  - 4 Differential/8 Single-Ended Inputs
  - Variable Data Word Length
  - Power Shutdown
- Built-In Sample-and-Hold
- Direct 4-Wire Interface to Most MPU Serial Ports and All MPU Parallel Ports
- 25kHz Maximum Throughput Rate
- Available in 20-Lead PDIP and 20-Lead SW Packages

APPLICATIONS

- Minimum Guaranteed Supply Voltage: 2.7V
- Resolution: 12 Bits
- Fast Conversion Time: 26µs Max Over Temp
- Low Supply Currents: 1.0mA

DESCRIPTION

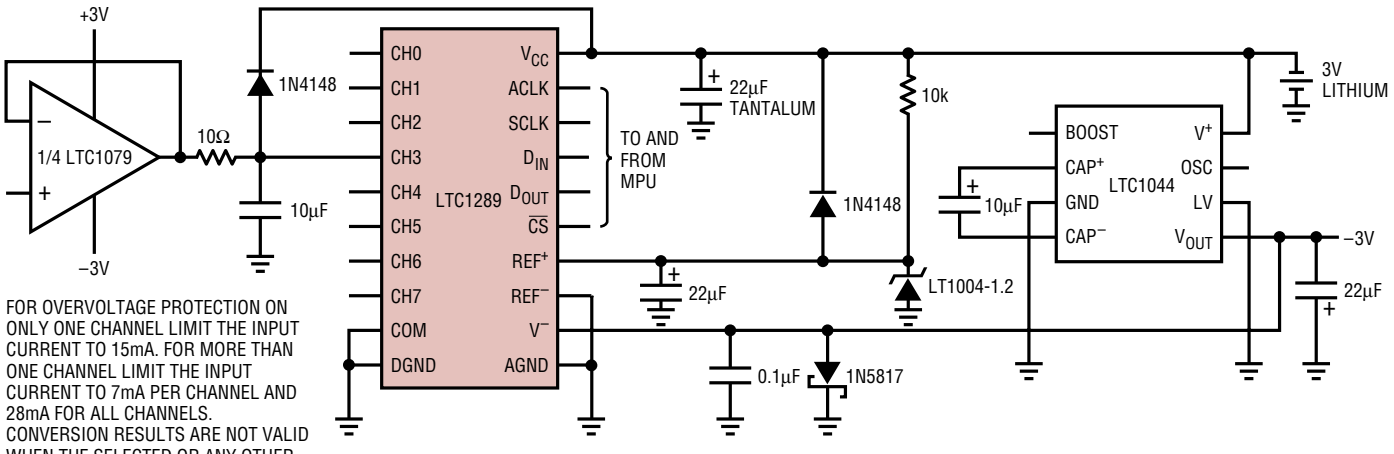
The LTC®1289 is a 3V data acquisition component which contains a serial I/O successive approximation A/D converter. The device specifications are guaranteed at a supply voltage of 2.7V. It uses LTCMOS™ switched capacitor technology to perform a 12-bit unipolar, or 11-bit plus sign bipolar A/D conversion. The 8 channel input multiplexer can be configured for either single-ended or differential inputs (or combinations thereof). An on-chip sample and hold is included for all single-ended input channels. When the LTC1289 is idle it can be powered down in applications where low power consumption is desired.

The serial I/O is designed to be compatible with industry standard full duplex serial interfaces. It allows either MSB- or LSB- first data and automatically provides 2's complement output coding in the bipolar mode. The output data word can be programmed for a length of 8, 12 or 16 bits. This allows easy interface to shift registers and a variety of processors.

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TYPICAL APPLICATION

Single Cell 3V 12-Bit Data Acquisition System



FOR OVERVOLTAGE PROTECTION ON ONLY ONE CHANNEL LIMIT THE INPUT CURRENT TO 15mA. FOR MORE THAN ONE CHANNEL LIMIT THE INPUT CURRENT TO 7mA PER CHANNEL AND 28mA FOR ALL CHANNELS. CONVERSION RESULTS ARE NOT VALID WHEN THE SELECTED OR ANY OTHER CHANNEL IS OVERVOLTAGED ($V_{IN} < V^-$ or $V_{IN} > V_{CC}$).

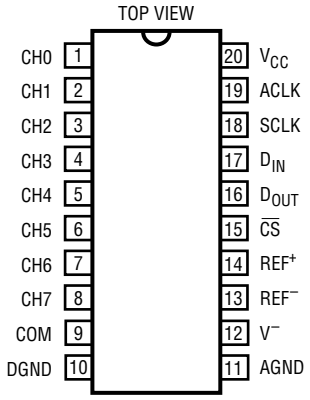
LTC1289 TA01

ABSOLUTE MAXIMUM RATINGS (Notes 1 and 2)

Supply Voltage V_{CC} to GND or V^- 12V
Negative Supply Voltage (V^-) ..... –6V to GND
Voltage
  Analog and Reference Inputs ... (V^-) –0.3V to V_{CC} + 0.3V
  Digital Inputs ..... –0.3V to 12V
  Digital Outputs ..... –0.3V to V_{CC} + 0.3V

Power Dissipation 500mW
Operating Temperature Range
  LTC1289BC, LTC1289CC ..... 0°C to 70°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec.) ..... 300°C

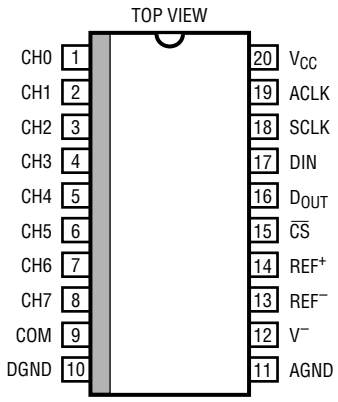
PACKAGE/ORDER INFORMATION



N PACKAGE, 20-LEAD PLASTIC DIP
T_{JMAX} = 110°C, θ_{JA} = 100°C/W (N)

J PACKAGE, 20-LEAD CERAMIC DIP
T_{JMAX} = 150°C, θ_{JA} = 80°C/W (J)

OBSOLETE PACKAGE
Consider the N Package for Alternate Source



SW PACKAGE
20-LEAD PLASTIC SO WIDE
T_{JMAX} = 110°C, θ_{JA} = 150°C/W (SW)

ORDER PART NUMBER		ORDER PART NUMBER
LTC1289BCN LTC1289CCN	LTC1289BIJ LTC1289CIJ LTC1289BCJ LTC1289CCJ	LTC1289BCSW LTC1289CCSW

Order Options Tape and Reel: Add #TR
Lead Free: Add #PBF Lead Free Tape and Reel: Add #TRPBF
Lead Free Part Marking: http://www.linear.com/leadfree/

Consult LTC Marketing for parts specified with wider operating temperature ranges.

CONVERTER AND MULTIPLEXER CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 3)

PARAMETER	CONDITIONS		LTC1289B MIN	LTC1289B TYP	LTC1289B MAX	LTC1289C MIN	LTC1289C TYP	LTC1289C MAX	UNITS
Offset Error	V_{CC} = 2.7V (Note 4)	●			±1.5			±1.5	LSB
Linearity Error (INL)	V_{CC} = 2.7V (Notes 4 and 5)	●			±0.5			±0.5	LSB
Gain Error	V_{CC} = 2.7V (Note 4)	●			±0.5			±1.0	LSB

CONVERTER AND MULTIPLEXER CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 3)

PARAMETER	CONDITIONS		LTC1289B MIN	LTC1289B TYP	LTC1289B MAX	LTC1289C MIN	LTC1289C TYP	LTC1289C MAX	UNITS
Minimum Resolution for Which No Missing Codes are Guaranteed		●			12			12	BITS
Analog and REF Input Range	(Note 7)		(V^-) – 0.05V		V_{CC} + 0.05V	(V^-) – 0.05V		V_{CC} + 0.05V	V
On Channel Leakage Current (Note 8)	On Channel = 3V Off Channel = 0V	●			±1			±1	µA
	On Channel = 0V Off Channel = 3V	●			±1			±1	µA
Off Channel Leakage Current (Note 8)	On Channel = 3V Off Channel = 0V	●			±1			±1	µA
	On Channel = 0V Off Channel = 3V	●			±1			±1	µA

AC CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		LTC1289B/C MIN	LTC1289B/C TYP	LTC1289B/C MAX	UNITS
f_{SCLK}	Shift Clock Frequency	(Note 6)		0		1.0	MHz
f_{ACLK}	A/D Clock Frequency	(Note 6)		(Note 10)		2.0	MHz
t_{ACC}	Delay time from $\overline{CS}$↓ to D_{OUT} Data Valid	(Note 9)			2		ACLK Cycles
t_{SMPL}	Analog Input Sample Time	See Operating Sequence			7		SCLK Cycles
t_{CONV}	Conversion Time	See Operating Sequence			52		ACLK Cycles
t_{CYC}	Total Cycle Time	See Operating Sequence (Note 6)		12 SCLK + 56 ACLK			Cycles
t_{dDO}	Delay Time, SCLK↓ to D_{OUT} Data Valid	See Test Circuits	●		200	350	ns
t_{dis}	Delay Time, $\overline{CS}$↑ to D_{OUT} Hi-Z	See Test Circuits	●		70	150	ns
t_{en}	Delay Time, 2nd ACLK↓ to D_{OUT} Enabled	See Test Circuits	●		130	250	ns
$t_{h\overline{CS}}$	Hold Time, $\overline{CS}$ After Last SCLK↓	(Note 6)		0			ns
t_{hDI}	Hold Time, D_{IN} After SCLK↑	(Note 6)		50			ns
t_{hDO}	Time Output Data Remains Valid After SCLK↓				50		ns
t_f	D_{OUT} Fall Time	See Test Circuits	●		40	100	ns
t_r	D_{OUT} Rise Time	See Test Circuits	●		40	100	ns
t_{suDI}	Setup Time, D_{IN} Stable Before SCLK↑	(Note 6 and 9)		50			ns
$t_{su\overline{CS}}$	Setup Time, $\overline{CS}$↓ Before Clocking in First Address Bit	(Note 6 and 9)		2 ACLK Cycles + 180ns			
$t_{WH\overline{CS}}$	$\overline{CS}$ High Time During Conversion	(Note 6)		52			ACLK Cycles
C_{IN}	Input Capacitance	Analog Inputs On Channel Analog Inputs Off Channel Digital Inputs			100 5 5		pF pF pF

DIGITAL AND DC ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		LTC1289B LTC1289C MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage	V_{CC} = 3.6V	●	2.1			V
V_{IL}	Low Level Input Voltage	V_{CC} = 3.0V	●			0.45	V
I_{IH}	High Level Input Current	V_{IN} = V_{CC}	●			2.5	µA
I_{IL}	Low Level Input Current	V_{IN} = 0V	●			–2.5	µA
V_{OH}	High Level Output Voltage	V_{CC} = 3.0V I_O = 20µA I_O = 400µA	 ● 	 2.7	 2.90 2.85	 	V
V_{OL}	Low Level Output Voltage	V_{CC} = 3.0V I_O = 20µA I_O = 400µA	 ● 	 	 0.05 0.10	 0.3	V
I_{OZ}	High Z Output Leakage	V_{OUT} = V_{CC}, $\overline{CS}$ High V_{OUT} = 0V, $\overline{CS}$ High	● ●			3 –3	µA µA
I_{SOURCE}	Output Source Current	V_{OUT} = 0V			–10		mA
I_{SINK}	Output Sink Current	V_{OUT} = V_{CC}			9		mA
I_{CC}	Positive Supply Current	$\overline{CS}$ High $\overline{CS}$ High, Power Shutdown, ACLK Off	● ●		1.5 1.0	5 10	mA µA
I_{REF}	Reference Current	V_{REF} = 2.5V	●		10	50	µA
I^-	Negative Supply Current	$\overline{CS}$ High	●		1	50	µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All voltage values are with respect to ground with DGND, AGND and REF⁻ wired together (unless otherwise noted).

Note 3: V_{CC} = 3V, V_{REF}+ = 2.5V, V_{REF}– = 0V, V^- = 0V for unipolar mode and –3V for bipolar mode, ACLK = 2.0MHz unless otherwise specified.

Note 4: These specs apply for both unipolar and bipolar modes. In bipolar mode, one LSB is equal to the bipolar input span ($2V_{REF}$) divided by 4096. For example, when V_{REF} = 2.5V, 1LSB(bipolar) = 2(2.5)/4096 = 1.22mV. V^- = –2.7V for bipolar mode.

Note 5: Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

Note 6: Recommended operating conditions.

Note 7: Two on-chip diodes are tied to each analog input which will conduct for analog voltages one diode drop below GND or one diode drop above V_{CC}. Be careful during testing at low V_{CC} levels, as high level analog inputs can cause this input diode to conduct, especially at elevated temperature, and cause errors for inputs near full scale. This spec allows 50mV forward bias of either diode. This means that as long as the analog input does not exceed the supply voltage by more than 50mV, the output code will be correct.

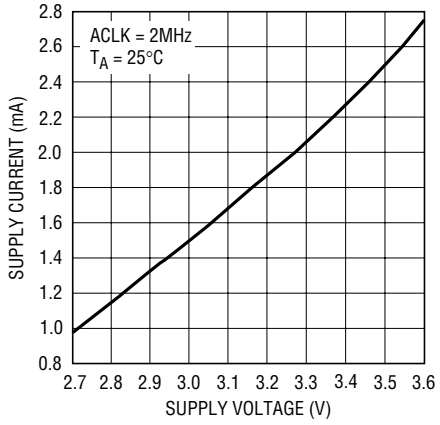
Note 8: Channel leakage current is measured after the channel selection.

Note 9: To minimize errors caused by noise at the chip select input, the internal circuitry waits for two ACLK falling edges after a chip select falling edge is detected before responding to control input signals. Therefore, no attempt should be made to clock an address in or data out until the minimum chip select set-up time has elasped. See Typical Peformance Characteristics curves for additional information ($t_{su\overline{CS}}$ vs V_{CC}).

Note 10: Increased leakage currents at elevated temperatures cause the S/H to droop, therefore it's recommended that $f_{ACLK} \geq$ 125kHz at 85°C and $f_{ACLK} \geq$ 15kHz at 25°C.

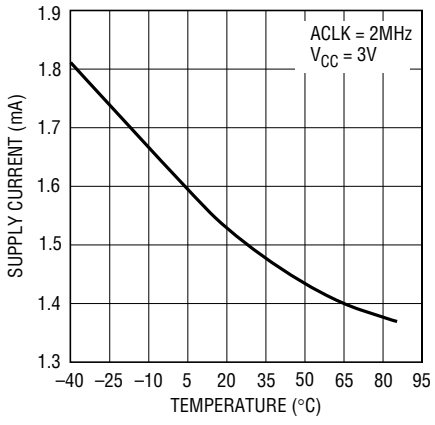
TYPICAL PERFORMANCE CHARACTERISTICS

Supply Current vs Supply Voltage



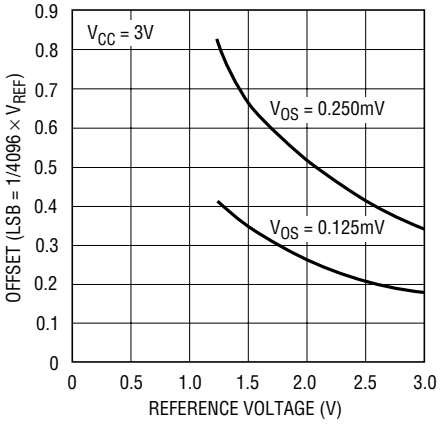
LTC1289 TPC01

Supply Current vs Temperature



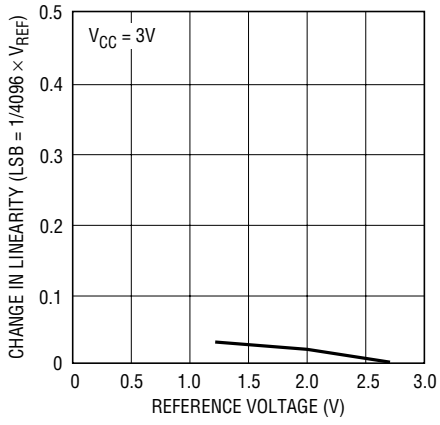
LTC 1289 TPC02

Unadjusted Offset Voltage vs Reference Voltage



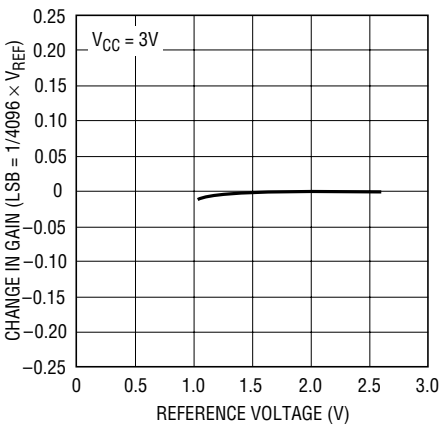
LTC1289 TPC03

Change in Linearity vs Reference Voltage



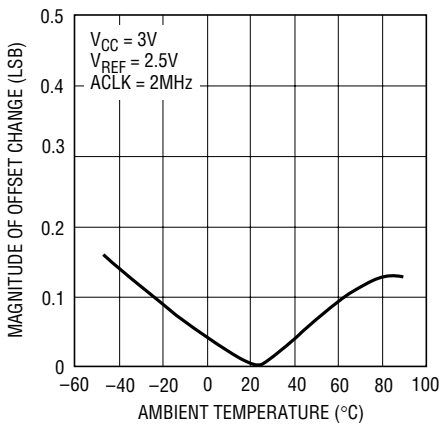
LTC1289 TPC04

Change in Gain vs Reference Voltage



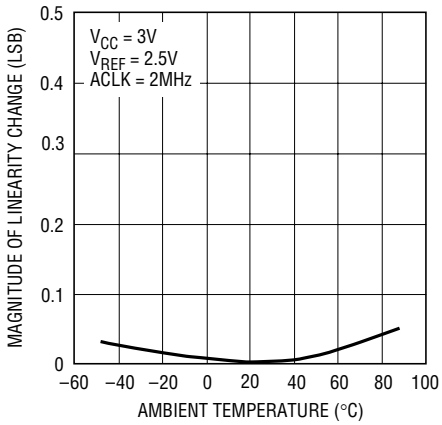
LTC1289 TPC05

Change in Offset vs Temperature



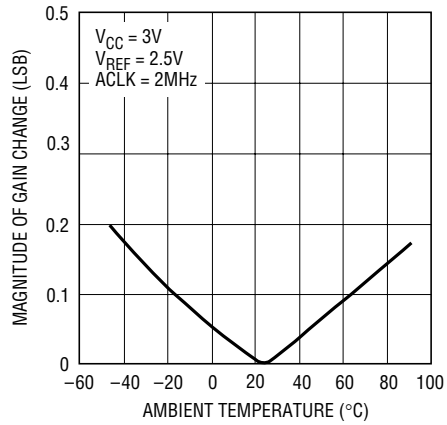
LTC1289 TPC06

Change in Linearity vs Temperature



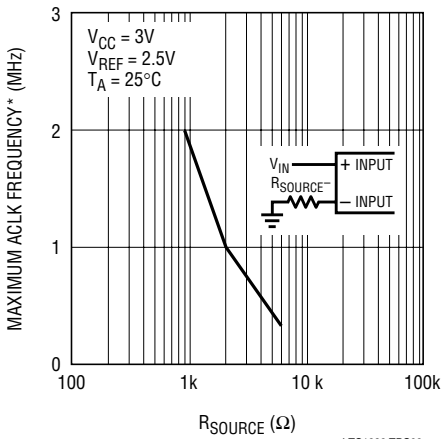
LTC1289 TPC07

Change in Gain vs Temperature



LTC1289 TPC08

Maximum ACLK Frequency vs Source Resistance

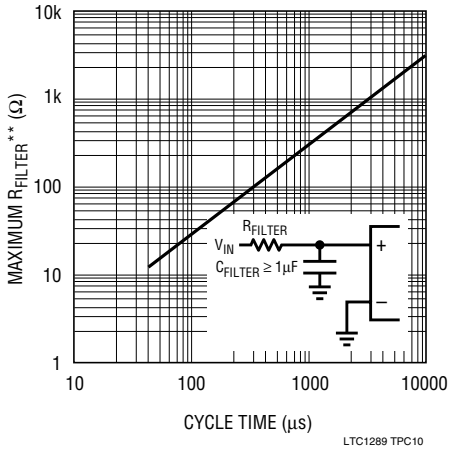


LTC1289 TPC09

* MAXIMUM ACLK FREQUENCY REPRESENTS THE ACLK FREQUENCY AT WHICH A 0.1LSB SHIFT IN THE ERROR AT ANY CODE TRANSITION FROM ITS 2MHZ VALUE IS FIRST DETECTED.

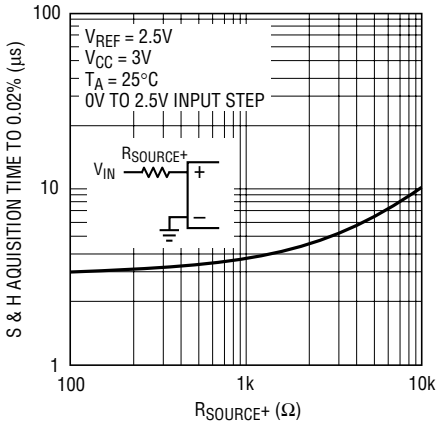
TYPICAL PERFORMANCE CHARACTERISTICS

Maximum Filter Resistor vs Cycle Time



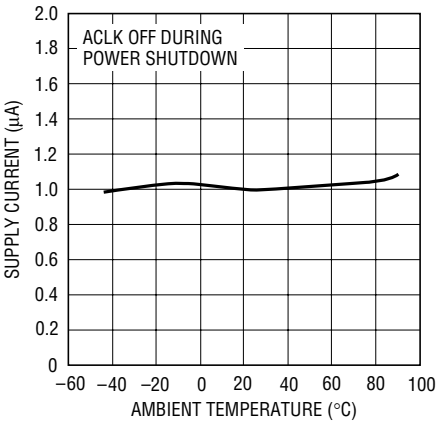
LTC1289 TPC10

Sample and Hold Acquisition Time vs Source Resistance



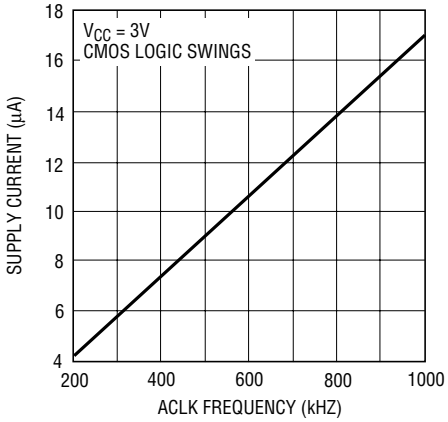
LTC1289 TPC11

Supply Current (Power Shutdown) vs Temperature



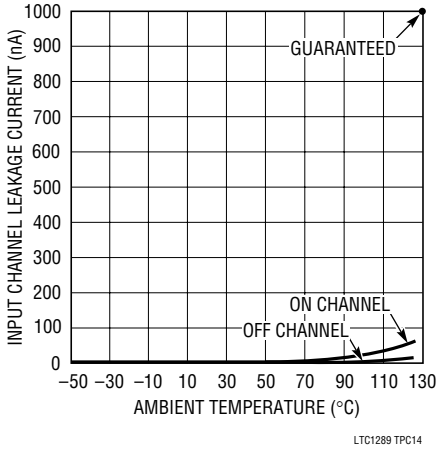
LTC1289 TPC12

Supply Current (Power Shutdown) vs ACLK



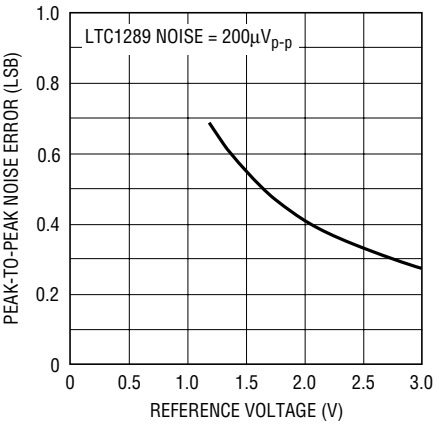
LTC1298 TPC13

Input Channel Leakage Current vs Temperature



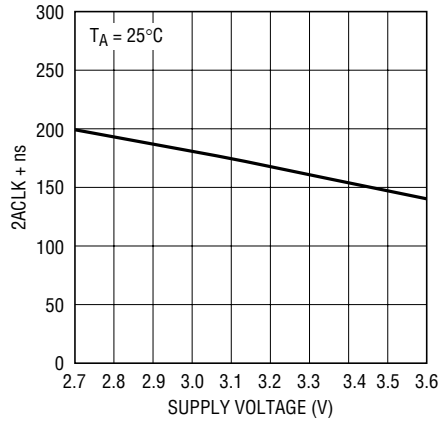
LTC1289 TPC14

Noise Error vs Reference Voltage



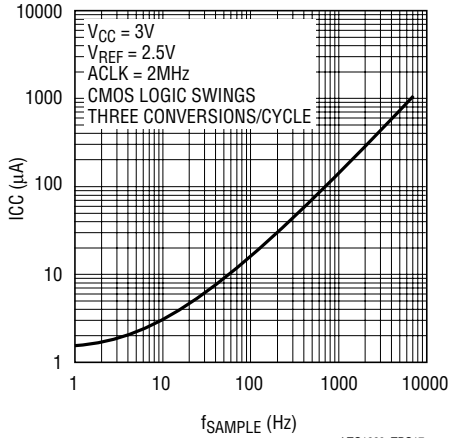
LTC1289 TPC15

$t_{su\overline{CS}}$ vs Supply Voltage



LTC1289 TPC16

Power Consumption with Power Shutdown vs f_{SAMPLE}



LTC1289 TPC17

** MAXIMUM R_{FILTER} REPRESENTS THE FILTER RESISTOR VALUE AT WHICH A 0.1LSB CHANGE IN FULL SCALE ERROR FROM ITS VALUE AT R_{FILTER} = 0 IS FIRST DETECTED.

PIN FUNCTIONS

CH0 – CH7 (Pins 1 – 8): Analog Inputs. The analog inputs must be free of noise with respect to AGND.

COM (Pin 9): Common. The common pin defines the zero reference point for all single-ended inputs. It must be free of noise and is usually tied to the analog ground plane.

DGND (Pin 10): Digital Ground. This is the ground for the internal logic. Tie to the ground plane.

AGND (Pin 11): Analog Ground. AGND should be tied directly to the analog ground plane.

V^- (Pin 12): Negative Supply. Tie V^- to the most negative potential in the circuit. (Ground in single supply applications.)

REF^-, REF^+ (Pins 13,14) Reference Inputs. The reference inputs must be kept free of noise with respect to AGND.

$\overline{CS}$ (Pin 15): Chip Select Input. A logic low on this input enables data transfer.

D_{OUT} (Pin 16): Digital Data Output. The A/D conversion result is shifted out of this output.

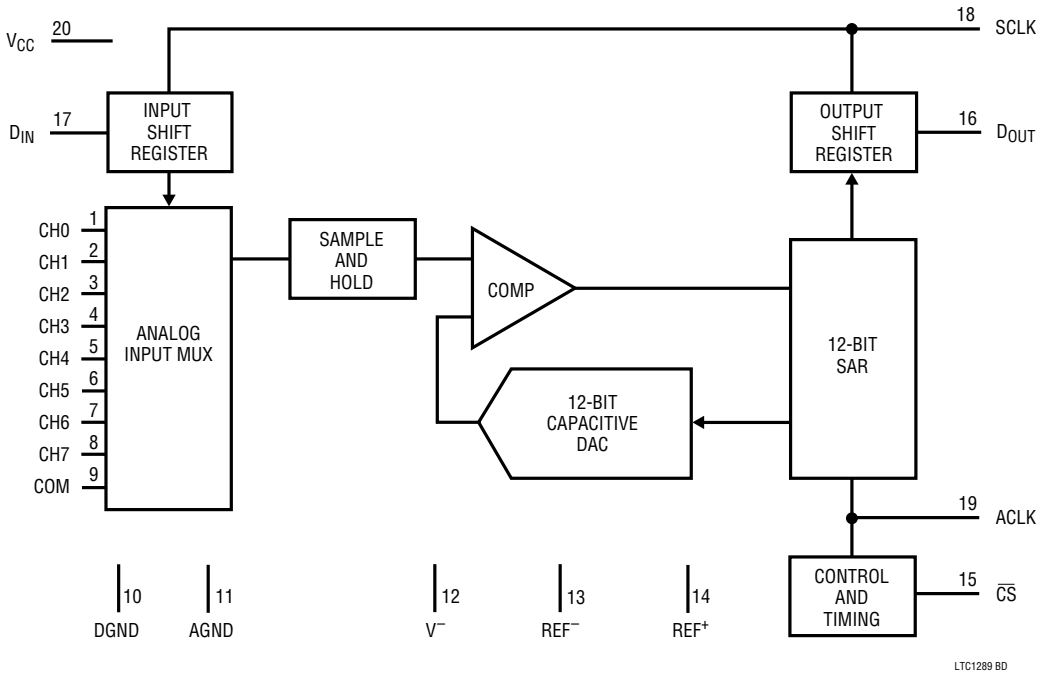
D_{IN} (Pin 17): Digital Input. The A/D configuration word is shifted into this input.

SCLK (Pin 18): Shift Clock. This clock synchronizes the serial data transfer.

ACLK (Pin 19): A/D Conversion Clock. This clock controls the A/D conversion process.

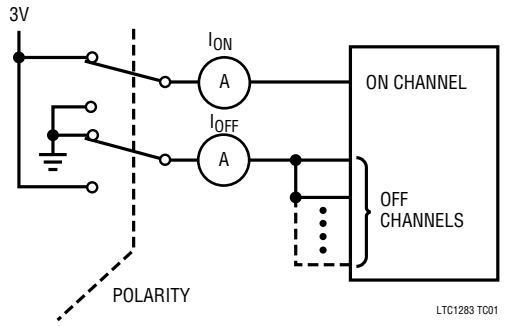
V_{CC} (Pin 20): Positive Supply. This supply must be kept free of noise and ripple by bypassing directly to the analog ground plane.

BLOCK DIAGRAM

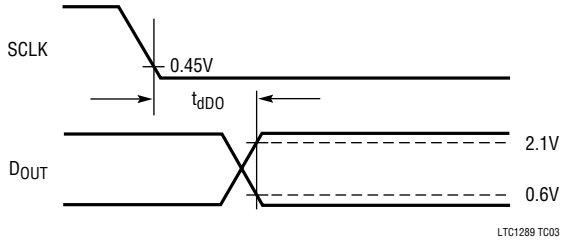


TEST CIRCUITS

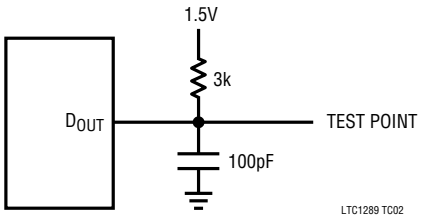
On and Off Channel Leakage Current



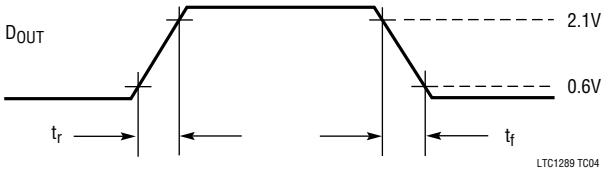
Voltage Waveforms for D_{OUT} Delay Time, t_{dDO}



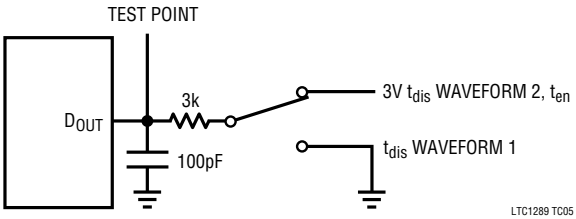
Load Circuit for t_{dDO}, t_r and t_f



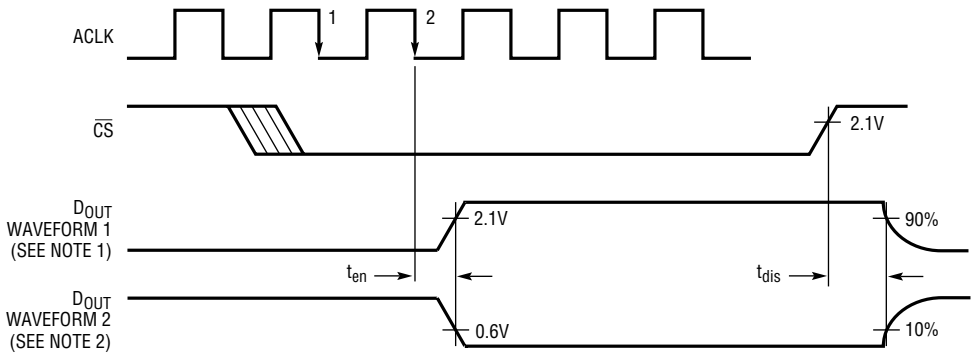
Voltage Waveforms for D_{OUT} Rise and Fall Times, t_r,t_f



Load Circuit for t_{dis} and t_{en}



Voltage Waveforms for t_{en} and t_{dis}



NOTE 1: WAVEFORM 1 IS FOR AN OUTPUT WITH CONDITIONS SUCH THAT THE OUTPUT IS HIGH UNLESS DISABLED BY THE OUTPUT CONTROL.
NOTE 2: WAVEFORM 2 IS FOR AN OUTPUT WITH INTERNAL CONDITIONS SUCH THAT THE OUTPUT IS LOW UNLESS DISABLED BY THE OUTPUT CONTROL.

LTC1289 TC06

APPLICATIONS INFORMATION

The LTC1289 is a data acquisition component which contains the following functional blocks:

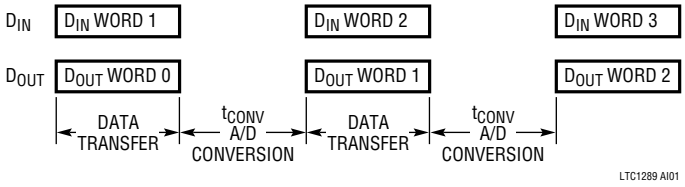
1. 12-bit successive approximation capacitive A/D converter
2. Analog multiplexer (MUX)
3. Sample-and-hold (S/H)
4. Synchronous, full duplex serial interface
5. Control and timing logic

DIGITAL CONSIDERATIONS

Serial Interface

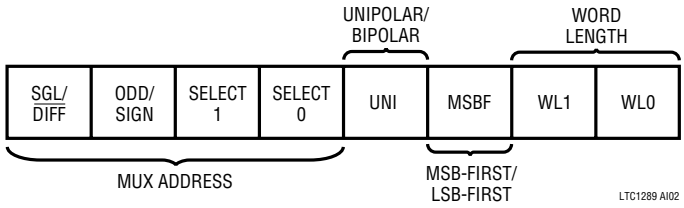
The LTC1289 communicates with microprocessors and other external circuitry via a synchronous, full duplex, four wire serial interface (see Operating Sequence). The shift clock (SCLK) synchronizes the data transfer with each bit being transmitted on the falling SCLK edge and captured on the rising SCLK edge in both transmitting and receiving systems. The data is transmitted and received simultaneously (full duplex).

Data transfer is initiated by a falling chip select ($\overline{CS}$) signal. After the falling $\overline{CS}$ is recognized, an 8-bit input word is shifted into the D_{IN} input which configures the LTC1289 for the next conversion. Simultaneously, the result of the previous conversion is output on the D_{OUT} line. At the end of the data exchange the requested conversion begins and $\overline{CS}$ should be brought high. After t_{CONV}, the conversion is complete and the results will be available on the next data transfer cycle. As shown below, the result of a conversion is delayed by one $\overline{CS}$ cycle from the input word requesting it.

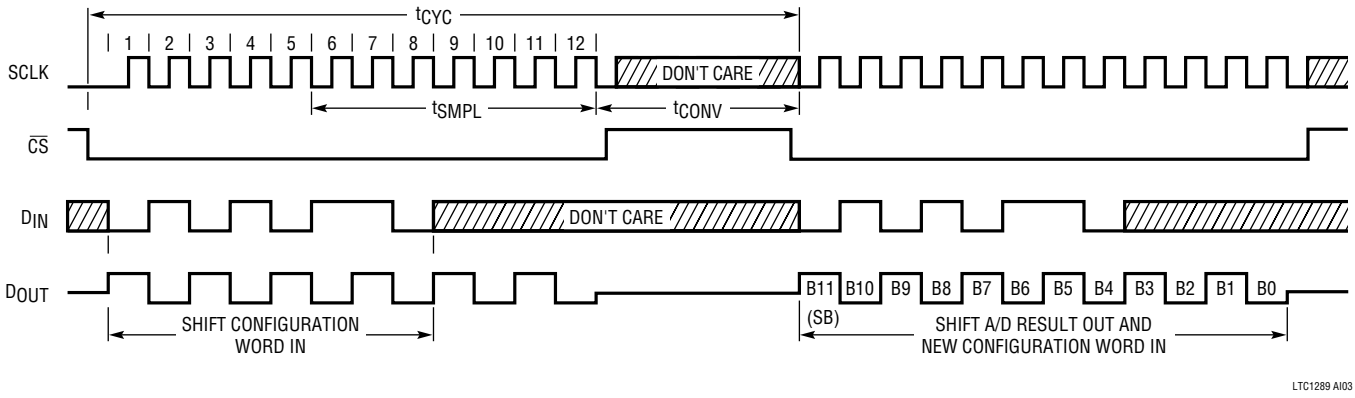


Input Data Word

The LTC1289 8-bit data word is clocked into the D_{IN} input on the first eight rising SCLK edges after chip select is recognized. Further inputs on the D_{IN} pin are then ignored until the next $\overline{CS}$ cycle. The eight bits of the input word are defined as follows:



Operating Sequence
(Example: Differential Inputs (CH3-CH2), Bipolar, MSB-First and 12-Bit Word Length)



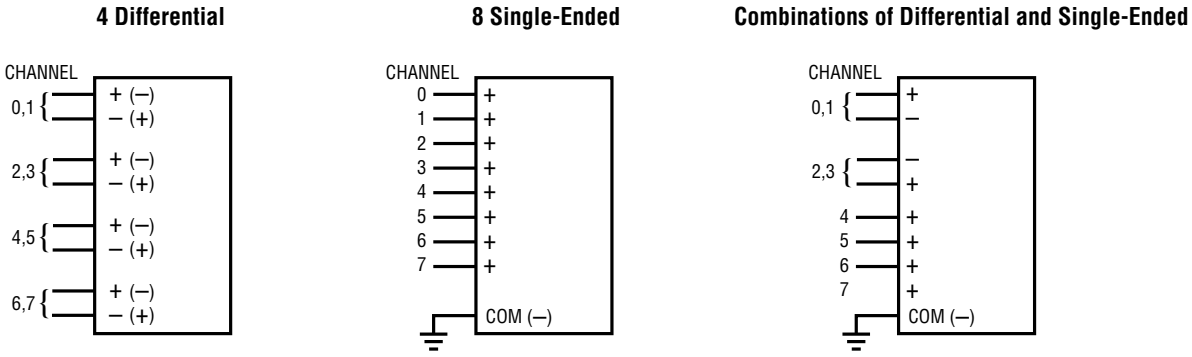
APPLICATIONS INFORMATION

MUX Address

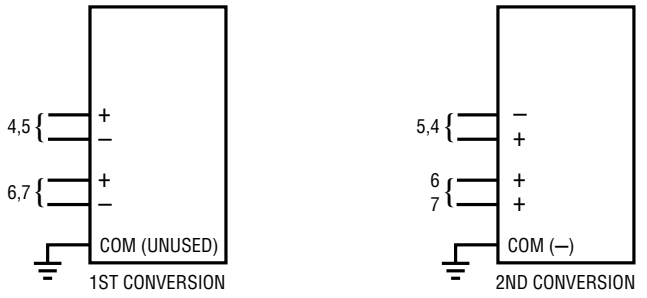
The first four bits of the input word assign the MUX configuration for the requested conversion. For a given channel selection, the converter will measure the voltage between the two channels indicated by the + and – signs in the selected row of Table 1. Note that in differential mode (SGL/$\overline{\text{DIFF}}$ = 0) measurements are limited to four adjacent input pairs with either polarity. In single-ended mode, all input channels are measured with respect to COM.

Table 1. Multiplexer Channel Selection

MUX ADDRESS			DIFFERENTIAL CHANNEL SELECTION								MUX ADDRESS			SINGLE-ENDED CHANNEL SELECTION							
SGL/$\overline{\text{DIFF}}$	ODD SIGN	SELECT 1 0	0	1	2	3	4	5	6	7	SGL/$\overline{\text{DIFF}}$	ODD SIGN	SELECT 1 0	0	1	2	3	4	5	6	7	COM
0	0	0 0	+	–							1	0	0 0	+								–
0	0	0 1			+	–					1	0	0 1			+						–
0	0	1 0					+	–			1	0	1 0					+				–
0	0	1 1							+	–	1	0	1 1							+		–
0	1	0 0	–	+							1	1	0 0		+							–
0	1	0 1			–	+					1	1	0 1				+					–
0	1	1 0					–	+			1	1	1 0						+			–
0	1	1 1							–	+	1	1	1 1								+	–



Changing the MUX Assignment "On the Fly"



LTC1289 AIF01

Figure 1. Examples of Multiplexer Options on the LTC1289

APPLICATIONS INFORMATION

Unipolar/Bipolar (UNI)

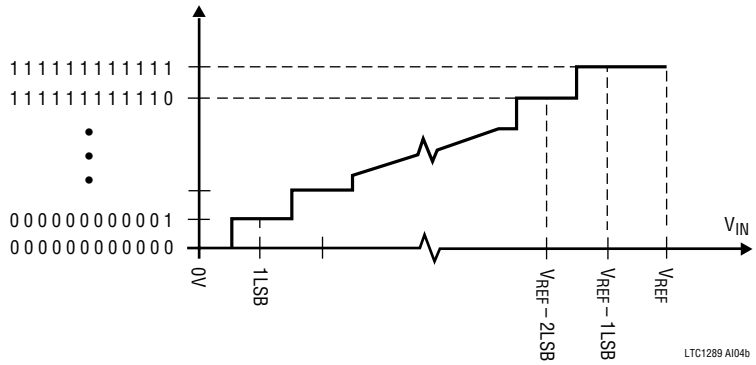
The fifth input bit (UNI) determines whether the conversion will be unipolar or bipolar. When UNI is a logical one, a unipolar conversion will be performed on the selected input voltage. When UNI is a logical zero, a bipolar conversion will result. The input span and code assignment for each conversion type are shown in the figures below.

Unipolar Output Code (UNI = 1)

OUTPUT CODE	INPUT VOLTAGE	INPUT VOLTAGE (V_{REF} = 2.5V)
1 1 1 1 1 1 1 1 1 1 1 1	V_{REF} – 1LSB	2.4994V
1 1 1 1 1 1 1 1 1 1 1 0	V_{REF} – 2LSB	2.4988V
•	•	•
•	•	•
•	•	•
0 0 0 0 0 0 0 0 0 0 0 1	1LSB	0.0006V
0 0 0 0 0 0 0 0 0 0 0 0	0V	0V

LTC1289 AI04a

Unipolar Transfer Curve (UNI = 1)



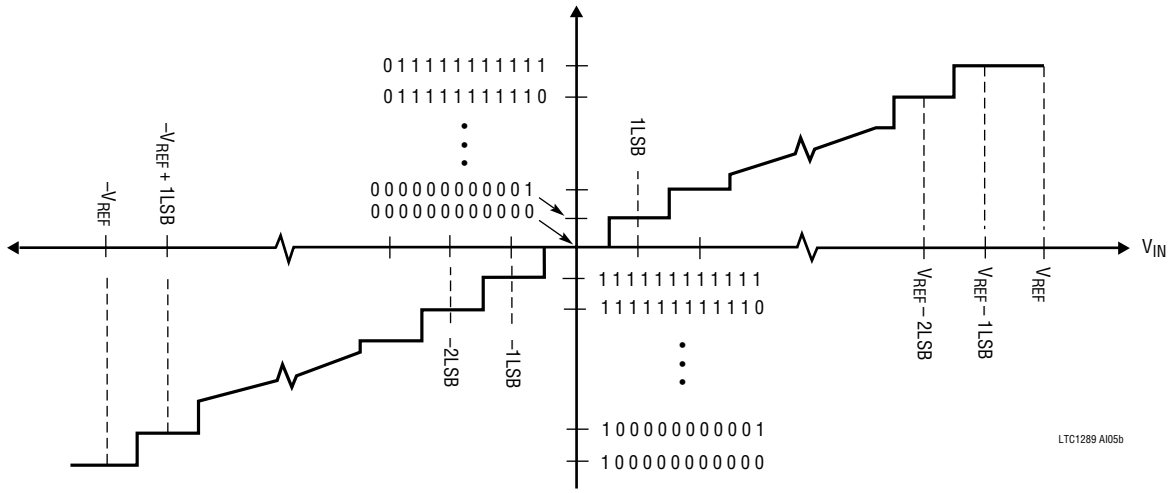
LTC1289 AI04b

Bipolar Output Code (UNI = 0)

OUTPUT CODE	INPUT VOLTAGE	INPUT VOLTAGE (V_{REF} = 2.5V)	OUTPUT CODE	INPUT VOLTAGE	INPUT VOLTAGE (V_{REF} = 2.5V)
0 1 1 1 1 1 1 1 1 1 1 1	V_{REF} – 1LSB	2.4988V	1 1 1 1 1 1 1 1 1 1 1 1	–1LSB	–0.0012V
0 1 1 1 1 1 1 1 1 1 1 0	V_{REF} – 2LSB	2.4976V	1 1 1 1 1 1 1 1 1 1 1 0	–2LSB	–0.0024V
•	•	•	•	•	•
•	•	•	•	•	•
•	•	•	•	•	•
0 0 0 0 0 0 0 0 0 0 0 1	1LSB	0.0012V	1 0 0 0 0 0 0 0 0 0 0 1	$-(V_{REF})$ + 1LSB	–2.4988V
0 0 0 0 0 0 0 0 0 0 0 0	0V	0V	1 0 0 0 0 0 0 0 0 0 0 0	$-(V_{REF})$	–2.5000V

LTC1289 AI05a

Bipolar Transfer Curve (UNI = 0)



LTC1289 AI05b

APPLICATIONS INFORMATION

The following discussion will demonstrate how the two reference pins are to be used in conjunction with the analog input multiplexer. In unipolar mode the input span of the A/D is set by the difference in voltage on the REF^+ pin and the REF^- pin. In the bipolar mode the input span is twice the difference in voltage on the REF^+ pin and the REF^- pin. In the unipolar mode the lower value of the input span is set by the voltage on the COM pin for single-ended inputs and by the voltage on the minus input pin for differential inputs. For the bipolar mode of operation the voltage on the COM pin or the minus input pin sets the center of the input span.

The upper and lower value of the input span can now be summarized in the following table:

INPUT CONFIGURATION		UNIPOLAR MODE	BIPOLAR MODE
Single-Ended	Lower Value	COM	$-(REF^+ - REF^-) + COM$
	Upper Value	$(REF^+ - REF^-) + COM$	$(REF^+ - REF^-) + COM$
Differential	Lower Value	IN^-	$-(REF^+ - REF^-) + IN^-$
	Upper Value	$(REF^+ - REF^-) + IN^-$	$(REF^+ - REF^-) + IN^-$

The reference voltages REF^+ and REF^- can fall between V_{CC} and V^-, but the difference ($REF^+ - REF^-$) must be less than or equal to V_{CC}. The input voltages must be less than or equal to V_{CC} and greater than or equal to V^-.

The following examples are for a single-ended input configuration.

Example 1: Let V_{CC} = 3.3V, V^- = 0V, REF^+ = 3V, REF^- = 1V and COM = 0V. Unipolar mode of operation. The resulting input span is $0V \le IN^+ \le 2V$.

Example 2: The same conditions as Example 1 except COM = 1V. The resulting input span is $1V \le IN^+ \le 3V$. Note if $IN^+ \ge 3V$ the resulting D_{OUT} word is all 1's. If $IN^+ \le 1V$ then the resulting D_{OUT} word is all 0's.

Example 3: Let V_{CC} = 3.3V, V^- = –3.3V, REF^+ = 3V, REF^- = 1V and COM = 1V. Bipolar mode of operation. The resulting input span is $-1V \le IN+ \le 3V$.

For differential input configurations with the same conditions as in the above three examples the resulting input spans are as follows:

Example 1 (Diff.): $IN^- \le IN^+ \le IN^- + 2V$

Example 2 (Diff.): $IN^- \le IN^+ \le IN^- + 2V$

Example 3 (Diff.): $IN^- - 2V \le IN^+ \le IN^- + 2V$.

MSB-First/LSB-First Format (MSBF)

The output data of the LTC1289 is programmed for MSB-first or LSB-first sequence using the MSBF bit. For MSB-first output data, the input word clocked to the LTC1289 should always contain a logical one in the sixth bit location (MSBF bit). Likewise for LSB-first output data the input word clocked to the LTC1289 should always contain a zero in the MSBF bit location. The MSBF bit affects only the order of the output data word. The order of the input word is unaffected by this bit.

MSBF	OUTPUT FORMAT
0	LSB-First
1	MSB-First

LTC1289 AI06

Word Length (WL1, WL0) and Power Shutdown

The last two bits of the input word (WL1 and WL0) program the output data word length and the power shutdown feature of the LTC1289. Word lengths of 8, 12 or 16 bits can be selected according to the following table.

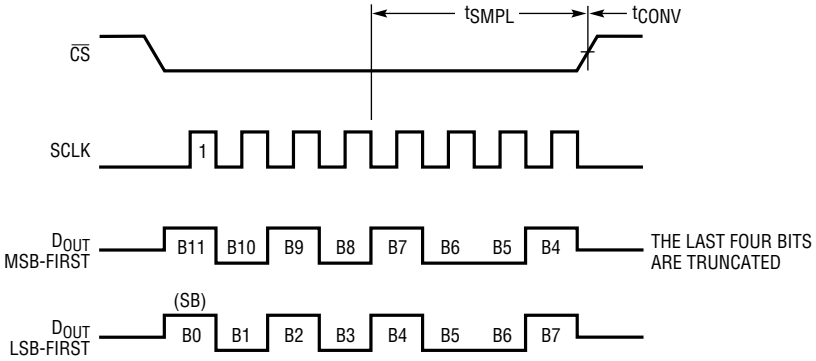
WL1	WL0	OUTPUT WORD LENGTH
0	0	8 Bits
0	1	Power Shutdown
1	0	12 Bits
1	1	16 Bits

LTC1289 AI07

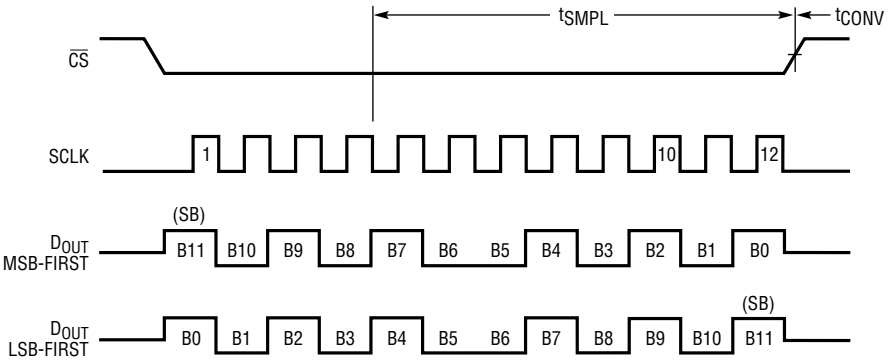
The WL1 and WL0 bits in a given D_{IN} word control the length of the present, not the next, D_{OUT} word. WL1 and WL0 are never "don't cares" and must be set for the correct D_{OUT} word length even when a "dummy" D_{IN} word is sent. On any transfer cycle, the word length should be made equal to the number of SCLK cycles sent by the MPU. Power down will occur when WL1 = 0 and WL0 = 1 is selected. The previous result will be clocked out as a 10 bit word so a "dummy"conversion is required before powering down the LTC1289. Conversions are resumed once $\overline{CS}$ goes low or an SCLK is applied, if $\overline{CS}$ is already low.

APPLICATIONS INFORMATION

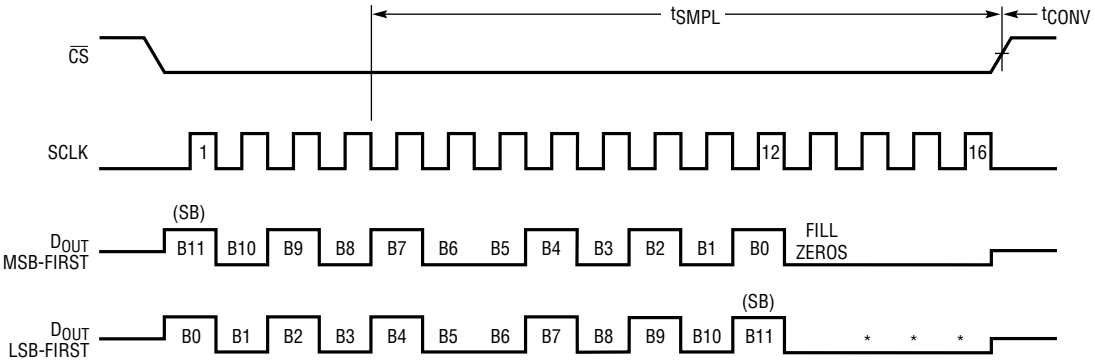
8-Bit Word Length



12-Bit Word Length



16-Bit Word Length



* IN UNIPOLAR MODE, THESE BITS ARE FILLED WITH ZEROS.
IN BIPOLAR MODE, THE SIGN BIT IS EXTENDED INTO THESE LOCATIONS.

LTC1289 AIF02

Figure 2. Data Output (D_{OUT}) Timing with Different Word Lengths

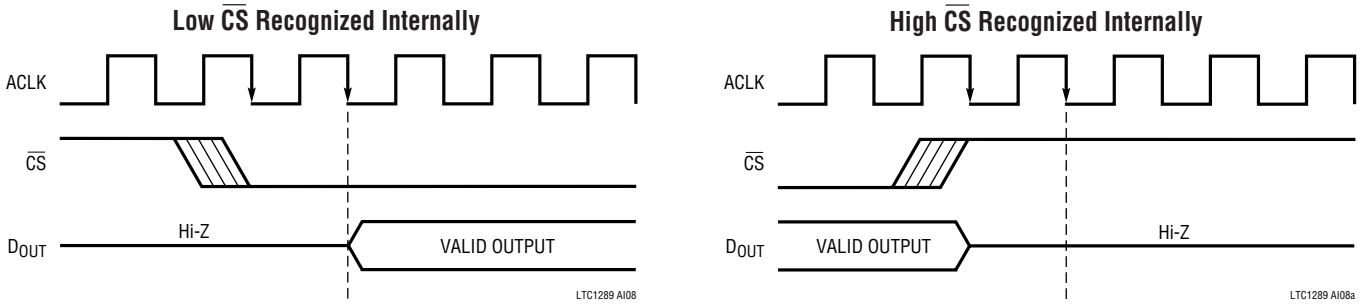
APPLICATIONS INFORMATION

Deglitcher

A deglitching circuit has been added to the Chip Select input of the LTC1289 to minimize the effects of errors caused by noise on that input. This circuit ignores changes in state on the $\overline{CS}$ input that are shorter in duration than one ACLK cycle. After a change of state on the $\overline{CS}$ input, the LTC1289 waits for two falling edge of the ACLK before recognizing a valid chip select. One indication of $\overline{CS}$ recognition is the D_{OUT} line becoming active (leaving the Hi-Z state). Note that the deglitching applies to both the rising and falling $\overline{CS}$ edges.

$\overline{CS}$ Low During Conversion

In the normal mode of operation, $\overline{CS}$ is brought high during the conversion time. The serial port ignores any SCLK activity while $\overline{CS}$ is high. The LTC1289 will also operate with $\overline{CS}$ low during the conversion. In this mode, SCLK must remain low during the conversion as shown in the following figure. After the conversion is complete, the D_{OUT} line will become active with the first output bit. Then the data transfer can begin as normal.



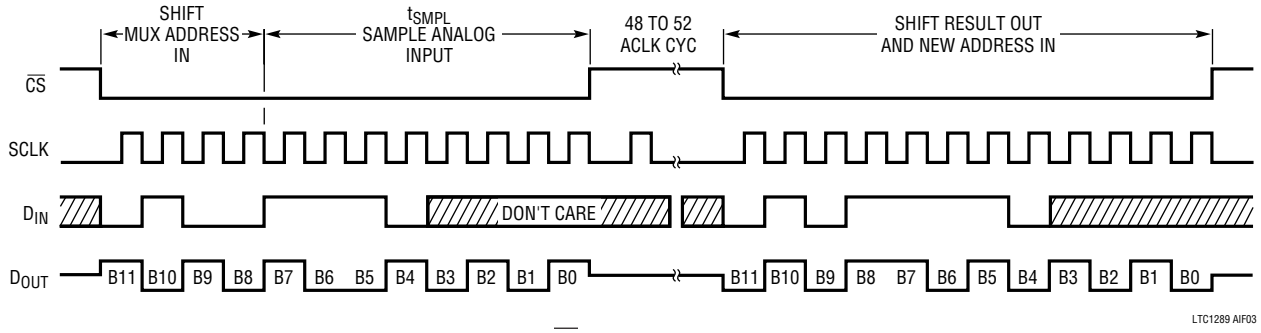


Figure 3. $\overline{CS}$ High During Conversion

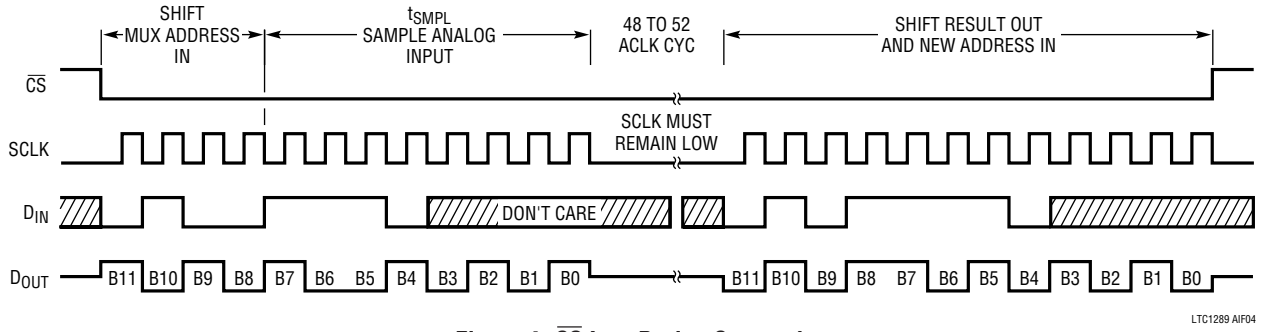


Figure 4. $\overline{CS}$ Low During Conversion

APPLICATIONS INFORMATION

Logic Levels

The logic level standards for this supply range have not been well defined. What standards that do exist are not universally accepted. The trip point on the logic inputs of the LTC1289 is $0.28 \times V_{CC}$. This makes the logic inputs compatible with HC type logic levels and processors that are specified at 3.3V. The output D_{OUT} is also compatible with the above standards. The following summarizes such levels.

V_{OH} (no load)	V_{CC} - 0.1V
V_{OL} (no load)	0.1V
V_{OH}	$0.9 \times V_{CC}$
V_{OL}	$0.1 \times V_{CC}$
V_{IH}	$0.7 \times V_{CC}$
V_{IL}	$0.2 \times V_{CC}$

The LTC1289 can be driven with 5V logic even when V_{CC} is at 3.3V. This is due to a unique input protection device that is found on the LTC1289.

Microprocessor Interfaces

The LTC1289 can interface directly (without external hardware) to most popular microprocessor (MPU) synchronous serial formats. If an MPU without a serial interface is used, then four of the MPU's parallel port lines can be programmed to form the serial link to the LTC1289. Many of the popular MPU's can operate with 3V supplies. For example the MC68HC11 is an MPU with a serial format (SPI). Likewise parallel MPU's that have the 8051 type architecture are also capable of operating at this voltage range. The code for these processors remains the same and can be found in the LTC1290 datasheet or application notes AN36A and AN36B.

Sharing the Serial Interface

The LTC1289 can share 3-wire serial interface with other peripheral components or other LTC1289s (See Figure 5). In this case, the $\overline{CS}$ signals decide which LTC1289 is being addressed by the MPU.

ANALOG CONSIDERATIONS

1. Grounding

The LTC1289 should be used with an analog ground plane and single point grounding techniques.

Pin 11 (AGND) should be tied directly to this ground plane.

Pin 10 (DGND) can also be tied directly to this ground plane because minimal digital noise is generated within the chip itself.

Pin 20 (V_{CC}) should be bypassed to the ground plane with a 22µF tantalum with leads as short as possible. Pin 12 (V^-) should be bypassed with a 0.1µF ceramic disk. For single supply applications, V^- can be tied to the ground plane.

It is also recommended that pin 13 (REF^-) and pin 9 (COM) be tied directly to the ground plane. All analog inputs should be referenced directly to the single point ground. Digital inputs and outputs should be shielded from and/or routed away from the reference and analog circuitry.

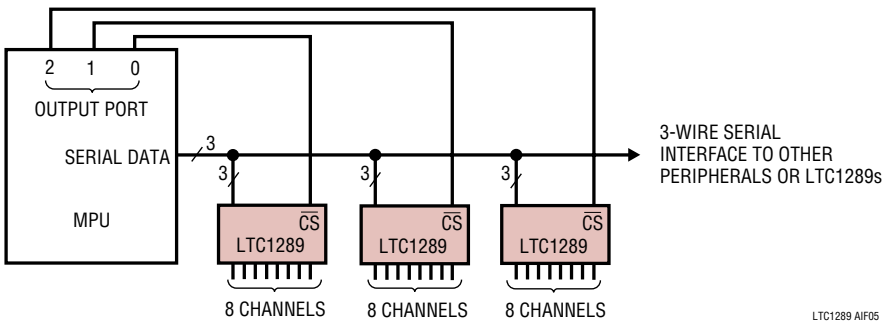


Figure 5. Several LTC1289s Sharing One 3-Wire Serial Interface

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Figure 6 shows an example of an ideal ground plane design for a two-sided board. Of course, this much ground plane will not always be possible, but users should strive to get as close to this ideal as possible.

2. Bypassing

For good performance, V_{CC} must be free of noise and ripple. Any changes in the V_{CC} voltage with respect to analog ground during a conversion cycle can induce errors or noise in the output code. V_{CC} noise and ripple can be kept below 0.5mV by bypassing the V_{CC} pin directly to the analog ground plane with a 22µF tantalum capacitor and leads as short as possible. The lead from the device to the V_{CC} supply should also be kept to a minimum and the V_{CC} supply should have a low output impedance such as that obtained from a voltage regulator (e.g., LT1117). Using a battery to power the LTC1289 will help reduce the amount of bypass capacitance required on the V_{CC} pin. A battery placed close to the device will only require 10µF to adequately bypass the supply pin. Figure 7 shows the effect of poor V_{CC} bypassing. Figure 8a shows the settling of a LT1117 low dropout regulator with a 22µF bypass capacitor. The noise and ripple is approximately 0.5mV. Figure 8b shows the response of a lithium battery with a 10µF bypass capacitor. The noise and ripple is kept below 0.5mV.

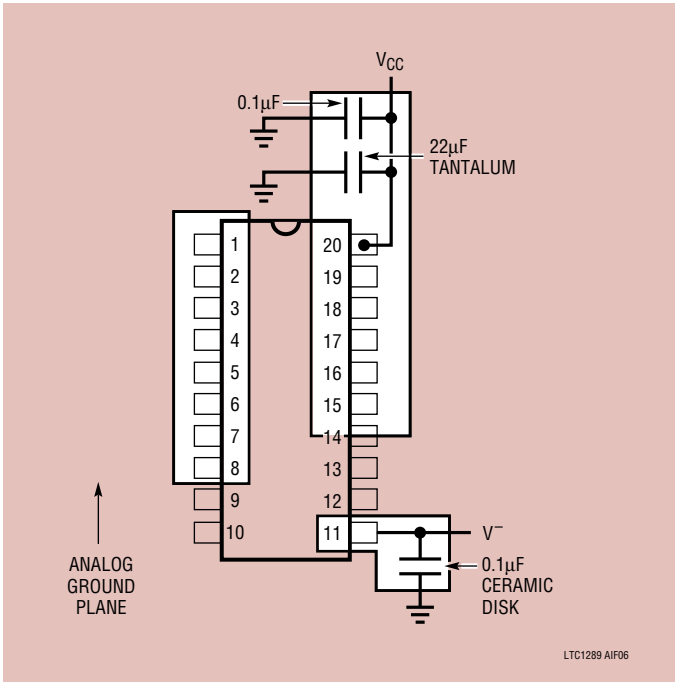


Figure 6. Example Ground Plane for the LTC1289

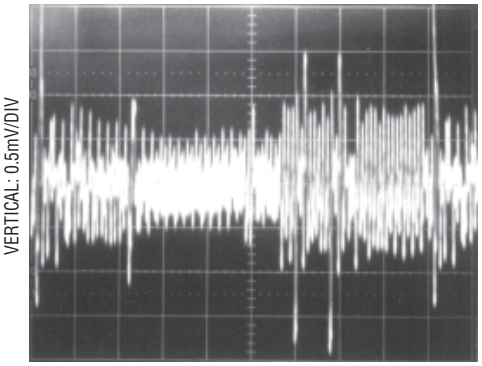


Figure 7. Poor V_{CC} Bypassing. Noise and Ripple Can Cause A/D Errors.

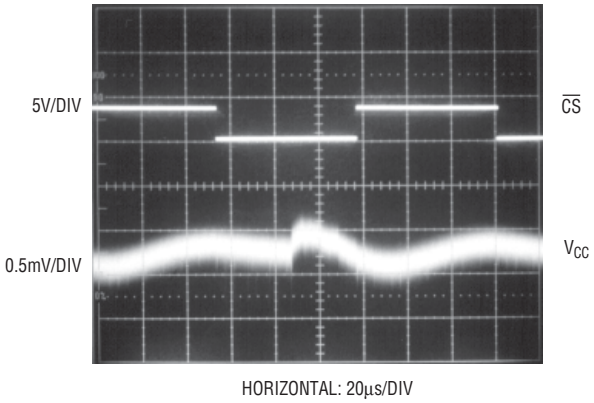


Figure 8a. LT1117 Regulator with 22µF Bypassing on V_{CC}

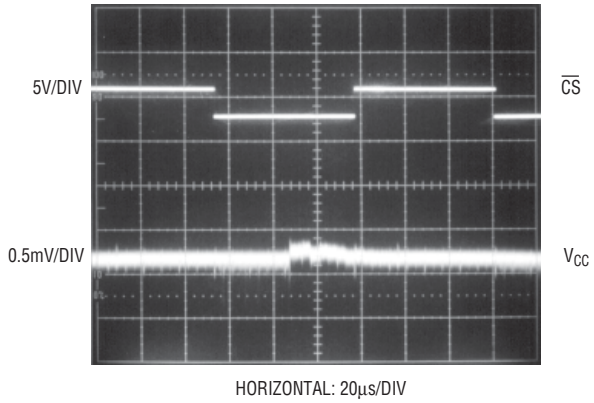


Figure 8b. Lithium Battery with 10µF Bypassing on V_{CC}

APPLICATIONS INFORMATION

3. Analog Inputs

Because of the capacitive redistribution A/D conversion techniques used, the analog inputs of the LTC1289 have capacitive switching input current spikes. These current spikes settle quickly and do not cause a problem. However, if large source resistances are used or if slow settling op amps drive the inputs, care must be taken to insure that the transients caused by the current spikes settle completely before the conversion begins.

Source Resistance

The analog inputs of the LTC1289 look like a 100pF capacitor (C_{IN}) is series with a 1500Ω resistor (R_{ON}) as shown in Figure 9. This value for R_{ON} is for V_{CC} = 2.7V. With larger supply voltages R_{ON} will be reduced. For example with V_{CC} = 2.7V and V^- = –2.7V R_{ON} becomes 500Ω. C_{IN} gets switched between the selected "+" and "–" inputs once during each conversion cycle. Large external source resistors and capacitances will slow the settling of the inputs. It is important that the overall RC time constants be short enough to allow the analog inputs to completely settle within the allotted time.

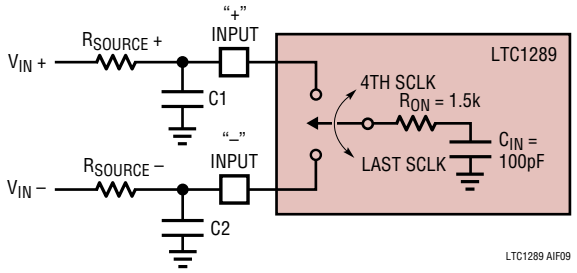


Figure 9. Analog Input Equivalent Circuit

"+" Input Settling

This input capacitor is switched onto the "+" input during the sample phase (t_{SMPL}, see Figure 10). The sample phase starts at the 4th SCLK cycle and lasts until the falling edge of the last SCLK (the 8th, 12th or 16th SCLK cycle depending on the selected word length). The voltage on the "+" input must settle completely within this sample time. Minimizing R_{SOURCE}^+ and C1 will improve the input settling time. If large "+" input source resistance must be used, the sample time can be increased by using a slower SCLK frequency or selecting a longer word length. With the minimum possible sample time of 4µs, **R_{SOURCE}^+ < 2k and C1 < 20pF will provide adequate settling**.

"–" Input Settling

At the end of the sample phase the input capacitor switches to the "–" input and the conversion starts (see Figure 10). During the conversion, the "+" input voltage is effectively "held" by the sample and hold and will not affect the conversion result. However, it is critical that the "–" input voltage be free of noise and settle completely during the first four ACLK cycles of the conversion time. Minimizing R_{SOURCE}^- and C2 will improve settling time. If large "–" input source resistance must be used, the time allowed for

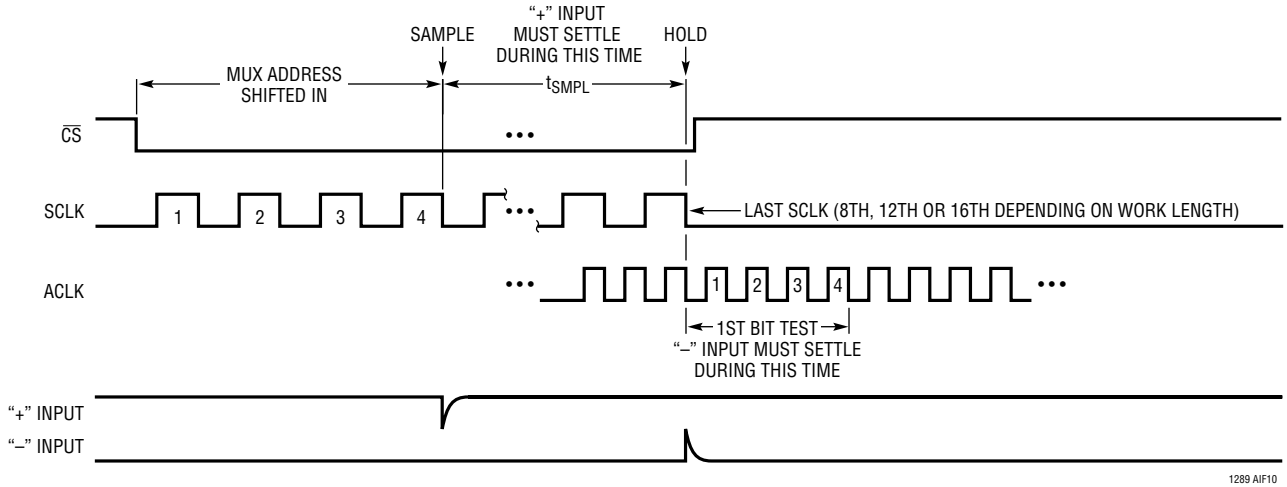


Figure 10. "+" and "–" Input Settling Windows

APPLICATIONS INFORMATION

settling can be extended by using a slower ACLK frequency. At the maximum ACLK rate of 2MHz, **R_{SOURCE} < 200Ω and C2 < 20pF will provide adequate settling.**

Input Op Amps

When driving the analog inputs with an op amp it is important that the op amp settle within the allowed time (see Figure 10). Again, the "+" and "–" input sampling times can be extended as described above to accommodate slower op amps. For single supply low voltage applications the LT1006, LT1013 and LT1014 can be made to settle well even with the minimum settling windows of 4µs ("+" input) and 2µs ("–" input) which occur at the maximum clock rates (ACLK = 2MHz and SCLK = 1MHz). Figures 11 and 12 show examples of adequate and poor op amp settling. The LT1077, LT1078 or LT1079 can be used here to reduce power consumption. Placing an RC network at the output of the op amps will improve the settling response and also reduce the broadband noise.

RC Input Filtering

It is possible to filter the inputs with an RC network as shown in Figure 13. For large values of C_F (e.g., 1µF), the capacitive input switching currents are averaged into a net DC current. Therefore, a filter should be chosen with a small resistor and large capacitor to prevent DC drops across the resistor. The magnitude of the DC current is approximately $I_{DC} = 100pF \times V_{IN}/t_{CYC}$ and is roughly proportional to V_{IN}. When running at the minimum cycle time of 40µs, the input current equals 6.3µA at V_{IN} = 2.5V. In this case, a filter resistor of 10Ω will cause 0.1LSB of full-scale error. If a larger filter resistor must be used, errors can be eliminated by increasing the cycle time as shown in the typical curve of Maximum Filter Resistor vs Cycle Time.

Input Leakage Current

Input leakage currents can also create errors if the source resistance gets too large. For instance, the maximum input leakage specification of 1µA (at 85°C) flowing through a source resistance of 1kΩ will cause a voltage drop of 1mV or 1.6LSB with V_{REF} = 2.5V. This error will be much reduced at lower temperatures because leakage drops rapidly (see typical curve of Input Channel Leakage Current vs Temperature).

Noise Coupling Into Inputs

High source resistance input signals (>500Ω) are more sensitive to coupling from external sources. It is preferable to use channels near the center of the package (i.e., CH2-CH7) for signals which have the highest output resistance because they are essentially shielded by the

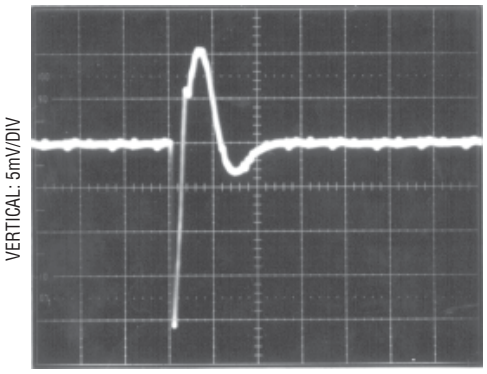


Figure 11. Adequate Settling of Op Amps Driving Analog Input

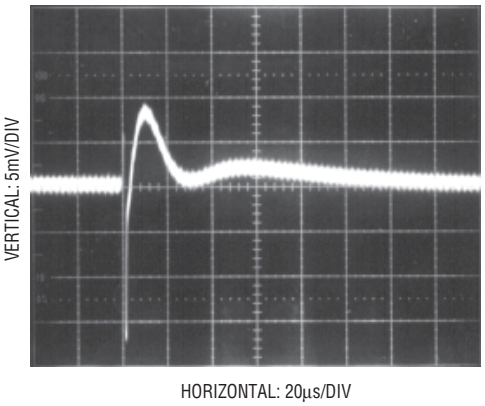


Figure 12. Poor Op Amp Settling Can Cause A/D Errors

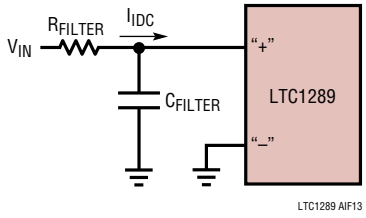


Figure 13. RC Input Filtering

APPLICATIONS INFORMATION

pins on the package ends (DGND and CH0). Grounding any unused inputs (especially the end pin, CH0) will also reduce outside coupling into high source resistances.

4. Sample and Hold

Single-Ended Inputs

The LTC1289 provides a built-in sample and hold (S&H) function for all signals acquired in the single-ended mode (COM pin grounded). This sample and hold allows the LTC1289 to convert rapidly varying signals (see typical curve of S&H Acquisition Time vs Source Resistance). The input voltage is sampled during the t_{SMPL} time as shown in Figure 10. The sampling interval begins after the fourth MUX address bit is shifted in and continues during the remainder of the data transfer. On the falling edge of the final SCLK, the S&H goes into hold mode and the conversion begins. The voltage will be held on either the 8th, 12th or 16th falling edge of the SCLK depending on the word length selected.

Differential Inputs

With differential inputs or when the COM pin is not tied to ground, the A/D no longer converts just a single voltage but rather the difference between two voltages. In these cases, the voltage on the selected "+" input is still sampled and held and therefore may be rapidly time varing just as in single ended mode. However, the voltage on the selected "–" input must remain constant and be free of noise and ripple throughout the conversion time. Otherwise, the differencing operation may not be performed accurately. The conversion time is 52 ACLK cycles. Therefore, a change in the "–" input voltage during this interval can cause conversion errors. For a sinusoidal voltage on the "–" input this error would be:

$$V_{ERROR\ (MAX)} = V_{PEAK} \times 2 \times \pi \times f(\text{“–”}) \times \frac{52}{f_{ACLK}}$$

Where f("–") is the frequency of the "–" input voltage, V_{PEAK} is its peak amplitude and f_{ACLK} is the frequency of the ACLK. In most cases V_{ERROR} will not be significant. For a 60Hz signal on the "–" input to generate a 1/4LSB error (150µV) with the converter running at ACLK = 2MHz, its peak value would have to be 15mV.

5. Reference Inputs

The voltage between the reference inputs of the LTC1289 defines the voltage span of the A/D converter. The reference inputs will have transient capacitive switching currents due to the switched capacitor conversion technique (see Figure 14). During each bit test of the conversion (every 4 ACLK cycles), a capacitive current spike will be generated on the reference pins by the A/D. These current spikes settle quickly and do not cause a problem. However, if slow settling circuitry is used to drive the reference inputs, care must be taken to insure that transients caused by these current spikes settle completely during each bit test of the conversion.

When driving the reference inputs, two things should be kept in mind:

1. Transients on the reference inputs caused by the capacitive switching currents must settle completely during each bit test (each 4 ACLK cycles). Figures 15 and 16 show examples of both adequate and poor settling. Using a slower ACLK will allow more time for the reference to settle. However, even at the maximum ACLK rate of 2MHz most references and op amps can be made to settle within the 2µs bit time. For example an LT1019 used in the shunt mode with a 10µF bypass capacitor will settle adequately. To minimize power an LT1004-2.5 can be used with a 10µF bypass capacitor. For lower value references the LT1004-1.2 with a 1µF bypass capacitor can be used.

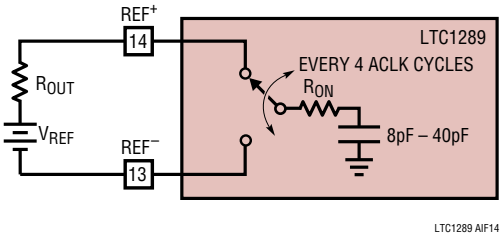


Figure 14. Reference Input Equivalent Circuit

APPLICATIONS INFORMATION

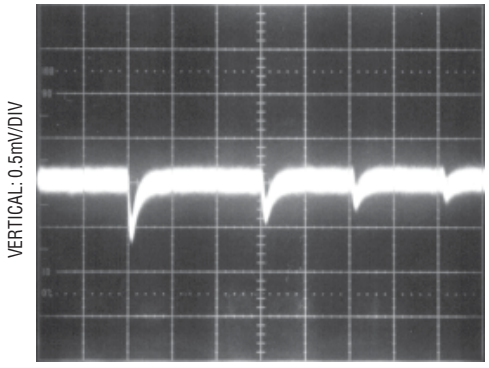


Figure 15. Adequate Reference Settling

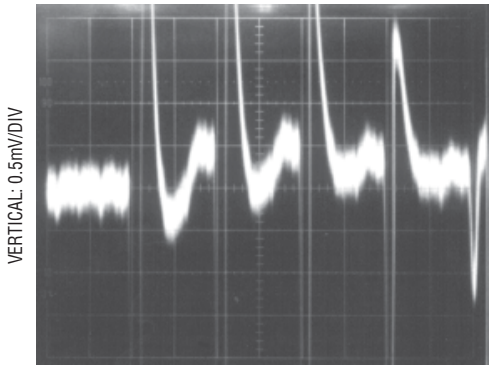


Figure 16. Poor Reference Settling Can Cause A/D Errors

2. It is recommended that REF^- input be tied directly to the analog ground plane. If REF^- is biased at a voltage other than ground, the voltage must not change during a conversion cycle. This voltage must also be free of noise and ripple with respect to analog ground.

6. Reduced Reference Operation

The effective resolution of the LTC1289 can be increased by reducing the input span of the converter. The LTC1289 exhibits good linearity and gain over a wide range of reference voltages (see typical curves of Linearity and Gain Error vs Reference Voltage). However, care must be taken when operating at low values of V_{REF} because of the reduced LSB step size and the resulting higher accuracy requirement placed on the converter. The following factors must be considered when operating at low V_{REF} values:

1. Offset
2. Noise

Offset with Reduced V_{REF}

The offset of the LTC1289 has a larger effect on the output code when the A/D is operated with reduced reference voltage. The offset (which is typically a fixed voltage) becomes a larger fraction of an LSB as the size of the LSB is reduced. The typical curve of Unadjusted Offset Error vs Reference Voltage shows how offset in LSBs is related to reference voltage for a typical value of V_{OS}. For example, a V_{OS} of 0.1mV which is 0.2LSB with a 2.5V reference becomes 0.4LSB with a 1.25V reference. If this offset is unacceptable, it can be corrected digitally by the receiving system or by offsetting the "–" input to the LTC1289.

Noise with Reduced V_{REF}

The total input referred noise of the LTC1289 can be reduced to approximately 200µV peak-to-peak using a ground plane, good bypassing, good layout techniques and minimizing noise on the reference inputs. This noise is insignificant with a 2.5V reference but will become a larger fraction of an LSB as the size of the LSB is reduced. The typical curve of Noise Error vs Reference Voltage shows the LSB contribution of this 200µV of noise.

For operation with a 2.5 reference, the 200µV noise is only 0.32LSB peak-to-peak. In this case, the LTC1289 noise will contribute virtually no uncertainty to the output code. However, for reduced references, the noise may become a significant fraction of an LSB and cause undesirable jitter in the output code. For example, with a 1.25V reference, this same 200µV noise is 0.64LSB peak-to-peak. This will reduce the range of input voltages over which a stable output code can be achieved by 0.64LSB. In this case averaging readings may be necessary.

This noise data was taken in a very clean setup. Any setup induced noise (noise or ripple on V_{CC}, V_{REF}, V_{IN} or V^-) will add to the internal noise. The lower the reference voltage to be used, the more critical it becomes to have a clean, noise-free setup.

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7. LTC1289 AC Characteristics

Two commonly used figures of merit for specifying the dynamic performance of the A/D's in digital signal processing applications are the Signal-to-Noise Ratio (SNR) and the "effective number of bits (ENOB)." SNR is defined as the ratio of the RMS magnitude of the fundamental to the RMS magnitude of all the nonfundamental signals up to the Nyquist frequency (half the sampling frequency). The theoretical maximum SNR for a sine wave input is given by:

$$SNR = (6.02N + 1.76dB)$$

where N is the number of bits. Thus the SNR is a function of the resolution of the A/D. For an ideal 12-bit A/D the SNR is equal to 74dB. A Fast Fourier Transform(FFT) plot of the output spectrum of the LTC1289 is shown in Figures 17a and 17b. The input (f_{IN}) frequencies are 1kHz and 12kHz with the sampling frequency (f_S) at 25kHz. The SNR obtained from the plot are 72.92dB and 72.23dB.

Rewriting the SNR expression it is possible to obtain the equivalent resolution based on the SNR measurement.

$$N = \frac{SNR - 1.76dB}{6.02}$$

This is the so-called effective number of bits (ENOB). For the example shown in Figures 17a and 17b, N = 11.8 bits and 11.7 bits, respectively. Figure 18 shows a plot of ENOB as a function of input frequency. The curve shows the A/D's ENOB remain in the range of 11.8 to 11.7 for input frequencies up to $f_S/2$

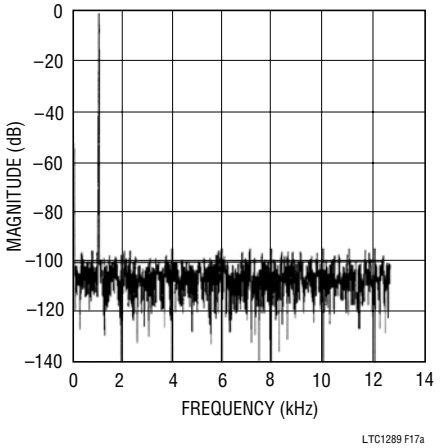


Figure 17a. f_{IN} = 1kHz, f_S = 25kHz, SNR = 72.92dB

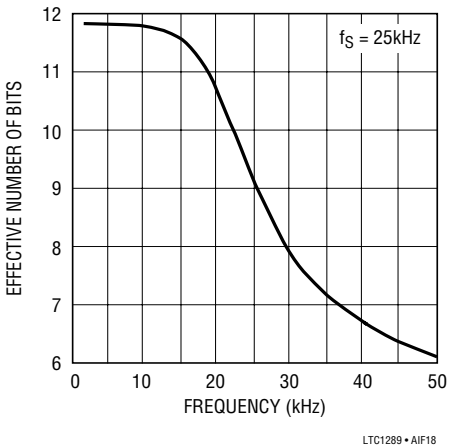


Figure 18. LTC1289 ENOB vs Input Frequency

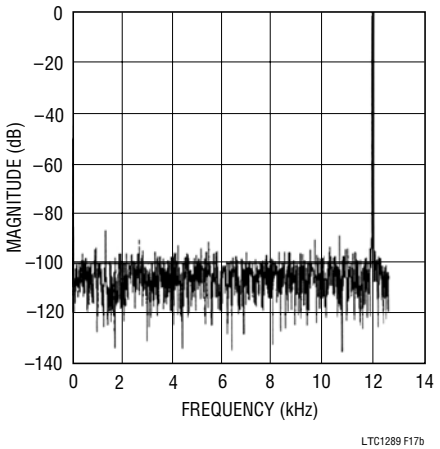


Figure 17b. f_{IN} = 12kHz, f_S = 25kHz, SNR = 72.23dB

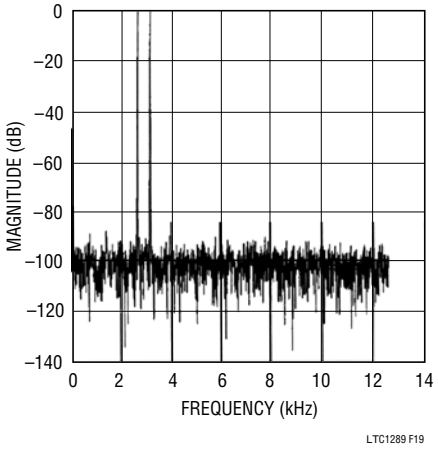


Figure 19. $f_{IN}1$ = 2.6kHz, $f_{IN}2$ = 3.1kHz, f_S = 25kHz

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Figure 19 shows an FFT plot of the output spectrum for two tones applied to the input of the A/D. Nonlinearities in the A/D will cause distortion products at the sum and difference frequencies of the fundamentals and products of the fundamentals. This is classically referred to as intermodulation distortion (IMD).

8. Overvoltage Protection

Applying signals to the analog MUX that exceed the positive or negative supply of the device will degrade the accuracy of the A/D and possibly damage the device. For example this condition would occur if a signal is applied to the analog MUX before power is applied to the LTC1289. Another example is the input source is operating from different supplies of larger value than the LTC1289. These conditions should be prevented either with proper supply sequencing or by use of external circuitry to clamp or current limit the input source. As shown in Figure 20, a 1kΩ resistor is enough to stand off ±15V (15mA for one only channel). If more than one channel exceeds the supplies than the following guidelines can be used. Limit the current to 7mA per channel and 28mA for all channels. This means four channels can handle 7mA of input current each. Reducing the ACLK and SCLK frequencies from the maximum of 2MHz and 1MHz, respectively (see Typical Peformance Characteristics curves Maximum ACLK Frequency vs Source Resistance and Sample and Hold Acquisition Time vs Source Resistance) allows the use of larger current limiting resistors. Use 1N4148 diode clamps from the MUX inputs to V_{CC} and V^- if the value of the series resistor will not allow the maximum clock speeds to be used or if an unknown source is used to drive the LTC1289 MUX inputs.

How the various power supplies to the LTC1289 are applied can also lead to overvoltage conditions. For single supply operation (i.e., unipolar mode), if V_{CC} and REF^+ are not tied together, then V_{CC} should be turned on first, then REF^+. If this sequence cannot be met, connecting a diode from REF^+ to V_{CC} is recommended (see Figure 21).

For dual supplies (bipolar mode) placing two Schottky diodes from V_{CC} and V^- to ground (Figure 22) will prevent power supply reversal from occuring when an input source is applied to the analog MUX before power is applied to the device. Power supply reversal occurs, for example, if the input is pulled below V^- then V_{CC} will pull a diode drop below ground which could cause the device not to power up properly. Likewise, if the input is pulled above V_{CC} then V^- will be pulled a diode drop above ground. If no inputs are present on the MUX, the Schottky diodes are not required if V^- is applied first, then V_{CC}.

Because a unique input protection structure is used on the digital input pins, the signal levels on these pins can exceed the device V_{CC} without damaging the device.

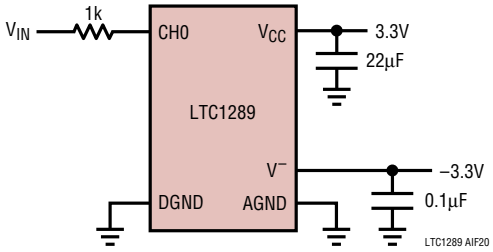


Figure 20. Overvoltage Protection for MUX

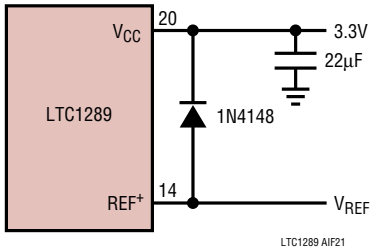


Figure 21.

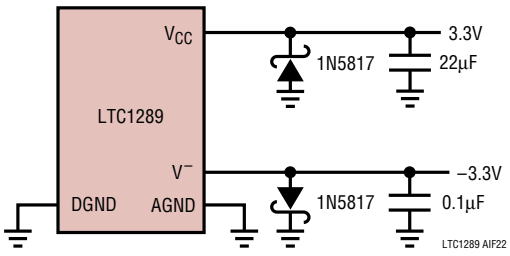


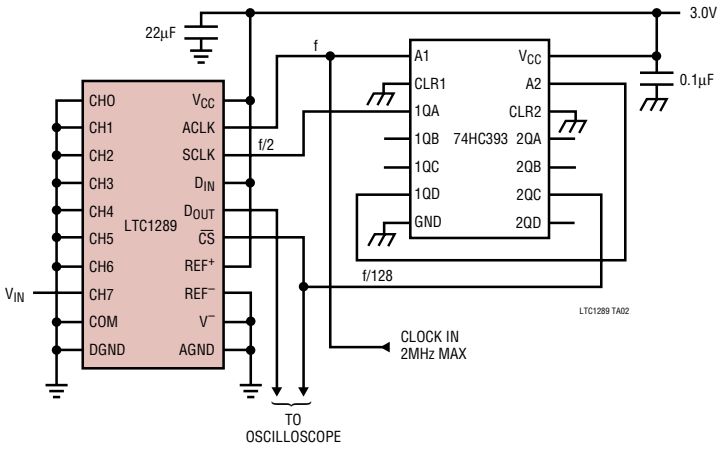
Figure 22. Power Supply Reversal

TYPICAL APPLICATIONS

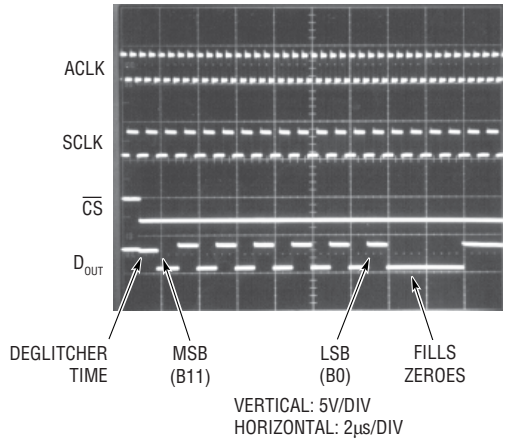
A "Quick Look" Circuit for the LTC1289

Users can get a quick look at the function and timing of the LTC1289 by using the following simple circuit. REF^+ and D_{IN} are tied to V_{CC} selecting a 3V input span, CH7 as a single-ended input, unipolar mode, MSB-first format and 16-bit word length. ACLK is driven by an external clock and SCLK is driven by one half the clock rate. $\overline{CS}$ is driven at 1/128 the clock rate by the 74HC393 and D_{OUT} outputs the data. All other pins are tied to a ground plane. The output data from the D_{OUT} pin can be viewed on an oscilloscope which is set up to trigger on the falling edge of $\overline{CS}$.

A "Quick Look" Circuit for the LTC1289



Scope Trace of LTC1289 "Quick Look" Circuit Showing A/D Output of 010101010101 (555_{HEX})

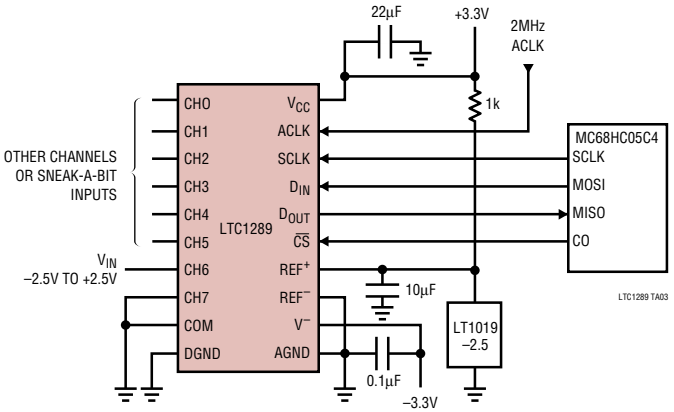


SNEAK-A-BIT™

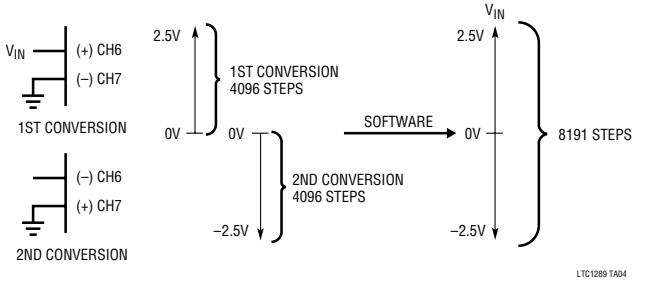
The LTC1289's unique ability to software select the polarity of the differential inputs and the output word length is used to achieve one more bit of resolution. Using the circuit below with two conversions and some software, a 2's complement 12-bit + sign word is returned to memory inside the MPU. The MC68HC05C4 was chosen as an example, however, any processor that operates at 3.3V could be used.

Two 12-bit unipolar conversions are performed: the first over a 0V to 2.5V span and the second over a 0V to –2.5V span (by reversing the polarity of the inputs). The sign of the input is determined by which of the two spans contained it. Then the resulting number (ranging from –4095 to +4095 decimal) is converted to 2's complement notation and stored in RAM.

SNEAK-A-BIT Circuit



SNEAK-A-BIT

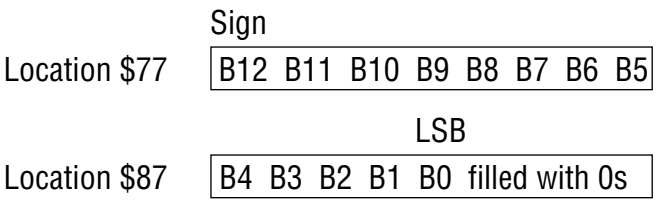


SNEAK-A-BIT is a trademark of Linear Technology Corp.

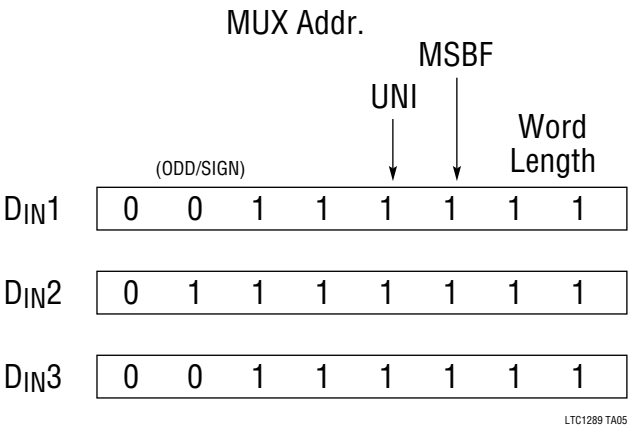
TYPICAL APPLICATIONS

SNEAK-A-BIT Code

D_{OUT} from LTC1289 in MC68HC05C4 RAM



D_{IN} words for LTC1289



SNEAK-A-BIT Code for the LTC1289 Using the MC68HC05C4

MNEMONIC			DESCRIPTION
	LDA	#$50	Configuration data for SPCR
	STA	$0A	Load configuration data into $0A
	LDA	#$FF	Configuration data for port C DDR
	STA	$06	Load configuration data into port C DDR
	BSET	0, $02	Make sure $\overline{CS}$ is high
	JSR	READ –/+	Dummy read configures LTC1289 for next read
	JSR	READ +/–	Read CH6 with respect to CH7
	JSR	READ –/+	Read CH7 with respect to CH6
	JSR	CHK SIGN	Determines which reading has valid data, converts to 2's complement and stores in RAM
READ –/+:	LDA	#$3F	Load D_{IN} word for LTC1289 into ACC
	JSR	TRANSFER	Read LTC1289 routine
	LDA	$60	Load MSBs from LTC1289 in ACC
	STA	$71	Store MSBs in $71
	LDA	$61	Load LSBs from LTC1289 in ACC
	STA	$72	Store LSBs in $72
	RTS		Return

SNEAK-A-BIT Code for the LTC1289 Using the MC68HC05C4

MNEMONIC			DESCRIPTION
READ +/–:	LDA	#$7F	Load D_{IN} word for LTC1289 into ACC
	JSR	TRANSFER	Read LTC1289 routine
	LDA	$60	Load MSBs from LTC1289 into ACC
	STA	$73	Store MSBs in $73
	LDA	$61	Load LSBs from LTC1289 into ACC
	STA	$74	Store LSBs in $74
	RTS		Return
TRANSFER:	BCLR	0, $02	$\overline{CS}$ goes low
	STA	$0C	Load D_{IN} into SPI. Start transfer
LOOP 1:	TST	$0B	Test status of SPIF
	BPL	LOOP 1	Loop to previous instruction if not done
	LDA	$0C	Load contents of SPI data reg into ACC
	STA	$0C	Start next cycle
	STA	$60	Store MSBs in $60
LOOP 2:	TST	$0B	Test status of SPIF
	BPL	LOOP 2	Loop to previous instruction if not done
	BSET	0, $02	$\overline{CS}$ goes high
	LDA	$0C	Load contents of SPI data reg into ACC
	STA	$61	Store LSBs in $61
	RTS		Return
CHK SIGN:	LDA	$73	Load MSBs of +/– read into ACC
	ORA	$74	Or ACC (MSBs) with LSBs of +/– read
	BEQ	MINUS	If result is 0 goto minus
	CLC		Clear carry
	ROR	$73	Rotate right $73 through carry
	ROR	$74	Rotate right $74 through carry
	LDA	$73	Load MSBs of +/– read into ACC
	STA	$77	Store MSBs in RAM locations $77
	LDA	$74	Load LSBs of +/– read into ACC
	STA	$87	Store LSBs in RAM location $87
	BRA	END	Goto end of routine
MINUS:	CLC		Clear carry
	ROR	$71	Shift MSBs of –/+ read right
	ROR	$72	Shift LSBs of –/+ read right
	COM	$71	1's complement of MSBs
	COM	$72	1's complement of LSBs
	LDA	$72	Load LSBs into ACC
	ADD	#$01	Add 1 to LSBs
	STA	$72	Store ACC in $72
	CLRA		Clear ACC
	ADC	$71	Add with carry to MSBs. Result in ACC
	STA	$71	Store ACC in $71
	STA	$77	Store MSBs in RAM locations $77
	LDA	$72	Load LSBs in ACC
	STA	$87	Store LSBs in RAM location $87
END:	RTS		Return

TYPICAL APPLICATIONS

Power Shutdown

For battery-powered applications it is desirable to keep power dissipation at a minimum. The LTC1289 can be powered down when not in use reducing the supply current from a nominal value of 1mA to typically 1µA (with ACLK turned off). See the Curve for Supply Current (Power Shutdown) vs ACLK if ACLK cannot be turned off when the LTC1289 is powered down. In this case the supply current is proportional to the ACLK frequency and is independent of temperature until it reaches the magnitude of the supply current attained with ACLK turned off.

As an example of how to use this feature let's add this to the previous application, SNEAK-A-BIT. After the CHK SIGN subroutine call insert the following:

```
                    •
                    •
JSR CHK SIGN        Determines which reading has valid
                    data, converts to 2's complement
                    and stores in RAM
JSR SHUTDOWN        LTC1289 power shutdown routine
```

The actual subroutine is:

```
SHUTDOWN:  LDA  #$3D        Load DIN word for
                            LTC1289 into ACC
           JSR TRANSFER     Read LTC1289 routine
           RTS              Return
```

To place the device in power shutdown the word length bits are set to WL1 = 0 and WL0 = 1. The LTC1289 is powered up on the next request for conversion and it's ready to digitize an input signal immediately.

Power Shutdown Timing Considerations

After power shutdown has been requested, the LTC1289 is powered up on the next request for a conversion. This request can be initiated either by bringing $\overline{CS}$ low or by starting the next cycle of SCLKs if $\overline{CS}$ is kept low (see Figures 3 and 4). When the SCLK frequency is much slower than the ACLK frequency a situation can arise where the LTC1289 could power down and then prematurely power back up. Power shutdown begins at the negative going edge of the 10th SCLK once it has been requested. A dummy conversion is executed and the LTC1289 waits for the next request for conversion. If the SCLKs have not finished once the LTC1289 has finished its dummy conversion, it will recognize the next remaining SCLKs as a request to start a conversion and power up the LTC1289 (see Figure 23). To prevent this, bring either $\overline{CS}$ high at the 19th SCLK (Figure 24) or clock out only 10 SCLKs (Figure 25) when power shutdown is requested.

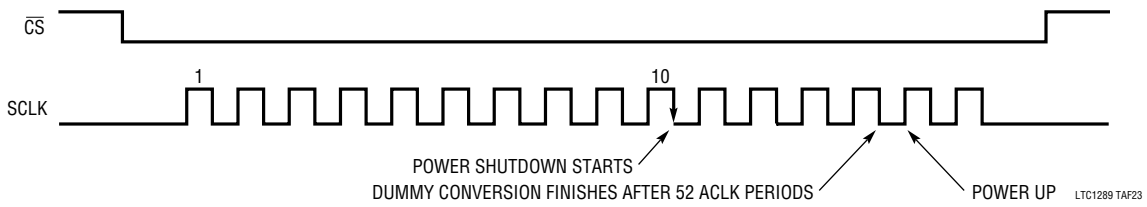


Figure 23. Power Shutdown Timing Problem

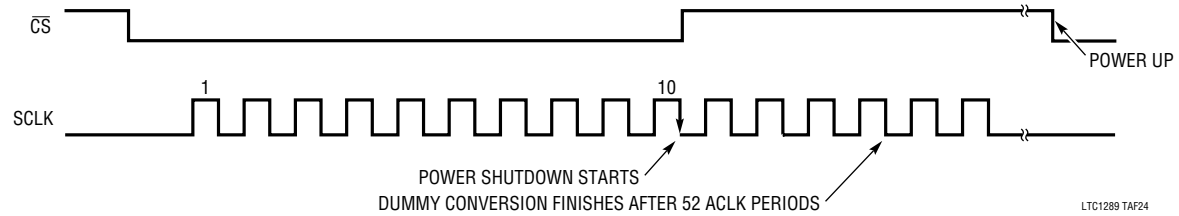


Figure 24. Power Shutdown Timing

TYPICAL APPLICATIONS

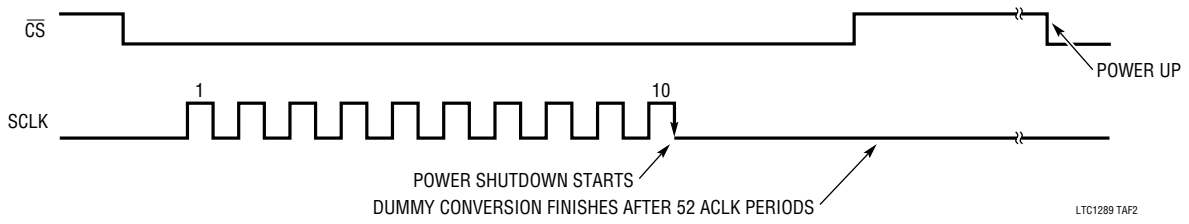
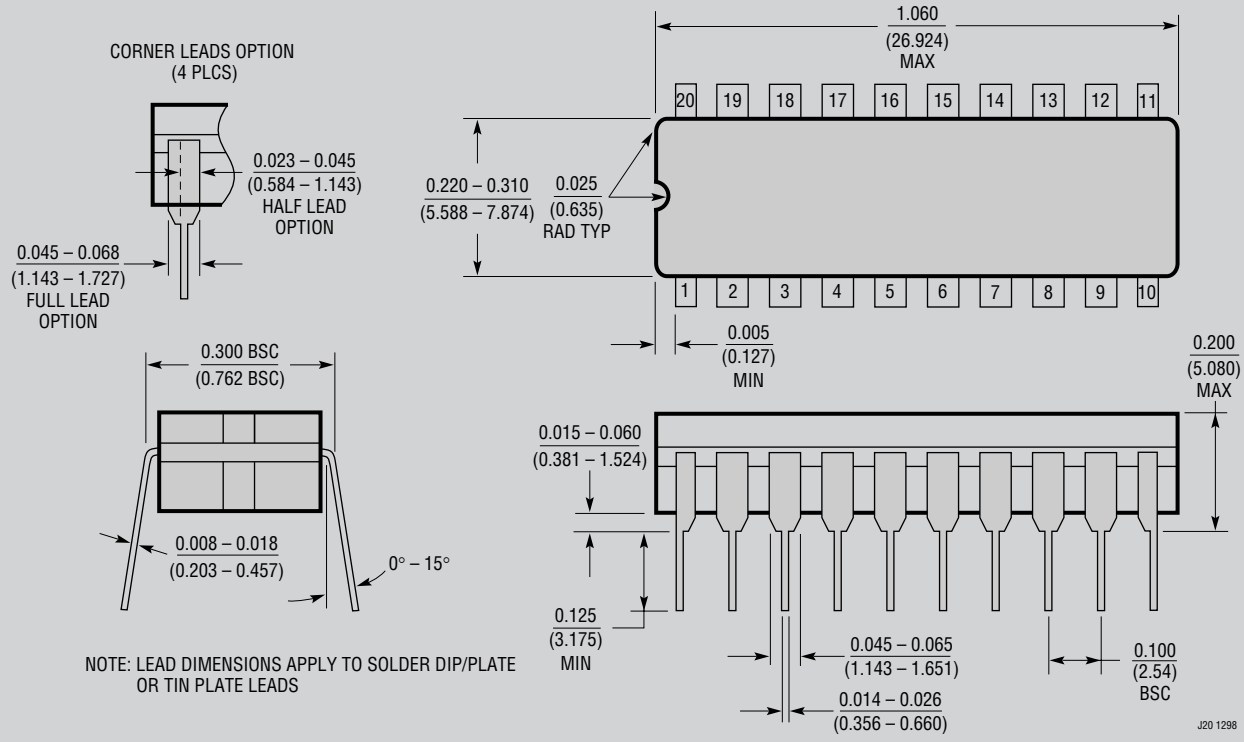


Figure 25. Power Shutdown Timing

PACKAGE DESCRIPTION

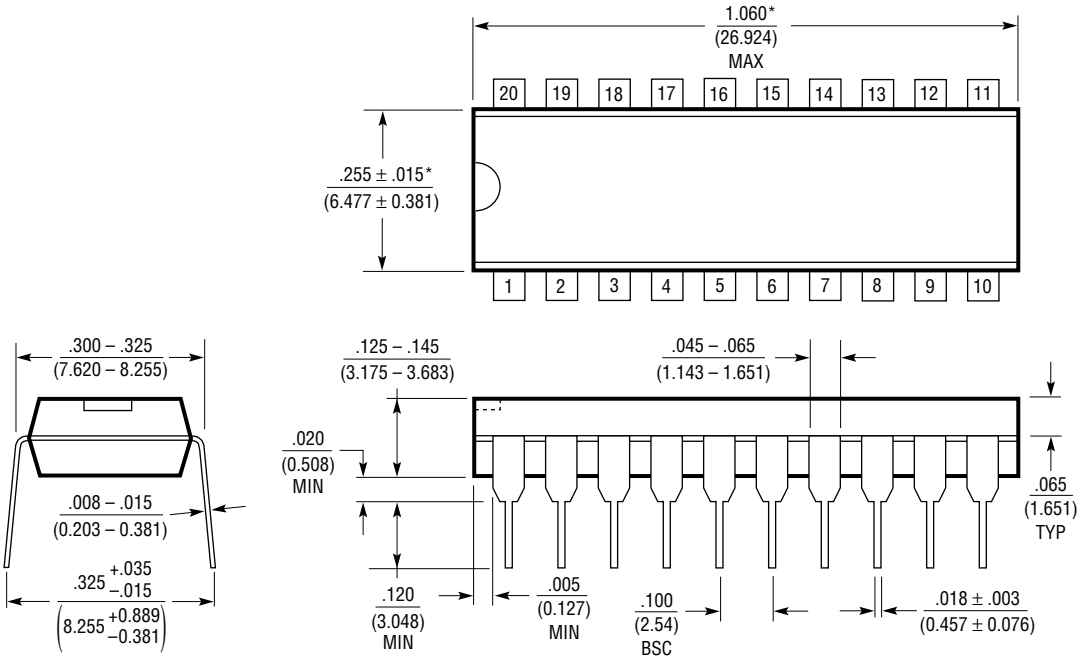
J Package
20-Lead CERDIP (Narrow .300 Inch, Hermetic)
(Reference LTC DWG # 05-08-1110)



OBSOLETE PACKAGE

PACKAGE DESCRIPTION

N Package
20-Lead PDIP (Narrow .300 Inch)
(Reference LTC DWG # 05-08-1510)



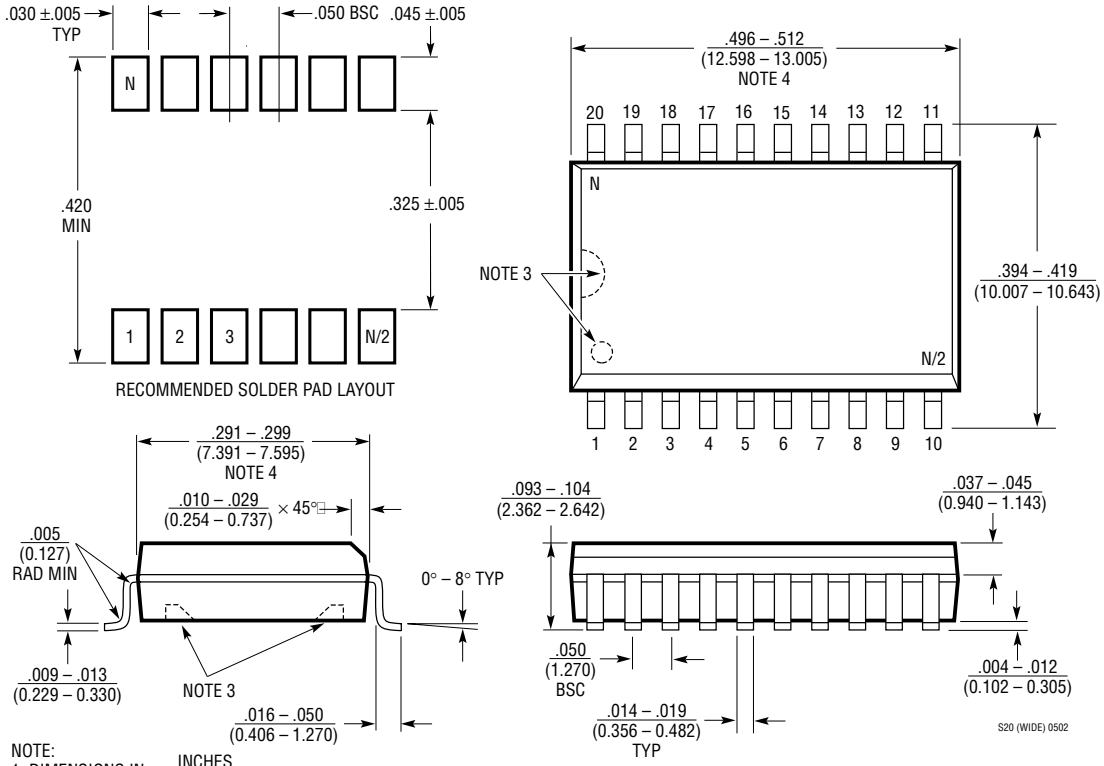
NOTE:
1. DIMENSIONS ARE INCHES / MILLIMETERS

*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH (0.254mm)

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of circuits as described herein will not infringe on existing patent rights.

PACKAGE DESCRIPTION

SW Package
20-Lead Plastic Small Outline (Wide .300 Inch)
(Reference LTC DWG # 05-08-1620)



NOTE:
1. DIMENSIONS IN $\frac{\text{INCHES}}{(\text{MILLIMETERS})}$
2. DRAWING NOT TO SCALE
3. PIN 1 IDENT, NOTCH ON TOP AND CAVITIES ON THE BOTTOM OF PACKAGES ARE THE MANUFACTURING OPTIONS. THE PART MAY BE SUPPLIED WITH OR WITHOUT ANY OF THE OPTIONS
4. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1285/LTC1288	1-/2-Channel, 3V, Micropower 12-Bit ADC	Autoshutdown, SO-8 Package
LTC1290	8-Channel Configurable, 5V, 12-Bit ADC	Pin-Compatible with LTC1289
LTC1391	Serial-Controlled 8-to-1 Analog Multiplexer	Low R_{ON}, Low Power, 16-Pin SO and SSOP Package
LTC1401	3V, 12-Bit, 200ksps Serial ADC	15mW, Internal Reference, SO-8 Package
LTC1448	Dual 12-Bit V_{OUT} DACs in SO-8 Package	0.5LBS DNL, 3V to 5V Supply, Swings 0V to V_{REF}
LTC1454/LTC1454L	Dual 12-Bit V_{OUT} DACs in SO-16 Package	5V/3V, Buffered Rail-to-Rail Output, 0.5LSB DNL
LTC1458/LTC1458L	Quad 12-Bit V_{OUT} DACs	5V/3V, Buffered Rail-to-Rail Output, 0.5LSB DNL
LTC1594/LTC1598L	4-/8-Channel, 3V Micropower 12-Bit ADC	Low Power, Small Size
LTC1852/LTC1853	10-Bit/12-Bit, 8-Channel, 400ksps ADCs	3V or 5V, Programmable MUX and Sequencer
LTC2404/LTC2408	24-Bit, 4-/8-Channel, No Latency ΔΣ ADC	4ppm INL, 10ppm Total Unadjusted Error, 200μA
LTC2424/LTC2428	20-Bit, 4-/8-Channel, No Latency ΔΣ ADC	1.2ppm Noise, 8ppm INL, Pin Compatible with LTC2404/LTC2408

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LT 0506 REV B • PRINTED IN USA

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