3V Single Chip 12-Bit Data Acquisition System

FEATURES

- Single Supply 3.3V Operation
- Built-In Sample-and-Hold
- Direct 3-Wire Interface to Most MPU Serial Ports and All MPU Parallel Ports
- 30kHz Maximum Throughput Rate

KEY SPECIFICATIONS

- Minimum Guaranteed Supply Voltage: 2.7V
- Resolution: 12 Bits
- Fast Conversion Time: 24µs Max Over Temp.
- Low Supply Current: 1.0mA

APPLICATIONS

- Battery-Powered Instruments
- Data Logger
- Data Acquisition Modules

DESCRIPTION

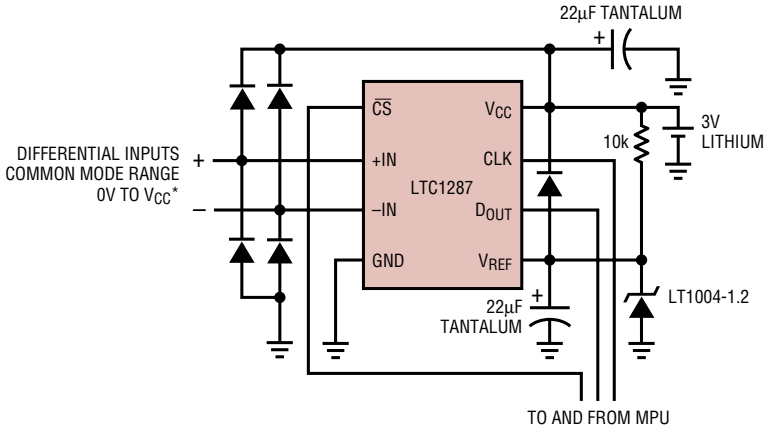
The LTC®1287 is a 3V data acquisition component which contains a serial I/O successive approximation A/D converter. The device specifications are guaranteed at a supply voltage of 2.7V. It uses LTCMOS™ switched capacitor technology to perform a 12-bit unipolar, A/D conversion. The differential input has an on-chip sample-and-hold on the (+) input.

The serial I/O is designed to communicate without external hardware to most MPU serial ports and all MPU parallel I/O ports allowing data to be transmitted and received over three wires. The low voltage operating capability and the low power consumption of this device make it ideally suited for battery applications. Given the ease of use, small package size and the minimum number of interconnects for I/O, the LTC1287 can be used for remote sensing applications.

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LTCMOS is a trademark of Linear Technology Corporation

TYPICAL APPLICATION

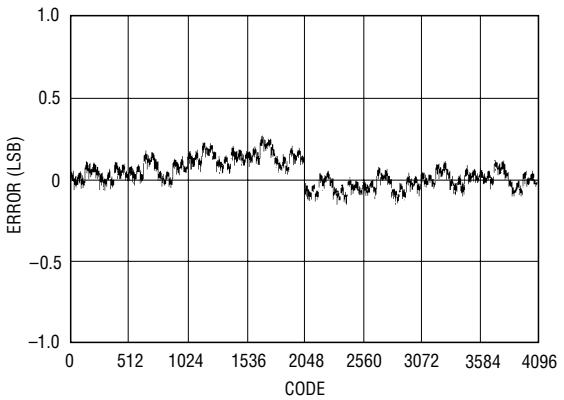
3V Differential Input Data Acquisition System



* FOR OVERVOLTAGE PROTECTION, LIMIT THE INPUT CURRENT TO 15mA PER PIN OR CLAMP THE INPUTS TO V_{CC} AND GND WITH 1N4148 DIODES. CONVERSION RESULTS ARE NOT VALID WHEN THE SELECTED CHANNEL OR OTHER CHANNEL IS OVERVOLTAGED (V_{IN} < GND OR V_{IN} > V_{CC}). SEE SECTION ON OVERVOLTAGE PROTECTION IN THE APPLICATIONS INFORMATION.

1287 TA01

INL with V_{REF} = 1.2V



LTC1287 TA02

ABSOLUTE MAXIMUM RATINGS

(Notes 1 and 2)

Supply Voltage (V_{CC}) to GND 12V

Voltage

Analog and Reference Inputs .... –0.3V to V_{CC} + 0.3V

Digital Inputs ..... –0.3V to 12V

Digital Outputs ..... –0.3V to V_{CC} + 0.3V

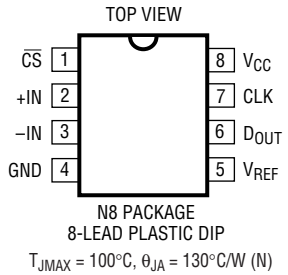
Power Dissipation 500mW

Operating Temperature Range ..... 0°C to 70°C

Storage Temperature Range ..... –65°C to 150°C

Lead Temperature (Soldering, 10 sec.)..... 300°C

PACKAGE/ORDER INFORMATION



N8 PACKAGE
8-LEAD PLASTIC DIP
T_{JMAX} = 100°C, θ_{JA} = 130°C/W (N)

ORDER PART NUMBER

LTC1287BCN8
LTC1287CCN8

J8 PACKAGE
8-LEAD CERAMIC DIP
T_{JMAX} = 150°C, θ_{JA} = 100°C/W (J)

LTC1287BCJ8
LTC1287CCJ8

OBSOLETE PACKAGE
Consider N8 Package for Alternate Source

Consult LTC Marketing for parts specified with wider operating temperature ranges.

CONVERTER AND MULTIPLEXER CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 3)

PARAMETER	CONDITIONS		LTC1287B MIN	LTC1287B TYP	LTC1287B MAX	LTC1287C MIN	LTC1287C TYP	LTC1287C MAX	UNITS
Offset Error	V_{CC} = 2.7V (Note 4)	●			±3.0			±3.0	LSB
Linearity Error (INL)	V_{CC} = 2.7V (Notes 4 & 5)	●			±0.5			±0.5	LSB
Gain Error	V_{CC} = 2.7V (Note 4)	●			±0.5			±1.0	LSB
Minimum Resolution for Which No Missing Codes are Guaranteed		●			12			12	Bits
Analog and REF Input Range	(Note 7)			– 0.05V to V_{CC} + 0.05V					V
On Channel Leakage Current (Note 8)	On Channel = 3V Off Channel = 0V	●			±1			±1	µA
	On Channel = 0V Off Channel = 3V	●			±1			±1	µA
Off Channel Leakage Current (Note 8)	On Channel = 3V Off Channel = 0V	●			±1			±1	µA
	On Channel = 0V Off Channel = 3V	●			±1			±1	µA

AC CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		LTC1287B/LTC1287C MIN	LTC1287B/LTC1287C TYP	LTC1287B/LTC1287C MAX	UNITS
f_{CLK}	Clock Frequency	(Note 6)		(Note 9)		0.5	MHz
t_{SMPL}	Analog Input Sample Time	See Operating Sequence			1.5		CLK Cycles
t_{CONV}	Conversion Time	See Operating Sequence			12		CLK Cycles
t_{CYC}	Total Cycle Time	See Operating Sequence (Note 6)		14 CLK+5.0µs			Cycles
t_{dDO}	Delay Time, CLK↓ to D_{OUT} Data Valid	See Test Circuits	●		250	450	ns
t_{dis}	Delay Time, $\overline{CS}$↑ to D_{OUT} Hi-Z	See Test Circuits	●		80	160	ns
t_{en}	Delay Time, CLK↓ to D_{OUT} Enabled	See Test Circuits	●		130	250	ns

AC CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		LTC1287B/LTC1287C MIN	TYP	MAX	UNITS
t_{hDO}	Time Output Data Remains Valid After CLK↓				50		ns
t_f	D_{OUT} Fall Time	See Test Circuits	●		40	100	ns
t_r	D_{OUT} Rise Time	See Test Circuits	●		40	100	ns
t_{WHCLK}	CLK High Time	V_{CC} = 3V (Note 6)		600			ns
t_{WLCLK}	CLK Low Time	V_{CC} = 3V (Note 6)		800			ns
$t_{su\overline{CS}}$	Setup Time, $\overline{CS}$↓ Before CLK↑	V_{CC} = 3V (Note 6)		100			ns
$t_{WH\overline{CS}}$	$\overline{CS}$ High Time Between Data Transfer Cycles	V_{CC} = 3V (Note 6)		5.0			µs
$t_{WL\overline{CS}}$	$\overline{CS}$ Low Time During Data Transfer	V_{CC} = 3V (Note 6)		14			CLK Cycles
C_{IN}	Input Capacitance	Analog Inputs On Channel Analog Inputs Off Channel Digital Inputs			100 5 5		pF pF pF

DIGITAL AND DC ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		LTC1287B/LTC1287C MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage	V_{CC} = 3.6V	●	2.1			V
V_{IL}	Low Level Input Voltage	V_{CC} = 3.0V	●			0.45	V
I_{IH}	High Level Input Current	V_{IN} = V_{CC}	●			2.5	µA
I_{IL}	Low Level Input Current	V_{IN} = 0V	●			–2.5	µA
V_{OH}	High Level Output Voltage	V_{CC} = 3.0V, I_O = 20µA I_O = 400µA	 ●	 2.7	2.90 2.85		V V
V_{OL}	Low Level Output Voltage	V_{CC} = 3.0V, I_O = 20µA I_O = 400µA	 ●		0.05 0.10	 0.3	V V
I_{OZ}	High Z Output Leakage	V_{OUT} = V_{CC}, $\overline{CS}$ High V_{OUT} = 0V, $\overline{CS}$ High	● ●			3 –3	µA µA
I_{SOURCE}	Output Source Current	V_{OUT} = 0V			–10		mA
I_{SINK}	Output Sink Current	V_{OUT} = V_{CC}			9		mA
I_{CC}	Positive Supply Current	$\overline{CS}$ High	●		1.5	5	mA
I_{REF}	Reference Current	V_{REF} = 2.5V	●		10	50	µA

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: All voltage values are with respect to ground (unless otherwise noted).

Note 3: V_{CC} = 3V, V_{REF} = 2.5V, CLK = 500kHz unless otherwise specified.

Note 4: One LSB is equal to V_{REF} divided by 4096. For example, when V_{REF} = 2.5V, 1LSB = 2.5V/4096 = 0.61mV.

Note 5: Integral nonlinearity error is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

Note 6: Recommended operating conditions.

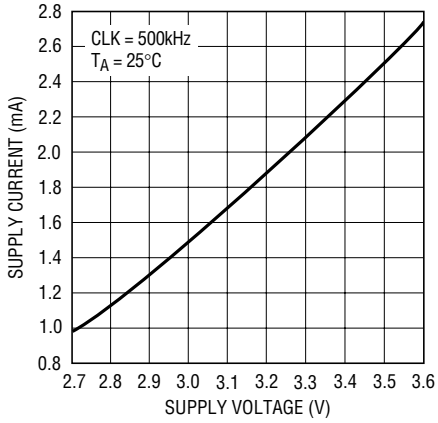
Note 7: Two on-chip diodes are tied to each analog input which will conduct for analog voltages one diode drop below GND or one diode drop above V_{CC}. Be careful during testing at low V_{CC} levels, as high level analog inputs can cause this input diode to conduct, especially at elevated temperature, and cause errors for inputs near full scale. This spec allows 50mV forward bias of either diode. This means that as long as the analog input does not exceed the supply voltage by more than 50mV, the output code will be correct.

Note 8: Channel leakage current is measured after the channel selection.

Note 9: Increased leakage currents at elevated temperatures cause the S/H to droop, therefore it is recommended that $f_{CLK} \geq$ 30kHz at 85°C and $f_{CLK} \geq$ 3kHz at 25°C.

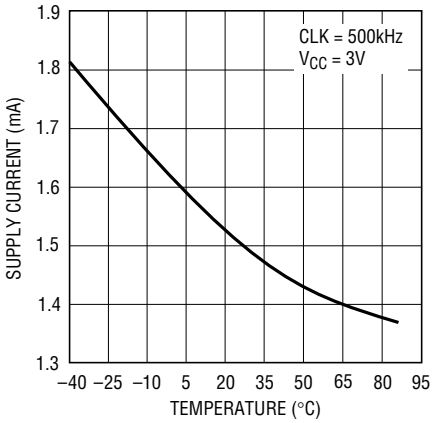
TYPICAL PERFORMANCE CHARACTERISTICS

Supply Current vs Supply Voltage



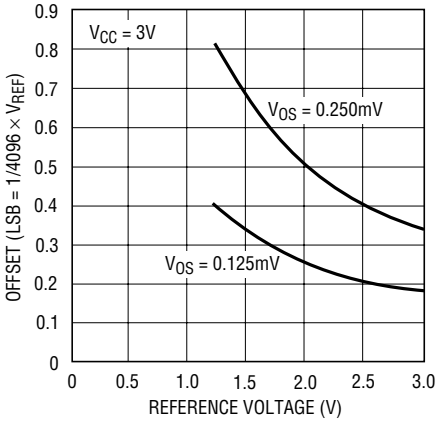
LTC1287 G1

Supply Current vs Temperature



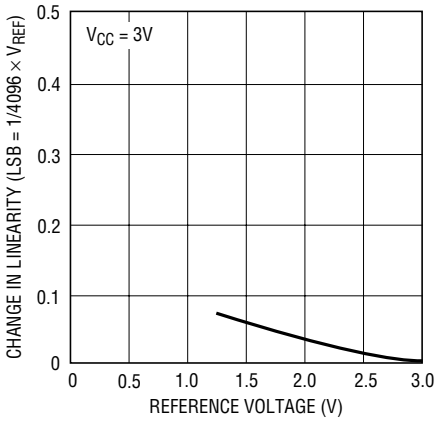
LTC1287 G2

Unadjusted Offset Voltage vs Reference Voltage



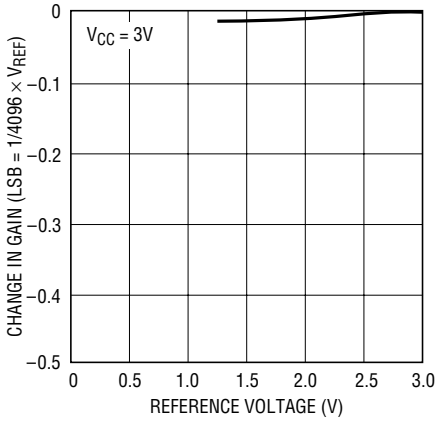
LTC1287 G3

Change in Linearity vs Reference Voltage



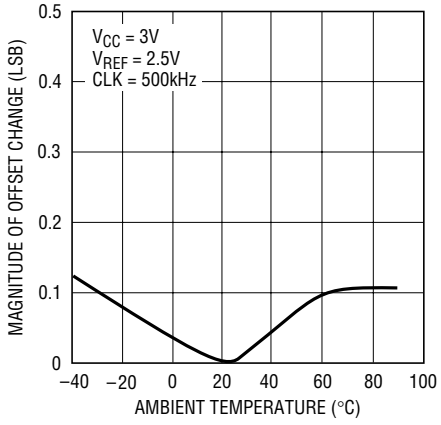
LTC1287 G4

Change in Gain vs Reference Voltage



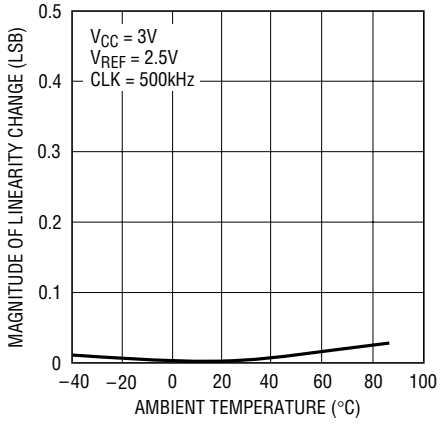
LTC1287 G5

Change in Offset vs Temperature



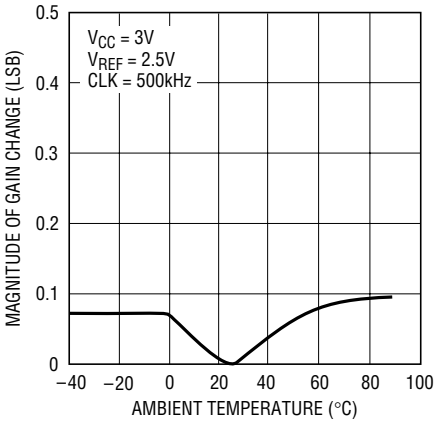
LTC1287 G6

Change in Linearity vs Temperature



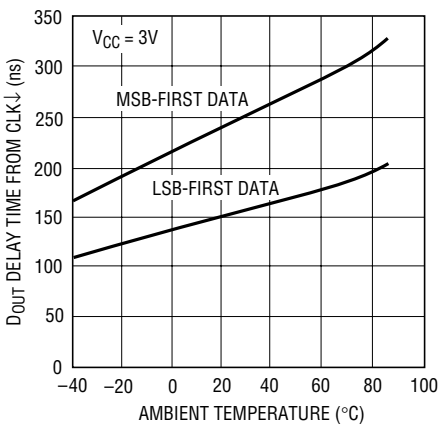
LTC1287 G7

Change in Gain vs Temperature



LTC1287 G8

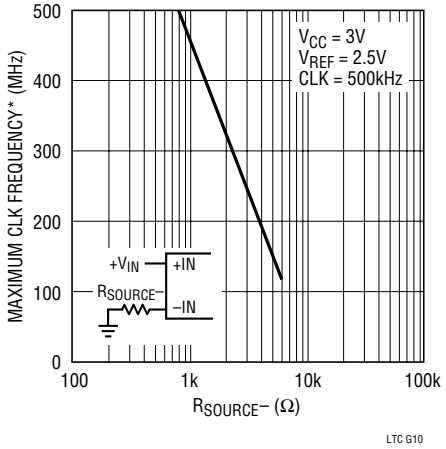
D_{OUT} Delay Time vs Temperature



LTC1287 G9

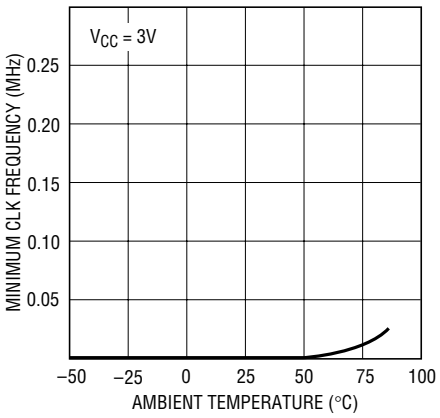
TYPICAL PERFORMANCE CHARACTERISTICS

Maximum Clock Rate vs Source Resistance



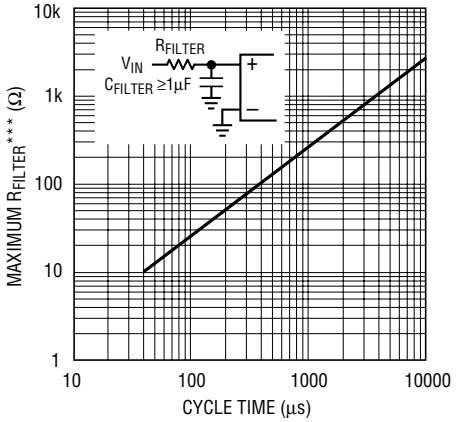
LTC G10

Minimum Clock Rate for 0.1LSB Error**



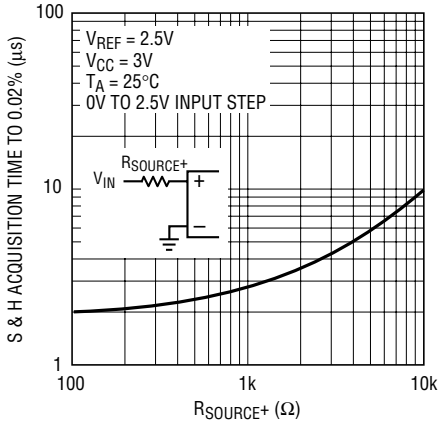
LTC1287 G11

Maximum Filter Resistor vs Cycle Time



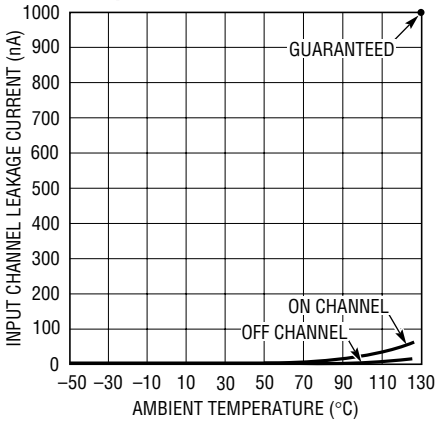
LTC1287 G12

Sample-and-Hold Acquisition Time vs Source Resistance



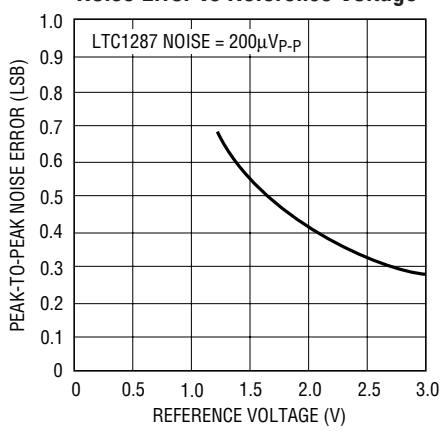
LTC1287 G13

Input Channel Leakage Current vs Temperature



LTC1287 G14

Noise Error vs Reference Voltage



LTC1287 G15

* MAXIMUM CLK FREQUENCY REPRESENTS THE CLK FREQUENCY AT WHICH A 0.1LSB SHIFT IN THE ERROR AT ANY CODE TRANSITION FROM ITS 500kHz VALUE IS FIRST DETECTED.

** AS THE CLK FREQUENCY IS DECREASED FROM 1MHz, MINIMUM CLK FREQUENCY (ΔERROR ≤ 0.1LSB) REPRESENTS THE FREQUENCY AT WHICH A 0.1LSB SHIFT IN ANY CODE TRANSITION FROM ITS 500kHz VALUE IS FIRST DETECTED.

*** MAXIMUM R_{FILTER} REPRESENTS THE FILTER RESISTOR VALUE AT WHICH A 0.1LSB CHANGE IN FULL SCALE ERROR FROM ITS VALUE AT R_{FILTER} = 0Ω IS FIRST DETECTED.

PIN FUNCTIONS

$\overline{CS}$ (Pin 1): Chip Select Input. A logic low on this input enables the LTC1287.

+IN, –IN (Pin 2,3): Analog Inputs. These inputs must be free of noise with respect to GND.

GND (Pin 4): Analog Ground GND should be tied directly to an analog ground plane.

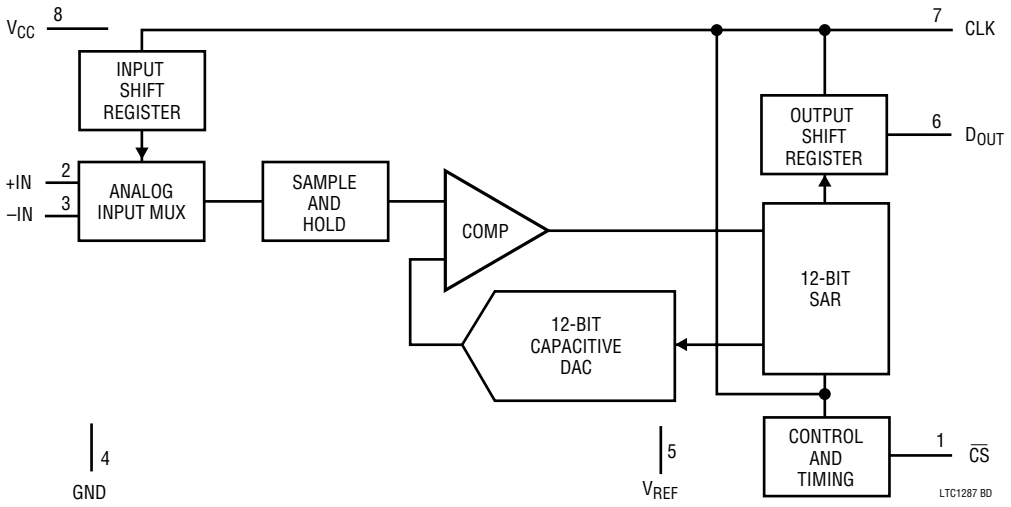
V_{REF} (Pin 5): Reference Input. The reference input defines the span of the A/D converter and must be kept free of noise with respect to GND.

D_{OUT} (Pin 6): Digital Data Output. The A/D conversion result is shifted out of this output.

CLK (Pin 7): Shift Clock. This clock synchronizes the serial data transfer.

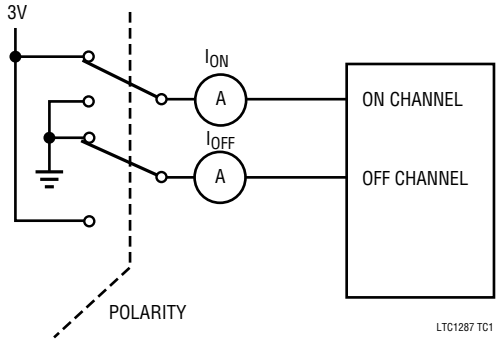
V_{CC} (Pin 8): Positive Supply. This supply must be kept free of noise and ripple by bypassing directly to the analog ground plane.

BLOCK DIAGRAM

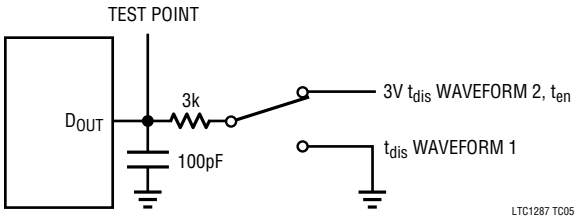


TEST CIRCUITS

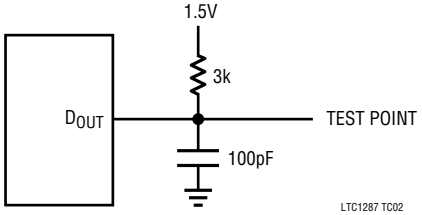
On and Off Channel Leakage Current



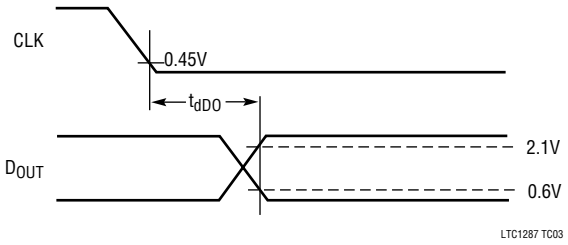
Load Circuit for t_{dis} and t_{en}



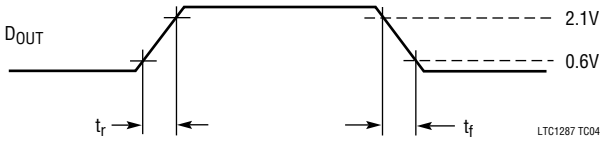
Load Circuit for t_{dDO}, t_r and t_f



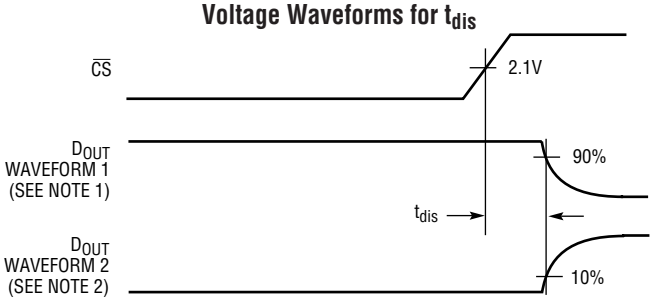
Voltage Waveforms for D_{OUT} Delay Time, t_{dDO}



Voltage Waveforms for D_{OUT} Rise and Fall Times, t_r, t_f

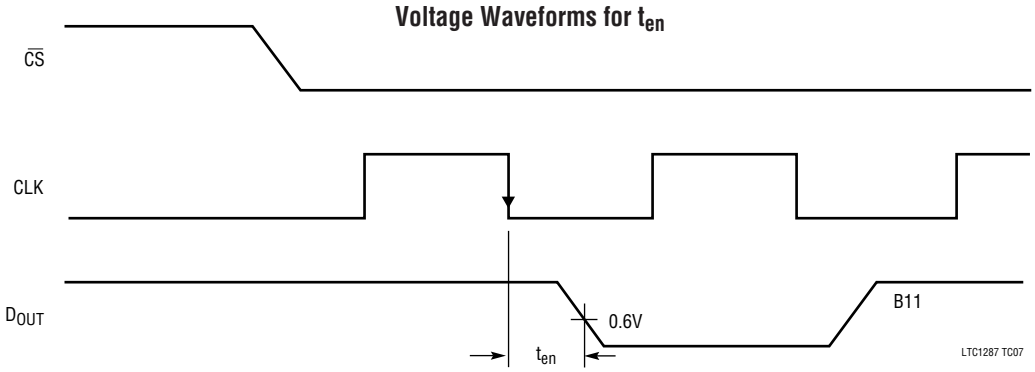


Voltage Waveforms for t_{dis}



NOTE 1: WAVEFORM 1 IS FOR AN OUTPUT WITH INTERNAL CONDITIONS SUCH THAT THE OUTPUT IS HIGH UNLESS DISABLED BY THE OUTPUT CONTROL.
NOTE 2: WAVEFORM 2 IS FOR AN OUTPUT WITH INTERNAL CONDITIONS SUCH THAT THE OUTPUT IS LOW UNLESS DISABLED BY THE OUTPUT CONTROL.

TEST CIRCUITS



APPLICATIONS INFORMATION

The LTC1287 is a data acquisition component which contains the following functional blocks:

1. 12-bit successive approximation capacitive A/D converter
2. Analog multiplexer (MUX)
3. Sample-and-hold (S/H)
4. Synchronous, half-duplex serial interface
5. Control and timing logic

DIGITAL CONSIDERATIONS

Serial Interface

The LTC1287 communicates with microprocessors and other external circuitry via a synchronous, half-duplex, three-wire serial interface (see Operating Sequence). The clock (CLK) synchronizes the data transfer with each bit being transmitted on the falling CLK edge. The LTC1287 does not require a configuration input word and has no D_{IN} pin. It is permanently configured to have a single differential input and to operate in unipolar mode. A falling $\overline{CS}$ initiates data transfer. The first CLK pulse enables D_{OUT}. After one null bit, the A/D conversion result is output on the D_{OUT} line with a MSB-first sequence followed by a LSB-first sequence. With the half duplex serial interface the D_{OUT} data is from the current conversion. This provides easy interface to MSB- or LSB-first serial ports. Bringing $\overline{CS}$ high resets the LTC1287 for the next data exchange.

Logic Levels

The logic level standards for this supply range have not been well defined. What standards that do exist are not universally accepted. The trip point on the logic inputs of the LTC1287 is $0.28 \times V_{CC}$. This makes the logic inputs compatible with HC-type levels and processors that are

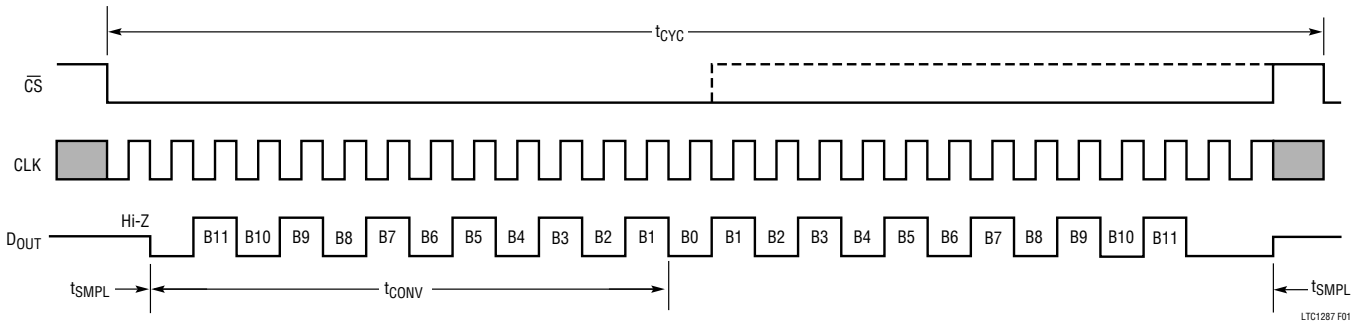


Figure 1. LTC1287 Operating Sequence

APPLICATIONS INFORMATION

specified at 3.3V. The output D_{OUT} is also compatible with the above standards. The following summarizes such levels.

V_{OH} (no load)	$V_{CC} - 0.1V$
V_{OL} (no load)	0.1V
V_{OH}	$0.9 \times V_{CC}$
V_{OL}	$0.1 \times V_{CC}$
V_{IH}	$0.7 \times V_{CC}$
V_{IL}	$0.2 \times V_{CC}$

The LTC1287 can be driven with 5V logic even when V_{CC} is at 3.3V. This is due to a unique input protection device that is found on the LTC1287.

Microprocessor Interfaces

The LTC1287 can interface directly (without external hardware) to most popular microprocessor (MPU) synchronous serial formats. If an MPU without a serial interface is used, then three of the MPU's parallel port lines can be programmed to form the serial link to the LTC1287. Many of the popular MPUs can operate with 3V supplies. For example the MC68HC11 is an MPU with a serial format (SPI). Likewise parallel MPUs that have the 8051 type architecture are also capable of operating at this voltage range. The code for these processors remains the same and can be found in the LTC1292 data sheet.

Sharing the Serial Interface

The LTC1287 can share the same two-wire serial interface with other peripheral components or other LTC1287s (Figure 2). In this case, the $\overline{CS}$ signals decide which LTC1287 is being addressed by the MPU.

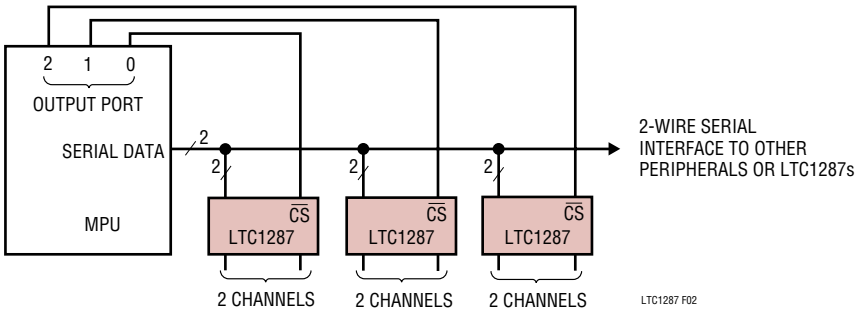


Figure 2. Several LTC1287s Sharing One 2-Wire Serial Interface

ANALOG CONSIDERATIONS

Grounding

The LTC1287 should be used with an analog ground plane and single point grounding techniques. Do not use wire wrapping techniques to breadboard and evaluate the device. To achieve the optimum performance use a PC board. The ground pin (Pin 4) should be tied directly to the ground plane with minimum lead length (a low profile socket is fine). Pin 7 (V_{CC}) should be bypassed to the ground plane with a 22µF (minimum value) tantalum with leads as short as possible and as close as possible to the pin. A 0.1µF ceramic disk also should be placed in parallel with the 22µF and again with leads as short as possible and as close to V_{CC} as possible. Figure 3 shows an example of an ideal LTC1287 ground plane design for a two-sided board. Of course this much ground plane will not always be possible, but users should strive to get as close to this ideal as possible.

Bypassing

For good performance, V_{CC} must be free of noise and ripple. Any changes in the V_{CC} voltage with respect to ground during a conversion cycle can induce errors or noise in the output code. V_{CC} noise and ripple can be kept below 0.5mV by bypassing the V_{CC} pin directly to the analog plane with a minimum of 22µF tantalum capacitor and with leads as short as possible. The lead from the device to the V_{CC} supply also should be kept to a minimum and the V_{CC} supply should have a low output impedance

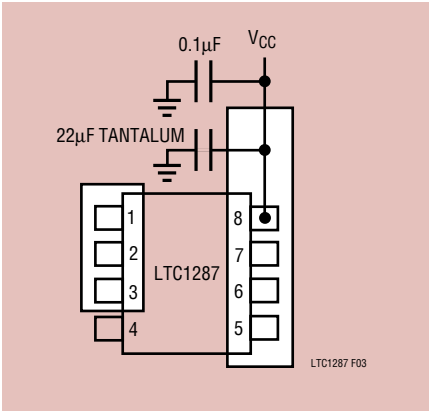


Figure 3. Example Ground Plane for the LTC1287

APPLICATIONS INFORMATION

such as obtained from a voltage regulator (e.g., LT1117). For high frequency bypassing a 0.1µF ceramic disk placed in parallel with the 22µF is recommended. Again the leads should be kept to a minimum. Using a battery to power the LTC1287 will help reduce the amount of bypass capacitance required on the V_{CC} pin. A battery placed close to the device will only require 10µF to adequately bypass the supply pin. Figure 4 shows the effect of poor V_{CC} bypassing. Figure 5 shows the settling of a LT1117 low dropout regulator with a 22µF bypass capacitor. The noise and ripple is kept around 0.5mV. Figure 6 shows the response of a lithium battery with a 10µF bypass capacitor. The noise and ripple is kept below 0.5mV.

Analog Inputs

Because of the capacitive redistribution A/D conversion techniques used, the analog inputs of the LTC1287 have capacitive switching input current spikes. These current spikes settle quickly and do not cause a problem. If large source resistances are used or if slow settling op amps drive the inputs, take care to insure the transients caused by the current spikes settle completely before the conversion begins.

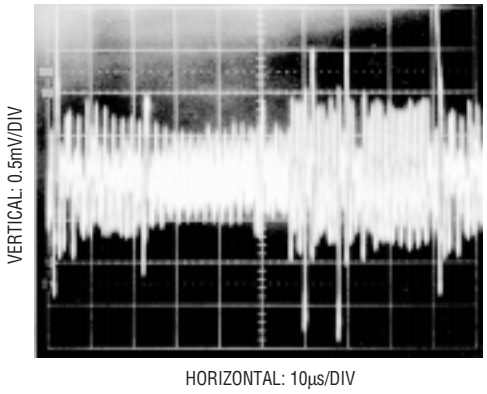


Figure 4. Poor V_{CC} Bypassing. Noise and Ripple Can Cause A/D Errors

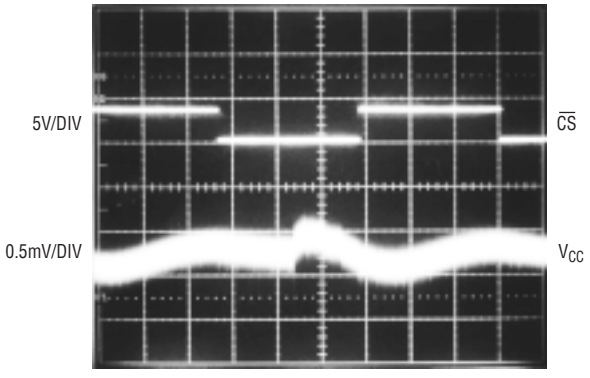


Figure 5. LT1117 Regulator with 22µF Bypassing on V_{CC}

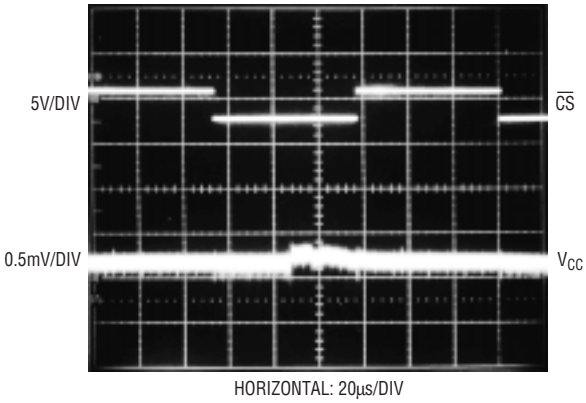


Figure 6. Lithium Battery with 10µF Bypassing on V_{CC}

Source Resistance

The analog inputs of the LTC1287 look like a 100pF capacitor (C_{IN}) in series with a 1.5k resistor (R_{ON}). This value for R_{ON} is for V_{CC} = 2.7V. With larger supply voltages R_{ON} will be reduced. For example, with V_{CC} = 2.7V and V^- = –2.7V, R_{ON} becomes 500Ω. C_{IN} gets switched between (+) and (–) inputs once during each conversion cycle. Large external source resistors and capacitances will slow the settling of the inputs. It is important that the overall RC time constant is short enough to allow the analog inputs to settle completely within the allowed time.

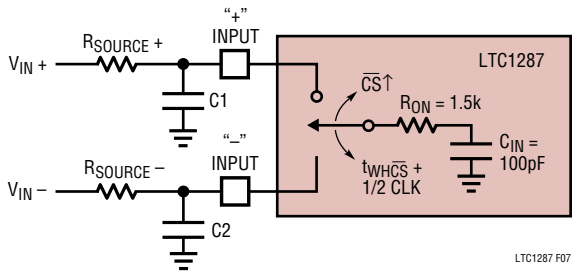


Figure 7. Analog Input Equivalent Circuit

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"+" Input Settling

The input capacitor is switched onto the "+" input during the sample phase (t_{SMPL}, see Figures 8a, 8b and 8c). The sample period can be as short as t_{WHCS} + 0.5 CLK cycle or as long as t_{WHCS} + 1.5 CLK cycles before a conversion starts. This variability depends on where $\overline{CS}$ falls relative to CLK. The voltage on the "+" input must settle completely within the sample period. Minimizing R_{SOURCE}+ and C1 will improve the settling time. If large "+" input source resistance must be used, the sample time can be increased by using a slower CLK frequency. With the minimum possible sample time of 6.0µs, **R_{SOURCE}+ < 4.0k and C1 < 20pF will provide adequate settle time.**

"–" Input Settling

At the end of the sample phase the input capacitor switches to the "–" input and the conversion starts (see Figures 8a, 8b and 8c). During the conversion, the "+" input voltage is

"+" and "–" Input Settling Windows

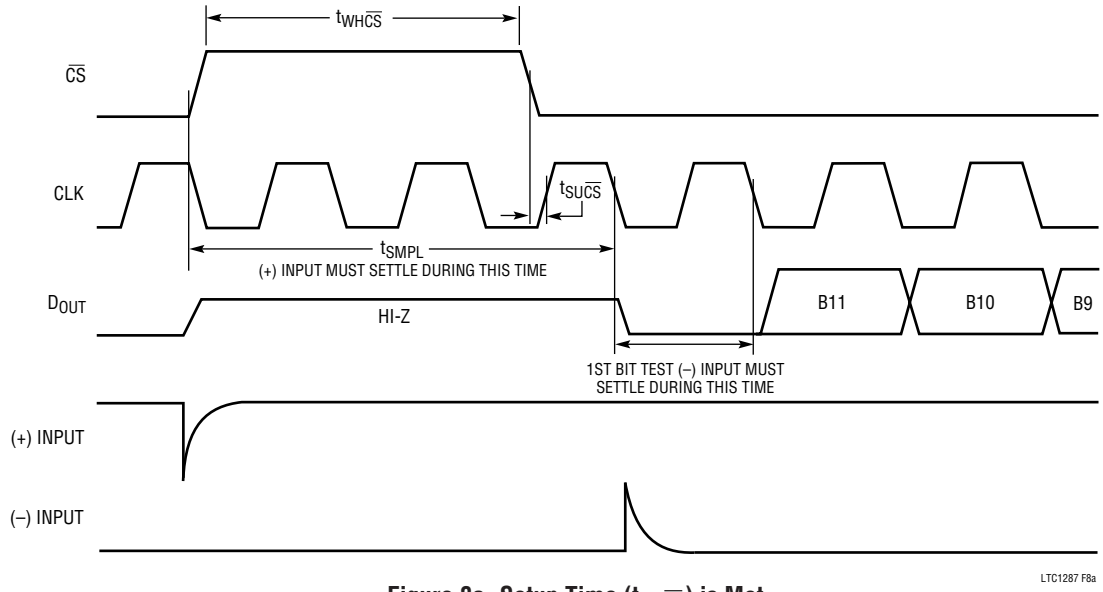


Figure 8a. Setup Time (t_{SUCS}) is Met

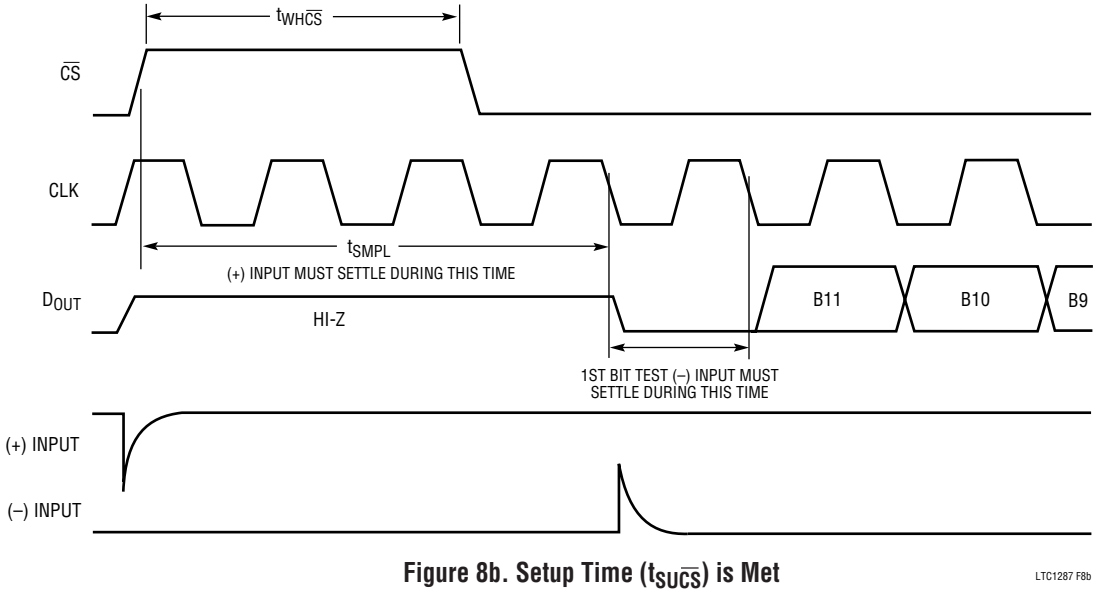


Figure 8b. Setup Time (t_{SUCS}) is Met

APPLICATIONS INFORMATION

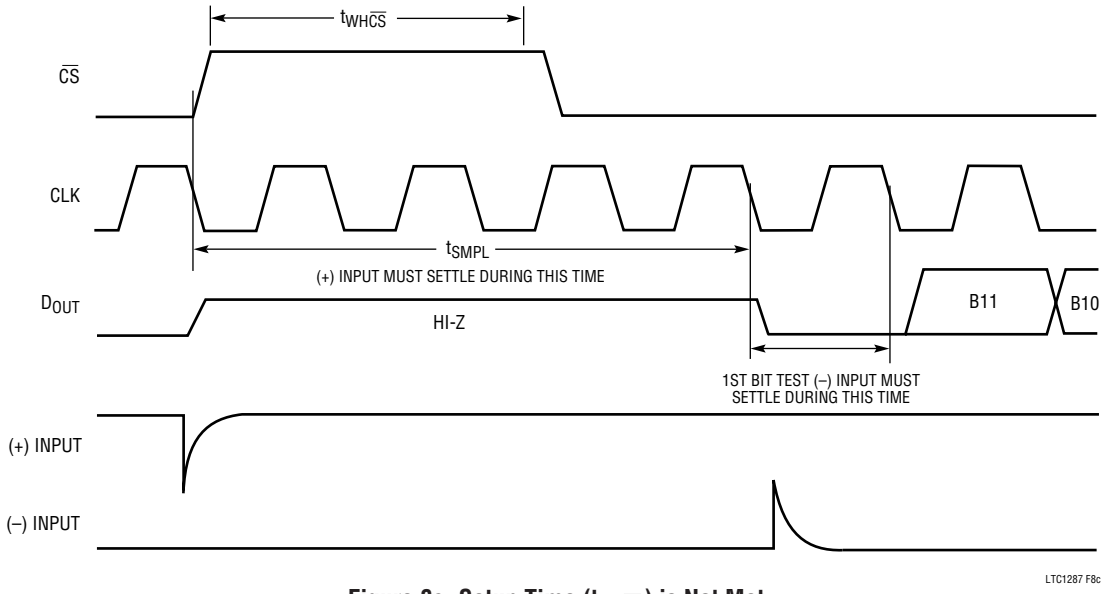


Figure 8c. Setup Time (t_{SUCS}) is Not Met

effectively "held" by the sample and hold and will not affect the conversion result. It is critical that the "–" input voltage be free of noise and settle completely during the first CLK cycle of the conversion. Minimizing R_{SOURCE}– and C2 will improve settling time. If large "–" input source resistance must be used the time can be extended by using a slower CLK frequency. At the maximum CLK frequency of 500kHz, **R_{SOURCE}– < 200Ω and C2 < 20pF will provide adequate settling.**

Input Op Amps

When driving the analog inputs with an op amp it is important that the op amp settles within the allowed time (see Figures 8a, 8b and 8c). Again the "+" and "–" input sampling times can be extended as described above to accommodate slower op amps. For single supply low voltage application the LT1797 and LT1677 can be made to settle well even with the minimum settling windows of 6µs ("+" input) and 2µs ("–" input) which occur at the maximum clock rates (CLK = 500kHz). Figures 9 and 10 show examples of adequate and poor op amp settling. The LT1077, LT1078 or LT1079 can be used here to reduce power consumption. Placing an RC network at the output of the op amps will inprove the settling response and also reduce the broadband noise.

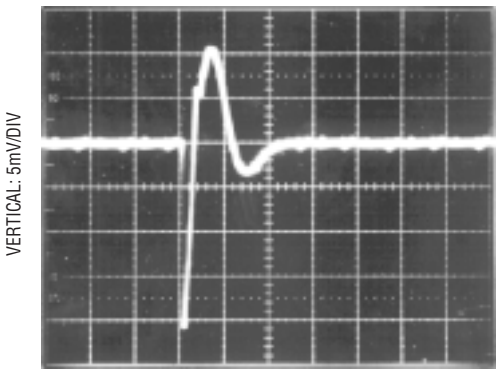


Figure 9. Adequate Settling of Op Amp Driving Analog Input

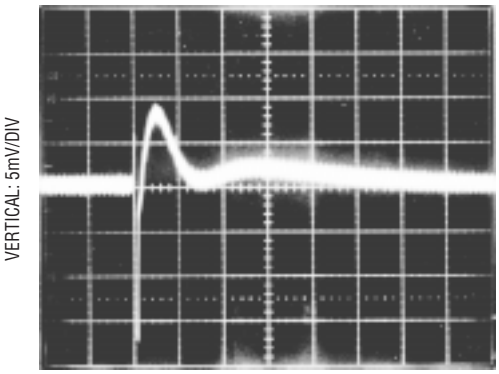


Figure 10. Poor Op Amp Settling Can Cause A/D Errors

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RC Input filtering

It is possible to filter the inputs with an RC network as shown in Figure 11. For large values of C_F (e.g., 1µF) the capacitive input switching currents are averaged into a net DC current. A filter should be chosen with a small resistor and large capacitor to prevent DC drops across the resistor. The magnitude of the DC current is approximately $I_{DC} = 100pF \times V_{IN}/t_{CYC}$ and is roughly proportional to V_{IN}. When running at the minimum cycle time of 33µs, the input current equals 7.6µA at V_{IN} = 2.5V. Here a filter resistor of 8Ω will cause 0.1LSB of full-scale error. If a large filter resistor must be used, errors can be reduced by increasing the cycle time as shown in the Typical Performance Characteristics curve Maximum Filter Resistor vs Cycle Time.

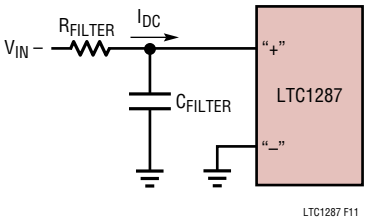


Figure 11. RC Input Filtering

Input Leakage Current

Input leakage currents also can create errors if the source resistance gets too large. For example, the maximum input leakage specification of 1µA (at 85°C) flowing through a source resistance of 1k will cause a voltage drop of 1mV or 1.6LSB with V_{REF} = 2.5V. This error will be much reduced at lower temperatures because leakage drops rapidly (see Typical Performance Characteristics curve Input Channel Leakage Current vs Temperature).

SAMPLE-AND-HOLD

Single-Ended Input

The LTC1287 provides a built-in sample and hold (S&H) function on the +IN input for signals acquired in the single ended mode (–IN pin grounded). The sample and hold allows the LTC1287 to convert rapidly varying signals (see Typical Performance Characteristics curve of S&H Acquisition Time vs Source Resistance). The input voltage is sampled during the t_{SMPL} time as shown in Figure 8. The sampling interval begins at rising edge of $\overline{CS}$ and continues until the falling edge of the CLK before the conversion begins. On this falling edge the S&H goes into the hold mode and the conversion begins.

Differential Input

With a differential input the A/D no longer converts a single voltage but converts the difference between two voltages. The voltage on the +IN pin is sampled and held and can be rapidly time varying. The voltage on the –IN pin must remain constant and be free of noise and ripple throughout the conversion time. Otherwise the differencing operation will not be done accurately. The conversion time is 12 CLK cycles. Therefore a change in the –IN input voltage during this interval can cause conversion errors. For a sinusoidal voltage on the –IN input this error would be:

$$V_{ERROR(MAX)} = \left(2\pi f_{(-IN)} V_{PEAK}\right)\left(\frac{12}{f_{CLK}}\right)$$

Where $f_{(-IN)}$ is the frequency of the –IN input voltage, V_{PEAK} is its peak amplitude and f_{CLK} is the frequency of the CLK. Usually V_{ERROR} will not be significant. For a 60Hz signal on the –IN input to generate a 0.25LSB error (150µV) with the converter running at CLK = 500kHz, its peak value would have to be 16mV. Rearranging the above equation, the maximum sinusoidal signal that can be digitized to a given accuracy is given as:

$$f_{(-IN)MAX} = \left(\frac{V_{ERROR(MAX)}}{2\pi V_{PEAK}}\right)\left(\frac{f_{CLK}}{12}\right)$$

For 0.25LSB error (150µV) the maximum input sinusoid with a 2.5V peak amplitude that can be digitized is 0.4Hz.

Reference Input

The voltage on the reference input of the LTC1287 determines the voltage span of the A/D converter. The reference input has transient capacitive switching currents due to the switched capacitor conversion technique (see Figure 12). During each bit test of the

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conversion (every CLK cycle) a capacitive current spike will be generated on the reference pin by the A/D. These current spikes settle quickly and do not cause a problem. If slow settling circuitry is used to drive the reference input, take care to insure that transients caused by these current spikes settle completely during each bit test of the conversion.

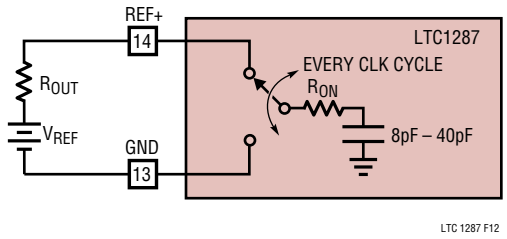


Figure 12. Reference Input Equivalent Circuit

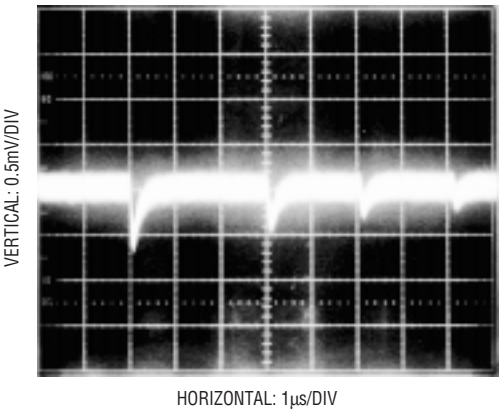


Figure 13. Adequate Reference Settling

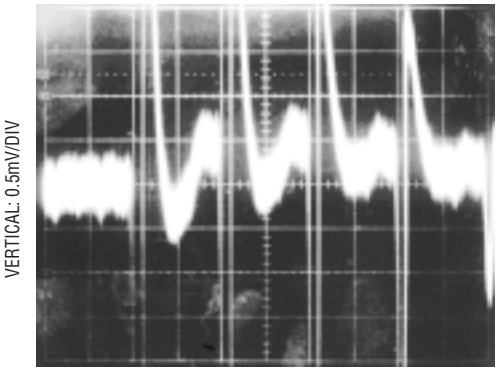


Figure 14. Poor Reference Settling Can Cause A/D Errors

Figures 13 and 14 show examples of both adequate and poor settling. Using a slower CLK will allow more time for the reference to settle. Even at the maximum CLK rate of 500kHz most references and op amps can be made to settle within the 2µs bit time. For example an LT1790 with a 4.7µF bypass capacitor will settle adequately.

Reduced Reference Operation

The effective resolution of the LTC1287 can be increased by reducing the input span of the converter. The LTC1287 exhibits good linearity over a range of reference voltages (seeTypical Performance Characteristics curves of Change in Linearity vs Reference Voltage). Care must be taken when operating at low values of V_{REF} because of the reduced LSB step size and the resulting higher accuracy requirement placed on the converter. Offset and Noise are factors that must be considered when operating at low V_{REF} values.

Offset with Reduced V_{REF}

The offset of the LTC1287 has a larger effect on the output code when the A/D is operated with a reduced reference voltage. The offset (which is typically a fixed voltage) becomes a larger fraction of an LSB as the size of the LSB is reduced. The Typical Performance Characteristics curve of Unadjusted Offset Error vs Reference Voltage shows how offset in LSBs is related to reference voltage for a typical value of V_{OS}. For example a V_{OS} of 0.1mV, which is 0.2LSB with a 2.5V reference becomes 0.4LSB with a 1.25 reference. If this offset is unacceptable, it can be corrected digitally by the receiving system or by offsetting the –IN input to the LTC1287.

Noise with Reduced V_{REF}

The total input referred noise of the LTC1287 can be reduced to approximately 200µV peak-to-peak using a ground plane, good bypassing, good layout techniques and minimizing noise on the reference inputs. This noise is insignificant with a 2.5V reference input but will become a larger fraction of an LSB as the size of the LSB is reduced. The Typical Performance Characteristics

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curve of Noise Error vs Reference Voltage shows the LSB contribution of this 200µV of noise.

For operation with a 2.5V reference, the 200µV noise is only 0.32LSB peak-to-peak. Here the LTC1287 noise will contribute virtually no uncertainty to the output code. For reduced references, the noise may become a significant fraction of an LSB and cause undesirable jitter in the output code. For example, with a 1.25V reference, this 200µV noise is 0.64LSB peak-to-peak. This will reduce the range of input voltages over which a stable output code can be achieved by 0.64LSB. Now averaging readings may be necessary.

This noise data was taken in a very clean test fixture. Any setup induced noise (noise or ripple on V_{CC}, V_{REF} or V_{IN}) will add to the internal noise. The lower the reference voltage used, the more critical it becomes to have a noise-free setup.

Overvoltage Protection

Applying signals to the LTC1287's analog inputs that exceed the positive supply or that go below ground will degrade the accuracy of the A/D and possibly damage the device. For example this condition would occur if a signal is applied to the analog inputs before power is applied to the LTC1287. Another example is the input source operating from different supplies of larger value than the LTC1287. These conditions should be prevented either with proper supply sequencing or by use of external circuitry to clamp or current limit the input source. There are two ways to protect the inputs. In Figure 15 diode clamps from the inputs to V_{CC} and GND are used. The second method is to put resistors in series with the analog inputs for current limiting. Limit the current to 15mA per channel. The +IN input can accept a resistor value of 1k but the –IN input cannot accept more than 200Ω when clocked at its maximum clock frequency of 500kHz. If the LTC1287 is clocked at the maximum clock frequency and 200Ω is not enough to current limit the input source then the clamp diodes are recommended (Figures 16 and 17). The reason for the limit on the resistor value is the MSB bit test is affected by the value of the resistor placed at the –IN input (see discussion on Analog Inputs and the Typical Performance Characteristics curve of Maximum CLK Frequency vs Source Resistance).

If V_{CC} and V_{REF} are not tied together, then V_{CC} should be turned on first, then V_{REF}. If this sequence cannot be met, connecting a diode from V_{REF} to V_{CC} is recommended (see Figure 18).

Because a unique input protection structure is used on the digital input pins, the signal levels on these pins can exceed the device V_{CC} without damaging the device.

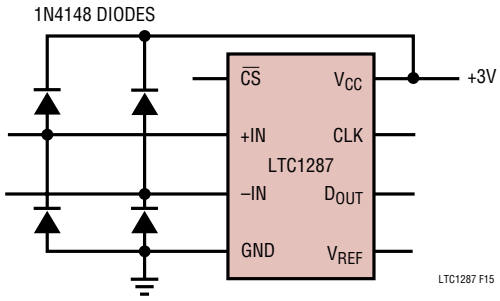


Figure 15. Overvoltage Protection for Inputs

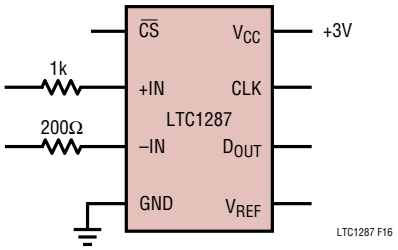


Figure 16. Overvoltage Protection for Inputs

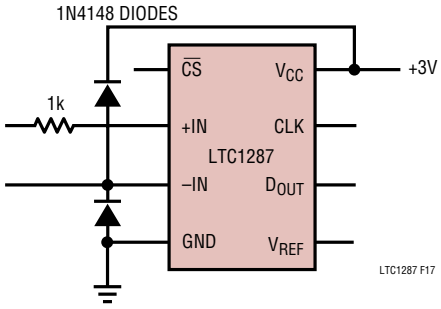


Figure 17. Overvoltage Protection for Inputs

APPLICATIONS INFORMATION

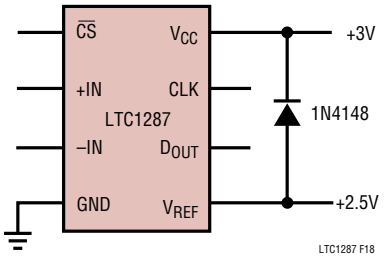


Figure 18

A "Quick Look" Circuit for the LTC1287

Users can get a quick look at the function and timing of the LTC1287 by using the following simple circuit (Figure 19). V_{REF} is tied to V_{CC}. V_{IN} is applied to the +IN input and the –IN input is tied to the ground plane. $\overline{CS}$ is driven at 1/32 the clock rate by the 74HC393 and D_{OUT} outputs the data. The output data from the D_{OUT} pin can be viewed on an oscilloscope that is set up to trigger on the falling edge of $\overline{CS}$ (Figure 20). Note the LSB data is partially clocked out before $\overline{CS}$ goes high.

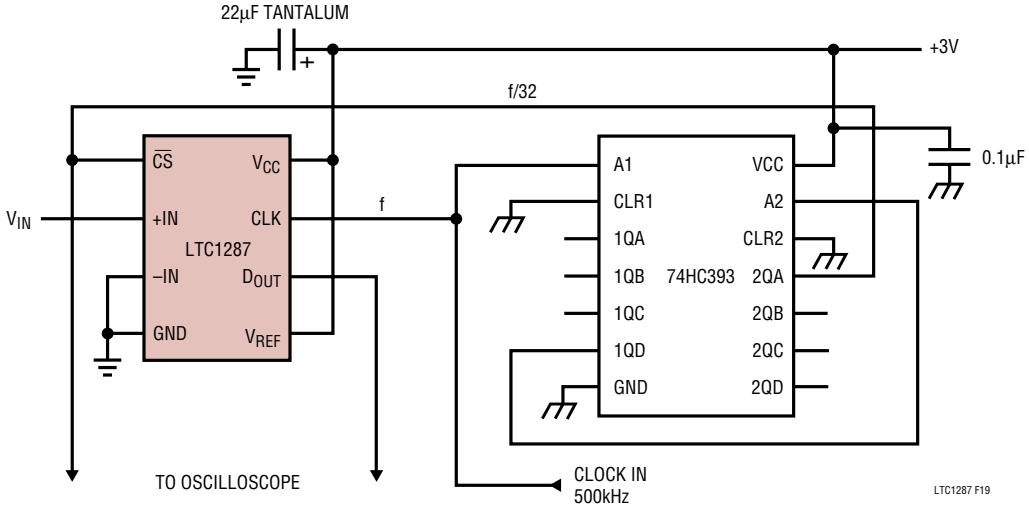


Figure 19. "Quick Look" Circuit for the LTC1287

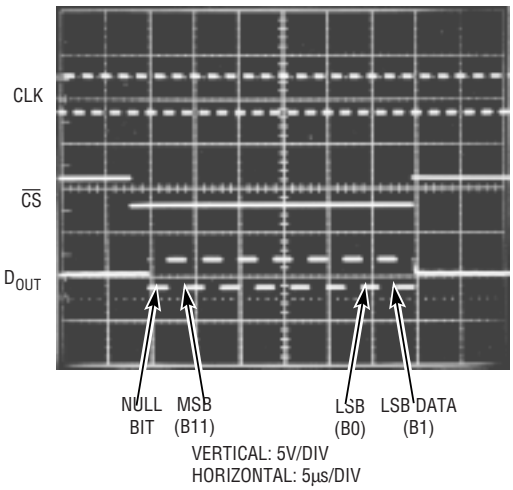
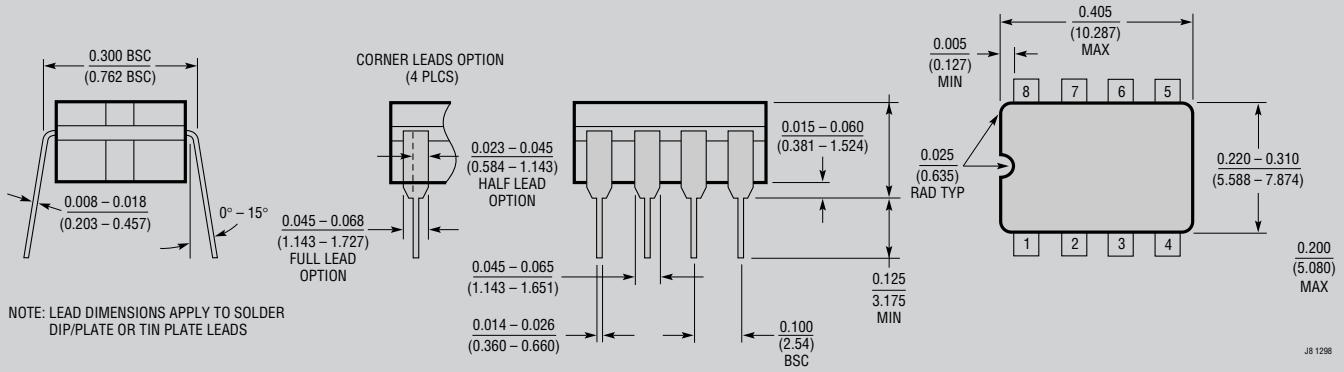


Figure 20. Scope Trace of the LTC1287 "Quick Look" Circuit Showing A/D Output 1010101010 (AAA_{HEX})

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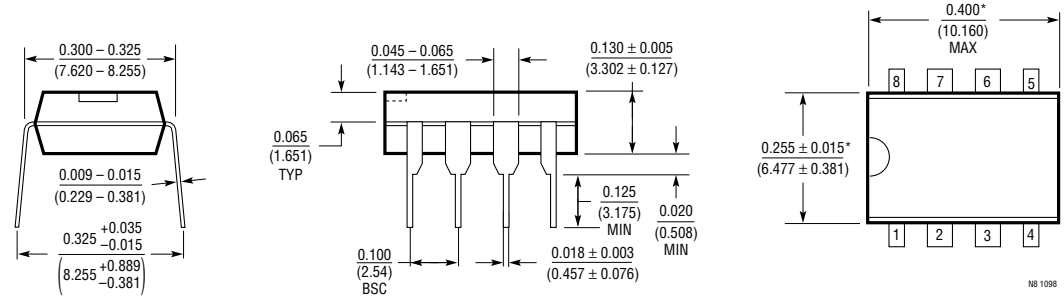
PACKAGE DESCRIPTION

J8 Package
8-Lead CERDIP (Narrow .300 Inch, Hermetic)
(Reference LTC DWG # 05-08-1110)



OBSOLETE PACKAGE

N8 Package
8-Lead PDIP (Narrow .300 Inch)
(Reference LTC DWG # 05-08-1510)



*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.010 INCH (0.254mm)

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1289	12-Bit, 8-Channel Serial ADC	3V or ±3V Supply, Programmable MUX, 25ksps
LTC1401	12-Bit, 200ksps Serial ADC in SO-8	3V Supply, 15mW, Internal References
LTC1594L/LTC1598L	12-Bit, 4-/8-Channel Serial ADC	3V, Micropower, Auto Shutdown, 10ksps
LTC1852/LTC1853	10-Bit/12-Bit, 8-Channel, 400ksps Parallel ADC	3V to 5V Supply, Programmable MUX and Sequencer
LTC1860/LTC1861	12-Bit, 1-/2-Channel Serial ADCs	5V, Micropower, 250ksps, MSOP Package

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