Linear Phase, Group Delay Equalized, 8th Order Lowpass Filter

FEATURES

- Steeper Roll-Off Than Bessel Filters
- High Speed: $f_C \leq 200kHz$
- Phase Equalized Filter in a 14-Pin Package
- Phase and Group Delay Response Fully Tested
- Transient Response Exhibits 5% Overshoot and No Ringing
- 65dB THD or Better Throughout a 100kHz Passband
- No External Components Needed
- Available in Plastic 14-Pin DIP and 16-Pin SO Wide Packages

APPLICATIONS

- Data Communication Filters
- Time Delay Networks
- Phase Matched Filters

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DESCRIPTION

The LTC1264-7 is a clock-tunable monolithic 8th order lowpass filter with linear passband phase and flat group delay. The amplitude response approximates a maximally flat passband and exhibits steeper roll-off than an equivalent 8th order Bessel filter. For instance, at twice the cutoff frequency, the filter attains 28dB attenuation (vs 12dB for Bessel), while at three times the cutoff frequency, the filter attains 55dB attenuation (vs 30dB for Bessel).

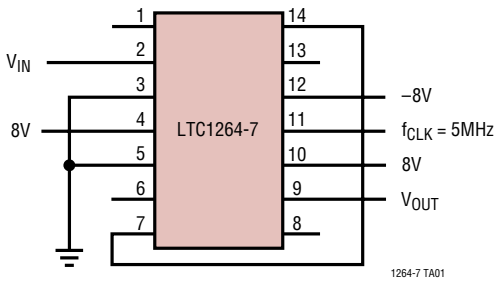
The cutoff frequency of the LTC1264-7 is tuned via an external TTL or CMOS clock. The clock-to-cutoff frequency ratio of the LTC1264-7 can be set to 25:1 (pin 10 to V^+) or 50:1 (pin 10 to V^-). When the filter operates at clock-to-cutoff frequency ratio of 25:1, the input is double-sampled to lower the risk of aliasing.

The LTC1264-7 is optimized for speed. Depending on the operating conditions, cutoff frequencies between 200kHz and 250kHz can be obtained. (Please refer to the Passband vs Clock Frequency graphs.)

The LTC1264-7 is pin-compatible with the LTC1064-X series.

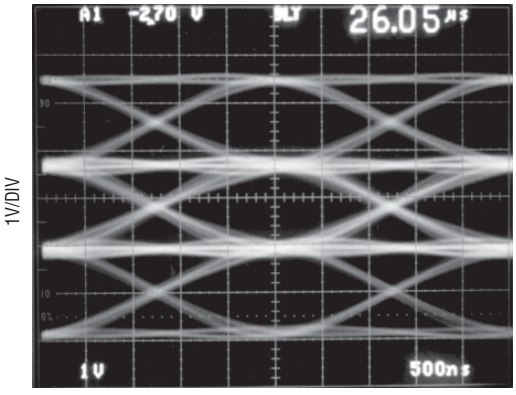
TYPICAL APPLICATION

200kHz Linear Phase Lowpass Filter



NOTE: THE POWER SUPPLIES SHOULD BE BYPASSED BY A 0.1µF CAPACITOR CLOSE TO THE PACKAGE AND ANY PRINTED CIRCUIT BOARD ASSEMBLY SHOULD MAINTAIN A DISTANCE OF AT LEAST 0.2 INCHES BETWEEN ANY OUTPUT OR INPUT PIN AND THE f_{CLK} LINE.

4-Level PAM Eye Diagram



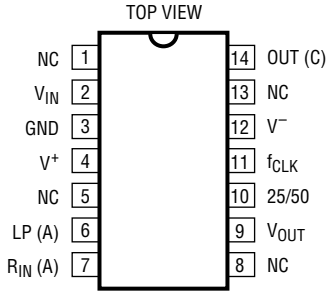
f_{CLK} = 5MHz
f_C = 200kHz

ABSOLUTE MAXIMUM RATINGS (Note 1)

Total Supply Voltage (V^+ to V^-) 16.5V
Power Dissipation 400mW
Burn-In Voltage 16.5V
Voltage at Any Input ..... $(V^- - 0.3V) \leq V_{IN} \leq (V^+ + 0.3V)$
Storage Temperature Range ..... –65°C to 150°C

Operating Temperature Range
LTC1264-7C ..... –40°C to 85°C
LTC1264-7M **(OBSOLETE)** ..... –55°C to 125°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



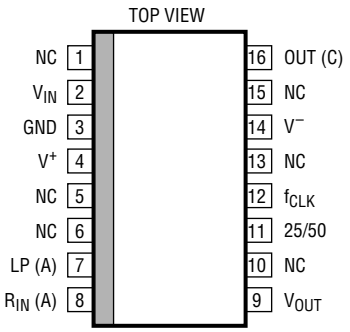
N PACKAGE
14-LEAD PLASTIC DIP
T_{JMAX} = 110°C, θ_{JA} = 65°C/W (N)

ORDER PART NUMBER
LTC1264-7CN

J PACKAGE
14-LEAD CERAMIC DIP
T_{JMAX} = 150°C, θ_{JA} = 65°C/W (J)

ORDER PART NUMBER
LTC1264-7CJ
LTC1264-7MJ

OBSOLETE PACKAGE
Consider the N14 Package for Alternate Source



SW PACKAGE
16-LEAD PLASTIC SO WIDE
T_{JMAX} = 110°C, θ_{JA} = 85°C/W

ORDER PART NUMBER
LTC1264-7CSW

Order Options Tape and Reel: Add #TR Lead Free: Add #PBF Lead Free Tape and Reel: Add #TRPBF
Lead Free Part Marking: http://www.linear.com/leadfree/

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at TA = 25°C. V_S = ±7.5V, R_L = 10k, f_{CUTOFF} = 100kHz or 50kHz, f_{CLK} = 2.5MHz, TTL or CMOS level (maximum clock rise or fall time ≤ 1µs) and all gain measurements are referenced to passband gain, unless otherwise specified.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Passband Gain	0.1Hz ≤ f ≤ 0.25 f_{CUTOFF} f_{TEST} = 25kHz, (f_{CLK}/f_C) = 25:1	 ●	 –0.50	 –0.10	 0.50	 dB
Gain at 0.50 f_{CUTOFF} (Note 4)	f_{TEST} = 50kHz, (f_{CLK}/f_C) = 25:1 f_{TEST} = 25kHz, (f_{CLK}/f_C) = 50:1	● ●	–0.50 –0.65	 –0.15	0.20 0.30	dB dB
Gain at 0.75 f_{CUTOFF}	f_{TEST} = 75kHz, (f_{CLK}/f_C) = 25:1	●	–1.5	–1.0	0.1	dB
Gain at f_{CUTOFF}	f_{TEST} = 100kHz, (f_{CLK}/f_C) = 25:1 f_{TEST} = 50kHz, (f_{CLK}/f_C) = 50:1	● ●	–3.7 –4.5	–3.0 –3.0	–1.9 –2.3	dB dB
Gain at 2.0 f_{CUTOFF}	f_{TEST} = 200kHz, (f_{CLK}/f_C) = 25:1 f_{TEST} = 100kHz, (f_{CLK}/f_C) = 50:1	● ●	–34 –34	–28 –30	–20 –27	dB dB
Gain with f_{CLK} = 20kHz	f_{TEST} = 200Hz, (f_{CLK}/f_C) = 50:1		–0.7	–0.3	0.1	dB
Gain with f_{CLK} = 400kHz, V_S = ±2.375V	f_{TEST} = 8kHz, (f_{CLK}/f_C) = 25:1 f_{TEST} = 16kHz, (f_{CLK}/f_C) = 25:1		–0.2 –3.5	0.15 –2.70	0.5 –1.4	dB dB
Gain with f_{CLK} = 4MHz	f_{TEST} = 160kHz, V_{IN} = 1V_{RMS} (f_{CLK}/f_C) = 25:1, T_A = 0°C to 70°C (f_{CLK}/f_C) = 25:1	 ●	 	 0.00±1.0 	 3.0	 dB dB

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_S = ±7.5V, R_L = 10k, f_{CUTOFF} = 100kHz or 50kHz, f_{CLK} = 2.5MHz, TTL or CMOS level (maximum clock rise or fall time ≤ 1µs) and all gain measurements are referenced to passband gain, unless otherwise specified.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Phase Factor (F) Phase = 180° – F (f/f_C) (Note 2)	(f_{CLK}/f_C) = 25:1, $f \le f_{CUTOFF}$ (f_{CLK}/f_C) = 50:1, $f \le f_{CUTOFF}$ (f_{CLK}/f_C) = 25:1, $f \le f_{CUTOFF}$ (f_{CLK}/f_C) = 50:1, $f \le f_{CUTOFF}$	 ● ●	 392 374	407 ± 2 388 ± 2	 423 414	Deg Deg Deg Deg
Phase Nonlinearity (Note 2)	(f_{CLK}/f_C) = 25:1, $f \le f_{CUTOFF}$ (f_{CLK}/f_C) = 50:1, $f \le f_{CUTOFF}$ (f_{CLK}/f_C) = 25:1, $f \le f_{CUTOFF}$ (f_{CLK}/f_C) = 50:1, $f \le f_{CUTOFF}$	 ● ●	 	±1.0 ±1.0 	 ±2.0 ±2.0	% % % %
Group Delay (t_d) $t_d = (F/360)(1/f_C)$; (Note 3, 4)	(f_{CLK}/f_C) = 25:1, $f \le f_{CUTOFF}$ (f_{CLK}/f_C) = 50:1, $f \le f_{CUTOFF}$ (f_{CLK}/f_C) = 25:1, $f \le f_{CUTOFF}$ (f_{CLK}/f_C) = 50:1, $f \le f_{CUTOFF}$	 ● ●	 10.9 20.8	11.3 21.6 	 11.7 22.9	µs µs µs µs
Group Delay Ripple (Note 3)	(f_{CLK}/f_C) = 25:1, $f \le f_{CUTOFF}$ (f_{CLK}/f_C) = 50:1, $f \le f_{CUTOFF}$ (f_{CLK}/f_C) = 25:1, $f \le f_{CUTOFF}$ (f_{CLK}/f_C) = 50:1, $f \le f_{CUTOFF}$	 ● ●	 	±1.0 ±1.0 	 ±2.0 ±2.0	% % % %
Input Frequency Range (Table 9, 10)	(f_{CLK}/f_C) = 25:1 (f_{CLK}/f_C) = 50:1	 	 	$<f_{CLK}$ $<f_{CLK}/2$	 	kHz kHz
Maximum f_{CLK}	V_S = Single 5V (GND = 2V) V_S = ±5V V_S = ±7.5V	 	 	2 3 5	 	MHz MHz MHz
Clock Feedthrough	25:1, ±7.5V, $f = f_{CLK}$			120		μV_{RMS}
Wideband Noise ($1Hz \le f < f_{CLK}$)	V_S = Single 5V V_S = ±5V V_S = ±7.5V	 	 	140 ± 5% 160 ± 5% 175 ± 5%	 	μV_{RMS} μV_{RMS} μV_{RMS}
Input Impedance			45	65	87	kΩ
Output DC Voltage Swing (Note 5)	V_S = ±2.375V V_S = ±5V V_S = ±7.5V	 ● ●	 ±2.0 ±3.0	±1.0 ±2.3 ±3.8	 	V V V
Output DC Offset (f_{CLK} = 1MHz)	25:1, V_S = ±5V 50:1, V_S = ±5V	 	 	±100 ±100	±220 ±220	mV mV
Output DC Offset TempCo	25:1, V_S = ±5V 50:1, V_S = ±5V	 	 	±200 ±200	 	µV/°C µV/°C
Power Supply Current (f_{CLK} = 1MHz)	V_S = ±2.375V V_S = ±5V V_S = ±7.5V 	 ● ● ●	 	11 14 17 	22 22 23 26 28 32	mA mA mA mA mA mA
Power Supply Range			±2.375		±8	V

ELECTRICAL CHARACTERISTICS

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: Input frequencies, f, are linearly phase shifted through the filter as long as $f \leq f_C$; f_C = cutoff frequency.

Figure 1 curve (A) shows the typical phase response of an LTC1264-7 operating at f_{CLK} = 2.5MHz, f_C = 100kHz. An endpoint straight line, curve (B), depicts the ideal linear phase response of the filter. It is described by: phase shift = $180° - F(f/f_C)$; $f \leq f_C$.

F is arbitrarily called the "phase factor" expressed in degrees. The phase factor together with the specified deviation from the ideal straight line allows the calculation of the phase at a given frequency. Note, the maximum phase nonlinearity, Figure 1, occurs at the vicinity of $f = 0.25\ f_C$ and $= 0.75\ f_C$. Example: The phase shift at 70kHz of the LTC1264-7 shown in Figure 1 is: phase shift = 180° – 407° (70kHz/100kHz) ± nonlinearity = –104.9° ± 1% or –104.9° ± 1.05°.

Note 3: Group delay and group delay deviation are calculated from the measured phase factor and phase deviation specifications.

Note 4: The filter cutoff frequency is abbreviated as f_{CUTOFF} or f_C.

Note 5: The AC swing is typically $9V_{P-P}$, $5.6V_{P-P}$, $1.8V_{P-P}$ with ±7.5V, ±5V, ±2.5V supply respectively. For more information refer to the THD + Noise vs Input graphs.

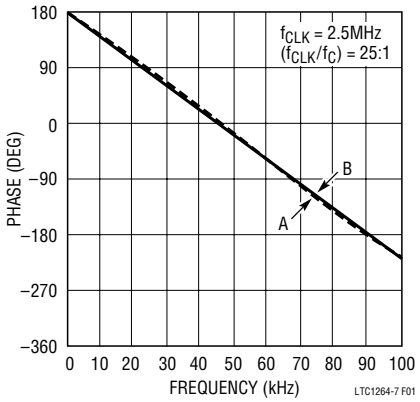
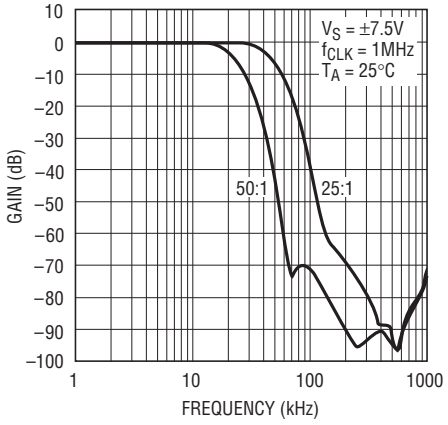


Figure 1. Phase Response in the Passband (Note 2)

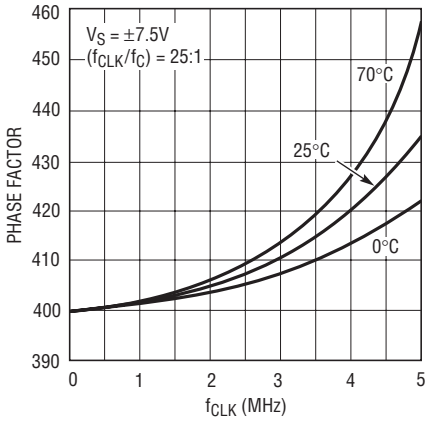
TYPICAL PERFORMANCE CHARACTERISTICS

Gain vs Frequency



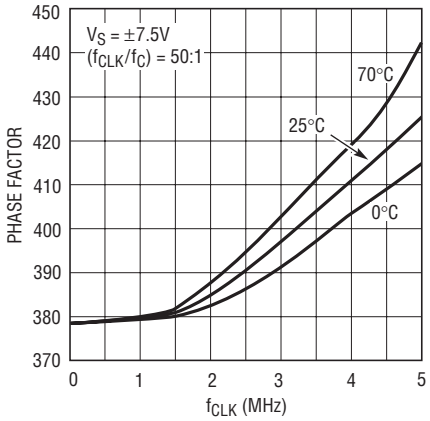
1264-7 G01

Phase Factor vs f_{CLK} (Typical Unit)



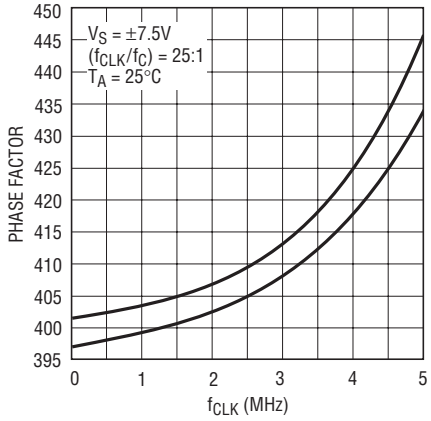
1264-7 G02

Phase Factor vs f_{CLK} (Typical Unit)



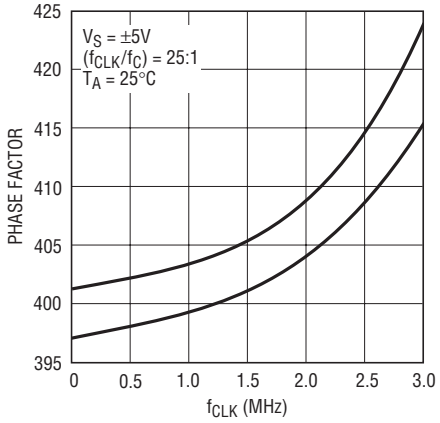
1264-7 G03

Phase Factor vs f_{CLK} (Min and Max Representative Units)



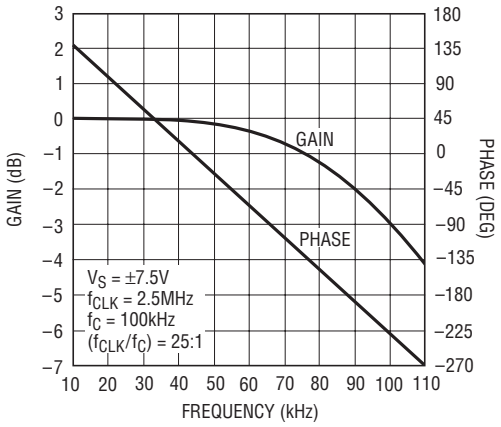
1264-7 G04

Phase Factor vs f_{CLK} (Min and Max Representative Units)



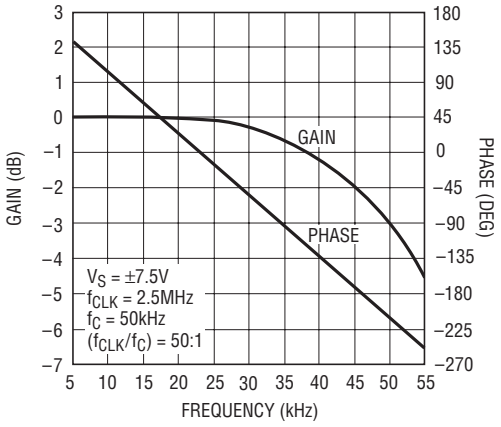
1264-7 G05

Passband Gain and Phase



1264-7 G06

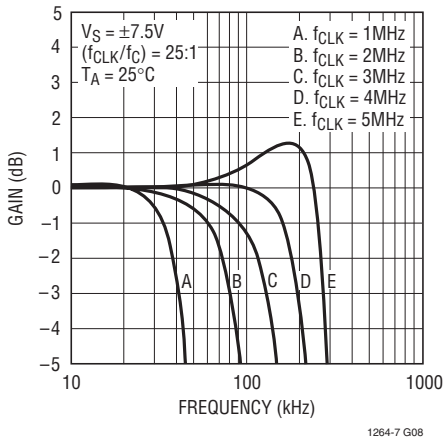
Passband Gain and Phase



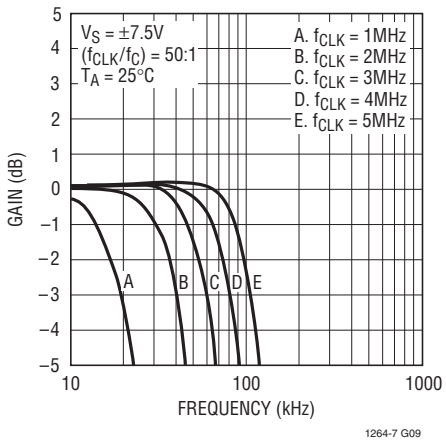
1264-7 G07

TYPICAL PERFORMANCE CHARACTERISTICS

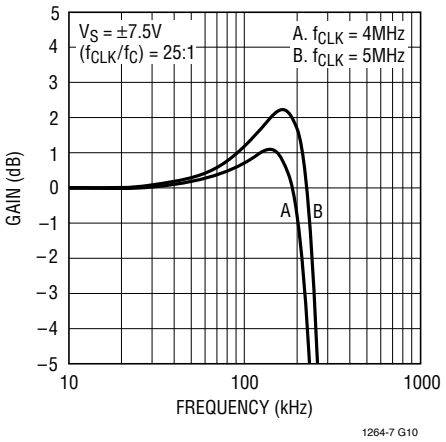
Passband Gain vs f_{CLK}



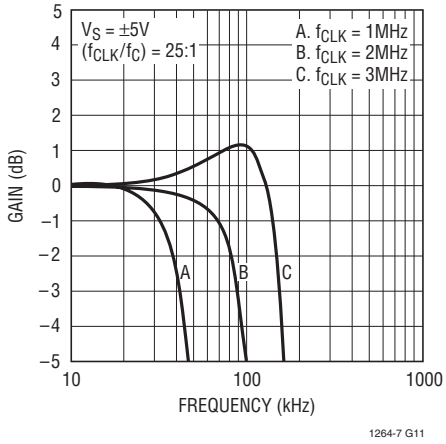
Passband Gain vs f_{CLK}



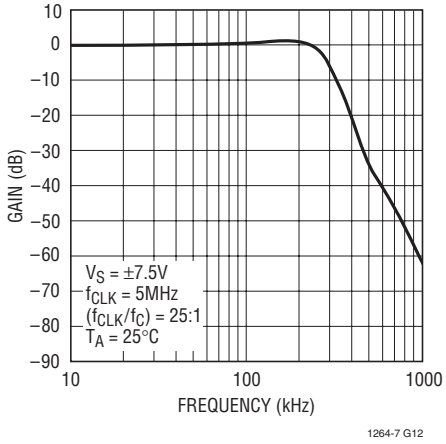
Passband Gain vs f_{CLK} at 85°C



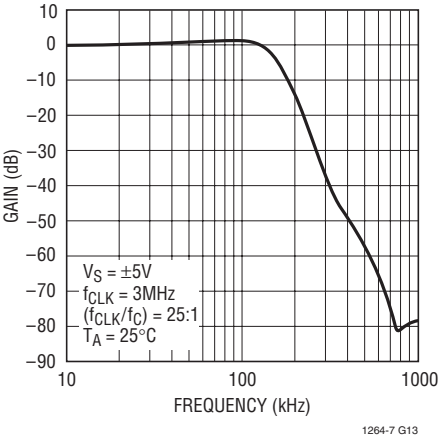
Passband Gain vs f_{CLK} at 85°C



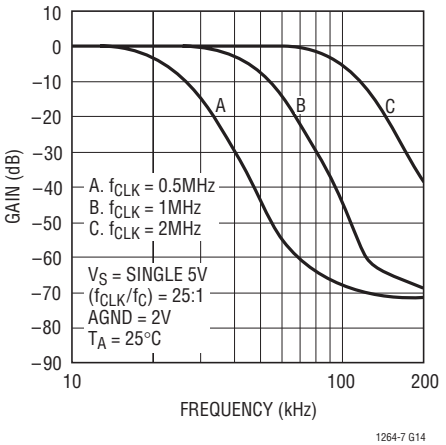
Gain vs Frequency



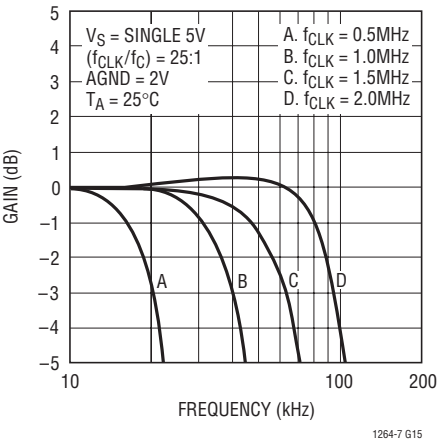
Gain vs Frequency



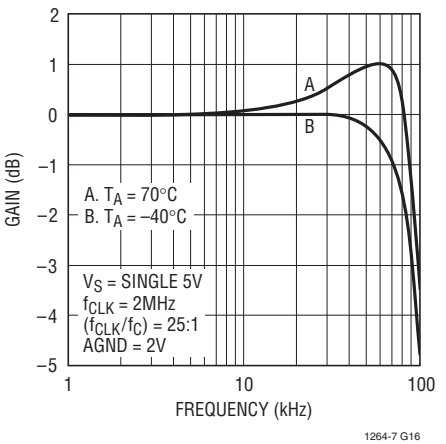
Gain vs f_{CLK}



Passband Gain vs f_{CLK}

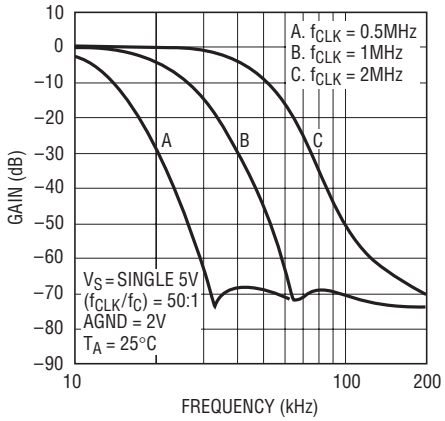


Maximum Passband vs Temperature

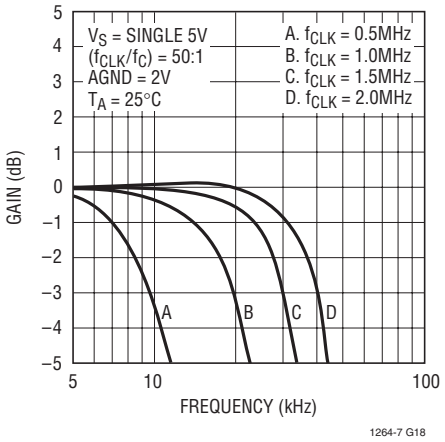


TYPICAL PERFORMANCE CHARACTERISTICS

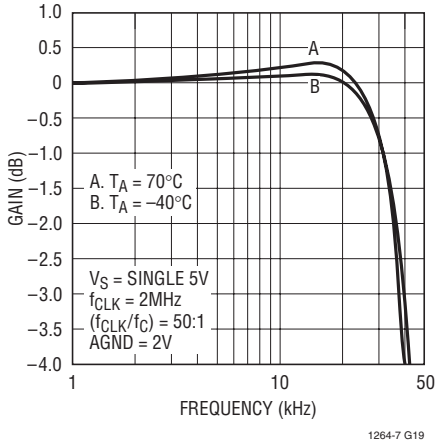
Gain vs f_{CLK}



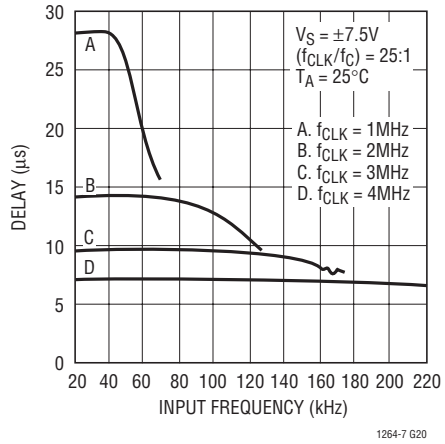
Passband Gain vs f_{CLK}



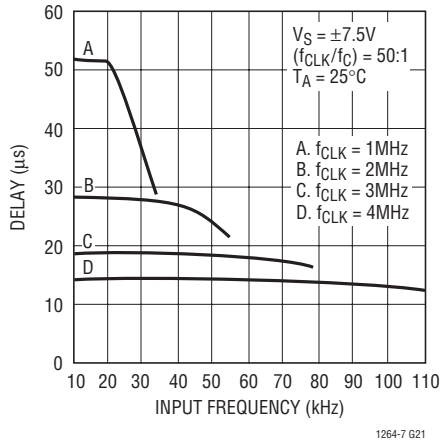
Maximum Passband vs Temperature



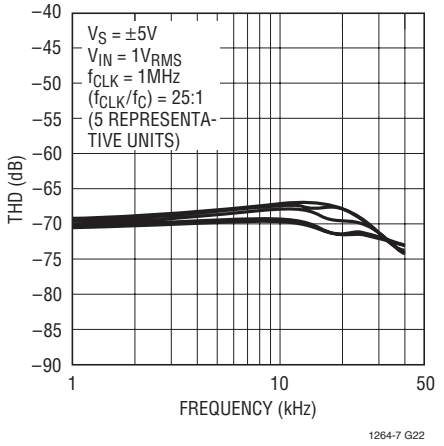
Delay vs f_{CLK}



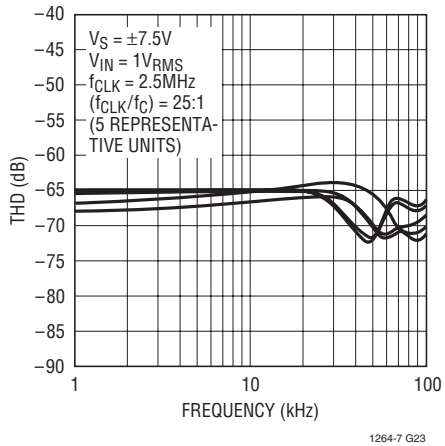
Delay vs f_{CLK}



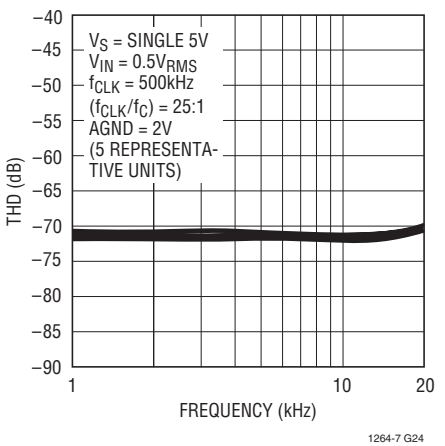
THD vs Frequency



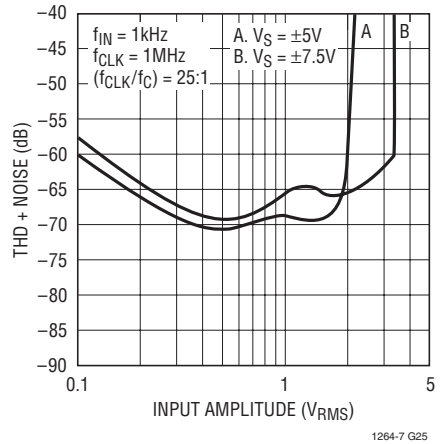
THD vs Frequency



THD vs Frequency

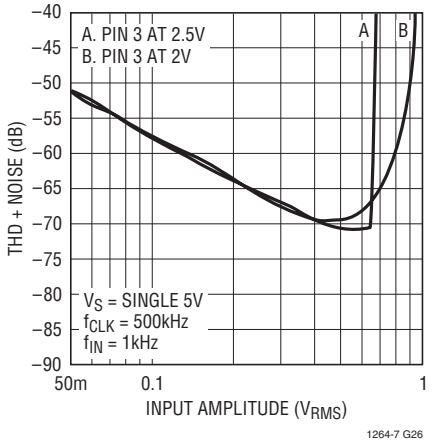


THD + Noise vs Input

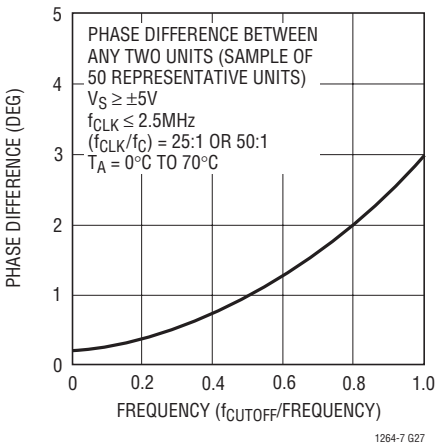


TYPICAL PERFORMANCE CHARACTERISTICS

THD + Noise vs Input



Phase Matching vs Frequency



Power Supply Current vs Power Supply Voltage

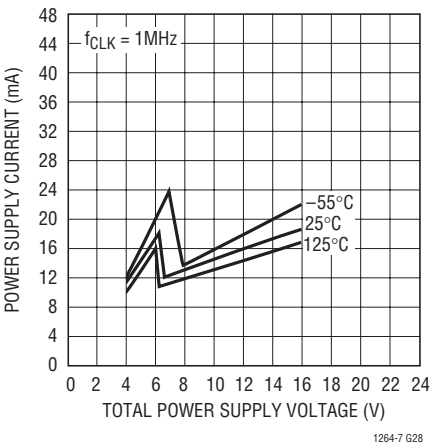


Table 1. Passband Gain and Phase
$V_S = \pm 7.5V$, $(f_{CLK}/f_C) = 25:1$, $T_A = 25°C$

FREQUENCY (kHz)	GAIN (dB)	PHASE (DEG)
f_{CLK} = 1MHz (Typical Unit)		
0.000	0.064	180.00
10.000	0.064	81.14
20.000	0.058	–19.18
30.000	–0.639	–120.63
40.000	–2.741	–221.78
f_{CLK} = 2MHz (Typical Unit)		
0.000	–0.006	180.00
20.000	–0.006	79.42
40.000	–0.164	–22.13
60.000	–0.958	–124.09
80.000	–3.003	–225.01
f_{CLK} = 3MHz (Typical Unit)		
0.000	–0.067	180.00
30.000	–0.067	77.49
60.000	–0.287	–25.54
90.000	–0.944	–128.51
120.000	–2.545	–230.19
f_{CLK} = 4MHz (Typical Unit)		
0.000	–0.031	180.00
40.000	–0.031	75.23
80.000	–0.078	–30.06
120.000	–0.332	–135.27
160.000	–1.275	–239.76
f_{CLK} = 5MHz (Typical Unit)		
0.000	0.073	180.00
50.000	0.073	71.77
100.000	0.365	–37.11
150.000	0.686	–146.19
200.000	0.521	–255.85

Table 2. Passband Gain and Phase
$V_S = \pm 7.5V$, $(f_{CLK}/f_C) = 50:1$, $T_A = 25°C$

FREQUENCY (kHz)	GAIN (dB)	PHASE (DEG)
f_{CLK} = 1MHz (Typical Unit)		
0.000	–0.048	180.00
5.000	–0.048	84.51
10.000	–0.351	–10.87
15.000	–1.253	–105.53
20.000	–3.348	–199.61
f_{CLK} = 2MHz (Typical Unit)		
0.000	–0.008	180.00
10.000	–0.008	83.39
20.000	–0.237	–13.09
30.000	–1.105	–108.91
40.000	–3.238	–204.09
f_{CLK} = 3MHz (Typical Unit)		
0.000	0.044	180.00
15.000	0.044	81.04
30.000	–0.065	–18.64
45.000	–0.863	–118.48
60.000	–3.022	–217.67
f_{CLK} = 4MHz (Typical Unit)		
0.000	0.071	180.00
20.000	0.071	78.04
40.000	0.039	–25.06
60.000	–0.664	–128.54
80.000	–2.755	–231.42
f_{CLK} = 5MHz (Typical Unit)		
0.000	0.089	180.00
25.000	0.089	74.36
50.000	0.141	–32.41
75.000	–1.437	–139.33
100.000	–2.421	–246.01

TYPICAL PERFORMANCE CHARACTERISTICS

Table 3. Passband Gain and Phase
V_S = ±5V, (f_{CLK}/f_C) = 25:1, T_A = 25°C

FREQUENCY (kHz)	GAIN (dB)	PHASE (DEG)
f_{CLK} = 1MHz (Typical Unit)		
0.000	0.081	180.00
10.000	0.081	80.94
20.000	0.071	–19.54
30.000	–0.631	–121.10
40.000	–2.732	–222.28
f_{CLK} = 2MHz (Typical Unit)		
0.000	–0.016	180.00
20.000	–0.016	78.78
40.000	–0.211	–23.21
60.000	–0.968	–125.42
80.000	–2.864	–226.47
f_{CLK} = 3MHz (Typical Unit)		
0.000	–0.006	180.00
30.000	–0.006	76.07
60.000	–0.044	–28.54
90.000	–0.369	–133.27
120.000	–1.507	–237.35

Table 4. Passband Gain and Phase
V_S = ±5V, (f_{CLK}/f_C) = 50:1, T_A = 25°C

FREQUENCY (kHz)	GAIN (dB)	PHASE (DEG)
f_{CLK} = 1MHz (Typical Unit)		
0.000	0.032	180.00
5.000	0.032	84.60
10.000	–0.249	–10.65
15.000	–1.135	–105.20
20.000	–3.225	–199.22
f_{CLK} = 2MHz (Typical Unit)		
0.000	0.101	180.00
10.000	0.101	82.47
20.000	–0.043	–15.45
30.000	–0.864	–113.28
40.000	–3.021	–210.54
f_{CLK} = 3MHz (Typical Unit)		
0.000	0.125	180.00
15.000	0.125	77.88
30.000	0.043	–25.31
45.000	–0.753	–128.74
60.000	–2.987	–231.29

Table 5. Passband Gain and Phase
V_S = Single 5V, (f_{CLK}/f_C) = 25:1, T_A = 25°C

FREQUENCY (kHz)	GAIN (dB)	PHASE (DEG)
f_{CLK} = 0.5MHz (Typical Unit)		
0.000	0.161	180.00
5.000	0.161	81.47
10.000	0.166	–18.52
15.000	–0.515	–119.79
20.000	–2.598	–220.82
f_{CLK} = 1MHz (Typical Unit)		
0.000	0.125	180.00
10.000	0.125	80.23
20.000	0.043	–20.75
30.000	–0.706	–122.53
40.000	–2.781	–223.59
f_{CLK} = 1.5MHz (Typical Unit)		
0.000	0.061	180.00
15.000	0.061	78.49
30.000	–0.096	–23.82
45.000	–0.741	–126.47
60.000	–2.432	–228.12
f_{CLK} = 2MHz (Typical Unit)		
0.000	0.151	180.00
20.000	0.151	75.03
40.000	0.321	–31.15
60.000	0.203	–137.86
80.000	–0.838	–244.58

Table 6. Passband Gain and Phase
V_S = Single 5V, (f_{CLK}/f_C) = 50:1, T_A = 25°C

FREQUENCY (kHz)	GAIN (dB)	PHASE (DEG)
f_{CLK} = 0.5MHz (Typical Unit)		
0.000	0.075	180.00
2.500	0.075	84.79
5.000	–0.217	–10.40
7.500	–1.108	–105.10
10.000	–3.198	–199.26
f_{CLK} = 1MHz (Typical Unit)		
0.000	0.114	180.00
5.000	0.114	83.96
10.000	–0.122	–11.88
15.000	–0.988	–107.02
20.000	–3.111	–201.63
f_{CLK} = 1.5MHz (Typical Unit)		
0.000	0.174	180.00
7.500	0.174	81.36
15.000	0.066	–17.84
22.500	–0.744	–117.12
30.000	–2.949	–215.79
f_{CLK} = 2MHz (Typical Unit)		
0.000	0.232	180.00
10.000	0.232	75.98
20.000	0.219	–29.26
30.000	–0.599	–134.63
40.000	–3.031	–239.09

PIN FUNCTIONS

NC Pin (1, 5, 8, 13)

Pins 1, 5, 8 and 13 are not connected to any internal circuit point on the device and should be preferably tied to analog ground.

Filter Input Pin (2)

The input pin is connected internally through a 50k resistor tied to the inverting input of an op amp.

Analog Ground Pins (3, 5)

The filter performance depends on the quality of the analog signal ground. For either dual or single supply operation, an analog ground plane surrounding the package is recommended. The analog ground plane should be connected to any digital ground at a single point. For dual supply operation, pin 3 should be connected to the analog ground plane. For single supply operation pin 3 should be biased at 1/2 supply and should be bypassed to the analog ground plane with at least a 1µF capacitor (Figure 3). For single 5V operation at the highest f_{CLK} of 2MHz, pin 3 should be biased at 2V. This minimizes passband gain and phase variations.

Power Supply Pins (4, 12)

The V^+ (pin 4) and the V^- (pin 12) should each be bypassed with a 0.1µF capacitor to an adequate analog ground. The filter's power supplies should be isolated from other digital or high voltage analog supplies. A low noise linear supply is recommended. Using a switching power supply will lower the signal-to-noise ratio of the filter. The supply during power-up should have a slew rate less than 1V/µs. When V^+ is applied before V^- and V^- is allowed to go above ground, a signal diode should clamp V^- to prevent latch-up. Figures 2 and 3 show typical connections for dual and single supply operation.

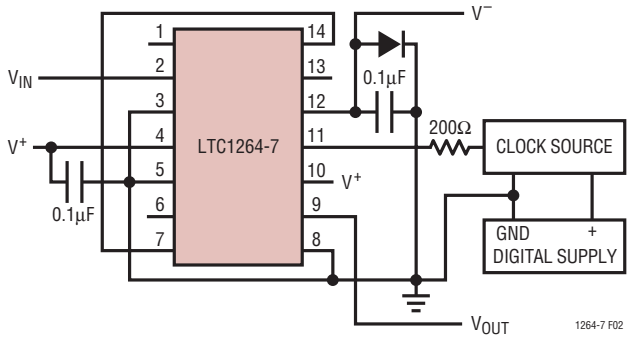


Figure 2. Dual Supply Operation for an f_{CLK}/f_{CUTOFF} = 25:1

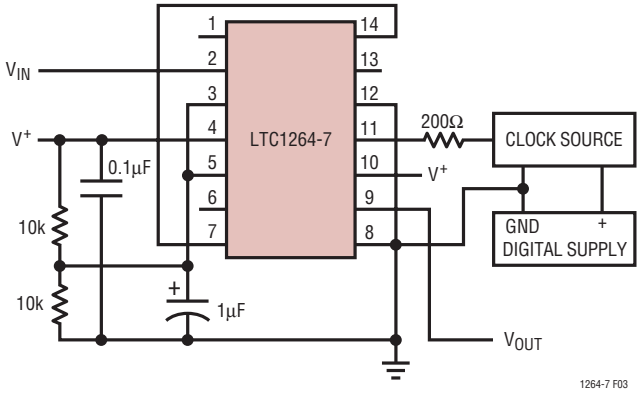


Figure 3. Single Supply Operation for an f_{CLK}/f_{CUTOFF} = 25:1

Filter Output Pins (6, 9)

Pin 9 is the specified output of the filter; it can typically source 3mA and sink 1mA. Driving coaxial cables or resistive loads less than 20k will degrade the total harmonic distortion of the filter. When evaluating the device's distortion an output buffer is required. A noninverting buffer, Figure 4, can be used provided that its input common-mode range is well within the filter's output swing. Pin 6 is an intermediate filter output providing an unspecified 6th order lowpass filter. Pin 6 should not be loaded.

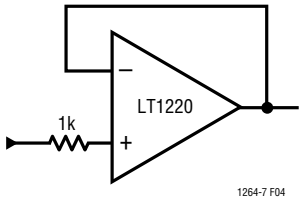


Figure 4. Buffer for Filter Output

PIN FUNCTIONS

External Connection Pins (7, 14)

Pins 7 and 14 should be connected together. In a printed circuit board the connection should be done under the IC package through a short trace surrounded by the analog ground plane.

Ratio Input Pin (10)

The DC level at this pin determines the ratio of the clock frequency to the cutoff frequency of the filter. Pin 10 at V^+ gives a 25:1 ratio and pin 10 at V^- gives a 50:1 ratio. For single supply operation the ratio is 25:1 when pin 10 is at V^+ and 50:1 when pin 10 is at ground. When pin 10 is not tied to ground, it should be bypassed to analog ground with a 0.1µF capacitor. If the DC level at pin 10 is switched mechanically or electrically at slew rates greater than 1V/µs while the device is operating, a 10k resistor should be connected between pin 10 and the DC source.

Clock Input Pin (11)

Any TTL or CMOS clock source with a square-wave output and 50% duty cycle (±10%) is an adequate clock source for the device. The power supply for the clock source should not be the filter's power supply. The analog ground for the filter should be connected to clock's ground at a single point only. Table 7 shows the clock's low and high level threshold values for a dual or single supply operation. A pulse generator can be used as a clock source provided the high level ON time is greater than 0.1µs. Sine waves are not recommended for clock input frequencies less than 100kHz, since excessively slow clock rise or fall times generate internal clock jitter (maximum clock rise or fall time ≤1µs). The clock signal should be routed from the right side of the IC package and perpendicular to it to avoid coupling to any input or output analog signal path. A 200Ω resistor between clock source and pin 11 will slow down the rise and fall times of the clock to further reduce charge coupling (Figures 2 and 3).

Table 7. Clock Source High and Low Threshold Levels

POWER SUPPLY	HIGH LEVEL	LOW LEVEL
Dual Supply = ±7.5V	≥ 2.18V	≤ 0.5V
Dual Supply = ±5V	≥ 1.45V	≤ 0.5V
Dual Supply = ±2.5V	≥ 0.73V	≤ –2.0V
Single Supply = 12V	≥ 7.80V	≤ 6.5V
Single Supply = 5V	≥ 1.45V	≤ 0.5V

APPLICATIONS INFORMATION

Clock Feedthrough

Clock feedthrough is defined as the RMS value of the clock frequency and its harmonics that are present at the filter's output pin (9). The clock feedthrough is tested with the input pin (2) grounded and it depends on PC board layout and on the value of the power supplies. With proper layout techniques the values of the clock feedthrough are shown in Table 8.

Table 8. Clock Feedthrough

V_S	25:1	50:1
Single 5V	$100\mu V_{RMS}$	$100\mu V_{RMS}$
±5V	$100\mu V_{RMS}$	$400\mu V_{RMS}$
±7.5V	$120\mu V_{RMS}$	$1000\mu V_{RMS}$

Note: The clock feedthrough at 25:1 is imbedded in the wideband noise of the filter. Clock waveform is a square wave.

Any parasitic switching transients during the rise and fall edges of the incoming clock are not part of the clock feedthrough specifications. Switching transients have frequency contents much higher than the applied clock; their amplitude strongly depends on scope probing techniques as well as grounding and power supply bypassing. The clock feedthrough, if bothersome, can be greatly reduced by adding a simple R/C lowpass network at the output of the filter pin (9). This R/C will completely eliminate any switching transients.

Wideband Noise

The wideband noise of the filter is the total RMS value of the device's noise spectral density and it is used to determine the operating signal-to-noise ratio. Most of its frequency contents lie within the filter passband and it cannot be reduced with post filtering. For instance, the LTC1264-7 wideband noise at ±5V supply is $160\mu V_{RMS}$, $145\mu V_{RMS}$ of which have frequency contents from DC up to the filter's cutoff frequency. The total wideband noise (μV_{RMS}) is nearly independent of the value of the clock. The clock feedthrough specifications are not part of the wideband noise.

Speed Limitations

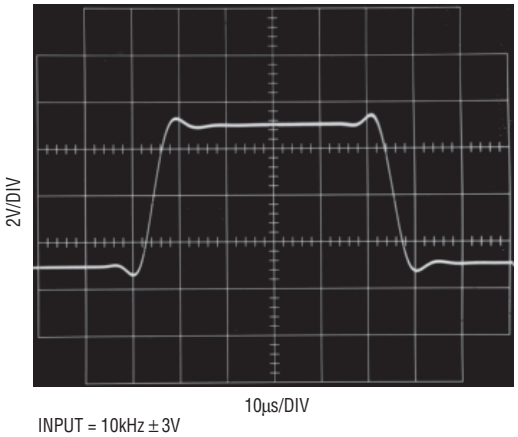
To avoid op amp slew rate limiting at maximum clock frequencies, the signal amplitude should be kept below a specified level as shown in Table 9.

APPLICATIONS INFORMATION

Table 9. Maximum V_{IN} vs V_S and Clock

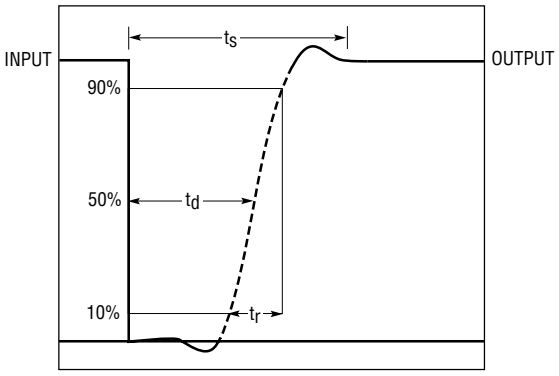
POWER SUPPLY	MAXIMUM f_{CLK}	MAXIMUM V_{IN}
±7.5V	5.0MHz	$1.6V_{RMS}$ ($f_{IN} \geq 160kHz$)
	4.5MHz	$2.0V_{RMS}$ ($f_{IN} \geq 160kHz$)
	4.0MHz	$2.5V_{RMS}$ ($f_{IN} \geq 160kHz$)
	≥3.5MHz	$1.6V_{RMS}$ ($f_{IN} \geq 500kHz$)
±5V	3.0MHz	$1.6V_{RMS}$ ($f_{IN} \geq 100kHz$)
	≥3.0MHz	$0.7V_{RMS}$ ($f_{IN} \geq 500kHz$)
Single 5V	2.0MHz	$0.5V_{RMS}$ ($f_{IN} \geq 400kHz$)

Transient Response



INPUT = 10kHz ± 3V
f_{CLK} = 2.5MHz
RATIO = 25:1

Figure 5



RISE TIME (t_r) = $\frac{0.36}{f_{CUTOFF}}$ ±5%

SETTLING TIME (t_S) = $\frac{2}{f_{CUTOFF}}$ ±5%
(TO 1% of OUTPUT)

TIME DELAY (t_d) = GROUP DELAY ≈ $\frac{1.15}{f_{CUTOFF}}$
(TO 50% OF OUTPUT)

1164-7 F06

Figure 6

Aliasing

Aliasing is an inherent phenomenon of sampled data systems and it occurs when input frequencies close to the sampling frequency are applied. For the LTC1264-7 case at 50:1, an input signal whose frequency is in the range of $f_{CLK} \pm 10\%$, will be aliased back into the filter's passband. If, for instance, an LTC1264-7 operating with a 100kHz clock and 2kHz cutoff frequency receives a 95kHz 10mV input signal, a 5kHz $56\mu V_{RMS}$ alias signal will appear at its output. When the LTC1264-7 operates with a clock-to-cutoff frequency of 25:1, aliasing occurs at twice the clock frequency. Table 10 shows details.

Table 10. Aliasing (f_{CLK} = 100kHz)

INPUT FREQUENCY (V_{IN} = $1V_{RMS}$, $f_{IN} = f_{CLK} \pm f_{OUT}$) (kHz)	OUTPUT LEVEL (Relative to Input, 0dB = $1V_{RMS}$) (dB)	OUTPUT FREQUENCY (Aliased Frequency f_{OUT} = ABS [$f_{CLK} \pm f_{IN}$]) (kHz)
25:1, f_{CUTOFF} = 4kHz		
175 (or 225)	–76	25
180 (or 220)	–69	20
185 (or 215)	–62	15
190 (or 210)	–43	10
195 (or 205)	–7	5
50:1, f_{CUTOFF} = 2kHz		
75 (or 125)	–96	25
80 (or 120)	–90	20
85 (or 115)	–82	15
90 (or 110)	–72	10
95 (or 105)	–45	5
99 (or 101)	0	1

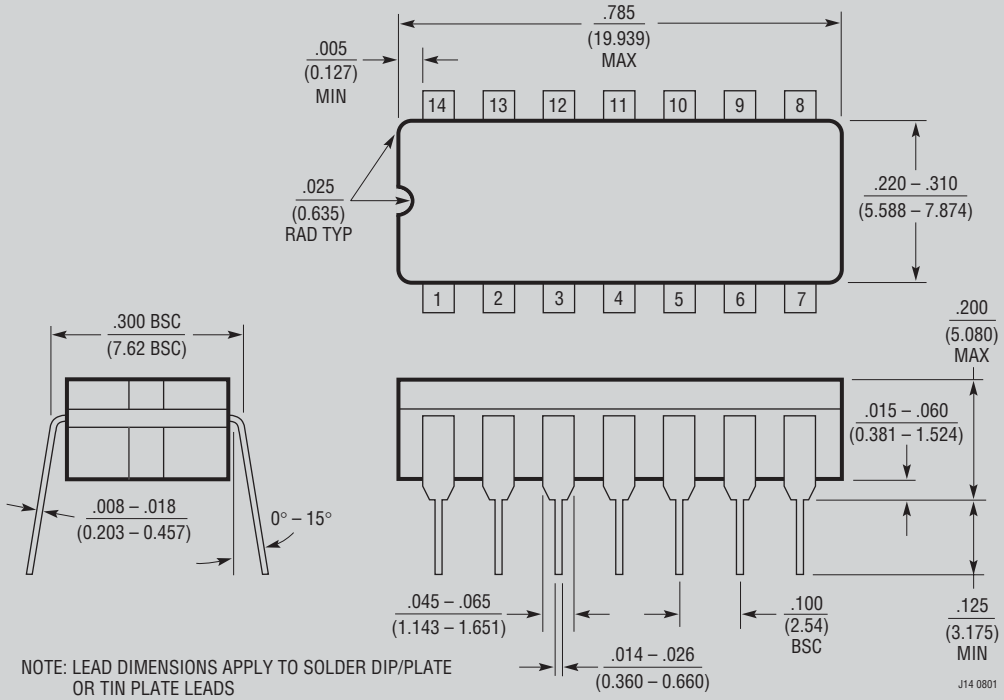
Table 11. Transient Response of LTC Lowpass Filters

LOWPASS FILTER	DELAY TIME* (SEC)	RISE TIME** (SEC)	SETTLING TIME*** (SEC)	OVER-SHOOT (%)
LTC1064-3 Bessel	$0.50/f_C$	$0.34/f_C$	$0.80/f_C$	0.5
LTC1164-5 Bessel	$0.43/f_C$	$0.34/f_C$	$0.85/f_C$	0
LTC1164-6 Bessel	$0.43/f_C$	$0.34/f_C$	$1.15/f_C$	1
LTC1264-7 Linear Phase	$1.15/f_C$	$0.36/f_C$	$2.05/f_C$	5
LTC1164-7 Linear Phase	$1.20/f_C$	$0.39/f_C$	$2.20/f_C$	5
LTC1064-7 Linear Phase	$1.20/f_C$	$0.39/f_C$	$2.20/f_C$	5
LTC1164-5 Butterworth	$0.80/f_C$	$0.48/f_C$	$2.40/f_C$	11
LTC1164-6 Elliptic	$0.85/f_C$	$0.54/f_C$	$4.30/f_C$	18
LTC1064-4 Elliptic	$0.90/f_C$	$0.54/f_C$	$4.50/f_C$	20
LTC1064-1 Elliptic	$0.85/f_C$	$0.54/f_C$	$6.50/f_C$	20

* To 50% ±5%, ** 10% to 90% ±5%, *** To 1% ±0.5%

PACKAGE DESCRIPTION

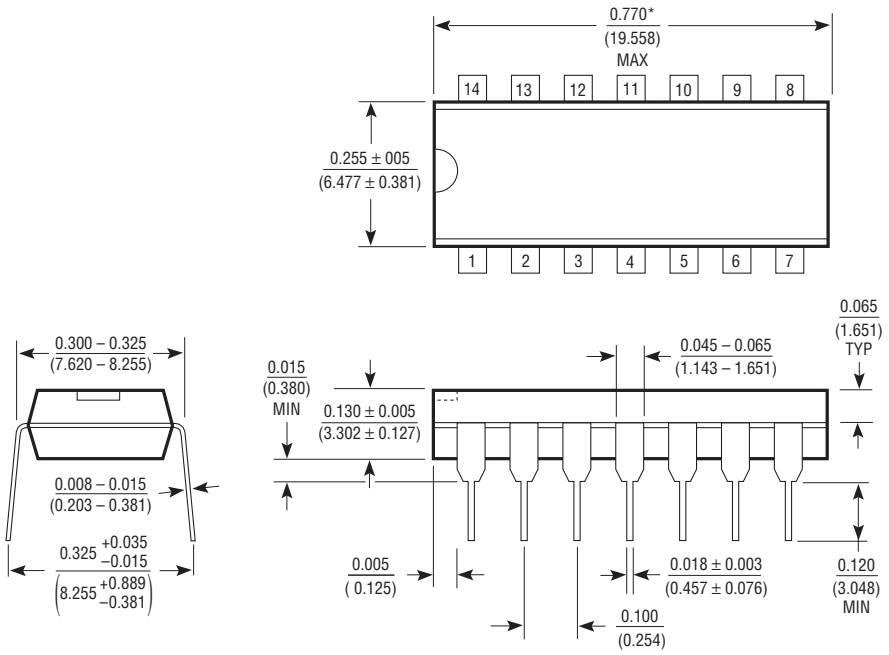
J Package
14-Lead CERDIP (Narrow .300 Inch, Hermetic)
(Reference LTC DWG # 05-08-1110)



OBSOLETE PACKAGE

PACKAGE DESCRIPTION

N Package
14-Lead PDIP (Narrow .300 Inch)
(Reference LTC DWG # 05-08-1510)



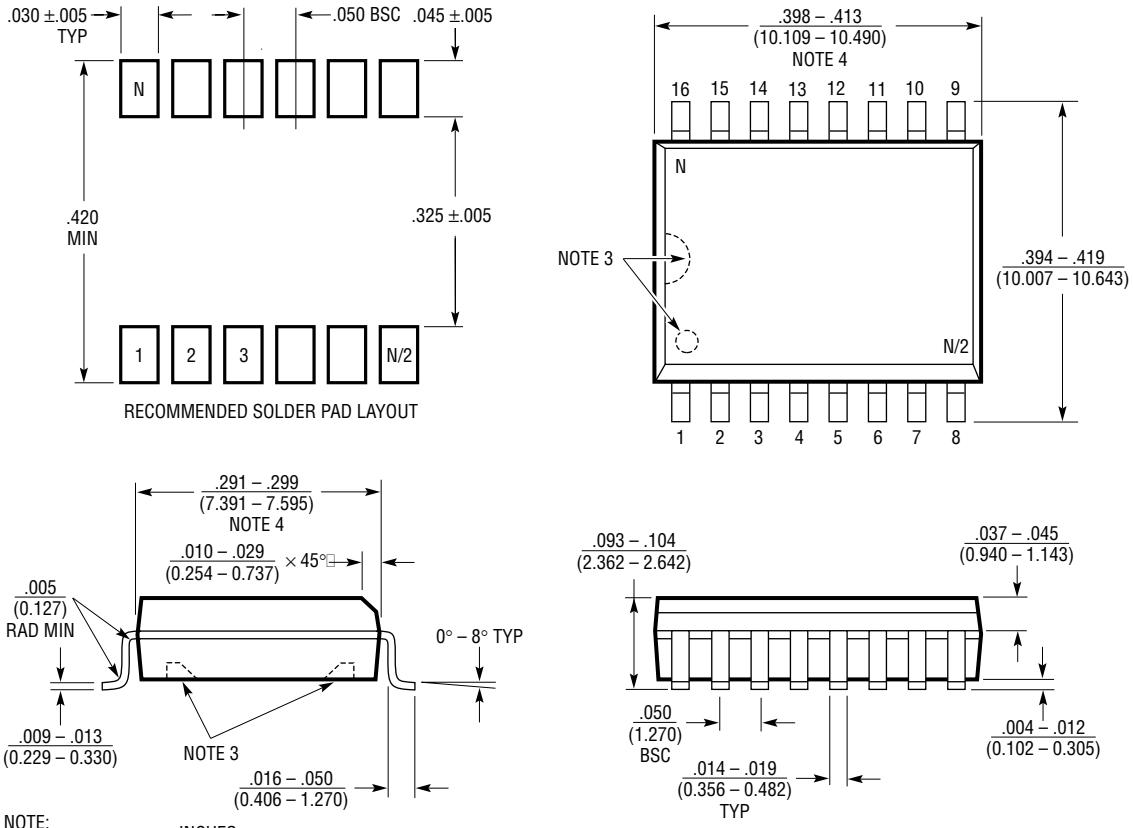
NOTE:
1. DIMENSIONS ARE $\frac{\text{INCHES}}{\text{MILLIMETERS}}$

*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.010 INCH (0.254MM)

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

TYPICAL APPLICATION

SW Package
16-Lead Plastic Small Outline (Wide .300 Inch)
(Reference LTC DWG # 05-08-1620)



NOTE:
1. DIMENSIONS IN $\frac{\text{INCHES}}{(\text{MILLIMETERS})}$
2. DRAWING NOT TO SCALE
3. PIN 1 IDENT, NOTCH ON TOP AND CAVITIES ON THE BOTTOM OF PACKAGES ARE THE MANUFACTURING OPTIONS. THE PART MAY BE SUPPLIED WITH OR WITHOUT ANY OF THE OPTIONS
4. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1569-6	Linear Phase, DC Accurate, 10th Order Lowpass Filter	Internal Resistor Set Clock, F_C < 64kHz
LTC1569-7	Linear Phase, DC Accurate, 10th Order Lowpass Filter	Internal Resistor Set Clock, F_C < 300kHz

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LT/LWI/LT 0905 REV A • PRINTED IN USA

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