Low Power, Low Noise, Quad Universal Filter Building Block

FEATURES

- Low Power
- 4 Filters in a 0.3" Wide Package
- 1/2 the Noise of the LTC1059, 60, 61 Devices
- Wide Output Swing
- Clock to Center Frequency Ratios of 50:1 and 100:1
- Operates from ±2.37V to ±8V Power Supplies
- Customized Version with Internal Resistors Available
- Ratio of 50:1 and 100:1 Simultaneously Available

APPLICATIONS

- Antialiasing Filters
- Telecom Filters
- Spectral Analysis
- Loop Filters
- For Fixed Lowpass Filter Requirements use the LTC1164-XX Series

DESCRIPTION

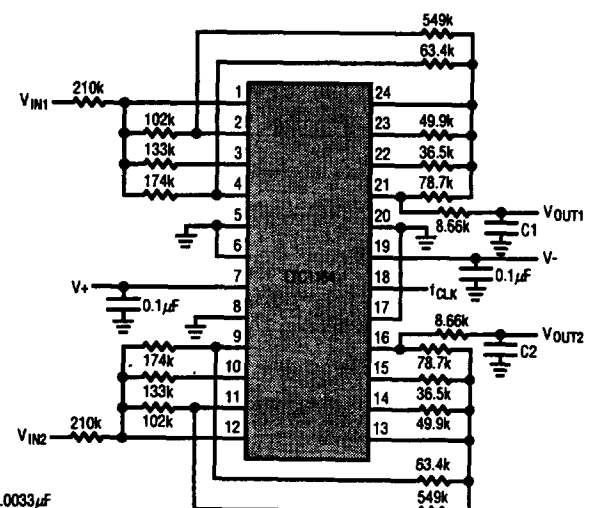
The LTC1164 consists of four low power, low noise 2nd order switched capacitor filter building blocks. Each building block typically consumes 850μA supply current. Low power is achieved without sacrificing noise and distortion. Each building block, together with 3 to 5 resistors, can provide 2nd order functions like lowpass, highpass, bandpass, and notch. The center frequency of each 2nd order section can be tuned with an external clock, or a clock and resistor ratio. For Q<5, the center frequency range is from 0.1Hz to 20kHz. Up to 8th order filters can be realized by cascading all four 2nd order sections. Any classical filter realization (such as Butterworth, Cauer, Bessel, and Chebyshev) can be formed.

A customized monolithic version of the LTC1164 including internal thin film resistors can be obtained. Consult LTC Marketing for details.

The LTC1164 is manufactured using Linear Technology's enhanced LTCMOS™ silicon gate process.

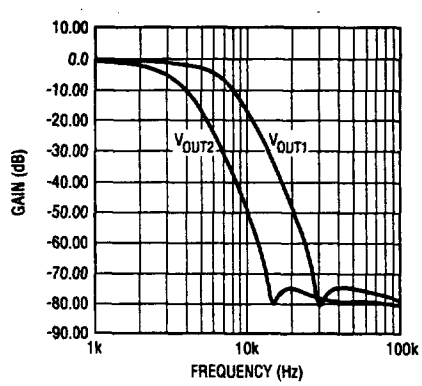
TYPICAL APPLICATION

Dual 5th Order Linear Phase Filter with Stopband Notch



C1 = 0.0033μF
C2 = 0.0068μF
f_{CLK} = 500kHz
WIDEBAND NOISE = 50μV_{RMS}
TOTAL SUPPLY CURRENT = 3mA
ALL RESISTORS ARE 1% METAL FILM

Dual 5th Order Linear Phase Filter with Stopband Notch, f_{CLK} = 500kHz



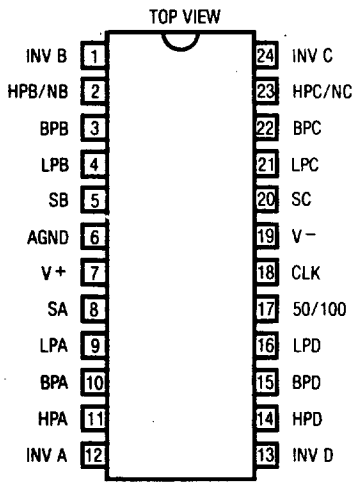
SUPPLY VOLTAGE	V_{IN}	TOTAL HARMONIC DISTORTION	SIGNAL/NOISE
±2.5V	1V_{RMS}	0.015% (–76dB)	86dB
±5.0V	2V_{RMS}	0.025% (–72dB)	92dB
±7.5V	4V_{RMS}	0.04% (–68dB)	98dB

8

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V^+ to V^-) 16.5V
Power Dissipation 500mW
Operating Temperature Range
LTC1164AM, LTC1164M ..... –55°C to 125°C
LTC1164AC, LTC1164C ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec.) ..... 300°C

PACKAGE/ORDER INFORMATION

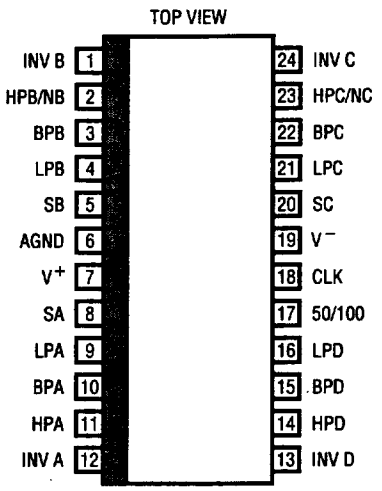


J PACKAGE
24-LEAD CERAMIC DIP

N PACKAGE
24-LEAD PLASTIC DIP

ORDER PART NUMBER

LTC1164AMJ
LTC1164MJ
LTC1164ACJ
LTC1164CJ
LTC1164ACN
LTC1164CN



SO PACKAGE
24-LEAD PLASTIC SOIC

ORDER PART NUMBER

LTC1164CS
LTC1164ACS

ELECTRICAL CHARACTERISTICS

(Internal Op Amps) $V_S = \pm 5V$, $T_A = 25°C$, $R_L = 5k\Omega$ unless otherwise specified.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage Range			±2.37		±8	V
Voltage Swings	$V_S = \pm 2.5V$			±1.6		V
	$V_S = \pm 5.0V$	●	±3.8	±4.2		V
	$V_S = \pm 7.5V$			±6.1		V
Output Short Circuit Current (Source/Sink)	$V_S = \pm 5.0V$			1		mA
DC Open Loop Gain	$V_S = \pm 5.0V$			80		dB
GBW Product	$V_S = \pm 5.0V$			2		MHz
Slew Rate	$V_S = \pm 5.0V$			1.6		V/μs

ELECTRICAL CHARACTERISTICS

(Complete Filter) $V_S = \pm 5V$, $T_A = 25°C$, TTL Clock Input Level, unless otherwise specified.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Center Frequency Range				0.1-20k		Hz
Input Frequency Range (Note 1)	50:1 100:1				$<f_{CLK}$ $<f_{CLK}/2$	Hz Hz
Clock to Center Frequency Ratio, f_{CLK}/f_o	Sides A, B, C: Mode 1, R1 = R3 = 50kΩ, R2 = 5kΩ, Side D: Mode 3, R1 = R3 = 50kΩ, R2 = R4 = 5kΩ f_o = 5kHz, Q = 10					
LTC1164A	50:1, f_{CLK} = 250kHz	●			50 ± 0.5	%
LTC1164	50:1, f_{CLK} = 250kHz	●			50 ± 0.9	%
LTC1164A	100:1, f_{CLK} = 500kHz	●			100 ± 0.5	%
LTC1164	100:1, f_{CLK} = 500kHz	●			100 ± 0.9	%
Clock to Center Frequency Ratio, Side to Side Matching	Sides A, B, C, Mode 1, f_o = 5kHz, Q = 10 Side D Mode 3, f_o = 5kHz, Q = 10					
LTC1164A	50:1, f_{CLK} = 250kHz	●			0.5	%
LTC1164	50:1, f_{CLK} = 250kHz	●			1.0	%
Q Accuracy	Sides A, B, C, Mode 1, f_o = 5kHz, Q = 10 50:1, f_{CLK} = 250kHz	●		±2	±5	%
	100:1, f_{CLK} = 500kHz	●		±2	±5	%
	Side D Mode 3, f_o = 5kHz, Q = 10 50:1, f_{CLK} = 250kHz	●		±3	±6	%
	100:1, f_{CLK} = 500kHz	●		±6	±12	%
f_o Temperature Coefficient	$f_{CLK} \leq 500kHz$			±1		ppm/°C
Q Temperature Coefficient	$f_{CLK} \leq 250kHz$			±5		ppm/°C
Maximum Clock Frequency	Mode 1, Q < 2.5 $V_S \geq \pm 7.0V$, 50:1 or 100:1			1.5		MHz
	Mode 3, Q < 5.0 $V_S \geq \pm 5.0V$, 50:1 or 100:1			1.0		MHz
	Mode 3, Q < 5.0 $V_S = \pm 2.5V$, 50:1 or 100:1			500		kHz
f_{CLK} Feedthrough	$f_{CLK} \leq 500kHz$, $V_S = \pm 5V$			200		μV_{RMS}
DC Offset Voltages (See Figure 1 and Table 1)	V_{OS1}	●		2	20	mV
	V_{OS2}	●		3	45	mV
	V_{OS3}	●		3	45	mV
Power Supply Current	$V_S = \pm 2.5V$			4.0		mA
	$V_S = \pm 5.0V$, Temp ≥ +25°C			3.6	5.0	mA
	$V_S = \pm 5.0V$	●		5.6	8	mA
	$V_S = \pm 7.5V$, Temp ≥ +25°C			6.0	8	mA
	$V_S = \pm 7.5V$	●		9.0	11.0	mA

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: Guaranteed by design. Not tested.

8

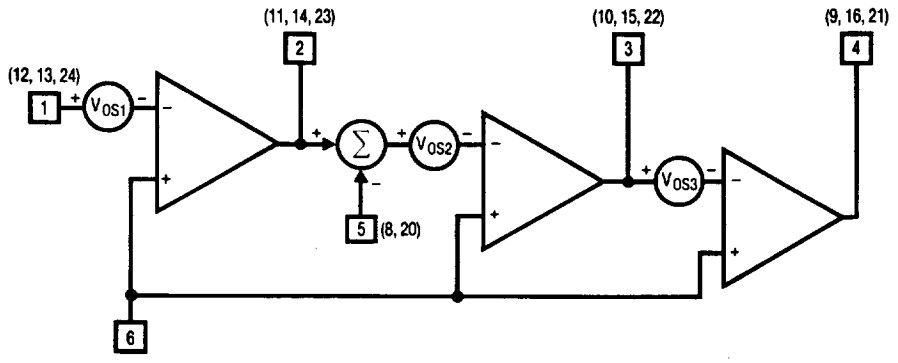
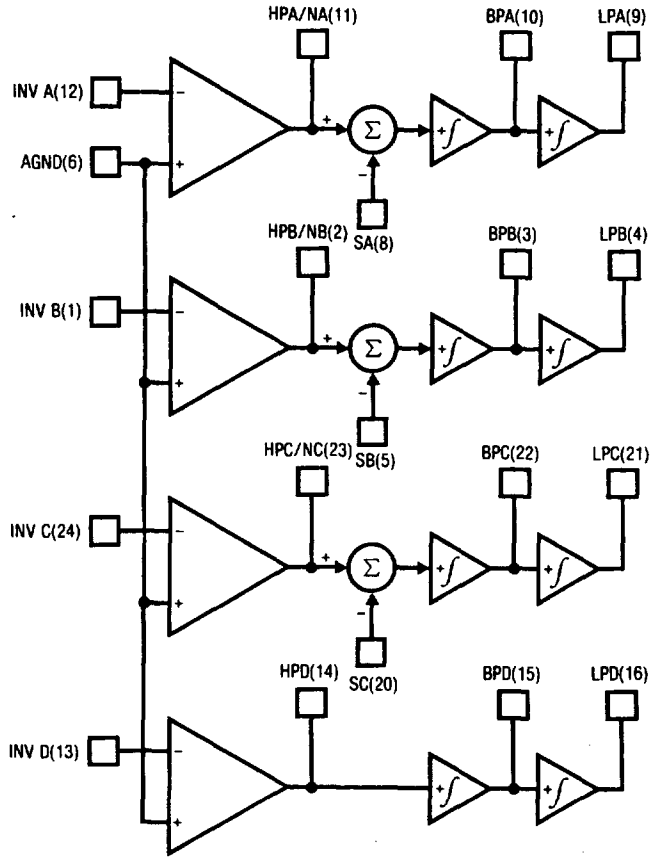


Figure 1. Equivalent Input Offsets of 1/4 LTC1164 Filter Building Block

Table 1. Output DC Offsets One 2nd Order Section

MODE	V_{OSN} PIN 2, 11, 14, 23	V_{OSBP} PIN 3, 10, 15, 22	V_{OSLP} PIN 4, 9, 16, 21
1	$V_{OS1}[(1/Q) + 1 + \|H_{OLP}\|] - V_{OS3}/Q$	V_{OS3}	$V_{OSN} - V_{OS2}$
1b	$V_{OS1}[(1/Q) + 1 + R2/R1] - V_{OS3}/Q$	V_{OS3}	$-(V_{OSN} - V_{OS2})(1 + R5/R6)$
2	$[V_{OS1}(1 + R2/R1 + R2/R3 + R2/R4) - V_{OS3}(R2/R3)] \times [R4/(R2 + R4)] + V_{OS2}[R2/(R2 + R4)]$	V_{OS3}	$V_{OSN} - V_{OS2}$
3	V_{OS2}	V_{OS3}	$V_{OS1}\left[1 + \frac{R4}{R1} + \frac{R4}{R2} + \frac{R4}{R3}\right] - V_{OS2}\left(\frac{R4}{R2}\right) - V_{OS3}\left(\frac{R4}{R3}\right)$

BLOCK DIAGRAM



BY TYING PIN 17 TO V^+ ALL SECTIONS OPERATE WITH (f_{CLK}/f_0) = (50:1)

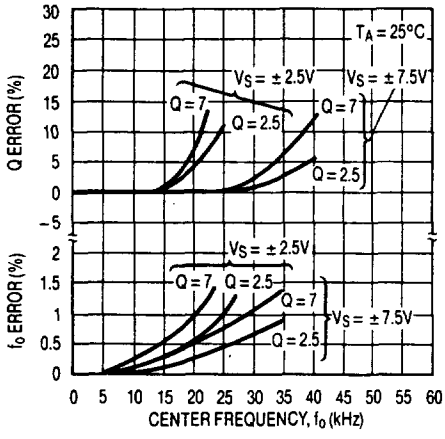
BY TYING PIN 17 TO V^- ALL SECTIONS OPERATE WITH (f_{CLK}/f_0) = (100:1)

BY TYING PIN 17 TO AGND SECTIONS A & D OPERATE WITH (f_{CLK}/f_0) = (100:1) AND SECTIONS B & C OPERATE AT (50:1)

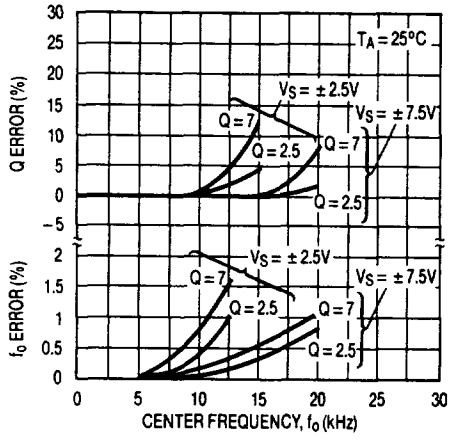
8

TYPICAL PERFORMANCE CHARACTERISTICS

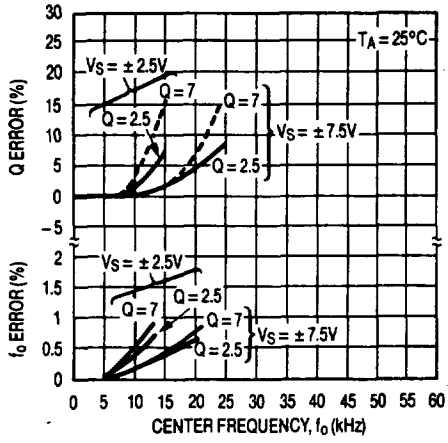
Graph 1. Mode 1, (f_{CLK}/f_o) = 50:1



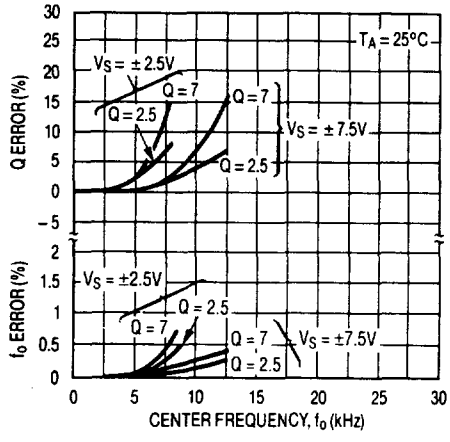
Graph 2. Mode 1, (f_{CLK}/f_o) = 100:1



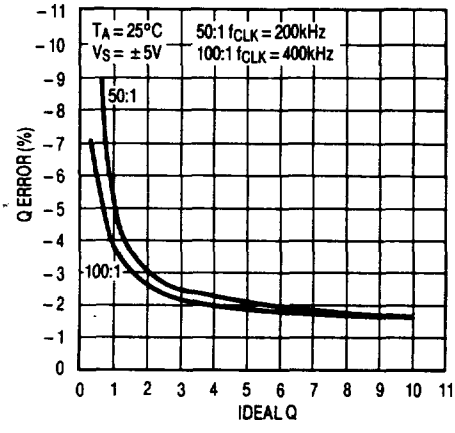
Graph 3. Mode 3, (f_{CLK}/f_o) = 50:1



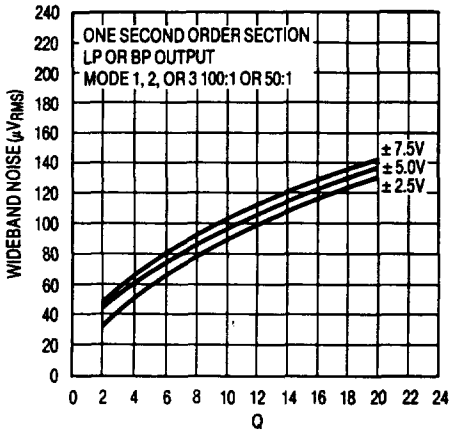
Graph 4. Mode 3, (f_{CLK}/f_o) = 100:1



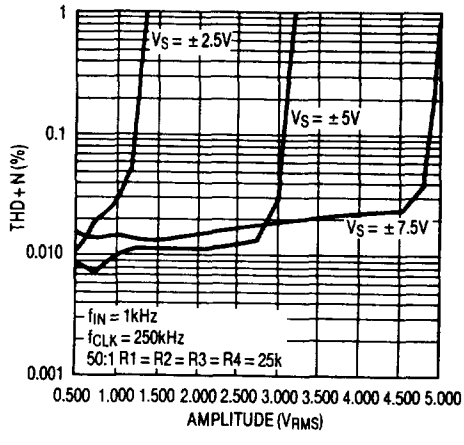
Graph 5. Mode 3 Q Error vs Ideal Q



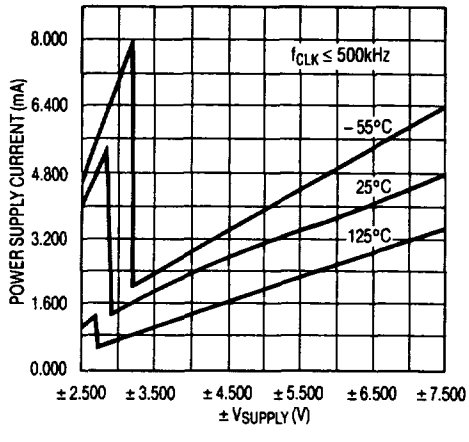
Graph 6. Wideband Noise vs Q



Graph 7. Total Harmonic Distortion vs Output Amplitude



Graph 8. Power Supply Current vs Voltage



PIN DESCRIPTION

Power Supplies (Pins 7, 19)

They should be bypassed with 0.1µF ceramic disc. Low noise, non-switching, power supplies are recommended. The device operates with a single 5V supply and with dual supplies. The absolute maximum operating power supply voltage is ±8.25V. Supply reversal is not allowed and can cause latch up. When using dual supplies, loads between the positive and negative supply (even light loads) can cause momentary supply reversal during power-up. A clamp diode from each supply to ground will prevent reversal and latch problems.

Clock (Pin 18)

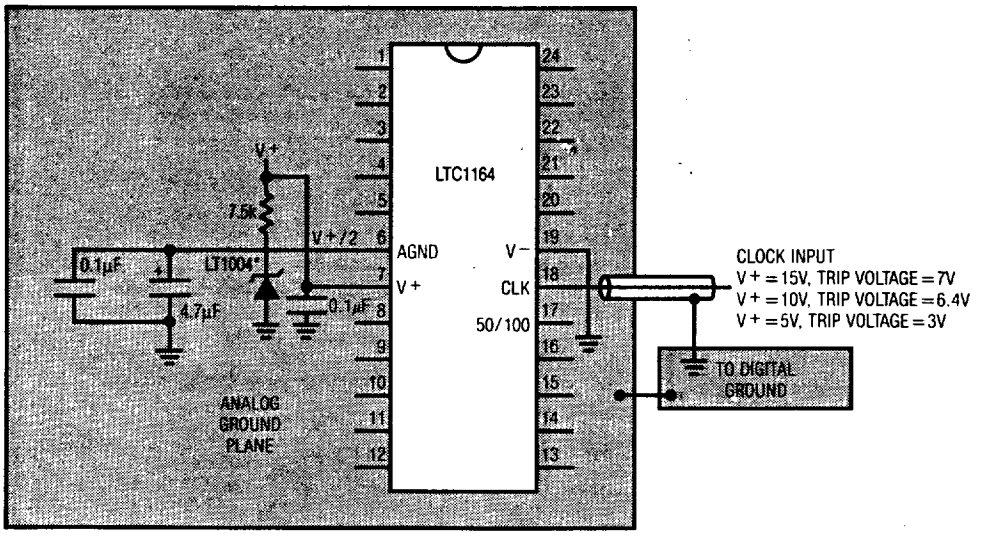
For ±5V supplies the logic threshold level is 1.8V. For ±8V and 0 to 5V supplies the logic threshold level is 2.8V. The logic threshold levels vary ±100mV over the full military temperature range. The recommended duty cycle of the input clock is 50%, although for clock frequencies below 500kHz the clock "on" time can be as low as 200ns. The maximum clock frequency for single 5V supply and Q values <5 is 500kHz and for ±5V supplies and above is 1MHz. The clock input can be applied before power is turned on as long as there is no chance the clock signal will go below the V^- supply.

AGND (Pin 6)

When the LTC1164 operates with dual supplies, Pin 6 should be tied to system ground. When the LTC1164 operates with a single positive supply, the analog ground pin should be tied to 1/2 supply and it should be bypassed with a 4.7µF solid tantalum in parallel with a 0.1µF ceramic disc, Figure 2. The positive input of all the internal op amps, as well as the common reference of all the internal switches, are internally tied to the analog ground pin. Because of this, a very "clean" ground is recommended.

50/100 (Pin 17)

By tying Pin 17 to V^+, all filter sections operate with a clock to center frequency ratio internally set at 50:1. When Pin 17 is at mid-supplies, sections B and C operate with $(f_{CLK}/f_0) = 50:1$ and sections A and D operate at (100:1). When Pin 17 is shorted to the negative supply pin, all filter sections operate with $(f_{CLK}/f_0) = 100:1$.



NOTE: PIN 5, 8, 20, IF NOT USED, SHOULD BE CONNECTED TO PIN 6.
*LT1004 CAN BE REPLACED WITH A 7.5k RESISTOR FOR $V^+ > 6.5V$.

Figure 2. Single Supply Operation

APPLICATIONS INFORMATION

ANALOG CONSIDERATIONS

1. Grounding and Bypassing

The LTC1164 should be used with separated analog and digital ground planes and single point grounding techniques.

Pin 6 (AGND) should be tied directly to the analog ground plane.

Pin 7 (V^+) should be bypassed to the ground plane with a 0.1μF ceramic disk with leads as short as possible. Pin 19 (V^-) should be bypassed with a 0.1μF ceramic disk. For single supply applications, V^- can be tied to the analog ground plane.

For good noise performance, V^+ and V^- must be free of noise and ripple.

All analog inputs should be referenced directly to the single point ground. The clock inputs should be shielded from and/or routed away from the analog circuitry and a separate digital ground plane used.

Figure 3 shows an example of an ideal ground plane design for a two sided board. Of course this much ground plane will not always be possible, but users should strive to get as close to this as possible. Proto boards are not recommended.

2. Buffering the Filter Output

When driving coaxial cables and 1× scope probes, the filter output should be buffered. This is important especially when high Qs are used to design a specific filter. *Inadequate buffering may cause errors in noise, distortion, Q, and gain measurements.* When 10× probes are used, buffering is usually not required. A buffer is recommended especially when THD tests are performed. As shown in Figure 4, the buffer should be adequately bypassed to minimize clock feedthrough.

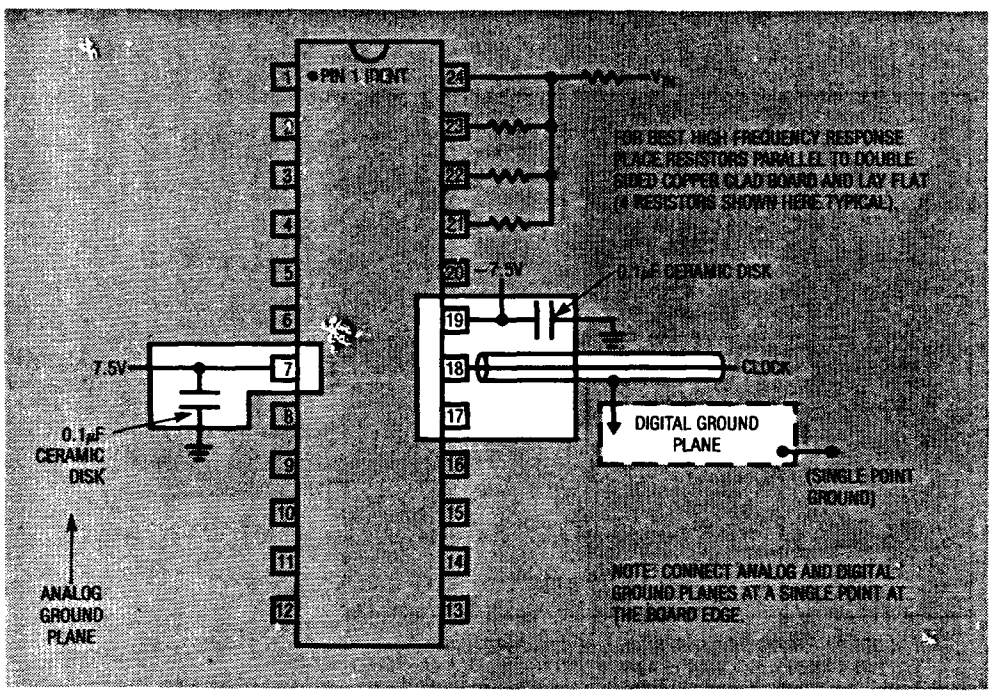


Figure 3. Example Ground Plane Breadboard Technique for LTC1164

APPLICATIONS INFORMATION

3. Offset Nulling

Lowpass filters may have too much DC offset for some users. A servo circuit may be used to actively null the offsets of the LTC1164 or any LTC switched capacitor filter. The circuit shown in Figure 5 will null offsets to better than 300μV. This circuit takes seconds to settle because of the integrator pole frequency.

4. Noise

All the noise performance mentioned excludes the clock feedthrough. Noise measurements will degrade if, the already described grounding, bypassing, and buffering techniques are not practiced. Graph 6 is a very good representation of the noise performance of this device.

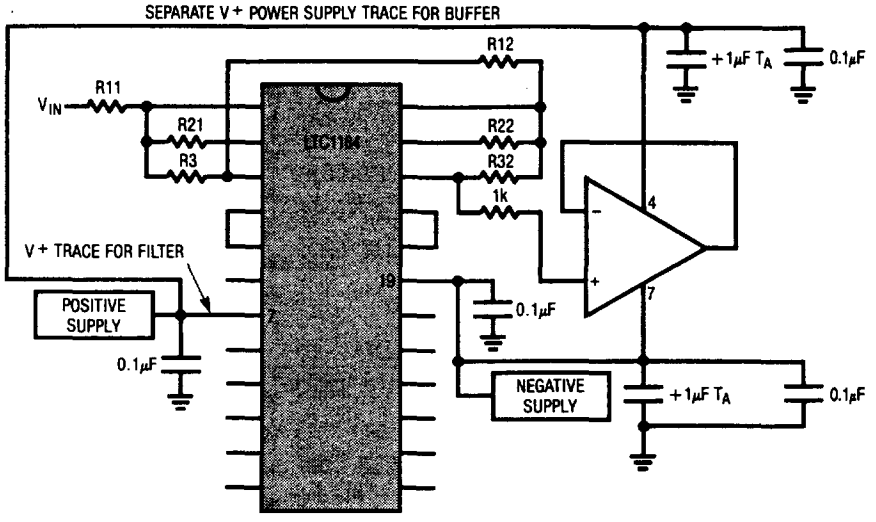


Figure 4. Buffering the Output of a 4th Order Bandpass Realization

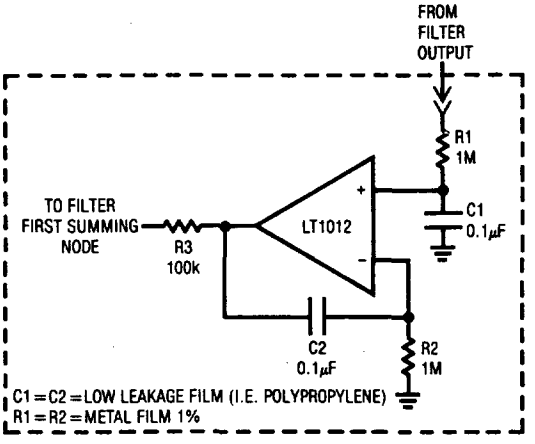


Figure 5. Servo Amplifier

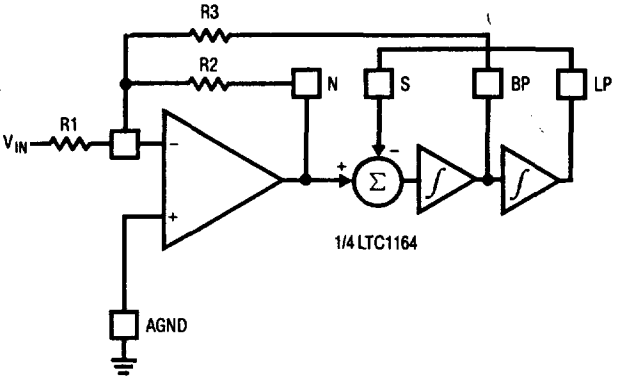
8

MODES OF OPERATION

PRIMARY MODES

Mode 1

In Mode 1, the ratio of the external clock frequency to the center frequency of each 2nd order section is internally fixed at 50:1 or 100:1. Figure 6 illustrates Mode 1 providing 2nd order notch, lowpass, and bandpass outputs. Mode 1 can be used to make high order Butterworth lowpass filters; it can also be used to make low Q notches and for cascading 2nd order bandpass functions tuned at the same center frequency with unity gain. Mode 1 is faster than Mode 3. Note that Mode 1 can only be implemented with 3 of the 4 LTC1164 sections because section D has no



$$f_o = \frac{f_{CLK}}{100(50)};\ f_n = f_o;\ H_{OLP} = -\frac{R2}{R1};\ H_{OBP} = -\frac{R3}{R1};\ H_{ON1} = -\frac{R2}{R1}\quad Q = \frac{R3}{R2}$$

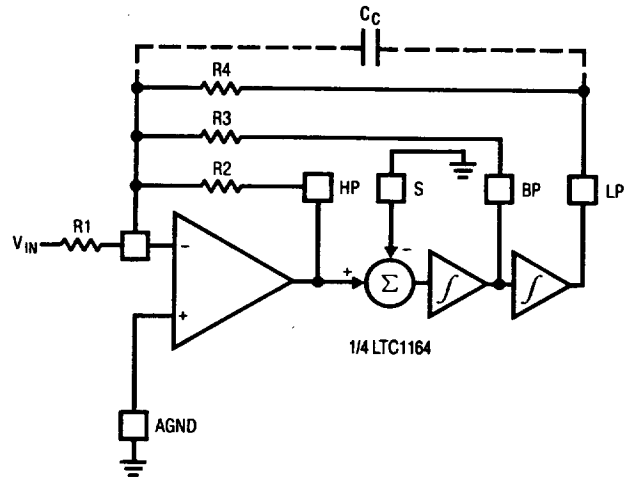
Figure 6. Mode 1: 2nd Order Filter Providing Notch, Bandpass, Lowpass

MODES OF OPERATION

externally available summing node. Section D, however, can be internally connected in Mode 1 upon special request.

Mode 3

Mode 3 is the second of the primary modes. In Mode 3, the ratio of the external clock frequency to the center frequency of each 2nd order section can be adjusted above or below 50:1 or 100:1. Side D of the LTC1164 can only be connected in Mode 3. Figure 7 illustrates Mode 3, the classical state variable configuration, providing highpass, bandpass, and lowpass 2nd order filter functions. Mode 3 is slower than Mode 1. Mode 3 can be used to make high order all-pole bandpass, lowpass, highpass and notch filters.



MODE 3 (100:1): $f_o = \frac{f_{CLK}}{100}\sqrt{\frac{R2}{R4}}$; $Q = \frac{R3}{R2}\sqrt{\frac{R2}{R4}}$; $H_{OHP} = -R2/R1$;

$H_{OBP} = -R3/R1$; $H_{OLP} = -R4/R1$

MODE 3 (50:1): $f_o = \frac{f_{CLK}}{50}\sqrt{\frac{R2}{R4}}$; $Q = \frac{1.005(\sqrt{R2/R4})}{(R2/R3)-(R2/16R4)}$;

$H_{OHP} = -R2/R1$; $H_{OBP} = -\frac{R3/R1}{1-(R3/16R4)}$; $H_{OLP} = -R4/R1$

NOTE: THE 50:1 EQUATIONS FOR MODE 3 ARE DIFFERENT FROM THE EQUATIONS FOR MODE 3 OPERATION OF THE LTC1059, LTC1060 AND LTC1061. START WITH f_o, CALCULATE R2/R4, SET R4; FROM THE Q VALUE, CALCULATE R3:

$$R3 = \frac{R2}{\frac{1.005}{Q}\sqrt{\frac{R2}{R4}} + \frac{R2}{16R4}}$$; THEN CALCULATE R1 TO SET THE DESIRED GAIN.

Figure 7. Mode 3: 2nd Order Filter Providing Highpass, Bandpass, Lowpass

When the internal clock to center frequency ratio is set at 50:1, the design equations for Q and bandpass gain are different from the 100:1 case. This was done to provide speed without penalizing the noise performance.

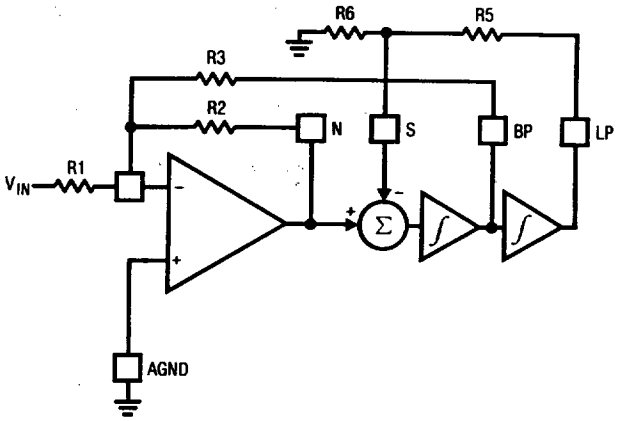
SECONDARY MODES

Mode 1b

Mode 1b is derived from Mode 1. In Mode 1b, Figure 8, two additional resistors R5 and R6, are added to alternate the amount of voltage fed back from the low pass output into the input of the SA (or SB or SC) switched capacitor summer. This allows the filter clock to center frequency ratio to be adjusted beyond 50:1 or 100:1. Mode 1b maintains the speed advantages of Mode 1.

Mode 2

Mode 2 is a combination of Mode 1 and Mode 3, as shown in Figure 9. With Mode 2, the clock to center frequency ratio, f_{CLK}/f_o, is always less than 50:1 or 100:1. The advantage of Mode 2 is that it provides less sensitivity to resistor tolerances than does Mode 3. As in Mode 1, Mode 2 has



$f_o = \frac{f_{CLK}}{100(50)}\sqrt{\frac{R6}{R5+R6}}$; $f_n = f_o$; $Q = \frac{R3}{R2}\sqrt{\frac{R6}{R5+R6}}$;

$H_{ON1}(f \to 0) = H_{ON2}\left(f \to \frac{f_{CLK}}{2}\right) = -\frac{R2}{R1}$; $H_{OLP} = \frac{-R2/R1}{R6/(R5+R6)}$;

$H_{OBP} = -\frac{R3}{R1}$; $(R5//R6) < 5k\Omega$

Figure 8. Mode 1b: 2nd Order Filter Providing Notch, Bandpass, Lowpass

MODES OF OPERATION

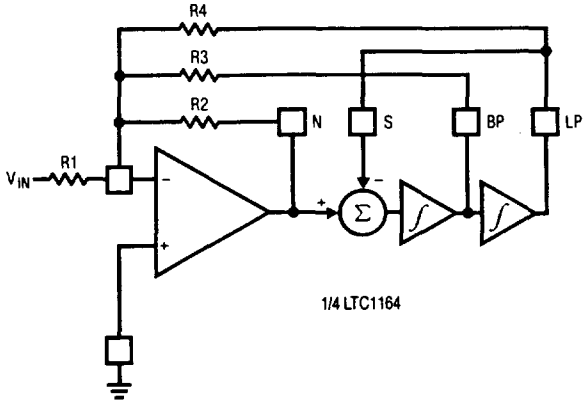
a notch output which depends on the clock frequency, and the notch frequency is therefore less than the center frequency, f_0.

When the internal clock to center frequency ratio is set at 50:1, the design equations for Q and bandpass gain are different from the 100:1 case.

Mode 3A

This is an extension of Mode 3 where the highpass and lowpass output are summed through two external resistors R_h and R_l to create a notch. This is shown in Figure 10. Mode 3A is more versatile than Mode 2 because the notch frequency can be higher or lower than the center frequency of the 2nd order section. The external op amp of Figure 10 is not always required. When cascading the sections of the LTC1164, the highpass and lowpass outputs can be summed directly into the inverting input of the next section. The topology of Mode 3A is useful for elliptic highpass and notch filters with clock to cutoff frequency ratios higher than 100:1. This is often required to extend the allowed input signal frequency range and to avoid premature aliasing.

PN *When the internal clock to center frequency ratio is set at 50:1, the design equations for Q and bandpass gain are different from the 100:1 case.*



MODE 2 (100:1): $f_o = \frac{f_{CLK}}{100}\sqrt{1+\frac{R2}{R4}}$; $f_n = \frac{f_{CLK}}{50}$; $Q = \frac{R3}{R2}\sqrt{1+\frac{R2}{R4}}$; $H_{OLP} = \frac{-R2/R1}{1+(R2/R4)}$

$H_{OBP} = -R3/R1$; $H_{ON1}(f\rightarrow 0) = \frac{-R2/R1}{1+(R2/R4)}$; $H_{ON2}\left(f\rightarrow\frac{f_{CLK}}{2}\right) = -R2/R1$

MODE 2 (50:1): $f_o = \frac{f_{CLK}}{50}\sqrt{1+\frac{R2}{R4}}$; $f_n = \frac{f_{CLK}}{50}$; $Q = \frac{1.005(\sqrt{1+R2/R4})}{(R2/R3)-(R2/16R4)}$; $H_{OLP} = \frac{-R2/R1}{1+(R2/R4)}$

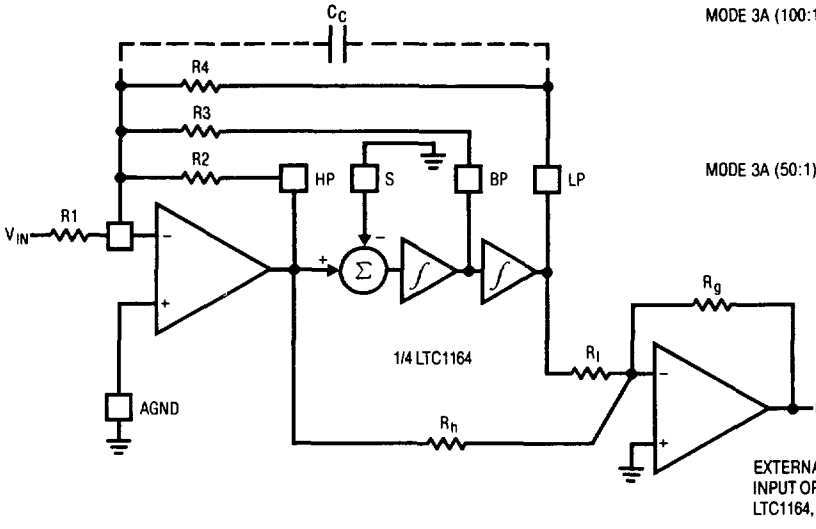
$H_{OBP} = -\frac{R3/R1}{1-(R3/16R4)}$; $H_{ON1}(f\rightarrow 0) = \frac{-R2/R1}{1+(R2/R4)}$

$H_{ON2}\left(f\rightarrow\frac{f_{CLK}}{2}\right) = -R2/R1$

NOTE: THE 50:1 EQUATIONS FOR MODE 2 ARE DIFFERENT FROM THE EQUATIONS FOR MODE 2 OPERATION OF THE LTC1059, LTC1060 AND LTC1061. START WITH f_o, CALCULATE R2/R4, SET R4; FROM THE Q VALUE, CALCULATE R3:

$$R3 = \frac{R2}{\frac{1.005}{Q}\sqrt{1+\frac{R2}{R4}}+\frac{R2}{16R4}}$$; THEN CALCULATE R1 TO SET THE DESIRED GAIN.

Figure 9. Mode 2: 2nd Order Filter Providing Notch, Bandpass, Lowpass



MODE 3A (100:1): $f_o = \frac{f_{CLK}}{100}\sqrt{\frac{R2}{R4}}$; $f_n = \frac{f_{CLK}}{100}\sqrt{\frac{R_h}{R_I}}$; $H_{OHP} = -R2/R1$; $H_{OBP} = -R3/R1$

$H_{OLP} = -R4/R1$; $H_{ON1}(f\rightarrow 0) = \frac{R_g}{R_I}\times\frac{R4}{R1}$; $H_{ON2}\left(f\rightarrow\frac{f_{CLK}}{2}\right) = \frac{R_g}{R_h}\times\frac{R2}{R1}$

$H_{ON}(f=f_o) = Q\left(\frac{R_g}{R_I}H_{OLP} - \frac{R_g}{R_h}H_{OHP}\right)$; $Q = \frac{R3}{R2}\sqrt{\frac{R2}{R4}}$

MODE 3A (50:1): $f_o = \frac{f_{CLK}}{50}\sqrt{\frac{R2}{R4}}$; $f_n = \frac{f_{CLK}}{50}\sqrt{\frac{R_h}{R_I}}$; $H_{OHP}\left(f\rightarrow\frac{f_{CLK}}{2}\right) = -R2/R1$

$H_{OBP} = -\frac{R3/R1}{1-(R3/16R4)}$; $H_{OLP}(f=0) = -R4/R1$; $Q = \frac{1.005(\sqrt{R2/R4})}{(R2/R3)-(R2/16R4)}$

NOTE: THE 50:1 EQUATIONS FOR MODE 3A ARE DIFFERENT FROM THE EQUATIONS FOR MODE 3A OPERATION OF THE LTC1059, LTC1060 AND LTC1061. START WITH f_o, CALCULATE R2/R4, SET R4; FROM THE Q VALUE, CALCULATE R3:

$$R3 = \frac{R2}{\frac{1.005}{Q}\sqrt{\frac{R2}{R4}}+\frac{R2}{16R4}}$$; THEN CALCULATE R1 TO SET THE DESIRED GAIN.

Figure 10. Mode 3A: 2nd Order Filter Providing Highpass, Bandpass, Lowpass, Notch

APPLICATION CIRCUITS

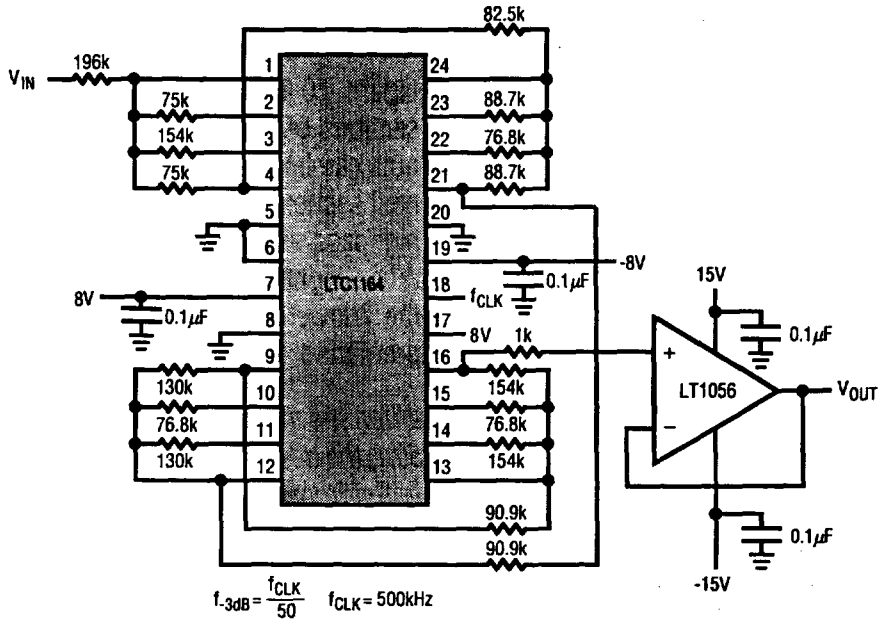
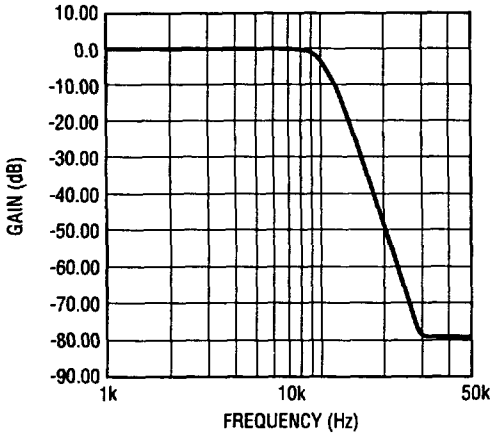
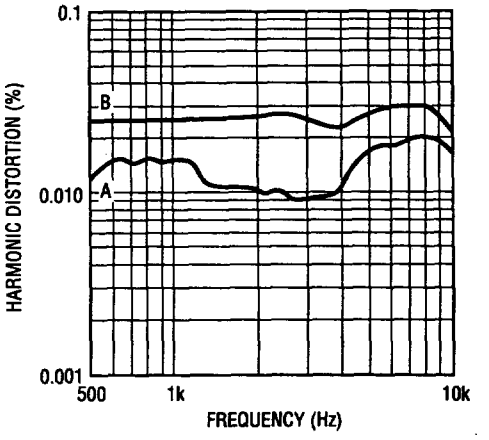


Figure 11. 8th Order Lowpass Butterworth, Passband Noise 90μV_{RMS} (Also Refer to the LTC1164-5)



Graph 9. LTC1164 8th Order Butterworth, f_{CLK} = 500kHz, f_{-3dB} = 10kHz



Graph 10. LTC1164 8th Order Butterworth, f_{CLK} = 500kHz, f_{-3dB} = 10kHz ±8V, A. 2V_{RMS}, B. 4V_{RMS}

APPLICATION CIRCUITS

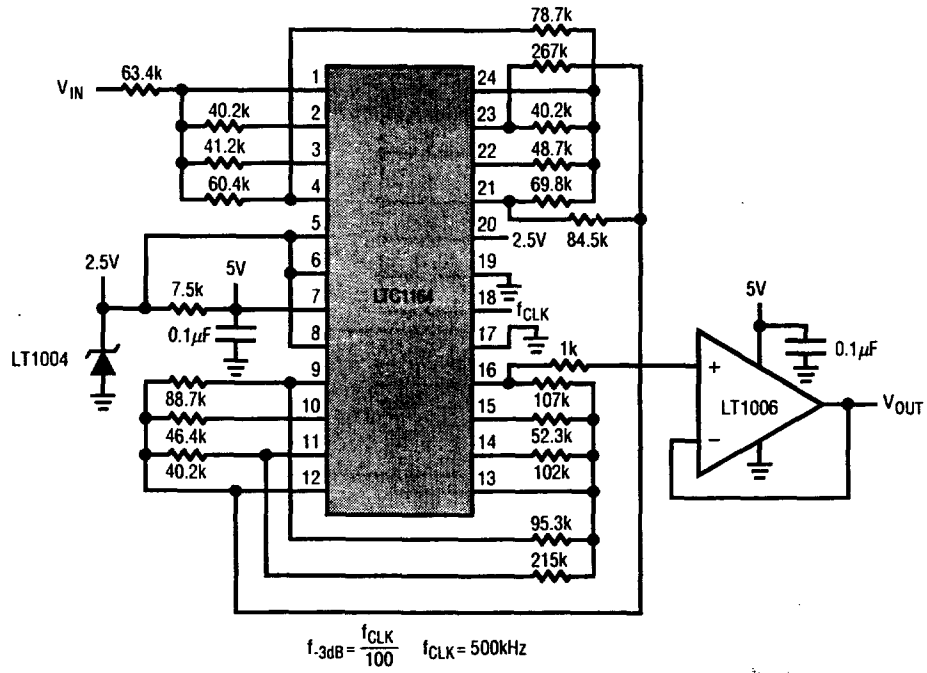
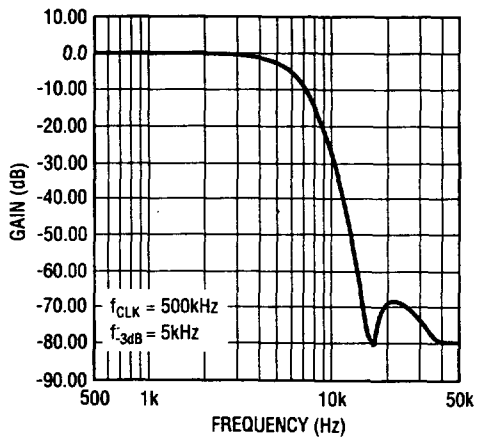
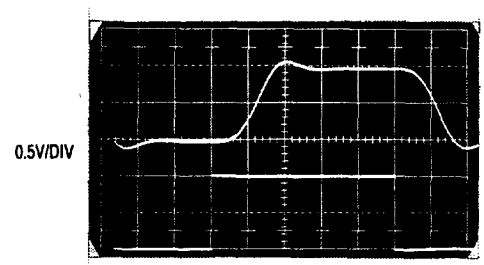


Figure 12. 8th Order Lowpass Single Supply Elliptic-Bessel Transitional Filter
Total Supply Current = 4mA, Passband Noise 50μV_{RMS}



Graph 11. LTC1164 8th Order Lowpass, Elliptic-Bessel Transitional Filter Single 5V Supply



8

APPLICATION CIRCUITS

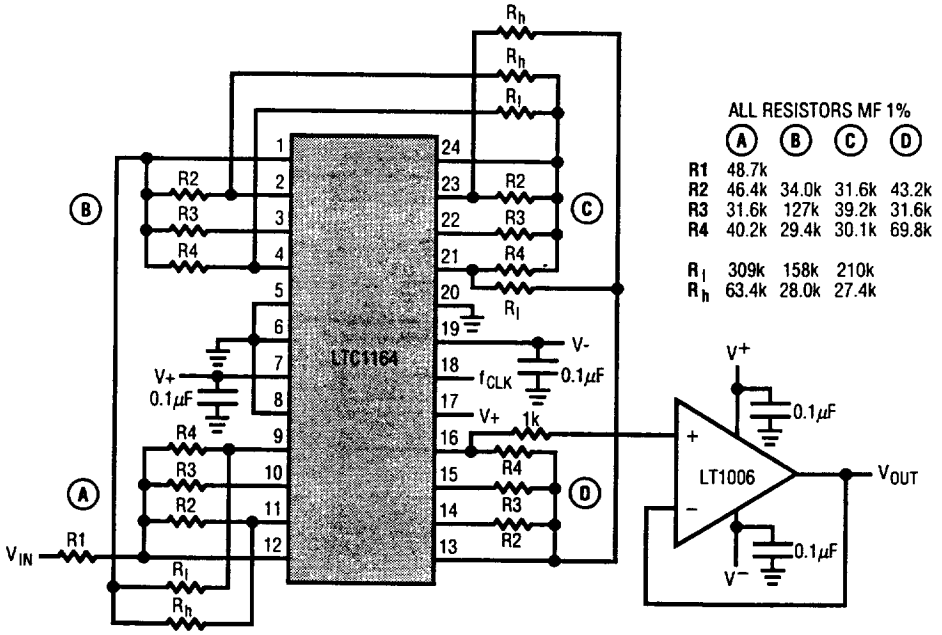


Figure 13. LTC1164 8th Order Lowpass Elliptic, f_{CUTOFF} = 5kHz, f_{CLK} = 250kHz, –78dB at 10kHz, Passband Noise = 110μV_{RMS} ±5V (Also Refer to the LTC1164-6)

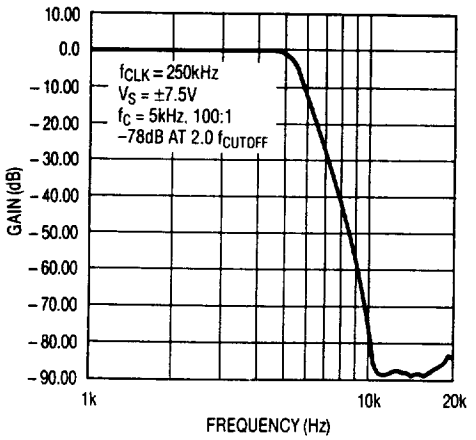


Figure 14. LTC1164 8th Order Lowpass Elliptic, f_{CUTOFF} = 5kHz

APPLICATION CIRCUITS

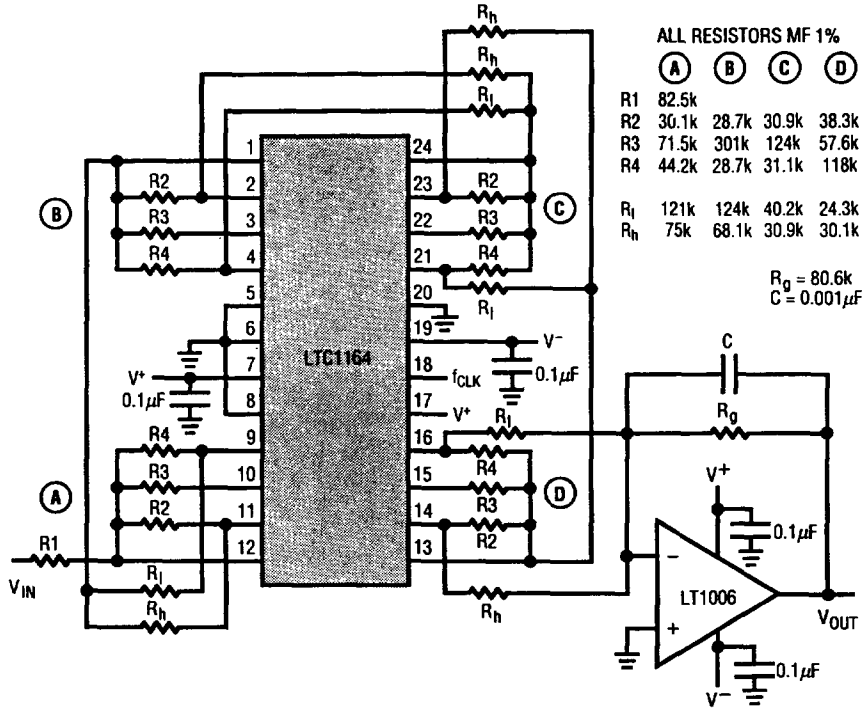


Figure 15. LTC1164 9th Order Lowpass Elliptic, Fixed $f_{CUTOFF} = 4kHz$, $f_{CLK} = 400kHz$, −74dB at 5kHz, Passband Noise = $210\mu V_{RMS} \pm 5V$

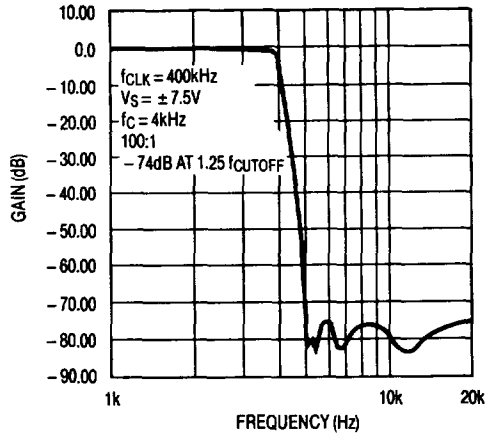


Figure 16. LTC1164 9th Order Lowpass Elliptic, $f_{CUTOFF} = 4kHz$

8