Micropower Sampling 8-Bit Serial I/O A/D Converters

FEATURES

- **80µA Maximum Supply Current**
- **1nA Typical Supply Current in Shutdown**
- **5V Operation (LTC1096/LTC1098)**
- **3V Operation (LTC1096L/LTC1098L)(2.65V Min)**
- Sample-and-Hold
- 16µs Conversion Time
- 33kHz Sample Rate
- ±0.5LSB Total Unadjusted Error Over Temp
- Direct 3-Wire Interface to Most MPU Serial Ports and All MPU Parallel I/O Ports
- 8-Pin SO Plastic Package

APPLICATIONS

- Battery-Operated Systems
- Remote Data Acquisition
- Battery Monitoring
- Battery Gas Gauges
- Temperature Measurement
- Isolated Data Acquisition

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DESCRIPTION

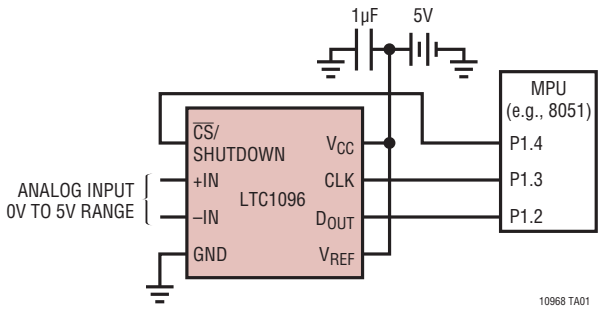
The LTC®1096/LTC1096L/LTC1098/LTC1098L are micropower, 8-bit A/D converters that draw only 80µA of supply current when converting. They automatically power down to 1nA typical supply current whenever they are not performing conversions. They are packaged in 8-pin SO packages and have both 3V (L) and 5V versions. These 8-bit, switched-capacitor, successive approximation ADCs include sample-and-hold. The LTC1096/LTC1096L have a single differential analog input. The LTC1098/LTC1098L offer a software selectable 2-channel MUX.

On-chip serial ports allow efficient data transfer to a wide range of microprocessors and microcontrollers over three wires. This, coupled with micropower consumption, makes remote location possible and facilitates transmitting data through isolation barriers.

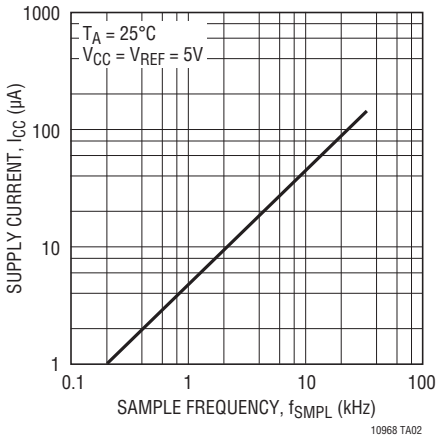
These circuits can be used in ratiometric applications or with an external reference. The high impedance analog inputs and the ability to operate with reduced spans (below 1V full scale) allow direct connection to sensors and transducers in many applications, eliminating the need for gain stages.

TYPICAL APPLICATION

10µW, S8 Package, 8-Bit A/D Samples at 200Hz and Runs Off a 5V Battery



Supply Current vs Sample Rate



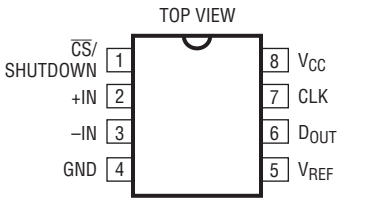
ABSOLUTE MAXIMUM RATINGS

(Notes 1 and 2)

Supply Voltage (V_{CC}) to GND 12V
Voltage
  Analog and Reference ..... –0.3V to V_{CC} + 0.3V
  Digital Inputs ..... –0.3V to 12V
  Digital Outputs ..... –0.3V to V_{CC} + 0.3V
Power Dissipation 500mW
Storage Temperature Range ..... –65°C to 150°C
Operating Temperature
  LTC1096AC/LTC1096C/LTC1096LC/
  LTC1098AC/LTC1098C/LTC1098LC ..... 0°C to 70°C
  LTC1096AI/LTC1096I/LTC1096LI/
  LTC1098AI/LTC1098I/LTC1098LI ..... –40°C to 85°C
Lead Temperature (Soldering, 10 sec.) ..... 300°C

PIN CONFIGURATION (Note 3)

LTC1096

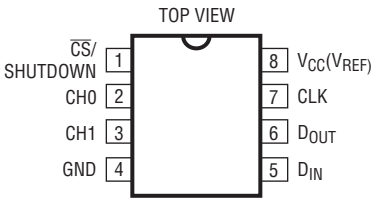


N8 PACKAGE
8-LEAD PLASTIC DIP

S8 PACKAGE
8-LEAD PLASTIC SOIC

T_{JMAX} = 150°C, θ_{JA} = 130°C/W (N8)
T_{JMAX} = 150°C, θ_{JA} = 175°C/W (S8)

LTC1098



N8 PACKAGE
8-LEAD PLASTIC DIP

S8 PACKAGE
8-LEAD PLASTIC SOIC

T_{JMAX} = 150°C, θ_{JA} = 130°C/W (N8)
T_{JMAX} = 150°C, θ_{JA} = 175°C/W (S8)

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC1096ACN8#PBF	LTC1096ACN8#TRPBF	LTC1096ACN8	8-Lead Plastic DIP	0°C to 70°C
LTC1096ACS8#PBF	LTC1096ACS8#TRPBF	1096A	8-Lead Plastic SOIC	0°C to 70°C
LTC1096AIN8#PBF	LTC1096AIN8#TRPBF	LTC1096AIN8	8-Lead Plastic DIP	–40°C to 85°C
LTC1096AIS8#PBF	LTC1096AIS8#TRPBF	1096AI	8-Lead Plastic SOIC	–40°C to 85°C
LTC1096CN8#PBF	LTC1096CN8#TRPBF	LTC1096CN8	8-Lead Plastic DIP	0°C to 70°C
LTC1096CS8#PBF	LTC1096CS8#TRPBF	1096	8-Lead Plastic SOIC	0°C to 70°C
LTC1096IN8#PBF	LTC1096IN8#TRPBF	LTC1096IN8	8-Lead Plastic DIP	–40°C to 85°C
LTC1096IS8#PBF	LTC1096IS8#TRPBF	1096I	8-Lead Plastic SOIC	–40°C to 85°C
LTC1096LCS8#PBF	LTC1096LCS8#TRPBF	1096L	8-Lead Plastic SOIC	0°C to 70°C
LTC1096LIS8#PBF	LTC1096LIS8#TRPBF	1096LI	8-Lead Plastic SOIC	–40°C to 85°C
LTC1098ACN8#PBF	LTC1098ACN8#TRPBF	LTC1098ACN8	8-Lead Plastic DIP	0°C to 70°C
LTC1098ACS8#PBF	LTC1098ACS8#TRPBF	1098A	8-Lead Plastic SOIC	0°C to 70°C
LTC1098CN8#PBF	LTC1098CN8#TRPBF	LTC1098CN8	8-Lead Plastic DIP	0°C to 70°C
LTC1098CS8#PBF	LTC1098CS8#TRPBF	1098	8-Lead Plastic SOIC	0°C to 70°C
LTC1098IN8#PBF	LTC1098IN8#TRPBF	LTC1098IN8	8-Lead Plastic DIP	–40°C to 85°C
LTC1098IS8#PBF	LTC1098IS8#TRPBF	1098I	8-Lead Plastic SOIC	–40°C to 85°C
LTC1098LCS8#PBF	LTC1098LCS8#TRPBF	1098L	8-Lead Plastic SOIC	0°C to 70°C
LTC1098LIS8#PBF	LTC1098LIS8#TRPBF	1098LI	8-Lead Plastic SOIC	–40°C to 85°C

ORDER INFORMATION

LEAD BASED FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC1096ACN8	LTC1096ACN8#TR	LTC1096ACN8	8-Lead Plastic DIP	0°C to 70°C
LTC1096ACS8	LTC1096ACS8#TR	1096A	8-Lead Plastic SOIC	0°C to 70°C
LTC1096AIN8	LTC1096AIN8#TR	LTC1096AIN8	8-Lead Plastic DIP	–40°C to 85°C
LTC1096AIS8	LTC1096AIS8#TR	1096AI	8-Lead Plastic SOIC	–40°C to 85°C
LTC1096CN8	LTC1096CN8#TR	LTC1096CN8	8-Lead Plastic DIP	0°C to 70°C
LTC1096CS8	LTC1096CS8#TR	1096	8-Lead Plastic SOIC	0°C to 70°C
LTC1096IN8	LTC1096IN8#TR	LTC1096IN8	8-Lead Plastic DIP	–40°C to 85°C
LTC1096IS8	LTC1096IS8#TR	1096I	8-Lead Plastic SOIC	–40°C to 85°C
LTC1096LCS8	LTC1096LCS8#TR	1096L	8-Lead Plastic SOIC	0°C to 70°C
LTC1096LIS8	LTC1096LIS8#TR	1096LI	8-Lead Plastic SOIC	–40°C to 85°C
LTC1098ACN8	LTC1098ACN8#TR	LTC1098ACN8	8-Lead Plastic DIP	0°C to 70°C
LTC1098ACS8	LTC1098ACS8#TR	1098A	8-Lead Plastic SOIC	0°C to 70°C
LTC1098CN8	LTC1098CN8#TR	LTC1098CN8	8-Lead Plastic DIP	0°C to 70°C
LTC1098CS8	LTC1098CS8#TR	1098	8-Lead Plastic SOIC	0°C to 70°C
LTC1098IN8	LTC1098IN8#TR	LTC1098IN8	8-Lead Plastic DIP	–40°C to 85°C
LTC1098IS8	LTC1098IS8#TR	1098I	8-Lead Plastic SOIC	–40°C to 85°C
LTC1098LCS8	LTC1098LCS8#TR	1098L	8-Lead Plastic SOIC	0°C to 70°C
LTC1098LIS8	LTC1098LIS8#TR	1098LI	8-Lead Plastic SOIC	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
This product is only offered in trays. For more information go to: http://www.linear.com/packaging/

RECOMMENDED OPERATING CONDITIONS

LTC1096/LTC1098

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC}	Supply Voltage	LTC1096 LTC1098	3.0 3.0		9 6	V V
V_{CC} = 5V Operation						
f_{CLK}	Clock Frequency	V_{CC} = 5V	25		500	kHz
t_{CYC}	Total Cycle Time	LTC1096, f_{CLK} = 500kHz LTC1098, f_{CLK} = 500kHz	29 29			µs µs
t_{hDI}	Hold Time, D_{IN} After CLK↑	V_{CC} = 5V	150			ns
$t_{su\overline{CS}}$	Setup Time $\overline{CS}$↓ Before First CLK↑ (See Operating Sequence)	V_{CC} = 5V, LTC1096 V_{CC} = 5V, LTC1098	500 500			ns ns
t_{WAKEUP}	Wake-Up Time $\overline{CS}$↓ Before First CLK↓ After First CLK↑ (See Figure 1 LTC1096 Operating Sequence)	V_{CC} = 5V, LTC1096	10			µs
	Wake-Up Time $\overline{CS}$↓ Before MSBF Bit CLK↓ (See Figure 2 LTC1098 Operating Sequence)	V_{CC} = 5V, LTC1098	10			µs
t_{suDI}	Setup Time, D_{IN} Stable Before CLK↑	V_{CC} = 5V	400			ns
t_{WHCLK}	CLK High Time	V_{CC} = 5V	0.8			µs
t_{WLCLK}	CLK Low Time	V_{CC} = 5V	0.8			µs

RECOMMENDED OPERATING CONDITIONS

LTC1096/LTC1098

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$t_{WH\overline{CS}}$	$\overline{CS}$ High Time Between Data Transfer Cycles	V_{CC} = 5V	1			µs
$t_{WL\overline{CS}}$	$\overline{CS}$ Low Time During Data Transfer	LTC1096, f_{CLK} = 500kHz LTC1098, f_{CLK} = 500kHz	28 28			µs µs
V_{CC} = 3V Operation						
f_{CLK}	Clock Frequency	V_{CC} = 3V	25		250	kHz
t_{CYC}	Total Cycle Time	LTC1096, f_{CLK} = 250kHz LTC1098, f_{CLK} = 250kHz	58 58			µs µs
t_{hDI}	Hold Time, D_{IN} After CLK↑	V_{CC} = 3V	450			ns
$t_{su\overline{CS}}$	Setup Time $\overline{CS}$↓ Before First CLK↑ (See Operating Sequence)	V_{CC} = 3V, LTC1096 V_{CC} = 3V, LTC1098	1 1			µs µs
t_{WAKEUP}	Wake-Up Time $\overline{CS}$↓ Before First CLK↓ After First CLK↑ (See Figure 1 LTC1096 Operating Sequence)	V_{CC} = 3V, LTC1096	10			µs
	Wake-Up Time $\overline{CS}$↓ Before MSBF Bit CLK↓ (See Figure 2 LTC1098 Operating Sequence)	V_{CC} = 3V, LTC1098	10			µs
t_{suDI}	Setup Time, D_{IN} Stable Before CLK↑	V_{CC} = 3V	1			µs
t_{WHCLK}	CLK High Time	V_{CC} = 3V	1.6			µs
t_{WLCLK}	CLK Low Time	V_{CC} = 3V	1.6			µs
$t_{WH\overline{CS}}$	$\overline{CS}$ High Time Between Data Transfer Cycles	V_{CC} = 3V	2			µs
$t_{WL\overline{CS}}$	$\overline{CS}$ Low Time During Data Transfer	LTC1096, f_{CLK} = 250kHz LTC1098, f_{CLK} = 250kHz	56 56			µs µs

LTC1096L/LTC1098L

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC}	Supply Voltage		2.65		4.0	V
f_{CLK}	Clock Frequency	V_{CC} = 2.65V	25		250	kHz
t_{CYC}	Total Cycle Time	LTC1096L, f_{CLK} = 250kHz LTC1098L, f_{CLK} = 250kHz	58 58			µs µs
t_{hDI}	Hold Time, D_{IN} After CLK↑	V_{CC} = 2.65V	450			ns
$t_{su\overline{CS}}$	Setup Time $\overline{CS}$↓ Before First CLK↑ (See Operating Sequence)	V_{CC} = 2.65V, LTC1096L V_{CC} = 2.65V, LTC1098L	1 1			µs µs
t_{WAKEUP}	Wake-Up Time $\overline{CS}$↓ Before First CLK↓ After First CLK↑ (See Figure 1 LTC1096L Operating Sequence)	V_{CC} = 2.65V, LTC1096L	10			µs
	Wake-Up Time $\overline{CS}$↓ Before MSBF Bit CLK↓ (See Figure 2 LTC1098L Operating Sequence)	V_{CC} = 2.65V, LTC1098L	10			µs
t_{suDI}	Setup Time, D_{IN} Stable Before CLK↑	V_{CC} = 2.65V	1			µs
t_{WHCLK}	CLK High Time	V_{CC} = 2.65V	1.6			µs
t_{WLCLK}	CLK Low Time	V_{CC} = 2.65V	1.6			µs
$t_{WH\overline{CS}}$	$\overline{CS}$ High Time Between Data Transfer Cycles	V_{CC} = 2.65V	2			µs
$t_{WL\overline{CS}}$	$\overline{CS}$ Low Time During Data Transfer	LTC1096L, f_{CLK} = 250kHz LTC1098L, f_{CLK} = 250kHz	56 56			µs µs

CONVERTER AND MULTIPLEXER CHARACTERISTICS

LTC1096/LTC1098

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 5V, V_{REF} = 5V, f_{CLK} = 500kHz, unless otherwise noted.

PARAMETER	CONDITIONS		LTC1096A/LTC1098A			LTC1096/LTC1098			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Resolution (No Missing Code)		●	8			8			Bits
Offset Error		●			±0.5			±0.5	LSB
Linearity Error	(Note 4)	●			±0.5			±0.5	LSB
Full Scale Error		●			±0.5			±1.0	LSB
Total Unadjusted Error (Note 5)	V_{REF} = 5.000V	●			±0.5			±1.0	LSB
Analog Input Range	(Notes 6, 7)			–0.05V to V_{CC} + 0.05V					V
REF Input Range (Notes 6, 7)	4.5 ≤ V_{CC} ≤ 6V 6V < V_{CC} ≤ 9V, LTC1096			–0.05V to V_{CC} + 0.05V –0.05V to 6V					V V
Analog Input Leakage Current	(Note 8)	●			±1.0			±1.0	µA

LTC1096/LTC1098

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 3V, V_{REF} = 2.5V, f_{CLK} = 250kHz, unless otherwise noted.

PARAMETER	CONDITIONS		LTC1096A/LTC1098A			LTC1096/LTC1098			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Resolution (No Missing Code)		●	8			8			Bits
Offset Error		●			±0.75			±1.0	LSB
Linearity Error	(Notes 4, 9)	●			±0.5			±1.0	LSB
Full-Scale Error		●			±1.0			±1.0	LSB
Total Unadjusted Error (Notes 5, 9)	V_{REF} = 2.500V	●			±1.0			±1.5	LSB
Analog Input Range	(Notes 6, 7)			–0.05V to V_{CC} + 0.05V					V
REF Input Range (Notes 6, 7, 9)	3V ≤ V_{CC} ≤ 6V			–0.05V to V_{CC} + 0.05V					V
Analog Input Leakage Current	(Notes 8, 9)	●			±1.0			±1.0	µA

LTC1096L/LTC1098L

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 2.65V, V_{REF} = 2.5V, f_{CLK} = 250kHz, unless otherwise noted.

PARAMETER	CONDITIONS		LTC1096A/LTC1098A			UNITS
			MIN	TYP	MAX	
Resolution (No Missing Code)		●	8			Bits
Offset Error		●			±1.0	LSB
Linearity Error	(Note 4)	●			±1.0	LSB
Full-Scale Error		●			±1.0	LSB
Total Unadjusted Error (Note 5)	V_{REF} = 2.5V	●			±1.5	LSB
Analog Input Range	(Notes 6, 7)			–0.05V to V_{CC} + 0.05V		V
REF Input Range (Note 6)	2.65V ≤ V_{CC} ≤ 4.0V			–0.05V to V_{CC} + 0.05V		V
Analog Input Leakage Current	(Note 8)	●			±1.0	µA

DIGITAL AND DC ELECTRICAL CHARACTERISTICS

LTC1096/LTC1098

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 5V, V_{REF} = 5V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage	V_{CC} = 5.25V	●	2.0			V
V_{IL}	Low Level Input Voltage	V_{CC} = 4.75V	●			0.8	V
I_{IH}	High Level Input Current	$V_{IN} = V_{CC}$	●			2.5	µA
I_{IL}	Low Level Input Current	V_{IN} = 0V	●			–2.5	µA
V_{OH}	High Level Output Voltage	V_{CC} = 4.75V, I_O = 10µA V_{CC} = 4.75V, I_O = 360µA	● ●	4.5 2.4	4.74 4.72		V V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.75V, I_O = 1.6mA	●			0.4	V
I_{OZ}	Hi-Z Output Leakage	$\overline{CS} \geq V_{IH}$	●			±3.0	µA
I_{SOURCE}	Output Source Current	V_{OUT} = 0V			–25		mA
I_{SINK}	Output Sink Current	$V_{OUT} = V_{CC}$			45		mA
I_{REF}	Reference Current	$\overline{CS} = V_{CC}$ $t_{CYC} \geq 200µs$, $f_{CLK} \leq 50kHz$ t_{CYC} = 29µs, f_{CLK} = 500kHz	● ● ●		0.001 3.500 35.000	2.5 7.5 50.0	µA µA µA
I_{CC}	Supply Current	$\overline{CS} = V_{CC}$	●		0.001	3.0	µA
		LTC1096, $t_{CYC} \geq 200µs$, $f_{CLK} \leq 50kHz$ LTC1096, t_{CYC} = 29µs, f_{CLK} = 500kHz	● ●		40 120	80 180	µA µA
		LTC1098, $t_{CYC} \geq 200µs$, $f_{CLK} \leq 50kHz$ LTC1098, t_{CYC} = 29µs, f_{CLK} = 500kHz	● ●		44 155	88 230	µA µA

LTC1096/LTC1098

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 3V, V_{REF} = 2.5V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage	V_{CC} = 3.6V	●	1.9			V
V_{IL}	Low Level Input Voltage	V_{CC} = 3V	●			0.45	V
I_{IH}	High Level Input Current (Note 9)	$V_{IN} = V_{CC}$	●			2.5	µA
I_{IL}	Low Level Input Current (Note 9)	V_{IN} = 0V	●			–2.5	µA
V_{OH}	High Level Output Voltage	V_{CC} = 3V, I_O = 10µA V_{CC} = 3V, I_O = 360µA	● ●	2.3 2.1	2.69 2.64		V V
V_{OL}	Low Level Output Voltage	V_{CC} = 3V, I_O = 400µA	●			0.3	V
I_{OZ}	Hi-Z Output Leakage (Note 9)	$\overline{CS} \geq V_{IH}$	●			±3.0	µA
I_{SOURCE}	Output Source Current (Note 9)	V_{OUT} = 0V			–10		mA
I_{SINK}	Output Sink Current (Note 9)	$V_{OUT} = V_{CC}$			15		mA
I_{REF}	Reference Current (Note 9)	$\overline{CS} = V_{CC}$ $t_{CYC} \geq 200µs$, $f_{CLK} \leq 50kHz$ t_{CYC} = 58µs, f_{CLK} = 250kHz	● ● ●		0.001 3.500 35.000	2.5 7.5 50.0	µA µA µA
I_{CC}	Supply Current (Note 9)	$\overline{CS} = V_{CC}$	●		0.001	3.0	µA
		LTC1096, $t_{CYC} \geq 200µs$, $f_{CLK} \leq 50kHz$ LTC1096, t_{CYC} = 58µs, f_{CLK} = 250kHz	● ●		40 120	80 180	µA µA
		LTC1098, $t_{CYC} \geq 200µs$, $f_{CLK} \leq 50kHz$ LTC1098, t_{CYC} = 58µs, f_{CLK} = 250kHz	● ●		44 155	88 230	µA µA

DIGITAL AND DC ELECTRICAL CHARACTERISTICS

LTC1096L/LTC1098L

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 2.65V, V_{REF} = 2.5V, f_{CLK} = 250kHz, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage	V_{CC} = 3.6V	●	1.9			V
V_{IL}	Low Level Input Voltage	V_{CC} = 2.65V	●			0.45	V
I_{IH}	High Level Input Current	V_{IN} = V_{CC}	●			2.5	µA
I_{IL}	Low Level Input Current	V_{IN} = 0V	●			–2.5	µA
V_{OH}	High Level Output Voltage	V_{CC} = 2.65V, I_O = 10µA V_{CC} = 2.65V, I_O = 360µA	● ●	2.3 2.1	2.64 2.50		V V
V_{OL}	Low Level Output Voltage	V_{CC} = 2.65V, I_O = 400µA	●			0.3	V
I_{OZ}	Hi-Z Output Leakage	$\overline{CS}$ ≥ High	●			±3.0	µA
I_{SOURCE}	Output Source Current	V_{OUT} = 0V			–10		mA
I_{SINK}	Output Sink Current	V_{OUT} = V_{CC}			15		mA
I_{REF}	Reference Current	$\overline{CS}$ = V_{CC} t_{CYC} ≥ 200µs, f_{CLK} ≤ 50kHz t_{CYC} = 58µs, f_{CLK} = 250kHz	● ● ●		0.001 3.500 35.000	2.5 7.5 50.0	µA µA µA
I_{CC}	Supply Current	$\overline{CS}$ = V_{CC}	●		0.001	3.0	µA
		LTC1096L, t_{CYC} ≥ 200µs, f_{CLK} ≤ 50kHz LTC1096L, t_{CYC} = 58µs, f_{CLK} = 250kHz	● ●		40 120	80 180	µA µA
		LTC1098L, t_{CYC} ≥ 200µs, f_{CLK} ≤ 50kHz LTC1098L, t_{CYC} = 58µs, f_{CLK} = 250kHz	● ●		44 155	88 230	µA µA

AC CHARACTERISTICS

LTC1096/LTC1098

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 5V, V_{REF} = 5V, f_{CLK} = 500kHz, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{SMPL}	Analog Input Sample Time	See Operating Sequence			1.5		CLK Cycles
$f_{SMPL(MAX)}$	Maximum Sampling Frequency		●	33			kHz
t_{CONV}	Conversion Time	See Operating Sequence			8		CLK Cycles
t_{dDO}	Delay Time, CLK↓ to D_{OUT} Data Valid	See Test Circuits	●		200	450	ns
t_{dis}	Delay Time, $\overline{CS}$↑ to D_{OUT} Hi-Z	See Test Circuits	●		170	450	ns
t_{en}	Delay Time, CLK↓ to D_{OUT} Enable	See Test Circuits	●		60	250	ns
t_{hDO}	Time Output Data Remains Valid After CLK↓	C_{LOAD} = 100pF			180		ns
t_f	D_{OUT} Fall Time	See Test Circuits	●		70	250	ns
t_r	D_{OUT} Rise Time	See Test Circuits	●		25	100	ns
C_{IN}	Input Capacitance	Analog Inputs On Channel Analog Inputs Off Channel			25 5		pF pF
		Digital Input			5		pF

AC CHARACTERISTICS

LTC1096/LTC1098

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 3V, V_{REF} = 2.5V, f_{CLK} = 250kHz, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{SMPL}	Analog Input Sample Time	See Operating Sequence			1.5		CLK Cycles
$f_{SMPL(MAX)}$	Maximum Sampling Frequency		●	16.5			kHz
t_{CONV}	Conversion Time	See Operating Sequence			8		CLK Cycles
t_{dDO}	Delay Time, CLK↓ to D_{OUT} Data Valid	See Test Circuits (Note 9)	●		500	1000	ns
t_{dis}	Delay Time, $\overline{CS}$↑ to D_{OUT} Hi-Z	See Test Circuits (Note 9)	●		220	800	ns
t_{en}	Delay Time, CLK↓ to D_{OUT} Enable	See Test Circuits (Note 9)	●		160	480	ns
t_{hDO}	Time Output Data Remains Valid After CLK↓	C_{LOAD} = 100pF			400		ns
t_f	D_{OUT} Fall Time	See Test Circuits (Note 9)	●		70	250	ns
t_r	D_{OUT} Rise Time	See Test Circuits (Note 9)	●		50	150	ns
C_{IN}	Input Capacitance	Analog Inputs On Channel Analog Inputs Off Channel			25 5		pF pF
		Digital Input			5		pF

LTC1096L/LTC1098L

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 2.65V, V_{REF} = 2.5V, f_{CLK} = 250kHz, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{SMPL}	Analog Input Sample Time	See Operating Sequence			1.5		CLK Cycles
$f_{SMPL(MAX)}$	Maximum Sampling Frequency		●	16.5			kHz
t_{CONV}	Conversion Time	See Operating Sequence			8		CLK Cycles
t_{dDO}	Delay Time, CLK↓ to D_{OUT} Data Valid	See Test Circuits	●		500	1000	ns
t_{dis}	Delay Time, $\overline{CS}$↑ to D_{OUT} Hi-Z	See Test Circuits	●		220	800	ns
t_{en}	Delay Time, CLK↓ to D_{OUT} Enable	See Test Circuits	●		160	480	ns
t_{hDO}	Time Output Data Remains Valid After CLK↓	C_{LOAD} = 100pF			400		ns
t_f	D_{OUT} Fall Time	See Test Circuits	●		70	250	ns
t_r	D_{OUT} Rise Time	See Test Circuits	●		50	200	ns
C_{IN}	Input Capacitance	Analog Inputs On Channel Analog Inputs Off Channel			25 5		pF pF
		Digital Input			5		pF

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All voltage values are with respect to GND.

Note 3: For the 8-lead PDIP, consult the factory.

Note 4: Linearity error is specified between the actual and points of the A/D transfer curve.

Note 5: Total unadjusted error includes offset, full scale, linearity, multiplexer and hold step errors.

Note 6: Two on-chip diodes are tied to each reference and analog input which will conduct for reference or analog input voltages one diode drop below GND or one diode drop above V_{CC}. This spec allows 50mV forward bias of either diode. This means that as long as the reference or analog input does not exceed the supply voltage by more than 50mV, the output code will be correct. To achieve an absolute 0V to 5V input voltage range will therefore require a minimum supply voltage of 4.950V over initial tolerance, temperature variations and loading. For 5.5V < V_{CC} ≤ 9V, reference and analog input range cannot exceed 5.55V. If reference and analog input range are greater than 5.55V, the output code will not be guaranteed to be correct.

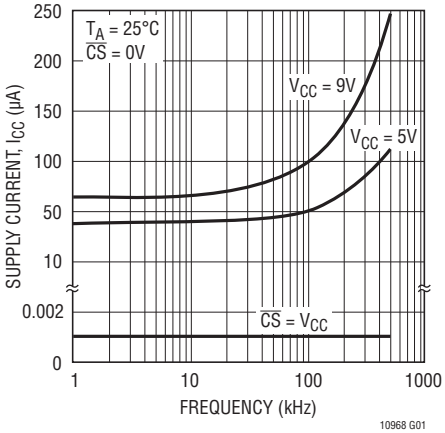
Note 7: The supply voltage range for the LTC1096L/LTC1098L is from 2.65V to 4V. The supply voltage range for the LTC1096 is from 3V to 9V, but the supply voltage range for the LTC1098 is only from 3V to 6V.

Note 8: Channel leakage current is measured after the channel selection.

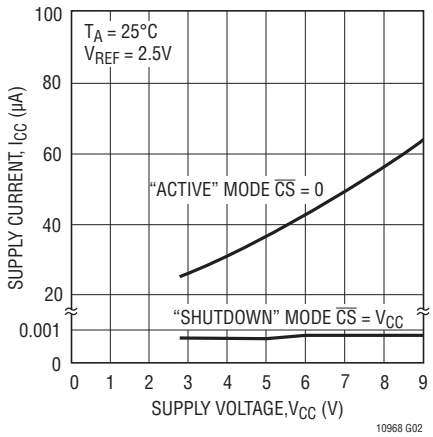
Note 9: These specifications are either correlated from 5V specifications or guaranteed by design.

TYPICAL PERFORMANCE CHARACTERISTICS

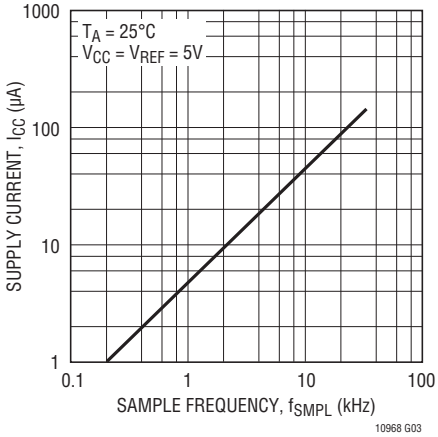
Supply Current vs Clock Rate for Active and Shutdown Modes



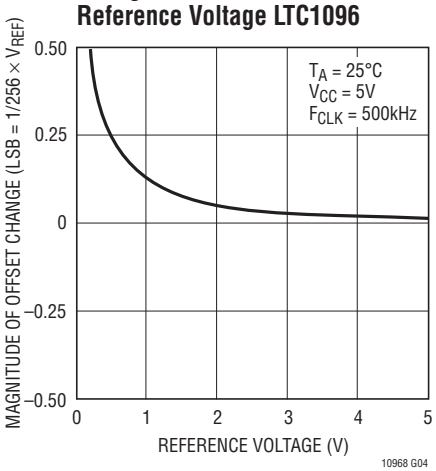
Supply Current vs Supply Voltage Active and Shutdown Modes



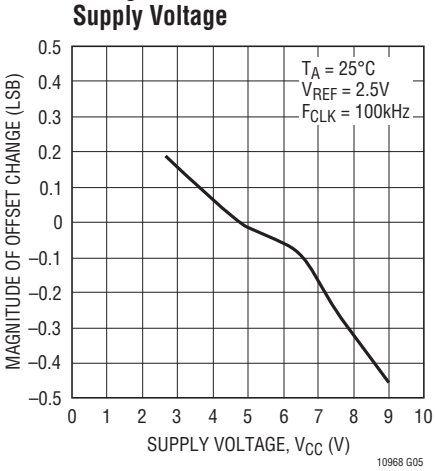
Supply Current vs Sample Frequency LTC1096



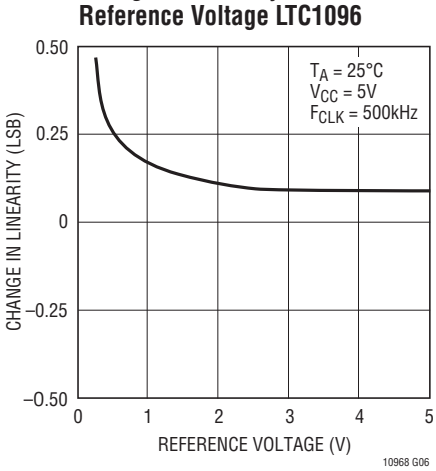
Change in Offset vs Reference Voltage LTC1096



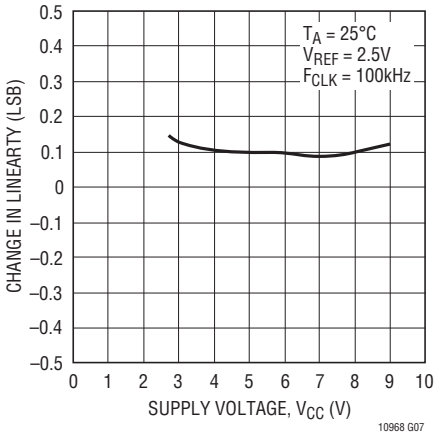
Change in Offset vs Supply Voltage



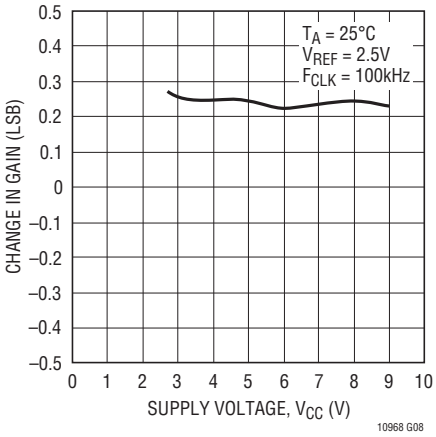
Change in Linearity vs Reference Voltage LTC1096



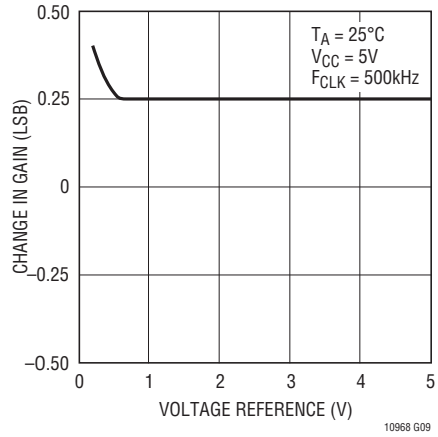
Change in Linearity vs Supply Voltage



Change in Gain vs Supply Voltage

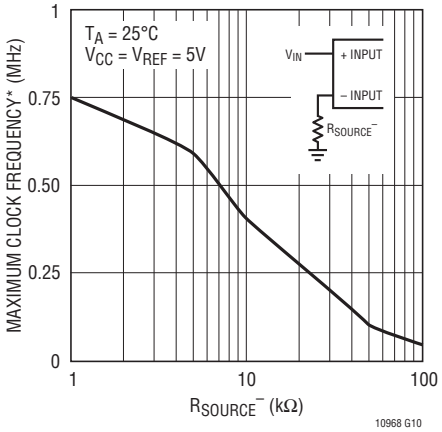


Change in Gain vs Reference Voltage LTC1096

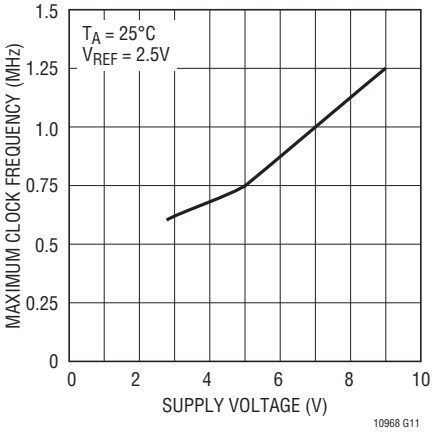


TYPICAL PERFORMANCE CHARACTERISTICS

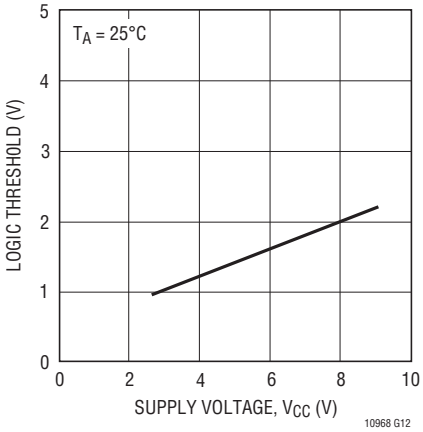
Maximum Clock Frequency vs Source Resistance



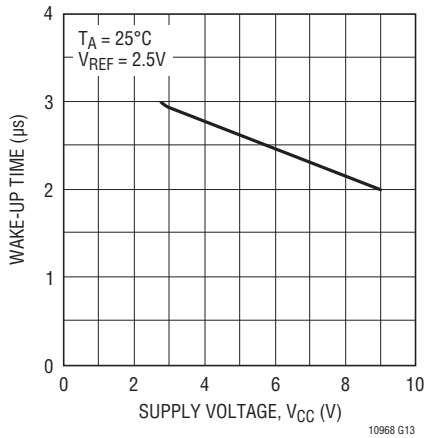
Maximum Clock Frequency vs Supply Voltage



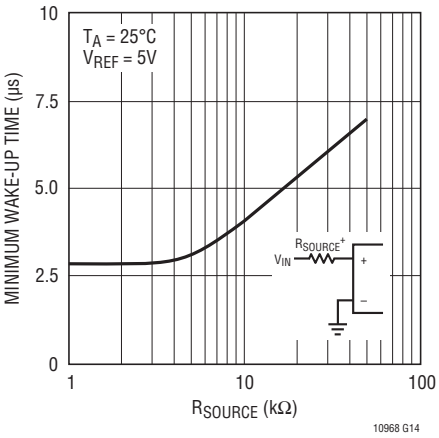
Digital Input Logic Threshold vs Supply Voltage



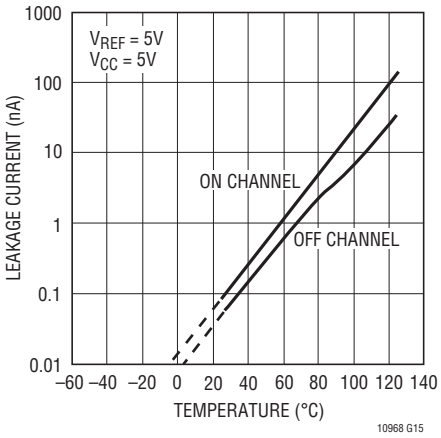
Wake-Up Time vs Supply Voltage



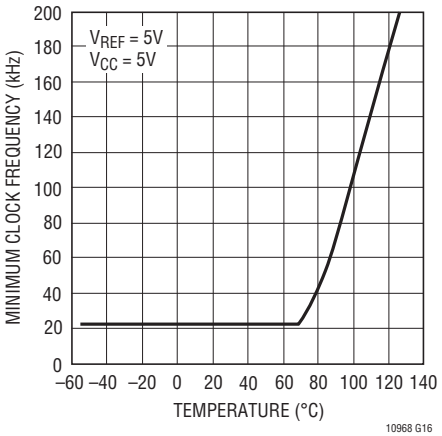
Minimum Wake-Up Time vs Source Resistance



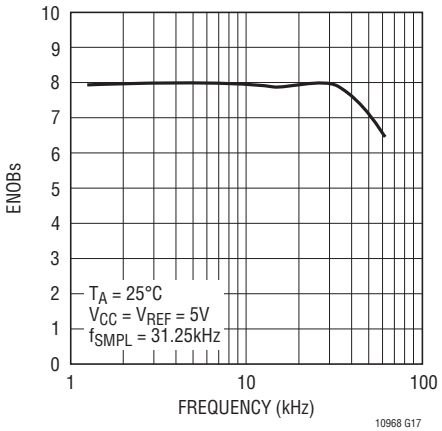
Input Channel Leakage Current vs Temperature



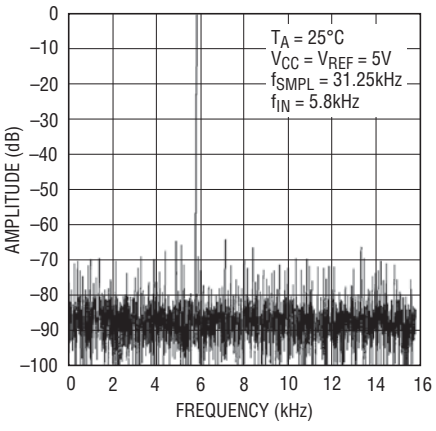
Minimum Clock Frequency for 0.1LSB Error† vs Temperature



ENOBs vs Frequency



FFT Plot



*Maximum CLK frequency represents the clock frequency at which a 0.1LSB shift in the error at any code transition from its 0.75MHz value is first detected.

†As the CLK frequency is decreased from 500kHz, minimum CLK frequency (Δerror ≤ 0.1LSB) represents the frequency at which a 0.1LSB shift in any code transition from its 500kHz value is first detected.

PIN FUNCTIONS

LTC1096/LTC1096L

$\overline{CS}$/SHDN (Pin 1): Chip Select Input. A logic low on this input enables the LTC1096/LTC1096L. A logic high on this input disables the LTC1096/LTC1096L and disconnects the power to the LTC1096/LTC1096L.

IN^+ (Pin 2): Analog Input. This input must be free of noise with respect to GND.

IN^- (Pin 3): Analog Input. This input must be free of noise with respect to GND.

GND (Pin 4): Analog Ground. GND should be tied directly to an analog ground plane.

V_{REF} (Pin 5): Reference Input. The reference input defines the span of the A/D converter and must be kept free of noise with respect to GND.

D_{OUT} (Pin 6): Digital Data Output. The A/D conversion result is shifted out of this output.

CLK (Pin 7): Shift Clock. This clock synchronizes the serial data transfer.

V_{CC} (Pin 8): Power Supply Voltage. This pin provides power to the A/D converter. It must be free of noise and ripple by bypassing directly to the analog ground plane.

LTC1098/LTC1098L

$\overline{CS}$/SHDN (Pin 1): Chip Select Input. A logic low on this input enables the LTC1098/LTC1098L. A logic high on this input disables the LTC1098/LTC1098L and disconnects the power to the LTC1098/LTC1098L.

CH0 (Pin 2): Analog Input. This input must be free of noise with respect to GND.

CH1 (Pin 3): Analog Input. This input must be free of noise with respect to GND.

GND (Pin 4): Analog Ground. GND should be tied directly to an analog ground plane.

D_{IN} (Pin 5): Digital Data Input. The multiplexer address is shifted into this pin.

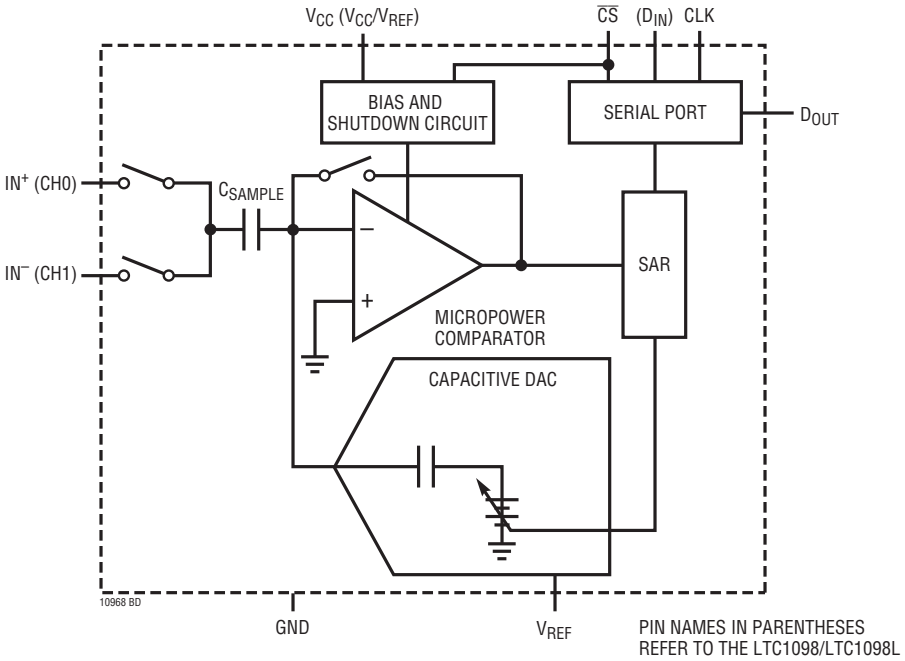
D_{OUT} (Pin 6): Digital Data Output. The A/D conversion result is shifted out of this output.

CLK (Pin 7): Shift Clock. This clock synchronizes the serial data transfer.

V_{CC} (V_{REF}) (Pin 8): Power Supply Voltage. This pin provides power and defines the span of the A/D converter. It must be free of noise and ripple by bypassing directly to the analog ground plane.

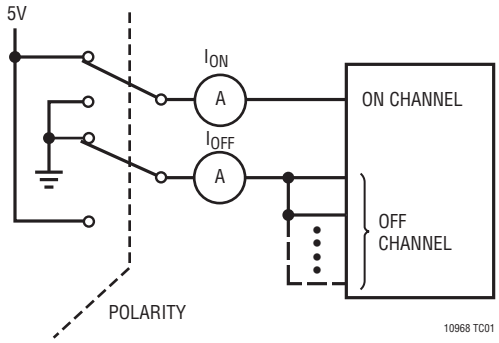
BLOCK DIAGRAM

LTC1096/LTC1096L

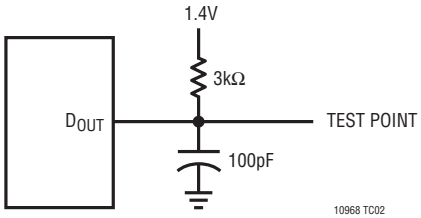


TEST CIRCUITS

On and Off Channel Leakage Current

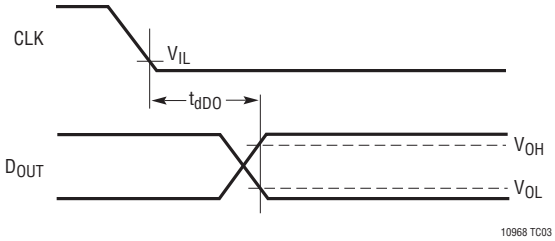


Load Circuit for t_{dDO}, t_r and t_f

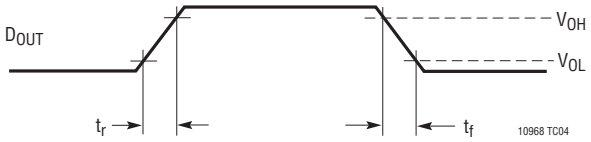


TEST CIRCUITS

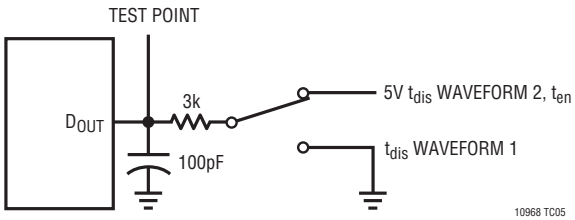
Voltage Waveforms for D_{OUT} Delay Time, t_{dDO}



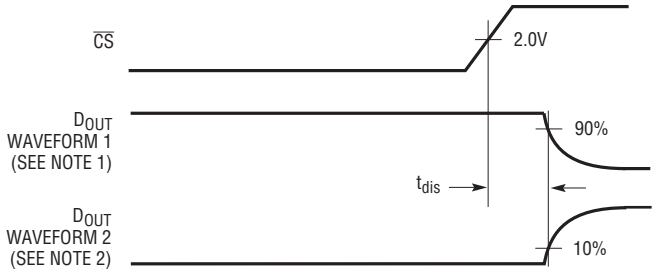
Voltage Waveforms for D_{OUT} Rise and Fall Times, t_r, t_f



Load Circuit for t_{dis} and t_{en}



Voltage Waveforms for t_{dis}



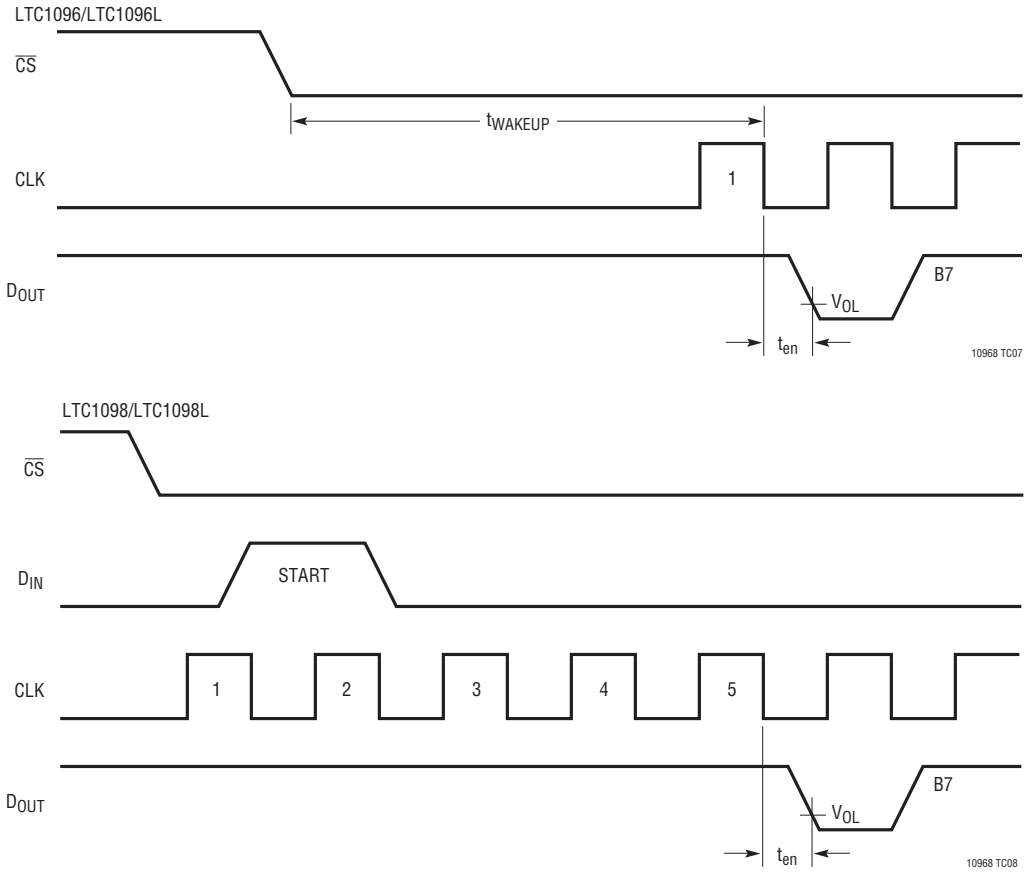
NOTE 1: WAVEFORM 1 IS FOR AN OUTPUT WITH INTERNAL CONDITIONS SUCH THAT THE OUTPUT IS HIGH UNLESS DISABLED BY THE OUTPUT CONTROL.

NOTE 2: WAVEFORM 2 IS FOR AN OUTPUT WITH INTERNAL CONDITIONS SUCH THAT THE OUTPUT IS LOW UNLESS DISABLED BY THE OUTPUT CONTROL.

10968 TC06

TEST CIRCUITS

Voltage Waveforms for t_{en}



APPLICATIONS INFORMATION

OVERVIEW

The LTC1096/LTC1096L/LTC1098/LTC1098L are 8-bit micropower, switched-capacitor A/D converters. These sampling ADCs typically draw 120µA of supply current when sampling up to 33kHz. Supply current drops linearly as the sample rate is reduced (see Supply Current vs Sample Rate on the first page of this data sheet). The ADCs automatically power down when not performing conversion, drawing only leakage current. They are packaged in 8-pin SO packages. The LTC1096L/LTC1098L operate on a single supply ranging from 2.65V to 4V. The LTC1096 operates on a single supply ranging from 3V to 9V while the LTC1098 operates from 3V to 6V supplies.

The LTC1096/LTC1096L/LTC1098/LTC1098L comprise an 8-bit, switched-capacitor ADC, a sample-and-hold and a serial port (see Block Diagram). Although they share the same basic design, the LTC1096(L) and LTC1098(L) differ in some respects. The LTC1096(L) has a differential input and has an external reference input pin. It can measure signals floating on a DC common mode voltage and can operate with reduced spans down to 250mV. Reducing the span allows it to achieve 1mV resolution. The LTC1098(L) has a 2-channel input multiplexer and can convert either channel with respect to ground or the difference between the two.

SERIAL INTERFACE

The LTC1098(L) communicates with microprocessors and other external circuitry via a synchronous, half duplex, 4-wire serial interface while the LTC1096(L) uses a 3-wire interface (see Operating Sequence in Figures 1 and 2).

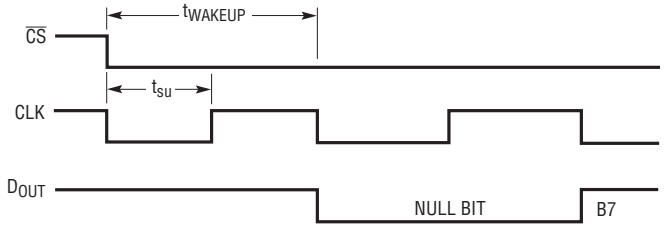
Power Down and Wake-Up Time

The LTC1096(L)/LTC1098(L) draw power when the $\overline{CS}$ pin is low and shut themselves down when that pin is high. In order to have a correct conversion result, a 10µs wake-up time must be provided from $\overline{CS}$ falling to the first falling clock (CLK) after the first rising CLK for the LTC1096(L) and from $\overline{CS}$ falling to the MSBF bit CLK falling for the LTC1098(L) (see Operating Sequence). If the LTC1096(L)/LTC1098(L) are running with clock frequency less than or equal to 100kHz, the wake-up time is inherently provided.

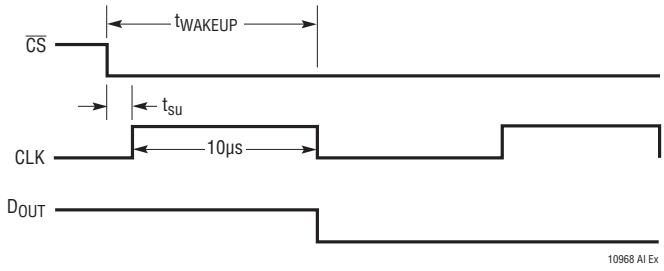
Example

Two cases are shown at right to illustrate the relationship among wake-up time, setup time and CLK frequency for the LT1096(L).

In Case 1 the clock frequency is 100kHz. One clock cycle is 10µs which can be the wake-up time, while half of that can be the setup time. In Case 2 the clock frequency is 50kHz, half of the clock cycle plus the setup time (=1µs) can be the wake-up time. If the CLK frequency is higher than 100kHz, Figure 1 shows the relationship between the wake-up time and setup time.

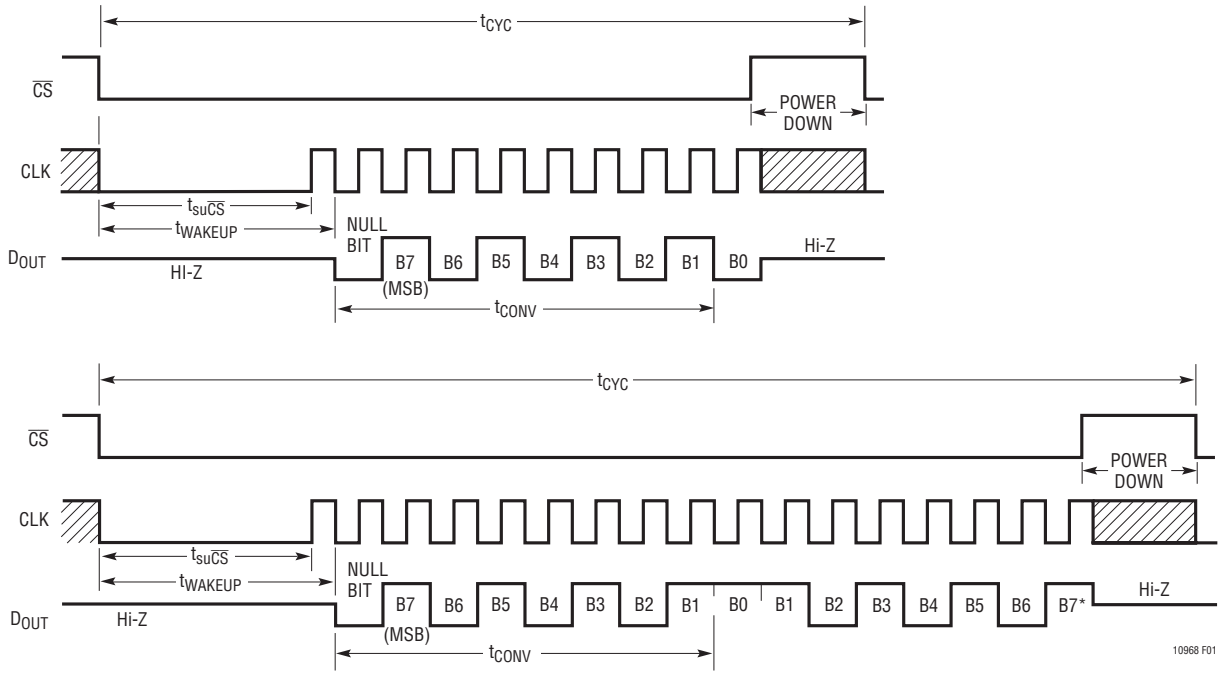


Case 1. Timing Diagram



Case 2. Timing Diagram

APPLICATIONS INFORMATION



*AFTER COMPLETING THE DATA TRANSFER, IF FURTHER CLOCKS ARE APPLIED WITH $\overline{CS}$ LOW, THE ADC WILL OUTPUT ZEROS INDEFINITELY.

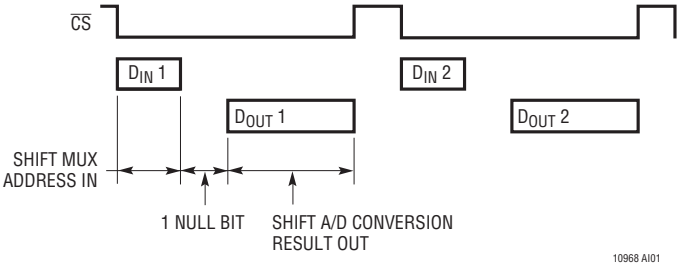
Figure 1. LTC1096(L) Operating Sequence

The wake-up time is inherently provided for the LTC1098(L) with setup time = 1µs (see Figure 2).

Data Transfer

The CLK synchronizes the data transfer with each bit being transmitted on the falling CLK edge and captured on the rising CLK edge in both transmitting and receiving systems. The LTC1098(L) first receives input data and then transmits back the A/D conversion result (half duplex). Because of the half duplex operation, D_{IN} and D_{OUT} may be tied together allowing transmission over just three wires: $\overline{CS}$, CLK and DATA (D_{IN}/D_{OUT}).

Data transfer is initiated by a falling chip select ($\overline{CS}$) signal. After $\overline{CS}$ falls the LTC1098(L) looks for a start bit. After the start bit is received, the 3-bit input word is shifted into the D_{IN} input which configures the LTC1098(L) and starts the conversion. After one null bit, the result of the conversion

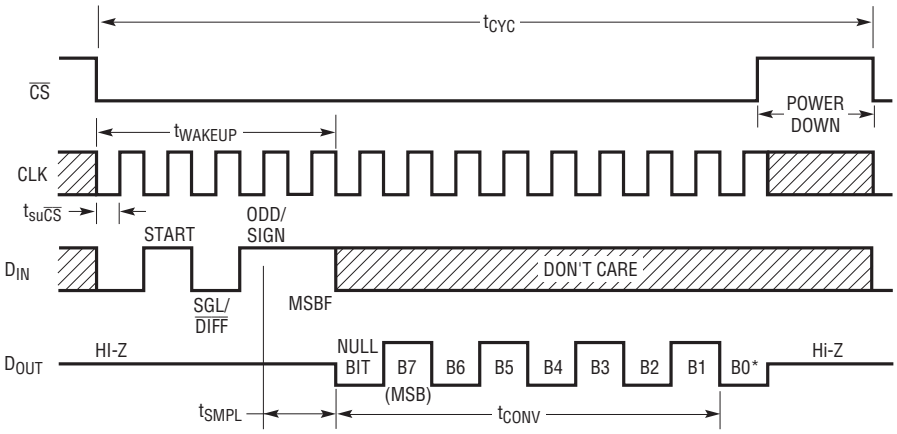


is output on the D_{OUT} line. At the end of the data exchange $\overline{CS}$ should be brought high. This resets the LTC1098(L) in preparation for the next data exchange.

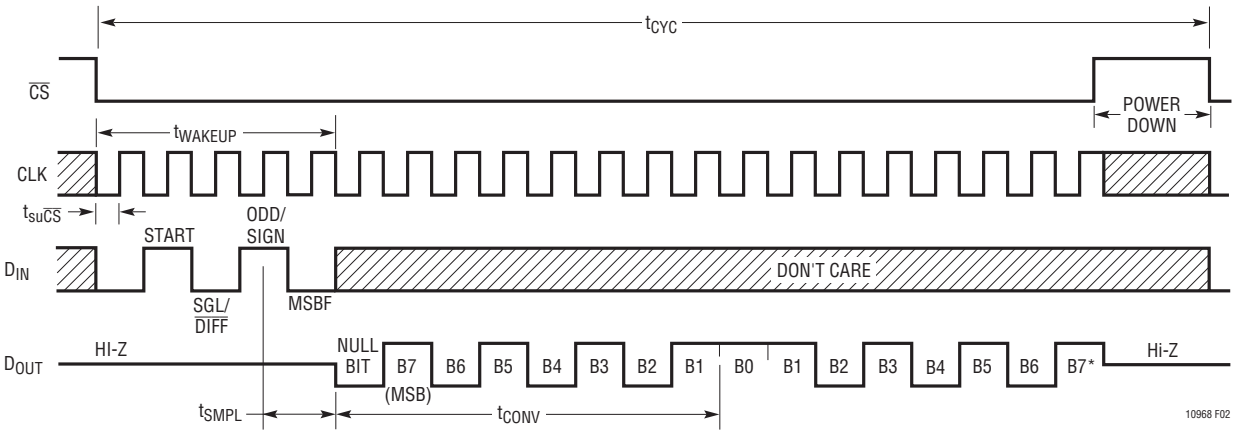
The LTC1096(L) does not require a configuration input word and has no D_{IN} pin. A falling $\overline{CS}$ initiates data transferas shown in the LTC1096(L) operating sequence. After $\overline{CS}$ falls, the first CLK pulse enables D_{OUT}. After one null bit, the A/D conversion result is output on the D_{OUT} line. Bringing $\overline{CS}$ high resets the LTC1096(L) for the next data exchange.

APPLICATIONS INFORMATION

MSB-FIRST DATA (MSBF = 1)



MSB-FIRST DATA (MSBF = 0)



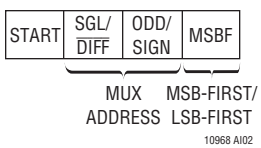
*AFTER COMPLETING THE DATA TRANSFER, IF FURTHER CLOCKS ARE APPLIED WITH $\overline{CS}$ LOW, THE ADC WILL OUTPUT ZEROS INDEFINITELY.

Figure 2. LTC1098(L) Operating Sequence Example: Differential Inputs (CH^+, CH^-)

Input Data Word

The LTC1096(L) requires no D_{IN} word. It is permanently configured to have a single differential input. The conversion result, in which output on the D_{OUT} line is MSB-first sequence, followed by LSB sequence providing easy interface to MSB- or LSB-first serial ports.

The LTC1098(L) clocks data into the D_{IN} input on the rising edge of the clock. The input data words are defined as follows:



Start Bit

The first "logical one" clocked into the D_{IN} input after $\overline{CS}$ goes low is the start bit. The start bit initiates the data transfer. The LTC1098(L) will ignore all leading zeros which precede this logical one. After the start bit is received, the remaining bits of the input word will be clocked in. Further inputs on the D_{IN} pin are then ignored until the next $\overline{CS}$ cycle.

APPLICATIONS INFORMATION

Multiplexer (MUX) Address

The bits of the input word following the START bit assign the MUX configuration for the requested conversion. For a given channel selection, the converter will measure the voltage between the two channels indicated by the "+" and "–" signs in the selected row of the followintg tables. In single-ended mode, all input channels are measured with respect to GND.

LTC1098(L) Channel Selection

	MUX ADDRESS		CHANNEL #		
	SGL/$\overline{DIFF}$	ODD/SIGN	0	1	GND
SINGLE-ENDED MUX MODE	1	0	+		–
	1	1		+	–
DIFFERENTIAL MUX MODE	0	0	+	–	
	0	1	–	+	

10968 AI03

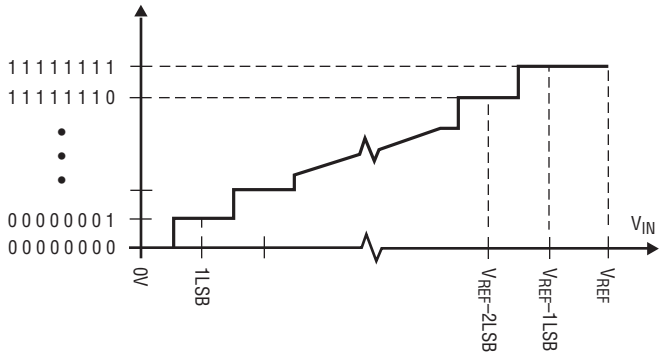
MSB-First/LSB-First (MSBF)

The output data of the LTC1098(L) is programmed for MSB-first or LSB-first sequence using the MSBF bit. When the MSBF bit is a logical one, data will appear on the D_{OUT} line in MSB-first format. Logical zeros will be filled in indefinitely following the last data bit. When the MSBF bit is a logical zero, LSB-first data will follow the normal MSB-first data on the D_{OUT} line. (see Operating Sequence)

Unipolar Transfer Curve

The LTC1096(L)/LTC1098(L) are permanently configured for unipolar only. The input span and code assignment for this conversion type are shown in the following figures for a 5V reference.

Unipolar Transfer Curve



10968 AI04

Unipolar Output Code

OUTPUT CODE	INPUT VOLTAGE	INPUT VOLTAGE (V_{REF} = 5.000V)
11111111	V_{REF} – 1LSB	4.9805V
11111110	V_{REF} – 2LSB	4.9609V
•	•	•
•	•	•
•	•	•
00000001	1LSB	0.0195V
00000000	0V	0V

10968 AI05

Operation with D_{IN} and D_{OUT} Tied Together

The LTC1098(L) can be operated with D_{IN} and D_{OUT} tied together. This eliminates one of the lines required to communicate to the microprocessor (MPU). Data is transmitted in both directions on a single wire. The processor pin connected to this data line should be configurable as either an input or an output. The LTC1098(L) will take control of

APPLICATIONS INFORMATION

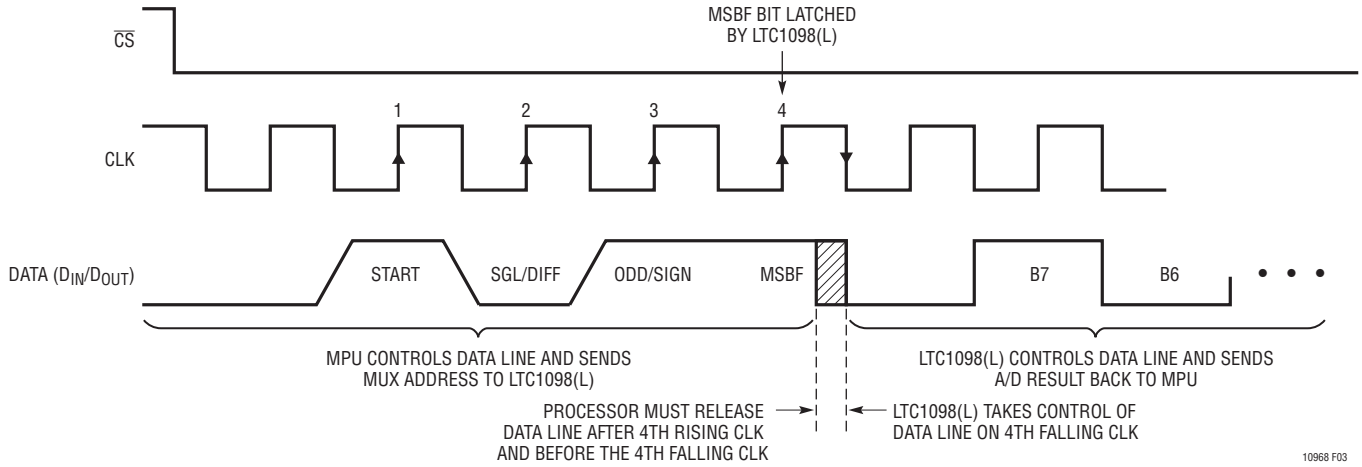


Figure 3. LTC1098(L) Operation with D_{IN} and D_{OUT} Tied Together

the data line and drive it low on the 4th falling CLK edge after the start bit is received (see Figure 3). Therefore the processor port line must be switched to an input before this happens, to avoid a conflict.

In the Typical Applications section, there is an example of interfacing the LTC1098(L) with D_{IN} and D_{OUT} tied together to the Intel 8051 MPU.

ACHIEVING MICROPOWER PERFORMANCE

With typical operating currents of 40µA and automatic shutdown between conversions, the LTC1096/LTC1098 achieves extremely low power consumption over a wide range of sample rates (see Figure 4). In systems that convert continuously, the LTC1096/LTC1098 will draw its normal operating power continuously. Figure 5 shows that the typical current varies from 40µA at clock rates below 50kHz to 100µA at 500kHz. Several things must be taken into account to achieve such a low power consumption.

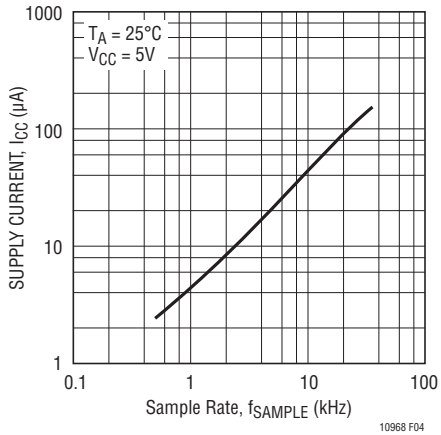


Figure 4. Automatic Power Shutdown Between Conversions Allows Power Consumption to Drop with Sample Rate

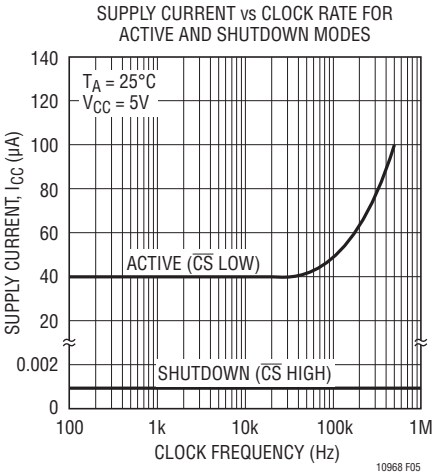


Figure 5. After a Conversion, When the Microprocessor Drives CS High, the ADC Automatically Shuts Down Until the Next Conversion. The Supply Current, Which Is Very Low During cConversions, Drops to Zero in Shutdown

Shutdown

Figures 1 and 2 show the operating sequence of the LTC1096/LTC1098. The converter draws power when the CS pin is low and powers itself down when that pin is high. If the CS pin is not taken to ground when it is low and not taken to supply voltage when it is high, the input buffers

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of the converter will draw current. This current may be larger than the typical supply current. It is worthwhile to bring the $\overline{CS}$ pin all the way to ground when it is low and all the way to supply voltage when it is high to obtain the lowest supply current.

When the $\overline{CS}$ pin is high (= supply voltage), the converter is in shutdown mode and draws only leakage current. The status of the D_{IN} and CLK input have no effect on supply current during this time. There is no need to stop D_{IN} and CLK with $\overline{CS}$ = high, except the MPU may benefit.

Minimize $\overline{CS}$ Low Time

In systems that have significant time between conversions, lowest power drain will occur with the minimum $\overline{CS}$ low time. Bringing $\overline{CS}$ low, waiting 10µs for the wake-up time, transferring data as quickly as possible, and then bringing it back high will result in the lowest current drain. This minimizes the amount of time the device draws power. Even though the device draws more power at high clock rates, the net power is less because the device is on for a shorter time.

D_{OUT} Loading

Capacitive loading on the digital output can increase power consumption. A 100pF capacitor on the D_{OUT} pin can more than double the 100µA supply current drain at a 500kHz clock frequency. An extra 100µA or so of current goes into charging and discharging the load capacitor. The same goes for digital lines driven at a high frequency by any logic. The CxVxf currents must be evaluated and the troublesome ones minimized.

Lower Supply Voltage

For lower supply voltages, LTC offers the LTC1096L/LTC1098L. These pin compatible devices offer specified performance to 2.65V_{MIN} supply.

OPERATING ON OTHER THAN 5V SUPPLIES

The LTC1096 operates from 3V to 9V supplies and the LTC1098 operates from 3V to 6V supplies. To operate the LTC1096/LTC1098 on other than 5V supplies, a few things must be kept in mind.

Wake-Up Time

A 10µs wake-up time must be provided for the ADCs to convert correctly on a 5V supply. The wake-up time is typically less than 3µs over the supply voltage range (see typical curve of Wake-Up Time vs Supply Voltage). With 10µs wake-up time provided over the supply range, the ADCs will have adequate time to wake up and acquire input signals.

Input Logic Levels

The input logic levels of $\overline{CS}$, CLK and D_{IN} are made to meet TTL on 5V supply. When the supply voltage varies, the input logic levels also change. For the LTC1096/LTC1098 to sample and convert correctly, the digital inputs have to meet logic low and high levels relative to the operating supply voltage (see typical curve of Digital Input Logic Threshold vs Supply Voltage). If achieving micropower consumption is desirable, the digital inputs must go rail-to-rail between supply voltage and ground (see ACHIEVING MICROPOWER PERFORMANCE section).

Clock Frequency

The maximum recommended clock frequency is 500kHz for the LTC1096/LTC1098 running off a 5V supply. With the supply voltage changing, the maximum clock frequency for the devices also changes (see the typical curve of Maximum Clock Rate vs Supply Voltage). If the maximum clock frequency is used, care must be taken to ensure that the device converts correctly.

Mixed Supplies

It is possible to have a microprocessor running off a 5V supply and communicate with the LTC1096/LTC1098 operating on 3V or 9V supplies. The requirement to achieve this is that the outputs of $\overline{CS}$, CLK and D_{IN} from the MPU have to be able to trip the equivalent inputs of the ADCs and the output of D_{OUT} from the ADCs must be able to toggle the equivalent input of the MPU (see typical curve of Digital Input Logic Threshold vs Supply Voltage). With the LTC1096 operating on a 9V supply, the output of D_{OUT} may go between 0V and 9V. The 9V output may damage the MPU running off a 5V supply. The way to get around this possibility is to have a resistor divider on D_{OUT}

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(Figure 6) and connect the center point to the MPU input. It should be noted that to get full shutdown, the $\overline{CS}$ input of the LTC1096/LTC1098 must be driven to the V_{CC} voltage. This would require adding a level shift circuit to the $\overline{CS}$ signal in Figure 6.

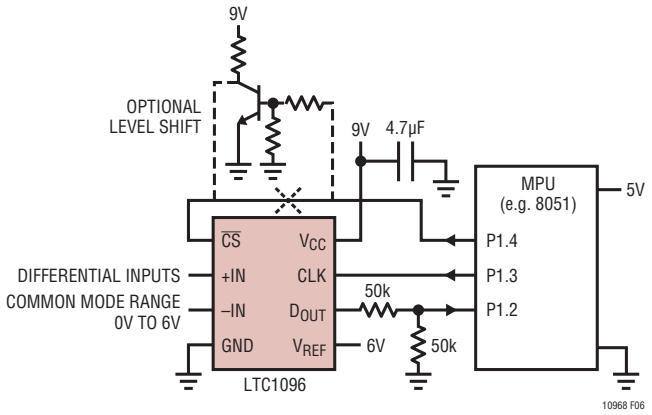


Figure 6. Interfacing a 9V Powered LTC1096 to a 5V System

BOARD LAYOUT CONSIDERATIONS

Grounding and Bypassing

The LTC1096(L)/LTC1098(L) should be used with an analog ground plane and single point grounding techniques. The GND pin should be tied directly to the ground plane.

The V_{CC} pin should be bypassed to the ground plane with a 1µF tantalum with leads as short as possible. If power supply is clean, the LTC1096(L)/LTC1098(L) can also operate with smaller 0.1µF surface mount or ceramic bypass capacitors. All analog inputs should be referenced directly to the single point ground. Digital inputs and outputs should be shielded from and/or routed away from the reference and analog circuitry.

SAMPLE-AND-HOLD

Both the LTC1096(L) and the LTC1098(L) provide a built-in sample-and-hold (S&H) function to acquire signals. The S&H of the LTC1096(L) acquires input signals from "+" input relative to "–" input during the t_{WAKEUP} time (see Figure 1). However, the S&H of the LTC1098(L) can sample input signals in the single-ended mode or in the differential inputs during the t_{SMPL} time (see Figure 7).

Single-Ended Inputs

The sample-and-hold of the LTC1098(L) allows conversion of rapidly varying signals. The input voltage is sampled during the t_{SMPL} time as shown in Figure 7. The sampling interval begins as the bit preceding the MSBF bit is shifted

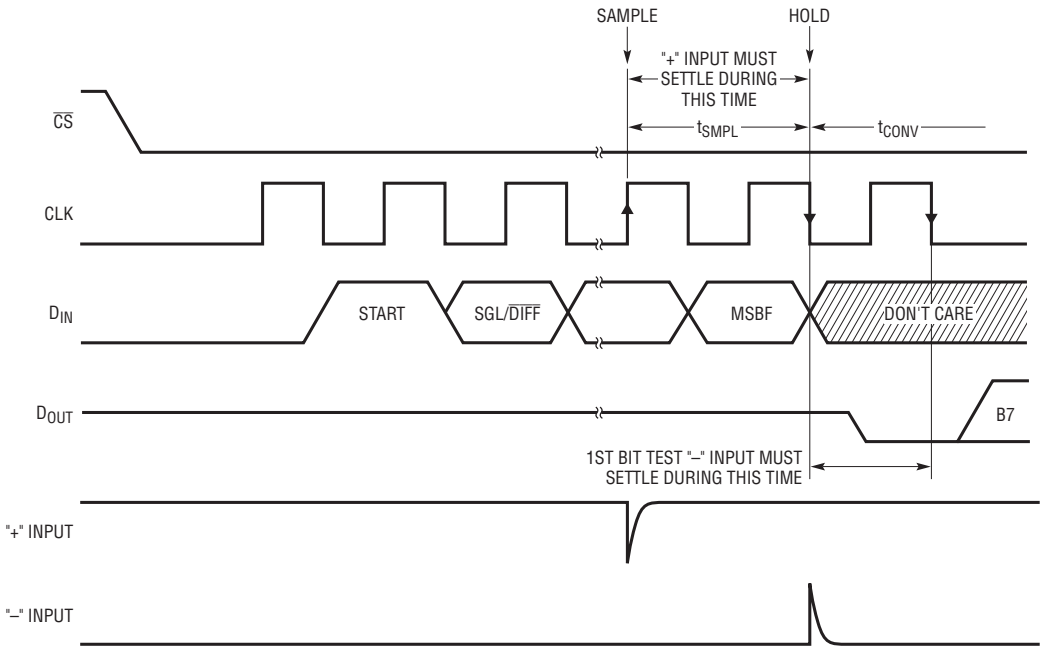


Figure 7. LTC1098(L) "+" and "–" Input Settling Windows

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in and continues until the falling CLK edge after the MSBF bit is received. On this falling edge, the S&H goes into hold mode and the conversion begins.

Differential Inputs

With differential inputs, the ADC no longer converts just a single voltage but rather the difference between two voltages. In this case, the voltage on the selected "+" input is still sampled and held and therefore may be rapidly time varying just as in single-ended mode. However, the voltage on the selected "–" input must remain constant and be free of noise and ripple throughout the conversion time. Otherwise, the differencing operation may not be performed accurately. The conversion time is 8 CLK cycles. Therefore, a change in the "–" input voltage during this interval can cause conversion errors. For a sinusoidal voltage on the "–" input this error would be:

$$V_{ERROR\ (MAX)} = V_{PEAK} \bullet 2 \bullet \pi \bullet f(\text{"–"}) \bullet 8/f_{CLK}$$

Where f("–") is the frequency of the "–" input voltage, V_{PEAK} is its peak amplitude and f_{CLK} is the frequency of the CLK. In most cases V_{ERROR} will not be significant. For a 60Hz signal on the "–" input to generate a 1/4LSB error (5mV) with the converter running at CLK = 500kHz, its peak value would have to be 750mV.

ANALOG INPUTS

Because of the capacitive redistribution A/D conversion techniques used, the analog inputs of the LTC1096(L)/LTC1098(L)have capacitive switching input current spikes. These current spikes settle quickly and do not cause a problem. However, if large source resistances are used or if slow settling op amps drive the inputs, care must be taken to ensure that the transients caused by the current spikes settle completely before the conversion begins.

"+" Input Settling

The input capacitor of the LTC1096(L) is switched onto "+" input during the wake-up time (see Figure 1) and samples the input signal within that time. However, the input capacitor of the LTC1098(L) is switched onto "+" input during the sample phase (t_{SMPL}, see Figure 7). The sample phase is 1.5 CLK cycles before conversion starts. The voltage on the "+" input must settle completely within t_{WAKEUP} or t_{SMPL} for the LTC1096(L) or the LTC1098(L) respectively. Minimizing R_{SOURCE}^+ and C1 will improve the input settling time. If a large "+" input source resistance must be used, the sample time can be increased by using a slower CLK frequency.

"–" Input Settling

At the end of the t_{WAKEUP} or t_{SMPL}, the input capacitor switches to the "–" input and conversion starts (see Figures 1 and 7). During the conversion the "+" input voltage is effectively "held" by the sample-and-hold and will not affect the conversion result. However, it is critical that the "–" input voltage settles completely during the first CLK cycle of the conversion time and be free of noise. Minimizing R_{SOURCE}^- and C2 will improve settling time. If a large "–" input source resistance must be used, the time allowed for settling can be extended by using a slower CLK frequency.

Input Op Amps

When driving the analog inputs with an op amp it is important that the op amp settle within the allowed time (see Figure 7). Again, the "+" and "–" input sampling times can be extended as described above to accommodate slower op amps. Most op amps, including the LT1006 and LT1413 single supply op amps, can be made to settle well even with the minimum settling windows of 3µs ("+" input) which occur at the maximum clock rate of 500kHz.

Source Resistance

The analog inputs of the LTC1096/LTC1098 look like a 25pF capacitor (C_{IN}) in series with a 500Ω resistor (R_{ON}) as shown in Figure 8. C_{IN} gets switched between the selected "+" and "–" inputs once during each conversion cycle.

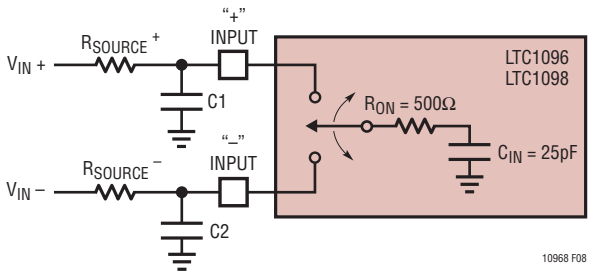


Figure 8. Analog Input Equivalent Circuit

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Large external source resistors and capacitances will slow the settling of the inputs. It is important that the overall RC time constants be short enough to allow the analog inputs to completely settle within the allowed time.

RC Input Filtering

It is possible to filter the inputs with an RC network as shown in Figure 9. For large values of C_F (e.g., 1µF), the capacitive input switching currents are averaged into a net DC current. Therefore, a filter should be chosen with a small resistor and large capacitor to prevent DC drops across the resistor. The magnitude of the DC current is approximately $I_{DC} = 25pF(V_{IN}/t_{CYC})$ and is roughly proportional to V_{IN}. When running at the minimum cycle time of 29µs, the input current equals 4.3µA at $V_{IN} = 5V$. In this case, a filter resistor of 390Ω will cause 0.1LSB of full-scale error. If a larger filter resistor must be used, errors can be eliminated by increasing the cycle time.

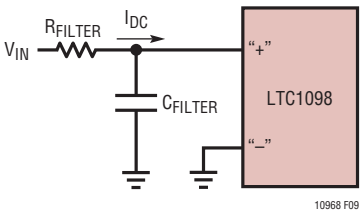


Figure 9. RC Input Filtering

Input Leakage Current

Input leakage currents can also create errors if the source resistance gets too large. For instance, the maximum input leakage specification of 1µA (at 125°C) flowing through a source resistance of 3.9k will cause a voltage drop of 3.9mV or 0.2LSB. This error will be much reduced at lower temperatures because leakage drops rapidly (see typical curve of Input Channel Leakage Current vs Temperature).

REFERENCE INPUTS

The voltage on the reference input of the LTC1096 defines the voltage span of the A/D converter. The reference input transient capacitive switching currents due to the switched-capacitor conversion technique (see Figure 10). During each bit test of the conversion (every CLK cycle), a capacitive current spike will be generated on the reference pin by the ADC. These current spikes settle quickly and do not cause a problem.

Using a slower CLK will allow more time for the reference to settle. Even at the maximum CLK rate of 500kHz most references and op amps can be made to settle within the 2µs bit time.

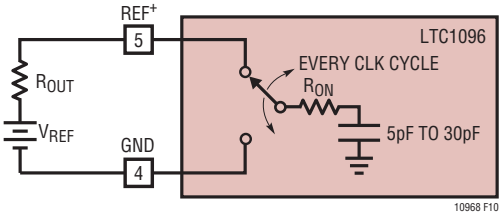


Figure 10. Reference Input Equivalent Circuit

Reduced Reference Operation

The minimum reference voltage of the LTC1098 is limited to 3V because the V_{CC} supply and reference are internally tied together. However, the LTC1096 can operate with reference voltages below 1V.

The effective resolution of the LTC1096 can be increased by reducing the input span of the converter. The LTC1096 exhibits good linearity and gain over a wide range of reference voltages (see typical curves of Linearity and Full Scale Error vs Reference Voltage). However, care must be taken when operating at low values of V_{REF} because of the reduced LSB step size and the resulting higher accuracy requirement placed on the converter. The following factors must be considered when operating at low V_{REF} values.

1. Offset
2. Noise
3. Conversion speed (CLK frequency)

Offset with Reduced V_{REF}

The offset of the LTC1096 has a larger effect on the output code when the ADC is operated with reduced reference voltage. The offset (which is typically a fixed voltage) becomes a larger fraction of an LSB as the size of the LSB is reduced. The typical curve of Unadjusted Offset Error vs Reference Voltage shows how offset in LSBs is

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related to reference voltage for a typical value of V_{OS}. For example, a V_{OS} of 2mV which is 0.1LSB with a 5V reference becomes 0.5LSB with a 1V reference and 2.5LSBs with a 0.2V reference. If this offset is unacceptable, it can be corrected digitally by the receiving system or by offsetting the "–" input of the LTC1096.

Noise with Reduced V_{REF}

The total input referred noise of the LTC1096 can be reduced to approximately 1mV peak-to-peak using a ground plane, good bypassing, good layout techniques and minimizing noise on the reference inputs. This noise is insignificant with a 5V reference but will become a larger fraction of an LSB as the size of the LSB is reduced.

For operation with a 5V reference, the 1mV noise is only 0.05LSB peak-to-peak. In this case, the LTC1096 noise will contribute virtually no uncertainty to the output code. However, for reduced references, the noise may become a significant fraction of an LSB and cause undesirable jitter in the output code. For example, with a 1V reference, this same 1mV noise is 0.25LSB peak-to-peak. This will reduce the range of input voltages over which a stable output code can be achieved by 1LSB. If the reference is further reduced to 200mV, the 1mV noise becomes equal to 1.25LSBs and a stable code may be difficult to achieve. In this case averaging readings may be necessary.

This noise data was taken in a very clean setup. Any setup-induced noise (noise or ripple on V_{CC}, V_{REF} or V_{IN}) will add to the internal noise. The lower the reference voltage to be used, the more critical it becomes to have a clean, noise free setup.

Conversion Speed with Reduced V_{REF}

With reduced reference voltages the LSB step size is reduced and the LTC1096 internal comparator overdrive is reduced. Therefore, it may be necessary to reduce the maximum CLK frequency when low values of V_{REF} are used.

Input Divider

It is OK to use an input divider on the reference input of the LTC1096 as long as the reference input can be made to settle within the bit time at which the clock is running. When using a larger value resistor divider on the reference input the "–" input should be matched with an equivalent resistance.

Bypassing Reference Input with Divider

Bypassing the reference input with a divider is also possible. However, care must be taken to make sure that the DC voltage on the reference input will not drop too much below the intended reference voltage.

AC PERFORMANCE

Two commonly used figures of merit for specifying the dynamic performance of the ADCs in digital signal processing applications are the signal-to-noise ratio (SNR) and the effective number of bits (ENOBs).

Signal-to-Noise Ratio

The signal-to-noise ratio (SNR) is the ratio between the RMS amplitude of the fundamental input frequency to the RMS amplitude of all other frequency components at the A/D output. This includes distortion as well as noise products and for this reason it is sometimes referred to as signal-to-noise + distortion [S/(N + D)]. The output is band limited to frequencies from DC to one half the sampling frequency. Figure 11 shows spectral content from DC to 15.625kHz which is 1/2 the 31.25kHz sampling rate.

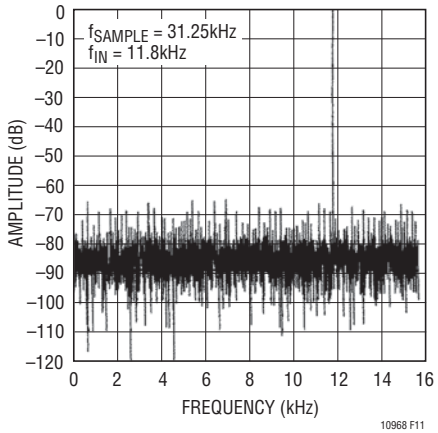


Figure 11. This Clean FFT of an 11.8kHz Input Shows Remarkable Performance for an ADC That Draws Only 100µA When Sampling at the 31.25kHz Rate

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Effective Number of Bits

The effective number of bits (ENOBs) is a measurement of the resolution of an A/D and is directly related to the S/(N + D) by the equation:

$$ENOB = [S/(N + D) - 1.76]/6.02$$

where S/(N + D) is expressed in dB. At the maximum sampling rate of 33kHz the LTC1096 maintains 7.5 ENOBs or better to 40kHz. Above 40kHz the ENOBs gradually decline, as shown in Figure 12, due to increasing second harmonic distortion. The noise floor remains approximately 70dB.

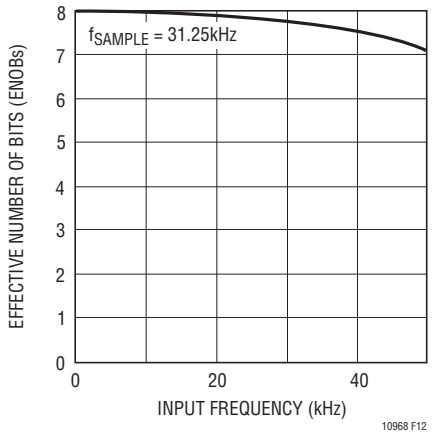


Figure 12. Dynamic Accuracy Is Maintained Up to an Input Frequency of 40kHz

TYPICAL APPLICATIONS

MICROPROCESSOR INTERFACES

The LTC1096(L)/LTC1098(L) can interface directly (without external hardware to most popular microprocessor (MPU) synchronous serial formats (see Table 1). If an MPU without a dedicated serial port is used, then three or four of the MPU's parallel port lines can be programmed to form the serial link to the LTC1096(L)/LTC1098(L). Included here is one serial interface example and one example showing a parallel port programmed to form the serial interface.

Motorola SPI (MC68HC05C4,CM68HC11)

The MC68HC05C4 has been chosen as an example of an MPU with a dedicated serial port. This MPU transfer data MSB-first and in 8-bit increments. With two 8-bit transfers, the A/D result is read into the MPU. The first 8-bit transfer sends the D_{IN} word to the LTC1098(L) and clocks into the processor. The second 8-bit transfer clocks the A/D conversion result, B7 through B0, into the MPU.

ANDing the first MUP received byte with 00Hex clears the first byte. Notice how the position of the start bit in the first MPU transmit word is used to position the A/D result right-justified in two memory locations.

Table 1. Microprocessor with Hardware Serial Interfaces Compatible with the LTC1096(L)/LTC1098(L)

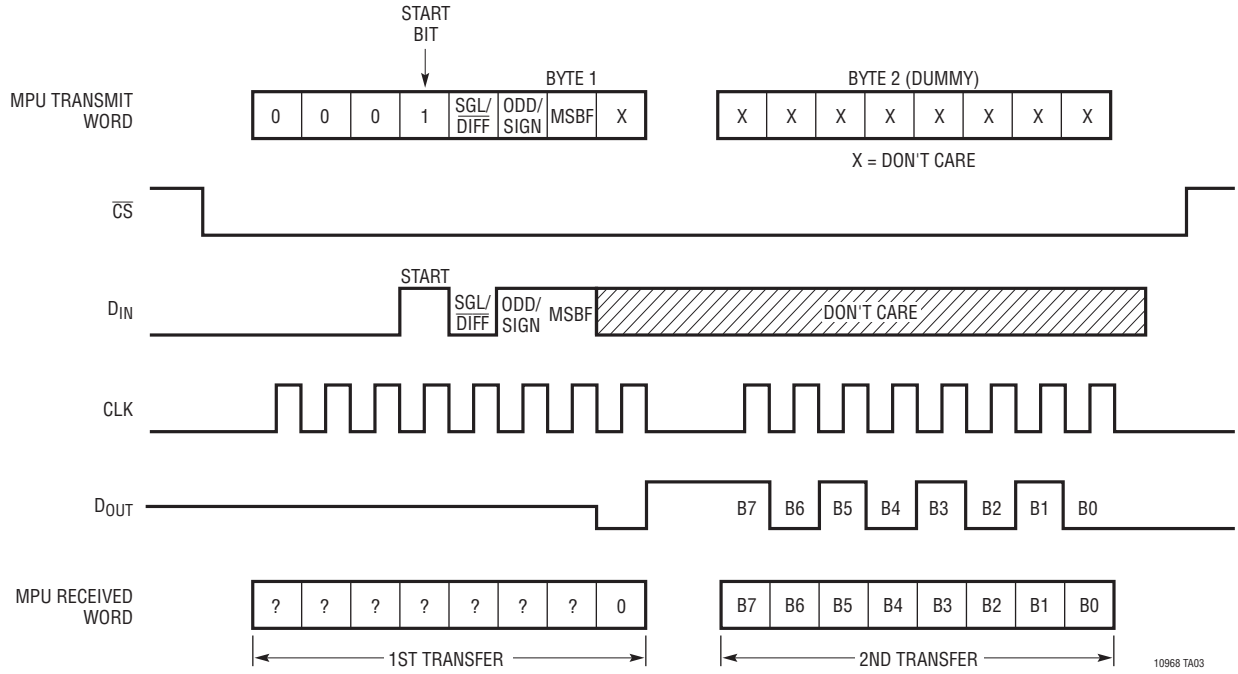
PART NUMBER	TYPE OF INTERFACE
Motorola	
MC6805S2,S3	SPI
MC68HC11	SPI
MC68HC05	SPI
RCA	
CDP68HC05	SPI
Hitachi	
HD6305	SCI Synchronous
HD63705	SCI Synchronous
HD6301	SCI Synchronous
HD63701	SCI Synchronous
HD6303	SCI Synchronous
HD64180	CSI/O
National Semiconductor	
COP400 Family	MICROWIRE™
COP800 Family	MICROWIRE/PLUS™
NS8050U	MICROWIRE/PLUS
HPC16000 Family	MICROWIRE/PLUS
Texas Instruments	
TMS7002	Serial Port
TMS7042	Serial Port
TMS70C02	Serial Port
TMS70C42	Serial Port
TMS32011*	Serial Port
TMS32020	Serial Port

* Requires external hardware

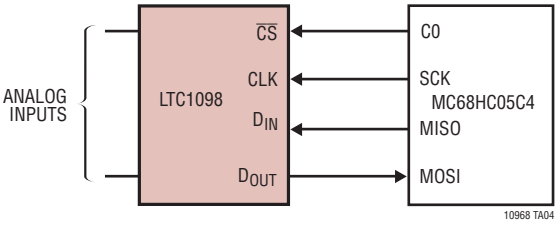
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TYPICAL APPLICATIONS

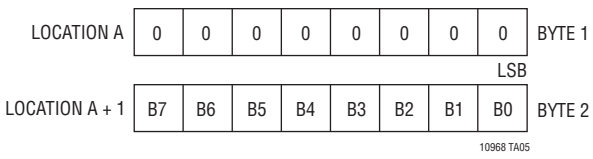
Data Exchange Between LTC1098(L) and MC68HC05C4



Hardware and Software Interface to Motorola MC68HC05C4



D_{OUT} from LTC1098(L) Stored in MC68HC05C4



LABEL	MNEMONIC	COMMENTS
START	BCLRn	Bit 0 Port C goes low ($\overline{CS}$ goes low)
	LDA	Load LTC1098(L) D_{IN} word into Acc.
	STA	Load LTC1098(L) D_{IN} word into SPI from Acc. Transfer begins.
	TST	Test status of SPIF
	BPL	Loop to previous instruction if not done with transfer
	LDA	Load contents of SPI data register into Acc. (D_{OUT} MSBs)
	STA	Start next SPI cycle
	AND	Clear the first D_{OUT} word
	STA	Store in memory location A (MSBs)
	TST	Test status of SPIF
	BPL	Loop to previous instruction if not done with transfer
	BSETn	Set B0 of Port C ($\overline{CS}$ goes high)
	LDA	Load contents of SPI data register into Acc. (D_{OUT} LSBs)
	STA	Store in memory location A + 1 (LSBs)

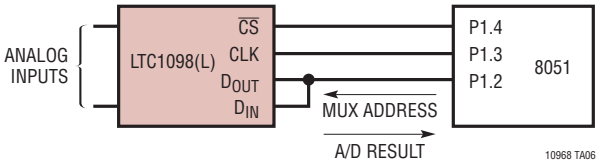
TYPICAL APPLICATIONS

Interfacing to the Parallel Port of the Intel 8051 Family

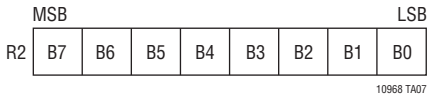
The Intel 8051 has been chosen to demonstrate the interface between the LTC1098(L) and parallel port microprocessors. Normally the $\overline{CS}$, CLK and D_{IN} signals would be generated on three port lines and the D_{OUT} signal read on a fourth port line. This works very well. However, we will demonstrate here an interface with the D_{IN} and D_{OUT} of the LTC1098(L) tied together as described in the SERIAL INTERFACE section. This saves one wire.

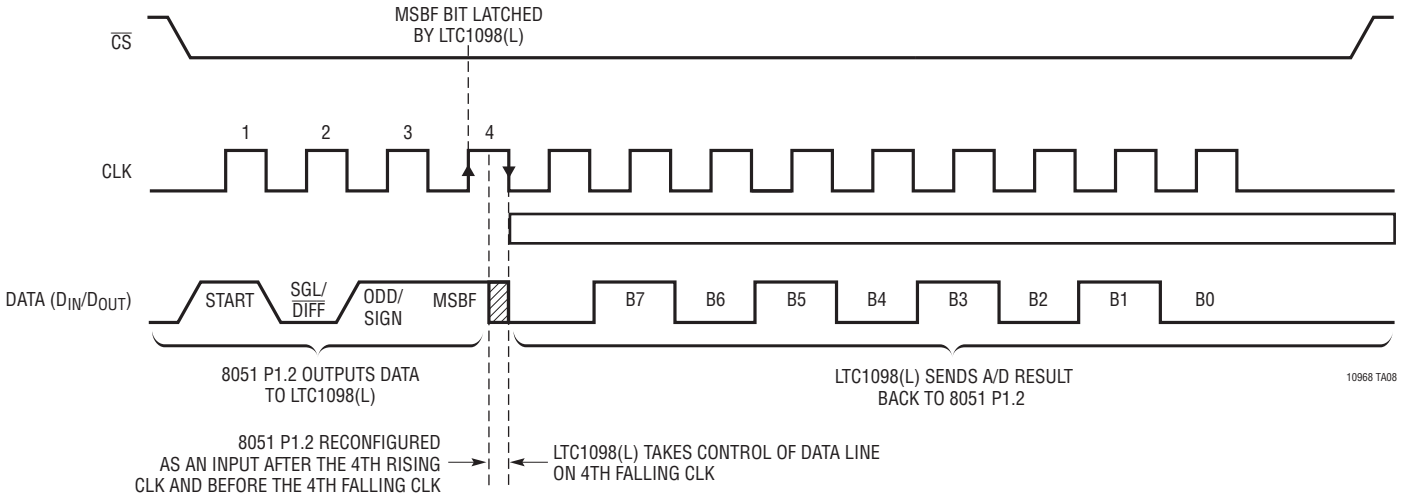
The 8051 first sends the start bit and MUX address to the LTC1098(L) over the data line connected to P1.2. Then P1.2 is reconfigured as an input (by writing to it a one) and the 8051 reads back the 8-bit A/D result over the same data line.

LABEL	MNEMONIC	OPERAND	COMMENTS
	MOV	A, #FFH	D_{IN} word for LTC1098(L)
	SETB	P1.4	Make sure $\overline{CS}$ is high
	CLR	P1.4	$\overline{CS}$ goes low
LOOP 1	MOV	R4, #04	Load counter
	RLC	A	Rotate D_{IN} bit into Carry
	CLR	P1.3	CLK goes low
	MOV	P1.2, C	Output D_{IN} bit to LTC1098(L)
	SETB	P1.3	CLK goes high
	DJNZ	R4, LOOP 1	Next bit
	MOV	P1, #04	Bit 2 becomes an input
	CLR	P1.3	CLK goes low
LOOP	MOV	R4, #09	Load counter
	MOV	C, P1.2	Read data bit into Carry
	RLC	A	Rotate data bit into Acc.
	SETB	P1.3	CLK goes high
	CLR	P1.3	CLK goes low
	DJNZ	R4, LOOP	Next bit
	MOV	R2, A	Store MSBs in R2
	SETB	P1.4	$\overline{CS}$ goes high



D_{OUT} from LTC1098(L) Stored in 8051 RAM





A "Quick Look" Circuit for the LTC1096

Users can get a quick look at the function and timing of the LT1096 by using the following simple circuit (Figure 13). V_{REF} is tied to V_{CC}. V_{IN} is applied to the +IN input and the –IN input is tied to the ground. $\overline{CS}$ is driven at 1/16 the clock rate by the 74C161 and D_{OUT} outputs the data. The output data from the D_{OUT} pin can be viewed on an oscilloscope that is set up to trigger on the falling edge of $\overline{CS}$ (Figure 14). Note the LSB data is partially clocked out before $\overline{CS}$ goes high.

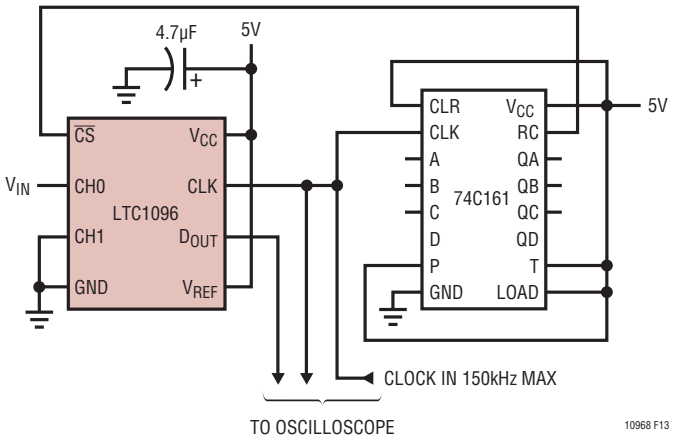


Figure 13. "Quick Look" Circuit for the LTC1096

Figure 15 shows a temperature measurement system. The LTC1096 is connected directly to the low cost silicon temperature sensor. The voltage applied to the V_{REF} pin adjusts the full scale of the A/D to the output range of the sensor. The zero point of the converter is matched to the zero output voltage of the sensor by the voltage on the LTC1096's negative input.

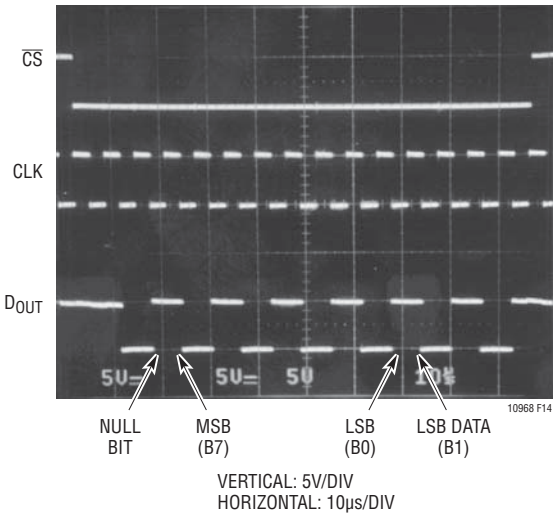


Figure 14. Scope Trace the LTC1096 "Quick Look" Circuit Showing A/D Output 10101010 (AA_{HEX})

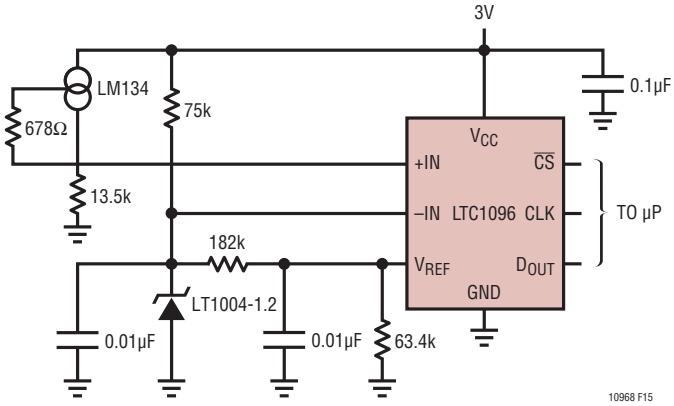


Figure 15. The LTC1096's High Impedance Input Connects Directly to This Temperature Sensor, Eliminating Signal Conditioning Circuitry in This 0°C to 70°C Thermometer

Remote or Isolated Systems

Figure 16 shows a floating system that sends data to a grounded host system. The floating circuitry is isolated by two optoisolators and powered by a simple capacitor diode charge pump. The system has very low power requirements because the LTC1096 shuts down between conversions and the optoisolators draw power only when data is being transferred. The system consumes only 50µA at a sample rate of 10Hz (1ms on-time and 99ms off-time). This is easily within the current supplied by the charge pump running at 5MHz. If a truly isolated system is required, the system's low power simplifies generating an isolated supply or powering the system from a battery.

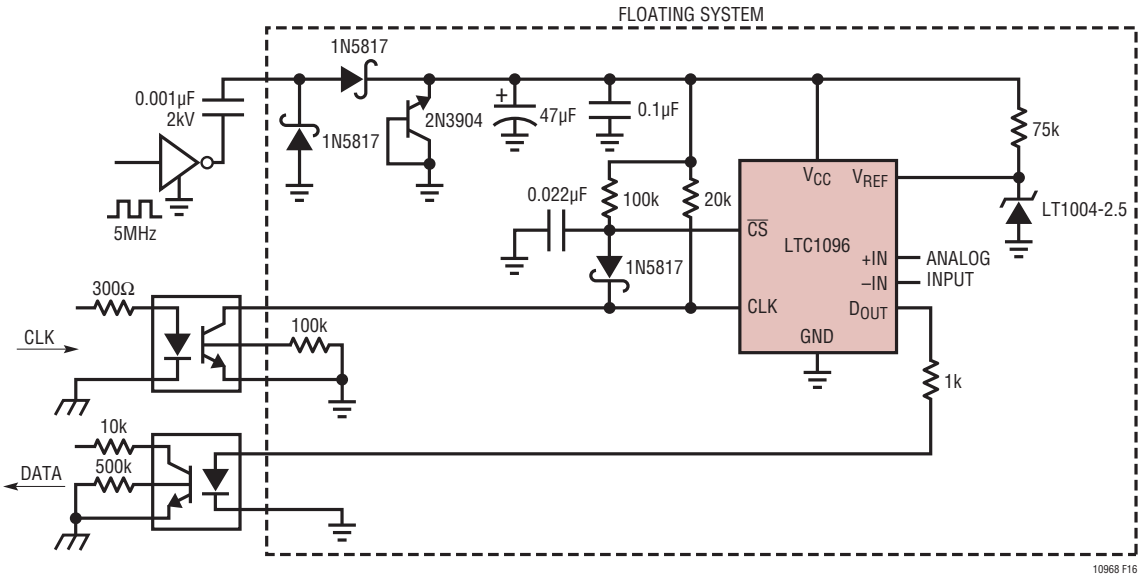
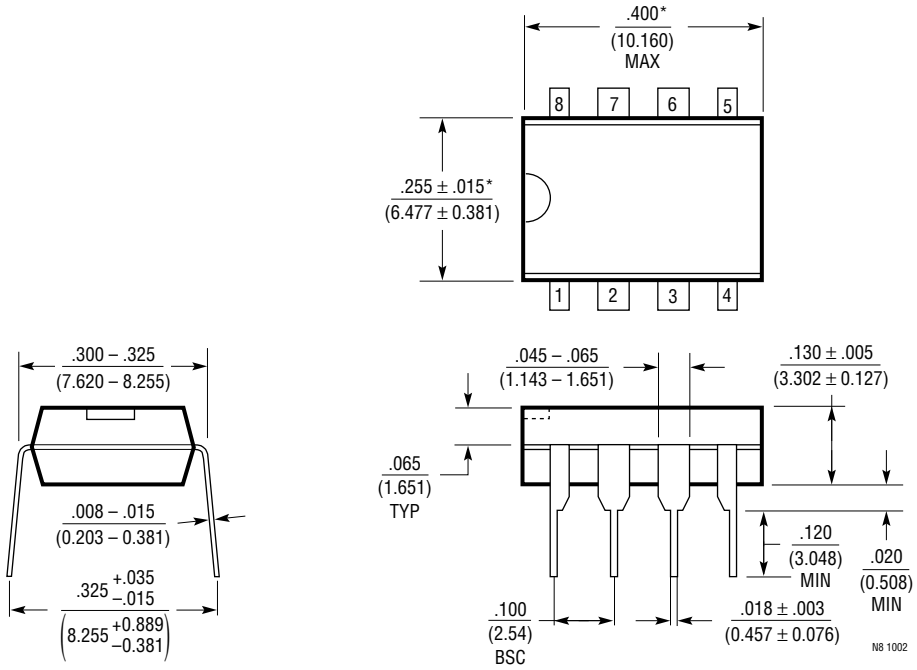


Figure 16. Power for This Floating A/D System Is Provided by a Simple Capacitor Diode Charge Pump. The Two Optoisolators Draw No Current Between Samples, Turning On Only to Send the Clock and Receive Data

PACKAGE DESCRIPTION

N8 Package
8-Lead PDIP (Narrow .300 Inch)
(Reference LTC DWG # 05-08-1510)

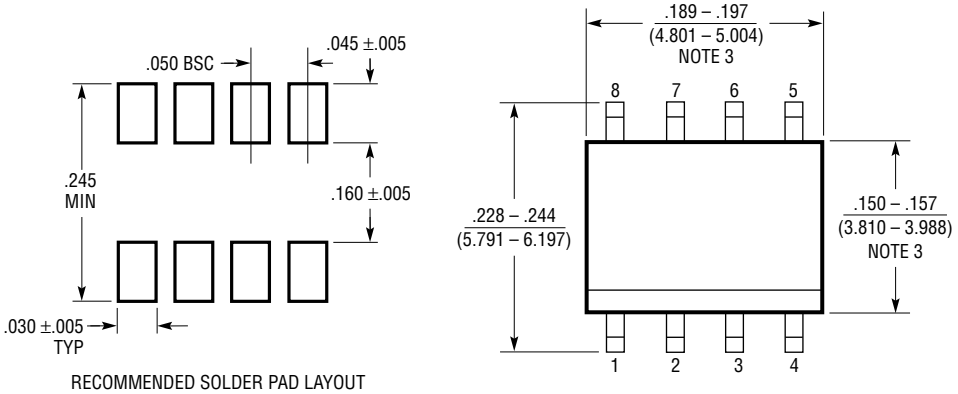


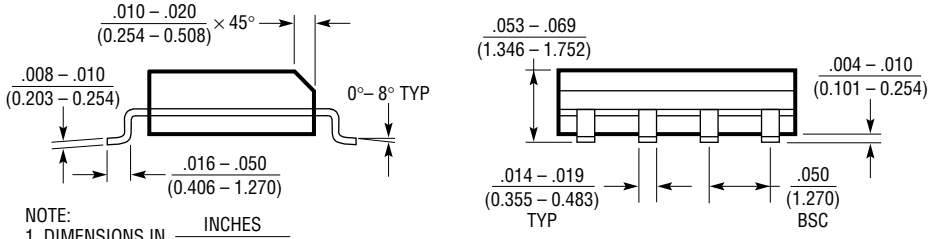
NOTE:
1. DIMENSIONS ARE INCHES / MILLIMETERS

*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH (0.254mm)

PACKAGE DESCRIPTION

S8 Package
8-Lead Plastic Small Outline (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1610)





NOTE:
1. DIMENSIONS IN $\frac{\text{INCHES}}{(\text{MILLIMETERS})}$
2. DRAWING NOT TO SCALE
3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
   MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)

SO8 0303

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TYPICAL APPLICATION

A/D Conversion for 3V Systems

The LTC1096/LTC1098 are ideal for 3V systems. Figure 17 shows a 3V to 6V battery current monitor that draws only 70µA from the battery it monitors. The battery current is sensed with the 0.02Ω resistor and amplified by the LT1178. The LTC1096 digitizes the amplifier output and sends it to the microprocessor in serial format. The LT1004 provides the full-scale reference for the ADC. The other half of the LTC1178 is used to provide low battery detection. The circuit's 70µA supply current is dominated by the op amps and the reference. The circuit can be located near the battery and data transmitted serially to the microprocessor.

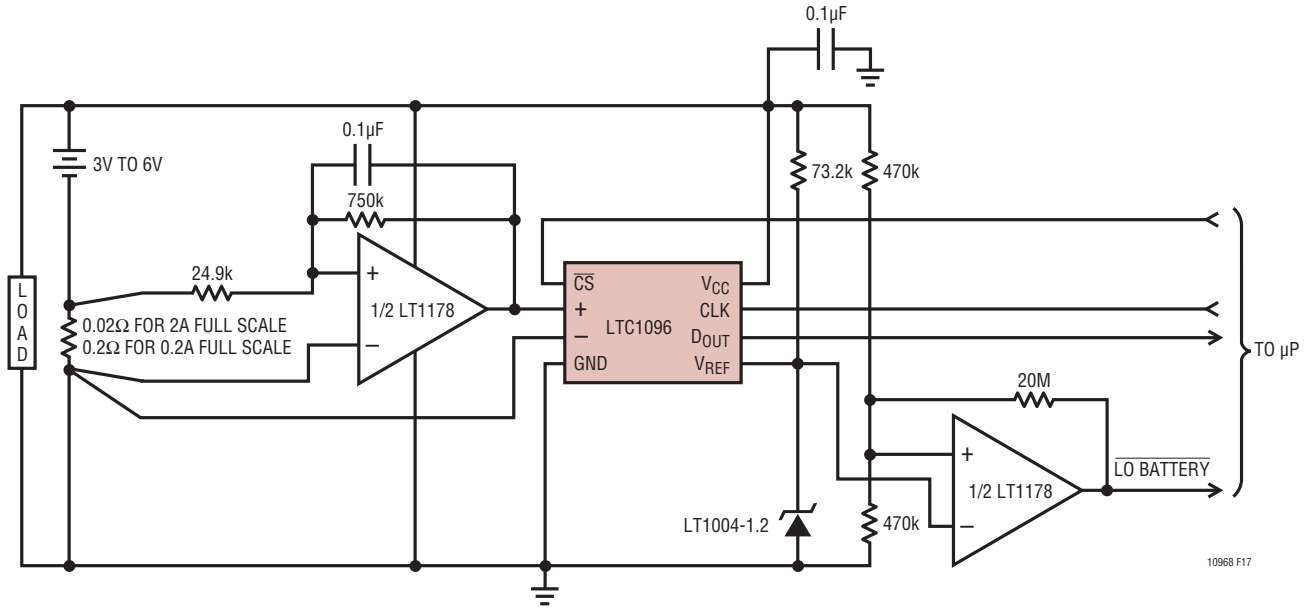


Figure 17. This 0A to 2A Battery Current Monitor Draws Only 70µA from a 3V Battery

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1196/LTC1198	8-Pin SO, 1Msps, 8-Bit ADCs	Low Power, Small Size, Low Cost
LTC1286/LTC1298	8-Pin SO, 5V Micropower, 12-Bit ADCs	1- or 2-Channel, Auto Shutdown
LTC1285/LTC1298	8-Pin SO, 3V Micropower, 12-Bit ADCs	1- or 2-Channel, Auto Shutdown
LTC1400	5V High Speed,Serial 12-Bit ADC	400ksps, Complete with V_{REF}, CLK, Sample-and-Hold
LTC1594/LTC1598	4- and 8-Channel, 5V Micropower, 12-Bit ADCs	Low Power, Small Size, Low Cost
LTC1594L/LTC1598L	4- and 8-Channel, 3V Micropower, 12-Bit ADCs	Low Power, Small Size, Low Cost

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