

65V, 8A Synchronous Step-Down Silent Switcher with 2.5μA Quiescent Current

FEATURES

- Silent Switcher® Architecture
 - Ultralow EMI Emissions
 - Optional Spread Spectrum Modulation
- High Efficiency at High Frequency
 - Up to 95% Efficiency at 1MHz, 12V_{IN} to 5V_{OUT}
 - Up to 94% Efficiency at 2MHz, 12V_{IN} to 5V_{OUT}
- Wide Input Voltage Range: 3.4V to 65V
- Ultralow Quiescent Current Burst Mode Operation
 - 2.5μA I_Q Regulating 12V_{IN} to 3.3V_{OUT}
 - Output Ripple < 10mV_{P-P}
- Fast Minimum Switch On-Time: 40ns
- Low Dropout Under All Conditions: 60mV at 1A
- Adjustable and Synchronizable: 200kHz to 2.2MHz
- Peak Current Mode Operation
- Output Soft-Start and Tracking
- Small 32-Lead 6mm × 4mm LQFN Package
- AEC-Q100 Qualification In Progress

APPLICATIONS

- Automotive and Industrial Supplies
- General Purpose Step-Down
- GSM Power Supplies

DESCRIPTION

The LT®8645S-2 synchronous step-down regulator features Silent Switcher architecture designed to minimize EMI emissions while delivering high efficiency at high switching frequencies. This performance makes the LT8645S-2 ideal for noise sensitive applications and environments.

The fast, clean, low-overshoot switching edges enable high efficiency operation even at high switching frequencies, leading to a small overall solution size. Peak current mode control with a 40ns minimum on-time allows high step-down ratios even at high switching frequencies.

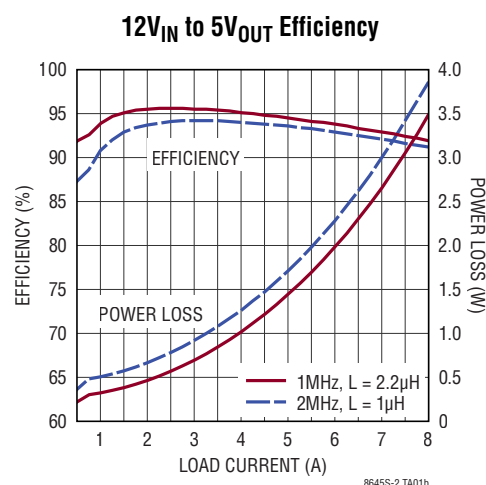
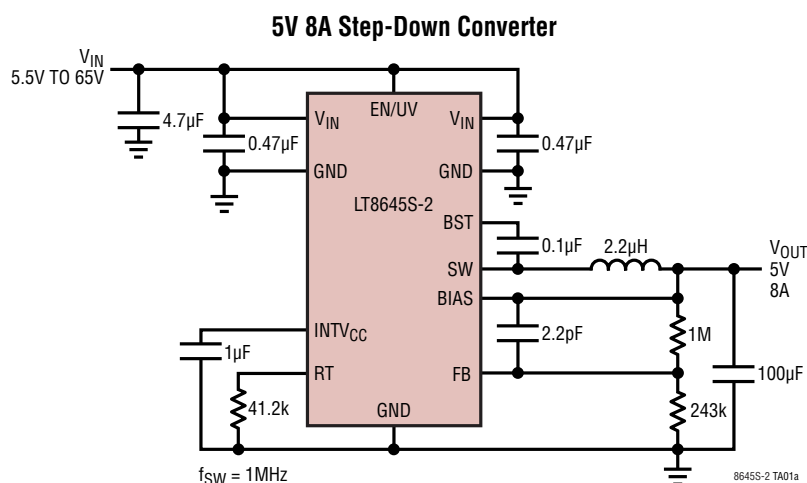
Burst Mode® operation enables ultralow standby current consumption, pulse-skipping mode allows full switching frequency at lower output loads, or spread spectrum operation can further reduce EMI emissions.

	INTERNAL CAPS	V _C COMP	150°C GRADE
LT8645S*	Yes	Internal	No
LT8646S*	Yes	External	No
LT8645S-2	No	Internal	Yes

*See LT8645S/LT8646S Datasheet

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TYPICAL APPLICATION



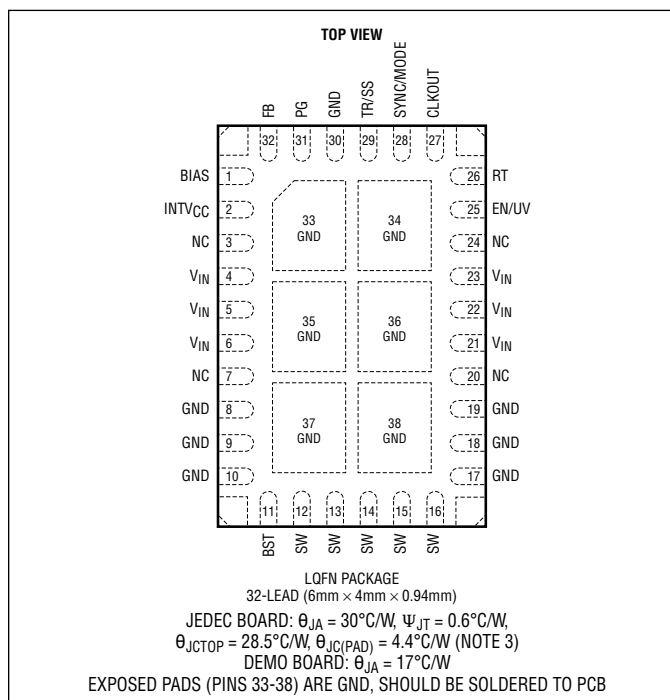
LT8645S-2

ABSOLUTE MAXIMUM RATINGS

(Note 1)

V _{IN} , EN/UV	65V
PG	42V
BIAS	25V
FB, TR/SS	4V
SYNC/MODE Voltage	6V
Operating Junction Temperature Range (Note 2)	
LT8645S-2E	−40°C to 125°C
LT8645S-2J	−40°C to 150°C
LT8645S-2H	−40°C to 150°C
Storage Temperature Range	−65°C to 150°C
Maximum Reflow (Package Body) Temperature ...	260°C

PIN CONFIGURATION



ORDER INFORMATION

PART NUMBER	PART MARKING*	FINISH CODE	PAD FINISH	PACKAGE TYPE**	MSL RATING	TEMPERATURE RANGE
LT8645SEV-2#PBF	86452	e4	Au (RoHS)	LQFN (Laminate Package with QFN Footprint)	3	-40°C to 125°C
LT8645SJV-2#PBF						-40°C to 150°C
LT8645SHV-2#PBF						

AUTOMOTIVE PRODUCTS***

LT8645SEV-2#WPBF	86452	e4	Au (RoHS)	LQFN (Laminate Package with QFN Footprint)	3	-40°C to 125°C
LT8645SJV-2#WPBF						-40°C to 150°C
LT8645SHV-2#WPBF						

• Contact the factory for parts specified with wider operating temperature ranges. *Pad or ball finish code is per IPC/JEDEC J-STD-609.

- [Recommended LGA and BGA PCB Assembly and Manufacturing Procedures](#)
- [LGA and BGA Package and Tray Drawings](#)

Parts ending with PBF are RoHS and WEEE compliant. **The LT8645S-2 package has the same footprint as a standard 6mm × 4mm QFN Package.

***Versions of this part are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. These models are designated with a #W suffix. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Minimum Input Voltage		●		3.0	3.4	V
V_{IN} Quiescent Current in Shutdown	$V_{EN/UV} = 0V$	●		0.9	3	μA
				0.9	20	μA
V_{IN} Quiescent Current in Sleep	$V_{EN/UV} = 2V$, $V_{FB} > 0.97V$, $V_{SYNC} = 0V$	●		1.7	4	μA
				1.7	20	μA
V_{IN} Current in Regulation	$V_{OUT} = 0.97V$, $V_{IN} = 6V$, $I_{LOAD} = 1mA$, $V_{SYNC} = 0V$	●		200	500	μA
Feedback Reference Voltage	$V_{IN} = 6V$	●	0.964	0.970	0.976	V
	$V_{IN} = 6V$	●	0.956	0.970	0.982	V
Feedback Voltage Line Regulation	$V_{IN} = 4.0V$ to $42V$	●		0.004	0.025	%/V
Feedback Pin Input Current	$V_{FB} = 1V$		-20		20	nA
BIAS Pin Current Consumption	$V_{BIAS} = 3.3V$, $f_{SW} = 2MHz$			22		mA
Minimum On-Time	$I_{LOAD} = 2.5A$, $SYNC = 0V$	●		40	65	ns
	$I_{LOAD} = 2.5A$, $SYNC = 2V$	●		35	60	ns
Minimum Off-Time				80	110	ns
Oscillator Frequency	$R_T = 221k$	●	180	210	240	kHz
	$R_T = 60.4k$	●	665	700	735	kHz
	$R_T = 18.2k$	●	1.8	1.95	2.1	MHz
Top Power NMOS On-Resistance	$I_{SW} = 1A$			36		m Ω
Top Power NMOS Current Limit		●	10.5	14	17.5	A
Bottom Power NMOS On-Resistance	$V_{INTVCC} = 3.4V$, $I_{SW} = 1A$			25		m Ω
Bottom Power NMOS Current Limit	$V_{INTVCC} = 3.4V$		8.5	11	14	A
SW Leakage Current	$V_{IN} = 42V$, $V_{SW} = 0V$, $42V$		-1.5		1.5	μA
EN/UV Pin Threshold	EN/UV Rising	●	0.95	1.01	1.07	V
EN/UV Pin Hysteresis				45		mV
EN/UV Pin Current	$V_{EN/UV} = 2V$		-20		20	nA
PG Upper Threshold Offset from V_{FB}	V_{FB} Falling	●	5	7.5	10	%
PG Lower Threshold Offset from V_{FB}	V_{FB} Rising	●	-10.5	-8	-5.5	%
PG Hysteresis				0.4		%
PG Leakage	$V_{PG} = 3.3V$		-40		40	nA
PG Pull-Down Resistance	$V_{PG} = 0.1V$	●		750	2000	Ω
SYNC/MODE Threshold	SYNC/MODE DC and Clock Low Level Voltage	●	0.7	0.9		V
	SYNC/MODE Clock High Level Voltage	●		1.2	1.4	V
	SYNC/MODE DC High Level Voltage	●	2.2	2.55	2.9	V
Spread Spectrum Modulation Frequency Range	$R_T = 60.4k$, $V_{SYNC} = 3.3V$			24		%
Spread Spectrum Modulation Frequency	$V_{SYNC} = 3.3V$			2.5		kHz
TR/SS Source Current		●	1.2	2	2.8	μA
TR/SS Pull-Down Resistance	Fault Condition, $TR/SS = 0.1V$			220		Ω

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$.

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LT8645S-2E is guaranteed to meet performance specifications from 0°C to 125°C junction temperature. Specifications over the -40°C to 125°C operating junction temperature range are assured by design, characterization, and correlation with statistical process controls. The LT8645S-2J and LT8645-2H are guaranteed over the full -40°C to 150°C operating junction temperature range. High junction temperatures degrade operating lifetimes. Operating lifetime is derated at junction temperatures greater than 125°C .

The junction temperature (T_J , in $^\circ\text{C}$) is calculated from the ambient temperature (T_A in $^\circ\text{C}$) and power dissipation (PD, in Watts) according to the formula:

$$T_J = T_A + (PD \cdot \theta_{JA})$$

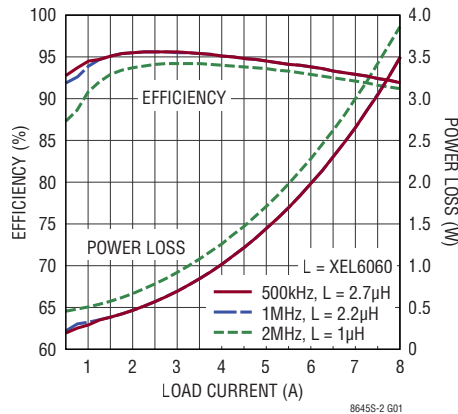
where θ_{JA} (in $^\circ\text{C}/\text{W}$) is the package thermal impedance.

Note 3: θ values determined per JEDEC 51-7, 51-12. See Applications Information Section for information on improving the thermal resistance and for actual temperature measurements of a demo board in typical operating conditions.

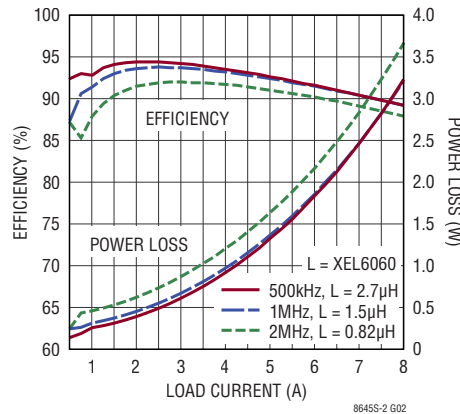
Note 4: This IC includes overtemperature protection that is intended to protect the device during overload conditions. Junction temperature will exceed 150°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature will reduce lifetime.

TYPICAL PERFORMANCE CHARACTERISTICS

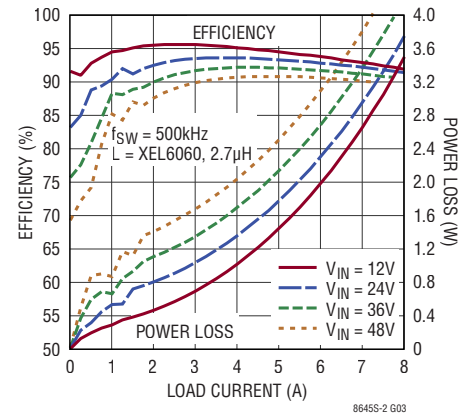
12V_{IN} to 5V_{OUT} Efficiency vs Frequency



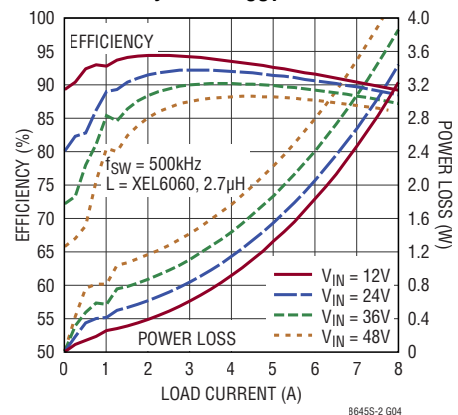
12V_{IN} to 3.3V_{OUT} Efficiency vs Frequency



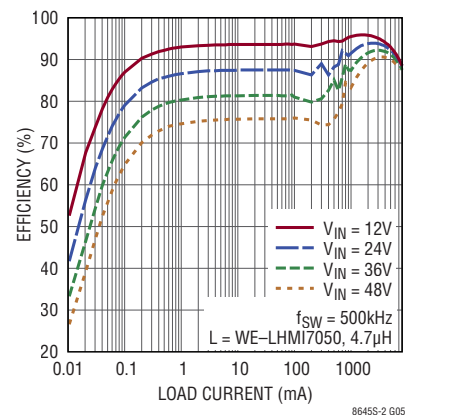
Efficiency at 5V_{OUT}



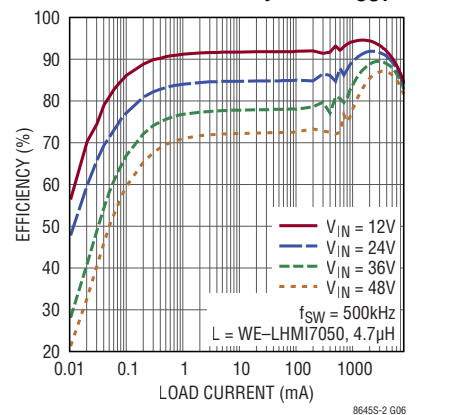
Efficiency at 3.3V_{OUT}



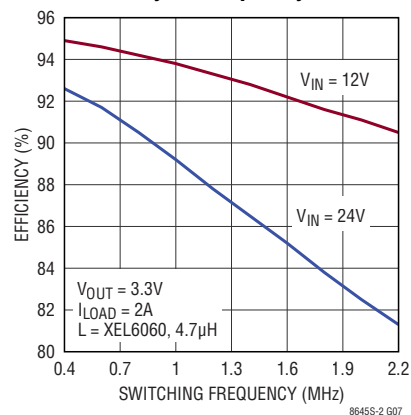
Low Load Efficiency at 5V_{OUT}



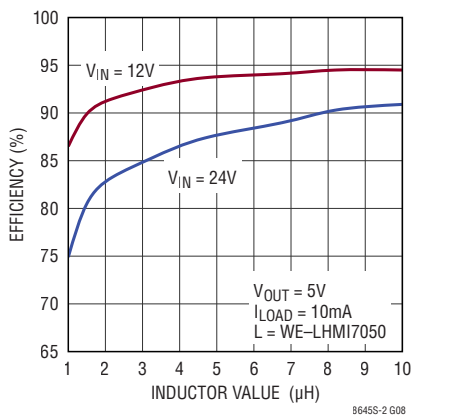
Low Load Efficiency at 3.3V_{OUT}



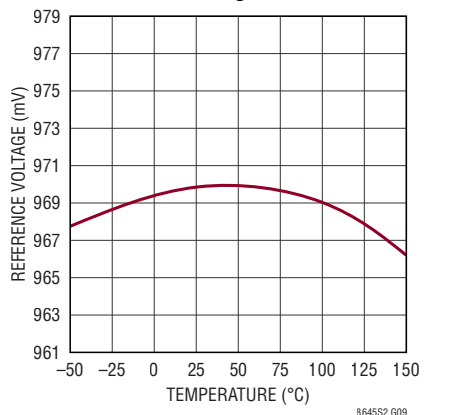
Efficiency vs Frequency



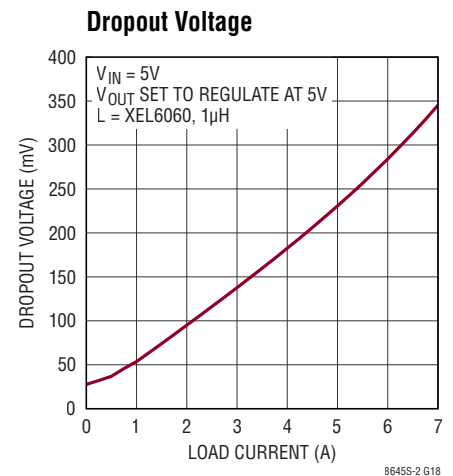
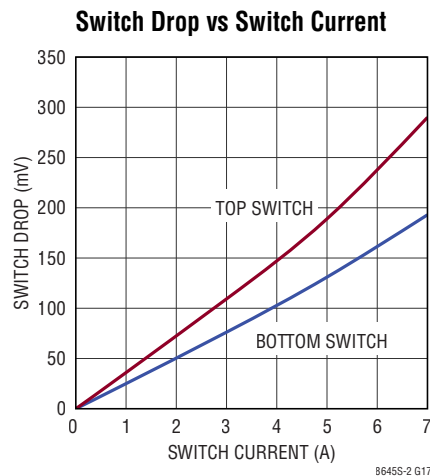
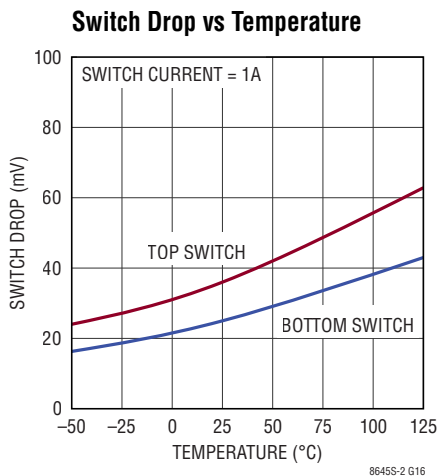
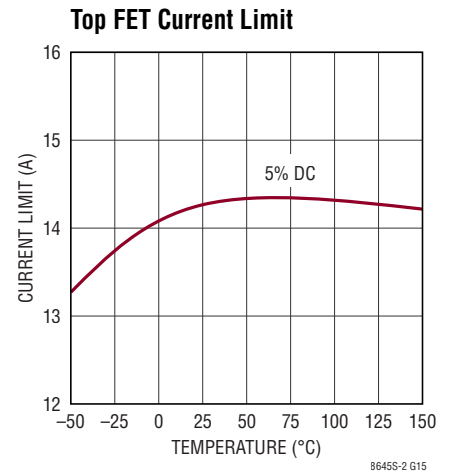
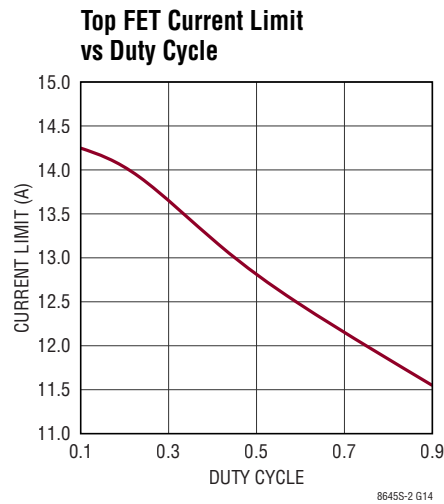
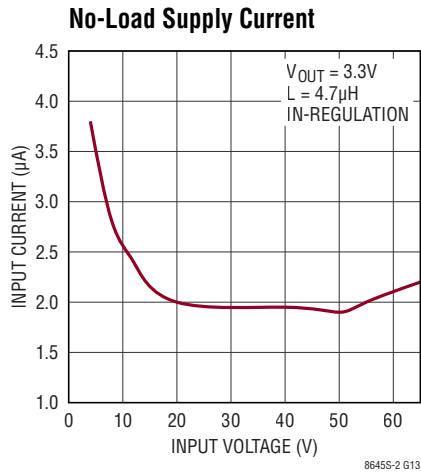
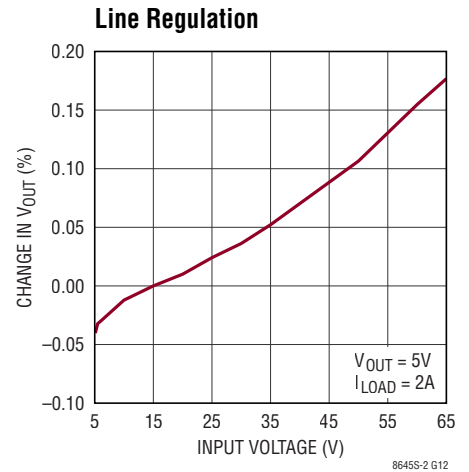
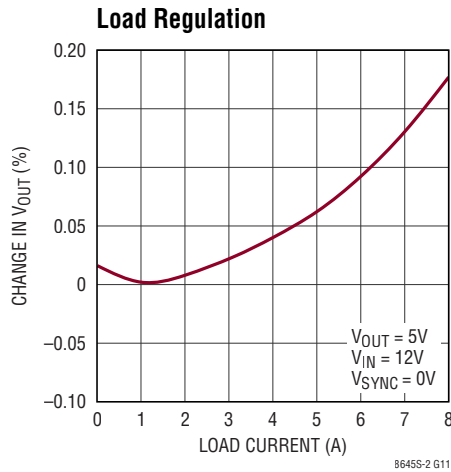
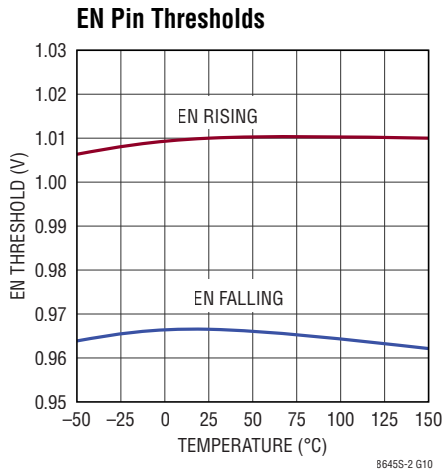
Burst Mode Operation Efficiency vs Inductor Value



Reference Voltage

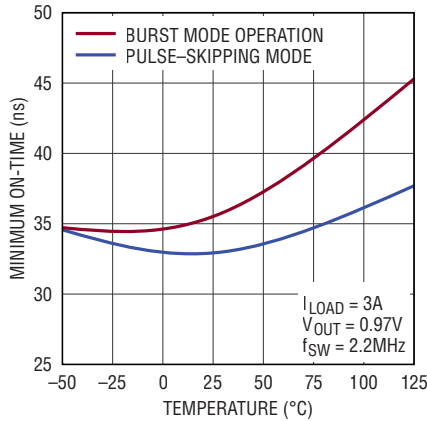


TYPICAL PERFORMANCE CHARACTERISTICS

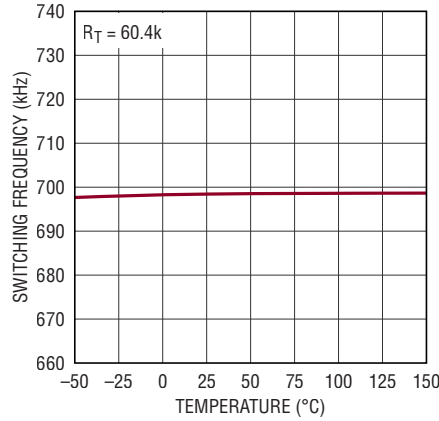


TYPICAL PERFORMANCE CHARACTERISTICS

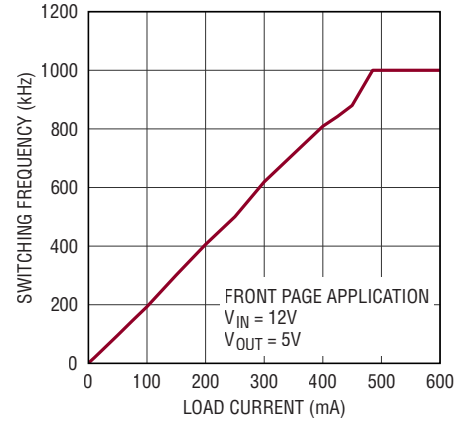
Minimum On-Time



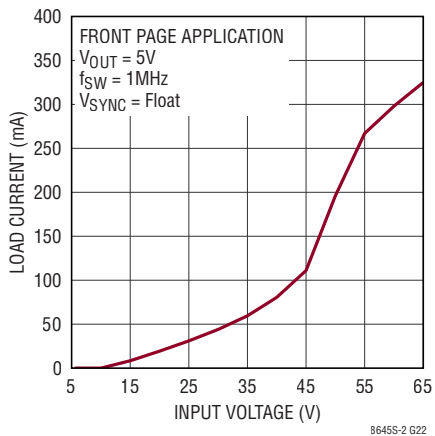
Switching Frequency



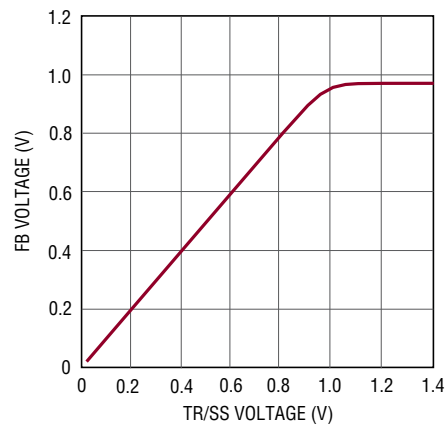
Burst Frequency



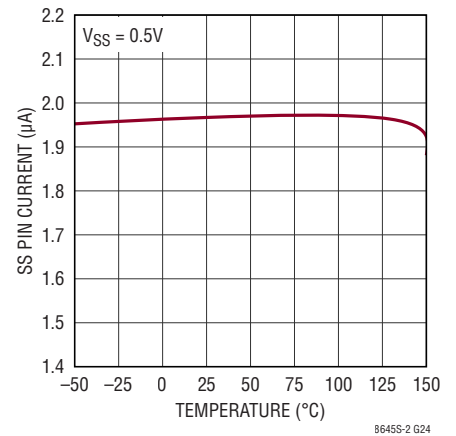
Minimum Load to Full Frequency (Pulse-Skipping Mode)



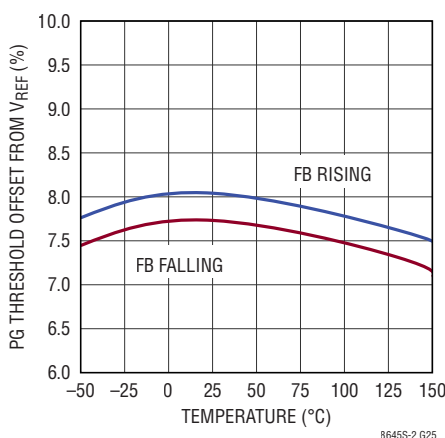
Soft-Start Tracking



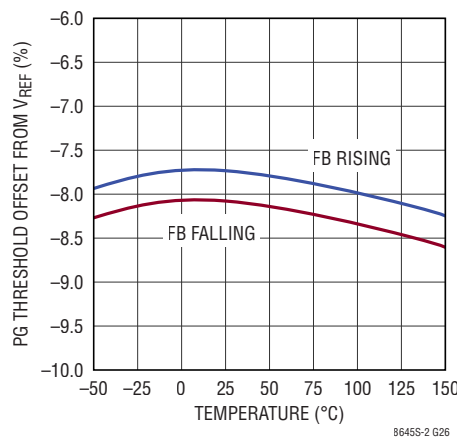
Soft-Start Current



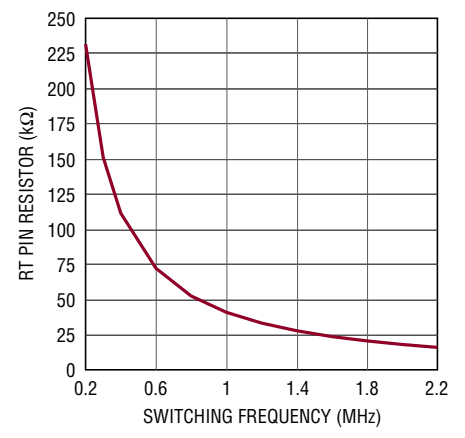
PG High Thresholds



PG Low Thresholds

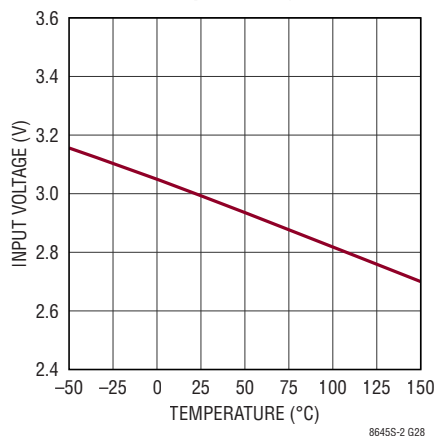


RT Programmed Switching Frequency

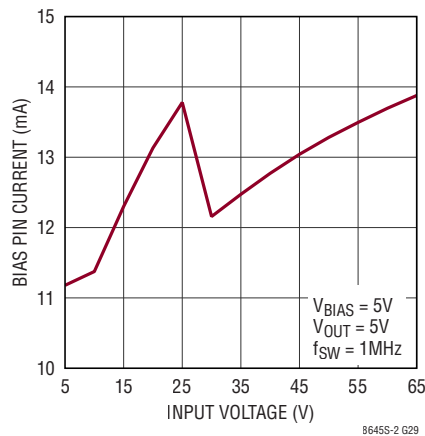


TYPICAL PERFORMANCE CHARACTERISTICS

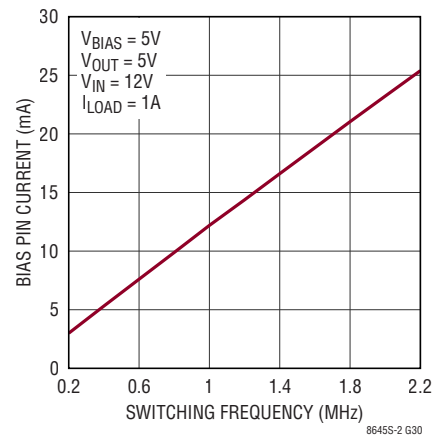
Minimum Input Voltage



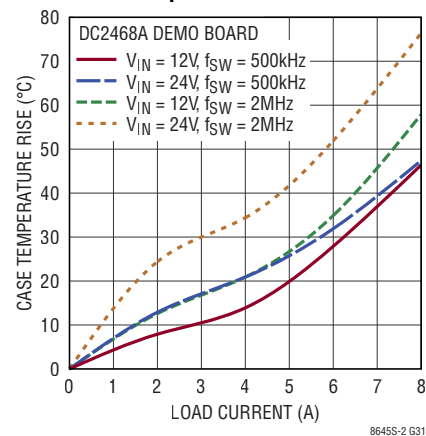
Bias Pin Current



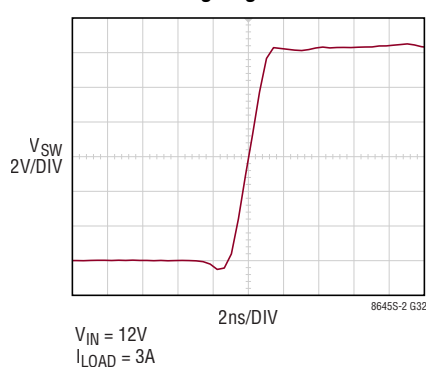
Bias Pin Current



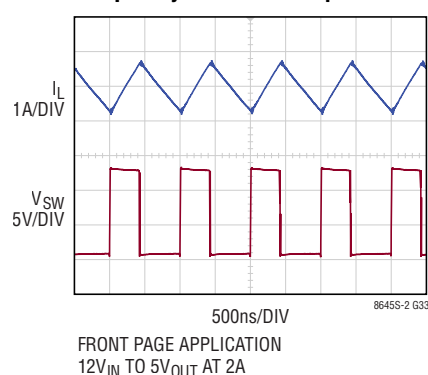
Case Temperature Rise



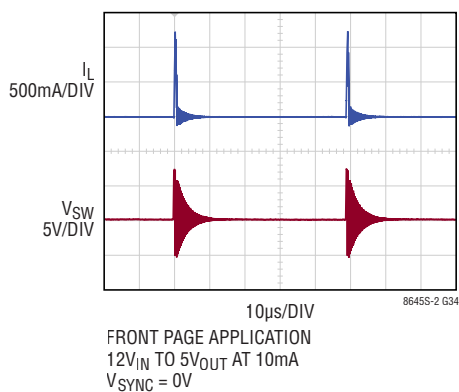
Switch Rising Edge



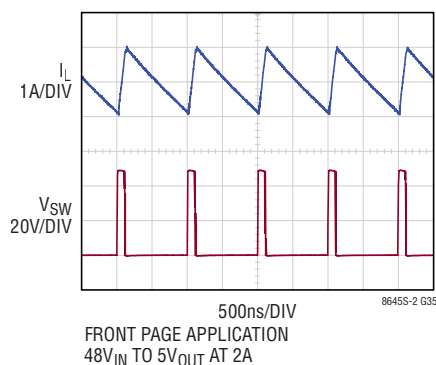
Switching Waveforms, Full Frequency Continuous Operation



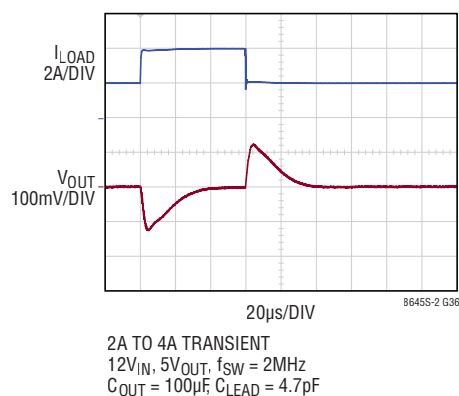
Switching Waveforms, Burst Mode Operation



Switching Waveforms

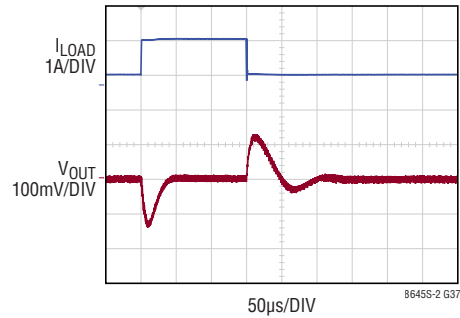


Transient Response; Internal Compensation



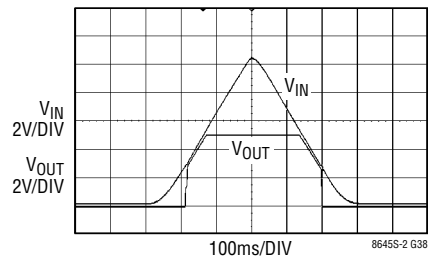
TYPICAL PERFORMANCE CHARACTERISTICS

**Transient Response; 300mA
(Burst Mode Operation) to 1.3A
Transient**



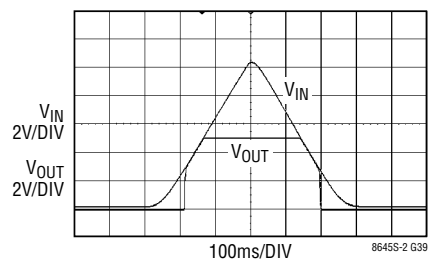
300mA TO 1.3A TRANSIENT
12V_{IN}, 5V_{OUT}, f_{SW} = 2MHz
C_{OUT} = 100µF, C_{LEAD} = 4.7pF

Start-Up Dropout Performance



2.5Ω LOAD
(2A IN REGULATION)

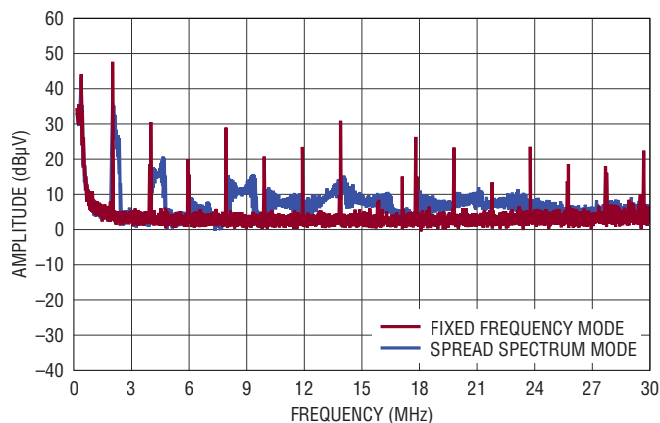
Start-Up Dropout Performance



20Ω LOAD
(250mA IN REGULATION)

TYPICAL PERFORMANCE CHARACTERISTICS

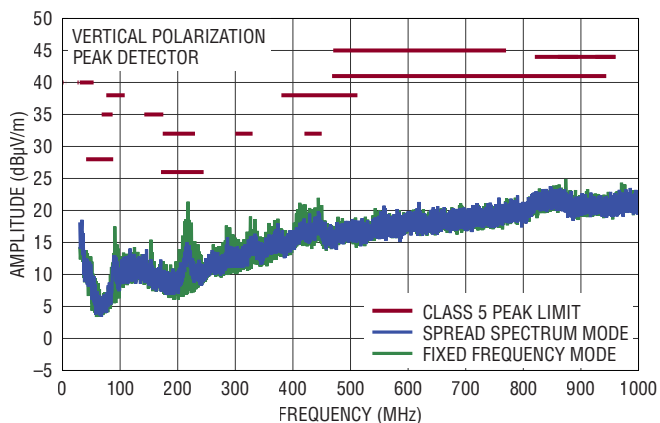
Conducted EMI Performance



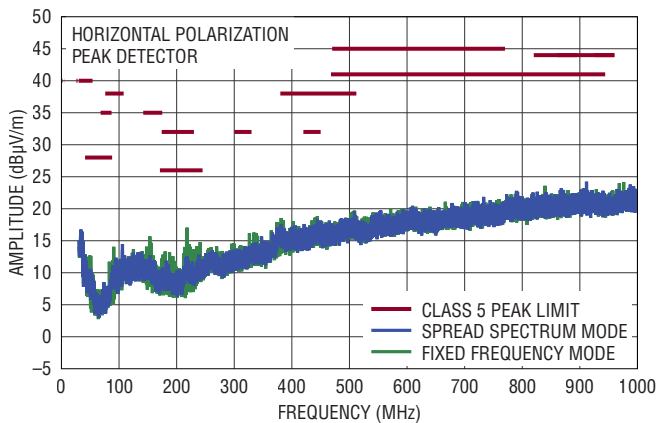
DC2468A DEMO BOARD USING LT8645S
(WITH EMI FILTER INSTALLED)
14V INPUT TO 5V OUTPUT AT 4A, $f_{SW} = 2\text{MHz}$

8645S-2 G40

Radiated EMI Performance (CISPR25 Radiated Emission Test with Class 5 Peak Limits)



8645S-2 G41



8645S-2 G42

DC2468A DEMO BOARD USING LT8645S
(WITH EMI FILTER INSTALLED)
14V INPUT TO 5V OUTPUT AT 4A, $f_{SW} = 2\text{MHz}$

PIN FUNCTIONS

BIAS (Pin 1): The internal regulator will draw current from BIAS instead of V_{IN} when BIAS is tied to a voltage higher than 3.1V. For output voltages of 3.3V to 25V this pin should be tied to V_{OUT} . If this pin is tied to a supply other than V_{OUT} use a 1 μ F local bypass capacitor on this pin. If no supply is available, tie to GND. However, especially for high input or high frequency applications, BIAS should be tied to output or an external supply of 3.3V or above.

INTV_{CC} (Pin 2): Internal 3.4V Regulator Bypass Pin. The internal power drivers and control circuits are powered from this voltage. INTV_{CC} maximum output current is 25mA. Do not load the INTV_{CC} pin with external circuitry. INTV_{CC} current will be supplied from BIAS if BIAS > 3.1V, otherwise current will be drawn from V_{IN} . Voltage on INTV_{CC} will vary between 2.8V and 3.4V when BIAS is between 3.0V and 3.6V. Place a low ESR ceramic capacitor of at least 1 μ F from this pin to ground close to the IC.

NC (Pins 3, 7, 20, 24): No Connect. This pin is not connected to internal circuitry and can be tied anywhere on the PCB, typically ground.

V_{IN} (Pins 4, 5, 6, 21, 22, 23): The V_{IN} pins supply current to the LT8645S-2 internal circuitry and to the internal topside power switch. The LT8645S-2 requires the use of multiple V_{IN} bypass capacitors. Two small 0.47 μ F capacitors should be placed as close as possible to the LT8645S-2, one capacitor on each side of the device (C_{IN1} , C_{IN2}). A third capacitor with a large value, 4.7 μ F or higher, should be placed near C_{IN1} or C_{IN2} . See the Applications Information section for a sample layout.

GND (Pins 8, 9, 10, 17, 18, 19, Exposed Pad Pins 33–38): Ground. Place the negative terminal of the input capacitor as close to the GND pins as possible. See the Applications Information section for a sample layout. The exposed pads should be soldered to the PCB for good thermal performance. If necessary due to manufacturing limitations Pins 33 to 38 may be left disconnected, however thermal performance will be degraded.

BST (Pin 11): This pin is used to provide a drive voltage, higher than the input voltage, to the topside power switch. Place a 0.1 μ F boost capacitor as close as possible to the IC.

SW (Pins 12, 13, 14, 15, 16): The SW pins are the outputs of the internal power switches. Tie these pins together and connect them to the inductor and boost capacitor. This node should be kept small on the PCB for good performance and low EMI.

EN/UV (Pin 25): The LT8645S-2 is shut down when this pin is low and active when this pin is high. The hysteretic threshold voltage is 1.01V going up and 0.965V going down. Tie to V_{IN} if the shutdown feature is not used. An external resistor divider from V_{IN} can be used to program a V_{IN} threshold below which the LT8645S-2 will shut down.

RT (Pin 26): A resistor is tied between RT and ground to set the switching frequency.

CLKOUT (Pin 27): In pulse-skipping mode, spread spectrum, and synchronization modes, the CLKOUT pin will provide a ~200ns wide pulse at the switch frequency. The low and high levels of the CLKOUT pin are ground and INTV_{CC} respectively, and the drive strength of the CLKOUT pin is several hundred ohms. In Burst Mode operation, the CLKOUT pin will be low. Float this pin if the CLKOUT function is not used.

SYNC/MODE (Pin 28): This pin programs four different operating modes: 1) Burst Mode. Tie this pin to ground for Burst Mode operation at low output loads—this will result in ultralow quiescent current. 2) Pulse-skipping mode. This mode offers full frequency operation down to low output loads before pulse skipping occurs. Float this pin for pulse-skipping mode. When floating, pin leakage currents should be <1 μ A. 3) Spread spectrum mode. Tie this pin high to INTV_{CC} (~3.4V) or an external supply of 3V to 4V for pulse-skipping mode with spread spectrum modulation. 4) Synchronization mode. Drive this pin with a clock source to synchronize to an external frequency. During synchronization the part will operate in pulse-skipping mode.

PIN FUNCTIONS

TR/SS (Pin 29): Output Tracking and Soft-Start Pin. This pin allows user control of output voltage ramp rate during start-up. A TR/SS voltage below 0.97V forces it to regulate the FB pin to equal the TR/SS pin voltage. When TR/SS is above 0.97V, the tracking function is disabled and the internal reference resumes control of the error amplifier. An internal 2 μ A pull-up current from INTV_{CC} on this pin allows a capacitor to program output voltage slew rate. This pin is pulled to ground with an internal 200 Ω MOSFET during shutdown and fault conditions; use a series resistor if driving from a low impedance output. This pin may be left floating if the tracking function is not needed.

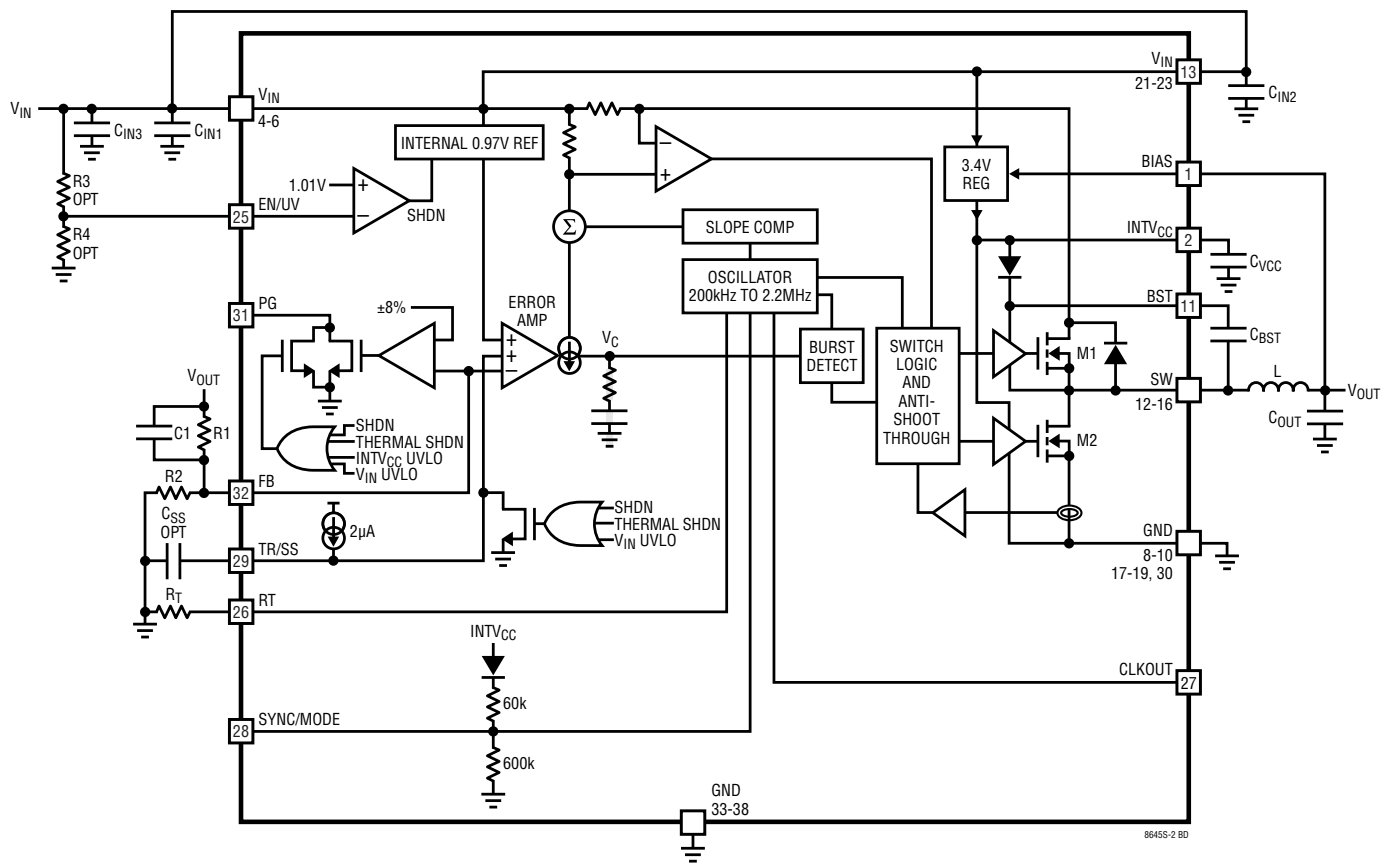
GND (Pin 30): Ground. Connect this pin to system ground and to the ground plane.

PG (Pin 31): The PG pin is the open-drain output of an internal comparator. PG remains low until the FB pin is within $\pm 8\%$ of the final regulation voltage, and there are no fault conditions. PG is pulled low when EN/UV is below 1V, INTV_{CC} has fallen too low, V_{IN} is too low, or thermal shutdown. PG is valid when V_{IN} is above 3.4V.

FB (Pin 32): The LT8645S-2 regulates the FB pin to 0.97V. Connect the feedback resistor divider tap to this pin. Also, connect a phase lead capacitor between FB and V_{OUT}. Typically, this capacitor is 1pF to 10pF.

Corner Pins: These pins are for mechanical support only and can be tied anywhere on the PCB, typically ground.

BLOCK DIAGRAM



OPERATION

The LT8645S-2 is a monolithic, constant frequency, current mode step-down DC/DC converter. An oscillator, with frequency set using a resistor on the RT pin, turns on the internal top power switch at the beginning of each clock cycle. Current in the inductor then increases until the top switch current comparator trips and turns off the top power switch. The peak inductor current at which the top switch turns off is controlled by the voltage on the internal VC node. The error amplifier servos the VC node by comparing the voltage on the V_{FB} pin with an internal 0.97V reference. When the load current increases it causes a reduction in the feedback voltage relative to the reference leading the error amplifier to raise the VC voltage until the average inductor current matches the new load current. When the top power switch turns off, the synchronous power switch turns on until the next clock cycle begins or inductor current falls to zero. If overload conditions result in more than 11A flowing through the bottom switch, the next clock cycle will be delayed until switch current returns to a safe level.

If the EN/UV pin is low, the LT8645S-2 is shut down and draws approximately 1μA from the input. When the EN/UV pin is above 1.01V, the switching regulator will become active.

To optimize efficiency at light loads, the LT8645S-2 operates in Burst Mode operation in light load situations. Between bursts, all circuitry associated with controlling the output switch is shut down, reducing the input supply current to 1.7μA. In a typical application, 2.5μA will be consumed from the input supply when regulating with no load. The SYNC/MODE pin is tied low to use Burst Mode operation and can be floated to use pulse-skipping mode. If a clock is applied to the SYNC/MODE pin, the part will synchronize to an external clock frequency and operate in pulse-skipping

mode. While in pulse-skipping mode the oscillator operates continuously and positive SW transitions are aligned to the clock. During light loads, switch pulses are skipped to regulate the output and the quiescent current will be several hundred μA.

To improve EMI, the LT8645S-2 can operate in spread spectrum mode. This feature varies the clock with a triangular frequency modulation of +20%. For example, if the LT8645S-2's frequency is programmed to switch at 2MHz, spread spectrum mode will modulate the oscillator between 2MHz and 2.4MHz. The SYNC/MODE pin should be tied high to INTV_{CC} (~3.4V) or an external supply of 3V to 4V to enable spread spectrum modulation with pulse-skipping mode.

To improve efficiency across all loads, supply current to internal circuitry can be sourced from the BIAS pin when biased at 3.3V or above. Else, the internal circuitry will draw current from V_{IN}. The BIAS pin should be connected to V_{OUT} if the LT8645S-2 output is programmed at 3.3V to 25V.

Comparators monitoring the FB pin voltage will pull the PG pin low if the output voltage varies more than ±8% (typical) from the set point, or if a fault condition is present.

The oscillator reduces the LT8645S-2's operating frequency when the voltage at the FB pin is low. This frequency foldback helps to control the inductor current when the output voltage is lower than the programmed value which occurs during start-up or overcurrent conditions. When a clock is applied to the SYNC/MODE pin, the SYNC/MODE pin is floated, or held DC high, the frequency foldback is disabled and the switching frequency will slow down only during overcurrent conditions.

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Low EMI PCB Layout

The LT8645S-2 is specifically designed to minimize EMI emissions and also to maximize efficiency when switching at high frequencies. For optimal performance the LT8645S-2 requires the use of multiple V_{IN} bypass capacitors.

Two small 0.47 μ F capacitors should be placed as close as possible to the LT8645S-2: One capacitor on each side of the device (C_{IN1} , C_{IN2}). A third capacitor with a larger value, 4.7 μ F or higher, should be placed near C_{IN1} or C_{IN2} .

See Figure 1 for a recommended PCB layout.

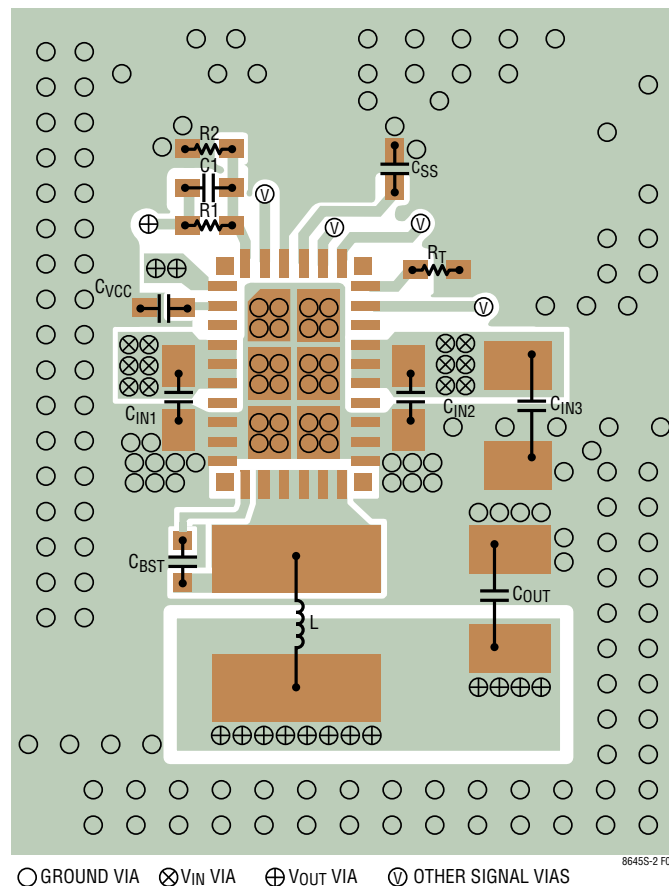


Figure 1. Recommended PCB Layout for the LT8645S-2

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For more detail and PCB design files refer to the Demo Board guide for the LT8645S.

Note that large, switched currents flow in the LT8645S-2 V_{IN} and GND pins and the input capacitors. The loops formed by the input capacitors should be as small as possible by placing the capacitors adjacent to the V_{IN} and GND pins. Capacitors with small case size such as 0603 or 0805 are optimal due to lowest parasitic inductance.

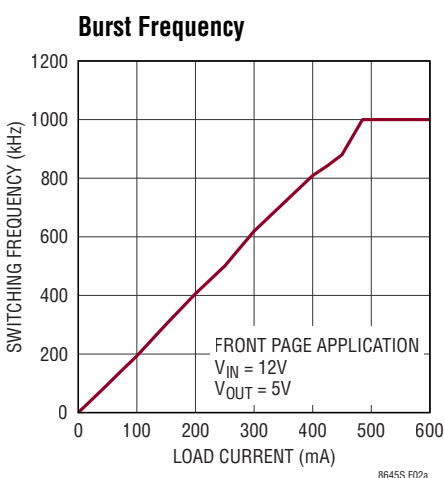
The input capacitors, along with the inductor and output capacitors, should be placed on the same side of the circuit board, and their connections should be made on that layer. Place a local, unbroken ground plane under the application circuit on the layer closest to the surface layer. The SW and BOOST nodes should be as small as possible. Finally, keep the FB and RT nodes small so that the ground traces will shield them from the SW and BOOST nodes.

The exposed pads on the bottom of the package should be soldered to the PCB to reduce thermal resistance to ambient. To keep thermal resistance low, extend the ground plane from the GND pins as much as possible, and add thermal vias to additional ground planes within the circuit board and on the bottom side.

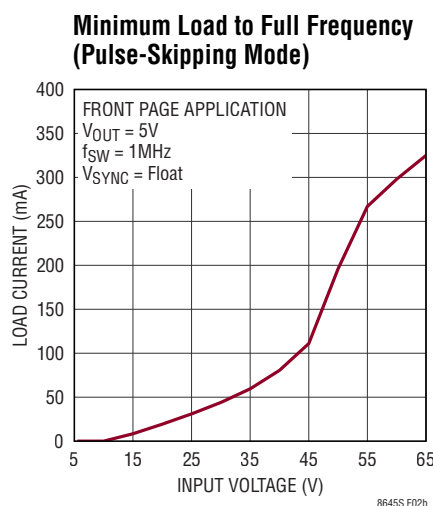
Burst Mode Operation

To enhance efficiency at light loads, the LT8645S-2 operates in low ripple Burst Mode operation, which keeps the output capacitor charged to the desired output voltage while minimizing the input quiescent current and minimizing output voltage ripple. In Burst Mode operation the LT8645S-2 delivers single small pulses of current to the output capacitor followed by sleep periods where the output power is supplied by the output capacitor. While in sleep mode the LT8645S-2 consumes $1.7\mu A$.

As the output load decreases, the frequency of single current pulses decreases (see Figure 2a) and the percentage of time the LT8645S-2 is in sleep mode increases, resulting in much higher light load efficiency than for typical converters. By maximizing the time between pulses, the LT8645S-2's quiescent current approaches $2.5\mu A$ for a typical application when there is no output load. Therefore, to optimize the quiescent current performance at light loads, the current in the feedback resistor divider must be minimized as it appears to the output as load current.



(2a)



(2b)

Figure 2. SW Frequency vs Load Information in Burst Mode Operation (2a) and Pulse-Skipping Mode (2b)

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In order to achieve higher light load efficiency, more energy must be delivered to the output during the single small pulses in Burst Mode operation such that the LT8645S-2 can stay in sleep mode longer between each pulse. This can be achieved by using a larger value inductor (i.e., 4.7 μ H), and should be considered independent of switching frequency when choosing an inductor. For example, while a lower inductor value would typically be used for a high switching frequency application, if high light load efficiency is desired, a higher inductor value should be chosen. See curve in Typical Performance Characteristics.

While in Burst Mode operation the current limit of the top switch is approximately 1.25A (as shown in Figure 3), resulting in low output voltage ripple. Increasing the output capacitance will decrease output ripple proportionally. As load ramps upward from zero the switching frequency will increase but only up to the switching frequency programmed by the resistor at the RT pin as shown in Figure 2a.

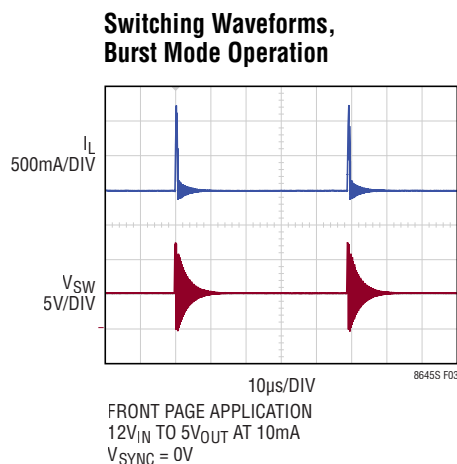


Figure 3. Burst Mode Operation

The output load at which the LT8645S-2 reaches the programmed frequency varies based on input voltage, output voltage, and inductor choice. To select low ripple Burst Mode operation, tie the SYNC/MODE pin below 0.4V (this can be ground or a logic low output).

Pulse-Skipping Mode

For some applications it is desirable for the LT8645S-2 to operate in pulse-skipping mode, offering two major differences from Burst Mode operation. First is the clock stays awake at all times and all switching cycles are aligned to the clock. In this mode much of the internal circuitry is awake at all times, increasing quiescent current to several hundred μ A. Second is that full switching frequency is reached at lower output load than in Burst Mode operation (see Figure 2b). To enable pulse-skipping mode, float the SYNC/MODE pin. Leakage current in this pin should be <1 μ A. See Block Diagram for internal pull-up and pull-down resistance.

Spread Spectrum Mode

The LT8645S-2 features spread spectrum operation to further reduce EMI emissions. To enable spread spectrum operation, the SYNC/MODE pin should be tied high to INTV_{CC} (~3.4V) or an external supply of 3V to 4V. In this mode, triangular frequency modulation is used to vary the switching frequency between the value programmed by RT to approximately 20% higher than that value. The modulation frequency is approximately 3kHz. For example, when the LT8645S-2 is programmed to 2MHz, the frequency will vary from 2MHz to 2.4MHz at a 3kHz rate. When spread

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spectrum operation is selected, Burst Mode operation is disabled, and the part will run in pulse-skipping mode.

Synchronization

To synchronize the LT8645S-2 oscillator to an external frequency, connect a square wave to the SYNC/MODE pin. The square wave amplitude should have valleys that are below 0.4V and peaks above 1.5V (up to 6V), with a minimum on-time and off-time of 50ns.

The LT8645S-2 will not enter Burst Mode operation at low output loads while synchronized to an external clock, but instead will pulse-skip to maintain regulation. The LT8645S-2 may be synchronized over a 200kHz to 2.2MHz range. The RT resistor should be chosen to set the LT8645S-2 switching frequency equal to or below the lowest synchronization input. For example, if the synchronization signal will be 500kHz and higher, the RT should be selected for 500kHz. The slope compensation is set by the RT value, while the minimum slope compensation required to avoid subharmonic oscillations is established by the inductor size, input voltage, and output voltage. Since the synchronization frequency will not change the slopes of the inductor current waveform, if the inductor is large enough to avoid subharmonic oscillations at the frequency set by RT, then the slope compensation will be sufficient for all synchronization frequencies.

The LT8645S-2 does not operate in forced continuous mode regardless of SYNC/MODE signal.

FB Resistor Network

The output voltage is programmed with a resistor divider between the output and the FB pin. Choose the resistor values according to:

$$R1 = R2 \left(\frac{V_{OUT}}{0.97V} - 1 \right) \quad (1)$$

Reference designators refer to the Block Diagram. 1% resistors are recommended to maintain output voltage accuracy.

For the LT8645S-2, if low input quiescent current and good light-load efficiency are desired, use large resistor values for the FB resistor divider. The current flowing in the divider acts as a load current, and will increase the no-load input current to the converter, which is approximately:

$$I_Q = 1.7\mu A + \left(\frac{V_{OUT}}{R1 + R2} \right) \left(\frac{V_{OUT}}{V_{IN}} \right) \left(\frac{1}{n} \right) \quad (2)$$

where 1.7μA is the quiescent current of the LT8645S-2 and the second term is the current in the feedback divider reflected to the input of the buck operating at its light load efficiency n. For a 3.3V application with R1 = 1M and R2 = 412k, the feedback divider draws 2.3μA. With VIN = 12V and n = 80%, this adds 0.8μA to the 1.7μA quiescent current resulting in 2.5μA no-load current from the 12V supply. Note that this equation implies that the no-load current is a function of VIN; this is plotted in the Typical Performance Characteristics section.

When using large FB resistors, a 1pF to 10pF phase-lead capacitor should be connected from VOUT to FB.

Setting the Switching Frequency

The LT8645S-2 uses a constant frequency PWM architecture that can be programmed to switch from 200kHz to 2.2MHz by using a resistor tied from the RT pin to ground. A table showing the necessary RT value for a desired switching frequency is in Table 1.

The RT resistor required for a desired switching frequency can be calculated using:

$$R_T = \frac{46.5}{f_{SW}} - 5.2 \quad (3)$$

where RT is in kΩ and fSW is the desired switching frequency in MHz.

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Table 1. SW Frequency vs R_T Value

f _{SW} (MHz)	R _T (kΩ)
0.2	232
0.3	150
0.4	110
0.5	88.7
0.6	71.5
0.7	60.4
0.8	52.3
1.0	41.2
1.2	33.2
1.4	28.0
1.6	23.7
1.8	20.5
2.0	17.8
2.2	15.8

Operating Frequency Selection and Trade-Offs

Selection of the operating frequency is a trade-off between efficiency, component size, and input voltage range. The advantage of high frequency operation is that smaller inductor and capacitor values may be used. The disadvantages are lower efficiency and a smaller input voltage range.

The highest switching frequency (f_{SW(MAX)}) for a given application can be calculated as follows:

$$f_{SW(MAX)} = \frac{V_{OUT} + V_{SW(BOT)}}{t_{ON(MIN)}(V_{IN} - V_{SW(TOP)} + V_{SW(BOT)})} \quad (4)$$

where V_{IN} is the typical input voltage, V_{OUT} is the output voltage, V_{SW(TOP)} and V_{SW(BOT)} are the internal switch drops (~0.3V, ~0.2V, respectively at maximum load) and t_{ON(MIN)} is the minimum top switch on-time (see the Electrical Characteristics). This equation shows that a slower switching frequency is necessary to accommodate a high V_{IN}/V_{OUT} ratio.

For transient operation, V_{IN} may go as high as the absolute maximum rating of 65V regardless of the R_T value, however the LT8645S-2 will reduce switching frequency as necessary to maintain control of inductor current to assure safe operation.

The LT8645S-2 is capable of a maximum duty cycle of approximately 99%, and the V_{IN}-to-V_{OUT} dropout is limited by the R_{DS(ON)} of the top switch. In this mode the LT8645S-2 skips switch cycles, resulting in a lower switching frequency than programmed by R_T.

For applications that cannot allow deviation from the programmed switching frequency at low V_{IN}/V_{OUT} ratios use the following formula to set switching frequency:

$$V_{IN(MIN)} = \frac{V_{OUT} + V_{SW(BOT)}}{1 - f_{SW} \cdot t_{OFF(MIN)}} - V_{SW(BOT)} + V_{SW(TOP)} \quad (5)$$

where V_{IN(MIN)} is the minimum input voltage without skipped cycles, V_{OUT} is the output voltage, V_{SW(TOP)} and V_{SW(BOT)} are the internal switch drops (~0.3V, ~0.2V, respectively at maximum load), f_{SW} is the switching frequency (set by R_T), and t_{OFF(MIN)} is the minimum switch off-time. Note that higher switching frequency will increase the minimum input voltage below which cycles will be dropped to achieve higher duty cycle.

Inductor Selection and Maximum Output Current

The LT8645S-2 is designed to minimize solution size by allowing the inductor to be chosen based on the output load requirements of the application. During overload or short-circuit conditions the LT8645S-2 safely tolerates operation with a saturated inductor through the use of a high speed peak-current mode architecture.

A good first choice for the inductor value is:

$$L = \left(\frac{V_{OUT} + V_{SW(BOT)}}{f_{SW}} \right) \cdot 0.4 \quad (6)$$

where f_{SW} is the switching frequency in MHz, V_{OUT} is the output voltage, V_{SW(BOT)} is the bottom switch drop (~0.2V) and L is the inductor value in μH.

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To avoid overheating and poor efficiency, an inductor must be chosen with an RMS current rating that is greater than the maximum expected output load of the application. In addition, the saturation current (typically labeled I_{SAT}) rating of the inductor must be higher than the load current plus 1/2 of inductor ripple current:

$$I_{L(PEAK)} = I_{LOAD(MAX)} + \frac{1}{2} \Delta I_L \quad (7)$$

where ΔI_L is the inductor ripple current as calculated in Equation 9 and $I_{LOAD(MAX)}$ is the maximum output load for a given application.

As a quick example, an application requiring 2A output should use an inductor with an RMS rating of greater than 2A and an I_{SAT} of greater than 3A. During long duration overload or short-circuit conditions, the inductor RMS rating requirement is greater to avoid overheating of the inductor. To keep the efficiency high, the series resistance (DCR) should be less than 0.02Ω , and the core material should be intended for high frequency applications.

The LT8645S-2 limits the peak switch current in order to protect the switches and the system from overload faults. The top switch current limit (I_{LIM}) is 14A at low duty cycles and decreases linearly to 11.5A at $DC = 0.9$. The inductor value must then be sufficient to supply the desired maximum output current ($I_{OUT(MAX)}$), which is a function of the switch current limit (I_{LIM}) and the ripple current.

$$I_{OUT(MAX)} = I_{LIM} - \frac{\Delta I_L}{2} \quad (8)$$

The peak-to-peak ripple current in the inductor can be calculated as follows:

$$\Delta I_L = \frac{V_{OUT}}{L \cdot f_{SW}} \cdot \left(1 - \frac{V_{OUT}}{V_{IN(MAX)}} \right) \quad (9)$$

where f_{SW} is the switching frequency of the LT8645S-2, and L is the value of the inductor. Therefore, the maximum output current that the LT8645S-2 will deliver depends on the switch current limit, the inductor value, and the input and output voltages. The inductor value may have to be increased if the inductor ripple current does not allow sufficient maximum output current ($I_{OUT(MAX)}$) given the

switching frequency, and maximum input voltage used in the desired application.

When operating at high V_{IN} (greater than 40V) and at a frequency and duty cycle that would require a switch on-time of less than 100ns, choose an inductor such that the ΔI_L is greater than 1.5A in order to prevent duty cycle jitter.

In order to achieve higher light load efficiency, more energy must be delivered to the output during the single small pulses in Burst Mode operation such that the LT8645S-2 can stay in sleep mode longer between each pulse. This can be achieved by using a larger value inductor (i.e., 4.7μH), and should be considered independent of switching frequency when choosing an inductor. For example, while a lower inductor value would typically be used for a high switching frequency application, if high light load efficiency is desired, a higher inductor value should be chosen. See curve in Typical Performance Characteristics.

The optimum inductor for a given application may differ from the one indicated by this design guide. A larger value inductor provides a higher maximum load current and reduces the output voltage ripple. For applications requiring smaller load currents, the value of the inductor may be lower and the LT8645S-2 may operate with higher ripple current. This allows use of a physically smaller inductor, or one with a lower DCR resulting in higher efficiency. Be aware that low inductance may result in discontinuous mode operation, which further reduces maximum load current.

For more information about maximum output current and discontinuous operation, see Analog Devices' Application Note 44.

For duty cycles greater than 50% ($V_{OUT}/V_{IN} > 0.5$), a minimum inductance is required to avoid subharmonic oscillation (See Equation 10). See Application Note 19 for more details.

$$L_{MIN} = \frac{V_{IN}(2 \cdot DC - 1)}{3 \cdot f_{SW}} \quad (10)$$

where DC is the duty cycle ratio (V_{OUT}/V_{IN}) and f_{SW} is the switching frequency.

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Input Capacitors

The V_{IN} of the LT8645S-2 should be bypassed with at least three ceramic capacitors for best performance. Two small ceramic capacitors of $0.47\mu\text{F}$ should be placed close to the part; one on each side of the device (C_{IN1} , C_{IN2}). These capacitors should be 0603 or 0805 in size. For automotive applications requiring 2 series input capacitors, two small 0603 or 0805 may be placed at each side of the LT8645S-2.

A third, larger ceramic capacitor of $4.7\mu\text{F}$ or larger should be placed close to C_{IN1} or C_{IN2} . See layout section for more detail. X7R or X5R capacitors are recommended for best performance across temperature and input voltage variations.

Note that larger input capacitance is required when a lower switching frequency is used. If the input power source has high impedance, or there is significant inductance due to long wires or cables, additional bulk capacitance may be necessary. This can be provided with a low performance electrolytic capacitor.

A ceramic input capacitor combined with trace or cable inductance forms a high quality (under damped) tank circuit. If the LT8645S-2 circuit is plugged into a live supply, the input voltage can ring to twice its nominal value, possibly exceeding the LT8645S-2's voltage rating. This situation is easily avoided (see Analog Devices Application Note 88).

Output Capacitor and Output Ripple

The output capacitor has two essential functions. Along with the inductor, it filters the square wave generated by the LT8645S-2 to produce the DC output. In this role it determines the output ripple, thus low impedance at the switching frequency is important. The second function is to store energy in order to satisfy transient loads and stabilize the LT8645S-2's control loop. Ceramic capacitors have very low equivalent series resistance (ESR) and provide the best ripple performance. For good starting values, see the Typical Applications section.

Use X5R or X7R types. This choice will provide low output ripple and good transient response. Transient performance can be improved with a higher value output capacitor and

the addition of a feedforward capacitor placed between V_{OUT} and FB. Increasing the output capacitance will also decrease the output voltage ripple. A lower value of output capacitor can be used to save space and cost but transient performance will suffer and may cause loop instability. See the Typical Applications in this data sheet for suggested capacitor values.

When choosing a capacitor, special attention should be given to the data sheet to calculate the effective capacitance under the relevant operating conditions of voltage bias and temperature. A physically larger capacitor or one with a higher voltage rating may be required.

Ceramic Capacitors

Ceramic capacitors are small, robust and have very low ESR. However, ceramic capacitors can cause problems when used with the LT8645S-2 due to their piezoelectric nature. When in Burst Mode operation, the LT8645S-2's switching frequency depends on the load current, and at very light loads the LT8645S-2 can excite the ceramic capacitor at audio frequencies, generating audible noise. Since the LT8645S-2 operates at a lower current limit during Burst Mode operation, the noise is typically very quiet to a casual ear. If this is unacceptable, use a high performance tantalum or electrolytic capacitor at the output. Low noise ceramic capacitors are also available.

A final precaution regarding ceramic capacitors concerns the maximum input voltage rating of the LT8645S-2. As previously mentioned, a ceramic input capacitor combined with trace or cable inductance forms a high quality (under-damped) tank circuit. If the LT8645S-2 circuit is plugged into a live supply, the input voltage can ring to twice its nominal value, possibly exceeding the LT8645S-2's rating. This situation is easily avoided (see Analog Devices Application Note 88).

Enable Pin

The LT8645S-2 is in shutdown when the EN pin is low and active when the pin is high. The rising threshold of the EN comparator is 1.01V , with 45mV of hysteresis. The EN pin can be tied to V_{IN} if the shutdown feature is not used, or tied to a logic level if shutdown control is required.

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Adding a resistor divider from V_{IN} to EN programs the LT8645S-2 to regulate the output only when V_{IN} is above a desired voltage (see the Block Diagram). Typically, this threshold, $V_{IN(EN)}$, is used in situations where the input supply is current limited, or has a relatively high source resistance. A switching regulator draws constant power from the source, so source current increases as source voltage drops. This looks like a negative resistance load to the source and can cause the source to current limit or latch low under low source voltage conditions. The $V_{IN(EN)}$ threshold prevents the regulator from operating at source voltages where the problems might occur. This threshold can be adjusted by setting the values R3 and R4 such that they satisfy the following equation:

$$V_{IN(EN)} = \left(\frac{R3}{R4} + 1 \right) \cdot 1.01V \quad (11)$$

where the LT8645S-2 will remain off until V_{IN} is above $V_{IN(EN)}$. Due to the comparator's hysteresis, switching will not stop until the input falls slightly below $V_{IN(EN)}$.

When operating in Burst Mode operation for light load currents, the current through the $V_{IN(EN)}$ resistor network can easily be greater than the supply current consumed by the LT8645S-2. Therefore, the $V_{IN(EN)}$ resistors should be large to minimize their effect on efficiency at low loads.

INTV_{CC} Regulator

An internal low dropout (LDO) regulator produces the 3.4V supply from V_{IN} that powers the drivers and the internal bias circuitry and must be bypassed to ground with a minimum of 1μF ceramic capacitor. The INTV_{CC} can supply enough current for the LT8645S-2's circuitry. To improve efficiency the internal LDO can also draw current from the BIAS pin when the BIAS pin is at 3.1V or higher. Typically the BIAS pin can be tied to the output of the LT8645S-2, or can be tied to an external supply of 3.3V or above. If BIAS is connected to a supply other than V_{OUT} , be sure to bypass with a local ceramic capacitor. If the BIAS pin is below 3.0V, the internal LDO will consume current from V_{IN} . Applications with high input voltage and high switching

frequency where the internal LDO pulls current from V_{IN} will increase die temperature because of the higher power dissipation across the LDO. Do not connect an external load to the INTV_{CC} pin.

Output Voltage Tracking and Soft-Start

The LT8645S-2 allows the user to program its output voltage ramp rate by means of the TR/SS pin. An internal 2μA pulls up the TR/SS pin to INTV_{CC}. Putting an external capacitor on TR/SS enables soft starting the output to prevent current surge on the input supply. During the soft-start ramp the output voltage will proportionally track the TR/SS pin voltage.

For output tracking applications, TR/SS can be externally driven by another voltage source. From 0V to 0.97V, the TR/SS voltage will override the internal 0.97V reference input to the error amplifier, thus regulating the FB pin voltage to that of TR/SS pin. When TR/SS is above 0.97V, tracking is disabled and the feedback voltage will regulate to the internal reference voltage. The TR/SS pin may be left floating if the function is not needed.

An active pull-down circuit is connected to the TR/SS pin which will discharge the external soft-start capacitor in the case of fault conditions and restart the ramp when the faults are cleared. Fault conditions that clear the soft-start capacitor are the EN/UV pin transitioning low, V_{IN} voltage falling too low, or thermal shutdown.

Output Power Good

When the LT8645S-2's output voltage is within the ±8% window of the regulation point, the output voltage is considered good and the open-drain PG pin goes high impedance and is typically pulled high with an external resistor. Otherwise, the internal pull-down device will pull the PG pin low. To prevent glitching both the upper and lower thresholds include 0.4% of hysteresis. PG is valid when V_{IN} is above 3.4V

The PG pin is also actively pulled low during several fault conditions: EN/UV pin is below 1V, INTV_{CC} has fallen too low, V_{IN} is too low, or thermal shutdown.

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Shorted and Reversed Input Protection

The LT8645S-2 will tolerate a shorted output. Several features are used for protection during output short-circuit and brownout conditions. The first is the switching frequency will be folded back while the output is lower than the set point to maintain inductor current control. Second, the bottom switch current is monitored such that if inductor current is beyond safe levels switching of the top switch will be delayed until such time as the inductor current falls to safe levels.

Frequency foldback behavior depends on the state of the SYNC pin: If the SYNC pin is low the switching frequency will slow while the output voltage is lower than the programmed level. If the SYNC pin is connected to a clock source, floated, or tied high, the LT8645S-2 will stay at the programmed frequency without foldback and only slow switching if the inductor current exceeds safe levels.

There is another situation to consider in systems where the output will be held high when the input to the LT8645S-2 is absent. This may occur in battery charging applications or in battery-backup systems where a battery or some other supply is diode ORed with the LT8645S-2's output. If the

V_{IN} pin is allowed to float and the EN pin is held high (either by a logic signal or because it is tied to V_{IN}), then the LT8645S-2's internal circuitry will pull its quiescent current through its SW pin. This is acceptable if the system can tolerate several μA in this state. If the EN pin is grounded the SW pin current will drop to near $1\mu A$. However, if the V_{IN} pin is grounded while the output is held high, regardless of EN, parasitic body diodes inside the LT8645S-2 can pull current from the output through the SW pin and the V_{IN} pin. Figure 4 shows a connection of the V_{IN} and EN/UV pins that will allow the LT8645S-2 to run only when the input voltage is present and that protects against a shorted or reversed input.

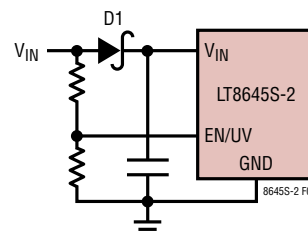


Figure 4. Reverse V_{IN} Protection

APPLICATIONS INFORMATION

Thermal Considerations

For higher ambient temperatures, care should be taken in the layout of the PCB to ensure good heat sinking of the LT8645S-2. The ground pins on the bottom of the package should be soldered to a ground plane. This ground should be tied to large copper layers below with thermal vias; these layers will spread heat dissipated by the LT8645S-2. Placing additional vias can reduce thermal resistance further. The maximum load current should be derated as the ambient temperature approaches the maximum junction rating. Power dissipation within the LT8645S-2 can be estimated by calculating the total power loss from an efficiency measurement and subtracting the inductor loss. The die temperature is calculated by multiplying the LT8645S-2 power dissipation by the thermal resistance from junction to ambient.

The internal overtemperature protection monitors the junction temperature of the LT8645S-2. If the junction temperature reaches approximately 180°C, the LT8645S-2 will stop switching and indicate a fault condition until the temperature drops about 10°C cooler.

Temperature rise of the LT8645S-2 is worst when operating at high load, high V_{IN} , and high switching frequency. If the case temperature is too high for a given application,

then either V_{IN} , switching frequency, or load current can be decreased to reduce the temperature to an acceptable level. Figure 5 shows examples of how case temperature rise can be managed by reducing V_{IN} , switching frequency, or load.

The LT8645S-2's top switch current limit decreases with higher duty cycle operation for slope compensation. This also limits the output current the LT8645S-2 can deliver for a given application. See curve in the Typical Performance Characteristics section.

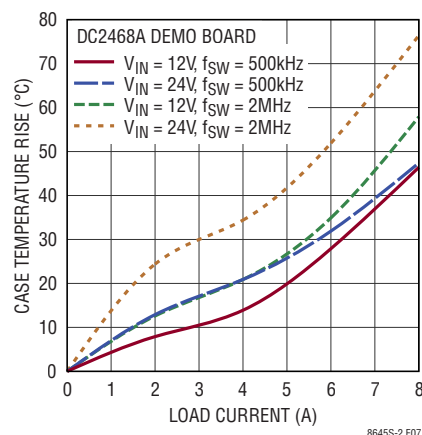
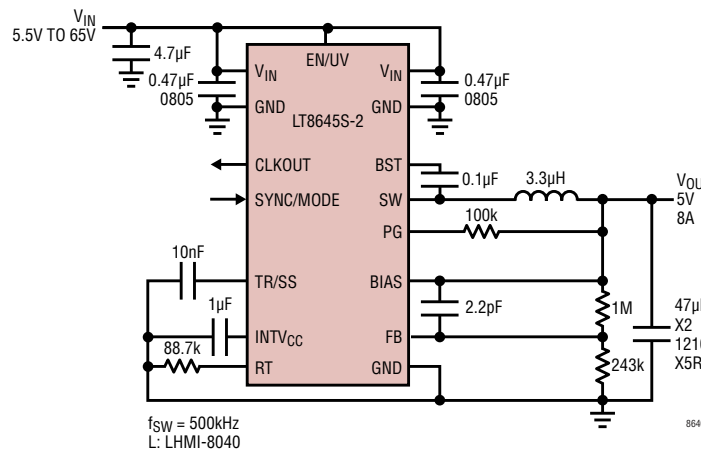


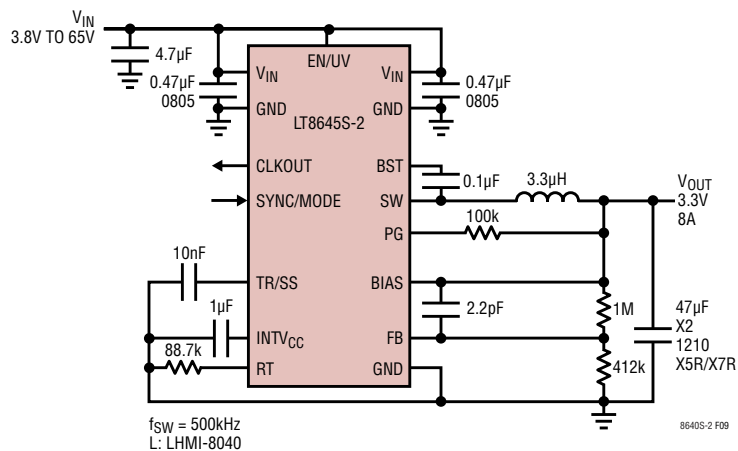
Figure 5. Case Temperature Rise

TYPICAL APPLICATIONS

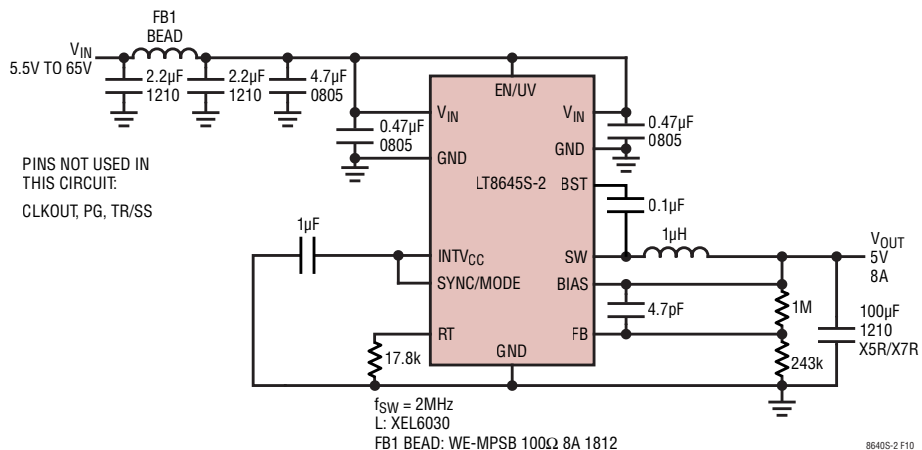
5V 8A Step-Down Converter with Soft-Start and Power Good



3.3V, 8A Step-Down Converter with Soft Start and Power Good

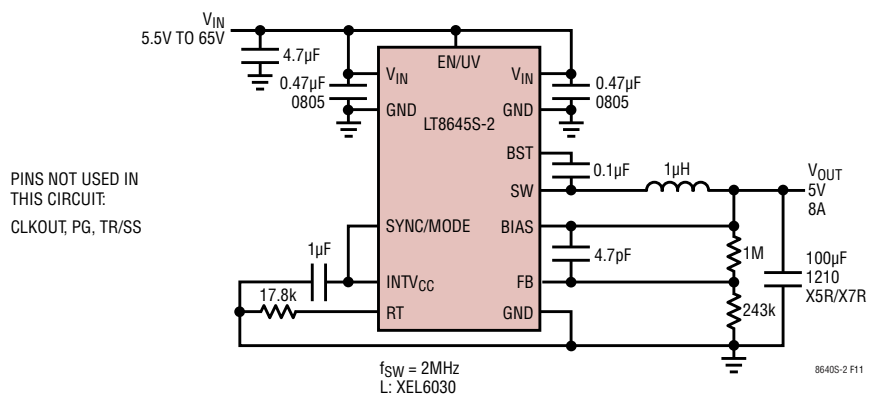


Ultralow EMI 5V, 8A Step-Down Converter with Spread Spectrum

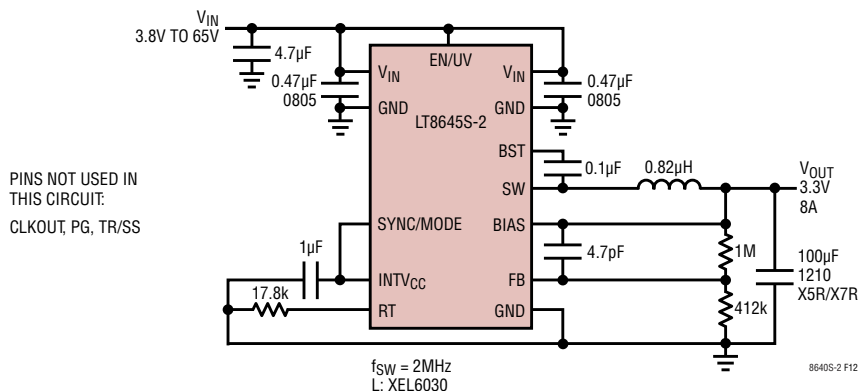


TYPICAL APPLICATIONS

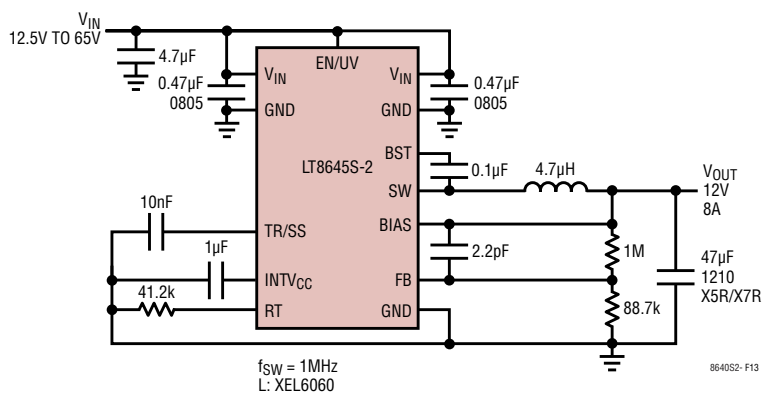
2MHz 5V, 8A Step-Down Converter with Spread Spectrum



2MHz 3.3V, 8A Step-Down Converter with Spread Spectrum



12V, 8A Step-Down Converter



PACKAGE DESCRIPTION

LQFN Package
32-Lead (6mm × 4mm × 0.94mm)
(Reference LTC DWG # 05-08-1512 Rev C)

