42V, Low I_Q, Quad Output Triple Monolithic Buck Converter and Boost Controller

FEATURES

- **Flexible Power Supply System Capable of Four Regulated Outputs with V_{BATT} << V_{OUT}**
- **Two High Voltage Synchronous Buck Regulators**
  - **3V to 42V Input Voltage Range**
  - **Output Currents Up to 2.5A and 1.5A**
- **One Low Voltage Synchronous Buck Regulator**
  - **2.6V to 5.5V Input Voltage Range**
  - **Output Currents Up to 1.8A**
- **One Boost Controller Allows Buck Converters to Regulate with V_{BATT} << V_{OUT}**
- **Selectable Burst Mode® Operation Allows Low 28µA I_Q with High Voltage Channels Active**
- Programmable Power-On Reset
- Individual Channel Power Good Indicators
- Step-Down Switching Frequency: 250kHz to 2.2MHz
- Available in 40-Lead QFN (6mm × 6mm) Package
- AEC-Q100 Qualified for Automotive Applications

APPLICATIONS

- Automotive Stop-Start and Cold Crank Ride Through
- Last-Gasp CPU Power Hold-Up
- Industrial Controls and Power Supplies

DESCRIPTION

The LT®8603 is a highly flexible, quad output regulator combining two high input voltage capable monolithic step-down switching regulators, one low input voltage capable monolithic step-down regulator, and a boost controller to satisfy a wide range of applications while occupying minimal board space.

With the boost controller configured to supply the chip V_{IN} supply, the LT8603 produces three precisely regulated outputs even when the boost input voltage falls significantly below the regulated output voltages, such as during an automotive cold crank scenario. Alternatively, with the boost controller driven from one of the step-down regulator outputs or configured as a SEPIC, the LT8603 provides four precisely regulated outputs over a wide input voltage range.

The LT8603 provides robust regulation by including a cycle-by-cycle current limit for all step-down regulators, thermal shutdown, and a boost controller that can tolerate reverse battery connections and negative transient input voltages down to –42V.

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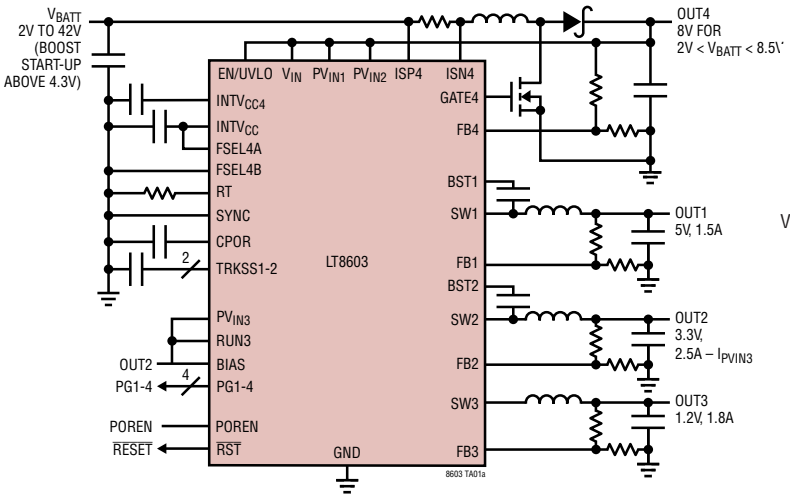
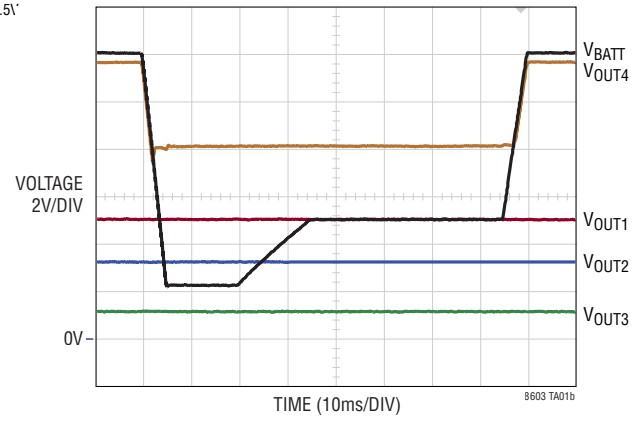
TYPICAL APPLICATION

Cold Crank Tolerant Automotive Triple Output Supply



LT8603 Response to a Cold Crank Automotive Input Waveform



ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltages

V_{IN}, $PV_{IN1,2}$ ..... –0.3V to 42V

PV_{IN3} ..... –0.3V to 6V

EN/UVLO 42V

ISP4, ISN4 ..... –42V to 42V

TRKSS1-2, RUN3, FB4, PG1-4, SYNC 6V

FSEL4A, FSEL4B, $\overline{RST}$.....6V

FB1-3, CPOR, POREN.....3.6V

BIAS..... –0.3V to 15V

Operating Junction Temperature (Notes 2, 5)

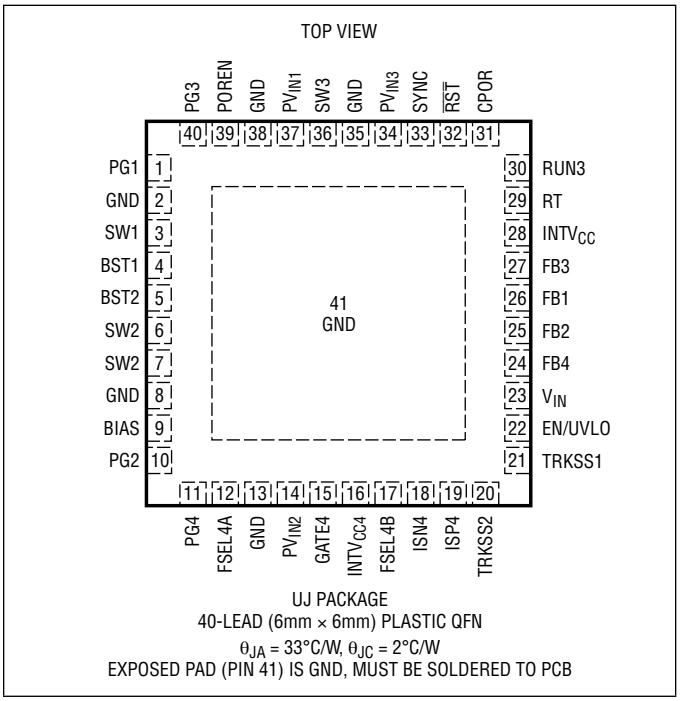
LT8603E ..... –40°C to 125°C

LT8603I ..... –40°C to 125°C

LT8603J ..... –40°C to 150°C

Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



UJ PACKAGE
40-LEAD (6mm × 6mm) PLASTIC QFN
θ_{JA} = 33°C/W, θ_{JC} = 2°C/W
EXPOSED PAD (PIN 41) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT8603EUJ#PBF	LT8603EUJ#TRPBF	LT8603UJ	40-Lead (6mm × 6mm) Plastic QFN	–40°C to 125°C
LT8603IUJ#PBF	LT8603IUJ#TRPBF	LT8603UJ	40-Lead (6mm × 6mm) Plastic QFN	–40°C to 125°C
LT8603JUJ#PBF	LT8603JUJ#TRPBF	LT8603UJ	40-Lead (6mm x 6mm) Plastic QFN	–40°C to 150°C
AUTOMOTIVE PRODUCTS**				
LT8603EUJ#WPBF	LT8603EUJ#WTRPBF	LT8603UJ	40-Lead (6mm × 6mm) Plastic QFN	–40°C to 125°C
LT8603IUJ#WPBF	LT8603IUJ#WTRPBF	LT8603UJ	40-Lead (6mm × 6mm) Plastic QFN	–40°C to 125°C
LT8603JUJ#WPBF	LT8603JUJ#WTRPBF	LT8603UJ	40-Lead (6mm × 6mm) Plastic QFN	–40°C to 150°C

Contact the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

**Versions of this part are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. These models are designated with a #W suffix. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 12V, EN/UVLO = 3V unless otherwise noted. (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Bias and Internal Regulators						
Minimum Operating V_{IN} for Channels 1, 2 and 3		●		2.7	3.0	V
Minimum V_{IN} to Start for Channels 1, 2 and 3		●		3.1	3.3	V
Minimum Operating V_{IN} for Channel 4		●		3.0	3.2	V
Minimum V_{IN} to Start for Channel 4		●		4.0	4.15	V
V_{IN} Quiescent Current, Shutdown	V_{BIAS} = 0V, EN/UVLO = 0.4V			0.1	1	µA
Total Operating Current V_{BATT}	V_{BATT} = 12V, Channels 1 and 2 Active, No-Load (Note 4) V_{BATT} = 12V, All Channels Active, No-Load (Note 4)			28 50		µA µA
EN/UVLO Threshold	EN/UVLO Rising	●	1.15	1.2	1.25	V
	EN/UVLO Falling	●	1.1	1.15	1.2	V
EN/UVLO Input Current	EN/UVLO = 1.2V		–50		50	nA
$INTV_{CC4}$ Regulated Voltage	V_{BIAS} = 0V V_{BIAS} = 6V	● ●	4.4 4.7	4.6 5	4.8 5.2	V V
$INTV_{CC4}$ Regulator Load Regulation	$INTV_{CC4}$ at 1mA – $INTV_{CC4}$ at 40mA			70		mV
Oscillator						
Switching Frequency	R_T = 28.7kΩ, E, I-Grade R_T = 28.7kΩ, J-Grade R_T = 243kΩ, E, I ,J-Grade	● ● ●	1.8 1.75 0.224	2 2 0.25	2.2 2.2 0.284	MHz MHz MHz
SYNC Input Frequency Range		●	0.25		2.2	MHz
SYNC Input Voltage Low		●			0.3	V
SYNC Input Voltage High		●	1.2			V
SYNC Input Current			–100		100	nA
FSEL4A, FSEL4B Input Voltage Low		●			0.4	V
FSEL4A, FSEL4B Input Voltage High		●	2			V
FSEL4A, FSEL4B Input Current		●	–100		100	nA
Channel 1						
Feedback Voltage FB1	E-, I-Grade J-Grade	● ●	0.985 0.98	1 1	1.015 1.015	V V
Input Current FB1		●	–100		100	nA
FB1 Line Regulation	V_{IN} = 3V to 42V			0.002	0.01	%/V
SW1 Peak Current Limit (Note 3)			2.0	2.7	3.7	A
SW1 Leakage Current				0.1	1	µA
SW1 Top On-Resistance	I_{SW1} = 1A			240		mΩ
SW1 Bottom On-Resistance	I_{SW1} = 1A			170		mΩ
Lower FB1 Power Good Threshold	Percentage of V_{FB1}, V_{FB1} Falling	●	89	92	95	%
Upper FB1 Power Good Threshold	Percentage of V_{FB1}, V_{FB1} Rising	●	104	107	110	%
Power Good Threshold Hysteresis				0.8		%
PG1 Output Voltage Low	I_{PG1} = 350µA	●		0.13	0.3	V
PG1 Leakage Current	PG1 = 5V, FB1 = 1V	●			6	µA
TRKSS1 Pull-Up Current	TRKSS1 = 0.2V		1.5	2.4	3.1	µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 12V, EN/UVLO = 3V unless otherwise noted. (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Channel 2						
Feedback Voltage FB2	E-, I-Grade J-Grade	● ●	0.985 0.98	1 1	1.015 1.015	V V
Input Current FB2		●	–100		100	nA
FB2 Line Regulation	V_{IN} = 3V to 42V			0.002	0.01	%/V
SW2 Peak Current Limit (Note 3)			3.2	4.0	5.3	A
SW2 Leakage Current				0.1	1	µA
SW2 Top On-Resistance	I_{SW2} = 1A			150		mΩ
SW2 Bottom On-Resistance	I_{SW2} = 1A			100		mΩ
Lower FB2 Power Good Threshold	Percentage of V_{FB2}, V_{FB2} Falling	●	89	92	95	%
Upper FB2 Power Good Threshold	Percentage of V_{FB2}, V_{FB2} Rising	●	104	107	110	%
Power Good Threshold Hysteresis				0.8		%
PG2 Output Voltage Low	I_{PG2} = 350µA	●		0.13	0.3	V
PG2 Leakage Current	PG2 = 5V, FB2 = 1V	●			6	µA
TRKSS2 Pull-Up Current	TRKSS2 = 0.2V		1.5	2.4	3.1	µA
Channel 3						
PV_{IN3} Operating Voltage	PV_{IN3} Falling	●	2.6		5.5	V
PV_{IN3} Undervoltage Lockout	PV_{IN3} Falling	●		2.35	2.6	V
Feedback Voltage FB3	E-, I-Grade J-Grade	● ●	788 784	800 800	812 812	mV mV
FB3 Line Regulation	V_{IN} = 3V to 42V			0.002	0.01	%/V
Input Current FB3		●	–100		100	nA
SW3 Leakage Current				0.1	1	µA
SW3 Peak Current Limit (Note 3)			2.6	3.2	3.8	A
SW3 PMOS On-Resistance	I_{SW3} = 1A			150		mΩ
SW3 NMOS On-Resistance	I_{SW3} = 1A			100		mΩ
Lower FB3 Power Good Threshold	Percentage of V_{FB3}, V_{FB3} Falling	●	89	92	95	%
Upper FB3 Power Good Threshold	Percentage of V_{FB3}, V_{FB3} Rising	●	104	107	110	%
Power Good Threshold Hysteresis				0.2		%
PG3 Output Voltage Low	I_{PG3} = 350µA	●		0.13	0.3	V
PG3 Leakage Current	PG3 = 5V, FB3 = 0.8V	●			6	µA
RUN3 Threshold Voltage		●	1.15	1.20	1.25	V
RUN3 Input Current			–100		100	nA
Soft-Start Time			0.7	1	1.3	ms

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 12V, EN/UVLO = 3V unless otherwise noted. (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Channel 4						
Feedback Voltage FB4	E-, I-Grade J-Grade	● ●	788 784	800 800	812 812	mV mV
FB4 Line Regulation	V_{IN} = 3.2V to 42V			0.002	0.01	%/V
Input Current FB4		●	–100		100	nA
Soft-Start Time				1		ms
Current Comparator Limit Threshold	V_{ISP4} to V_{ISN4}, V_{CM} = 2V to 42V, E, I-Grade V_{ISP4} to V_{ISN4}, V_{CM} = 2V to 42V, J-Grade	● ●	43 41	50 50	57 57	mV mV
Current Comparator Input Common Mode Range			2		42	V
ISP4, ISN4 Input Currents, Sleep	V_{ISP4} = V_{ISN4} = 2V to 42V, FB4 = 1V, SYNC = 0V				200	nA
ISP4, ISN4 Input Currents, Active	V_{ISP4} = V_{ISN4} = 2V to 42V, FB4 = 0V, SYNC = 0V			34	44	µA
ISP4, ISN4 Input Currents	V_{ISP4} = V_{ISN4} = –42V			7	10	mA
GATE4 High Side PMOS On-Resistance				2.5		Ω
GATE4 Low Side NMOS On-Resistance				1.25		Ω
FB4 Power Good Threshold	Percentage of V_{FB4}, V_{FB4} Falling	●	89	92	95	%
Power Good Threshold Hysteresis				0.2		%
PG4 Output Voltage Low	I_{PG4} = 350µA	●		0.13	0.3	V
PG4 Leakage Current	PG4 = 5V, FB4 = 0.8V	●			6	µA
Power-On Reset						
POR Delay Time	CPOR = 1000pF	●	31	35.2	39.4	ms
$\overline{RST}$ Output Voltage Low	$I_{\overline{RST}}$ = 100µA	●		0.1	0.2	V
$\overline{RST}$ Pull-Up Current	POR Timed Out, $\overline{RST}$ = 0V			20		µA
$\overline{RST}$ Leakage Current	POR Timed Out, $\overline{RST}$ = 6V		–100		100	nA
POREN Threshold		●	1.15	1.2	1.25	V
POREN Pull-Up Current	POREN = 0V		0.6	1.0	1.4	µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LT8603E is guaranteed to meet performance specifications from 0°C to 125°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LT8603I is guaranteed to meet performance specifications from –40°C to 125°C junction temperature. The LT8603J is guaranteed over the full –40°C to 150°C operating junction temperature range. High junction temperatures degrade operating lifetimes. Operating lifetime is derated at junction temperatures above 125°C.

Note 3: Current limit is assured by design and/or correlation to static test. Slope compensation reduces current limit at higher duty cycles.

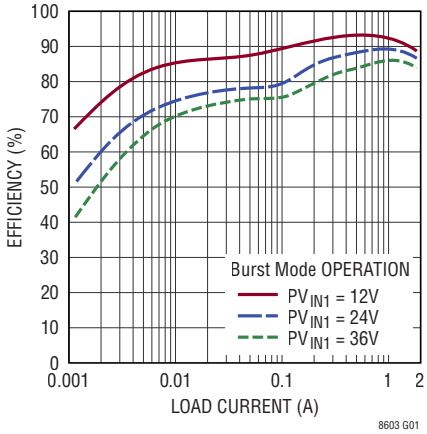
Note 4: Measurement made using the circuit titled, “Details of Front Page Application” in the Typical Applications section.

Note 5: This IC includes overtemperature protection that is intended to protect the device during overload conditions. Junction temperature will exceed 150°C when overtemperature protection is active. Continuous operation above the specified maximum junction temperature will reduce lifetime.

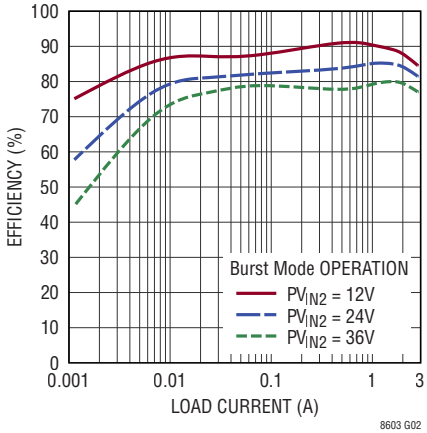
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{IN} = PV_{IN1} = PV_{IN2} = 12V, EN/UVLO = 3V and PV_{IN3} = 3.3V unless otherwise noted.

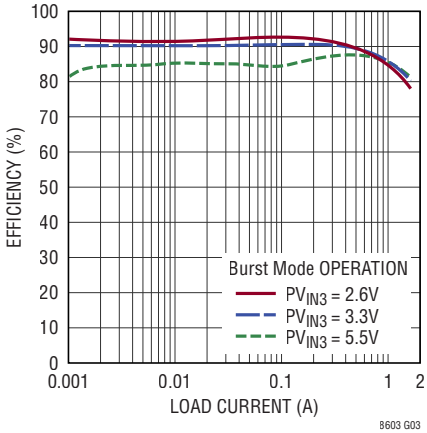
Channel 1 Efficiency vs Load
V_{OUT1} = 5V, f_{SW} = 1MHz



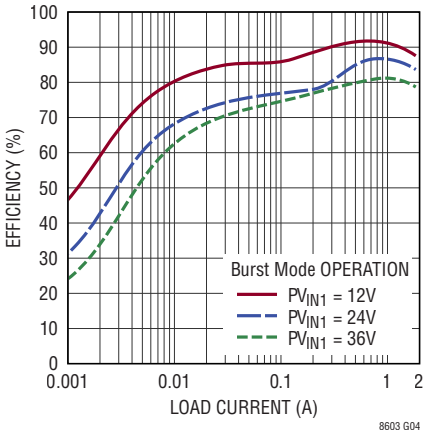
Channel 2 Efficiency vs Load
V_{OUT2} = 3.3V, f_{SW} = 1MHz



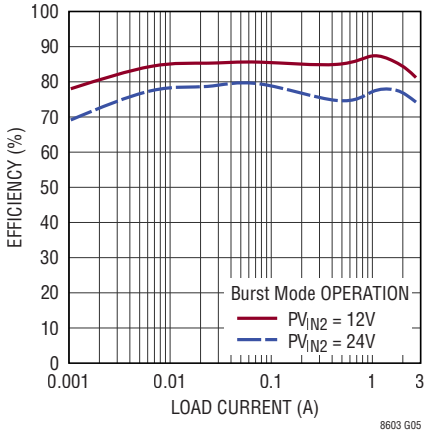
Channel 3 Efficiency vs Load
V_{OUT3} = 1.2V, f_{SW} = 1MHz



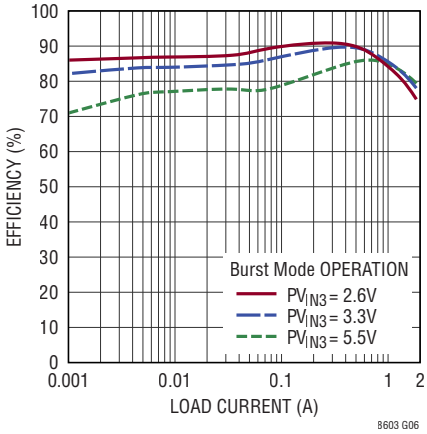
Channel 1 Efficiency vs Load
V_{OUT1} = 5V, f_{SW} = 2MHz



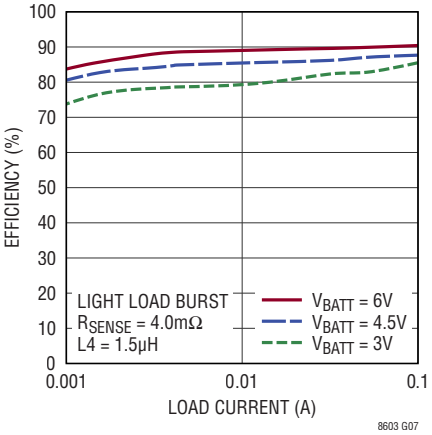
Channel 2 Efficiency vs Load
V_{OUT2} = 3.3V, f_{SW} = 2MHz



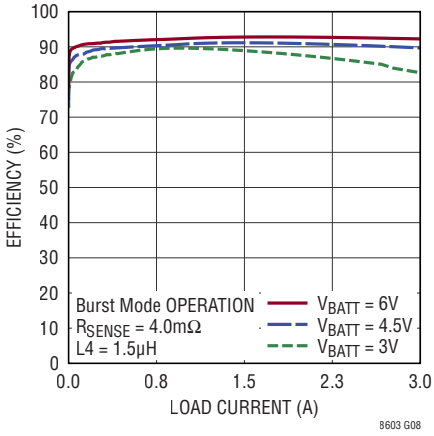
Channel 3 Efficiency vs Load
V_{OUT3} = 1.2V, f_{SW} = 2MHz



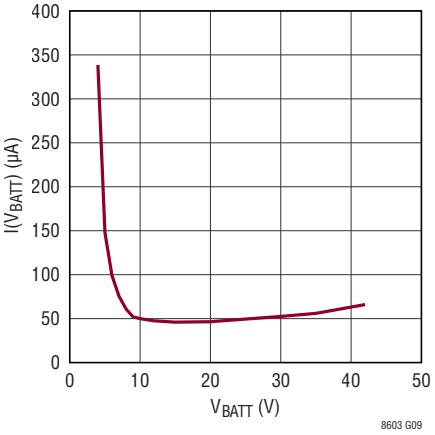
Channel 4 Efficiency vs Load
V_{OUT4} = 8V, f_{SW} = 1MHz



Channel 4 Efficiency vs Load
V_{OUT4} = 8V, f_{SW} = 1.0MHz



No-Load I (V_{IN}) vs V_{IN}
All Channels Enabled (Note 4)



TYPICAL PERFORMANCE CHARACTERISTICS

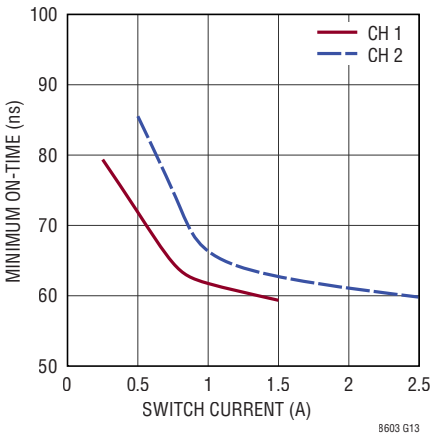
T_A = 25°C, V_{IN} = PV_{IN1} = PV_{IN2} = 12V, EN/UVLO = 3V and PV_{IN3} = 3.3V unless otherwise noted.

Channel 1
Peak Current Limit vs Duty Cycle

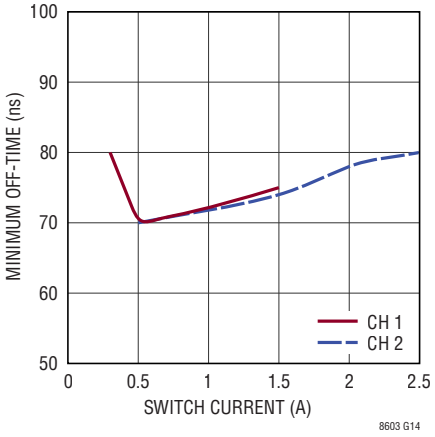
Channel 2
Peak Current Limit vs Duty Cycle

Channel 3
Peak Current Limit vs Duty Cycle

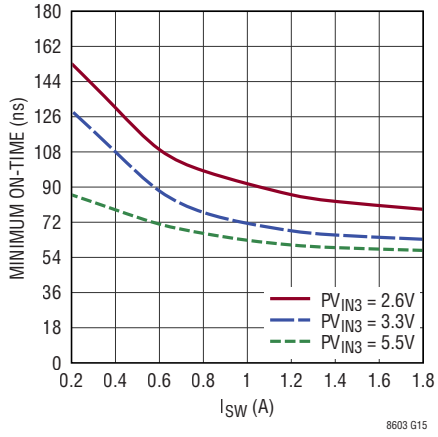
Channels 1, 2
Minimum On-Time vs I_{SW}



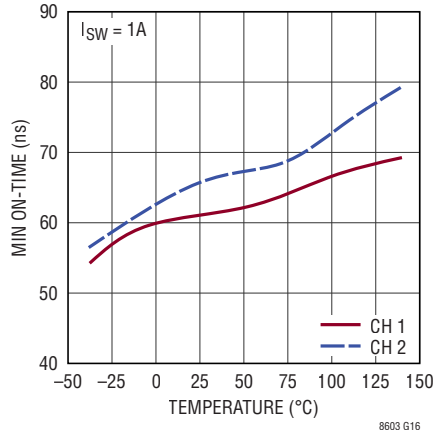
Channels 1, 2
Minimum Off-Time vs I_{SW}



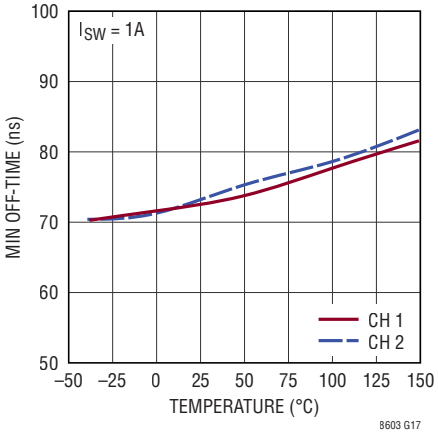
Channel 3
Minimum On-Time vs I_{SW}



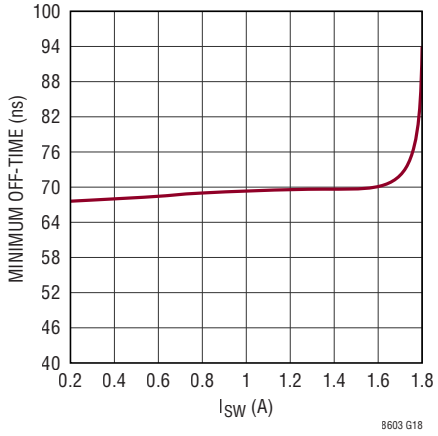
Channels 1, 2
Minimum On-Time vs Temperature



Channels 1, 2
Minimum Off-Time vs Temperature



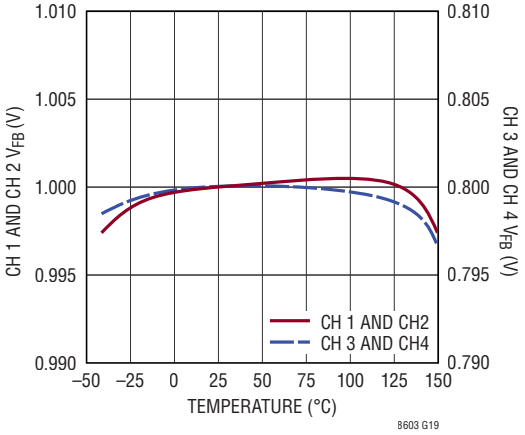
Channel 3
Minimum Off-Time vs I_{SW}



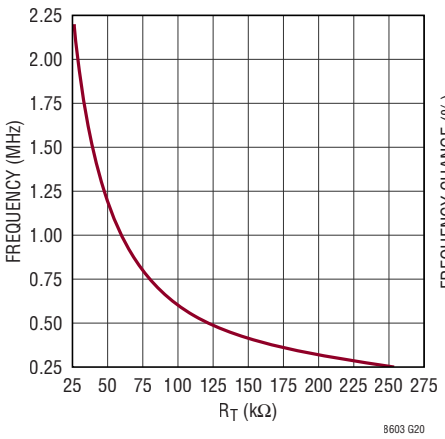
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{IN} = PV_{IN1} = PV_{IN2} = 12V, EN/UVLO = 3V and PV_{IN3} = 3.3V unless otherwise noted.

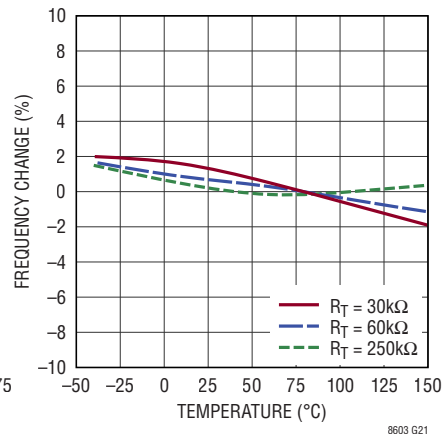
Feedback Voltage vs Temperature



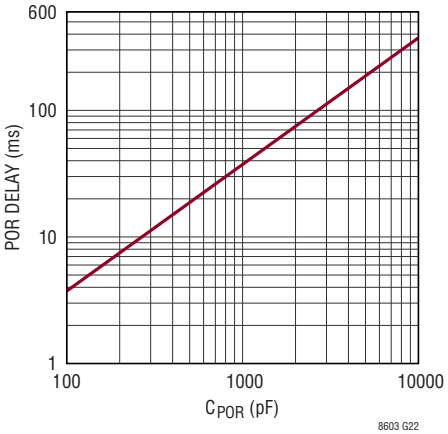
Switching Frequency vs R_T



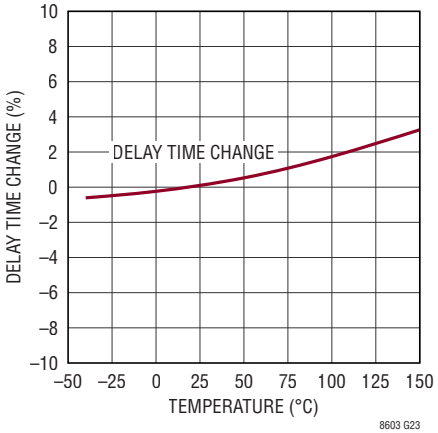
Switching Frequency vs Temperature



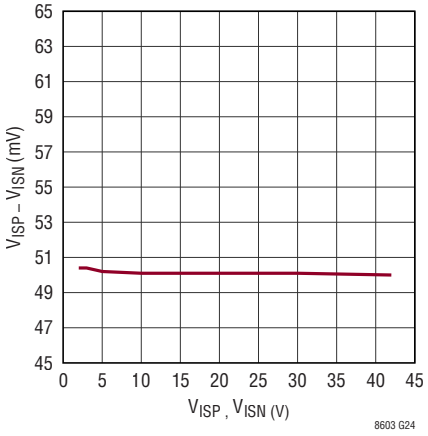
POR Delay vs C_{POR}



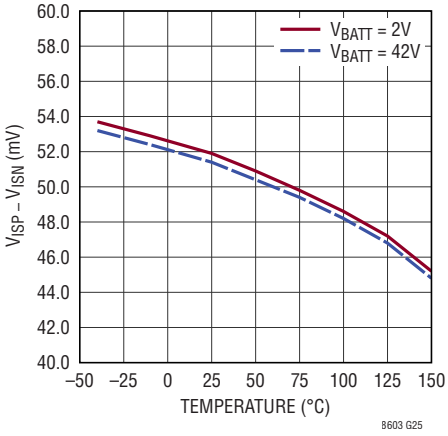
POR Delay Time vs Temperature



Channel 4 I_{LIM} Threshold vs Common Mode



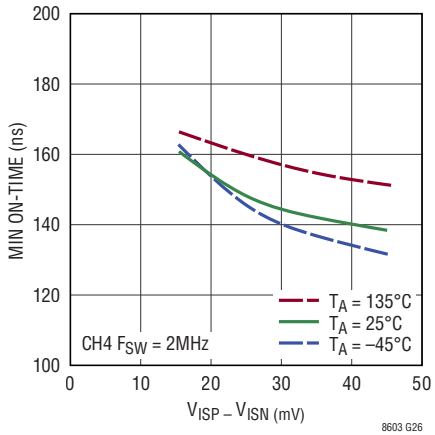
Channel 4 I_{LIM} Threshold vs Temperature



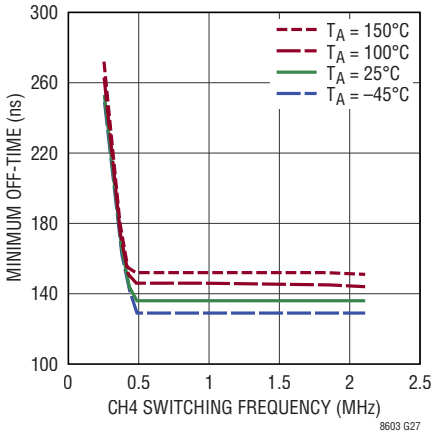
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{IN} = PV_{IN1} = PV_{IN2} = 12V, EN/UVLO = 3V and PV_{IN3} = 3.3V unless otherwise noted.

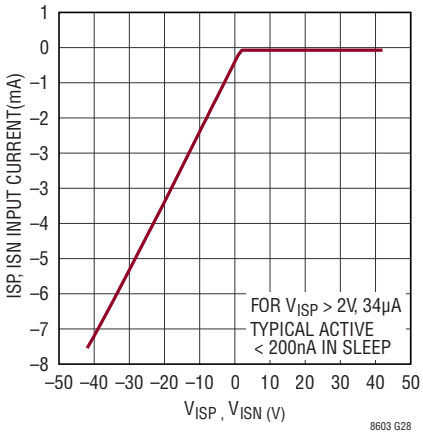
Channel 4 Minimum On-Time vs $V_{ISP} - V_{ISN}$



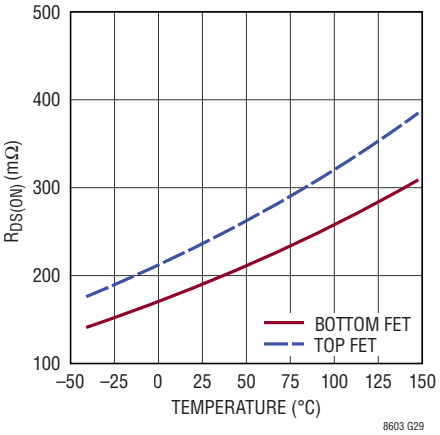
Channel 4 Minimum Off-Time vs $V_{ISP} - V_{ISN}$



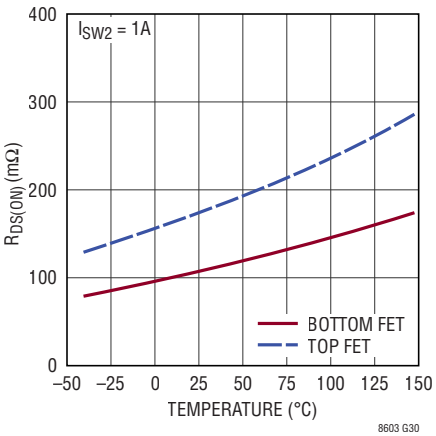
Channel 4 ISP, ISN Input Current vs V_{ISP}, V_{ISN}



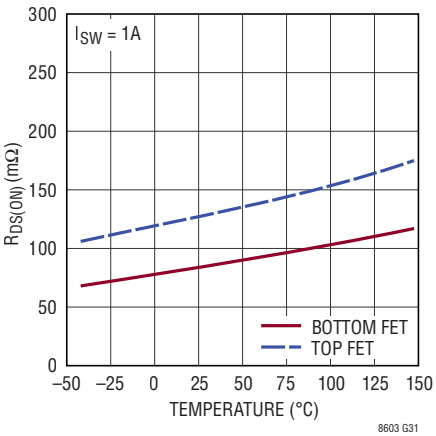
Channel 1 $R_{DS(ON)}$ vs Temperature



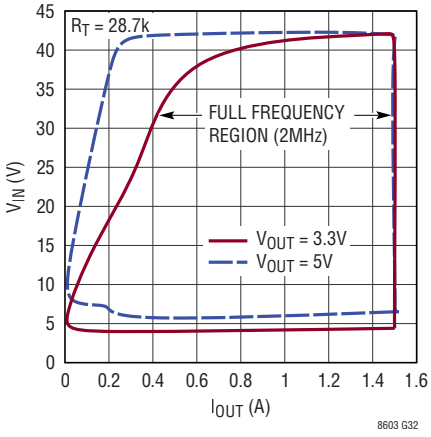
Channel 2 $R_{DS(ON)}$ vs Temperature



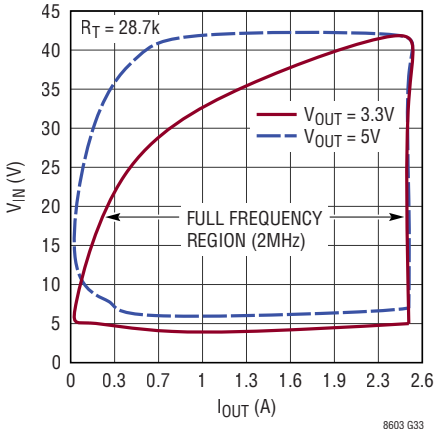
Channels 3 $R_{DS(ON)}$ vs Temperature



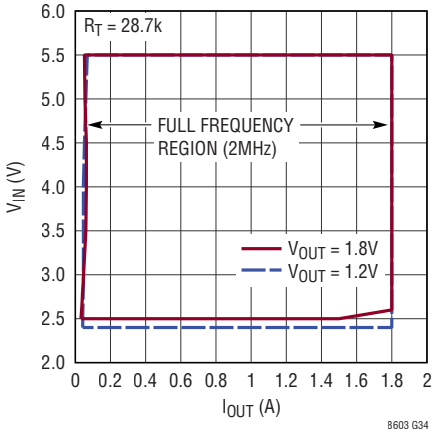
Channel 1 Full Frequency V_{IN} vs Load Current



Channel 2 Full Frequency V_{IN} vs Load Current



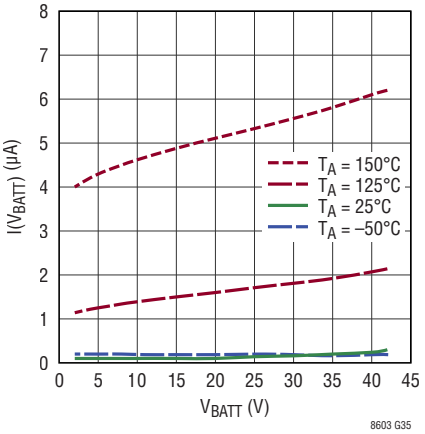
Channel 3 Full Frequency V_{IN} vs Load Current



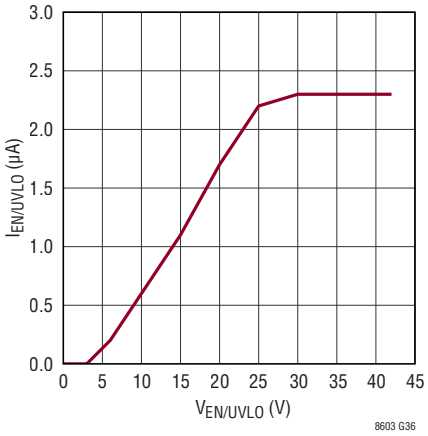
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{IN} = PV_{IN1} = PV_{IN2} = 12V, EN/UVLO = 3V and PV_{IN3} = 3.3V, unless otherwise noted.

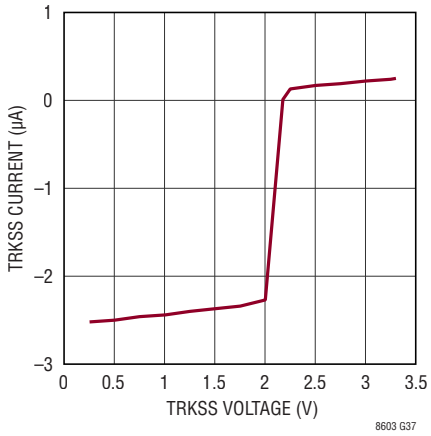
Shutdown I_Q from the Battery Overvoltage/Temperature



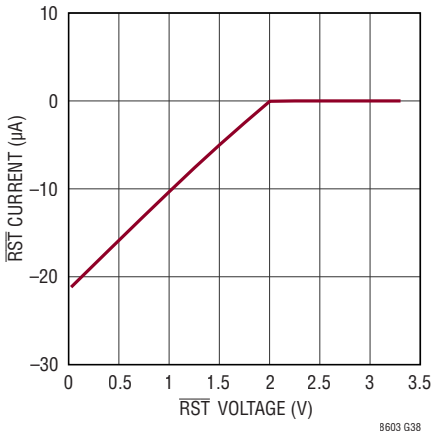
EN/UVLO Current vs Voltage



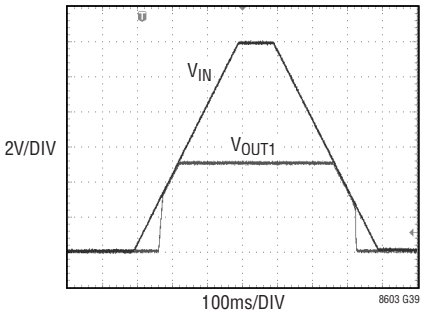
TRKSS Pull-Up Current vs Voltage



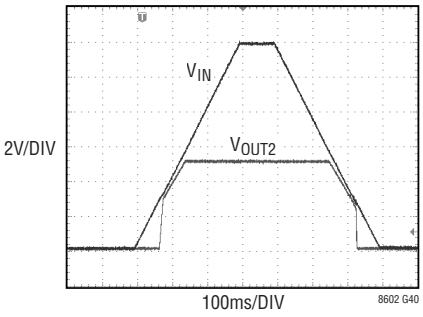
$\overline{RST}$ Pull-Up Current vs Voltage



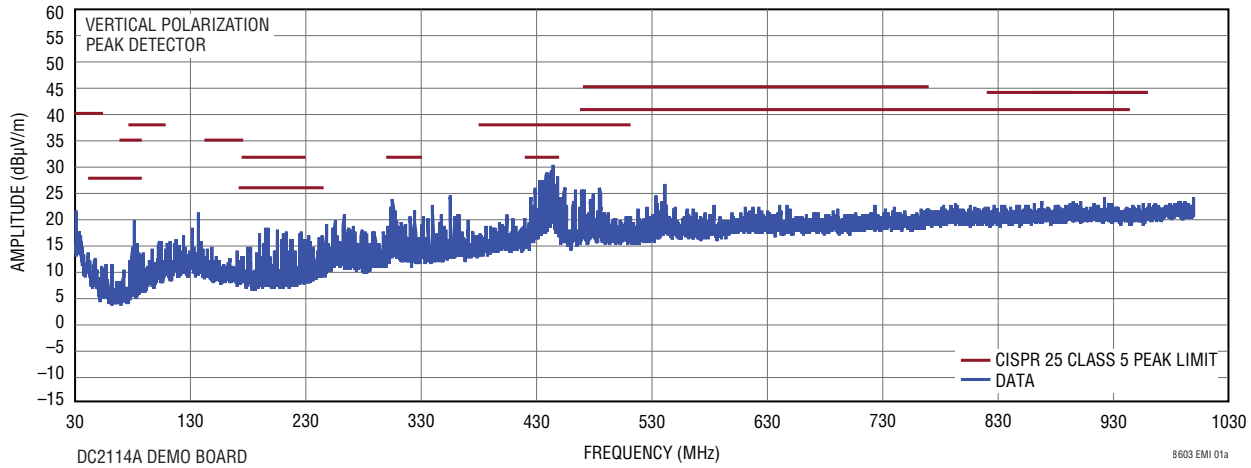
Channel 1 Start-Up and Dropout, R_L = 20Ω



Channel 2 Start-Up and Dropout, R_L = 2Ω



Radiated EMI Performance, CISPR 25 Radiated Emission Tests with Class 5 Peak Limits



DC2114A DEMO BOARD
(WITH EMI FILTER INSTALLED)
V_{BATT} = 14V, V_{OUT1} = 5V, V_{OUT2} = 3.3V, V_{OUT3} = 1.8V, $I_{OUT1,2,3}$ = 1A
f_{SW} = 2MHz, FSELA = $INTV_{CC}$, FSELB = Ground

PIN FUNCTIONS

PG1, PG2, PG3 (Pins 1, 10, 40): Power Good Indicators for Channels 1, 2 and 3, respectively. These pins are open-drain outputs that pull down until the associated FB pin is within ±8% of the target regulation voltage.

GND (Pins 2, 8, 13, 35, 38, Exposed Pad 41): Ground. All ground pins and the exposed pad must be soldered to PCB ground. See the Applications Information section for PCB layout recommendations.

SW1 (Pin 3): High Voltage Converter 1 Switch Node. This is the output of the internal power switches for Channel 1.

BST1, BST2 (Pins 4, 5): Boost Voltage for High Voltage Converters. These pins provide the drive voltage required by the internal power MOSFETs. A capacitor should be connected from BST to the associated SW pin.

SW2 (Pins 6, 7): High Voltage Converter 2 Switch Node. This is the output of the internal power switches for Channel 2. These pins should be soldered to the same PCB trace for even current distribution.

BIAS (Pin 9): Alternate Power Source for $INTV_{CC}$ and $INTV_{CC4}$ Regulators. If BIAS > 3.1V for $INTV_{CC}$ or > 4.6V for $INTV_{CC4}$ the internal regulators will draw their power from BIAS. This will reduce the on-chip power dissipation during full frequency operation and reduce the effective no-load sleep current at the input.

PG4 (Pin 11): Power Good Indicator Channel 4. This pin is an open-drain output that pulls low until the Channel 4 feedback voltage is greater than 92% of its reference voltage.

FSEL4A, FSEL4B (Pins 12, 17): Boost Converter Frequency Select and RUN Control. These pins are logic inputs. When both pins are low, the boost controller is shut down. The boost controller switching frequency is controlled using these pins according to Table 2 in the Applications Information section.

GATE4 (Pin 15): External MOSFET Gate Drive Output. This pin switches from GND to $V_{INTVCC4}$ to turn on the low side power MOSFET in the BOOST converter. See the Applications Information section for information on MOSFET selection.

$INTV_{CC4}$ (Pin 16): Internal Boost Regulator Output. Do not load the $INTV_{CC4}$ pin with external circuitry. $INTV_{CC4}$ is 4.6V when BIAS < 4.6V, 5V when BIAS > 5V, and equal to BIAS when BIAS is between 4.6V and 5V. Decouple to ground with a low ESR 4.7µF capacitor.

ISP4, ISN4 (Pins 19, 18): Boost Controller Current Sense Inputs. Connect a current sense resistor of appropriate value between these pins with ISP4 connected to the input supply and ISN4 to the application inductor. See the Applications Information section for sense resistor selection details.

TRKSS1, TRKSS2 (Pins 21, 20): Track/Soft-Start Inputs for the High Voltage Converters. When this pin is below 1V, the converter regulates the FB pin to the TRKSS voltage instead of the internal reference. The TRKSS pin has a 2.4µA pull-up current. Connect a capacitor between either of these pins to ground to program a soft-start time for the associated channel.

EN/UVLO (Pin 22): Enable/Undervoltage Lockout Input. The LT8603 is in low power shutdown when this pin is below 0.4V. Between 0.4V and 1.1V, the part will turn on the internal reference. A precision threshold at 1.2V (rising) enables the switching regulators. The precision threshold allows the EN/UVLO pin to be used as an input undervoltage lockout by connecting to resistor divider between V_{IN} and GND. When the EN/UVLO voltage is between 0.4V and 1.2V, the LT8603 input current will depend on the mode selected, the V_{IN} voltage and EN/UVLO voltage.

V_{IN} (Pin 23): Power Supply to Internal Functions. This pin provides power to the LT8603 internal circuitry. This pin must reach 4V for the boost converter to complete its internal soft-start delay of 1ms.

FB4 (Pin 24): Feedback Input Pin for the Boost Converter. The converter regulates FB4 to 0.8V.

FB1, FB2 (Pins 26, 25): Feedback Input Pins for the High Voltage Converters. The converters regulate the

PIN FUNCTIONS

corresponding feedback pin to the lesser of 1V or the voltage on the associated TRKSS pin.

FB3 (Pin 27): Feedback Input Pin for the Low Voltage Converter. The converter regulates FB3 to 0.8V.

$INTV_{CC}$ (Pin 28): Internal Regulator Bypass. Do not load the $INTV_{CC}$ pin with external circuitry. $INTV_{CC}$ is 3.1V when BIAS < 3.1V, 3.4V when BIAS > 3.4V, and equal to BIAS when BIAS is between 3.1V and 3.4V. Decouple to ground with a low ESR 4.7µF capacitor.

RT (Pin 29): Frequency Programming Resistor. Connect a resistor between this pin and ground to set the internal oscillator frequency. This pin should not be left open.

RUN3 (Pin 30): Enable Input For Low Voltage Channel 3. Channel 3 is enabled when the voltage on this pin exceeds 1.2V. The RUN3 pin has a precise threshold so it can be used to create a UVLO function or be sequenced from another channel. There is an internal soft-start timer which ramps the output up in approximately 1ms.

CPOR (Pin 31): Power-On Reset Timing Capacitor. A capacitor from this pin to ground sets the period of the power-on reset oscillator timer. See the Applications Information Section for details.

$\overline{RST}$ (Pin 32): Active Low Reset Output. This pin is the output of the power-on reset function. This pin is an open-drain output with a weak pull-up to approximately 2V. This pin is held low until the power on reset timer times out.

SYNC (Pin 33): Clock Synchronization and Mode Select Input. This pin allows the LT8603 to synchronize its switching frequency to an external clock. When an external clock is applied, the LT8603 will operate in pulse-skipping mode. If clock synchronization is not used, connect this pin to ground to enable low ripple Burst Mode operation or connect high to enable pulse-skipping operation.

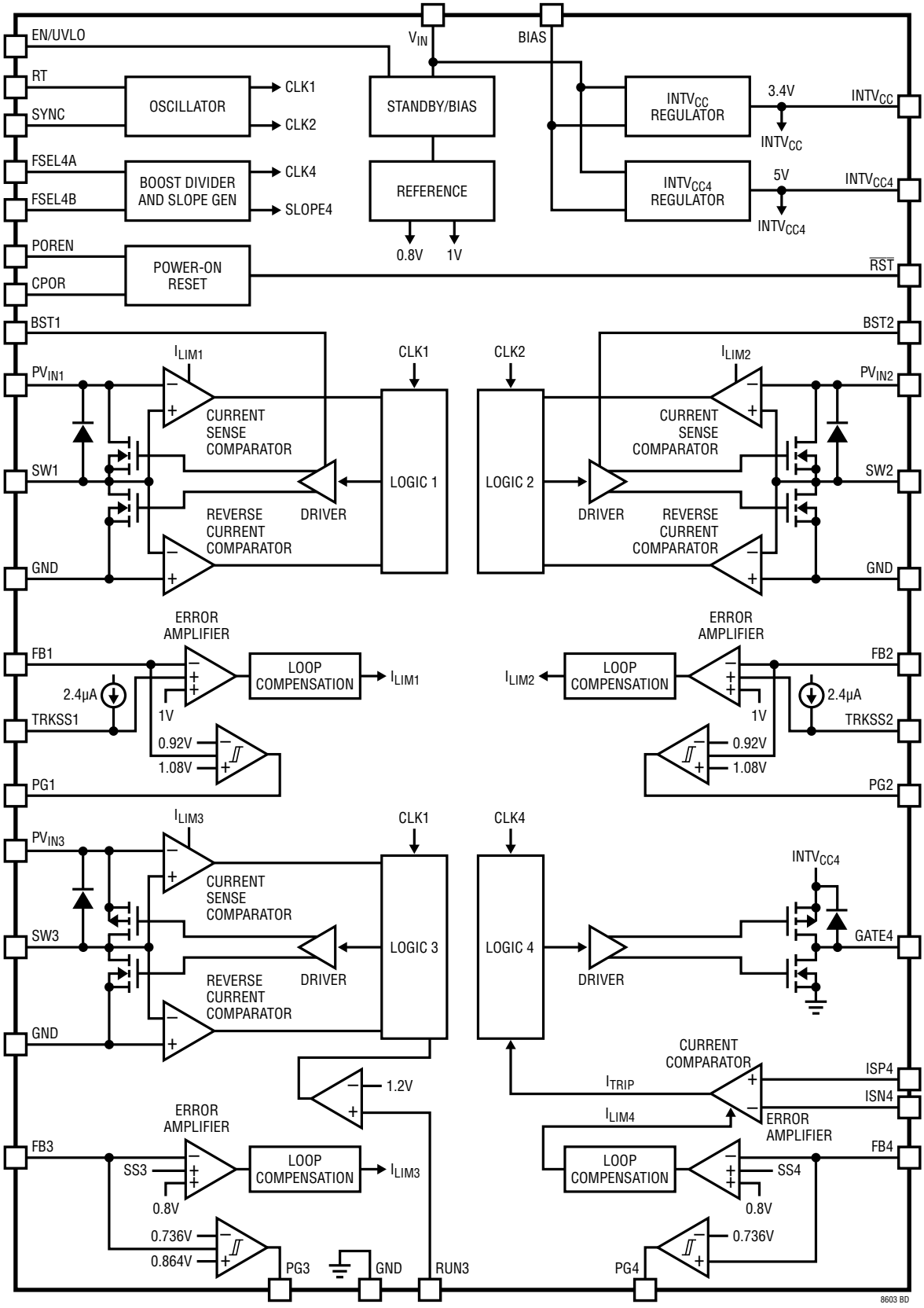
PV_{IN3} (Pin 34): Input Supply Voltage to Low Voltage Channel 3. This pin will normally be connected to the output of one of the high voltage converters but can be supplied from any voltage in the specified range. It should be bypassed locally with a low ESR ceramic capacitor to ground with a low inductance connection to the exposed pad.

SW3 (Pin 36): Low Voltage Converter Switch Node. This is the output of the internal power switches for Channel 3.

PV_{IN1}, PV_{IN2} (Pins 37, 14): Input Supply to High Voltage Channels 1 and 2, respectively. These pins can be powered from the boost converter output or any voltage in the specified range. Each pin should be bypassed locally with a low ESR ceramic capacitor to ground with a low inductance connection to the exposed pad.

POREN (Pin 39): Power-On Reset Enable. This is a logic input that starts the ramp on the POR timing capacitor. This input has a weak pull-up to allow direct connection to open-drain outputs.

BLOCK DIAGRAM



OPERATION

The LT8603 combines two 42V input step-down converters (Channels 1 and 2), one 5.5V input step-down converter (Channel 3) and a boost controller (Channel 4) to provide a flexible system that can be configured to generate up to four regulated outputs. For example, the boost controller may be used to guarantee a supply to the high voltage converters above their minimum dropout voltage even during the cold crank cycle in an automobile.

Start-Up

When enabled by setting the EN/UVLO voltage above its threshold, the LT8603 $INTV_{CC}$ regulator charges its output capacitor to supply the internal chip circuitry. If BIAS is higher than 3.1V, BIAS supplies current to the $INTV_{CC}$ regulator to reduce V_{IN} quiescent current.

The boost controller is enabled with a logic high on either one or both of the FSEL4A and FSEL4B pins. Once enabled, the $INTV_{CC4}$ regulator charges its output capacitor bringing the $INTV_{CC4}$ supply into regulation. When the voltage at $INTV_{CC4}$ exceeds 4.0V, the boost controller gate driver will begin supplying gate drive pules to the external MOSFET. Like the $INTV_{CC}$ regulator, the $INTV_{CC4}$ regulator can also draw power from the BIAS pin when BIAS exceeds 4.6V.

High Voltage Buck Regulators (Channels 1 and 2)

Each high voltage channel is a synchronous buck regulator that operates from an independent PV_{IN} pin. The internal top power MOSFET is turned on at the beginning of each oscillator cycle, and turned off when the current flowing through the top MOSFET reaches a level determined by the error amplifier. The error amplifier measures the output voltage through an external resistor divider tied to the FB pin to control the peak current in the top switch. The reference of the error amplifier is determined by the lower of the internal 1V reference and the voltage at its TRKSS pin. While the top MOSFET is off, the bottom MOSFET is turned on for the remainder of the oscillator cycle or until the inductor current starts to reverse. If overload conditions result in more than 2A for Channel 1 or 3.3A for Channel 2 flowing through the bottom switch, the next clock cycle will be delayed until switch current returns to a safe level. The TRKSS pins can be used for controlled start-up or tracking of another supply.

Low Voltage Buck Regulator (Channel 3)

The low voltage channel is a synchronous buck regulator that operates from an independent PV_{IN} pin. The PV_{IN} pin has an undervoltage lockout set at 2.35V. The top power MOSFET is turned on at the beginning of each oscillator cycle, and turned off when the current flowing through the top MOSFET reaches a level determined by the error amplifier. The error amplifier measures the output voltage through an external resistor divider tied to the FB3 pin to control the peak current in the top switch. The reference of the error amplifier is an internal 800mV reference. While the top MOSFET is off, the bottom MOSFET is turned on for the remainder of the oscillator cycle or until the inductor current starts to reverse. If overload conditions result in more than 2.4A flowing through the bottom switch, the next clock cycle will be delayed until switch current returns to a safe level.

The low voltage channel has a RUN3 pin to allow power sequencing, plus an internal soft-start circuit that ramps the output voltage up in 1ms.

Boost Controller (Channel 4)

The boost controller includes an error amplifier, loop compensation, current comparator, switch control logic, and a gate driver. The controller is enabled and its clock frequency selected by control of the FSEL4A and FSEL4B pins as described in the Applications Information section.

The required external N-channel MOSFET is turned on by the internal clock and turned off when the inductor current sensed by the current comparator exceeds its threshold. The error amplifier adjusts the current comparator threshold by comparing the FB4 voltage to an internal 0.8V reference voltage. The output voltage is set by a resistor divider from the output to the FB4 pin. The internal $INTV_{CC4}$ regulator provides the gate drive for the external MOSFET.

OPERATION

Multiphase Switching

The oscillator generates two clock signals 180° out of phase with each other. Channels 1 and 3 operate from CLK1, while Channels 2 and 4 operate from CLK2. The clock for Channel 4 may be selected as either a ÷1, ÷2 or ÷5 version of CLK2 using the FSEL4A and FSEL4B pins. Regardless of the divide ratio chosen, the Channel 4 clock edges remain aligned to the CLK2 edges.

Since a buck regulator only draws input current during the top switch on cycle, multiphase operation reduces peak input current and doubles the input current frequency. These effects reduce input current ripple and reduce the input capacitance required.

Undervoltage Lockout

The EN/UVLO pin is used to put the LT8603 in shutdown, reducing the input current to less than 1µA. The accurate 1.2V threshold of the EN/UVLO pin provides a programmable V_{IN} undervoltage lockout through an external resistor divider tied to the EN/UVLO pin. A 50mV hysteresis voltage on the EN/UVLO pin prevents switching noise from inadvertently shutting down the LT8603.

Power Good Comparators

Channels 1, 2 and 3 have power good comparators that trip when the feedback pin is more than 8% above or below its reference voltage. Channel 4 has a power good comparator that indicates when the output voltage is more than 8% below its reference. The PG output pins are open-drain and pulled low when the corresponding output is out of regulation. The PG outputs are not valid until $INTV_{CC}$ rises to 2.7V.

Power-On Reset Timer

The LT8603 includes a power-on reset timer. The power-on reset timeout period is adjustable using an external capacitor on the CPOR pin as described in the Applications Information section. The timer is initiated when the POREN pin is higher than 1.2V. The output of the POR timer, the $\overline{RST}$ pin, is an open-drain output with a weak internal pull-up of 100k to approximately 2V. $\overline{RST}$ is held low until the expiration of the POR timer. The $\overline{RST}$ pin is only valid when the LT8603 is enabled and $INTV_{CC}$ is above 2.7V.

APPLICATIONS INFORMATION

SYSTEM ARCHITECTURE

The LT8603 combines three buck converters with a boost controller to provide a flexible system supply that can be configured to generate up to four regulated outputs. The 4 channels are independently powered and can be connected in a variety of ways. For example, the output of the boost may be used to supply the input voltage to the buck converters resulting in three tightly regulated outputs even when the boost input voltage falls below the regulated buck outputs such as occurs during an automotive cold crank scenario. Alternatively, if the boost controller is driven from a buck output or is configured as a SEPIC converter, the LT8603 provides up to four tightly regulated outputs.

V_{IN} Voltage Range

The minimum voltage at V_{IN} for the LT8603 internal circuitry and the buck converters to start is 3.1V, however, at least 4V is required for the boost controller and the $INTV_{CC4}$ regulator to start. The boost controller can be configured to supply V_{IN} and the PV_{IN} pins once it has started; after start-up the input voltage to the boost controller can go lower than 3V.

Enable and Undervoltage Lockout

The EN/UVLO pin can be used to to program a minimum system start voltage or an undervoltage lockout (UVLO) voltage. It has an internal threshold of 1.2V with 50mV hysteresis. The UVLO divider circuit is shown in Figure 1.

The UVLO threshold is given by:

$$V_{(UVLO)} = \frac{R_{UV1}+R_{UV2}}{R_{UV2}} \bullet 1.2V$$

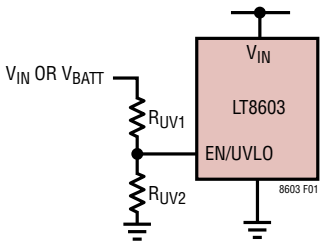


Figure 1. UVLO Divider

Switching Frequency

All 4 channels share a single oscillator. The buck channels switch at the oscillator frequency. The boost channel can switch at f_{OSC}, $f_{OSC}/2$ or $f_{OSC}/5$. The switching frequency range of all 4 channels should be determined before selecting the oscillator frequency. A low frequency usually provides better efficiency and a wider operating range due to lower switching losses and less sensitivity to timing constraints such as minimum on- and off-times. A high switching frequency uses smaller components and moves the switching noise away from sensitive frequency bands, such as the AM radio band, but does so at the cost of lower efficiency. A high switching frequency also decreases the duty cycle range because of finite minimum on- and off-times which are independent of the switching frequency.

The oscillator frequency can be programmed from 250kHz to 2.2MHz by tying a resistor from the RT pin to ground. Table 1 shows the necessary value of R_T for some common switching frequencies.

Table 1. Oscillator Frequency (f_{OSC}) vs R_T Value

OSCILLATOR FREQUENCY (MHz)	R_T (kΩ)
0.25	244
0.35	173
0.5	120
0.75	79.2
1.0	58.9
1.25	46.8
1.5	38.7
1.75	33.0
2.0	28.7
2.2	26.0

The following equation approximates the values shown in Table 1:

$$R_T = \frac{59.8}{(f_{OSC} - 0.007)} - 1.3$$

The RT pin is sensitive to noise so the resistor should be placed close to the LT8603 and away from noise sources.

APPLICATIONS INFORMATION

The internal oscillator of the LT8603 can be synchronized to an external clock of 250kHz up to 2.2MHz applied to the SYNC pin. The R_T value should be chosen such that the frequency set by R_T is close to the anticipated external clock frequency.

Mode Selection and Synchronization

To select low ripple Burst Mode operation, the SYNC pin should be connected to a voltage below 0.3V such as ground. To select pulse-skipping operation, connect the SYNC pin to an available voltage above 1.2V such as $INTV_{CC}$.

To synchronize the LT8603 to an external frequency, drive the SYNC pin with a pulse train with a high voltage above 1.2V and a low voltage below 0.3V. The minimum pulse width is 120ns for a high pulse and 90ns for a low pulse. The LT8603 will operate in pulse-skipping mode while synchronized to an external clock. The LT8603 may be synchronized over a 250kHz to 2.2MHz range. The R_T resistor should be chosen to set the LT8603 switching frequency close to the synchronization input.

For some applications it is desirable for the LT8603 to operate in pulse-skipping mode, offering two major differences from Burst Mode operation. First, in pulse-skipping mode the clock stays awake at all times and all switching cycles are aligned to the clock. Second, full frequency switching is reached at a lower output load in pulse-skipping than Burst Mode operation. These two differences come at the expense of increased quiescent current for pulse-skipping. To enable pulse-skipping mode, the SYNC pin is tied high either to a logic output or to the $INTV_{CC}$ pin. Do not leave the SYNC pin floating.

$INTV_{CC}$ Regulator

The $INTV_{CC}$ supplies the common circuitry such as the oscillator and reference but its main current demand comes from the gate drivers for the high voltage buck converters. The current draw will depend on the operating frequency, the higher the switching frequency, the greater the current drawn from $INTV_{CC}$. The regulator is supplied by V_{IN} at start-up, but it will draw its supply current from BIAS if BIAS is at least 3.1V. If the BIAS pin is connected to a switching regulator channel it will improve efficiency, reduce on-chip dissipation and lower the sleep current. The $INTV_{CC}$ may be used to configure other inputs and supply pull-ups related to the LT8603. It is not recommended to draw more than 1mA or connect $INTV_{CC}$ to any components not related to the LT8603 to avoid unexpected interactions.

BOOST CONTROLLER

Functional Description

Channel 4 is a set of functional elements that are connected to external components to form a boost converter. The Block Diagram in Figure 2 shows these elements and how they are connected internally.

The error amplifier compares a fractional part of the output voltage to an 800mV reference. The output, I_{LIM4}, goes to the current comparator to set the peak current.

The current comparator senses the inductor current using a small sense resistor across the ISP4 and ISN4 pins. The trip level is set by the error amplifier output, I_{LIM4}, and the slope compensation signal, SLOPE4. The maximum

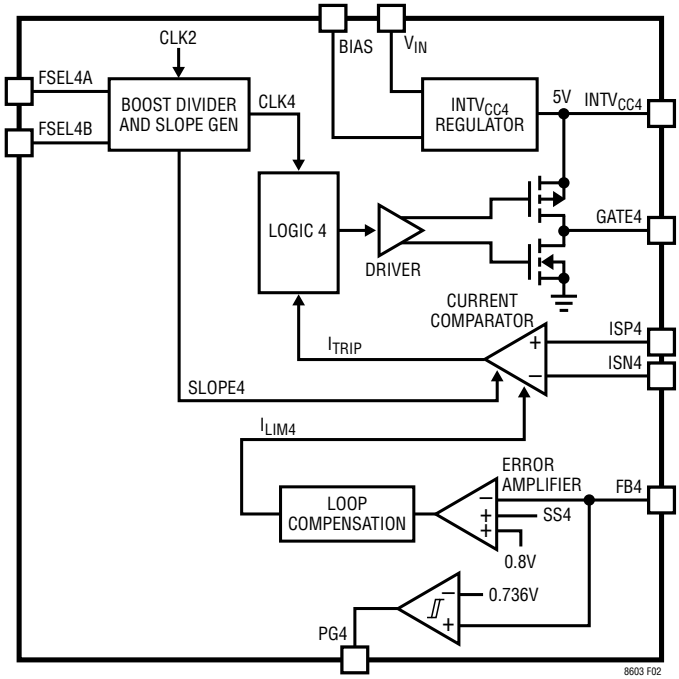


Figure 2. Boost Controller Block Diagram

APPLICATIONS INFORMATION

trip level is 50mV. ISP4 and ISN4 have an operational common range of 2V to 42V and an absolute maximum rating of ±42V. This allows reverse battery protection with a single diode in series with external MOSFET drain.

The logic block turns on the external MOSFET on a CLK4 signal, and then turns it off on an I_{TRIP} from the current comparator, or when maximum duty cycle is reached.

The LT8603 has a frequency divider that allows the controller switching frequency to be less than the oscillator frequency. The boost controller is specified for a f_{SW} between 250kHz and 2.2MHz; do not set the divider to operate the boost controller below 250kHz. The FSEL4A and FSEL4B pins control the oscillator frequency as shown in Table 2.

Table 2. Boost Frequency Selection

BOOST FREQ f_{SW4}	FSEL4A	FSEL4B
0 (Boost Shutdown)	Low	Low
$f_{OSC}/5$	High	Low
$f_{OSC}/2$	Low	High
f_{OSC}	High	High

The boost controller is enabled by the FSEL4A and FSEL4B pins. When both pins are low, the boost controller is shut down. When either or both pins are set high, a boost controller start-up sequence is initiated. During start-up, the $INTV_{CC4}$ regulator is turned on charging the external $INTV_{CC4}$ capacitor. Once $INTV_{CC4}$ reaches 4V, the controller logic is turned on and switching begins. A 1ms soft-start ramp is applied to the error amplifier to minimize inrush current.

The $INTV_{CC4}$ regulator is a low dropout, linear regulator that provides power to the GATE4 drive circuit. It is dedicated to the boost controller and is shut down when the boost controller is shut down. It can draw power from either V_{IN} or BIAS, depending on the BIAS voltage. When BIAS is less that 4.6V, the regulator will draw power from V_{IN} and regulate to 4.6V. When BIAS is greater than 4.6V but less than 5V, the regulator sets $INTV_{CC4}$ equal to BIAS and draws power from BIAS. When BIAS is greater than 5V, the regulator generates 5V and draws power from BIAS. Do not use the $INTV_{CC4}$ output for external circuitry.

A comparator senses when the output voltage is above 92% of the programmed value and generates a power good signal at the PG4 pin.

Setting the Output Voltage

The boost controller's output voltage is set by connecting the FB4 pin to a resistor divider from the output as shown in Figure 3.

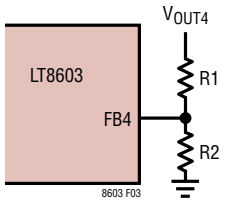


Figure 3. Feedback Resistor Divider

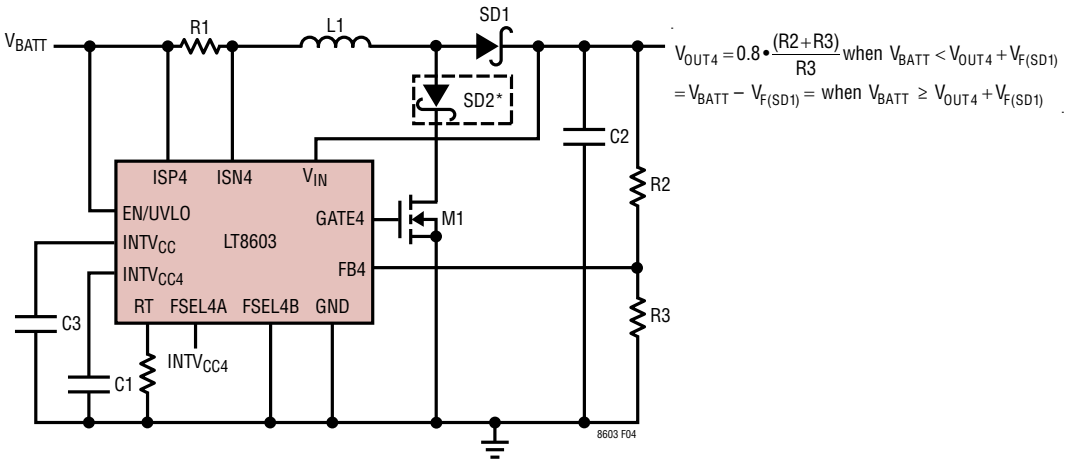
The value of R2 is best selected first as this establishes how much current is in the string based on $I = V_{FB4}/R2$ where V_{FB4} = 0.8V. The current should be chosen such that it is not influenced by anticipated leakage or noise. R1 can then be calculated from:

$$R1 = R2 \bullet ((V_{OUT4}/V_{FB4}) - 1)$$

Boost Configuration

The LT8603 boost controller configured as a standard boost regulator is shown in Figure 4. The boost controller output voltage is set by connecting FB4 to an external divider. For the following example, R2 and R3 are chosen such that OUT4 = 8V. If the battery voltage (V_{BATT}) is above 8V plus a diode forward voltage, the boost controller will be inactive consuming minimal quiescent current. If the battery voltage drops below 8V plus a diode forward voltage, such as during an automotive cold crank cycle, the boost controller will become active to maintain 8V at OUT4. With OUT4 connected to V_{IN}, the input supply must reach 4V plus the diode forward voltage to start.

APPLICATIONS INFORMATION



*SD2 IS FOR REVERSE INPUT PROTECTION. SHORT IF NOT NEEDED.

Figure 4. Channel 4 in Boost Configuration

Once started however, the LT8603 will maintain the output voltage at OUT4 with V_{BATT} as low as 2V. The ISP4 and ISN4 pins sense the inductor current for the current mode control loop across current sense resistor R1. The ISP4 and ISN4 pins will accurately sense the inductor current down to 2V and will tolerate negative voltages as large as –42V without damage.

By adding diode SD2 in series with the main switch transistor M1, the entire regulator will be tolerant of negative input supply voltages.

One of the limitations of the boost configuration is that it cannot provide short-circuit protection for the boost output as the diode always provides a DC current path from input to output. If short-circuit overload protection is required the SEPIC configuration should be considered. See the SEPIC Configuration section for more information on the SEPIC converter.

Boost: Duty Cycle and Max Switching Frequency

In continuous conduction mode (CCM), the operating duty cycle as a function of input and output voltage is given by:

$$D = \left(\frac{V_{OUT} + V_D - V_{BATT}}{V_{OUT} + V_D} \right)$$

where V_D is the forward voltage drop of the diode.

Thus the maximum duty cycle (D_{MAX}) in terms of the minimum V_{BATT} is:

$$D_{MAX} = \frac{V_{OUT} + V_D - V_{BATT(MIN)}}{V_{OUT} + V_D}$$

For a given input and output voltage, the switching frequency is limited by the expected maximum duty cycle, D_{MAX}, and minimum switch off time, $t_{OFF(MIN)}$. The $f_{SW(MAX)}$ at D_{MAX} is given by:

$$f_{SW(MAX)} = \frac{D_{MAX}}{t_{OFF(MIN)}}$$

Boost: Inductor and Sense Resistor Selection

The boost regulator inductor and sense resistor (R_{SENSE}) should be sized according to the maximum input current. The maximum input current will occur at the minimum input voltage (maximum duty cycle) and maximum output load.

The maximum average inductor current, which is equal to the average input current, can be calculated from:

$$I_{L(MAX)} = \frac{I_{OUT(MAX)}}{1 - D_{MAX}}$$

APPLICATIONS INFORMATION

From this the ripple current can be specified using:

$$\Delta I_L = \chi \bullet I_{L(MAX)} = \chi \bullet I_{OUT(MAX)} \bullet \frac{1}{1 - D_{MAX}}$$

where χ in the above equation represents the percentage peak-to-peak ripple current in the inductor relative to $I_{L(MAX)}$. Choosing the inductor ripple current, ΔI_L, has a direct impact on the choice of the inductor value and the converter's maximum output current capability. Choosing smaller values of ΔI_L increases the converter's output current capability but requires larger inductors. Choosing larger values of ΔI_L provides faster transient response and allows the use of smaller inductors but results in higher input current ripple, greater core losses, and lower output current capability. In addition, larger values of ΔI_L at high duty cycle may result in sub-harmonic oscillation. The typical range for χ is 20% to 40% though careful evaluation of system stability should be made to ensure adequate design margin. The peak inductor current will be the average inductor current plus half the ripple current. The LT8603 current sense comparator has a built-in current limit threshold of 50mV across ISP4 and ISN4 so the peak voltage across the sense resistor should be kept to no more than 80% of this or 40mV. Therefore, the value of R_{SENSE} should be:

$$R_{SENSE} = \frac{0.04}{I_{L(PEAK)}}$$

$I_{L(PEAK)}$ can be calculated from:

$$I_{L(PEAK)} = \left(1 + \frac{\chi}{2}\right) \bullet \frac{I_{OUT(MAX)}}{1 - D_{MAX}}$$

The inductor value to achieve the required ripple is given by following equation:

$$L = \frac{V_{BATT(MIN)}}{\Delta I_L \bullet f_{SW}} \bullet D_{MAX}$$

The inductor should have a saturation current exceeding the current limit value of:

$$I_{LIM} = \frac{0.05}{R_{SENSE}}$$

Finally, the ESR and magnetic loss of the inductor contribute to overall system power loss. For best efficiency, an inductor with low ESR and a core rated for the desired operating frequency should be chosen. The sense resistor should be chosen to have adequate power handling capability. The maximum power dissipation is given by:

$$P_{RSENSE} = \frac{0.05^2}{R_{SENSE}}$$

For example, a 4mΩ could dissipate up to 0.625W.

Boost: MOSFET Selection

For the boost configuration, the selected external MOSFET should have a BV_{DSS} rating exceeding, with margin, the larger of either the maximum input voltage or the boost output voltage plus a diode forward voltage. The maximum input voltage should include careful consideration of possible transient conditions. In addition, the chosen MOSFET should be compatible with the LT8603's nominal gate drive of 4.6V and have a low value of $R_{DS(ON)}$ for best efficiency. The current rating for the MOSFET must be greater than the peak inductor current. Finally, the maximum gate drive current required by the external MOSFET should not exceed the 40mA capability of the LT8603. The current drawn by the gate driver is given by:

$$I_{DRIVE} = Q_g \bullet f_{sw}$$

where Q_g is the MOSFET gate charge and f_{SW} is programmed switching frequency.

For example, if Q_g is 20nC and f_{SW} is 1MHz, the drive requirement is 20mA.

Boost: Diode Selection

In the boost converter, the rectifier diode, SD1, only conducts when the switch is off. The average diode current is equal to the output current. The peak current is equal to the peak inductor current and is given by:

$$I_{D(PEAK)} = \left(1 + \frac{\chi}{2}\right) \bullet \frac{I_{OUT(MAX)}}{1 - D_{MAX}}$$

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The power dissipated by the diode is given by:

$$P_D = I_{OUT(MAX)} \bullet V_D$$

Therefore, a rectifier diode should be chosen with a low forward voltage drop at peak current for best efficiency and a reverse breakdown voltage greater than $V_{OUT4(MAX)}$.

If the reverse protection diode (SD2) is needed, the reverse breakdown voltage must be greater than the desired reverse polarity protection.

Boost: Output Capacitor

The output capacitor has two essential functions. First, the output capacitor filters the LT8603's discontinuous output current to produce the DC output current. In this role, the capacitor determines the output ripple, thus low impedance at the switching frequency is important. Second, the output capacitor stores energy in order to satisfy transient load conditions and stabilize the LT8603's control loop. Typically, the low equivalent series resistance of X5R and X7R ceramic capacitors provide low output ripple and good transient response.

For some applications, transient performance can be improved with higher output capacitance and/or the addition of a feedforward capacitor placed between the boost output voltage and the boost feedback pin. Note that larger output capacitance may be required when lower switching frequencies are used or when there is significant inductance to the load due to long wire or cables. Increasing the output capacitance will also decrease the output ripple.

When choosing a capacitor, special attention should be given to the capacitor's data sheet to understand the effective capacitance under the relevant operating conditions of voltage bias and temperature. For good starting values, refer to the Typical Applications section. For all applications, careful evaluation of system stability should be made to ensure adequate design margin.

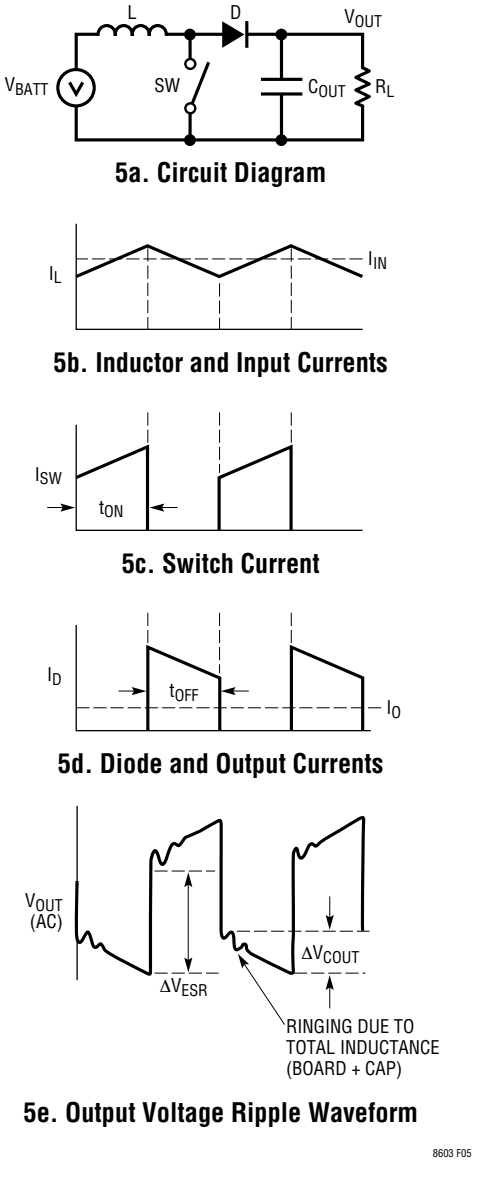

Figure 5. Switching Waveforms for a Boost Converter

Boost: Input Capacitor

The input capacitor is in series with the inductor so the input current waveform is continuous and the d_i/d_t is limited.

An input capacitor should be chosen to handle the RMS input capacitor ripple current as given by:

$$I_{RMS(CIN)} = 0.6 \bullet \chi \bullet I_{OUTMAX}$$

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Ensure that capacitors present at the input are rated to withstand any voltage transients that may be applied.

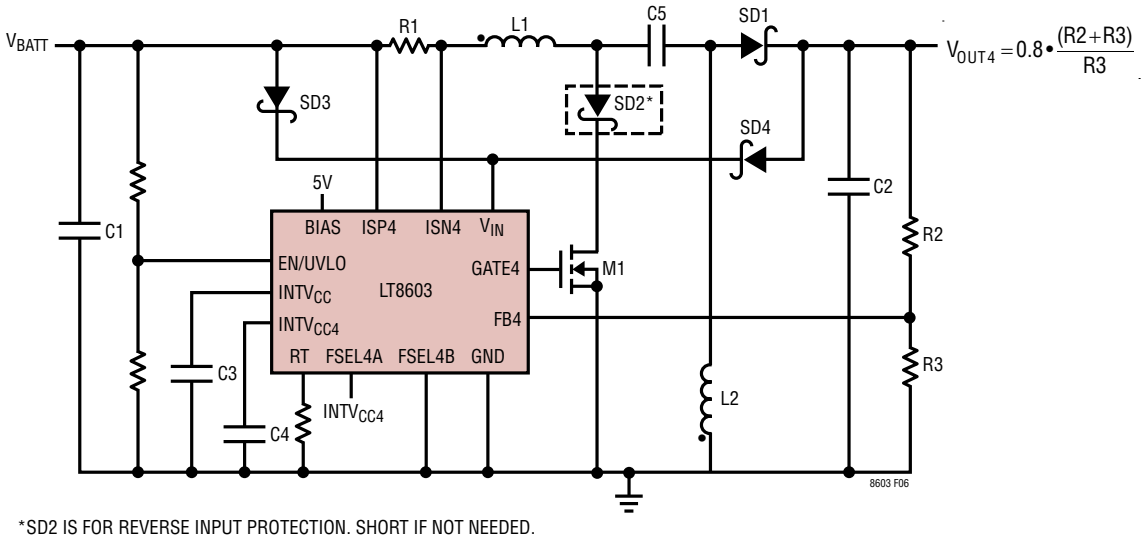
The value of input capacitance is a function of the source impedance. In general, the higher the source impedance, the higher the required input capacitance. The Typical Applications section provides reasonable starting values for input capacitance but careful evaluation of each application must be made to ensure adequate design margin.

SEPIC Configuration

Figure 6 shows the boost controller configured as a single-ended primary inductance converter or SEPIC. The SEPIC configuration offers two primary advantages over the standard boost configuration. First, it operates like a buck/boost which means it will regulate to an accurate output voltage for any input voltage. Second, it offers short-circuit protection and 0V output in shutdown since there is no DC path from the input to the output. The disadvantage is a more complex circuit requiring additional components as compared to a standard boost configuration. Since there is no DC path to the output, the LT8603 V_{IN} cannot be connected directly to the SEPIC output. As a result, diode SD3 is used to ensure start-up, and SD4 is used to ensure operation to low V_{BATT} once started. If V_{BATT} drops below 4V after the SEPIC is in regulation, SD4 maintains V_{IN} at the SEPIC output voltage. Just as with the standard boost configuration, optional diode SD2 provides reverse battery protection.

Figure 7 shows a simplified topology and the current flow for each of the switch positions once steady state is reached. Both inductors increase current during the switch on cycle (Figure 7b). The DC currents of L1 and L2 are not necessarily equal: $I_{L1(DC)}$ must be equal to $I_{VBATT(DC)}$ since there is no other DC path for the current flow from V_{BATT}. By the same argument, $I_{L2(DC)}$ must be equal to $I_{OUT(DC)}$. Figure 8 shows the current waveforms of the SEPIC converter.

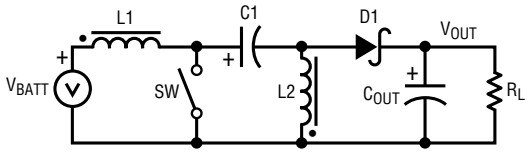
Although uncoupled inductors can be used in the SEPIC converter, coupled inductors provide several advantages and are preferred for most applications. Uncoupled inductors require double the inductance of the coupled inductors and two inductors at twice the inductance usually cost more than one coupled inductor. Also, uncoupled inductors form a tank with the coupling capacitor which can ring at very low frequencies. Uncoupled inductors can be an advantage, however, in high power or high duty cycle converters since the current is split between two cores.



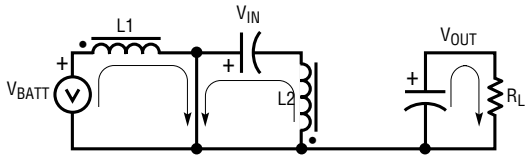
*SD2 IS FOR REVERSE INPUT PROTECTION. SHORT IF NOT NEEDED.

Figure 6. Channel 4 in SEPIC Configuration

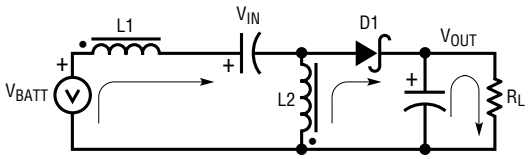
APPLICATIONS INFORMATION



7a. SEPIC Topology



7b. Current Flow During Switch On-Time



7c. Current Flow During Switch Off-Time

8603 F07

Figure 7. SEPIC Topology and Current Flow

SEPIC: Duty Cycle and Frequency

With the SEPIC configuration operating in continuous conduction mode (CCM), the duty cycle is given by:

$$D = \left(\frac{V_{OUT} + V_D}{V_{BATT} + V_{OUT} + V_D} \right)$$

The maximum switching frequency of the SEPIC converter is limited by both maximum and minimum duty cycles. The maximum duty cycle is set by $V_{BATT(MIN)}$. The maximum switching frequency, $f_{SW(MAX)}$ at $V_{BATT(MIN)}$ is given by:

$$f_{SW(MAX)@V_{BATT(MIN)}} = 1 - \frac{\left[\frac{V_{OUT} + V_D}{V_{BATT(MIN)} + V_{OUT} + V_D} \right]}{t_{OFF(MIN)}}$$

The minimum duty cycle is set by $V_{BATT(MAX)}$. The maximum switching frequency at $V_{BATT(MAX)}$ is given by:

$$f_{SW(MAX)@V_{BATT(MAX)}} = \frac{\left[\frac{V_{OUT} + V_D}{V_{BATT(MAX)} + V_{OUT} + V_D} \right]}{t_{ON(MIN)}}$$

The lower of these frequencies is the maximum switching frequency for the SEPIC converter.

SEPIC: Inductor and R_{SENSE} Selection

Choosing the inductor ripple current, ΔI_L, has a direct impact on the choice of the inductor value and the converter's maximum output current capability. Choosing smaller values of ΔI_L increases the converter's output current capability but requires larger inductors. Choosing larger values of ΔI_L provides faster transient response and allows the use of smaller inductors but results in higher input current ripple, greater core losses, and lower output current capability. In addition, larger values of ΔI_L at high duty cycle may result in sub-harmonic oscillation.

Given an operating input voltage range and operating frequency, the inductor value is given by:

$$L = \frac{V_{BATT(MIN)} \bullet D_{MAX}}{\Delta I_L \bullet f_{SW}}$$

where,

$$\Delta I_L = \frac{\chi \bullet I_{OUT(MAX)} \bullet D_{MAX}}{1 - D_{MAX}}$$

χ in the above equation represents the percentage peak-to-peak ripple current in the inductor relative to the maximum average inductor current. The typical range of χ is 20% to 40% though careful evaluation of system stability should be made to ensure adequate design margin.

For coupled inductors, L1 = L2 and the effective inductance is doubled due to the mutual inductance. The value of each equal winding is given by:

$$L1 = L2 = \frac{V_{BATT(MIN)} \bullet D_{MAX}}{2 \bullet \Delta I_L \bullet f_{SW}}$$

The maximum input current of the SEPIC converter is calculated at the minimum input voltage and full load current.

The peak inductor current can be significantly higher than the output current. The following equations assume CCM operation and calculate the maximum peak inductor current at minimum V_{BATT}:

APPLICATIONS INFORMATION

For a coupled inductor:

$$I_{L(PEAK)} = \left(1+\frac{\chi}{2}\right) \bullet I_{OUT(MAX)} \bullet \left(1+\frac{V_{OUT}+V_D}{V_{BATT(MIN)}}\right)$$

For uncoupled inductors:

$$I_{L1(PEAK)} = \left(1+\frac{\chi}{2}\right) \bullet I_{OUTMAX} \bullet \frac{V_{OUT}+V_D}{V_{BATT(MIN)}}$$

$$I_{L2(PEAK)} = \left(1+\frac{\chi}{2}\right) \bullet I_{OUT(MAX)} \bullet \frac{V_{BATT(MIN)}+V_D}{V_{BATT(MIN)}}$$

R_{SENSE} can then be calculated by:

$$R_{SENSE} = \frac{0.04}{I_{L1(PEAK)}}$$

The chosen inductor(s) should be rated for the maximum expected current.

SEPIC: MOSFET Selection

For the SEPIC configuration, the selected MOSFET should have a BVD_{SS} rating exceeding, with margin, the maximum input voltage plus the maximum output voltage plus the maximum diode forward voltage. The maximum input voltage should include careful consideration of possible transient conditions. In addition, the chosen MOSFET should be compatible with the LT8603's nominal gate drive of 4.6V and have a low value of $R_{DS(ON)}$ for best efficiency. The current rating for the MOSFET must be greater than the peak switch current of:

$$I_{SW(PEAK)} = \left(1+\frac{\chi}{2}\right) \bullet I_{OUT(MAX)} \bullet \frac{1}{1-D_{MAX}}$$

Finally, the maximum gate drive current required by the external MOSFET should not exceed the 40mA capability of the LT8603. The current drawn by the gate driver is given by:

$$I_{DRIVE} = Q_g \bullet f_{SW}$$

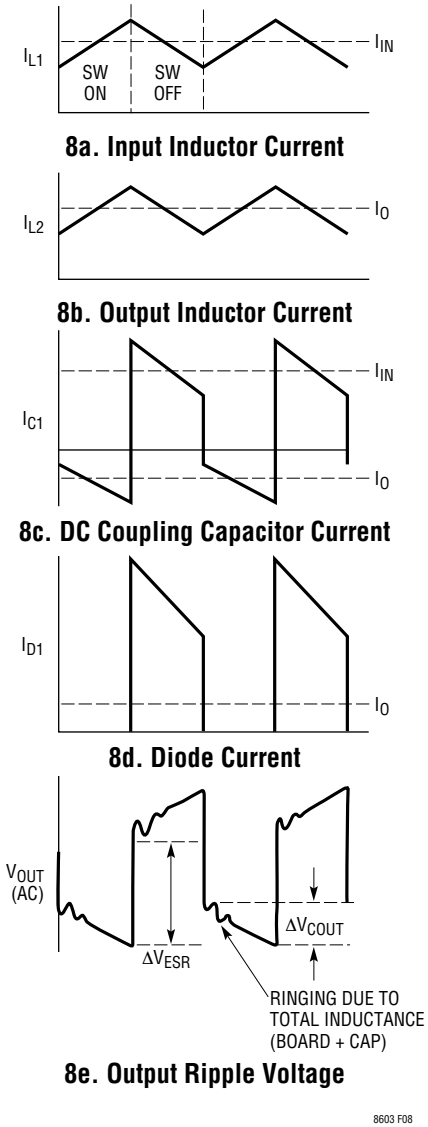


Figure 8. SEPIC Converter Switching Waveforms

SEPIC: Diode Selection

For the rectifier diode, SD1, the peak reverse voltage that the diode must withstand is:

$$V_{BATT(MAX)} + V_{OUT}$$

The average forward current is equal to the output current and the peak current is given by:

$$I_{D(PEAK)} = \left(1+\frac{\chi}{2}\right) \bullet I_{OUT(MAX)} \bullet \left(\frac{V_{OUT}+V_D}{V_{BATT(MIN)}}+1\right)$$

APPLICATIONS INFORMATION

The power dissipated by the diode is:

$$P_D = I_{OUT(MAX)} \bullet V_D$$

If the reverse protection diode, SD2, is needed, the peak reverse voltage must be greater than the maximum reverse polarity input expected. The average forward current is equal to the input current and the peak forward current is the same as for the rectifier diode above.

The start-up diodes, SD3 and SD4, have modest current requirements; the forward current will be less than 50mA under all input conditions. The peak reverse voltage on SD3 is the maximum reverse polarity input expected and the peak reverse voltage on SD4 is the maximum input voltage.

SEPIC: DC-Coupling Capacitor

The DC-coupling capacitor CC (C5 in Figure 6) sees a nearly rectangular current waveform as shown in Figure 8c. During the switch "off" time, the current through CC is approximately I_{IN}, and approximately $-I_{OUT}$ during the switch "on" time. This current ripple creates a triangular ripple voltage on CC:

$$\Delta V_{CC(P-P)} = \frac{I_{OUT(MAX)}}{CC \bullet f_{sw}} \bullet \frac{V_{OUT}}{V_{BATT} + V_{OUT} + V_D}$$

The maximum voltage on CC is then:

$$V_{CC(MAX)} = V_{BATT(MAX)} + \frac{\Delta V_{CC(P-P)}}{2}$$

which is typically close to $V_{BATT(MAX)}$. The ripple current through CC is:

$$I_{RMS(CC)} = I_{OUT(MAX)} \bullet \sqrt{\frac{V_{OUT} + V_D}{V_{BATT(MIN)}}}$$

The capacitance value should be chosen large enough that $\Delta V_{CC(P-P)}$ is less than 10% of $V_{BATT(MIN)}$. If $\Delta V_{CC(P-P)}$ is small then the voltage rating is close to $V_{BATT(MAX)}$.

SEPIC: Output Capacitor

The output capacitor has two essential functions. First, the output capacitor filters the LT8603's discontinuous output current to produce the DC output current. In this role, the capacitor determines the output ripple, thus low impedance at the switching frequency is important. Second, the output capacitor stores energy in order to satisfy transient load conditions and stabilize the LT8603's control loop. Typically, the low equivalent series resistance of X5R and X7R ceramic capacitors provide low output ripple and good transient response.

For some applications, transient performance can be improved with higher output capacitance and/or the addition of a feedforward capacitor placed between the output voltage and the feedback pin. Note that larger output capacitance may be required when lower switching frequencies are used or when there is significant inductance to the load due to long wire or cables. Increasing the output capacitance will also decrease the output ripple.

When choosing a capacitor, special attention should be given to the capacitor's data sheet to understand the effective capacitance under the relevant operating conditions of voltage bias and temperature. For good starting values, refer to the Typical Applications section. For all applications, careful evaluation of system stability should be made to ensure adequate design margin.

SEPIC: Input Capacitor

The input capacitor is in series with the inductor so the input current waveform is continuous and the d_i/d_t is limited.

An input capacitor should be chosen to handle the RMS input capacitor ripple current as given by:

$$I_{RMS(CIN)} = 0.3 \bullet \frac{V_{BATT(MIN)}}{L \bullet f_{sw}} \bullet D_{MAX}$$

Ensure that capacitors present at the input are rated to withstand any voltage transients that may be applied.

APPLICATIONS INFORMATION

The value of input capacitance is a function of the source impedance. In general, the higher the source impedance, the higher the required input capacitance. The Typical Applications section provides reasonable starting values for input capacitance but careful evaluation of each application must be made to ensure adequate design margin.

BUCK REGULATORS

Setting the Output Voltages

The output voltages of the buck channels are set with a resistor divider from the output to the related FBx pin as shown in Figure 9.

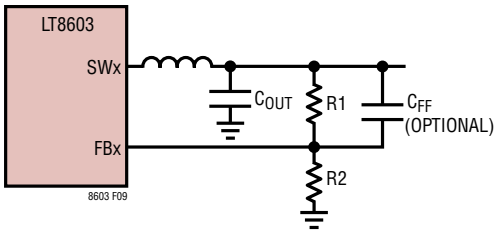


Figure 9. Feedback Resistor Divider

The value of R2 is best selected first as this establishes how much current is in the string based on $I = V_{FB}/R2$ where V_{FB} = 1.0V for the high voltage channels and 0.8V for the low voltage channel. The current should be chosen such that it is not influenced by anticipated leakage or noise. R1 can then be calculated from:

$$R1 = R2 \bullet \left(\frac{V_{OUTx}}{V_{FB}} - 1 \right)$$

C_{FF} can optionally be used to improve the transient response and stability of the internally compensated feedback loops. The values shown in the Typical Applications section will provide a good starting point for selecting CFF though careful evaluation of regulator stability should be made to ensure adequate design margin.

Buck: Operating Frequency and Input Voltage Range

Each buck regulator's respective minimum on-time, $t_{ON(MIN)}$, and minimum off-time, $t_{OFF(MIN)}$, impose limitations on the achievable duty cycle range and operating frequency. For buck regulators, the duty cycle is given by:

$$D = \frac{V_{OUT}}{PV_{IN}}$$

Further, the minimum duty cycle achievable at a given operating frequency is given by:

$$D_{MIN} = t_{ON(MIN)} \bullet f_{SW}$$

where f_{SW} is the programmed operating frequency.

The maximum duty cycle achievable at a given operating frequency is given by:

$$D_{MAX} = 1 - (t_{OFF(MIN)} \bullet f_{SW})$$

Combining these equations, the minimum PV_{IN} voltage allowed while regulating at full frequency is:

$$PV_{INx(MIN)} = \frac{V_{OUTx}}{1 - (t_{OFF(MIN)} \bullet f_{SW})}$$

and the maximum PV_{IN} voltage allowed while regulating at full frequency is:

$$PV_{INx(MAX)} = \frac{V_{OUTx}}{t_{ON(MIN)} \bullet f_{SW}}$$

If the $PV_{IN(MAX)}$ given above is exceeded during regulation, the buck regulator will skip switch-on cycles and no longer maintain the programmed operating frequency.

Buck: Inductor Selection

Inductor selection involves inductance, saturation current, series resistance (DCR) and magnetic loss.

A good starting point for choosing inductor values is:

$$L = \frac{1.05 \bullet (V_{OUTx} + V_{BOTx})}{f_{SW}} \text{ for Channels 1 and 3}$$

and

$$L = \frac{0.70 \bullet (V_{OUTx} + V_{BOTx})}{f_{SW}} \text{ for Channel 2}$$

APPLICATIONS INFORMATION

where V_{OUTx} is the output voltage for the corresponding channel, V_{BOTx} is the voltage across the bottom switch for the corresponding channel, f_{SW} is the switching frequency in MHz, and L is in µH.

Once the inductance is selected, the inductor current ripple and peak current can be calculated as:

$$\Delta I_{Lx} = \frac{V_{OUTx}}{Lx \bullet f_{SW}} \bullet \left(1 - \frac{V_{OUTx}}{PV_{INx(MAX)}}\right)$$

$$I_{Lx(PEAK)} = I_{OUTx(MAX)} + \frac{\Delta I_{Lx}}{2}$$

where $PV_{INx(MAX)}$ is the maximum input voltage for each channel in a given application and $I_{OUTx(MAX)}$ is the maximum output current for each channel in a given application. To avoid overheating and poor efficiency, an inductor must be chosen with an RMS current rating that is greater than the maximum expected output load of the application. In addition, the saturation current rating of the inductor must be higher than the load plus half the ripple current. Finally, for best efficiency the inductor series resistance should be as small as possible, and the core material should be intended for the application switching frequency.

The optimum inductor for a given application may differ from the one indicated by this design guide. Careful evaluation of the application circuit should be completed with the chosen inductor to ensure adequate design margin.

Buck: Shorted Output Protection

If the bottom MOSFET current exceeds the valley current limit at the start of a clock cycle, the top MOSFET is kept off until the overcurrent situation clears. This prevents the buildup of inductor current during a shorted output condition. Further, during overload or short-circuit conditions, the LT8603 safely tolerates operation with a saturated inductor.

Buck: Input Capacitor Selection

Step-down converters draw current from the input supply in pulses with very fast rise and fall times. An input capacitor is required to reduce the resultant voltage ripple at the input and minimize EMI. For this function, a ceramic X7R or X5R bypass capacitor should be placed between each buck channel's PV_{IN} pin and ground. To be most effective, the input capacitor must have low impedance at the switching frequency and an adequate ripple current rating.

The worst case ripple current occurs when V_{OUT} is one-half PV_{IN}. Under this condition, the ripple current is:

$$I_{CIN(RMS)} = \frac{I_{OUT}}{2}$$

Reasonable starting values for the input capacitor are:

4.7µF for Channels 1 and 3

10µF for Channel 2

A word of caution is in order regarding the use of ceramic capacitors at the input. A ceramic input capacitor can combine with stray inductance to form a resonant tank circuit back to the supply. If power is applied quickly (for example by plugging the circuit into a live power source), this tank can ring, as much as doubling the input voltage. The solution is to either clamp the input voltage or dampen the tank circuit by adding a lossy capacitor in parallel with the ceramic capacitor. For details see Analog Devices Application Note 88.

Buck: Output Capacitor Selection

The output capacitor performs two functions. First, it filters the inductor current to generate an output with low voltage ripple. Second, it stores energy to minimize droop and overshoot during transient loads. Because the LT8603 buck converters are able to operate at a high frequency, minimal output capacitance is necessary. The internally compensated current mode control loops are stable without requiring a minimum series resistance (ESR) in the output capacitor. Therefore ceramic capacitors may be used and will result in very low output ripple.

You can estimate output ripple with the following equations as appropriate:

$$V_{RIPPLE} = \frac{\Delta I_L}{8 \bullet f_{SW} \bullet C_{OUT}}, \text{for ceramic}$$

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$$V_{RIPPLE} = \Delta I_L \bullet ESR, \text{ for aluminum or tantalum}$$

where V_{RIPPLE} is the peak-to-peak output ripple, f_{SW} is the switching frequency, ΔI_L is the peak-to-peak ripple current in the inductor, C_{OUT} is the output capacitor value in µF and ESR is the output capacitor series resistance.

The low ESR and small size of ceramic capacitors make them the preferred type for LT8603 applications. However, not all ceramic capacitors are the same. Many of the higher value capacitors use dielectrics with high temperature and voltage coefficients. In particular Y5V and Z5U types lose a large fraction of their capacitance with applied voltage and at temperature extremes. Because loop stability, transient response ripple and EMI depend on the value of the input and output capacitors it is best to use X5R (max 85°C), X7R (max 125°C), or X8R (max 150°C) capacitors depending on the operating temperature range.

Electrolytic capacitors are also an option. The ESRs of most aluminum electrolytic capacitors are too large to deliver low output ripple. Tantalum, as well as newer, lower ESR organic electrolytic capacitors intended for power supply use are suitable. Choose a capacitor with a low enough ESR for the required output ripple. Because the volume of the capacitor determines its ESR, both the size and value will be larger than a ceramic capacitor that would give similar ripple performance. One benefit is that larger capacitance may give better transient response for large changes in load current.

The Typical Applications section provides a reasonable starting point for output capacitor values. Note, for applications that intend to operate near minimum on-time, larger output capacitance values may be required to minimize output voltage ripple. Careful evaluation of each application must be made to ensure adequate design margin.

Buck: Boost Capacitor Selection

The high voltage channels require a voltage above PV_{IN} to drive the gates of the top NFET switches. Connecting a capacitor between each channel's BST and SW pins creates this voltage with an approximate value of 3.3V. For most applications, a 0.1µF ceramic capacitor is a good choice.

Buck: RUN, Soft-Start, Tracking

In addition to the global EN/UVLO pin that controls the entire chip, each channel has its own independent control pin or pins.

The low voltage channel has a RUN pin with a fixed internal threshold of 1.2V. When the RUN pin exceeds 1.2V, a soft start is initiated which brings the low voltage channel into regulation in approximately 1.0ms.

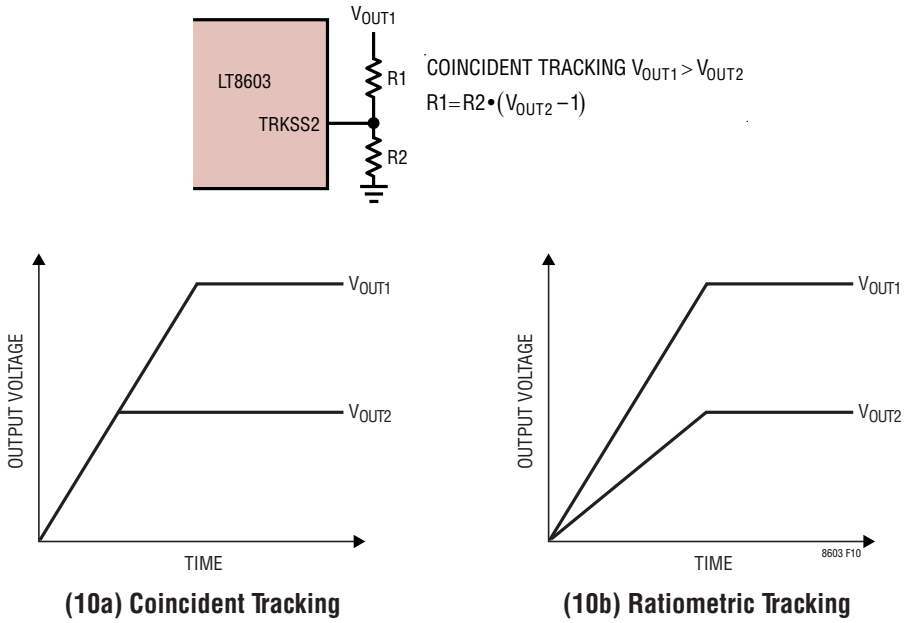
Channel 1 and Channel 2 have dual purpose TRKSSx control pins which can be used to ramp each output in a controlled way. Each channel's feedback pin voltage will regulate to the lower of the corresponding TRKSS pin and the internal 1V reference. These pins can therefore provide output voltage tracking. In addition, there is an internal constant current pull-up of 2.4µA at each TRKSS pin that can be used to charge an external capacitor to provide a programmable output soft-start function. The soft-start ramp time can be calculated from:

$$t_{SS} = C_{TRKSS} \bullet \frac{1V}{2.4\mu A}$$

The TRKSSx pin is pulled down through approximately 330Ω. It will be pulled down if temperature protection is activated.

To achieve coincident tracking, connect a resistor divider from the controlling output to the TRKSS pin of the slave output. Figure 10 shows the divider required for Channel 2 to track V_{OUT1}. With this circuit, R1 and R2 values should be chosen to minimize the offset from the 2.4µA pull-up current. To achieve ratiometric tracking, connect both TRKSS1 and TRKSS2 to a single capacitor to ground. Figure 10 shows the output waveforms for both coincident and ratiometric tracking. Note: Pulling TRKSS1 and TRKSS2 to ground does not guarantee the respective channel will never display a switching cycle.

APPLICATIONS INFORMATION



(10a) Coincident Tracking **(10b) Ratiometric Tracking**

Figure 10. Tracking Output Waveforms

Buck: Burst Mode Operation

With the SYNC pin held low to select Burst Mode operation, the LT8603 will automatically transition to Burst Mode at light load for best efficiency. In Burst Mode operation, most of the circuits are shut down between switch-on bursts to minimize power loss. If at least one channel remains full frequency, the oscillator remains on and all bursts are synchronized to the appropriate phase of the oscillator. If all channels go into Burst Mode operation, the oscillator will also shut off between bursts with a further savings in power. Because the channels of the LT8603 may have different loads, channels can have different switching frequencies when in Burst Mode operation.

GENERAL FUNCTIONS

General: Power Good Comparators

Each LT8603 channel has a power good comparator with an open drain output pin, PGx. For the buck channels, each PG pin is pulled low when the corresponding feedback voltage is either above or below its reference voltage by more than 8%. The boost channel's PG pin is pulled low when its feedback voltage is below its reference voltage by more than 8%. See the Electrical Characteristics table for more information on each channel's power good thresholds. Note, the PG outputs are not valid until $INTV_{CC}$ rises above 2.7V.

General: Power-On Reset Timer

The LT8603 provides a programmable reset timer. The POREN pin is the enable for the reset timer and includes a 1µA internal pull-up. Once enabled, the reset timer begins an internal clock counter that terminates after 64 cycles. Upon counter termination, the $\overline{RST}$ open-drain pull-down releases allowing the pin to transition high. The $\overline{RST}$ output includes a weak, 100k, internal pull-up resistor to approximately 2V.

The power-on reset timeout period, $t_{\overline{RST}}$, can be programmed by connecting a capacitor, C_{POR}, between the CPOR pin and ground. The value of $t_{\overline{RST}}$ is calculated by:

$$t_{RST} = 35.2 \bullet C_{POR}$$

where C_{POR} is in pF and $t_{\overline{RST}}$ is in microseconds. For example, using a capacitor value of 8.2nF gives a 289ms reset timeout period. The accuracy of $t_{\overline{RST}}$ will be determined

APPLICATIONS INFORMATION

by several factors including the accuracy and temperature coefficient of the capacitor CPOR, parasitic capacitance on the CPOR pin and board trace, and system noise. It is not recommended to use capacitor values greater than 10nF for best accuracy. Figure 11 shows the power-on reset timing.

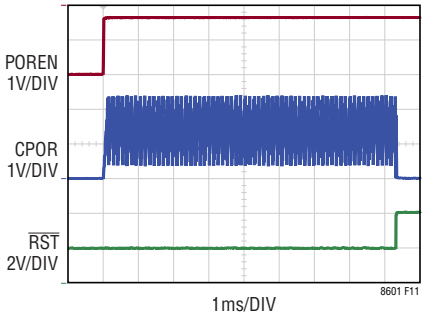


Figure 11. Power-On Reset Timing

General: Sequencing

The LT8603 provides flexibility in sequencing each channel's output including a power-on reset timer. Each channel has a power good output (PG1 to PG4) and input control pin or pins (TRKSS1, TRKSS2, RUN3, FSEL4A, and FSEL4B). The POR has a control input (POREN) and a reset output ($\overline{RST}$). All 5 outputs are open-drain. A sequencing example is shown in Figure 12.

In this example, Channel 4 starts first and soft-starts internally. When Channel 4 reaches regulation, Channels 1 and 2 start up and ramp according to $R1/C_{TRKSSx}$. Once both V_{OUT1} and V_{OUT2} reach regulation, Channel 3 starts. When OUT3 is in regulation, then the POR timer is started.

PCB LAYOUT

For proper operation and minimum EMI, care must be taken during printed circuit board layout. A recommended board layout is available with the latest LT8603 demo board. Some general guidelines are available in the remainder of this section.

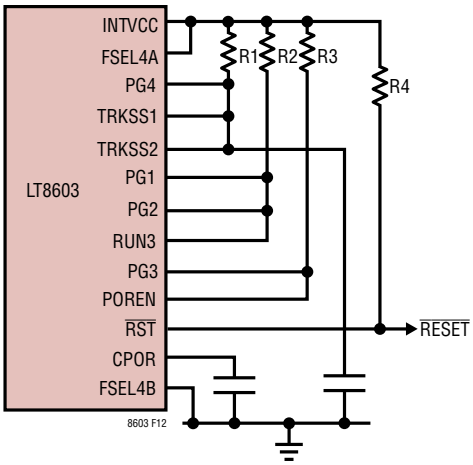


Figure 12. Sequencing the Outputs and POR

For each buck regulator, the current loop formed by the input capacitor has the highest di/dt and should be made as small as possible by placing the input capacitor close to the PV_{IN} pin and the adjacent GND pin. When using a physically large input capacitor, the resulting loop may be larger than optimum. In this case using a small case/value capacitor placed close to the PV_{IN} and GND pins plus a larger capacitor further away is preferred. These components, along with the inductor and output capacitor, should be placed on the same side of the circuit board, and their connections made on that layer.

The boost controller output loop, including the diode and output capacitor components, has the highest di/dt. As a result, the loop involving the diode and output capacitor should be kept as small as possible.

Place a local, unbroken ground plane under the application circuit on the layer closest to the surface layer. The SW and BST nodes should be made as small as possible to minimize noise coupling to sensitive traces. Minimize traces connecting to the RT and all FB pins and provide ground shielding as needed to minimize noise coupling to these sensitive nodes.

The exposed pad on the bottom of the package must have a good electrical and thermal connection to the board ground. For best performance, maximize board ground planes and thermal vias under and near the part.

APPLICATIONS INFORMATION

The recommended layer use for a 4-layer board is:

Layer 1 (Components): use 2oz (70µm) copper. Unbroken high frequency/high current routing. (C_{IN} loop, SW node, BST node, inductor, C_{OUT}), high current DC routing, ground plane fill.

Layer 2 (Internal): Unbroken ground plane.

Layer 3 (Internal): Signal routing, ground plane on remainder.

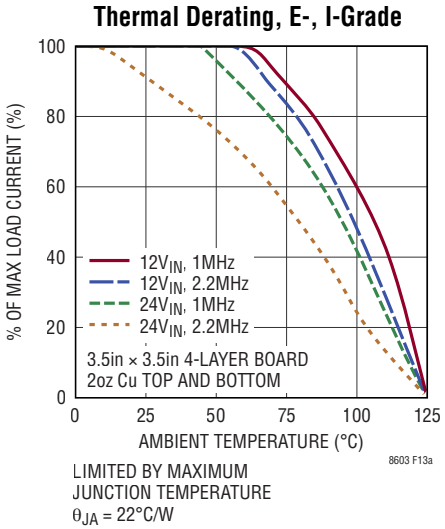
Layer 4 (Bottom): Use 2oz (70µm) copper; high current DC routing (PV_{IN}, V_{OUT}), ground plane on remainder.

THERMAL CONSIDERATIONS

The exposed pad is the main path for conducting heat from the silicon die to the PC board and the surrounding air. Thermal vias should be placed under the device to conduct heat down to internal ground planes and the back side of the board. Multiple small vias work better than a few large ones as copper is a much better conductor than any solder which may or may not fill them. The planes will distribute heat over a larger area and thus reduce the thermal resistance from the package to the air. A good design can achieve an effective θ_{JA} of 22°C/W. Power dissipation within the LT8603 can be estimated by summing the power dissipated in each channel. Calculate each channel's power loss from an efficiency measurement and subtract external component losses such as inductors, power transistors, and diodes. The die temperature is calculated by multiplying the total LT8603 power dissipation by the thermal resistance from junction to die θ_{JA} and adding the ambient temperature. The maximum load current should be derated as the ambient temperature approaches the maximum junction rating. Figure 13 shows the current derating factor to avoid exceeding the maximum junction temperature.

The thermal derating curves of Figure 13 are based on the front page application (Ch 1: 5V, Ch 2: 3.3V, Ch 3: 1.2V, Ch4: 8V). The currents decrease uniformly as a percentage of maximum. Although application dependent, this set of curves is representative of typical applications. Final current derating should be based on temperature measurements in the final application and environment.

The LT8603 will stop switching if the internal temperature rises too high. This thermal protection is above the maximum reliable operating temperature and is intended as a failsafe only.



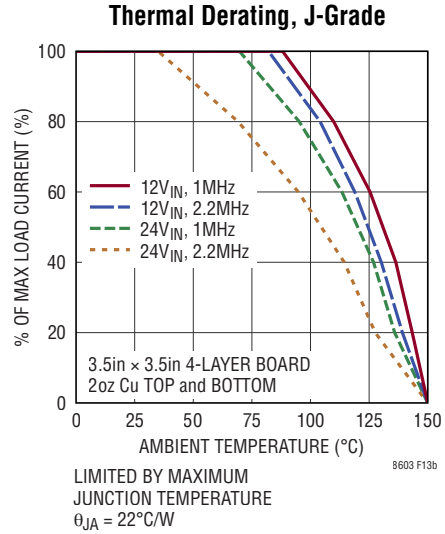
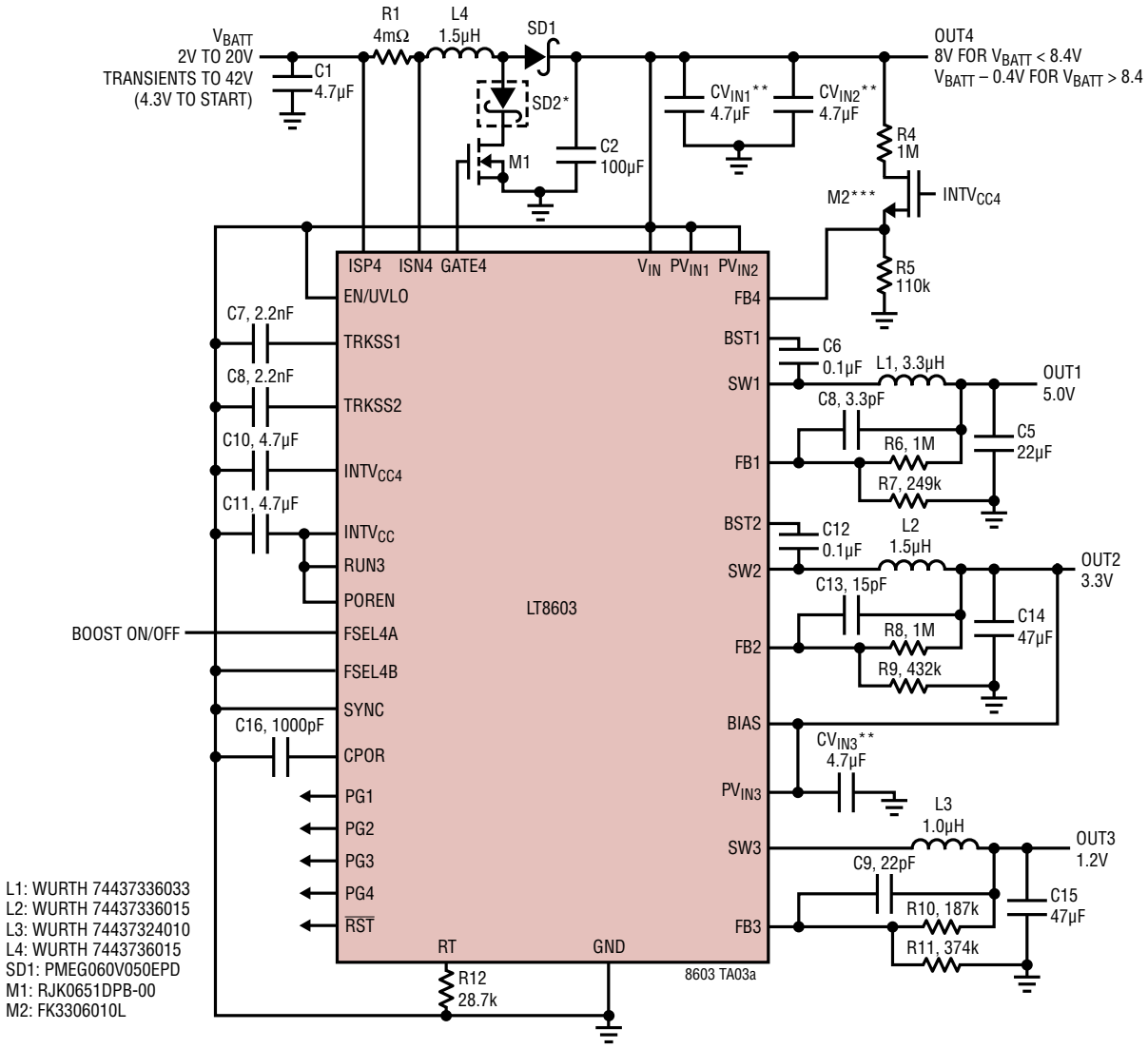


Figure 13. Thermal Derating, E-, I-, and J-Grade

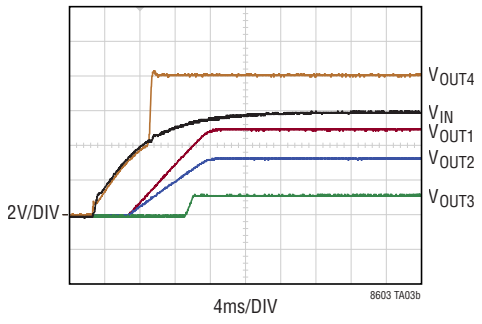
TYPICAL APPLICATIONS

Details of Front Page Application



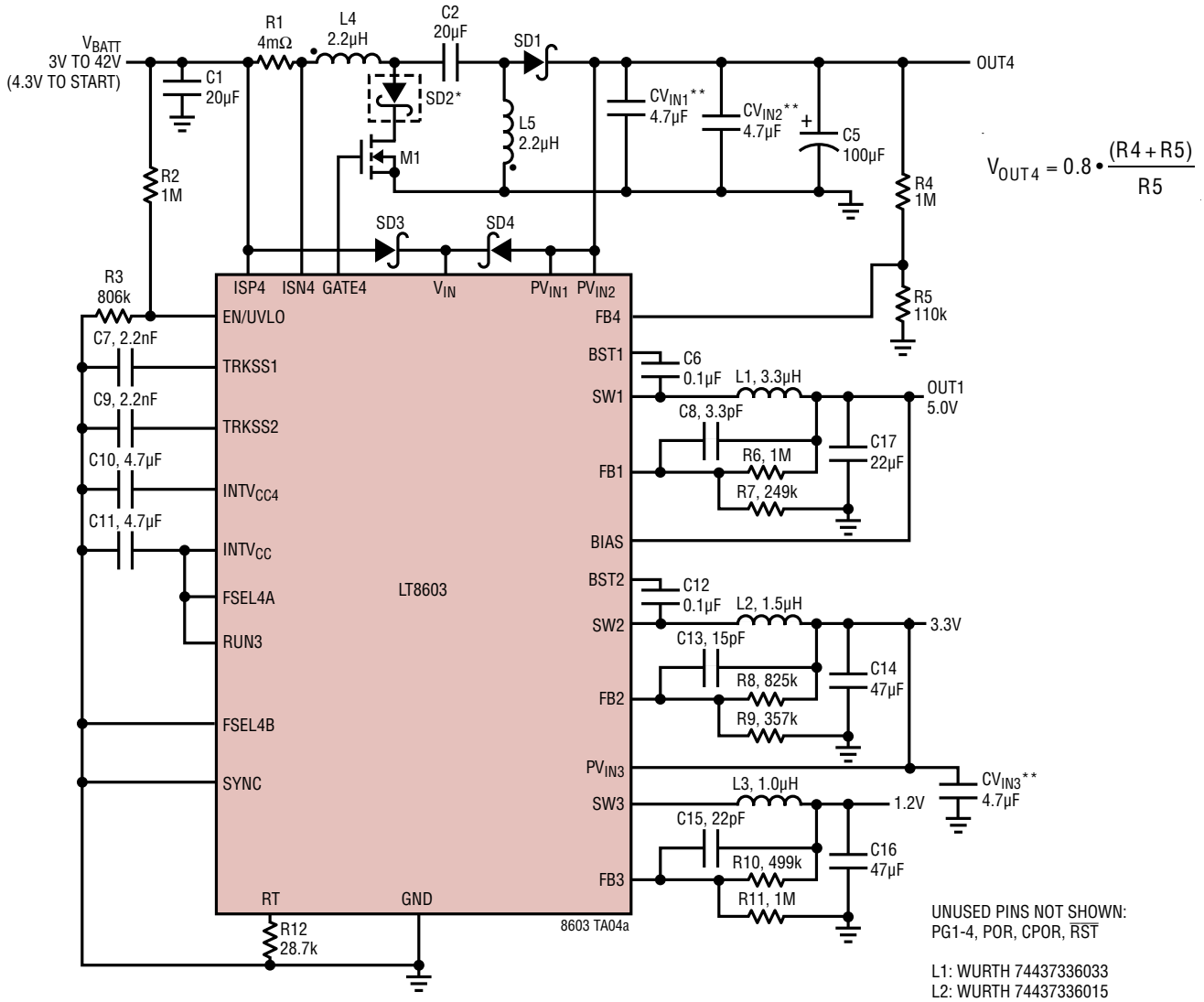
*SD2 OPTIONALLY PROVIDES REVERSE BATTERY PROTECTION. REPLACE WITH SHORT IF REQUIRED.
**CV_{IN1}, CV_{IN2}, AND CV_{IN3} SHOULD BE PLACED AS CLOSE AS POSSIBLE TO THEIR RESPECTIVE PV_{IN} PINS.
*** M2 IS RECOMMENDED FOR LOWEST QUIESCENT CURRENT WHEN CHANNEL 4 IS INACTIVE

Start-Up Sequence



TYPICAL APPLICATIONS

Four Regulated Outputs with Channel 4 Configured as a SEPIC



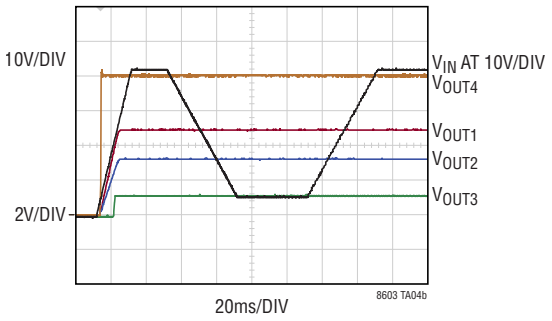
$$V_{OUT4} = 0.8 \bullet \frac{(R4 + R5)}{R5}$$

UNUSED PINS NOT SHOWN:
PG1-4, POR, CPOR, $\overline{RST}$

L1: WURTH 74437336033
L2: WURTH 74437336015
L3: WURTH 74437324010
L4: WURTH 74485540220
SD1: PMEG060V050EPD
M1: BSZ067N06LS3

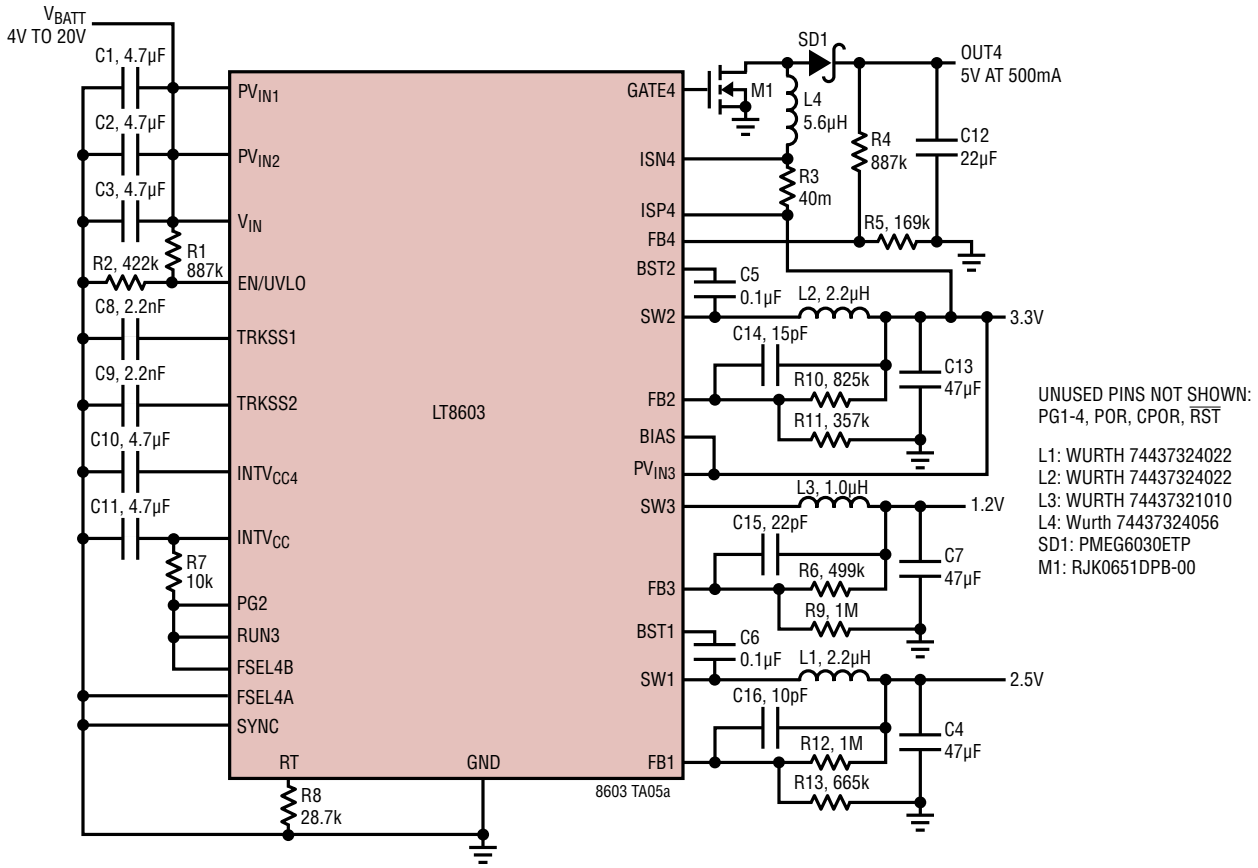
*SD2 OPTIONALLY PROVIDES REVERSE BATTERY PROTECTION. REPLACE WITH SHORT IF NOT REQUIRED. SD3 ENSURE START-UP. SD4 MAINAINS V_{IN} AT V_{BATT} < 4V.
**CV_{IN1}, CV_{IN2}, AND CV_{IN3} SHOULD BE PLACED AS CLOSE AS POSSIBLE TO THEIR RESPECTIVE PV_{IN} PINS.

Start-Up Sequence



TYPICAL APPLICATIONS

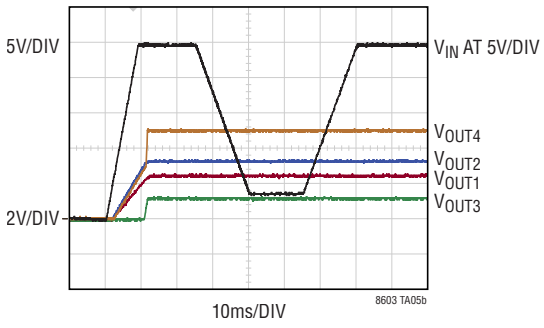
Four Regulated Outputs with Channel 4 Driven from Channel 2



UNUSED PINS NOT SHOWN:
PG1-4, POR, CPOR, $\overline{RST}$

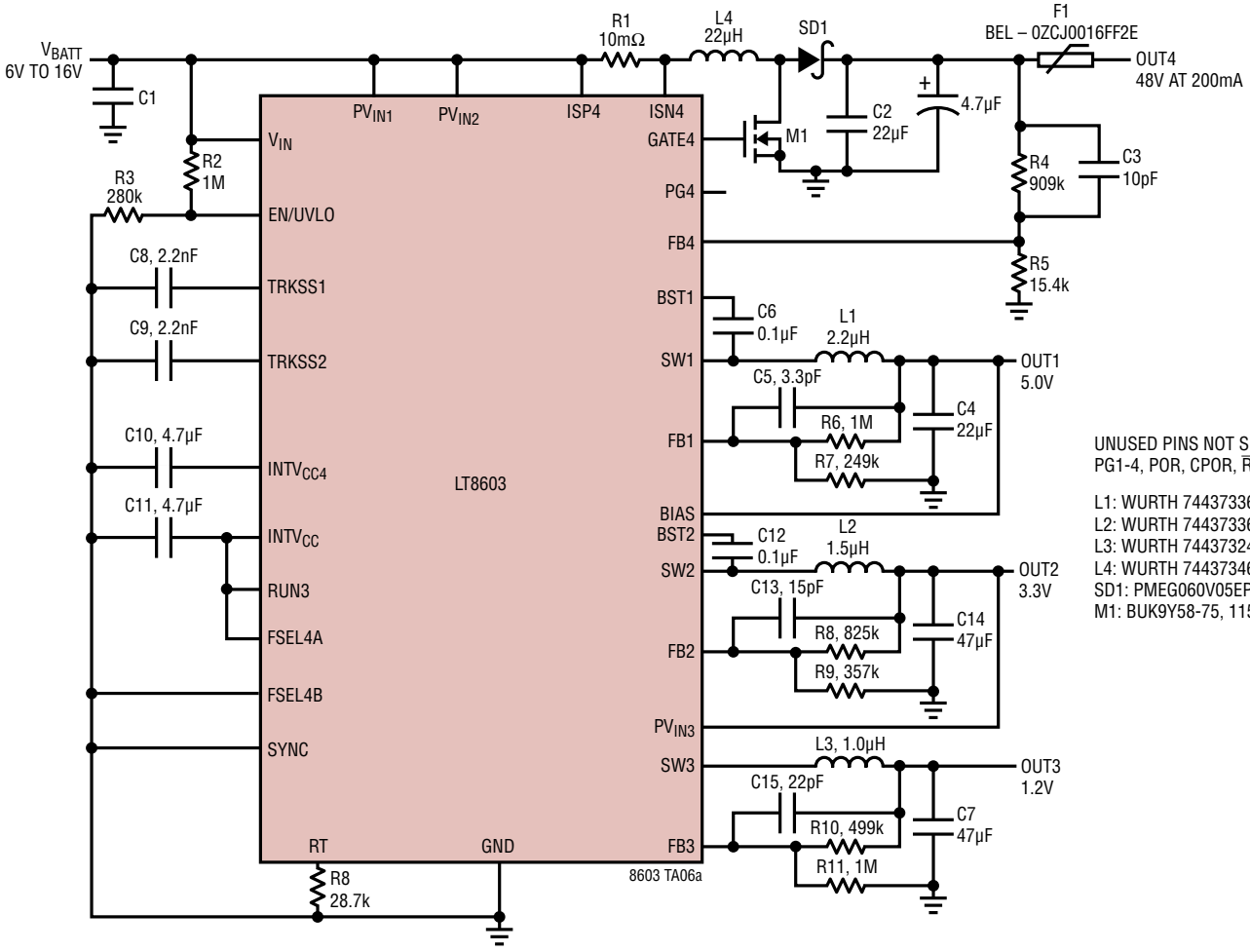
L1: WURTH 74437324022
L2: WURTH 74437324022
L3: WURTH 74437321010
L4: Wurth 74437324056
SD1: PMEG6030ETP
M1: RJK0651DPB-00

Start-Up Sequence



TYPICAL APPLICATIONS

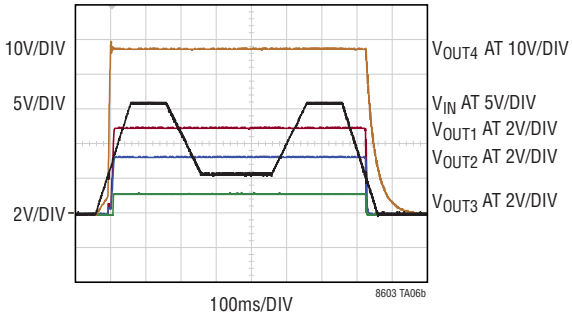
Four Regulated Outputs with Channel 4 Providing 48V Output



UNUSED PINS NOT SHOWN:
PG1-4, POR, CPOR, $\overline{RST}$

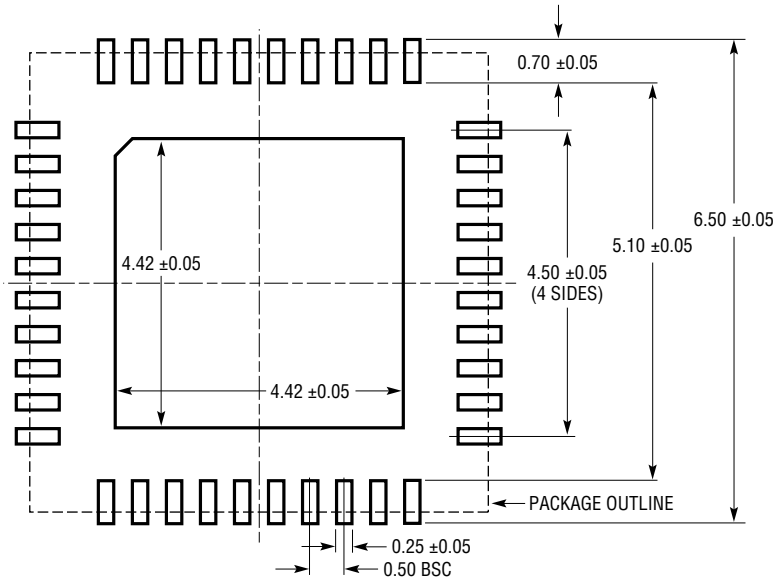
L1: WURTH 74437336022
L2: WURTH 74437336015
L3: WURTH 74437324010
L4: WURTH 74437346220
SD1: PMEG060V05EPD
M1: BUK9Y58-75, 115

Start-Up Sequence

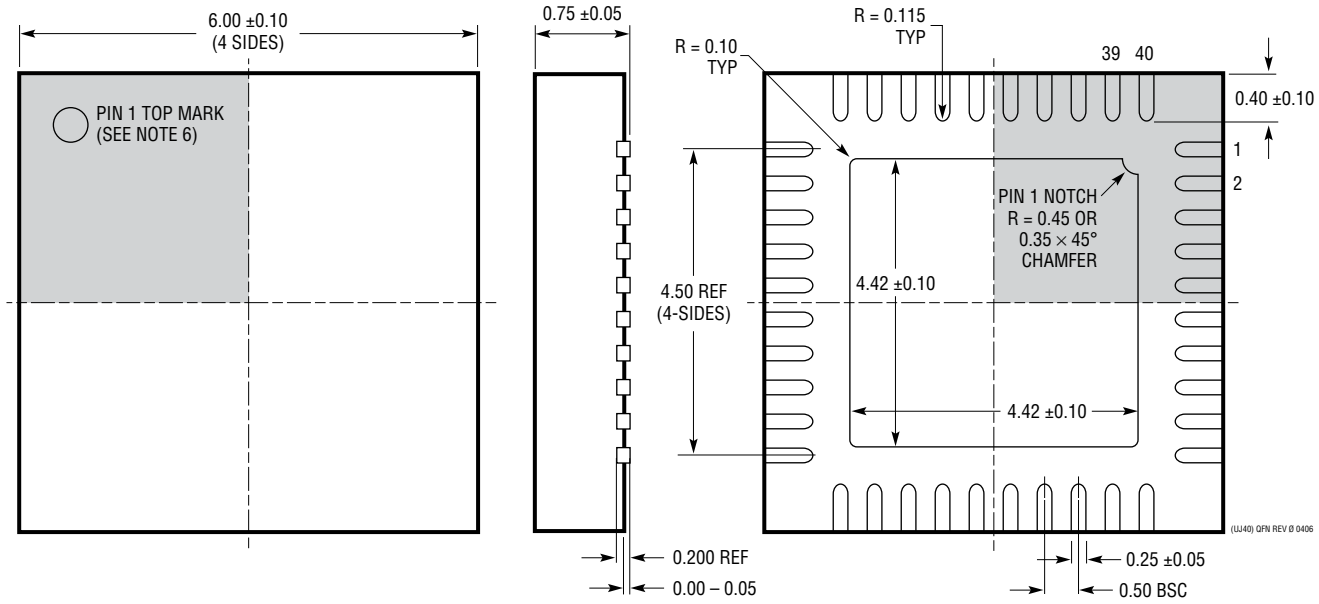


PACKAGE DESCRIPTION

UJ Package
40-Lead Plastic QFN (6mm × 6mm)
(Reference LTC DWG # 05-08-1728 Rev Ø)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING IS A JEDEC PACKAGE OUTLINE VARIATION OF (WJJD-2)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE
   MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE, IF PRESENT
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	09/19	Added AECQ-100 under Features.	1
		Added LT8603J under Absolute Maximum Ratings section.	2
		Added LT8603JUJ#PBF & LT8603JUJ3TRPBF to the order table.	2
		Added LT8603EUJ#WPBF/TRPBF and LT8603JUJ#WPBF/WTRPBF to the order table.	2
		Added statements regarding #W under order table.	2
		Added switching frequency specs for E, I- and J-Grade on EC table.	3
		Updated Feedback voltage FB1 for E-, I- and J-Grade on EC table.	3
		Updated Feedback voltage FB2 for E-, I- and J-Grade on EC table.	4
		Updated Feedback voltage FB3 for E-, I- and J-Grade on EC table.	4
		Updated Feedback voltage FB4 for E-, I- and J-Grade on EC table.	5
		Edit and add additional information for current comparator input common mode range conditions for W-, I- and J-Grade.	5
		Added LT8603J grade temperature statement to Note 2 under EC table.	2
		Replaced FB_{ref} with V_{FB} in R1 equation.	26
		Replaced V_{IN} with PV_{IN}.	26
		Added X8R information under Applications Information.	28
		Corrected di/dt typo.	30
		Added title for Figure 13 and Figure and second curve for thermal derating for J-Grade.	31
		Removed http info link.	36
B	04/20	Add LT8603IUJ#WPBF to the order information.	2

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RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT8602	42V, Quad Output (2.5A+1.5A+1.5A+1.5A) 95% Efficiency, 2.2MHz Synchronous Micropower Step-Down DC/DC Converter with I_Q = 25µA	V_{IN} = 3V to 42V, $V_{OUT(MIN)}$= 0.8V, I_Q = 25µA, I_{SD} < 1µA, 6mm × 6mm QFN-40 Package
LT8601	42V, 94% Efficiency, 2.2MHz Triple Output (1.5A+2.5A+1.8A) Synchronous Micropower Step-Down DC/DC Converter with I_Q = 30µA	V_{IN} = 3V to 42V, $V_{OUT(MIN)}$= 0.8V, I_Q = 30µA, I_{SD} < 1µA, 6mm × 6mm QFN-40 Package
LT8640	42V, 5A/7A Peak, 96% Efficiency, 3MHz Synchronous Micropower Step-Down DC/DC Converter with I_Q = 2.5µA	V_{IN} = 3.4V to 42V, $V_{OUT(MIN)}$ = 0.97V, I_Q = 2.5µA, I_{SD} < 1µA, 3mm × 4mm QFN-18 Package
LT8614	42V, 4A, 96% Efficiency, 2.2MHz Synchronous Micropower Step-Down DC/DC Converter with I_Q = 2.5µA	V_{IN} = 3.4V to 42V, $V_{OUT(MIN)}$ = 0.97V, I_Q = 2.5µA, I_{SD} < 1µA, 3mm × 4mm QFN-18 Package
LT8616	42V, Dual 2.5A + 1.5A, 95% Efficiency, 2.2MHz Synchronous Micropower Step-Down DC/DC Converter with I_Q = 5µA	V_{IN} = 3.4V to 42V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 5µA, I_{SD} < 1µA, TSSOP-28E, 3mm × 6mm QFN-28 Packages
LT8612	42V, 6A, 96% Efficiency, 2.2MHz Synchronous Micropower Step-Down DC/DC Converter with I_Q = 2.5µA	V_{IN} = 3.4V to 42V, $V_{OUT(MIN)}$ = 0.97V, I_Q = 3.0µA, I_{SD} < 1µA, 3mm × 6mm QFN-28 Package
LT8609/LT8609A	42V, 2A/3A Peak, 93% Efficiency, 2.2MHz Synchronous Micropower Step-Down DC/DC Converter with I_Q = 2.5µA	V_{IN} = 3.2V to 42V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 2.5µA, I_{SD} < 1µA, MSOP-10E Package
LT8610	42V, 2.5A, 96% Efficiency, 2.2MHz Synchronous Micropower Step-Down DC/DC Converter with I_Q = 2.5µA	V_{IN} = 3.4V to 42V, $V_{OUT(MIN)}$ = 0.97V, I_Q = 2.5µA, I_{SD} < 1µA, MSOP-16E Package
LT8611	42V, 2.5A, 96% Efficiency, 2.2MHz Synchronous Micropower Step-Down DC/DC Converter with I_Q = 2.5µA and Input/Output Current Limit/Monitor	V_{IN} = 3.4V to 42V, $V_{OUT(MIN)}$ = 0.97V, I_Q = 2.5µA, I_{SD} < 1µA, 3mm × 5mm QFN-24 Package
LT8610A/8610AB	42V, 3.5A, 96% Efficiency, 2.2MHz Synchronous Micropower Step-Down DC/DC Converter with I_Q = 2.5µA	V_{IN} = 3.4V to 42V, $V_{OUT(MIN)}$ = 0.97V, I_Q = 2.5µA, I_{SD} < 1µA, MSOP-16E Package
LT8610AC	42V, 3.5A, 96% Efficiency, 2.2MHz Synchronous Micropower Step-Down DC/DC Converter with I_Q = 2.5µA	V_{IN} = 3V to 42V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 2.5µA, I_{SD} < 1µA, MSOP-16E Package

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